UltraScale and UltraScale+ FPGAs Packaging and Pinouts

Product Specification

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Chapter 1

Packaging Overview

Introduction to the UltraScale Architecture

The AMD UltraScale™ architecture is the first ASIC-class architecture to enable multi-hundred gigabit-per-second levels of system performance with smart processing, while efficiently routing and processing data on-chip. UltraScale architecture-based devices address a vast spectrum of high-bandwidth, high-utilization system requirements by using industry-leading technical innovations, including next-generation routing, ASIC-like clocking, 3D-on-3D ICs, multiprocessor SoC (MPSoC) technologies, and new power reduction features. The devices share many building blocks, providing scalability across process nodes and product families to leverage system-level investment across platforms.

AMD Spartan™ UltraScale+™ devices provide high I/O to logic ratio, integrated memory controllers, and advanced I/O that help industrial, vision and healthcare (IVH), audio, video and broadcast (AVB), automotive, and other FPGA application developers looking to build cost-optimized solutions. Available in a wide array of packaging options, this family delivers a balance of cost, power, performance, and size.

AMD Artix™ UltraScale+ devices provide high serial bandwidth and signal compute density in a cost-optimized device for critical networking applications, vision and video processing, and secured connectivity. Coupled with the innovative InFO packaging, which provides excellent thermal and power distribution, Artix UltraScale+ devices are perfectly suited to applications requiring high compute density in a small footprint.

AMD Kintex™ UltraScale+ devices provide the best price/performance/watt balance in a 16 nm FinFET node, delivering the most cost-effective solution for high-end capabilities, including transceiver and memory interface line rates as well as 100G connectivity cores. Our newest mid-range family is ideal for both packet processing and DSP-intensive functions and is well suited for applications including wireless MIMO technology, Nx100G networking, and data center.

AMD Kintex UltraScale devices provide the best price/performance/watt at 20 nm and include the highest signal processing bandwidth in a mid-range device, next-generation transceivers, and low-cost packaging for an optimum blend of capability and cost-effectiveness. The family is ideal for packet processing in 100G networking and data centers applications as well as DSP-intensive processing needed in next-generation medical imaging, 8k4k video, and heterogeneous wireless infrastructure.

AMD Virtex™ UltraScale+ devices provide the highest performance and integration capabilities in a FinFET node, including both the highest serial I/O and signal processing bandwidth, as well as the highest on-chip memory density. As the industry's most capable FPGA family, the Virtex UltraScale+ devices are ideal for applications including 1+Tb/s networking and data center and fully integrated radar/early-warning systems.

AMD Virtex UltraScale devices provide the greatest performance and integration at 20 nm, including serial I/O bandwidth and logic capacity. As the industry's only high-end FPGA at the 20 nm process node, this family is ideal for applications including 400G networking, large scale ASIC prototyping, and emulation.

AMD Zynq™ UltraScale+ devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing. Integrating an Arm®-based system for advanced analytics and on-chip programmable logic for task acceleration creates unlimited possibilities for applications including 5G Wireless, next generation ADAS, and Industrial Internet-of-Things.

This packaging and pinout specification user guide is part of the UltraScale Architecture documentation suite available at: docs.amd.com.

Introduction to UltraScale and UltraScale+ FPGAs Packaging and Pinouts

This section describes the packages and pinouts for the UltraScale architecture-based FPGAs in various organic flip-chip 0.5 mm, 0.8 mm, 0.92 mm, and 1.0 mm pitch BGA packages.

- Kintex UltraScale, Kintex UltraScale+, Artix UltraScale+, and Spartan UltraScale+ devices are offered in low-cost, space-saving flip-chip and bare-die flip-chip packages that are optimally designed for high performance-to-price ratio.
- Virtex UltraScale and Virtex UltraScale+ devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for highest system capacity, bandwidth and signal performance. Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of power and GND pins.
- Zynq UltraScale+ MPSoCs are further described in the *Zynq UltraScale+ MPSoC Packaging and Pinouts User Guide* (UG1075).

IMPORTANT: *Many of the standard packages for commercial (XC) devices are lead-free (signified by an additional V in the package name). All of the UltraScale or UltraScale+ devices supported in a particular package are footprint compatible. Each device is split into I/O banks to allow for flexibility in the choice of I/O standards. See the UltraScale Architecture SelectIO Resources User Guide (UG571).*

UltraScale and UltraScale+ device's flip-chip assembly materials are manufactured using ultra-low alpha (ULA) materials defined as <0.002 cph/cm^2 or materials that emit less than 0.002 alpha-particles per square centimeter per hour.

Differences from Previous Generations

The packaging and pinout specifications for UltraScale architecture-based FPGAs differ from past generations, including the 7 series devices. These details are outlined in this section.

- All packages are constructed on organic laminate substrates.
- Many of the package and die components, including flip-chip solder bumps, are lead-free. The FLGx devices have lead in their bumps.
- Package names contain a single-character alphabetic designator followed by the exact number of pins found on the package.
- VCCAUX_IO pins are not divided into bank groups. VCCAUX_IO must be connected to VCCAUX at the board level.
- Internal logic is separated from I/O logic by the addition of the VCCINT_IO power pins. VCCINT_IO must be connected to VCCINT at the board level.
- Groups of gigabit serial transceiver (GT) power pins are separated by column for each column of GT Quads/Duals.
- Standard I/O banks each have a total of 52 SelectIO™ pins, optionally configurable as up to 24 differential pairs.
- Each bank has one dedicated VREF pin. These pins cannot be used as user I/Os.
- Four differential clock pin pairs per bank (two per 26-pin bank) consist of a single type of global clock (GC) input.
- Four memory byte groups per I/O bank (two per 26-pin bank) are each separated into an upper and a lower memory byte group.
- All configuration pins are located in bank 0 and bank 65.
- A POR_OVERRIDE pin is used to override the default power-on-reset delay. See Table 1-6.

Device/Package Combinations

Table 1-1 shows the size and BGA pitch of the UltraScale and UltraScale+ device packages. The devices with stacked-silicon interconnect (SSI) technology are labeled.

IMPORTANT: *All packages with BGA ball pitch 0.8 mm, 0.92 mm, or 1.0 mm packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC, and the third digit in the package name is Q (for example: FFQA1156).*

Table 1-1: **Package Specifications**

Packages[1]	Description	Package Specifications		
		Package Type	Pitch (mm)	Size (mm)
FCVA289	Flip-chip, chip scale	BGA	0.5	9 x 9
CMVA361	Flip-chip, chip scale		0.5	10 x 10
UBVA368	Bare-die, flip-chip, integrated fan out (InFO)		0.5	11.5 x 9.5
SBVB484	Bare-die, flip-chip, super-fine-pitch		0.8	19 x 19
SBVC484				
CMVA529	Flip-chip, chip scale		0.5	12 x 12
SBVB625	Bare-die, flip-chip, super-fine-pitch		0.8	21 x 21
FBVA676	Bare-die, flip-chip, fine-pitch		1.0	27 x 27
FFVA676	Flip-chip, fine-pitch			
FFVB676				
FFRB676	Ruggedized, flip-chip, fine-pitch			
RBA676				
SFVA784	Flip-chip, super-fine-pitch		0.8	23 x 23
SFVB784				
SFRB784	Ruggedized, flip-chip, super-fine pitch			
FBVA900	Bare-die, flip-chip, fine-pitch		1.0	31 x 31
FFVD900	Flip-chip, fine-pitch			
FFVE900				
FFVA1156	Flip-chip, fine-pitch			35 x 35
FFRA1156	Ruggedized, flip-chip, fine-pitch			
RFA1156				
VSVA1365	Flip-chip, fine-pitch lidless with stiffener ring		0.92	

Table 1-1: **Package Specifications *(Cont'd)***

Packages[1]	Description	Package Specifications		
		Package Type	Pitch (mm)	Size (mm)
FFVA1517	Flip-chip, fine-pitch	BGA	1.0	40 x 40
FFVC1517				
FFVD1517				
FFVE1517				
FFRC1517	Ruggedized, flip-chip, fine-pitch			
FFRE1517				
RLD1517	Ruggedized, SSI, flip-chip, fine-pitch			
FLVA1517	SSI, flip-chip, fine-pitch			
FLVD1517				
FFVA1760	Flip-chip, fine-pitch		1.0	42.5 x 42.5
FFVB1760				
FFVE1760				
FFVJ1760				
FLVB1760	SSI, flip-chip, fine-pitch			
FSVJ1760	SSI, flip-chip, fine-pitch, lidless with stiffener ring			
FLGF1924	SSI, flip-chip, fine-pitch			45 x 45
FLVD1924				
FLVF1924				
FSVH1924	SSI, flip-chip, fine-pitch, lidless with stiffener ring			
RLF1924	Ruggedized, SSI, flip-chip, fine-pitch			
FFVA2104	Flip-chip, fine-pitch			47.5 x 47.5
FFVB2104				
FFVC2104				
FLVA2104	SSI, flip-chip, fine-pitch			
FLVB2104				
FLVC2104				
FLGA2104	SSI, flip-chip, fine-pitch, RoHS 6/6 with exemption 15			47.5 x 47.5
FLGB2104				
FLGC2104				
FLRA2104	Ruggedized, SSI, flip-chip, fine-pitch			47.5 x 47.5
FLRB2104				
FLRC2104				

Table 1-1: **Package Specifications *(Cont'd)***

Packages(1)	Description	Package Specifications		
		Package Type	Pitch (mm)	Size (mm)
FSGD2104	SSI, flip-chip, fine-pitch, lidless with stiffener ring, RoHS 6/6 with exemption 15	BGA	1.0	47.5 x 47.5
FSVH2104	SSI, flip-chip, fine-pitch, lidless with stiffener ring			47.5 x 47.5
FHGA2104(2)	SSI, flip-chip, fine-pitch, overhang, RoHS 6/6 with exemption 15			52.5 x 52.5
FHGB2104(2)				
FHGC2104(2)				
FIGD2104(2)	SSI, flip-chip, fine-pitch, overhang, lidless with stiffener ring, RoHS 6/6 with exemption 15			52.5 x 52.5
FLGB2377	SSI, flip-chip, fine-pitch, RoHS 6/6 with exemption 15			50 x 50
FLGA2577	SSI, flip-chip, fine-pitch, RoHS 6/6 with exemption 15			52.5 x 52.5
FSGA2577	SSI, flip-chip, fine-pitch, lidless with stiffener ring, RoHS 6/6 with exemption 15			52.5 x 52.5
FLGA2892	SSI, flip-chip, fine-pitch, RoHS 6/6 with exemption 15			55 x 55
FSVH2892	SSI, flip-chip, fine-pitch, lidless with stiffener ring			55 x 55
FSVK2892				55 x 55
FSVA3824	SSI, flip-chip, fine-pitch, lidless with stiffener ring			65 x 65
FSVB3824	SSI, flip-chip, fine-pitch, lidless with stiffener ring			65 x 65

Notes:

1. FFV, FLV, and FLG packages are footprint compatible when the package code letter designator and pin count are identical. See the *UltraScale Architecture and Product Overview* (DS890) for specific letter codes and ordering code information.
2. These 52.5 x 52.5 packages have the same PCB ball footprint as the 47.5 x 47.5 packages and are footprint compatible.

Gigabit Transceiver Channels by Device/Package

Table 1-2 lists the quantity of gigabit transceiver channels for the UltraScale and UltraScale+ devices. In all devices, a gigabit transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins. For transceiver data rate limitations on specific device/package combinations, see UltraScale Device Data Sheets.

Table 1-2: **Serial Transceiver Channels (GTH/GTY) by Device/Package**

Device	Package	GTH Channels	GTY Channels
Kintex UltraScale Devices			
XCKU035	FBVA676	16	0
XCKU040		16	0
XCKU035	SFVA784	8	0
XCKU040		8	0

Table 1-2: **Serial Transceiver Channels (GTH/GTY) by Device/Package *(Cont'd)***

Device	Package	GTH Channels	GTY Channels
XCKU035	FBVA900	16	0
XCKU040		16	0
XCKU025	FFVA1156	12	0
XCKU035		16	0
XCKU040		20	0
XCKU060		28	0
XCKU095		20	8
XCKU060	FFVA1517	32	0
XCKU085	FLVA1517	48	0
XCKU115		48	0
XCKU095	FFVC1517	20	20
XCKU115	FLVD1517	64	0
XCKU095	FFVB1760	32	16
XCKU085	FLVB1760	44	0
XCKU115		52	0
XCKU115	FLVD1924	52	0
XCKU085	FLVF1924	56	0
XCKU115		64	0
XCKU115	FLVA2104	52	0
XCKU095	FFVB2104	32	32
XCKU115	FLVB2104	64	0
XQKU040	RBA676	16	0
XQKU040	RFA1156	20	0
XQKU060		28	0
XQKU095		20	0
XQKU115	RLD1517	64	0
XQKU115	RLF1924	64	0
Virtex UltraScale Devices			
XCVU065	FFVC1517	20	20
XCVU080		20	20
XCVU095		20	20
XCVU080	FFVD1517	32	32
XCVU095		32	32
XCVU125	FLVD1517	40	32

Table 1-2: **Serial Transceiver Channels (GTH/GTY) by Device/Package *(Cont'd)***

Device	Package	GTH Channels	GTY Channels
XCVU080	FFVB1760	32	16
XCVU095		32	16
XCVU125	FLVB1760	36	16
XCVU080	FFVA2104	28	24
XCVU095		28	24
XCVU125	FLVA2104	28	24
XCVU080	FFVB2104	32	32
XCVU095		32	32
XCVU125	FLVB2104	40	36
XCVU160	FLGB2104	40	36
XCVU190		40	36
XCVU095	FFVC2104	32	32
XCVU125	FLVC2104	40	40
XCVU160	FLGC2104	52	52
XCVU190		52	52
XCVU440	FLGB2377	36	0
XCVU190	FLGA2577	60	60
XCVU440	FLGA2892	48	0
Artix UltraScale+ Devices			
XCAU7P	FCVA289	4	0
XAAU7P		4	0
XCAU7P	SBVC484	4	0
XAAU7P		4	0
XCAU10P	UBVA368	8	0
XCAU15P		8	0
XCAU10P	SBVB484	12	0
XAAU10P		12	0
XCAU15P		12	0
XAAU15P		12	0
XCAU10P	FFVB676	12	0
XAAU10P		12	0
XCAU15P		12	0
XAAU15P		12	0
XCAU20P		0	12
XCAU25P		0	12

Table 1-2: **Serial Transceiver Channels (GTH/GTY) by Device/Package *(Cont'd)***

Device	Package	GTH Channels	GTY Channels
XCAU20P	SFVB784	0	12
XCAU25P		0	12
Kintex UltraScale+ Devices			
XCKU3P	FFVA676	0	16
XCKU5P		0	16
XCKU3P	FFVB676	0	16
XCKU5P		0	16
XCKU3P	SFVB784	0	16
XCKU5P		0	16
XCKU3P	FFVD900	0	16
XCKU5P		0	16
XCKU11P		16	0
XCKU9P	FFVE900	28	0
XCKU13P		28	0
XCKU11P	FFVA1156	20	8
XCKU15P		20	8
XCKU11P	FFVE1517	32	20
XCKU15P		32	24
XCKU15P	FFVA1760	44	32
XCKU15P	FFVE1760	32	24
XCKU19P	FFVJ1760	0	32
XCKU19P	FFVB2104	0	32
XQKU5P	FFRB676	0	16
XQKU5P	SFRB784	0	16
XQKU15P	FFRA1156	20	8
XQKU15P	FFRE1517	32	24
Virtex UltraScale+ Devices			
XCVU3P	FFVC1517	0	40
XCVU11P	FLGF1924	0	64
XCVU31P	FSVH1924	0	32

Table 1-2: **Serial Transceiver Channels (GTH/GTY) by Device/Package *(Cont'd)***

Device	Package	GTH Channels	GTY Channels
XCVU5P	FLVA2104	0	52
XCVU7P		0	52
XCVU9P	FLGA2104	0	52
XCVU13P	FHGA2104	0	52
XCVU5P	FLVB2104	0	76
XCVU7P		0	76
XCVU9P	FLGB2104	0	76
XCVU11P		0	76
XCVU13P	FHGB2104	0	76
XCVU5P	FLVC2104	0	80
XCVU7P		0	80
XCVU9P	FLGC2104	0	104
XCVU11P		0	96
XCVU13P	FHGC2104	0	104
XCVU9P	FSGD2104	0	76
XCVU11P		0	76
XCVU13P	FIGD2104	0	76
XCVU33P	FSVH2104	0	32
XCVU35P		0	64
XCVU45P		0	64
XCVU9P	FLGA2577	0	120
XCVU11P		0	96
XCVU13P		0	128
XCVU13P	FSGA2577	0	128
XCVU35P	FSVH2892	0	64
XCVU37P		0	96
XCVU45P		0	64
XCVU47P		0	96
XCVU19P	FSVA3824	0	48
XCVU19P	FSVB3824	0	80
XQVU3P	FFRC1517	0	40
XQVU7P	FLRA2104	0	52
XQVU7P	FLRB2104	0	76
XQVU11P	FLRC2104	0	96

Table 1-3: **Serial Transceiver Channels (GTH/GTY/GTM) by Device/Package**

Device	Package	GTH Channels	GTY Channels	GTM Channels
Virtex UltraScale+ Devices				
XCVU23P	VSVA1365	0	34	4
XCVU23P	FSVJ1760	0	34	4
XCVU27P	FIGD2104	0	16	30
XCVU29P		0	16	30
XCVU27P	FSGA2577	0	32	48
XCVU29P		0	32	48
XCVU57P	FSVK2892	0	32	32

Table 1-4: **Serial Transceiver Channels (GTH) by Device/Package**

Device	Package	GTH Channels
Spartan UltraScale+ Devices		
XCSU10P	CMVA361	0
	CMVA529	0
	SBVB625	0
XCSU25P	CMVA361	0
	CMVA529	0
	SBVB625	0
XCSU35P	CMVA361	0
	CMVA529	0
	SBVB625	0

User I/O Pins by Device/Package

Table 1-5 lists the number of available 3.3V-capable high-range (HR), 3.3V-capable high-density (HD), and 1.8V-capable high-performance (HP) I/Os and the number of differential I/O pairs for each UltraScale and UltraScale+ device/package combination.

IMPORTANT: *Because of package inductance, each device/package supports a limited number of simultaneous switching outputs. Limitations for specific applications can be determined using the AMD Vivado™ Design Suite report_ssn tool. See the Simultaneous Switching Outputs section of the UltraScale Architecture SelectIO Resources User Guide (UG571) for more information.*

Table 1-5: **Available I/O Pins by Device/Package**

Device	Package	Total User I/O			Differential I/O		
		HD(1)	HR(1)	HP(1)	HD	HR	HP
Kintex UltraScale Devices							
XCKU035	FBVA676	0	104	208	0	96	192
XCKU040		0	104	208	0	96	192
XCKU035	SFVA784	0	104	364	0	96	336
XCKU040		0	104	364	0	96	336
XCKU035	FBVA900	0	104	364	0	96	336
XCKU040		0	104	364	0	96	336
XCKU025	FFVA1156	0	104	208	0	96	192
XCKU035		0	104	416	0	96	384
XCKU040		0	104	416	0	96	384
XCKU060		0	104	416	0	96	384
XCKU095		0	52	468	0	48	432
XCKU060	FFVA1517	0	104	520	0	96	480
XCKU085	FLVA1517	0	104	520	0	96	480
XCKU115		0	104	520	0	96	480
XCKU095	FFVC1517	0	52	468	0	48	432
XCKU115	FLVD1517	0	104	234	0	96	216
XCKU095	FFVB1760	0	52	650	0	48	600
XCKU085	FLVB1760	0	104	572	0	96	528
XCKU115		0	104	650	0	96	600
XCKU115	FLVA2104	0	156	676	0	144	624
XCKU095	FFVB2104	0	52	650	0	48	600
XCKU115	FLVB2104	0	104	650	0	96	600
XCKU115	FLVD1924	0	156	676	0	144	624

Table 1-5: **Available I/O Pins by Device/Package *(Cont'd)***

Device	Package	Total User I/O			Differential I/O		
		HD[(1)]	HR[(1)]	HP[(1)]	HD	HR	HP
XCKU085	FLVF1924	0	104	520	0	96	480
XCKU115		0	104	624	0	96	576
XQKU040	RBA676	0	104	208	0	96	192
XQKU040	RFA1156	0	104	416	0	96	384
XQKU060		0	104	416	0	96	384
XQKU095		0	52	468	0	48	432
XQKU115	RLD1517	0	104	234	0	96	216
XQKU115	RLF1924	0	104	624	0	96	576
Virtex UltraScale Devices							
XCVU065	FFVC1517	0	52	468	0	48	432
XCVU080		0	52	468	0	48	432
XCVU095		0	52	468	0	48	432
XCVU080	FFVD1517	0	52	286	0	48	264
XCVU095		0	52	286	0	48	264
XCVU125	FLVD1517	0	52	286	0	48	264
XCVU080	FFVB1760	0	52	650	0	48	600
XCVU095		0	52	650	0	48	600
XCVU125	FLVB1760	0	52	650	0	48	600
XCVU080	FFVA2104	0	52	780	0	48	720
XCVU095		0	52	780	0	48	720
XCVU125	FLVA2104	0	52	780	0	48	720
XCVU080	FFVB2104	0	52	650	0	48	600
XCVU095		0	52	650	0	48	600
XCVU125	FLVB2104	0	52	650	0	48	600
XCVU160	FLGB2104	0	52	650	0	48	600
XCVU190		0	52	650	0	48	600
XCVU095	FFVC2104	0	52	364	0	48	336
XCVU125	FLVC2104	0	52	364	0	48	336
XCVU160	FLGC2104	0	52	364	0	48	336
XCVU190		0	52	364	0	48	336
XCVU440	FLGB2377	0	52	1248	0	48	1152
XCVU190	FLGA2577	0	0	448	0	0	412
XCVU440	FLGA2892	0	52	1404	0	48	1296

Table 1-5: **Available I/O Pins by Device/Package *(Cont'd)***

Device	Package	Total User I/O			Differential I/O		
		HD[(1)]	HR[(1)]	HP[(1)]	HD	HR	HP
Artix UltraScale+ Devices							
XCAU7P	FCVA289	72	0	58	72	0	54
XAAU7P		72	0	58	72	0	54
XCAU7P	SBVC484	144	0	104	144	0	96
XAAU7P		144	0	104	144	0	96
XCAU10P	UBVA368	24	0	104	24	0	96
XCAU15P		24	0	104	24	0	96
XCAU10P	SBVB484	48	0	156	48	0	144
XAAU10P		48	0	156	48	0	144
XCAU15P		48	0	156	48	0	144
XAAU15P		48	0	156	48	0	144
XCAU10P	FFVB676	72	0	156	72	0	144
XAAU10P		72	0	156	72	0	144
XCAU15P		72	0	156	72	0	144
XAAU15P		72	0	156	72	0	144
XCAU20P		72	0	156	72	0	144
XCAU25P		72	0	208	72	0	192
XCAU20P	SFVB784	72	0	156	72	0	144
XCAU25P		96	0	208	96	0	192
Kintex UltraScale+ Devices							
XCKU3P	FFVA676	48	0	208	48	0	192
XCKU5P		48	0	208	48	0	192
XCKU3P	FFVB676	72	0	208	72	0	192
XCKU5P		72	0	208	72	0	192
XCKU3P	SFVB784	96	0	208	96	0	192
XCKU5P		96	0	208	96	0	192
XCKU3P	FFVD900	96	0	208	96	0	192
XCKU5P		96	0	208	96	0	192
XCKU11P		96	0	312	96	0	288
XCKU9P	FFVE900	96	0	208	96	0	192
XCKU13P		96	0	208	96	0	192
XCKU11P	FFVA1156	48	0	416	48	0	384
XCKU15P		48	0	468	48	0	432

Table 1-5: **Available I/O Pins by Device/Package *(Cont'd)***

Device	Package	Total User I/O			Differential I/O		
		HD[(1)]	HR[(1)]	HP[(1)]	HD	HR	HP
XCKU11P	FFVE1517	96	0	416	96	0	384
XCKU15P		96	0	416	96	0	384
XCKU15P	FFVA1760	96	0	416	96	0	384
XCKU15P	FFVE1760	96	0	572	96	0	528
XCKU19P	FFVJ1760	72	0	468	72	0	432
XCKU19P	FFVB2104	72	0	468	72	0	432
XQKU5P	FFRB676	72	0	208	72	0	192
XQKU5P	SFRB784	96	0	208	96	0	192
XQKU15P	FFRA1156	48	0	468	48	0	432
XQKU15P	FFRE1517	96	0	416	96	0	384
Virtex UltraScale+ Devices							
XCVU3P	FFVC1517	0	0	520	0	0	480
XCVU23P	VSVA1365	0	0	364	0	0	336
XCVU23P	FSVJ1760	72	0	572	72	0	528
XCVU11P	FLGF1924	0	0	624	0	0	576
XCVU31P	FSVH1924	0	0	208	0	0	192
XCVU5P	FLVA2104	0	0	832	0	0	768
XCVU7P		0	0	832	0	0	768
XCVU9P	FLGA2104	0	0	832	0	0	768
XCVU13P	FHGA2104	0	0	832	0	0	768
XCVU5P	FLVB2104	0	0	702	0	0	648
XCVU7P		0	0	702	0	0	648
XCVU9P	FLGB2104	0	0	702	0	0	648
XCVU11P		0	0	572	0	0	528
XCVU13P	FHGB2104	0	0	702	0	0	648
XCVU5P	FLVC2104	0	0	416	0	0	384
XCVU7P		0	0	416	0	0	384
XCVU9P	FLGC2104	0	0	416	0	0	384
XCVU11P		0	0	416	0	0	384
XCVU13P	FHGC2104	0	0	416	0	0	384
XCVU9P	FSGD2104	0	0	676	0	0	624
XCVU11P		0	0	572	0	0	528
XCVU13P	FIGD2104	0	0	676	0	0	624

Table 1-5: **Available I/O Pins by Device/Package *(Cont'd)***

Device	Package	Total User I/O			Differential I/O		
		HD[(1)]	HR[(1)]	HP[(1)]	HD	HR	HP
XCVU27P	FIGD2104	0	0	520	0	0	240
XCVU29P		0	0	676	0	0	312
XCVU33P	FSVH2104	0	0	208	0	0	192
XCVU35P		0	0	416	0	0	384
XCVU45P		0	0	416	0	0	384
XCVU9P	FLGA2577	0	0	448	0	0	414
XCVU11P		0	0	448	0	0	414
XCVU13P		0	0	448	0	0	414
XCVU13P	FSGA2577	0	0	448	0	0	414
XCVU27P	FSGA2577	0	0	292	0	0	134
XCVU29P		0	0	448	0	0	206
XCVU35P	FSVH2892	0	0	416	0	0	384
XCVU37P		0	0	624	0	0	576
XCVU45P		0	0	416	0	0	384
XCVU47P		0	0	624	0	0	576
XCVU57P	FSVK2892	0	0	624	0	0	576
XCVU19P	FSVA3824	0	0	1976	0	0	1824
	FSVB3824	1	1	1664	0	0	1536
XQVU3P	FFRC1517	0	0	520	0	0	480
XQVU7P	FLRA2104	0	0	832	0	0	768
XQVU7P	FLRB2104	0	0	702	0	0	648
XQVU11P	FLRC2104	0	0	416	0	0	384
Spartan UltraScale+ Devices							
XCSU10P	CMVA361	168	0	52	168	0	48
	CMVA529	252	0	52	252	0	48
	SBVB625	252	0	52	252	0	48
XCSU25P	CMVA361	168	0	52	168	0	48
	CMVA529	252	0	52	252	0	48
	SBVB625	252	0	52	252	0	48
XCSU35P	CMVA361	168	0	52	168	0	48
	CMVA529	252	0	52	252	0	48
	SBVB625	252	0	52	252	0	48

Notes:
1. The maximum user I/O numbers do not include pins in the configuration bank 0 or the GT serial transceivers.

Pin Definitions

Table 1-6 lists the pin definitions used in UltraScale and UltraScale+ device packages.

Table 1-6: **Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_L[*1 to 24*][P or N]_T[*0 to 3*] [*U or L*]_N[*0 to 12*]_ [multi-function]_[bank number] or IO_T[*0 to 3*][*U or L*]_N[*0 to 12*]_[multi-function]_[bank number]			
	Multi-function	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. Each user I/O pin name consists of several indicator labels, where: • IO indicates a user I/O pin. • L[*1 to 24*] indicates a unique differential pair with P (positive) and N (negative) sides. User I/O pins without the L indicator are single-ended. • T[*0 to 3*][*U or L*] indicates the assigned byte group and nibble location (upper or lower portion) within that group for the pin. • N[*0 to 12*] the number of the I/O within its byte group. • [*multi-function*] indicates any other functions that the pin can provide. If not used for this function, the pin can be a user I/O. • [*bank number*] indicates the assigned bank for the user I/O pin.
GC or HDGC	Multi-function	Input/ Output	Four global clock (GC) pin pairs are in each bank. HDGC pins have direct access to the global clock buffers. GC pins have direct access to the global clock buffers, MMCMs, and PLLs that are in the clock management tile (CMT) adjacent to the same I/O bank. GC and HDGC inputs provide dedicated, high-speed access to the internal global and regional clock resources. GC and HDGC inputs use dedicated routing and must be used for clock inputs where the timing of various clocking features is imperative. GC or HDGC pins can be treated as user I/O when not used as input clocks. Up-to-date information about designing with the GC (or HDGC) pin is available in the *UltraScale Architecture Clocking Resources User Guide* (UG572).
VRP[(1)]	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with a reference resistor).

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
DBC QBC	Multi-function	Input	Byte lane clock (DBC and QBC) input pin pairs are clock inputs directly driving source synchronous clocks to the bit slices in the I/O banks. In memory applications, these are also known as DQS. For more information, consult the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
PERSTN[*0 to 1*]	Multi-function	Input	Default reset pin locations for the integrated block for PCI Express.
User I/O Multi-Function Configuration Pins			
For further descriptions, including configuration modes and recommended external pull-up/pull-down resistors, see the *UltraScale Architecture Configuration User Guide* (UG570).			
EMCCLK	Multi-function	Input	External master configuration clock.
DOUT_CSO_B	Multi-function	Output	Data output for serial daisy-chaining or active-Low chip-select output for SelectMAP daisy-chaining.
D[*04 to 31*]	Multi-function	Bidirectional	Configuration data pins.
A[*00 to 28*]	Multi-function	Output	Address output.
CSI_ADV_B	Multi-function	Input or Output	Active-Low chip-select input or address valid output.
FOE_B	Multi-function	Output	Active-Low flash output enable.
FWE_FCS2_B	Multi-function	Output	Active-Low flash write-enable for BPI flash or flash chip-select for second SPI (x8) flash.
RS[*0 to 1*]	Multi-function	Output	Revision select outputs.

Table 1-6: **Pin Definitions *(Cont'd)***

<table>
<tr><th>Pin Name</th><th>Type</th><th>Direction</th><th>Description</th></tr>
<tr><td colspan="4">Spartan UltraScale+ FPGA User I/O Multi-Function Configuration Pins (Only)</td></tr>
<tr><td colspan="4">For further descriptions, including configuration modes and recommended external pull-up/pull-down resistors, see the Spartan UltraScale+ Architecture Configuration User Guide (UG860).</td></tr>
<tr><td>BUSY</td><td rowspan="9">Multi-function</td><td>Output</td><td>Active-High output that must be connected to the host and monitored.</td></tr>
<tr><td>CSI_B</td><td>Input or Output</td><td>Active-Low input that enables the FPGA SelectMAP configuration interface.</td></tr>
<tr><td>D[04 to 11]_OSPID[00 to 07]</td><td>Input or Bidirectional</td><td rowspan="2">Configuration data pins.</td></tr>
<tr><td>D[12 to 31]</td><td>Input or Output</td></tr>
<tr><td>EMCCLK</td><td>Input</td><td>External master configuration clock.</td></tr>
<tr><td>FCS1_B</td><td>Output</td><td>Active-Low chip select output that enables dual stacked flash devices for post-configuration access.</td></tr>
<tr><td>OSPI_DS</td><td>Input</td><td>Data strobe used in OSPI mode for DDR mode.</td></tr>
<tr><td>OSPI_ECC_FAIL</td><td>Input</td><td>ECC failure input status available from select OSPI flash devices.</td></tr>
<tr><td>OSPI_RST_B</td><td>Output</td><td>Reset (active Low) signal used in OSPI mode to reset the OSPI flash device.</td></tr>
<tr><td colspan="4">Dedicated (Bank 0) Configuration Pins[(2)]</td></tr>
<tr><td colspan="4">For more information see the UltraScale Architecture Configuration User Guide (UG570).</td></tr>
<tr><td>M[0 to 2]_0</td><td>Dedicated</td><td>Input</td><td>Configuration mode selection.</td></tr>
<tr><td>INIT_B_0</td><td>Dedicated</td><td>Bidirectional (open-drain)</td><td>Active-Low initialization</td></tr>
<tr><td>CFGBVS_0</td><td>Dedicated</td><td>Input</td><td>Bank 0 and bank 65 voltage select. This pin determines the I/O voltage operating range and voltage tolerance for the dedicated configuration bank 0 and multi-function bank 65. Connect CFGBVS High or Low per the bank voltage requirements.
• V_{CCO_0} = 2.5V or 3.3V, tie CFGBVS High (connect to V_{CCO_0}).
• V_{CCO_0} = 1.5V or 1.8V, tie CFGBVS Low (connect to GND)
CAUTION! To avoid device damage, this pin must be connected correctly to either V_{CCO_0} or GND.</td></tr>
<tr><td>PUDC_B_0</td><td>Dedicated</td><td>Input</td><td>Active-Low input enables internal pull-ups during configuration on all SelectIO pins:
0 = Weak preconfiguration I/O pull-up resistors enabled.
1 = Weak preconfiguration I/O pull-up resistors disabled.</td></tr>
</table>

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
POR_OVERRIDE	Dedicated	Input	All configuration modes Power-on reset delay override. **CAUTION!** *Do not allow this pin to float before and during configuration. This pin must be tied to V_{CCINT} or GND. Do not connect to V_{CCO_0}.* Information about designing with the POR_OVERRIDE pin is available in the *UltraScale Architecture Configuration User Guide* (UG570).
DONE_0	Dedicated	Bidirectional	Active-High, DONE indicates successful completion of configuration.
PROGRAM_B_0	Dedicated	Input	Active Low, asynchronous reset to configuration logic.
TDO_0	Dedicated	Output	JTAG test data output.
TDI_0	Dedicated	Input	JTAG test data input.
RDWR_FCS_B_0	Dedicated	Input/ Output	Input control signal for SelectMAP data bus direction: High for reading or Low for writing configuration data. Or, active-Low flash chip-select output.
TMS_0	Dedicated	Input	JTAG test mode data select.
TCK_0	Dedicated	Input	JTAG test clock
CCLK_0	Dedicated	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
D00_MOSI_0	Dedicated	Bidirectional	Data Bit 0 or SPI master-output
D01_DIN_0	Dedicated	Bidirectional	Data Bit 1 or serial mode data input
D02_0	Dedicated	Bidirectional	Data Bit 2
D03_0	Dedicated	Bidirectional	Data Bit 3
Other Dedicated Pins			
DXN	Dedicated	N/A	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines.
DXP			

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
Spartan UltraScale+ FPGA Dedicated (Bank 0) Configuration Pins			
M[0 to 2]_0	Dedicated	Input	Configuration mode selection.
INIT_B_0	Dedicated	Bidirectional (open drain)	Active-Low initialization.
PUDC_B_0	Dedicated	Input	Active-Low input enables internal pull-ups during configuration on all SelectIO pins: 0 = Weak preconfiguration I/O pull-up resistors enabled. 1 = Weak preconfiguration I/O pull-up resistors disabled.
POR_OVERRIDE	Dedicated	Input	All configuration modes Power-on reset delay override. **CAUTION!** *Do not allow this pin to float before and during configuration. This pin must be tied to VCCINT or GND. Do not connect to VCCO_0.* Information about designing with the POR_OVERRIDE pin is available in the *Spartan UltraScale+ Architecture Configuration User Guide* (UG860).
DONE_0	Dedicated	Bidirectional	Active High, DONE indicates successful completion of configuration.
PROGRAM_B_0	Dedicated	Input	Active Low, asynchronous reset to configuration logic.
TDO_0	Dedicated	Output	JTAG test data output.
RDWR_FCS_B_0	Dedicated	Input/ Output	Input control signal for SelectMAP data bus direction: High for reading or Low for writing configuration data. Or, active-Low flash chip-select output.
TMS_0	Dedicated	Input	JTAG test mode data select.
TCK_0	Dedicated	Input	JTAG test clock.
CCLK_0	Dedicated	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
D00_MOSI_DOUT_0	Dedicated	Bidirectional	Data bit 0, SPI master-output, or data output for serial configuration daisy-chain.
D01_DIN_0	Dedicated	Bidirectional	Data bit 1 or serial mode data input.
D02_CS_B_0	Dedicated	Bidirectional	Data bit 2 or active-Low chip select input that enables the slave serial interface.
D03_READY_0	Dedicated	Bidirectional	Data bit 3 or open-drain output that must be connected to the host and monitored.

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
System Monitor Pins[(3)]			
AD[0 to 15][P or N]	Multi-function	Input	System Monitor differential auxiliary analog inputs 0–15.
VCCADC	Dedicated	N/A	System Monitor analog positive supply voltage.
GNDADC	Dedicated	N/A	System Monitor analog ground reference.
VREFP	Dedicated	N/A	Voltage reference input.
VREFN	Dedicated	N/A	Voltage reference GND.
VP	Dedicated	Input	System Monitor dedicated differential analog input (positive side).
VN	Dedicated	Input	System Monitor dedicated differential analog input (negative side).
I2C_SCLK	Multi-function	Bidirectional	I2C serial clock. Directly connected to the System Monitor DRP interface for I2C operation configuration. **IMPORTANT:** *Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.*
I2C_SDA	Multi-function	Bidirectional	I2C serial data line. Directly connected to the System Monitor DRP interface for I2C operation configuration. **IMPORTANT:** *Because the SYSMON I2C interface is active after power-on, this pin should only be used for I2C access until after configuration.*
SMBALERT	Multi-function	Bidirectional	Optional PMBus alert, interrupt signal. When Low, indicates a system fault that must be cleared using PMBus commands. Connect to SMBALERT_TS. For more information, see the *UltraScale Architecture System Monitor User Guide* (UG580). **IMPORTANT:** *By default, the PMBus is active prior to configuration. Only use as a multi-functional I/O pin in designs that can tolerated this pin being driven prior to configuration.* This pin is present on UltraScale+ devices.

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
Power/Ground Pins			
For more information on voltage specifications see the UltraScale Device Data Sheets.			
GND	Dedicated	N/A	Ground.
VCCINT	Dedicated	N/A	Power-supply pins for the internal logic.
VCCINT_IO	Dedicated	N/A	Power-supply pins for the I/O banks. For Kintex and *UltraScale Architecture PCB and Pin Planning User Guide* devices, connect VCCINT_IO to VCCINT. For Kintex and Virtex UltraScale+ devices, connect VCCINT_IO to VCCBRAM. Both migration and lower voltage differences (-1LI and -2LE at 0.72V) are discussed in the *UltraScale Architecture PCB Design Guide* (UG583). See the connection matrix in the *Power Supply Voltage Levels and VCCINT_IO Connection* section.
VCCINT_GT_[*L or R*]	Dedicated	N/A	GTM core power-supply pins.
VCCAUX	Dedicated	N/A	Power-supply pins for auxiliary circuits.
VCCAUX_IO	Dedicated	N/A	Auxiliary power-supply pins for the I/O banks. VCCAUX_IO must be connected to VCCAUX on the board. ***Note:*** Package files for XQ ruggedized Kintex and Virtex UltraScale+devices (for example: FFRB676) have unique pin names for VCCAUX_HPIO and VCCAUX_HDIO. These pins can be connected to a common VCCAUX_IO supply.
VCCIO_HBM_[HBM bank number]	Dedicated	N/A	HBM component I/O power supply (VDDQ)
VCC_HBM_[HBM bank number]	Dedicated	N/A	HBM component core power supply (VDDC)
VCCAUX_HBM_[HBM bank number]	Dedicated	N/A	HBM component word line voltage pump (VPP)
VCCBRAM	Dedicated	N/A	Block RAM power supply pins.
VBATT	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used.
VCCO_[bank number][4]	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VREF_[bank number]	Dedicated	N/A	These are input threshold voltage pins.

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
RSVDGND	Dedicated	N/A	Reserved pins—must be tied to GND. These pins are present on Artix UltraScale+, Kintex UltraScale+, and Virtex UltraScale+ devices. **TIP:** *In footprint compatible devices, this pin can be labeled differently and serve different purposes. When planning migration between devices, include the functionality between all footprint compatible devices.*
RSVD	Dedicated	N/A	Reserved pins—leave floating. **TIP:** *In footprint compatible devices, this pin can be labeled differently and serve different purposes. When planning migration between devices, include the functionality between all footprint compatible devices.*
Multi-gigabit Serial Transceiver Pins (GTHE3 and GTYE3)			
For more information on the GTH and GTY transceivers see the *UltraScale Architecture GTH Transceivers User Guide* (UG576) or *UltraScale Architecture GTY Transceivers User Guide* (UG578).			
MGTHRX[P or N][0 to 3] _[GT quad number]	Dedicated	Input	Differential receive port GTH Quad.
MGTHTX[P or N][0 to 3] _[GT quad number]	Dedicated	Output	Differential transmit port GTH Quad.
MGTYRX[P or N][0 to 3] _[GT quad number]	Dedicated	Input	Differential receive port GTY Quad.
MGTYTX[P or N][0 to 3] _[GT quad number]	Dedicated	Output	Differential transmit port GTY Quad.
MGTYRX[P or N][0 to 3] _[GT dual number]	Dedicated	Input	Differential receive port GTM Dual.
MGTYTX[P or N][0 to 3] _[GT dual number]	Dedicated	Output	Differential transmit port GTM Dual.
MGTAVCC_[L or R] [N, UC, C, LC, or S][5]	Dedicated	Input	Analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_[L or R] [N, UC, C, LC, or S][5]	Dedicated	Input	Analog power-supply pin for the transmit driver.

Table 1-6: **Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
MGTVCCAUX_[L or R] [N, UC, C, LC, or S][5]	Dedicated	Input	Auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.
MGTREFCLK[0 or 1] [P or N]	Dedicated	Input	Differential reference clock for the transceivers.
MGTAVTTRCAL_[L or R] [N, UC, C, LC, or S][5]	Dedicated	N/A	Precision reference resistor pin for internal calibration termination.
MGTRREF_[L or R] [N, UC, C, LC, or S][5]	Dedicated	Input	Precision reference resistor pin for internal calibration termination.

Notes:

1. See the DCI sections in *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information on the VRP pins.
2. All dedicated configuration pins are powered by V_{CCO_0}.
3. See the *UltraScale Architecture System Monitor User Guide* (UG580) for the default connections required to support on-chip monitoring.
4. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank (for package migration). Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or GND).
5. L (left) or R (right) plus N (north), UC (upper center), C (center), LC (lower center), and S (south) signify the GT transceiver quad power supply groups. For example, RUC signifies the right-upper-center power supply group and LLC signifies the left-lower-center power supply group in the FLGA2577 package.

Footprint Compatibility between Packages

UltraScale and UltraScale+ devices are footprint compatible only with other UltraScale and UltraScale+ devices with the same number of package pins and the same preceding alphabetic designator. For example, XCKU060-FFVA1517 is compatible with XCKU085-FLVA1517 and XCKU115-FLVA1517, but not with XCKU115-FLVD1517. Pins that are available in one device but are not available in another device with a compatible package include the other device's name in the *No Connect* column of the package file. These pins are labeled as *No Connects* in the other device's package file.

IMPORTANT: *Footprint compatibility does not necessarily imply that all pins will function in the same manner for different devices in a package. For limitations and guidelines on designing for footprint compatible packages, refer to the Migration Between UltraScale Devices and Packages section of UltraScale Architecture PCB Design Guide (UG583).*

Table 1-7 shows the footprint compatible devices available for each UltraScale and UltraScale+ device package. See *UltraScale Architecture and Product Overview* (DS890) for specific package letter code options.

IMPORTANT: *The height dimensions of footprint compatible packages can vary since some devices contain SSI technology.*

Table 1-7: **Footprint Compatibility**

Packages	Footprint Compatible Devices							
A289	XCAU7P	XAAU7P						
A361	XCSU10P	XCSU25P	XCSU35P					
A368	XCAU10P	XCAU15P						
B484	XCAU10P	XCAU15P	XAAU10P	XAAU15P				
C484	XCAU7P	XAAU7P						
A529	XCSU10P	XCSU25P	XCSU35P					
B625	XCSU10P	XCSU25P	XCSU35P					
A676	XCKU035	XCKU040	XQKU040	XCKU3P	XCKU5P			
B676	XCAU10P[(2)]	XCAU15P[(2)]	XCAU20P[(2)]	XCAU25P[(2)]	XAAU10P[(2)]	XAAU15P[(2)]	XCKU3P	XCKU5P	XQKU5P

Table 1-7: **Footprint Compatibility *(Cont'd)***

Packages	Footprint Compatible Devices													
A784	XCKU035	XCKU040												
B784	XCAU20P	XCAU25P	XCKU3P	XCKU5P	XQKU5P									
A900	XCKU035	XCKU040												
D900	XCKU3P	XCKU5P	XCKU11P											
E900	XCKU9P	XCKU13P												
A1156	XCKU025	XCKU035	XCKU040	XQKU040	XCKU060	XQKU060	XCKU095	XQKU095	XCKU11P	XCKU15P	XQKU15P			
A1365	XCVU23P													
A1517	XCKU060	XCKU085	XCKU115											
C1517	XCKU095	XCVU065	XCVU080	XCVU095	XCVU3P	XQVU3P								
D1517	XCKU115	XQKU115	XCVU080	XCVU095	XCVU125									
E1517	XCKU11P	XCKU15P	XQKU15P											
A1760	XCKU15P													
B1760	XCKU085	XCKU095	XCKU115	XCVU080	XCVU095	XCVU125								
E1760	XCKU15P													
J1760	XCKU19P	XCVU23P												
D1924	XCKU115													
F1924	XCKU085	XCKU115	XQKU115	XCVU11P										
H1924	XCVU31P													
A2104	XCKU115	XCVU080	XCVU095	XCVU125	XCVU5P	XCVU7P	XCVU9P	XCVU13P[1]	XQVU7P					
B2104	XCKU095	XCKU115	XCKU19P	XCVU080	XCVU095	XCVU125	XCVU160	XCVU190	XCVU5P	XCVU7P	XCVU9P	XCVU11P	XCVU13P[1]	XQVU7P
C2104	XCVU095	XCVU125	XCVU160	XCVU190	XCVU5P	XCVU7P	XCVU9P	XCVU11P	XCVU13P[1]	XQVU11P				
D2104	XCVU9P	XCVU11P	XCVU13P	XCVU27P[1]	XCVU29P[1]									
H2104	XCVU33P	XCVU35P	XCVU45P											
B2377	XCVU440													
A2577	XCVU190	XCVU9P	XCVU11P	XCVU13P	XCVU27P	XCVU29P								

Table 1-7: **Footprint Compatibility *(Cont'd)***

Packages	Footprint Compatible Devices				
A2892	XCVU440				
H2892	XCVU35P	XCVU37P	XCVU45P	XCVU47P	
K2892	XCVU57P				
A3824	XCVU19P				
B3824	XCVU19P				

Notes:

1. While footprint compatible, the body size for the VU13P, VU27P, and VU39P is 52.5 mm, which is larger than the 47.5 mm for a 2104 ball package.
2. While footprint compatible, incompatibilities exist between banks 85/86 (AU10P and AU15P) and 86/87 (AU20P and AU25P) with regards to the System Monitor analog inputs (AD pins). This incompatibility should be considered when designing for migration between these devices.

Many UltraScale and UltraScale+ devices that are footprint compatible in a package have different I/O bank and transceiver quad numbers connected to the same package pins. Due to these differences, when migrating between devices in a specific package, the type of bank (HP vs. HR) or quad (GTH vs. GTY), whether a bank is connected or NC at the package pins, and where the bank or quad is located on the die must be taken into consideration. Table 1-8 and Table 1-10 show how the banks and transceiver quads are numbered between devices in each package.

For all grouped-together footprint compatible packages, the bank and quad numbers in the same column for each device are connect to the same package pins. For example, in the FFVD1517 and FLVD1517 packages, bank 69 for the XCVU095 is connected to the same pins as bank 71 for the XCVU125.

A limited number of banks have fewer than 52 SelectIO pins. For a visual representation of all of this information, see the Die Level Bank Numbering Overview section.

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[(1)]**

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FCVA289	XCAU7P			65	66	84			104		106																				85, 86, 105
	XAAU7P			65	66	84			104		106																				85, 86, 105
CMVA361	XCSU10P			65	66	67	68	45	46					47																	
	XCSU25P			65	66	67	68	45	46					47																	
	XCSU35P			65	66	67	68	45	46					47																	
UBVA368	XCAU10P	84		65	66																										64, 85, 86
	XCAU15P	84		65	66																										64, 85, 86
SBVB484	XCAU10P		64	65	66	84	85																								86
	XAAU10P		64	65	66	84	85																								86
	XCAU15P		64	65	66	84	85																								86
	XAAU15P		64	65	66	84	85																								86
SBVC484	XCAU7P			65	66	84	85	86	104	105	106																				86
	XAAU7P			65	66	84	85	86	104	105	106																				86

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[(1)] *(Cont'd)***

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
CMVA529	XCSU10P			65	66	67	68	45	46					47																	
	XCSU25P			65	66	67	68	45	46					47																	
	XCSU35P			65	66	67	68	45	46					47																	
SBVB625	XCSU10P			65	66	67	68	45	46					47																	
	XCSU25P			65	66	67	68	45	46					47																	
	XCSU35P			65	66	67	68	45	46					47																	
FBVA676	XCKU035			65	66	44	45	46											64												47, 48, 67, 68
	XCKU040			65	66	44	45	46											64												47, 48, 67, 68
RBA676	XQKU040			65	66	44	45	46											64												47, 48, 67, 68
FFVA676	XCKU3P			65	66	64		67											84/85												86, 87
	XCKU5P			65	66	64		67											84/85												86, 87
FFVB676	XCAU10P[(2)]	84	64	65	66		85	86																							
	XAAU10P[(2)]	84	64	65	66		85	86																							
	XCAU15P[(2)]	84	64	65	66		85	86																							
	XAAU15P[(2)]	84	64	65	66		85	86																							
	XCAU20P[(2)]	84	64	65	66		86	87																							67, 85
	XCAU25P[(2)]	84	64	65	66	67	86	87																							85
	XCKU3P	84	64	65	66	67	86	87																							85
	XCKU5P	84	64	65	66	67	86	87																							85
FFRB676	XQKU5P	84	64	65	66	67	86	87																							85
SFVA784	XCKU035			65	44	45	46	47	66	68	67								64												48
	XCKU040			65	44	45	46	47	66	68	67								64												48

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[1] *(Cont'd)***

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
SFVB784	XCAU20P		64	65	66			86	84	85																					67, 87
	XCAU25P		64	65	66	67	87	86	84	85																					
	XCKU3P		64	65	66	67	87	86	84	85																					
	XCKU5P		64	65	66	67	87	86	84	85																					
SFRB784	XQKU5P		64	65	66	67	87	86	84	85																					
FBVA900	XCKU035			65	66	67	44	45	46	47	48								64												68
	XCKU040			65	66	67	44	45	46	47	48								64												68
FFVD900	XCKU3P			65	66	64	67			84	85	87	86																		
	XCKU5P			65	66	64	67			84	85	87	86																		
	XCKU11P			65	66	67	68	69	70	88	89	91	90																		71, 64
FFVE900	XCKU9P		64	65	66	67	44	47							48	49															50
	XCKU13P		64	65	66	67	44	47							48	49															50
FFVA1156	XCKU025			65	66			44	45	46									64												
	XCKU035			65	66	67	68	44	45	46	47	48							64												
	XCKU040			65	66	67	68	44	45	46	47	48							64												
	XCKU060			65	66	67	68	44	45	46	47	48							64												24, 25
	XCKU095			65	66	68	67	45	44	46	47	48							64												49, 50, 51, 69, 70, 71
	XCKU11P			65	66	70	71	67	64		68	69							88/89												90, 91
	XCKU15P			65	66	71	72	67	64	68	69	70							90/91												73, 74, 93, 94
FFRA1156	XQKU15P			65	66	71	72	67	64	68	69	70							90/91												73, 74, 93, 94
RFA1156	XQKU040			65	66	67	68	44	45	46	47	48							64												
	XQKU060			65	66	67	68	44	45	46	47	48							64												24, 25
	XQKU095			65	66	68	67	45	44	46	47	48							64												49, 50, 51, 69, 70, 71
VSVA1365	XCVU23P			65	66	67	68				72	73	74																		71, 70, 69, 64, 92, 90, 88

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[1] *(Cont'd)***

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FFVA1517	XCKU060			65	44	45	24	25	66	67	68	46	47	48					64												
FLVA1517	XCKU085			65	44	45	24	25	66	67	68	46	47	48					64												29, 30, 49, 50, 51, 52, 69, 70, 71, 72
	XCKU115			65	44	45	24	25	66	67	68	46	47	48					64												29, 30, 49, 50, 51, 52, 69, 70, 71, 72
FFVC1517	XCKU095		84/94	65	66	67	68	44	45	46	47	48																			51, 50, 49, 71, 70, 69
	XCVU080		84/94	65	66	67	68	44	45	46	47	48																			51, 50, 49, 71, 70, 69
	XCVU065		84/94	65	66	67	68	44	45	46	47	48																			
	XCVU095		84/94	65	66	67	68	44	45	46	47	48																			51, 50, 49, 71, 70, 69
	XCVU3P		64	65	66	67	68	44	45	46	47	48																			
FFRC1517	XQVU3P		64	65	66	67	68	44	45	46	47	48																			
FFVD1517	XCVU080		84/94	65	66	67[3]	69	70	71																						44, 45, 46, 47, 48, 49, 50, 51, 68
	XCVU095		84/94	65	66	67[3]	69	70	71																						44, 45, 46, 47, 48, 49, 50, 51, 68
FLVD1517	XCKU115		84/94	65	66	67[3]	71	72	73																						24, 25, 29, 30, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 68, 69, 70
	XCVU125		84/94	65	66	67[3]	71	72	73																						44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 68, 69, 70
RLD1517	XQKU115		84/94	65	66	67[3]	71	72	73																						24, 25, 29, 30, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 68, 69, 70
FFVE1517	XCKU11P			65	64	66	67	68							91	90	89	88	71	70	69										
	XCKU15P			65	64	66	67	68							94	93	91	90	71	70	69										74, 73, 72
FFRE1517	XQKU15P			65	64	66	67	68							94	93	91	90	71	70	69										74, 73, 72

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[1] *(Cont'd)***

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FFVA1760	XCKU15P			65	64	66	67	68							94	93	91	90	72	71	70										74, 73, 69
FLVB1760	XCKU085		84/94	65	66	67	44	45	46	47	48	49	50	51	52																24, 25, 29, 30, 68, 69, 70, 71, 72
	XCKU115		84/94	65	66	67	44	45	46	47	48	49	50	51	52	53[3]															24, 25, 29, 30, 68, 69, 70, 71, 72, 73
FFVB1760	XCKU095		84/94	65	66	67	44	45	46	47	48	70	71	49	50	51[3]															68, 69
	XCVU080		84/94	65	66	67	44	45	46	47	48	70	71	49	50	51[3]															68, 69
	XCVU095		84/94	65	66	67	44	45	46	47	48	70	71	49	50	51[3]															68, 69
FLVB1760	XCVU125		84/94	65	66	67	44	45	46	47	48	49	50	51	52	53[3]															68, 69, 70, 71, 72, 73
FFVE1760	XCKU15P			65	64	66	67	68	69						94	93	91	90	74	73	72	71	70								
FFVJ1760	XCKU19P			65	66	67	68	69							88	90	92		70	71	72	73									74, 64
FSVJ1760	XCVU23P		64	65	66	67	68	69							88	90	92		70	71	72	73	74								
FLVD1924	XCKU115		84/94	65	66	67	44	45	46	47	50	51	52	53	70	71	72	73													24, 25, 29, 30, 48, 49, 68, 69
FLVF1924	XCKU085			65	66	67	68	44	45	46	51	52		70	71	72															30, 29, 25, 24, 50, 49, 48, 47, 69, 64
	XCKU115			65	66	67	68	44	45	46	51	52	53	70	71	72	73														30, 29, 25, 24, 50, 49, 48, 47, 69, 64
RLF1924	XQKU115			65	66	67	68	44	45	46	51	52	53	70	71	72	73														30, 29, 25, 24, 50, 49, 48, 47, 69, 64
FLGF1924	XCVU11P			65	66	67	68	64			69	70	71	72	73	74	75														
FSVH1924	XCVU31P		64	65	66	67																									

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[(1)] *(Cont'd)***

Package	Device	Package to Device I/O Mapping																												Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FFVA2104	XCVU080		84/94	65	66	67	44	45	46	47	48	49	50	51	68	69	70	71													
	XCVU095		84/94	65	66	67	44	45	46	47	48	49	50	51	68	69	70	71													
FLVA2104	XCKU115		84/94	65	66	67	44	45	46	47	50	51	52	53	70	71	72	73													30, 29, 25, 24, 49, 48, 69, 68
	XCVU125		84/94	65	66	67	44	45	46	47	50	51	52	53	70	71	72	73													49, 48, 69, 68
	XCVU5P		64	65	66	67	44	45	46	47	50	51	52	53	70	71	72	73													49, 48, 69, 68
	XCVU7P		64	65	66	67	44	45	46	47	50	51	52	53	70	71	72	73													49, 48, 69, 68
FLRA2104	XQVU7P		64	65	66	67	44	45	46	47	50	51	52	53	70	71	72	73													49, 48, 69, 68
FLGA2104	XCVU9P		64	65	66	67	40	41	42	43	45	46	47	48	70	71	72	73													53, 52, 51, 50, 49, 44, 39, 69, 68, 63, 62, 61, 60, 59
FHGA2104	XCVU13P		64	65	66	67	60	61	62	63	68	69	70	71	72	73	74	75													

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[1]** ***(Cont'd)***

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FFVB2104	XCKU095		84/94	65	66	67	68[3]	44	45	46	49	50	51	69	70	71															48, 47
	XCVU080		84/94	65	66	67	68[3]	44	45	46	49	50	51	69	70	71															48, 47
	XCVU095		84/94	65	66	67	68[3]	44	45	46	49	50	51	69	70	71															48, 47
	XCKU19P		90/92	65	66	67	88				73	72	71	68	69	70															74, 64
FLVB2104	XCKU115		84/94	65	66	67	68[3]	44	45	46	51	52	53	71	72	73															30, 29, 25, 24, 50, 49, 48, 47, 70, 69
	XCVU125		84/94	65	66	67	68[3]	44	45	46	50	51	52	70	71	72															53, 49, 48, 47, 73, 69
	XCVU5P		64	65	66	67	68[3]	44	45	46	50	51	52	70	71	72															53, 49, 48, 47, 73, 69
	XCVU7P		64	65	66	67	68[3]	44	45	46	50	51	52	70	71	72															53, 49, 48, 47, 73, 69
FLRB2104	XQVU7P		64	65	66	67	68[3]	44	45	46	50	51	52	70	71	72															53, 49, 48, 47, 73, 69
FLGB2104	XCVU160		84/94	65	66	67	68[3]	44	45	46	50	51	52	70	71	72															53, 49, 48, 47, 43, 42, 41, 40, 73, 69, 63, 62, 61, 60
	XCVU190		84/94	65	66	67	68[3]	44	45	46	50	51	52	70	71	72															53, 49, 48, 47, 43, 42, 41, 40, 39, 73, 69, 63, 62, 61, 60, 59
	XCVU9P		64	65	66	67	68[3]	40	41	42	46	47	48	70	71	72															53, 52, 51, 50, 49, 45, 44, 43, 39, 73, 69, 63, 62, 61, 60, 59
	XCVU11P		64	65	66	67		68			69	70	71	72	73	74															75
FHGB2104	XCVU13P		64	65	66	67	68[3]	61	62	63	69	70	71	72	73	74															75, 60

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[(1)]** ***(Cont'd)***

Package	Device	Package to Device I/O Mapping																													Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FFVC2104	XCVU095		84/94	65	66	67	68	69	70	71																					51, 50, 49, 48, 47, 46, 45, 44
FLVC2104	XCVU125		84/94	65	66	67	68	70	71	72																					53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 73, 69
	XCVU5P		64	65	66	67	68	70	71	72																					53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 73, 69
	XCVU7P		64	65	66	67	68	70	71	72																					53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 73, 69
FLGC2104	XCVU160		84/94	65	66	67	68	70	71	72																					52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 69, 63, 62, 61, 60
	XCVU190		84/94	65	66	67	68	70	71	72																					53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 39, 73, 69, 63, 62, 61, 60, 59
	XCVU9P		64	65	66	67	68	70	71	72																					53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 39, 73, 69, 63, 62, 61, 60, 59
	XCVU11P		64	65	66	67	68	69	70	71																					75, 74, 73, 72
FLRC2104	XQVU11P		64	65	66	67	68	69	70	71																					75, 74, 73, 72
FHGC2104	XCVU13P		64	65	66	67	68	69	70	71																					75, 74, 73, 72, 63, 62, 61, 60
FSGD2104	XCVU9P		64	65	66	67	40	41	42		46	47	48	70	71	72															53, 52, 51, 50, 49, 45, 44, 43, 39, 73, 69, 68, 63, 62, 61, 60, 59
	XCVU11P		64	65	66	67	68				69	70	71	72	73	74															75
FIGD2104	XCVU13P		64	65	66	67	61	62	63		69	70	71	72	73	74															75, 68, 60
	XCVU27P		64	65	66	67	61	62	63		69	70	71	72	73	74															75, 68, 60
	XCVU29P		64	65	66	67	61	62	63		69	70	71	72	73	74															75, 68, 60
FSVH2104	XCVU33P		64	65	66			67																							
	XCVU35P		64	65	66			67	68	69	70	71																			
	XCVU45P		64	65	66			67	68	69	70	71																			

Table 1-8: **I/O Bank Migration: HP I/O Banks are Unshaded, HR I/O Banks are in Gray, and HD I/O Banks are in Dark Gray[1] *(Cont'd)***

Package	Device	Package to Device I/O Mapping																												Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	
FLGB2377	XCVU440		84/94	65	66	67	68	60	61	62	63	40	41	42	43	45	46	47	48	50	51	52	53	70	71	72	73				39, 44, 49, 59, 69
FLGA2577	XCVU190		66[3]	65	61	62	63	67	68[3]	70	71	72																			53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 39, 73, 69, 64, 60, 59
	XCVU9P		66[3]	65	61	62	63	67	68[3]	70	71	72																			53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41, 40, 39, 73, 69, 64, 60, 59
	XCVU11P		66[3]	65	68	69	70	71	72[3]	73	74	75																			67, 64
	XCVU13P		66[3]	65	61	62	63	70	71[3]	73	74	75																			72, 69, 68, 67, 64, 60
FSGA2577	XCVU13P		66[3]	65	61	62	63	70	71[3]	73	74	75																			72, 69, 68, 67, 64, 60
	XCVU27P		66[3]	65	61	62	63	70	71[3]	73	74	75																			72, 69, 68, 67, 64, 60
	XCVU29P		66[3]	65	61	62	63	70	71[3]	73	74	75																			72, 69, 68, 67, 64, 60
FLGA2892	XCVU440		84/94	65	66	67	68	60	61	62	63	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	70	71	72	73	59, 69
FSVH2892	XCVU35P		64	65	66	67	68	69		70	71																				
	XCVU37P		64	65	66	67	68	69		70	71	72	73	74	75																
	XCVU45P		64	65	66	67	68	69		70	71																				
	XCVU47P		64	65	66	67	68	69		70	71	72	73	74	75																
FSVK2892	XCVU57P		64	65	66	67	68	69		75	74	73	70	71	72																

Notes:

1. See the Die Level Bank Numbering Overview for specific changes in column numbering.
2. While footprint compatible, incompatibilities exist between banks 85/86 (AU10P and AU15P) and 86/87 (AU20P and AU25P) with regards to the System Monitor analog inputs (AD pins). This incompatibility should be considered when designing for migration between these devices.
3. A limited number of banks have fewer than 52 SelectIO pins. These banks are labeled as partial.

Table 1-9: **I/O Bank Migration for VU19P devices: HP I/O Banks are Unshaded and HD I/O Banks are in Dark Gray**

Package	Device	Package to Device I/O Mapping																																								Unbonded I/O Banks
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	AM	AN	AO	AP	
FSVA3824	XCVU19P	59	60	65	61	62	63	64	66	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	69	70	71	72	73	74	75	76	77	78	98	93	88	83	68, 67
FSVB3824	XCVU19P	60	61	65	62	66	67	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	70	71	72	75	76	77	98	93	88	83							78, 74, 73, 69, 68, 64, 63, 59

For each grouped set of footprint compatible packages listed in Table 1-10, there is a row detailing the power supply group for each quad. These groups are labeled according to the regions for the transceiver power supply pins, as listed in the ASCII Pinout Files linked from Chapter 2, Package Files. For a visual representation of all of this information, see the Die Level Bank Numbering Overview section.

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)**

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		R																																
FCVA289	XCAU7P		124																															
	XAAU7P		124																															
Power Supply Group		R																																
UBVA368	XCAU10P	224	225																															226
	XCAU15P	224	225																															226
Power Supply Group		R																																
SBVB484	XCAU10P	224	225	226																														
	XAAU10P	224	225	226																														
	XCAU15P	224	225	226																														
	XAAU15P	224	225	226																														
Power Supply Group		R																																
SBVC484	XCAU7P		124																															
	XAAU7P		124																															
Power Supply Group		—																																
FFVB676	XCAU10P	224	225	226																														
	XCAU15P	224	225	226																														

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray) *(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		—																																
FBVA676	XCKU035	224	225	226	227																													228
	XCKU040	224	225	226	227																													228
RBA676	XQKU040	224	225	226	227																													228
Power Supply Group		R																																
FFVA676	XCKU3P	224	225	226	227																													
	XCKU5P	224	225	226	227																													
Power Supply Group		R																																
FFVB676	XCAU10P	224	225	226																														
	XAAU10P	224	225	226																														
	XCAU15P	224	225	226																														
	XAAU15P	224	225	226																														
	XCAU20P	224	225	226																														227
	XCAU25P	224	225	226																														227
	XCKU3P	224	225	226	227																													
	XCKU5P	224	225	226	227																													
FFRA676	XQKU5P	224	225	226	227																													
Power Supply Group		—																																
SFVA784	XCKU035	224	225																															228,227,226
	XCKU040	224	225																															228,227,226

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		R																																
SFVB784	XCAU20P	224	225	226																														
SFVB784	XCAU25P	224	225	226																														
SFVB784	XCKU3P	224	225	226	227																													
SFVB784	XCKU5P	224	225	226	227																													
SFRB784	XQKU5P	224	225	226	227																													
Power Supply Group		—																																
FBVA900	XCKU035	224	225	226	227																													228
FBVA900	XCKU040	224	225	226	227																													228
Power Supply Group		R																																
FFVD900	XCKU3P	224	225	226	227																													
FFVD900	XCKU5P	224	225	226	227																													
FFVD900	XCKU11P	224	225	226	227																													131, 130, 129, 128, 127, 231, 230, 229, 228
Power Supply Group		R			L																													
FFVE900	XCKU9P	228	229	230	127	128	129	130																										
FFVE900	XCKU13P	228	229	230	127	128	129	130																										

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray) *(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		R					L																											
FFVA1156	XCKU025	224	225	226																														
	XCKU035	224	225	226	227																													228
	XCKU040	224	225	226	227	228																												
	XCKU060	224	225	226	227	228	127	128																										126
	XCKU095	224	225	226	227	228	129	130																										131, 128, 127, 126, 125, 124, 231, 230, 229
	XCKU11P	224	225	226	227	228	129	130																										131, 128, 127, 231, 230
	XCKU15P	224	225	226	227	228	129	130																										134, 133, 132, 131, 128, 127, 234, 233, 232, 231, 230, 229
FFRA1156	XQKU15P	224	225	226	227	228	129	130																										134, 133, 132, 131, 128, 127, 234, 233, 232, 231, 230, 229
RFA1156	XQKU040	224	225	226	227	228																												
	XQKU060	224	225	226	227	228	127	128																										126
	XQKU095	224	225	226	227	228	129	130																										131, 128, 127, 126, 125, 124, 231, 230, 229
Power Supply Group		RS				RC					RN																							
VSVA1365	XCVU23P	224	225	226	227	228	229	230	231	232	233	234																						

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		RS					RN				L																							
FFVA1517	XCKU060	224	225	226	227	228					126	127	128																					
FLVA1517	XCKU085	224	225	226	227	228	229	230	231	232	126	127	128																					132,131
	XCKU115	224	225	226	227	228	229	230	231	232	126	127	128																					132,131
Power Supply Group		R					L																											
FFVC1517	XCKU095	224	225	226	227	228	125	126	127	128	129																							131, 130, 124, 231, 230, 229
	XCVU080	224	225	226	227	228	125	126	127	128	129																							131, 130, 124, 231, 230, 229
	XCVU065	224	225	226	227	228	124	125	126	127	128																							
	XCVU095	224	225	226	227	228	125	126	127	128	129																							131, 130, 124, 231, 230, 229
	XCVU3P	224	225	226	227	228	124	125	126	127	128																							
FFRC1517	XQVU3P	224	225	226	227	228	124	125	126	127	128																							
Power Supply Group		RS					RN					LS				LN																		
FFVD1517	XCVU080	224	225	226	227	228	229	230	231			124	125	126	127	128	129	130	131															
	XCVU095	224	225	226	227	228	229	230	231			124	125	126	127	128	129	130	131															
FLVD1517	XCVU125	224	225	226	227	228	229	230	231	232	233	124	125	126	127	129	130	131	132															133,128
	XCKU115	224	225	226	227	228	229	230	231	232	233		126	127	128		131	132	133															
RLD1517	XQKU115	224	225	226	227	228	229	230	231	232	233		126	127	128		131	132	133															
Power Supply Group		RS				RN				L																								
FFVE1517	XCKU11P	224	225	226	227	228	229	230	231	127	128	129	130	131																				
	XCKU15P	224	225	226	227	228	229	230	231	127	128	129	130	131	132																			134, 133, 234, 233, 232
FFRE1517	XQKU15P	224	225	226	227	228	229	230	231	127	128	129	130	131	132																			134, 133, 234, 233, 232

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		RS						RN					LS				LN																	
FFVA1760	XCKU15P	224	225	226	227	228	229	230	231	232	233	234	127	128	129	130	131	132	133	134														
Power Supply Group		RS					RN				L																							
FLVB1760	XCKU085	224	225	226	227	228	230	231	232		128	131	132																					127,126,229
FLVB1760	XCKU115	224	225	226	227	228	230	231	232	233	128	131	132	133																				127,126,229
FFVB1760	XCKU095	224	225	226	227	228	229	230	231		128	129	130	131																				127,126,125,124
FFVB1760	XCVU080	224	225	226	227	228	229	230	231		128	129	130	131																				127,126,125,124
FFVB1760	XCVU095	224	225	226	227	228	229	230	231		128	129	130	131																				127,126,125,124
FLVB1760	XCVU125	224	225	226	227	228	230	231	232	233	129	130	131	132																				133, 128, 127, 126, 125, 229
Power Supply Group		RS				RN				L																								
FFVE1760	XCKU15P	224	225	226	227	228	229	230	231	127	128	129	130	131	132																			134, 133, 234, 233, 232
Power Supply Group		RS				RC					RN																							
FFVJ1760	XCKU19P		225	226	227	228	229	230	231	232																								
FSVJ1760	XCVU23P	224	225	226	227	228	229	230	231	232	233	234																						

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray) *(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																														Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		RS				RN			LS			LN																						
FLVD1924	XCKU115	224	225	226	227	231	232	233	126	127	128	131	132	133																				230,229,228
Power Supply Group		RS					RN					LS			LN																			
FLVF1924	XCKU085	224	225	226	227	228	229	230	231	232		126	127	128	131			132																
	XCKU115	224	225	226	227	228	229	230	231	232	233	126	127	128	131		133	132																
RLF1924	XQKU115	224	225	226	227	228	229	230	231	232	233	126	127	128	131		133	132																
FLGF1924	XCVU11P	224	225	226	227	228	229	230	231	232	233	125	126	127	129		131	130																135, 134, 133, 132, 128, 124, 235, 234
Power Supply Group		R				L																												
FSVH1924	XCVU31P	224	225	226	227	124	125	126	127																									

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		RS				RN			LS			LN																						
FFVA2104	XCVU080	224	225	226	227	228	229	230	125	126	127	128	129	130																				131, 124, 231
	XCVU095	224	225	226	227	228	229	230	125	126	127	128	129	130																				131, 124, 231
FLVA2104	XCKU115	224	225	226	227	231	232	233	126	127	128	131	132	133																				230, 229, 228
	XCVU125	224	225	226	227	231	232	233	125	126	127	130	131	132																				133, 129, 128, 124, 230, 229, 228
	XCVU5P	224	225	226	227	231	232	233	125	126	127	130	131	132																				133, 129, 128, 124, 230, 229, 228
	XCVU7P	224	225	226	227	231	232	233	125	126	127	130	131	132																				133, 129, 128, 124, 230, 229, 228
FLRA2104	XQVU7P	224	225	226	227	231	232	233	125	126	127	130	131	132																				133, 129, 128, 124, 230, 229, 228
FLGA2104	XCVU9P	224	225	226	227	231	232	233	120	121	122	125	126	127																				133, 132, 131, 130, 129, 128, 124, 123, 119, 230, 229, 228, 223, 222, 221, 220, 219
FHGA2104	XCVU13P	224	225	226	227	229	230	231	125	126	127	129	130	131																				135, 134, 133, 132, 128, 124, 123, 122, 121, 120, 235, 234, 233, 232, 228, 223, 222, 221, 220

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		RS					RN					LS				LN																		
FFVB2104	XCKU095	224	225	226	227	228	229	230	231			124	125	126	127	128	129	130	131															
	XCVU080	224	225	226	227	228	229	230	231			124	125	126	127	128	129	130	131															
	XCVU095	224	225	226	227	228	229	230	231			124	125	126	127	128	129	130	131															
	XCKU19P	225	226	227	228		229	230	231	232																								
FLVB2104	XCKU115	224	225	226	227	228	229	230	231	232	233	126	127	128			131	132	133															
	XCVU125	224	225	226	227	228	229	230	231	232	233	125	126	127	128	129	130	131	132	133														124
	XCVU5P	224	225	226	227	228	229	230	231	232	233	125	126	127	128	129	130	131	132	133														124
	XCVU7P	224	225	226	227	228	229	230	231	232	233	125	126	127	128	129	130	131	132	133														124
FLRB2104	XQVU7P	224	225	226	227	228	229	230	231	232	233	125	126	127	128	129	130	131	132	133														124
FLGB2104	XCVU160	224	225	226	227	228	229	230	231	232	233	125	126	127	128	129	130	131	132	133														124, 123, 122, 121, 120, 223, 222, 221, 220
	XCVU190	224	225	226	227	228	229	230	231	232	233	125	126	127	128	129	130	131	132	133														124, 123, 122, 121, 120, 119, 223, 222, 221, 220, 219
	XCVU9P	224	225	226	227	228	229	230	231	232	233	120	121	122	123	124	125	126	127	128														133, 132, 131, 130, 129, 119, 223, 222, 221, 220, 219
	XCVU11P	224	225	226	227	228	229	230	231	232	233	124	125	126	127	128	129	130	131	133														135, 134, 132, 235, 234
FHGB2104	XCVU13P	224	225	226	227	228	229	230	231	232	233	124	125	126	127	128	129	130	131	133														135, 134, 132, 123, 122, 121, 120, 235, 234, 223, 222, 221, 220

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	Unbonded GT Quads
Power Supply Group		RC					RN					RS			LC					LN					LS									
FFVC2104	XCVU095	224	225	226	227	228	229	230	231						124	125	126	127	128	129	130	131												
FLVC2104	XCVU125	224	225	226	227	228	229	230	231	232	233				124	125	126	127	128	129	130	131	132	133										
	XCVU5P	224	225	226	227	228	229	230	231	232	233				124	125	126	127	128	129	130	131	132	133										
	XCVU7P	224	225	226	227	228	229	230	231	232	233				124	125	126	127	128	129	130	131	132	133										
FLGC2104	XCVU160	224	225	226	227	228	229	230	231	232	233	220	221	222	124	125	126	127	128	129	130	131	132	133	120	121	122							123, 223
	XCVU190	224	225	226	227	228	229	230	231	232	233	220	221	222	124	125	126	127	128	129	130	131	132	133	120	121	122							123, 119, 223, 219
	XCVU9P	224	225	226	227	228	229	230	231	232	233	220	221	222	124	125	126	127	128	129	130	131	132	133	120	121	122							123, 119, 223, 219
	XCVU11P	226	227	228	229	230	231	232	233	234	235		224	225	126	127	128	129	130	131	132	133	134	135		124	125							
FLRC2104	XQVU11P	226	227	228	229	230	231	232	233	234	235		224	225	126	127	128	129	130	131	132	133	134	135		124	125							
FHGC2104	XCVU13P	224	225	226	227	228	229	230	231	232	233	221	222	223	124	125	126	127	128	129	130	131	132	133	121	122	123							135, 134, 120, 235, 234, 220

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray) *(Cont'd)***

Package	Device	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	Unbonded GT Quads
Power Supply Group		RS					RN					LS				LN																		
FSGD2104	XCVU9P	224	225	226	227	228	229	230	231	232	233	120	121	122	123	124	125	126	127	131														133, 132, 130, 129, 128, 119, 223, 222, 221, 220, 219
	XCVU11P	224	225	226	227	228	229	230	231	232	233	124	125	126	127	128	129	130	131	133														135, 134, 132, 235, 234
FIGD2104	XCVU13P	224	225	226	227	228	229	230	231	232	233	120	121	122	123	128	129	130	131	133														135, 134, 132, 127, 126, 125, 124, 235, 234, 223, 222, 221, 220
	XCVU27P	224	225	226	227	228	229	230	231	232	233	120	121	122	123	128	129	130	131	133														135, 134, 132, 127, 126, 125, 124, 235, 234, 223, 222, 221, 220
	XCVU29P	224	225	226	227	228	229	230	231	232	233	120	121	122	123	128	129	130	131	133														135, 134, 132, 127, 126, 125, 124, 235, 234, 223, 222, 221, 220
Power Supply Group		RS				RN				LS				LN																				
FSVH2104	XCVU33P	224	225	226	227					124	125	126	127																					
	XCVU35P	224	225	226	227	228	229	230	231	124	125	126	127	128	129	130	131																	
	XCVU45P	224	225	226	227	228	229	230	231	124	125	126	127	128	129	130	131																	
Power Supply Group		RC			RN			RS																										
FLGB2377	XCVU440	224	225	226	231	232	233	221	222	223																								233, 232, 231, 226, 225, 224, 223, 222, 221

Table 1-10: **Transceiver Quad Migration (GTH Quads are White, GTY Quads are Gray, GTM Duals are Dark Gray)** ***(Cont'd)***

Package	Device	Package to Device Transceiver Mapping																																Unbonded GT Quads
		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	
Power Supply Group		RLC			RUC				RN				RS				RLC	LLC			LUC				LN				LS				LLC	
FLGA2577	XCVU190	224	225	226	227	228	229	230	231	232	233		219	220	221	222	223	124	125	126	127	128	129	130	131	132	133		119	120	121	122	123	
	XCVU9P	224	225	226	227	228	229	230	231	232	233		219	220	221	222	223	124	125	126	127	128	129	130	131	132	133		119	120	121	122	123	
	XCVU11P	225	226	227	228	229	230	231	232	233	234	235					224	125	126	127	128	129	130	131	132	133	134	135					124	
	XCVU13P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124	
FSGA2577	XCVU13P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124	
	XCVU27P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124	
	XCVU29P	225	226	227	228	229	230	231	232	233	234	235	220	221	222	223	224	125	126	127	128	129	130	131	132	133	134	135	120	121	122	123	124	
Power Supply Group		RC				RN				RS																								
FLGA2892	XCVU440	224	225	226	227	229	230	231	232	219	220	221	222																					233, 228, 223
Power Supply Group		RS				RC				RN				LS				LC				LN												
FSVH2892	XCVU35P	224	225	226	227	228	229	230	231					124	125	126	127	128	129	130	131													
	XCVU37P	224	225	226	227	228	229	230	231	232	233	234	235	124	125	126	127	128	129	130	131	132	133	134	135									
	XCVU45P	224	225	226	227	228	229	230	231					124	125	126	127	128	129	130	131													
	XCVU47P	224	225	226	227	228	229	230	231	232	233	234	235	124	125	126	127	128	129	130	131	132	133	134	135									
Power Supply Group		RS				RC				RN				LS				LC				LN												
FSVK2892	XCVU57P	224	225	226	227	228	229	230	231	232	233	234	235	124	125	126	127	128	129	130	131	132	133	134	135									
Power Supply Group		RLC			RUC			RN			RS																							
FSVA3824	XCVU19P	225	226	227	230	231	232	235	236	237	220	221	222																					238, 234, 233, 229, 228, 224, 223, 219
Power Supply Group		RLC					RUC					RN					RS																	
FSVB3824	XCVU19P	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	219	220	221	222	223													

Die Level Bank Numbering Overview

Banking and Clocking Summary

- For each device, not all banks are bonded out in every package.

GTH/GTY/GTM Columns

- One GTH/GTY Quad = Four transceivers = Four GTHE3 or GTYE3 primitives.
- One GTM Dual = Two transceivers = Two GTME3 primitives
- Not all GT Quads/Duals are bonded out in every package.
- Also shown are quads/duals labeled with RCAL. This specifies the location of the RCAL masters for each device. With respect to the package, the RCAL masters are located on the same package pin for each package, regardless of the device.
- The XY coordinates shown in each quad/dual correspond to the transceiver channel number found in the pin names for that quad/dual, as shown in Figure 1-1.
- An alphabetic designator is shown in each quad/dual. Each letter corresponds to the columns in Table 1-8 and Table 1-10.
- The power supply group is shown in brackets [ ] for each quad/dual.

I/O Banks

- Each user I/O bank has a total of 52 I/Os where 48 can be used as differential (24 differential pairs) or single-ended I/Os. The remaining four function only as single-ended I/Os. All 52 pads of a bank are not always bonded out to pins.
- A limited number of banks have fewer than 52 SelectIO pins. These banks are labeled as partial.
- Adjacent to each bank is a physical layer (PHY) containing a CMT and other clock resources.
- Adjacent to each bank and PHY is a tile of logic resources that makes up a clock region.
- Banks are arranged in columns and separated into rows which are pitch-matched with adjacent PHY, clock regions, and GT blocks.
- An alphabetic designator is shown in each bank. Each letter corresponds to the columns in Table 1-8 and Table 1-10.

Clocking

- Each bank has four pairs of global clock (GC) inputs for four differential or four single-ended clock inputs. Single-ended clock inputs should be connected to the P side of the differential pair.
- Clock signals are distributed through global buffers driving routing and distribution networks to reach any clock region, I/O, or GT.
- Global clock inputs can connect to an MMCM and two PLLs within the horizontally adjacent CMT.

Bank Locations of Dedicated and Multi-Function Pins

- In all UltraScale and UltraScale+ devices, bank 65 contains the multi-function configuration pins. Bank 0 contains the dedicated configuration pins.
- In Figure 1-2 through Figure 1-135, the multi-function configuration bank 65 is shown adjacent to the SYSMON/CFG blocks. For devices with multiple super logic regions (SLRs), banks 60 and 70 are also shown adjacent to the SYSMON/CFG blocks. Due to the architectural differences between these and other banks, special consideration must be taken when using them under certain conditions. See the *State of I/Os During and After Configuration* and the *Special DCI Requirements in Some Banks* sections of *UltraScale Architecture SelectIO Resources User Guide* (UG571) for details.
- For UltraScale devices, all dedicated configuration I/Os (bank 0) and HR I/Os are 1.5V to 3.3V capable.
- For UltraScale+ devices, all dedicated configuration I/Os (bank 0) and HR I/Os are 1.5V to 1.8V capable.

SYSMON, Configuration, PCIe, Interlaken, and 100GE Integrated Blocks

- CFG: Configuration block
- SYSMON/CFG: Block shared between SYSMON and configuration
- PCIe: Integrated block for PCIe

  Note: Do not connect the integrated block for PCIe to transceiver channels through an SLR crossing. For further details, refer to the *Placement Rules* section of the *UltraScale Devices Gen3 Integrated Block for PCI Express Product Guide* (PG156) and *UltraScale+ Devices Integrated Block for PCI Express Product Guide* (PG213). Blocks with an additional (Tandem) label support Tandem configuration.

- ILKN: Interlaken block

  Note: Do not connect the Interlaken block to transceiver channels through an SLR crossing. For further details, refer to the *Transceiver Interface* section of the *Integrated Interlaken 150G Product Guide* (PG169).

- CMAC: 100G Ethernet block

  Note: Do not connect the 100G Ethernet block to transceiver channels through an SLR crossing. For further details, refer to the *Transceiver Selection Rules* section of the *UltraScale Devices Integrated Block for 100G Ethernet Product Guide* (PG165) or *UltraScale+ Devices Integrated 100G Ethernet Subsystem Product Guide* (PG203).

Device Diagrams

Figure 1-1 shows an example diagram with a brief explanation for each component.

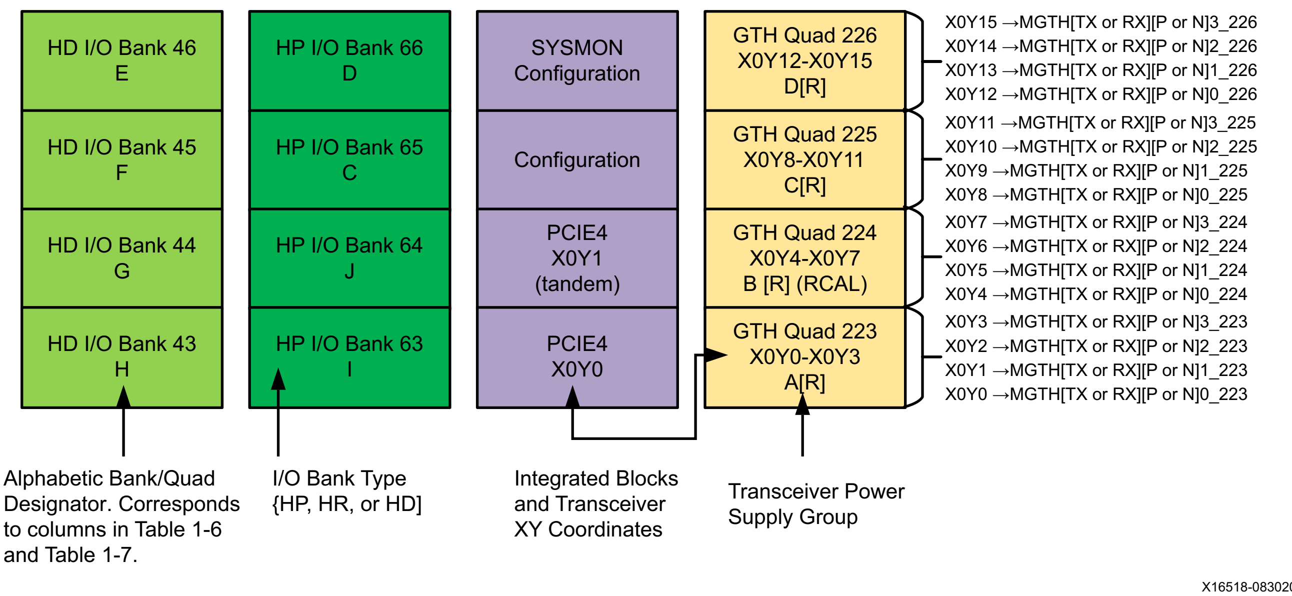

Figure 1-1: **Example Device Diagram**

TIP: *Due to design limitations, the device resources might be less than what is shown in the device diagrams. The actual available resources by device and package are listed in the UltraScale Architecture and Product Overview (DS890).*

The following figures show a die view of each device followed by a view with respect to each available package.

XCKU025 Bank Diagrams

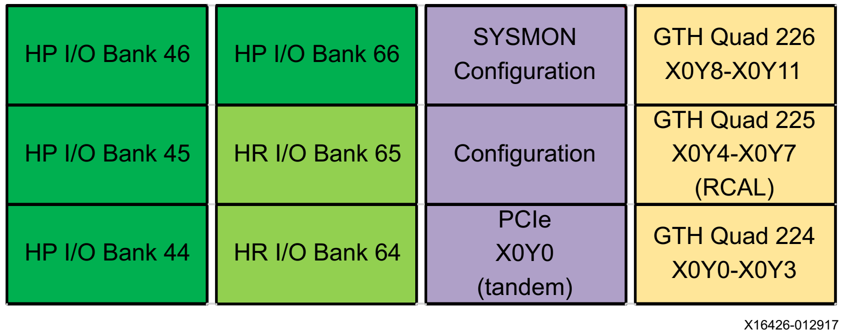

Figure 1-2: **XCKU025 Banks**

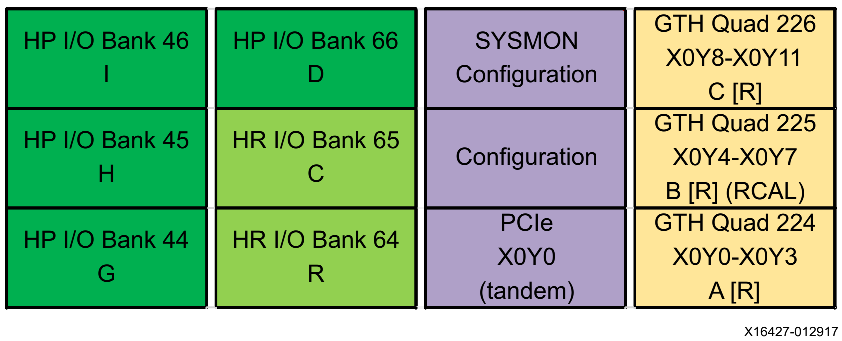

Figure 1-3: **XCKU025 Banks in FFVA1156 Package**

XCKU035 Bank Diagrams

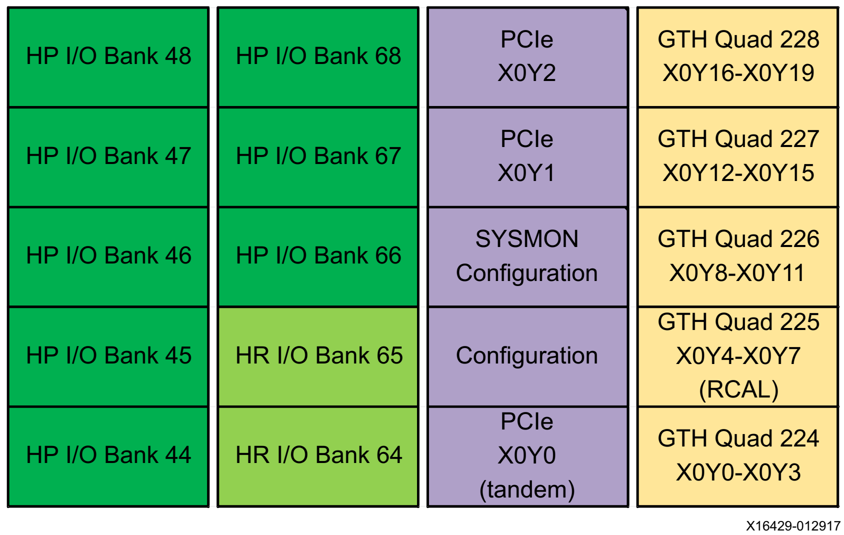

Figure 1-4: **XCKU035 Banks**

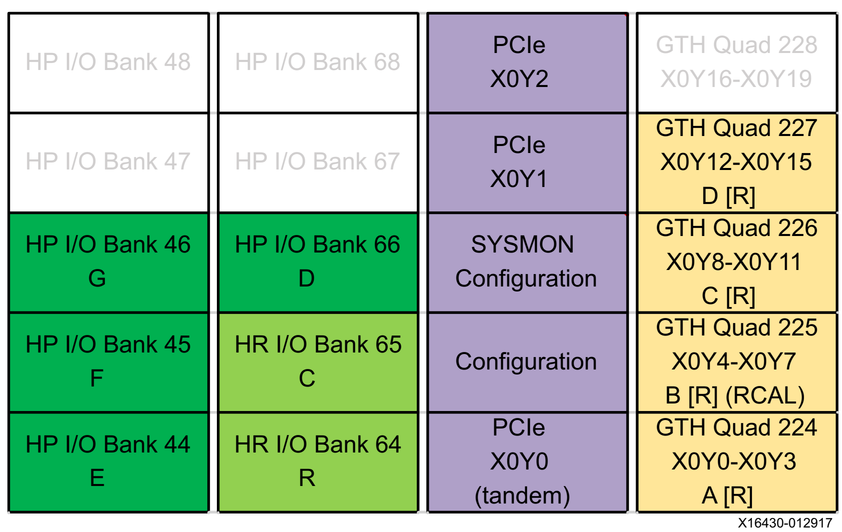

Figure 1-5: **XCKU035 Banks in FBVA676 Package**

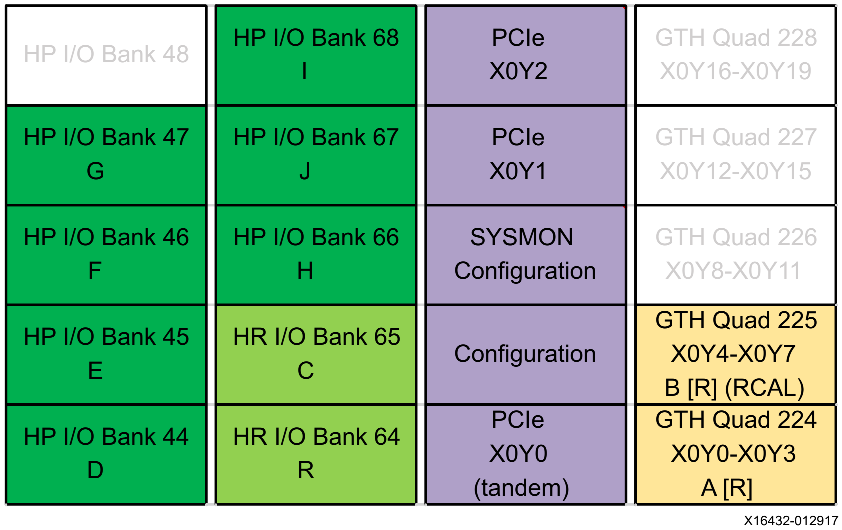

Figure 1-6: **XCKU035 Banks in SFVA784 Package**

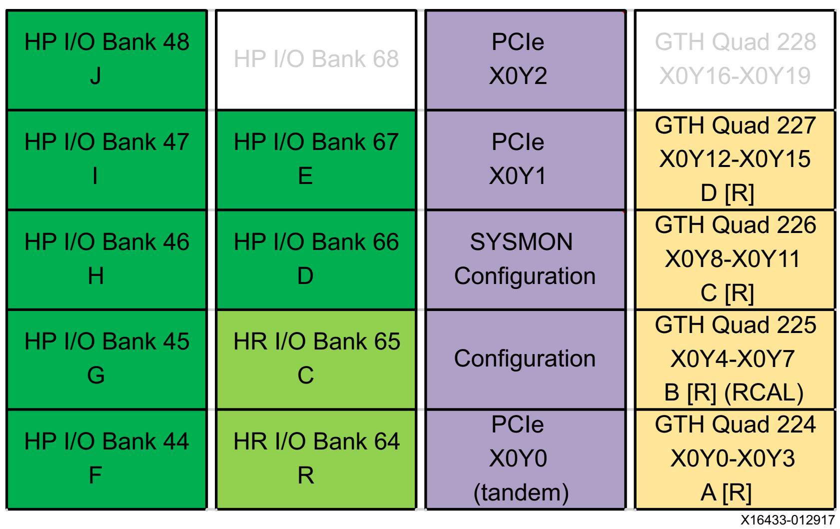

Figure 1-7: **XCKU035 Banks in FBVA900 Package**

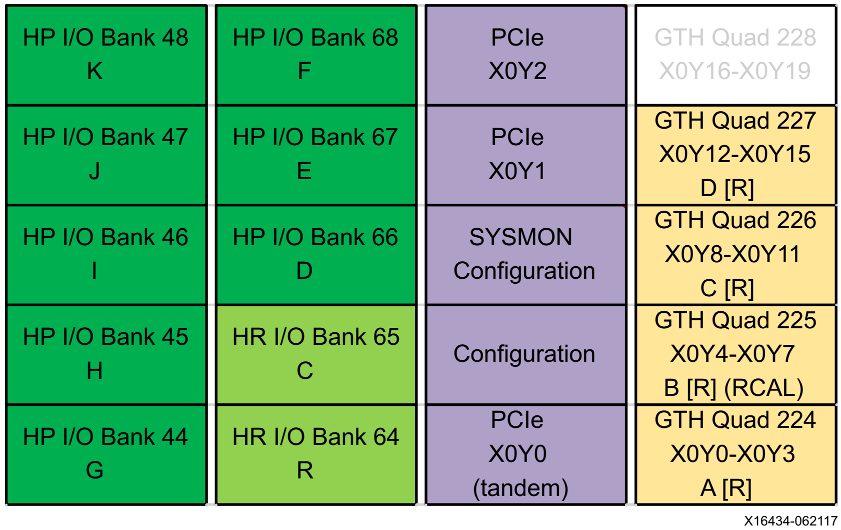

Figure 1-8: **XCKU035 Banks in FFVA1156 Package**

XCKU040 and XQKU040 Bank Diagrams

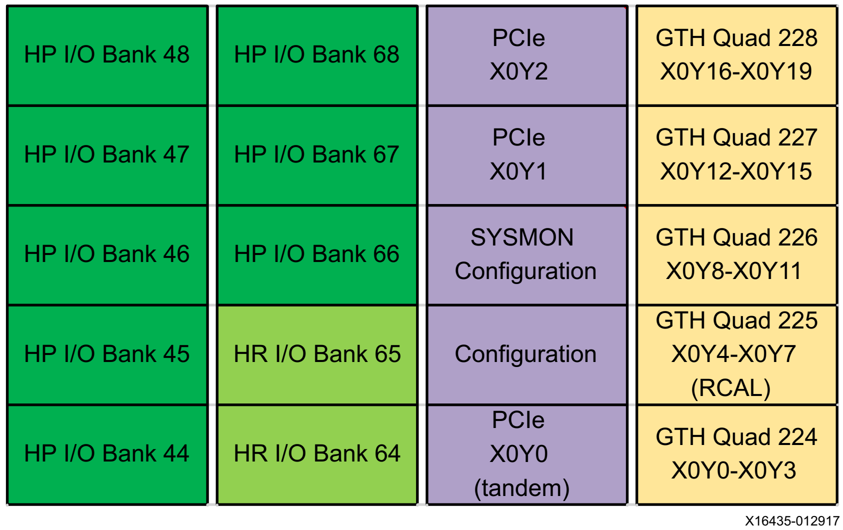

Figure 1-9: **XCKU040 and XQKU040 Banks**

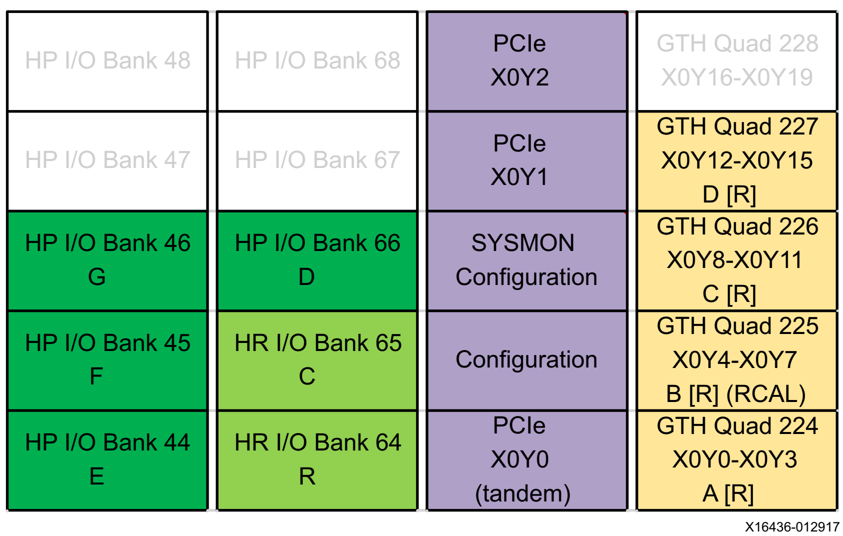

Figure 1-10: **XCKU040 Banks in FBVA676 Package and XQKU040 Banks in RBA676 Package**

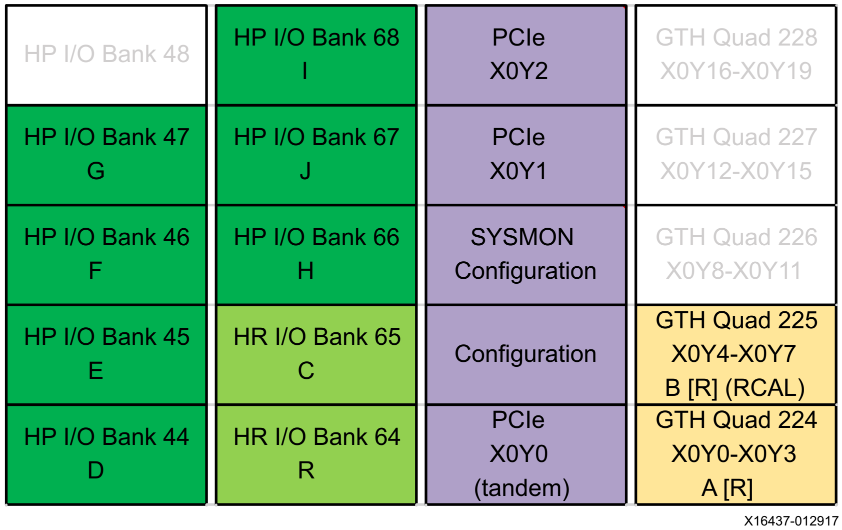

Figure 1-11: **XCKU040 Banks in SFVA784 Package**

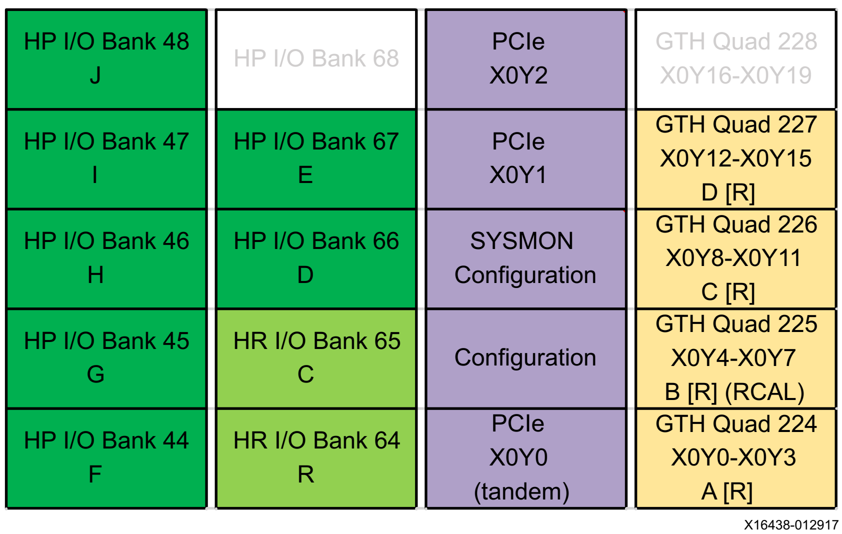

Figure 1-12: **XCKU040 Banks in FBVA900 Package**

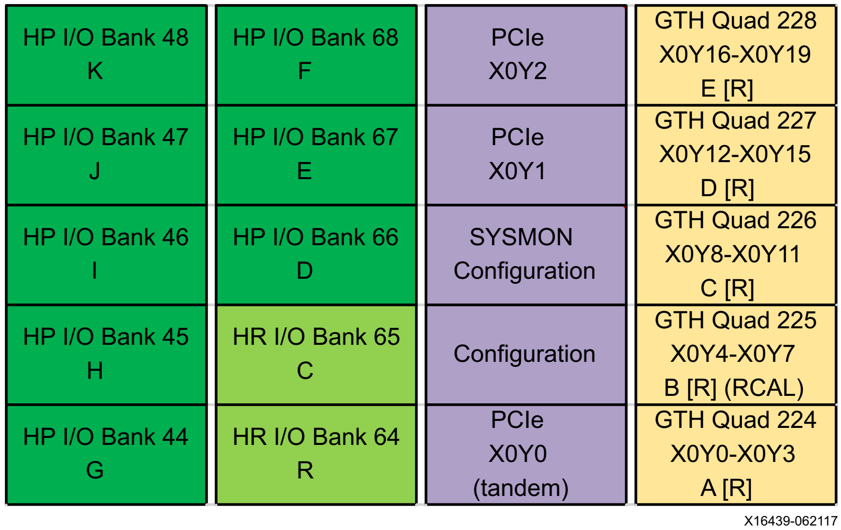

Figure 1-13: **XCKU040 Banks in FFVA1156 Package and XQKU040 in RFA1156 Package**

XCKU060 and XQKU060 Bank Diagrams

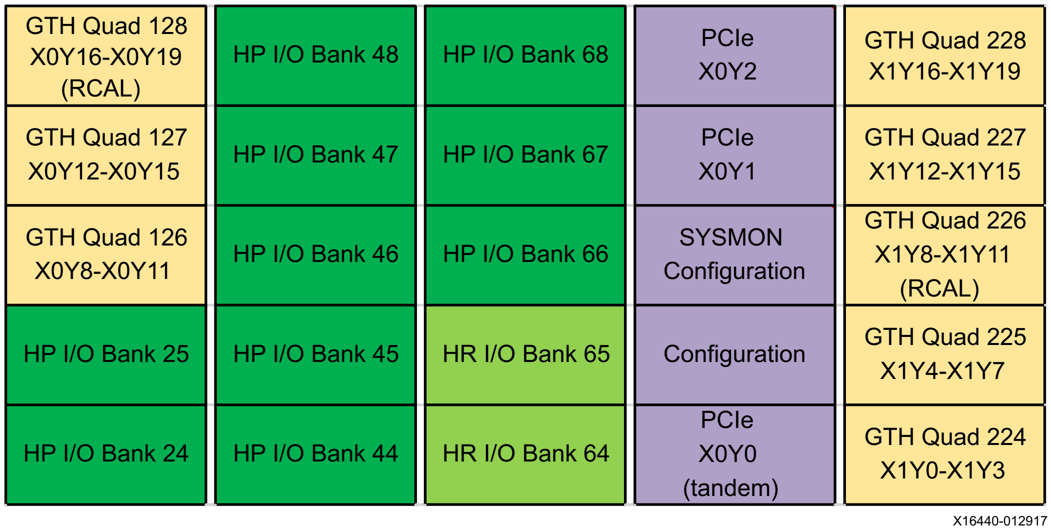

Figure 1-14: **XCKU060 and XQKU060 Banks**

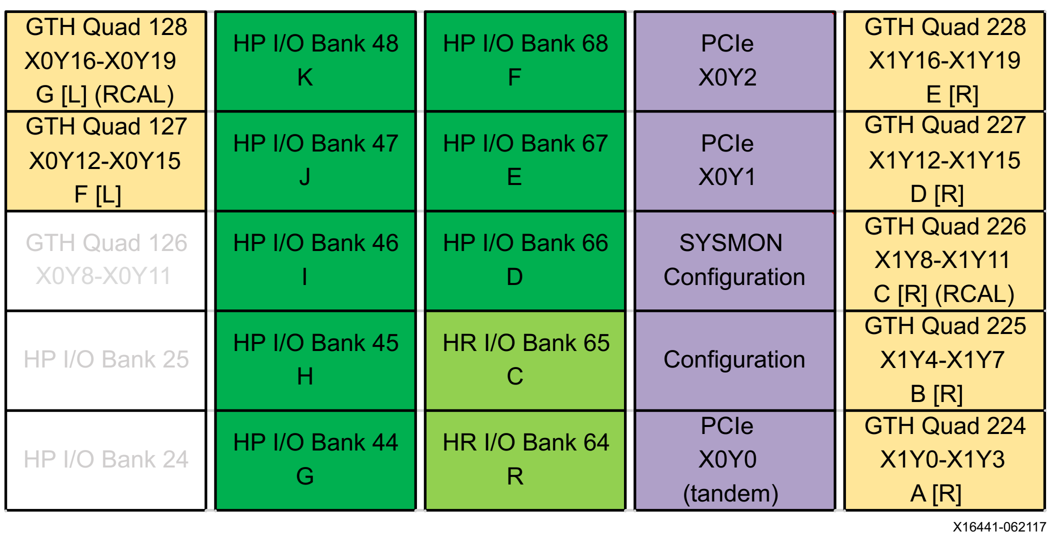

Figure 1-15: **XCKU060 Banks in FFVA1156 Package and XQKU060 Banks in RFA1156 Package**

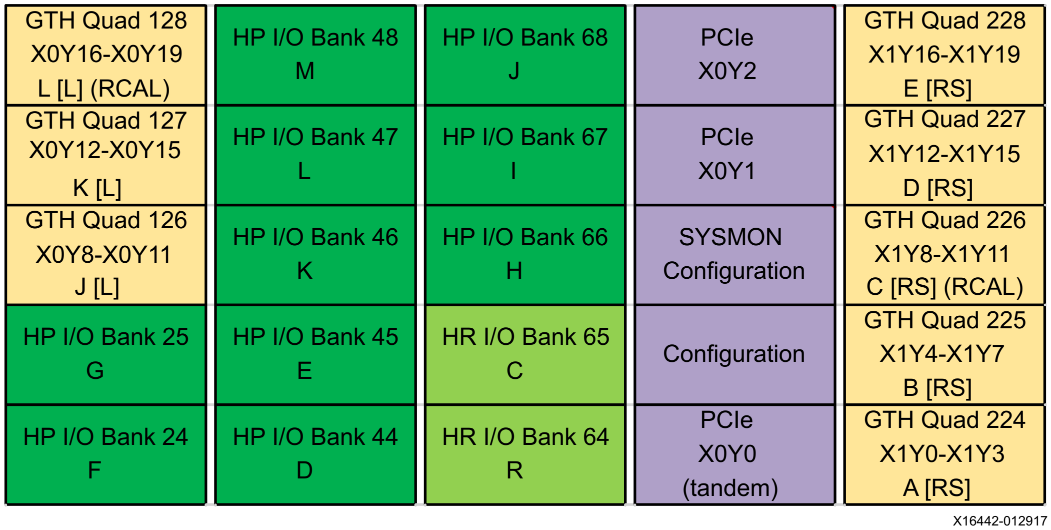

Figure 1-16: **XCKU060 Banks in FFVA1517 Package**

XCKU085 Bank Diagrams

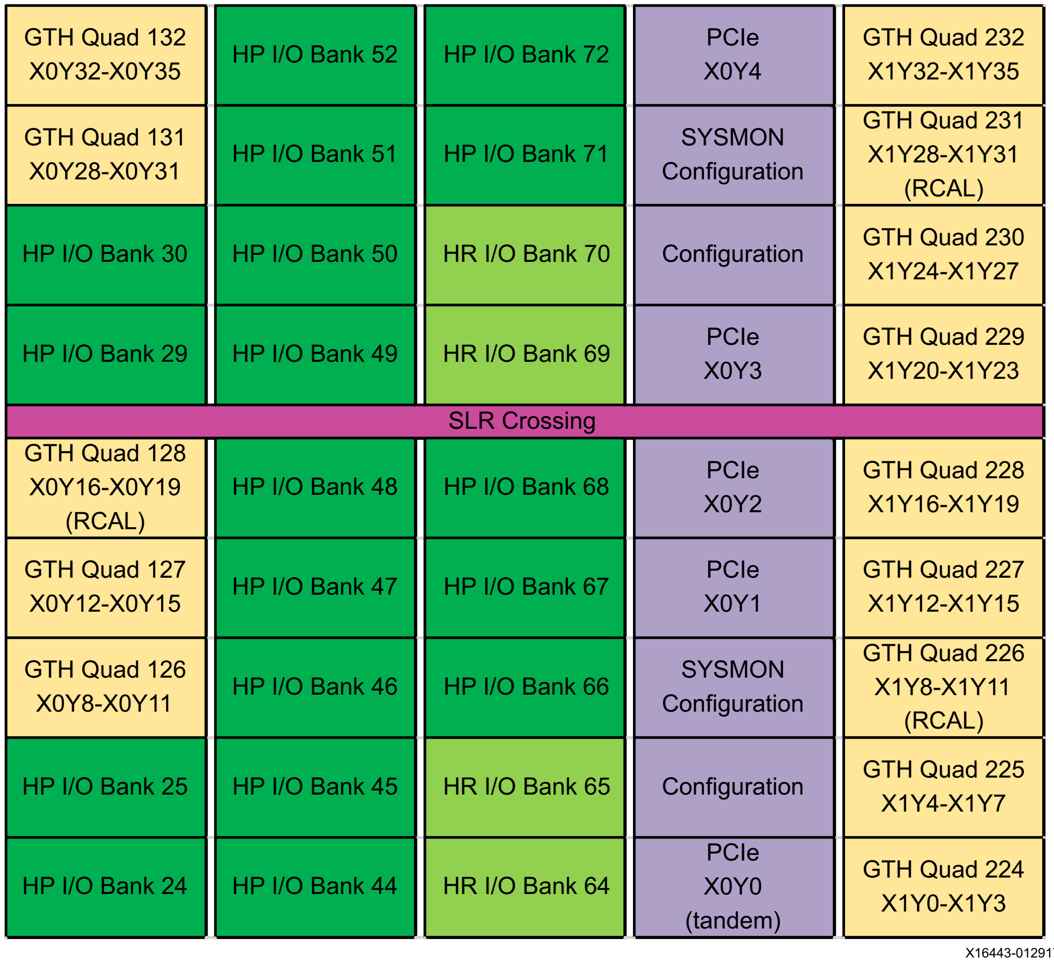

Figure 1-17: **XCKU085 Banks**

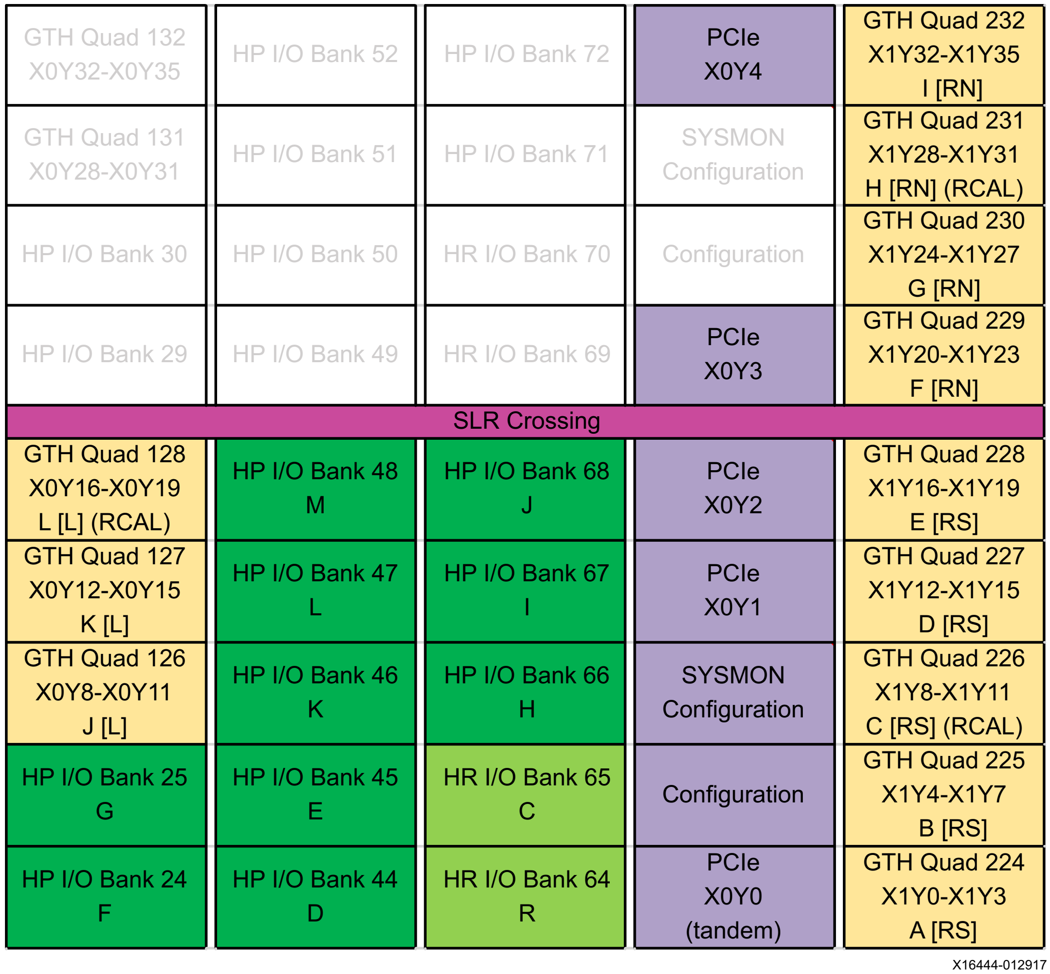

Figure 1-18: **XCKU085 Banks in FLVA1517 Package**

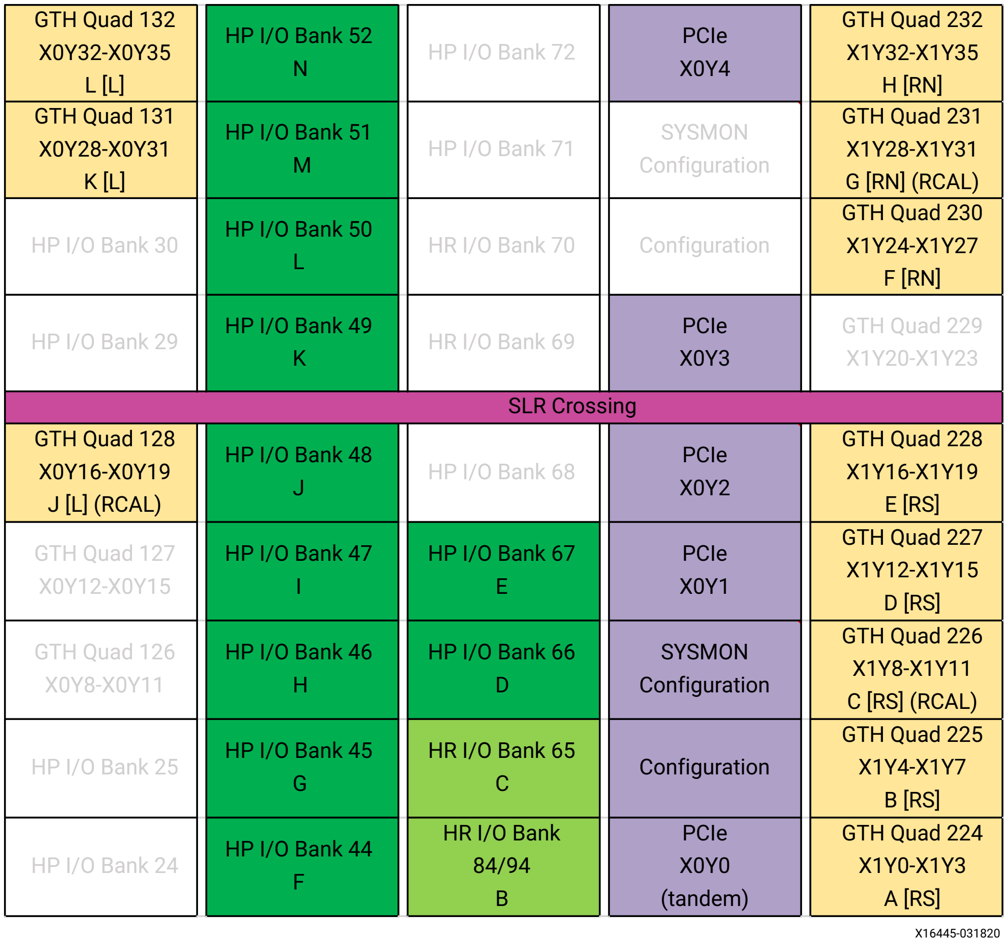

Figure 1-19: **XCKU085 Banks in FLVB1760 Package**

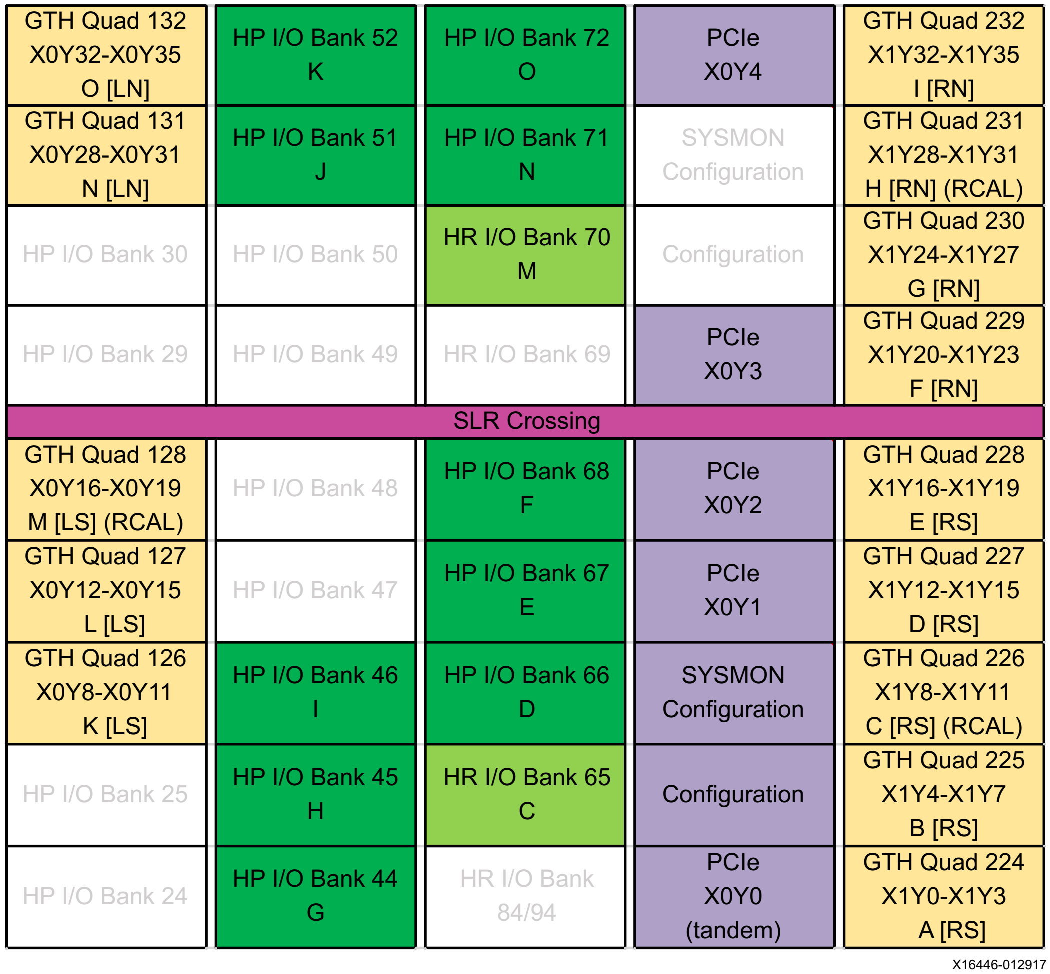

Figure 1-20: **XCKU085 Banks in FLVF1924 Package**

XCKU095 and XQKU095 Bank Diagrams

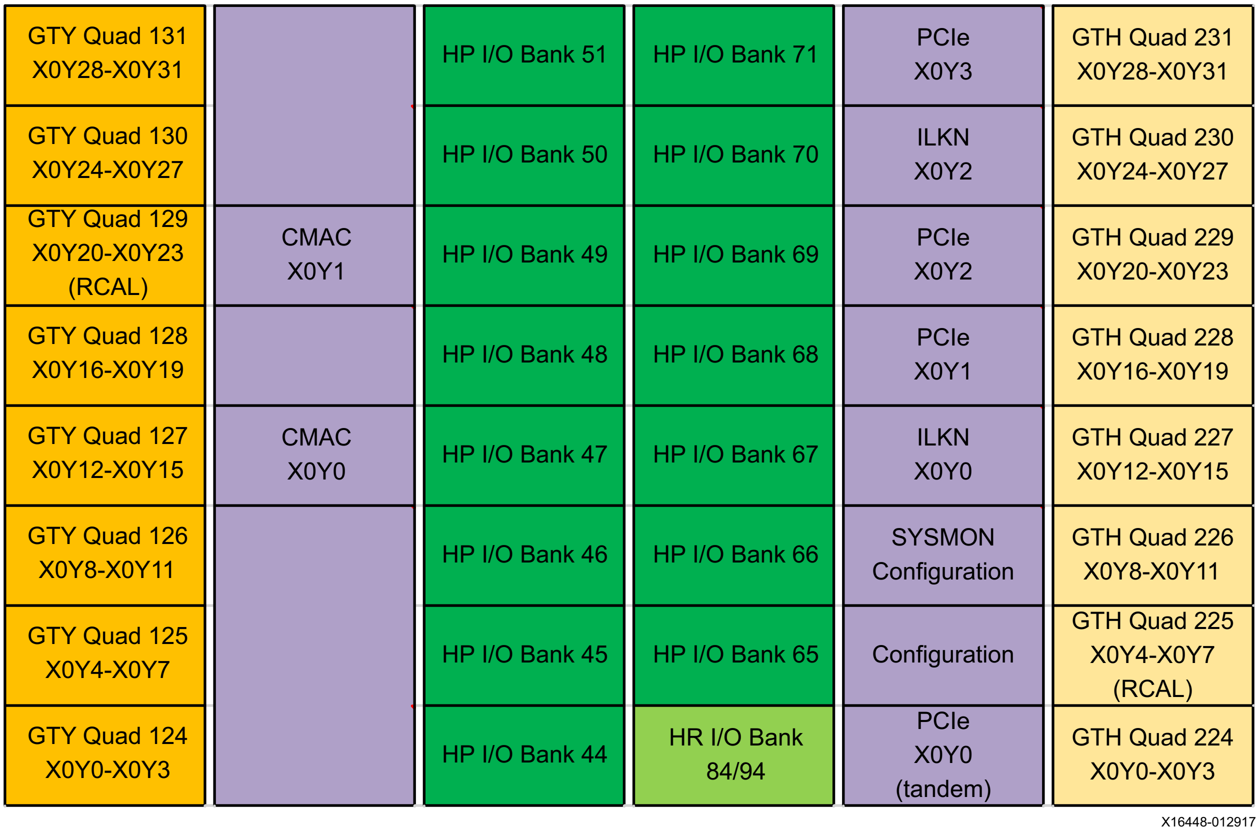

Figure 1-21: **XCKU095 and XQKU095 Banks**

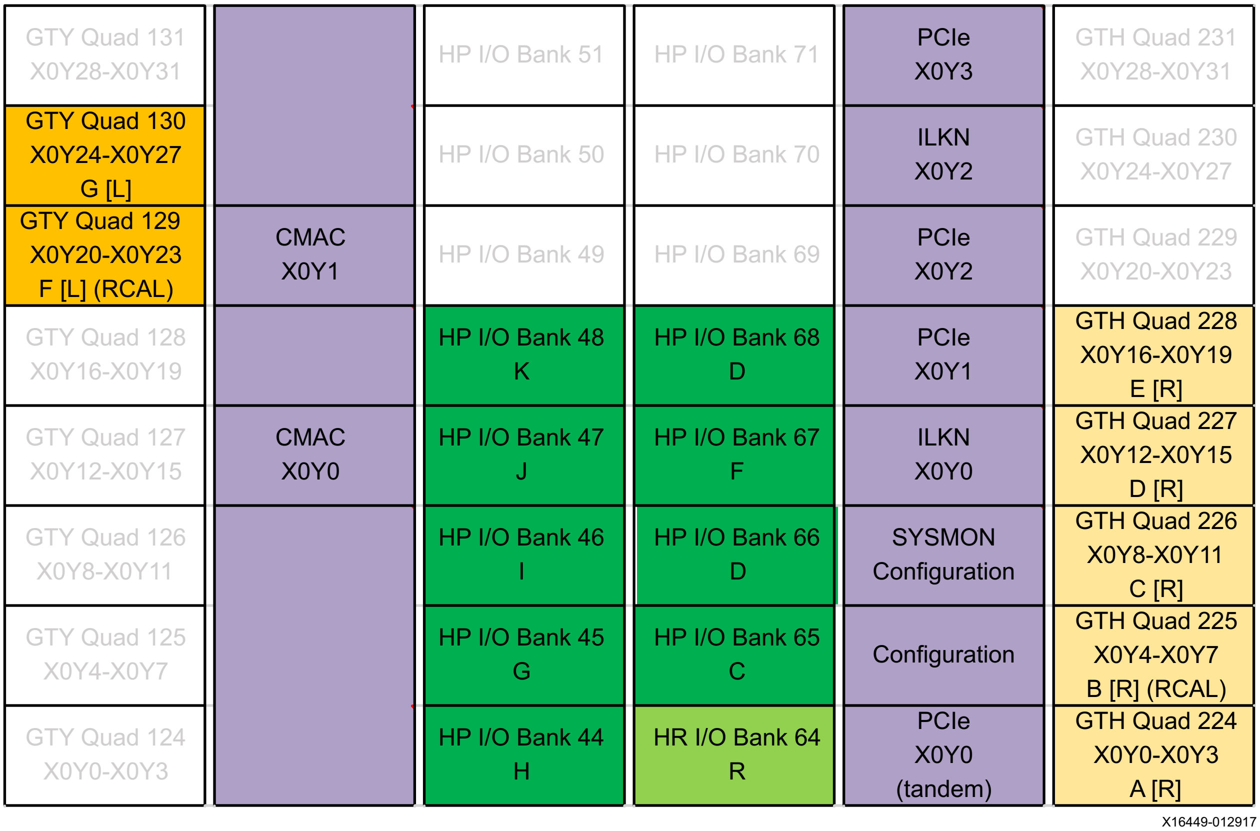

Figure 1-22: **XCKU095 Banks in FFVA1156 Package and XQKU095 in RFA1156 Package**

GTY Quad 131 X0Y28-X0Y31		HP I/O Bank 51	HP I/O Bank 71	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y24-X0Y27		HP I/O Bank 50	HP I/O Bank 70	ILKN X0Y2	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y20-X0Y23 J [L] (RCAL)	CMAC X0Y1	HP I/O Bank 49	HP I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23
GTY Quad 128 X0Y16-X0Y19 I [L]		HP I/O Bank 48 K	HP I/O Bank 68 F	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [R]
GTY Quad 127 X0Y12-X0Y15 H [L]	CMAC X0Y0	HP I/O Bank 47 J	HP I/O Bank 67 E	ILKN X0Y0	GTH Quad 227 X0Y12-X0Y15 D [R]
GTY Quad 126 X0Y8-X0Y11 G [L]		HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R]
GTY Quad 125 X0Y4-X0Y7 F [L]		HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R] (RCAL)
GTY Quad 124 X0Y0-X0Y3		HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

X16450-012917

Figure 1-23: **XCKU095 Banks in FFVC1517 Package**

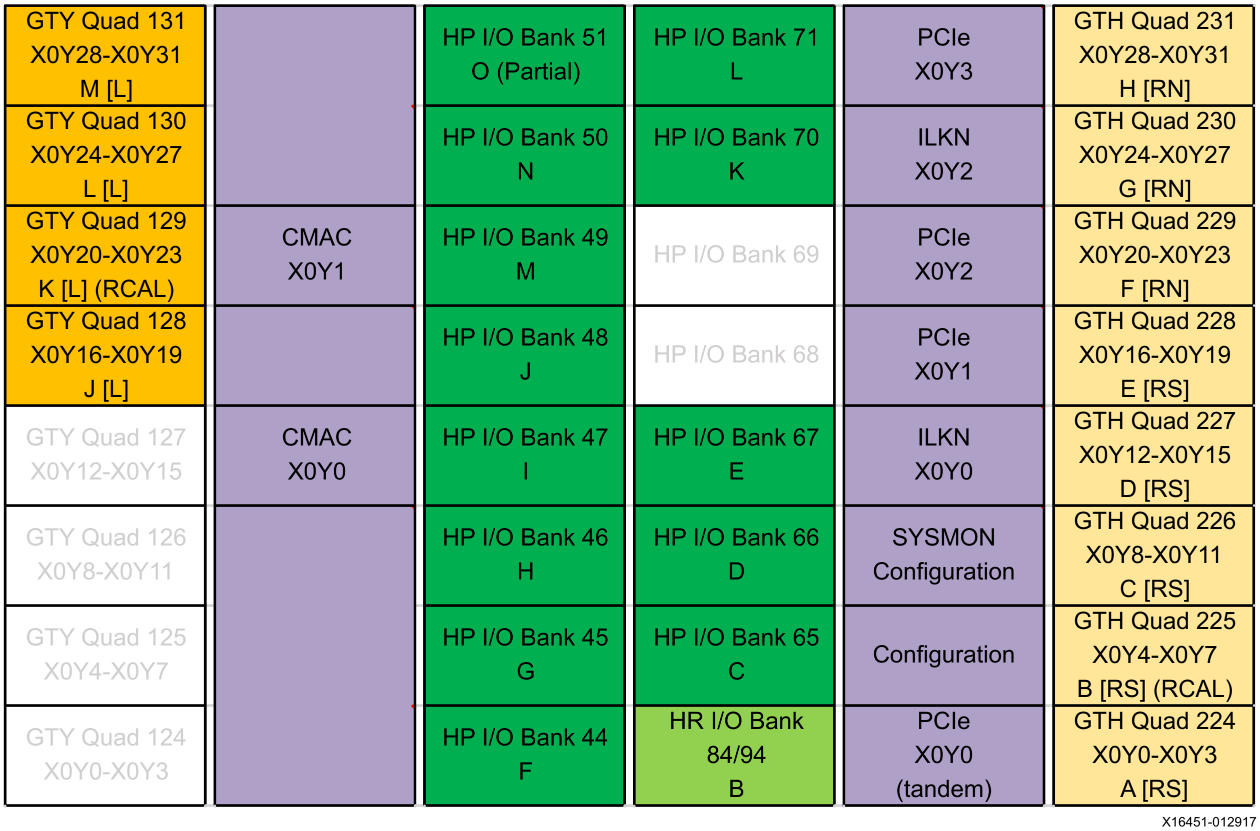

Figure 1-24: **XCKU095 Banks in FFVB1760 Package**

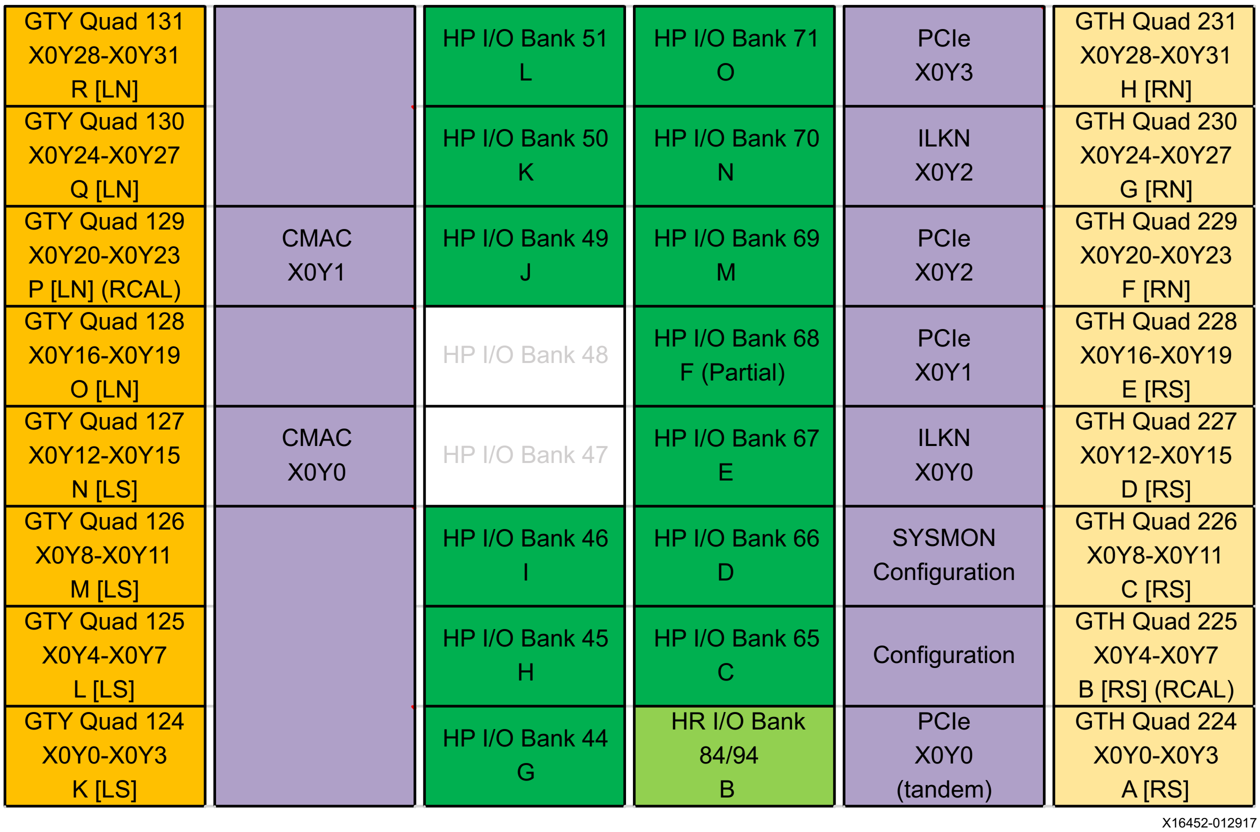

Figure 1-25: **XCKU095 Banks in FFVB2104 Package**

XCKU115 and XQKU115 Bank Diagrams

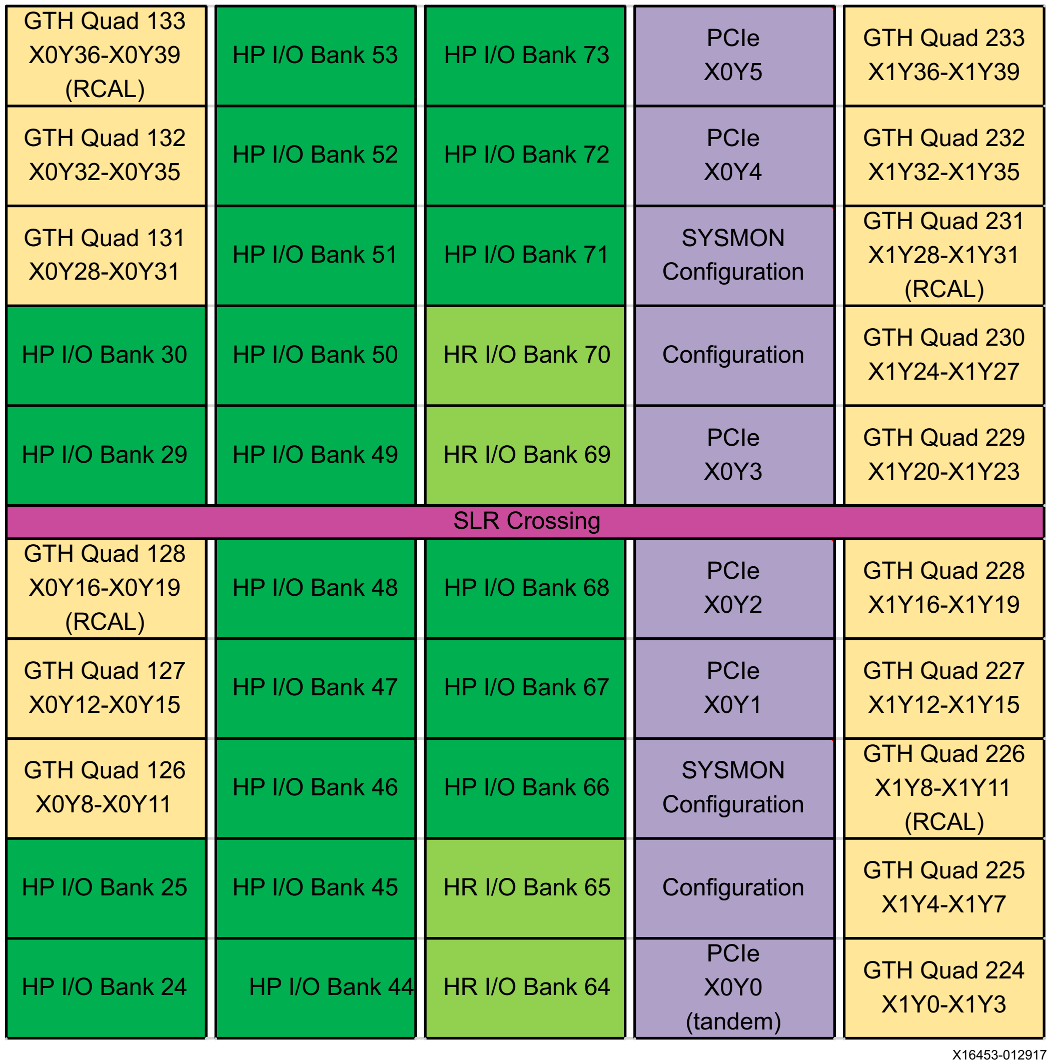

Figure 1-26: **XCKU115 and XQKU115 Banks**

TIP: *Bank 64 is labeled as 84/94 in some packages.*

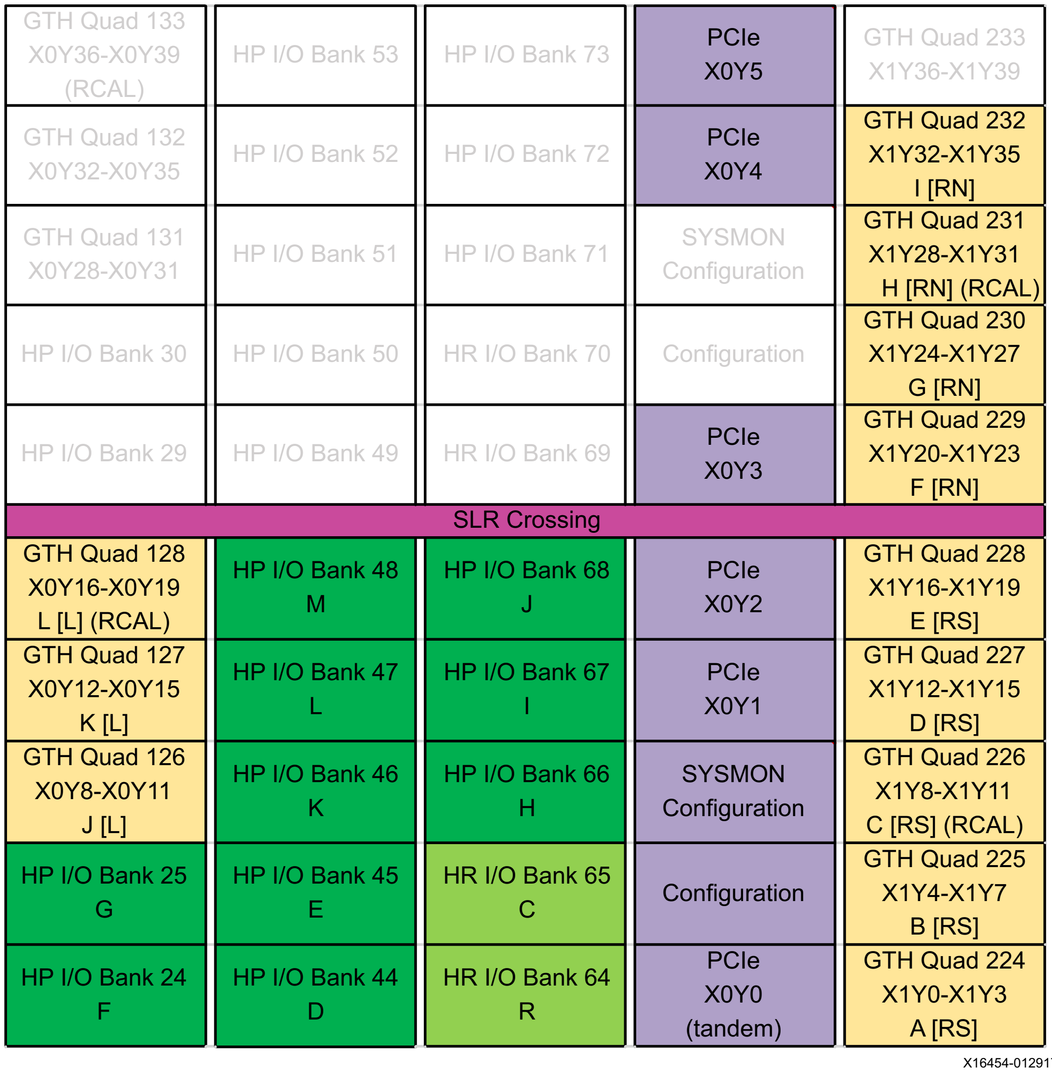

Figure 1-27: **XCKU115 Banks in FLVA1517 Package**

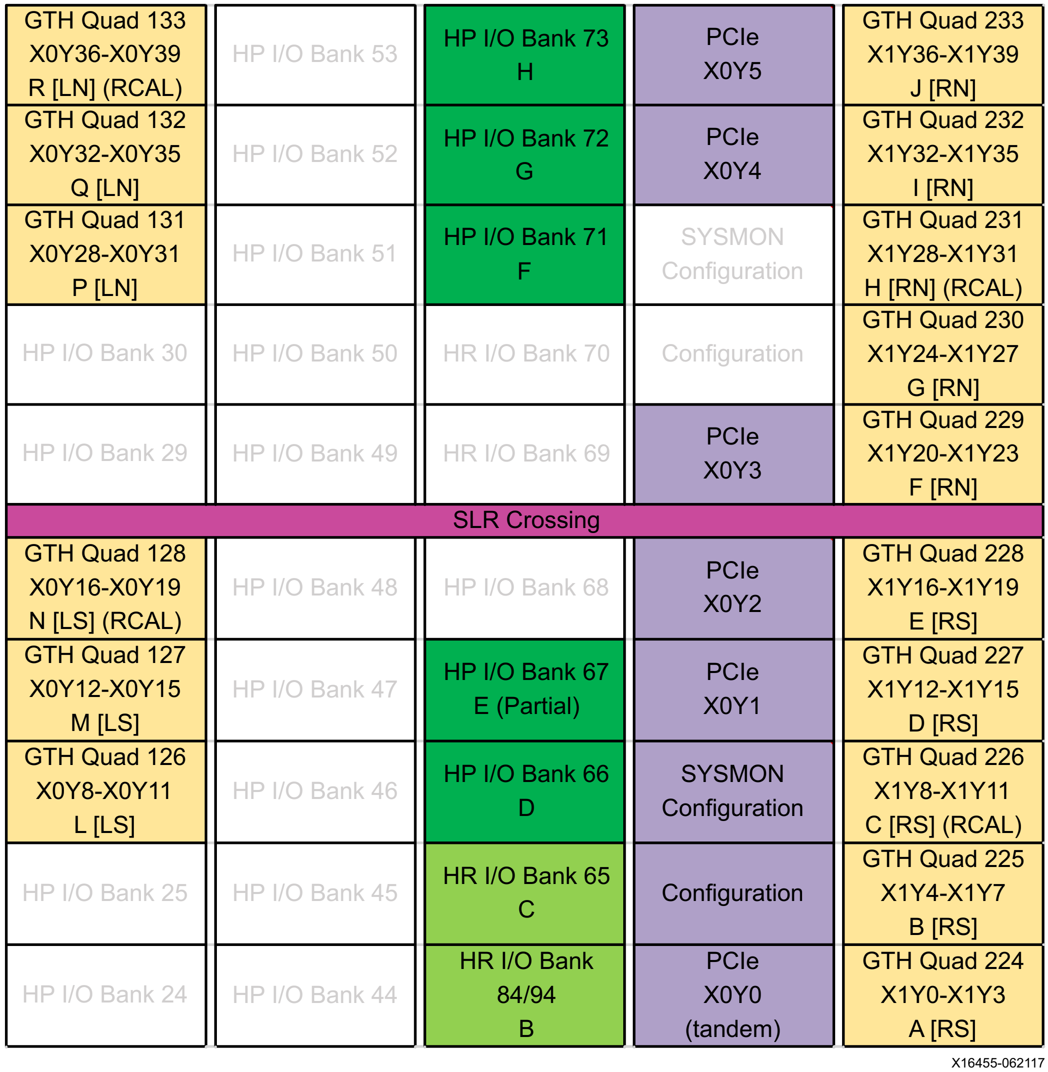

Figure 1-28: **XCKU115 Banks in FLVD1517 Package and XQKU115 in the RLD1517 Package**

TIP: *Bank 64 is labeled as 84/94 in some packages.*

Figure 1-29: **XCKU115 Banks in FLVB1760 Package**

TIP: *Bank 64 is labeled as 84/94 in some packages.*

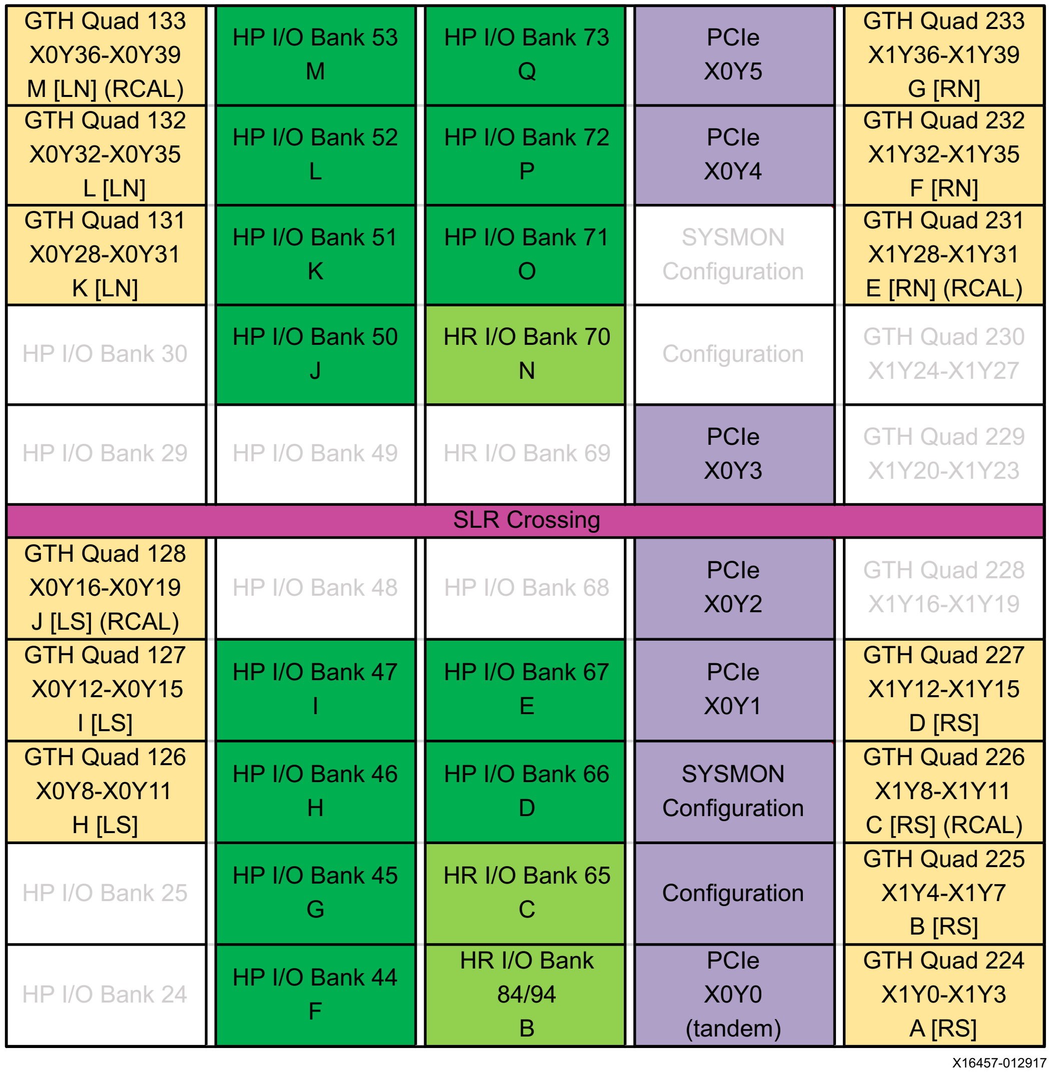

Figure 1-30: **XCKU115 Banks in FLVD1924 Package**

TIP: *Bank 64 is labeled as 84/94 in some packages.*

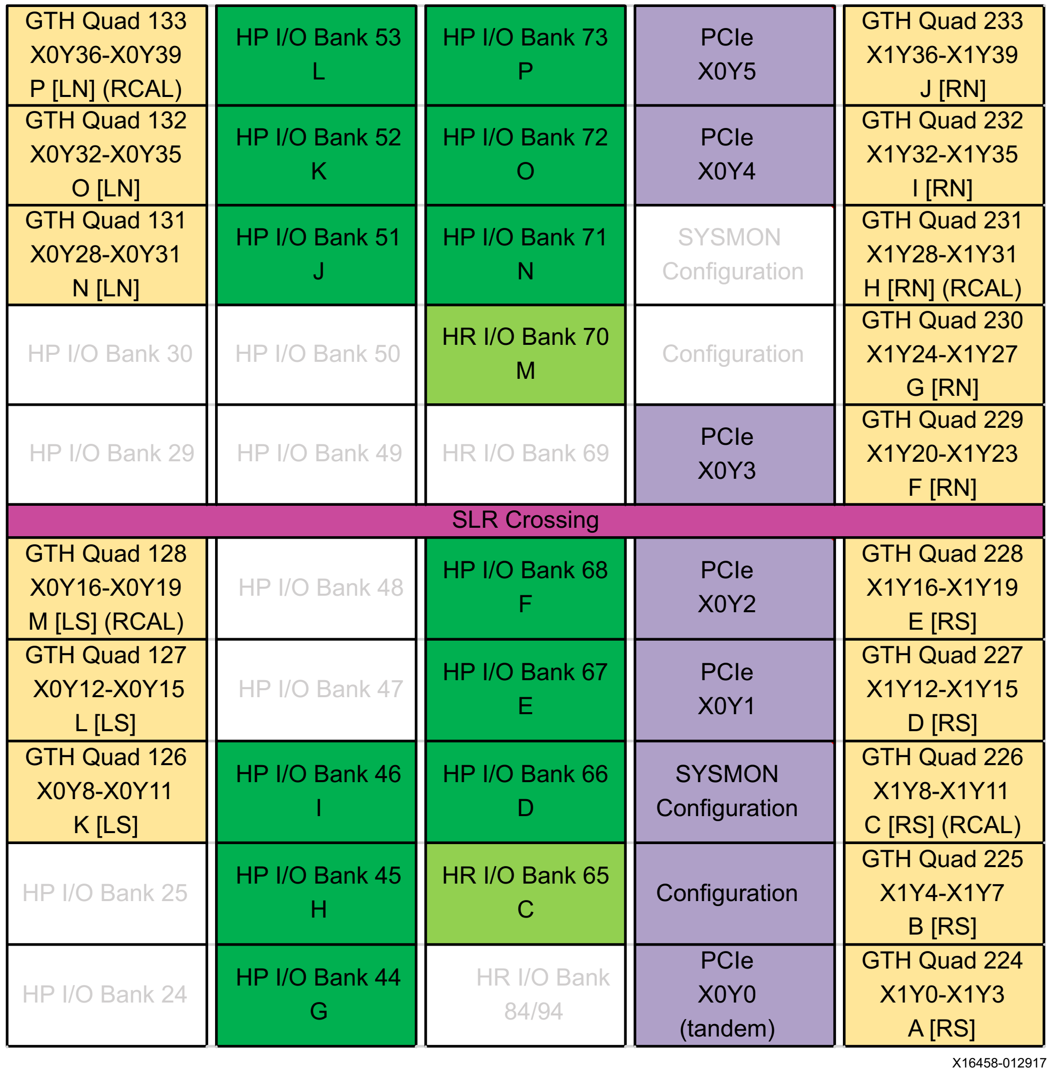

Figure 1-31: **XCKU115 Banks in FLVF1924 Package and XQKU115 Banks in RLF1924 Package**

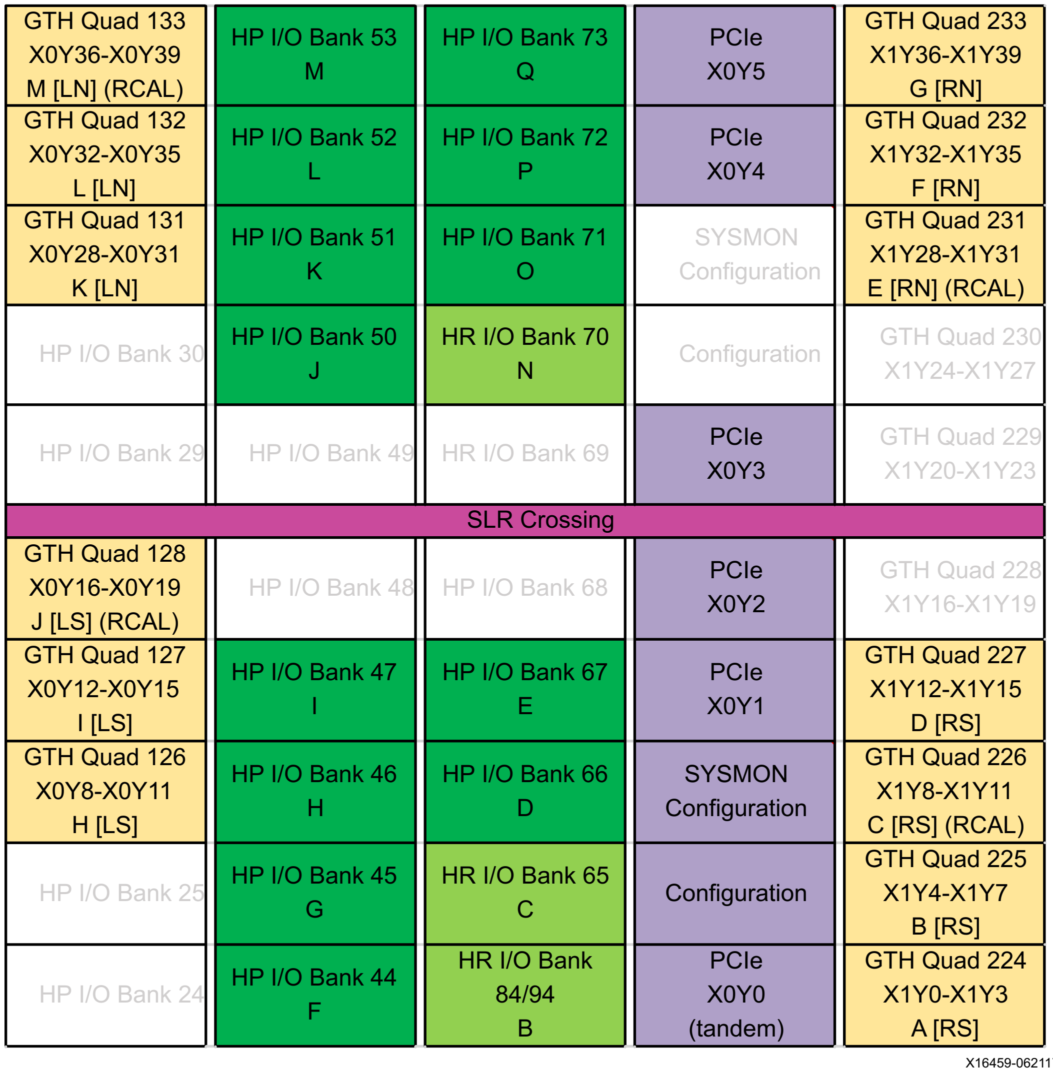

Figure 1-32: **XCKU115 Banks in FLVA2104 Package**

TIP: *Bank 64 is labeled as 84/94 in some packages.*

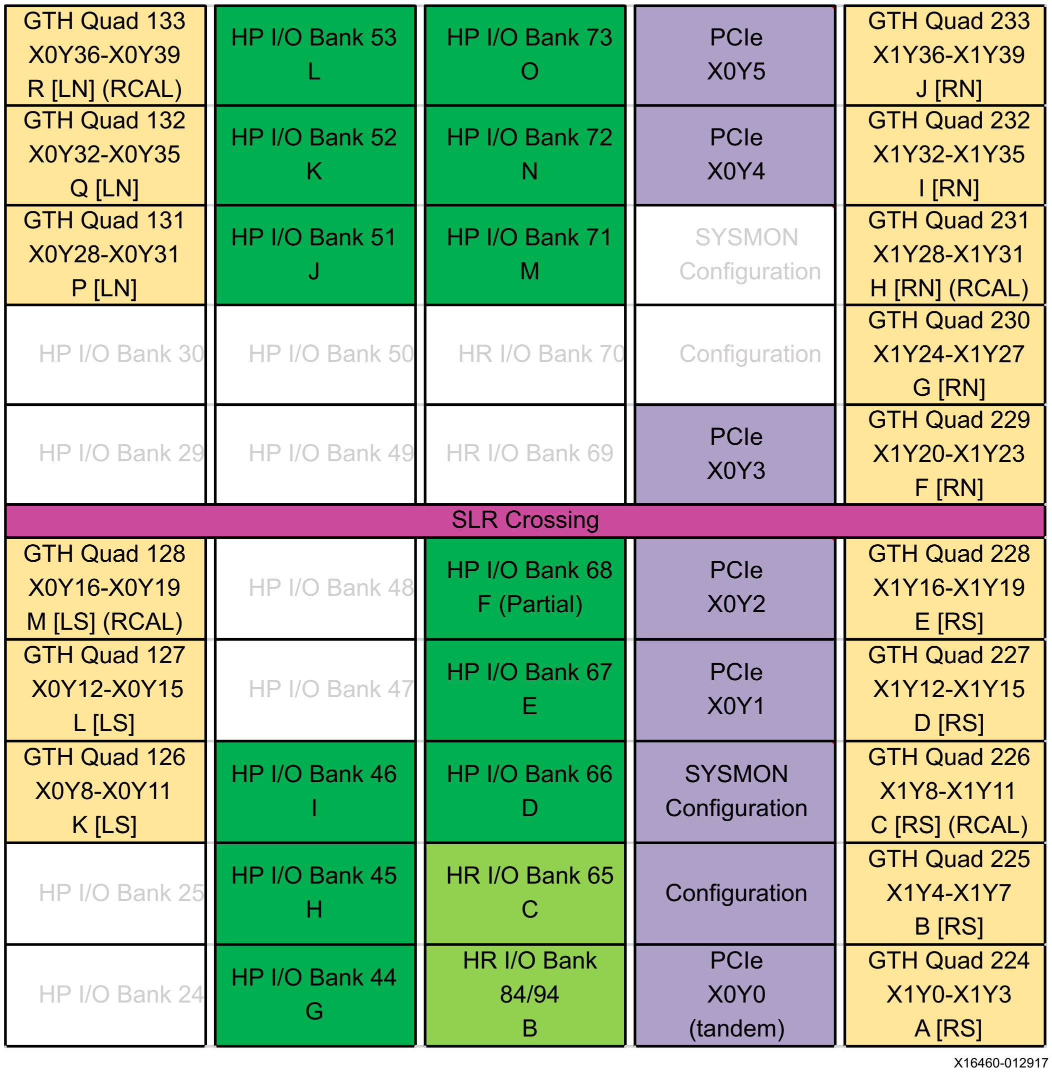

Figure 1-33: **XCKU115 Banks in FLVB2104 Package**

TIP: *Bank 64 is labeled as 84/94 in some packages.*

XCVU065 Bank Diagrams

GTY Quad 128 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19
GTY Quad 127 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15
GTY Quad 126 X0Y8-X0Y11	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 (RCAL)
GTY Quad 125 X0Y4-X0Y7 (RCAL)	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTH Quad 225 X0Y4-X0Y7
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3

X16466-012917

Figure 1-34: **XCVU065 Banks**

GTY Quad 128 X0Y16-X0Y19 J [L]	CMAC X0Y2	HP I/O Bank 48 K	HP I/O Bank 68 F	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [R]
GTY Quad 127 X0Y12-X0Y15 I [L]	CMAC X0Y1	HP I/O Bank 47 J	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [R]
GTY Quad 126 X0Y8-X0Y11 H [L]	ILKN X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R] (RCAL)
GTY Quad 125 X0Y4-X0Y7 G [L] (RCAL)	CMAC X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R]
GTY Quad 124 X0Y0-X0Y3 F [L]	ILKN X0Y0	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

X16467-062117

Figure 1-35: **XCVU065 Banks in FFVC1517 Package**

XCVU080 Bank Diagrams

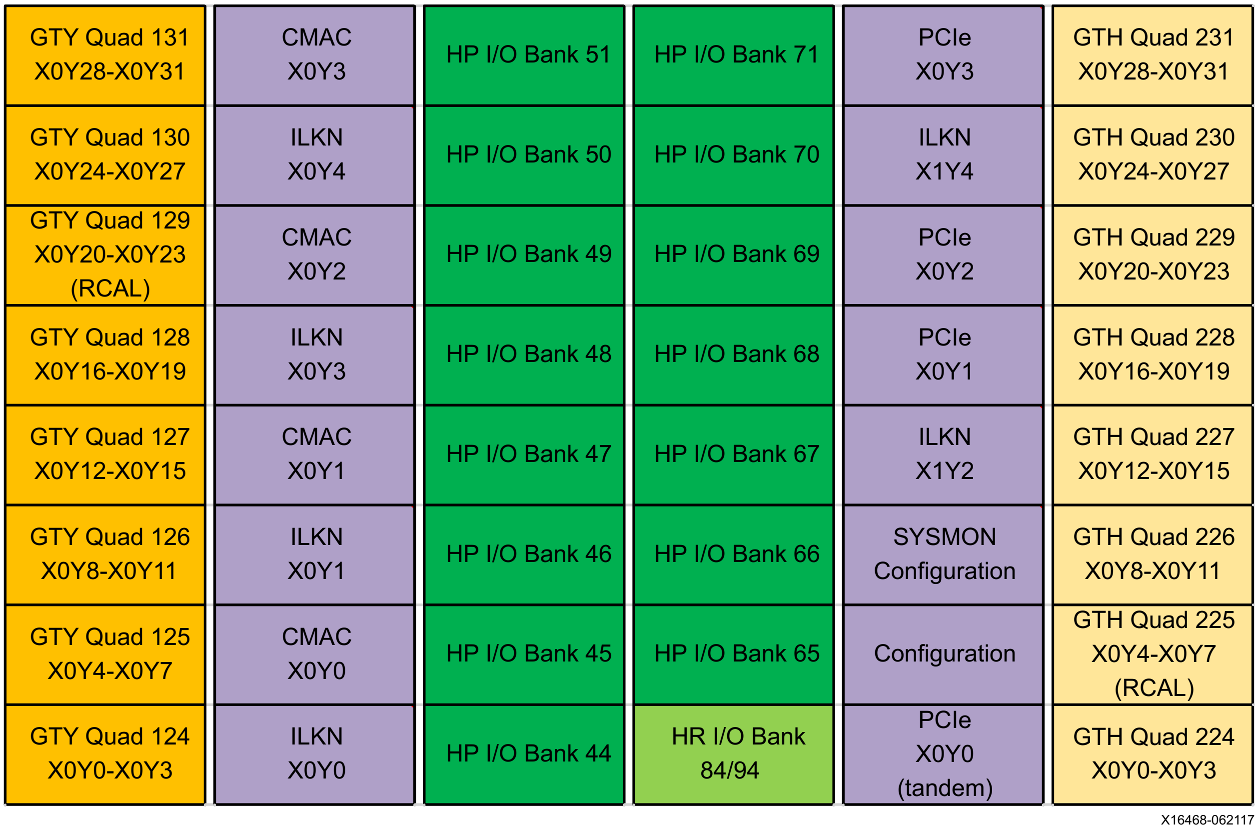

Figure 1-36: **XCVU080 Banks**

GTY Quad 131 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 51	HP I/O Bank 71	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y24-X0Y27	ILKN X0Y4	HP I/O Bank 50	HP I/O Bank 70	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y20-X0Y23 J [L] (RCAL)	CMAC X0Y2	HP I/O Bank 49	HP I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23
GTY Quad 128 X0Y16-X0Y19 I [L]	ILKN X0Y3	HP I/O Bank 48 K	HP I/O Bank 68 F	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [R]
GTY Quad 127 X0Y12-X0Y15 H [L]	CMAC X0Y1	HP I/O Bank 47 J	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [R]
GTY Quad 126 X0Y8-X0Y11 G [L]	ILKN X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R]
GTY Quad 125 X0Y4-X0Y7 F [L]	CMAC X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R] (RCAL)
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

X16469-062117

Figure 1-37: **XCVU080 Banks in FFVC1517 Package**

GTY Quad 131 X0Y28-X0Y31 R [LN]	CMAC X0Y3	HP I/O Bank 51	HP I/O Bank 71 H	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 Q [LN]	ILKN X0Y4	HP I/O Bank 50	HP I/O Bank 70 G	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 P [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49	HP I/O Bank 69 F	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 O [LN]	ILKN X0Y3	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15 N [LS]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E (Partial)	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 M [LS]	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 L [LS]	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3 K [LS]	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-38: **XCVU080 Banks in FFVD1517 Package**

GTY Quad 131 X0Y28-X0Y31 M [L]	CMAC X0Y3	HP I/O Bank 51 O (Partial)	HP I/O Bank 71 L	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 L [L]	ILKN X0Y4	HP I/O Bank 50 N	HP I/O Bank 70 K	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 K [L] (RCAL)	CMAC X0Y2	HP I/O Bank 49 M	HP I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 J [L]	ILKN X0Y3	HP I/O Bank 48 J	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 47 I	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11	ILKN X0Y1	HP I/O Bank 46 H	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7	CMAC X0Y0	HP I/O Bank 45 G	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 F	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-39: **XCVU080 Banks in FFVB1760 Package**

GTY Quad 131 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 51 M	HP I/O Bank 71 Q	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y24-X0Y27 M [LN]	ILKN X0Y4	HP I/O Bank 50 L	HP I/O Bank 70 P	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 L [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49 K	HP I/O Bank 69 O	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 K [LN]	ILKN X0Y3	HP I/O Bank 48 J	HP I/O Bank 68 N	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RN]
GTY Quad 127 X0Y12-X0Y15 J [LS]	CMAC X0Y1	HP I/O Bank 47 I	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 I [LS]	ILKN X0Y1	HP I/O Bank 46 H	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 H [LS]	CMAC X0Y0	HP I/O Bank 45 G	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 F	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-40: **XCVU080 Banks in FFVA2104 Package**

GTY Quad 131 X0Y28-X0Y31 R [LN]	CMAC X0Y3	HP I/O Bank 51 L	HP I/O Bank 71 O	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 Q [LN]	ILKN X0Y4	HP I/O Bank 50 K	HP I/O Bank 70 N	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 P [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49 J	HP I/O Bank 69 M	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 O [LN]	ILKN X0Y3	HP I/O Bank 48	HP I/O Bank 68 F (Partial)	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15 N [LS]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 M [LS]	ILKN X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 L [LS]	CMAC X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3 K [LS]	ILKN X0Y0	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-41: **XCVU080 Banks in FFVB2104 Package**

XCVU095 Bank Diagrams

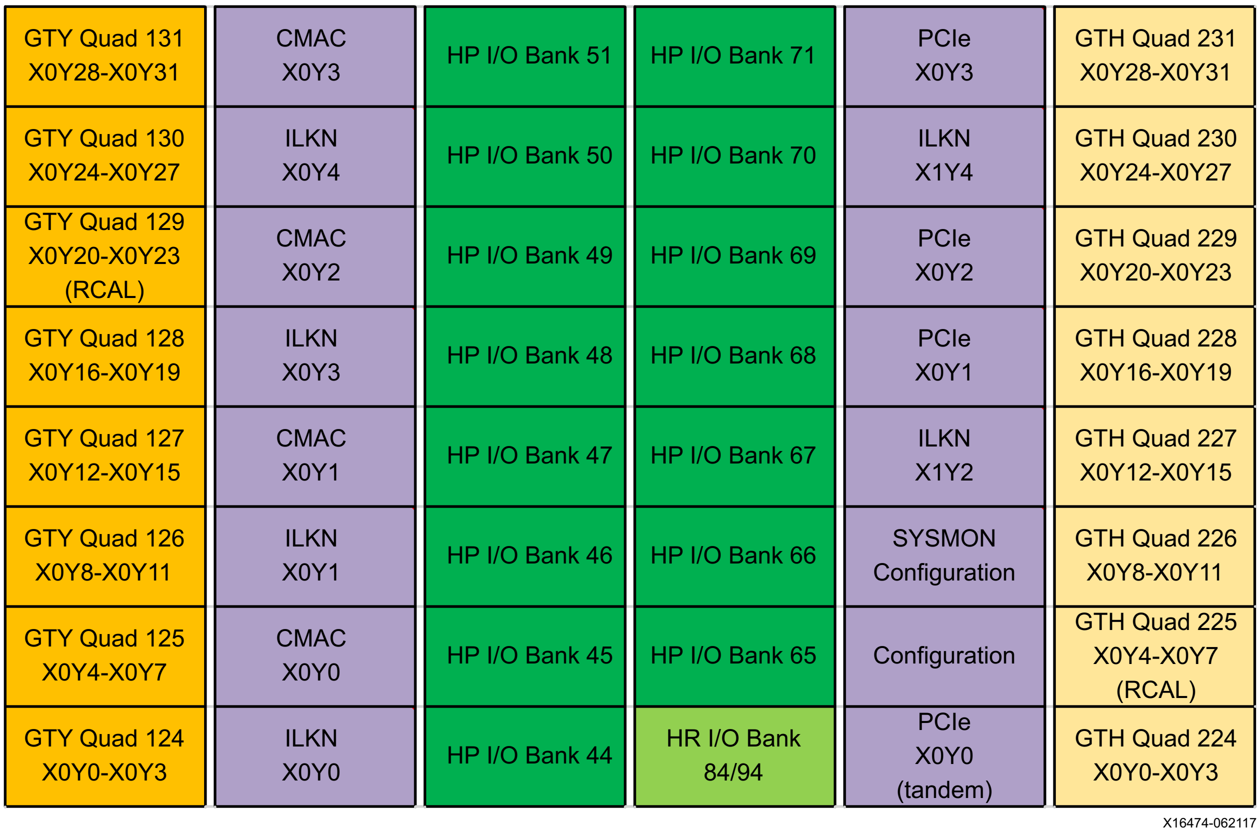

Figure 1-42: **XCVU095 Banks**

GTY Quad 131 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 51	HP I/O Bank 71	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y24-X0Y27	ILKN X0Y4	HP I/O Bank 50	HP I/O Bank 70	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y20-X0Y23 J [L] (RCAL)	CMAC X0Y2	HP I/O Bank 49	HP I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23
GTY Quad 128 X0Y16-X0Y19 I [L]	ILKN X0Y3	HP I/O Bank 48 K	HP I/O Bank 68 F	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [R]
GTY Quad 127 X0Y12-X0Y15 H [L]	CMAC X0Y1	HP I/O Bank 47 J	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [R]
GTY Quad 126 X0Y8-X0Y11 G [L]	ILKN X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [R]
GTY Quad 125 X0Y4-X0Y7 F [L]	CMAC X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [R] (RCAL)
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [R]

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Figure 1-43: **XCVU095 Banks in FFVC1517 Package**

GTY Quad 131 X0Y28-X0Y31 R [LN]	CMAC X0Y3	HP I/O Bank 51	HP I/O Bank 71 H	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 Q [LN]	ILKN X0Y4	HP I/O Bank 50	HP I/O Bank 70 G	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 P [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49	HP I/O Bank 69 F	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 O [LN]	ILKN X0Y3	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15 N [LS]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E (Partial)	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 M [LS]	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 L [LS]	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3 K [LS]	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-44: **XCVU095 Banks in FFVD1517 Package**

GTY Quad 131 X0Y28-X0Y31 M [L]	CMAC X0Y3	HP I/O Bank 51 O (Partial)	HP I/O Bank 71 L	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 L [L]	ILKN X0Y4	HP I/O Bank 50 N	HP I/O Bank 70 K	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 K [L] (RCAL)	CMAC X0Y2	HP I/O Bank 49 M	HP I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 J [L]	ILKN X0Y3	HP I/O Bank 48 J	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 47 I	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11	ILKN X0Y1	HP I/O Bank 46 H	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7	CMAC X0Y0	HP I/O Bank 45 G	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 F	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-45: **XCVU095 Banks in FFVB1760 Package**

GTY Quad 131 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 51 M	HP I/O Bank 71 Q	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31
GTY Quad 130 X0Y24-X0Y27 M [LN]	ILKN X0Y4	HP I/O Bank 50 L	HP I/O Bank 70 P	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 L [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49 K	HP I/O Bank 69 O	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 K [LN]	ILKN X0Y3	HP I/O Bank 48 J	HP I/O Bank 68 N	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RN]
GTY Quad 127 X0Y12-X0Y15 J [LS]	CMAC X0Y1	HP I/O Bank 47 I	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 I [LS]	ILKN X0Y1	HP I/O Bank 46 H	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 H [LS]	CMAC X0Y0	HP I/O Bank 45 G	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 F	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-46: **XCVU095 Banks in FFVA2104 Package**

GTY Quad 131 X0Y28-X0Y31 R [LN]	CMAC X0Y3	HP I/O Bank 51 L	HP I/O Bank 71 O	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 Q [LN]	ILKN X0Y4	HP I/O Bank 50 K	HP I/O Bank 70 N	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 P [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49 J	HP I/O Bank 69 M	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 O [LN]	ILKN X0Y3	HP I/O Bank 48	HP I/O Bank 68 F (Partial)	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15 N [LS]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 M [LS]	ILKN X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 L [LS]	CMAC X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3 K [LS]	ILKN X0Y0	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-47: **XCVU095 Banks in FFVB2104 Package**

GTY Quad 131 X0Y28-X0Y31 U [LN]	CMAC X0Y3	HP I/O Bank 51	HP I/O Bank 71 I	PCIe X0Y3	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 T [LN]	ILKN X0Y4	HP I/O Bank 50	HP I/O Bank 70 H	ILKN X1Y4	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 S [LN] (RCAL)	CMAC X0Y2	HP I/O Bank 49	HP I/O Bank 69 G	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y16-X0Y19 R [LC]	ILKN X0Y3	HP I/O Bank 48	HP I/O Bank 68 F	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RC]
GTY Quad 127 X0Y12-X0Y15 Q [LC]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RC]
GTY Quad 126 X0Y8-X0Y11 P [LC]	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RC]
GTY Quad 125 X0Y4-X0Y7 O [LC]	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RC] (RCAL)
GTY Quad 124 X0Y0-X0Y3 N [LC]	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RC]

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Figure 1-48: **XCVU095 Banks in FFVC2104 Package**

XCVU125 Bank Diagrams

GTY Quad 133 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y3	GTH Quad 233 X0Y36-X0Y39
GTY Quad 132 X0Y32-X0Y35	CMAC X0Y4	HP I/O Bank 52	HP I/O Bank 72	ILKN X1Y5	GTH Quad 232 X0Y32-X0Y35
GTY Quad 131 X0Y28-X0Y31	ILKN X0Y4	HP I/O Bank 51	HP I/O Bank 71	SYSMON Configuration	GTH Quad 231 X0Y28-X0Y31 (RCAL)
GTY Quad 130 X0Y24-X0Y27 (RCAL)	CMAC X0Y3	HP I/O Bank 50	HP I/O Bank 70	Configuration	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y20-X0Y23	ILKN X0Y3	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23
SLR Crossing					
GTY Quad 128 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19
GTY Quad 127 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15
GTY Quad 126 X0Y8-X0Y11	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 (RCAL)
GTY Quad 125 X0Y4-X0Y7 (RCAL)	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTH Quad 225 X0Y4-X0Y7
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3

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Figure 1-49: **XCVU125 Banks**

GTY Quad 133 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 53	HP I/O Bank 73 H	PCIe X0Y3	GTH Quad 233 X0Y36-X0Y39 J [RN]
GTY Quad 132 X0Y32-X0Y35 R [LN]	CMAC X0Y4	HP I/O Bank 52	HP I/O Bank 72 G	ILKN X1Y5	GTH Quad 232 X0Y32-X0Y35 I [RN]
GTY Quad 131 X0Y28-X0Y31 Q [LN]	ILKN X0Y4	HP I/O Bank 51	HP I/O Bank 71 F	SYSMON Configuration	GTH Quad 231 X0Y28-X0Y31 H [RN] (RCAL)
GTY Quad 130 X0Y24-X0Y27 P [LN] (RCAL)	CMAC X0Y3	HP I/O Bank 50	HP I/O Bank 70	Configuration	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 O [LN]	ILKN X0Y3	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
SLR Crossing					
GTY Quad 128 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y12-X0Y15 N [LS]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E (Partial)	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 M [LS]	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
GTY Quad 125 X0Y4-X0Y7 L [LS] (RCAL)	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
GTY Quad 124 X0Y0-X0Y3 K [LS]	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-50: **XCVU125 Banks in FLVD1517 Package**

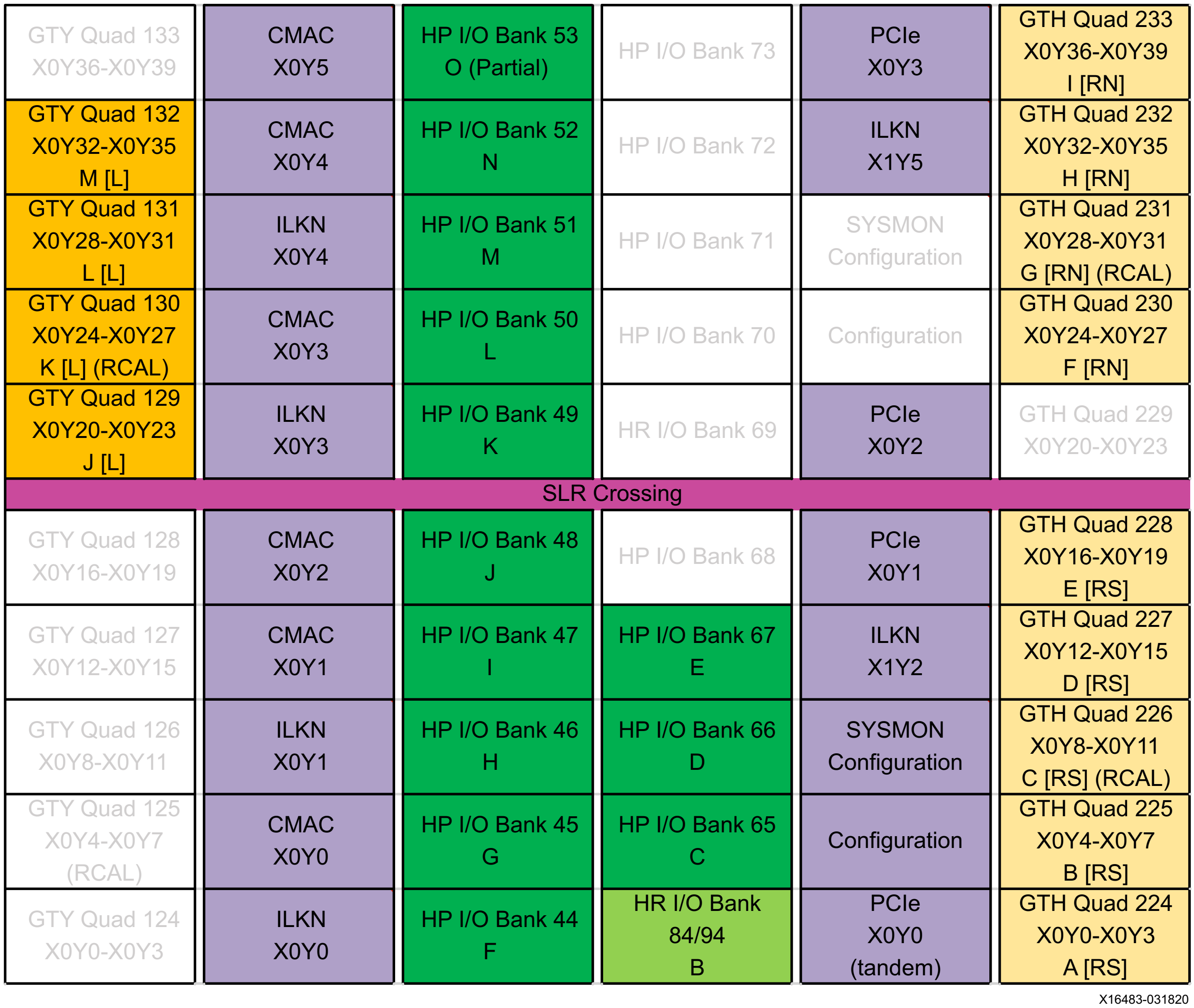

Figure 1-51: **XCVU125 Banks in FLVB1760 Package**

GTY Quad 133 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 53 M	HP I/O Bank 73 Q	PCIe X0Y3	GTH Quad 233 X0Y36-X0Y39 G [RN]
GTY Quad 132 X0Y32-X0Y35 M [LN]	CMAC X0Y4	HP I/O Bank 52 L	HP I/O Bank 72 P	ILKN X1Y5	GTH Quad 232 X0Y32-X0Y35 F [RN]
GTY Quad 131 X0Y28-X0Y31 L [LN]	ILKN X0Y4	HP I/O Bank 51 K	HP I/O Bank 71 O	SYSMON Configuration	GTH Quad 231 X0Y28-X0Y31 E [RN] (RCAL)
GTY Quad 130 X0Y24-X0Y27 K [LN] (RCAL)	CMAC X0Y3	HP I/O Bank 50 J	HP I/O Bank 70 N	Configuration	GTH Quad 230 X0Y24-X0Y27
GTY Quad 129 X0Y20-X0Y23	ILKN X0Y3	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23
SLR Crossing					
GTY Quad 128 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19
GTY Quad 127 X0Y12-X0Y15 J [LS]	CMAC X0Y1	HP I/O Bank 47 I	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 I [LS]	ILKN X0Y1	HP I/O Bank 46 H	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
GTY Quad 125 X0Y4-X0Y7 H [LS] (RCAL)	CMAC X0Y0	HP I/O Bank 45 G	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
GTY Quad 124 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 44 F	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-52: **XCVU125 Banks in FLVA2104 Package**

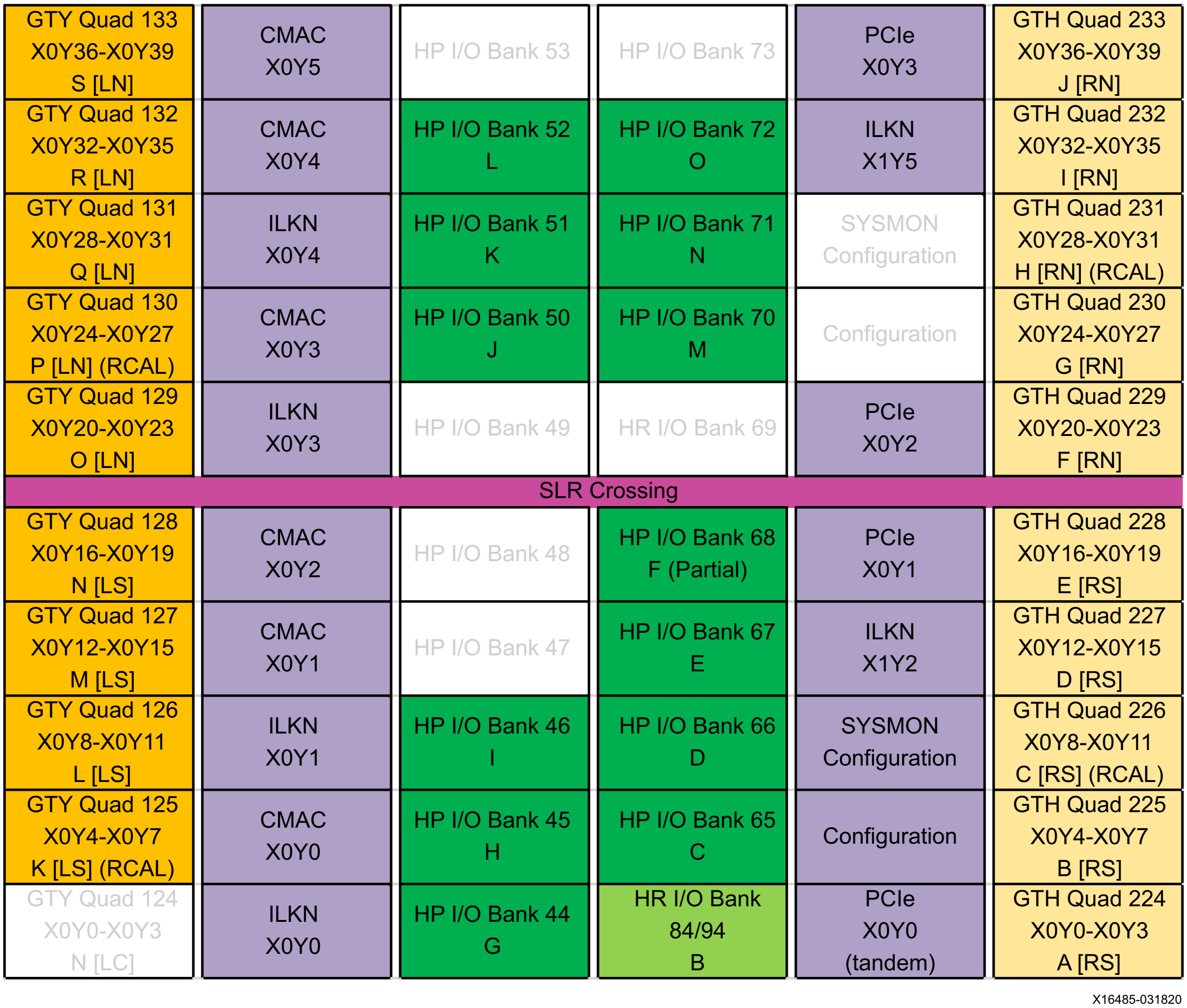

Figure 1-53: **XCVU125 Banks in FLVB2104 Package**

GTY Quad 133 X0Y36-X0Y39 W [LN]	CMAC X0Y5	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y3	GTH Quad 233 X0Y36-X0Y39 J [RN]
GTY Quad 132 X0Y32-X0Y35 V [LN]	CMAC X0Y4	HP I/O Bank 52	HP I/O Bank 72 I	ILKN X1Y5	GTH Quad 232 X0Y32-X0Y35 I [RN]
GTY Quad 131 X0Y28-X0Y31 U [LN]	ILKN X0Y4	HP I/O Bank 51	HP I/O Bank 71 H	SYSMON Configuration	GTH Quad 231 X0Y28-X0Y31 H [RN] (RCAL)
GTY Quad 130 X0Y24-X0Y27 T [LN] (RCAL)	CMAC X0Y3	HP I/O Bank 50	HP I/O Bank 70 G	Configuration	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 S [LN]	ILKN X0Y3	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y2	GTH Quad 229 X0Y20-X0Y23 F [RN]
SLR Crossing					
GTY Quad 128 X0Y16-X0Y19 R [LC]	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68 F	PCIe X0Y1	GTH Quad 228 X0Y16-X0Y19 E [RC]
GTY Quad 127 X0Y12-X0Y15 Q [LC]	CMAC X0Y1	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y2	GTH Quad 227 X0Y12-X0Y15 D [RC]
GTY Quad 126 X0Y8-X0Y11 P [LC]	ILKN X0Y1	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RC] (RCAL)
GTY Quad 125 X0Y4-X0Y7 O [LC] (RCAL)	CMAC X0Y0	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RC]
GTY Quad 124 X0Y0-X0Y3 N [LC]	ILKN X0Y0	HP I/O Bank 44	HR I/O Bank 84/94 B	PCIe X0Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RC]

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Figure 1-54: **XCVU125 Banks in FLVC2104 Package**

XCVU160 Bank Diagrams

GTY Quad 133 X0Y52-X0Y55	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y4	GTH Quad 233 X0Y52-X0Y55
GTY Quad 132 X0Y45-X0Y51	CMAC X0Y7	HP I/O Bank 52	HP I/O Bank 72	ILKN X1Y7	GTH Quad 232 X0Y45-X0Y51
GTY Quad 131 X0Y44-X0Y47	ILKN X0Y6	HP I/O Bank 51	HP I/O Bank 71	SYSMON Configuration	GTH Quad 231 X0Y44-X0Y47 (RCAL)
GTY Quad 130 X0Y40-X0Y43 (RCAL)	CMAC X0Y6	HP I/O Bank 50	HP I/O Bank 70	Configuration	GTH Quad 230 X0Y40-X0Y43
GTY Quad 129 X0Y36-X0Y39	ILKN X0Y5	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y3	GTH Quad 229 X0Y36-X0Y39
SLR Crossing					
GTY Quad 128 X0Y32-X0Y35	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y2	GTH Quad 228 X0Y32-X0Y35
GTY Quad 127 X0Y28-X0Y31	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y4	GTH Quad 227 X0Y28-X0Y31
GTY Quad 126 X0Y24-X0Y27	ILKN X0Y2	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTH Quad 226 X0Y24-X0Y27 (RCAL)
GTY Quad 125 X0Y20-X0Y23 (RCAL)	CMAC X0Y3	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTH Quad 225 X0Y20-X0Y23
GTY Quad 124 X0Y16-X0Y19	ILKN X0Y2	HP I/O Bank 44	HR I/O Bank 84/94	PCIe X0Y1 (tandem)	GTH Quad 224 X0Y16-X0Y19
SLR Crossing					
GTY Quad 123 X0Y12-X0Y15	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	PCIe X0Y0	GTH Quad 223 X0Y12-X0Y15
GTY Quad 122 X0Y8-X0Y11	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y1	GTH Quad 222 X0Y8-X0Y11
GTY Quad 121 X0Y4-X0Y7	ILKN X0Y0	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTH Quad 221 X0Y4-X0Y7 (RCAL)
GTY Quad 120 X0Y0-X0Y3 (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y0-X0Y3

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Figure 1-55: **XCVU160 Banks**

GTY Quad 133 X0Y52-X0Y55 S [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y4	GTH Quad 233 X0Y52-X0Y55 J [RN]
GTY Quad 132 X0Y45-X0Y51 R [LN]	CMAC X0Y7	HP I/O Bank 52 L	HP I/O Bank 72 O	ILKN X1Y7	GTH Quad 232 X0Y45-X0Y51 I [RN]
GTY Quad 131 X0Y44-X0Y47 Q [LN]	ILKN X0Y6	HP I/O Bank 51 K	HP I/O Bank 71 N	SYSMON Configuration	GTH Quad 231 X0Y44-X0Y47 H [RN] (RCAL)
GTY Quad 130 X0Y40-X0Y43 P [LN] (RCAL)	CMAC X0Y6	HP I/O Bank 50 J	HP I/O Bank 70 M	Configuration	GTH Quad 230 X0Y40-X0Y43 G [RN]
GTY Quad 129 X0Y36-X0Y39 O [LN]	ILKN X0Y5	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y3	GTH Quad 229 X0Y36-X0Y39 F [RN]
SLR Crossing					
GTY Quad 128 X0Y32-X0Y35 N [LS]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 F (Partial)	PCIe X0Y2	GTH Quad 228 X0Y32-X0Y35 E [RS]
GTY Quad 127 X0Y28-X0Y31 M [LS]	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y4	GTH Quad 227 X0Y28-X0Y31 D [RS]
GTY Quad 126 X0Y24-X0Y27 L [LS]	ILKN X0Y2	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y24-X0Y27 C [RS] (RCAL)
GTY Quad 125 X0Y20-X0Y23 K [LS] (RCAL)	CMAC X0Y3	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y20-X0Y23 B [RS]
GTY Quad 124 X0Y16-X0Y19	ILKN X0Y2	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y1 (tandem)	GTH Quad 224 X0Y16-X0Y19 A [RS]
SLR Crossing					
GTY Quad 123 X0Y12-X0Y15	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	PCIe X0Y0	GTH Quad 223 X0Y12-X0Y15
GTY Quad 122 X0Y8-X0Y11	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y1	GTH Quad 222 X0Y8-X0Y11
GTY Quad 121 X0Y4-X0Y7	ILKN X0Y0	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTH Quad 221 X0Y4-X0Y7 (RCAL)
GTY Quad 120 X0Y0-X0Y3 (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y0-X0Y3

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Figure 1-56: **XCVU160 Banks in FLGB2104 Package**

GTY Quad 133 X0Y52-X0Y55 W [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y4	GTH Quad 233 X0Y52-X0Y55 J [RN]
GTY Quad 132 X0Y45-X0Y51 V [LN]	CMAC X0Y7	HP I/O Bank 52 L	HP I/O Bank 72 I	ILKN X1Y7	GTH Quad 232 X0Y45-X0Y51 I [RN]
GTY Quad 131 X0Y44-X0Y47 U [LN]	ILKN X0Y6	HP I/O Bank 51 K	HP I/O Bank 71 H	SYSMON Configuration	GTH Quad 231 X0Y44-X0Y47 H [RN] (RCAL)
GTY Quad 130 X0Y40-X0Y43 T [LN] (RCAL)	CMAC X0Y6	HP I/O Bank 50 J	HP I/O Bank 70 G	Configuration	GTH Quad 230 X0Y40-X0Y43 G [RN]
GTY Quad 129 X0Y36-X0Y39 S [LN]	ILKN X0Y5	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y3	GTH Quad 229 X0Y36-X0Y39 F [RN]
	SLR Crossing				
GTY Quad 128 X0Y32-X0Y35 R [LC]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 F	PCIe X0Y2	GTH Quad 228 X0Y32-X0Y35 E [RC]
GTY Quad 127 X0Y28-X0Y31 Q [LC]	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y4	GTH Quad 227 X0Y28-X0Y31 D [RC]
GTY Quad 126 X0Y24-X0Y27 P [LC]	ILKN X0Y2	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y24-X0Y27 C [RC] (RCAL)
GTY Quad 125 X0Y20-X0Y23 O [LC] (RCAL)	CMAC X0Y3	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y20-X0Y23 B [RC]
GTY Quad 124 X0Y16-X0Y19 N [LC]	ILKN X0Y2	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y1 (tandem)	GTH Quad 224 X0Y16-X0Y19 A [RC]
	SLR Crossing				
GTY Quad 123 X0Y12-X0Y15	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	PCIe X0Y0	GTH Quad 223 X0Y12-X0Y15
GTY Quad 122 X0Y8-X0Y11 Z [LS]	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y1	GTH Quad 222 X0Y8-X0Y11 M [RS]
GTY Quad 121 X0Y4-X0Y7 Y [LS]	ILKN X0Y0	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTH Quad 221 X0Y4-X0Y7 L [RS] (RCAL)
GTY Quad 120 X0Y0-X0Y3 X [LS] (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y0-X0Y3 K [RS]

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Figure 1-57: **XCVU160 Banks in FLGC2104 Package**

XCVU190 Bank Diagrams

GTY Quad 133 X0Y56-X0Y59	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y5	GTH Quad 233 X0Y56-X0Y59
GTY Quad 132 X0Y52-X0Y55	CMAC X0Y7	HP I/O Bank 52	HP I/O Bank 72	ILKN X1Y8	GTH Quad 232 X0Y52-X0Y55
GTY Quad 131 X0Y48-X0Y51	ILKN X0Y7	HP I/O Bank 51	HP I/O Bank 71	SYSMON Configuration	GTH Quad 231 X0Y48-X0Y51 (RCAL)
GTY Quad 130 X0Y44-X0Y47 (RCAL)	CMAC X0Y6	HP I/O Bank 50	HP I/O Bank 70	Configuration	GTH Quad 230 X0Y44-X0Y47
GTY Quad 129 X0Y40-X0Y43	ILKN X0Y6	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y4	GTH Quad 229 X0Y40-X0Y43
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68	PCIe X0Y3	GTH Quad 228 X0Y36-X0Y39
GTY Quad 127 X0Y32-X0Y35	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y5	GTH Quad 227 X0Y32-X0Y35
GTY Quad 126 X0Y28-X0Y31	ILKN X0Y4	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTH Quad 226 X0Y28-X0Y31 (RCAL)
GTY Quad 125 X0Y24-X0Y27 (RCAL)	CMAC X0Y3	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTH Quad 225 X0Y24-X0Y27
GTY Quad 124 X0Y20-X0Y23	ILKN X0Y3	HP I/O Bank 44	HR I/O Bank 84/94	PCIe X0Y2 (tandem)	GTH Quad 224 X0Y20-X0Y23
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	PCIe X0Y1	GTH Quad 223 X0Y16-X0Y19
GTY Quad 122 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y2	GTH Quad 222 X0Y12-X0Y15
GTY Quad 121 X0Y8-X0Y11	ILKN X0Y1	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTH Quad 221 X0Y8-X0Y11 (RCAL)
GTY Quad 120 X0Y4-X0Y7 (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y4-X0Y7
GTY Quad 119 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 39	HR I/O Bank 59	PCIe X0Y0	GTH Quad 219 X0Y0-X0Y3

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Figure 1-58: **XCVU190 Banks**

GTY Quad 133 X0Y56-X0Y59 S [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y5	GTH Quad 233 X0Y56-X0Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55 R [LN]	CMAC X0Y7	HP I/O Bank 52 L	HP I/O Bank 72 O	ILKN X1Y8	GTH Quad 232 X0Y52-X0Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 Q [LN]	ILKN X0Y7	HP I/O Bank 51 K	HP I/O Bank 71 N	SYSMON Configuration	GTH Quad 231 X0Y48-X0Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47 P [LN] (RCAL)	CMAC X0Y6	HP I/O Bank 50 J	HP I/O Bank 70 M	Configuration	GTH Quad 230 X0Y44-X0Y47 G [RN]
GTY Quad 129 X0Y40-X0Y43 O [LN]	ILKN X0Y6	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y4	GTH Quad 229 X0Y40-X0Y43 F [RN]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39 N [LS]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 F (Partial)	PCIe X0Y3	GTH Quad 228 X0Y36-X0Y39 E [RS]
GTY Quad 127 X0Y32-X0Y35 M [LS]	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y5	GTH Quad 227 X0Y32-X0Y35 D [RS]
GTY Quad 126 X0Y28-X0Y31 L [LS]	ILKN X0Y4	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y28-X0Y31 C [RS] (RCAL)
GTY Quad 125 X0Y24-X0Y27 K [LS] (RCAL)	CMAC X0Y3	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y24-X0Y27 B [RS]
GTY Quad 124 X0Y20-X0Y23	ILKN X0Y3	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y2 (tandem)	GTH Quad 224 X0Y20-X0Y23 A [RS]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	PCIe X0Y1	GTH Quad 223 X0Y16-X0Y19
GTY Quad 122 X0Y12-X0Y15	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y2	GTH Quad 222 X0Y12-X0Y15
GTY Quad 121 X0Y8-X0Y11	ILKN X0Y1	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTH Quad 221 X0Y8-X0Y11 (RCAL)
GTY Quad 120 X0Y4-X0Y7 (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y4-X0Y7
GTY Quad 119 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 39	HR I/O Bank 59	PCIe X0Y0	GTH Quad 219 X0Y0-X0Y3

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Figure 1-59: **XCVU190 Banks in FLGB2104 Package**

GTY Quad 133 X0Y56-X0Y59 W [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y5	GTH Quad 233 X0Y56-X0Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55 V [LN]	CMAC X0Y7	HP I/O Bank 52 L	HP I/O Bank 72 I	ILKN X1Y8	GTH Quad 232 X0Y52-X0Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 U [LN]	ILKN X0Y7	HP I/O Bank 51 K	HP I/O Bank 71 H	SYSMON Configuration	GTH Quad 231 X0Y48-X0Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47 T [LN] (RCAL)	CMAC X0Y6	HP I/O Bank 50 J	HP I/O Bank 70 G	Configuration	GTH Quad 230 X0Y44-X0Y47 G [RN]
GTY Quad 129 X0Y40-X0Y43 S [LN]	ILKN X0Y6	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y4	GTH Quad 229 X0Y40-X0Y43 F [RN]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39 R [LC]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 F	PCIe X0Y3	GTH Quad 228 X0Y36-X0Y39 E [RC]
GTY Quad 127 X0Y32-X0Y35 Q [LC]	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y5	GTH Quad 227 X0Y32-X0Y35 D [RC]
GTY Quad 126 X0Y28-X0Y31 P [LC]	ILKN X0Y4	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y28-X0Y31 C [RC] (RCAL)
GTY Quad 125 X0Y24-X0Y27 O [LC] (RCAL)	CMAC X0Y3	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y24-X0Y27 B [RC]
GTY Quad 124 X0Y20-X0Y23 N [LC]	ILKN X0Y3	HP I/O Bank 44 G	HR I/O Bank 84/94 B	PCIe X0Y2 (tandem)	GTH Quad 224 X0Y20-X0Y23 A [RC]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	PCIe X0Y1	GTH Quad 223 X0Y16-X0Y19
GTY Quad 122 X0Y12-X0Y15 Z [LS]	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y2	GTH Quad 222 X0Y12-X0Y15 M [RS]
GTY Quad 121 X0Y8-X0Y11 Y [LS]	ILKN X0Y1	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTH Quad 221 X0Y8-X0Y11 L [RS] (RCAL)
GTY Quad 120 X0Y4-X0Y7 X [LS] (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y4-X0Y7 K [RS]
GTY Quad 119 X0Y0-X0Y3	ILKN X0Y0	HP I/O Bank 39	HR I/O Bank 59	PCIe X0Y0	GTH Quad 219 X0Y0-X0Y3

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Figure 1-60: **XCVU190 Banks in FLGC2104 Package**

GTY Quad 133 X0Y56-X0Y59 Z [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	PCIe X0Y5	GTH Quad 233 X0Y56-X0Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55 Y [LN]	CMAC X0Y7	HP I/O Bank 52	HP I/O Bank 72 K	ILKN X1Y8	GTH Quad 232 X0Y52-X0Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 X [LN]	ILKN X0Y7	HP I/O Bank 51	HP I/O Bank 71 J	SYSMON Configuration	GTH Quad 231 X0Y48-X0Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47 W [LUC] (RCAL)	CMAC X0Y6	HP I/O Bank 50	HP I/O Bank 70 I	Configuration	GTH Quad 230 X0Y44-X0Y47 G [RUC]
GTY Quad 129 X0Y40-X0Y43 V [LUC]	ILKN X0Y6	HP I/O Bank 49	HR I/O Bank 69	PCIe X0Y4	GTH Quad 229 X0Y40-X0Y43 F [RUC]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39 U [LUC]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 H (Partial)	PCIe X0Y3	GTH Quad 228 X0Y36-X0Y39 E [RUC]
GTY Quad 127 X0Y32-X0Y35 T [LUC]	CMAC X0Y4	HP I/O Bank 47	HP I/O Bank 67 G	ILKN X1Y5	GTH Quad 227 X0Y32-X0Y35 D [RUC]
GTY Quad 126 X0Y28-X0Y31 S [LLC]	ILKN X0Y4	HP I/O Bank 46	HP I/O Bank 66 B (Partial)	SYSMON Configuration	GTH Quad 226 X0Y28-X0Y31 C [RLC] (RCAL)
GTY Quad 125 X0Y24-X0Y27 R [LLC] (RCAL)	CMAC X0Y3	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y24-X0Y27 B [RLC]
GTY Quad 124 X0Y20-X0Y23 Q [LLC]	ILKN X0Y3	HP I/O Bank 44	HR I/O Bank 84/94	PCIe X0Y2 (tandem)	GTH Quad 224 X0Y20-X0Y23 A [RLC]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19 AF [LLC]	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63 F	PCIe X0Y1	GTH Quad 223 X0Y16-X0Y19 P [RLC]
GTY Quad 122 X0Y12-X0Y15 AE [LS]	CMAC X0Y1	HP I/O Bank 42	HP I/O Bank 62 E	ILKN X1Y2	GTH Quad 222 X0Y12-X0Y15 O [RS]
GTY Quad 121 X0Y8-X0Y11 AD [LS]	ILKN X0Y1	HP I/O Bank 41	HP I/O Bank 61 D	SYSMON Configuration	GTH Quad 221 X0Y8-X0Y11 N [RS] (RCAL)
GTY Quad 120 X0Y4-X0Y7 AC [LS] (RCAL)	CMAC X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTH Quad 220 X0Y4-X0Y7 M [RS]
GTY Quad 119 X0Y0-X0Y3 AB [LS]	ILKN X0Y0	HP I/O Bank 39	HR I/O Bank 59	PCIe X0Y0	GTH Quad 219 X0Y0-X0Y3 L [RS]

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Figure 1-61: **XCVU190 Banks in FLGA2577 Package**

XCVU440 Bank Diagrams

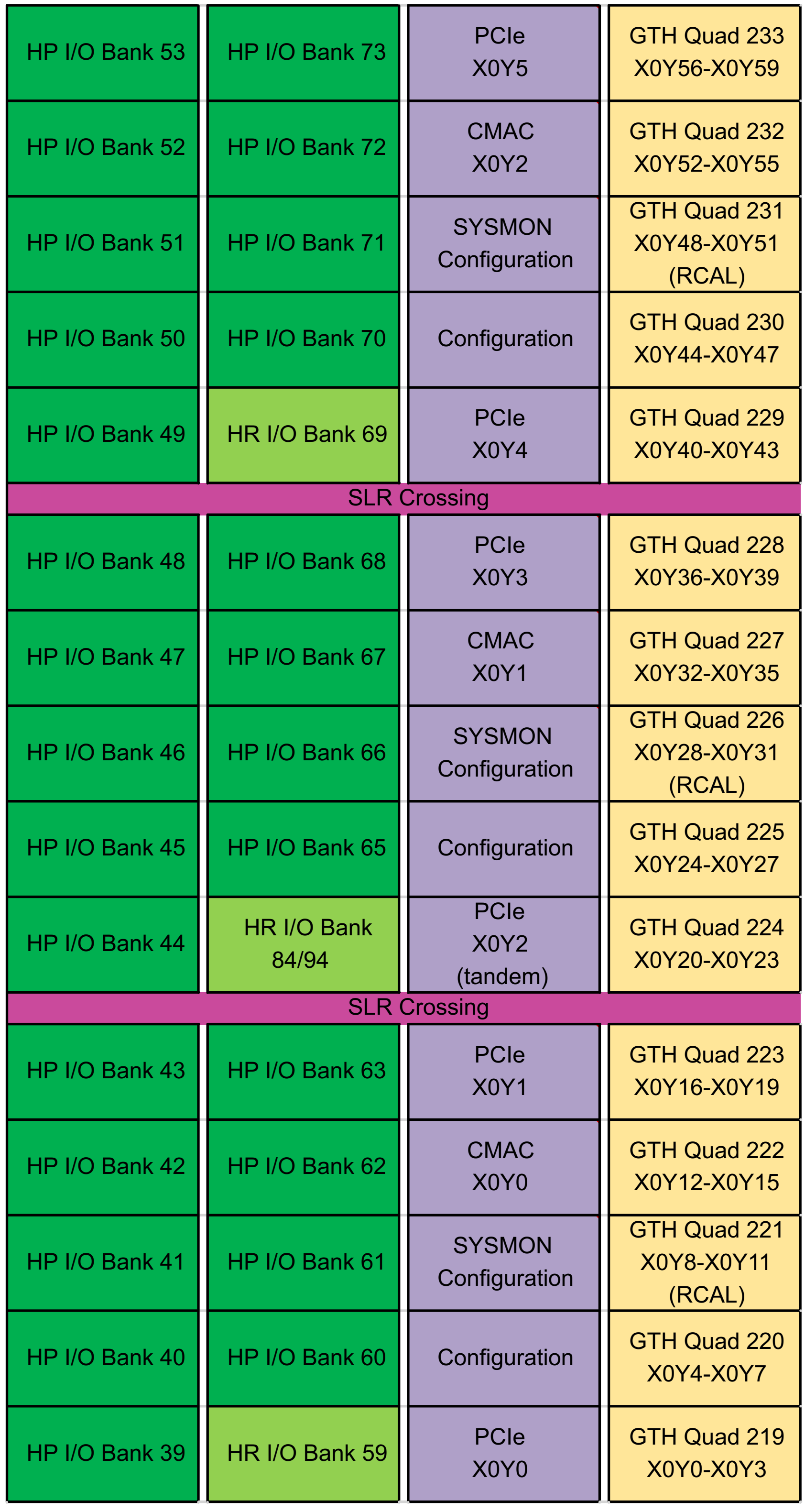

Figure 1-62: **XCVU440 Banks**

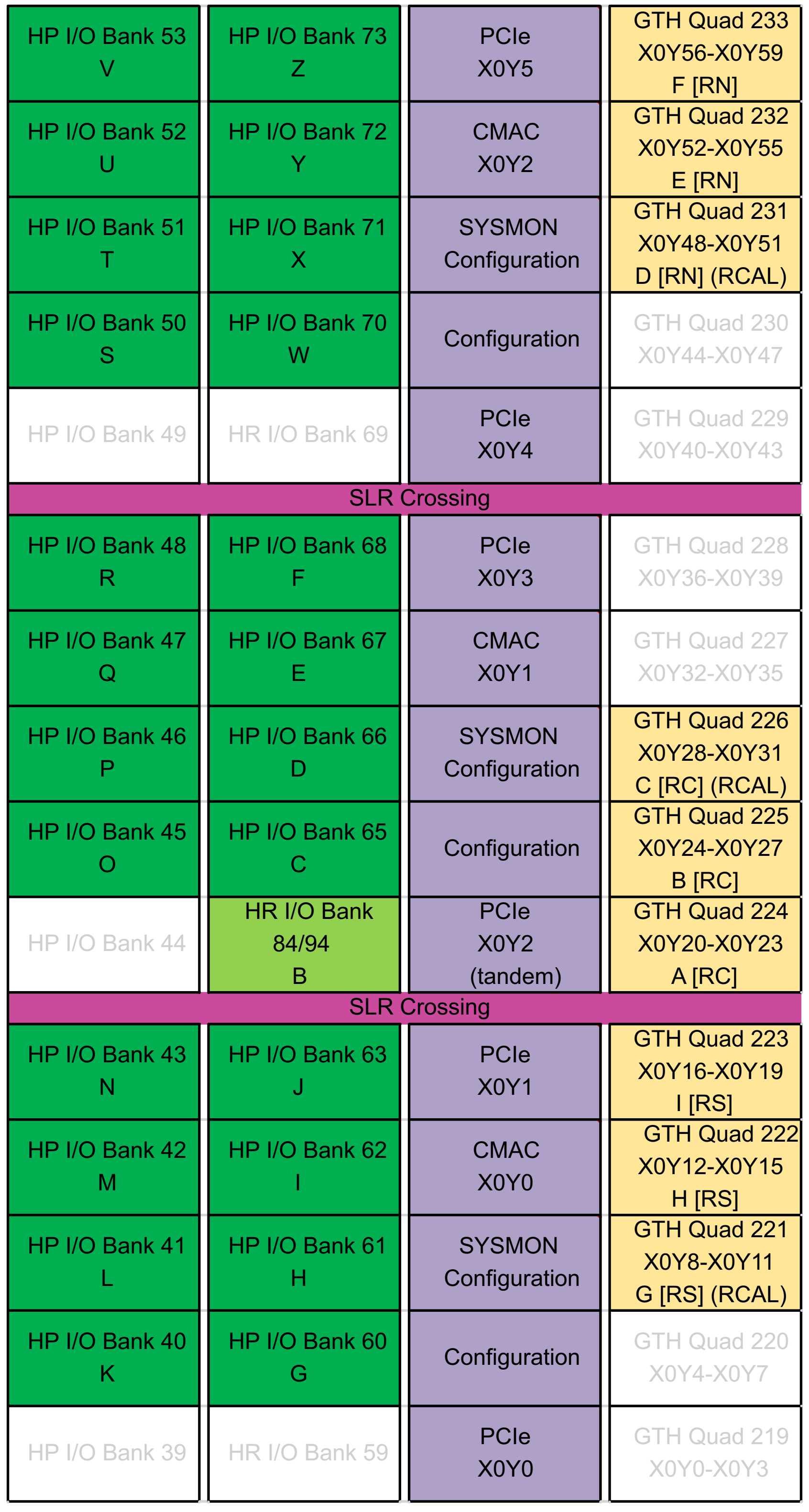

Figure 1-63: **XCVU440 Banks in FLGB2377 Package**

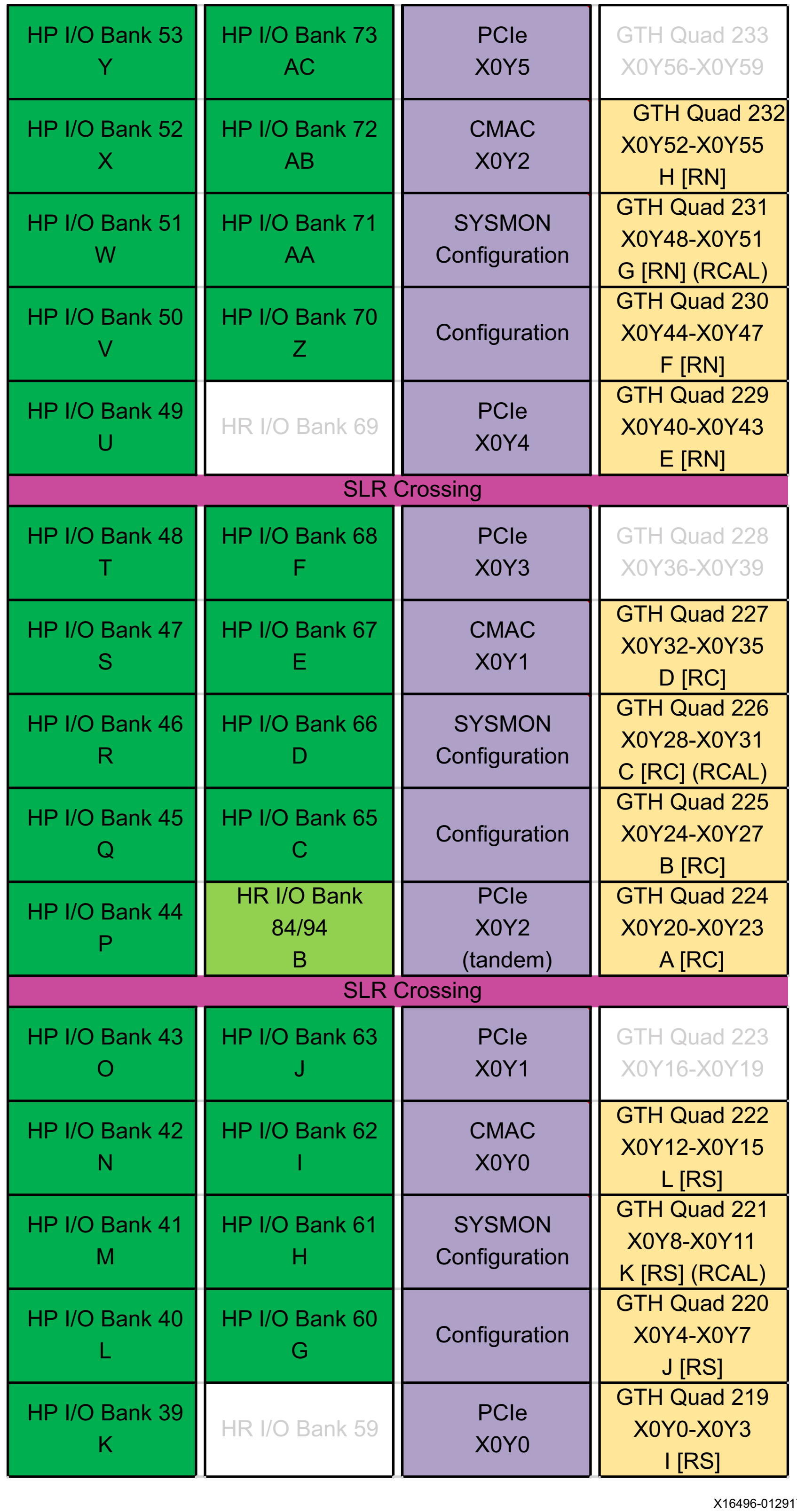

Figure 1-64: **XCVU440 Banks in FLGA2892 Package**

XCAU7P and XAAU7P Bank Diagrams

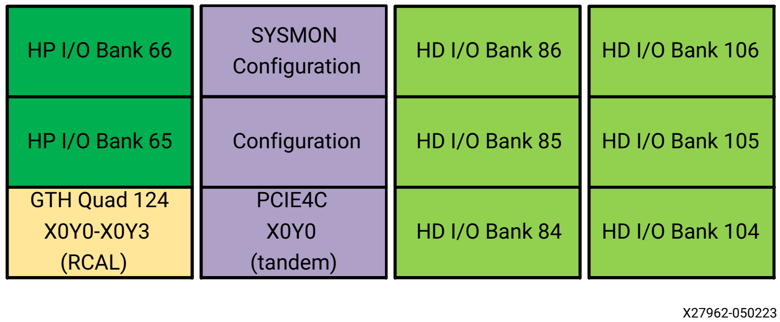

Figure 1-65: **XCAU7P and XAAU7P Banks**

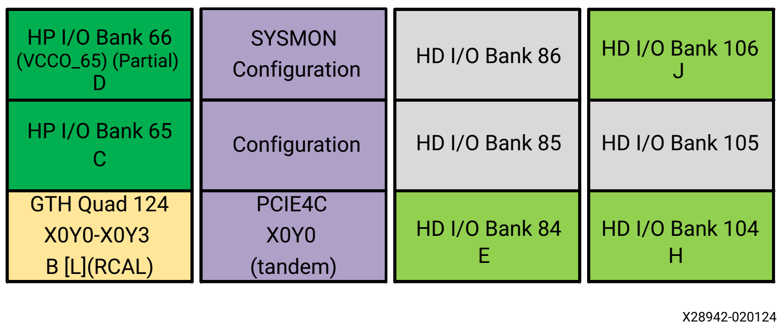

Figure 1-66: **XCAU7P and XAAU7P Banks in FCVA289 Package**

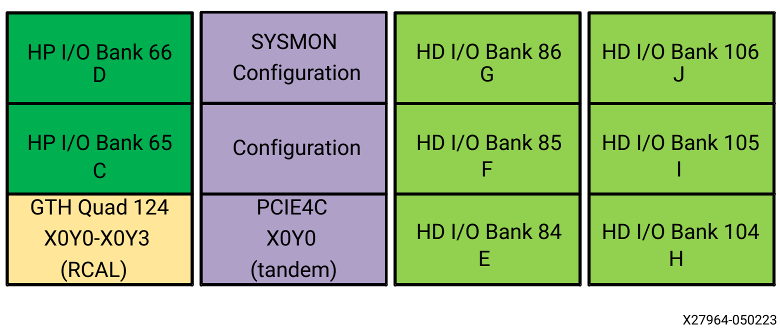

Figure 1-67: **XCAU7P and XAAU7P Banks in SBVC484 Package**

XCAU10P and XAAU10P Bank Diagrams

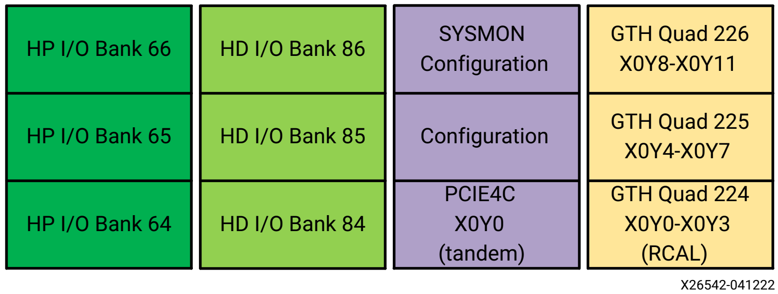

Figure 1-68: **XCAU10P Banks**

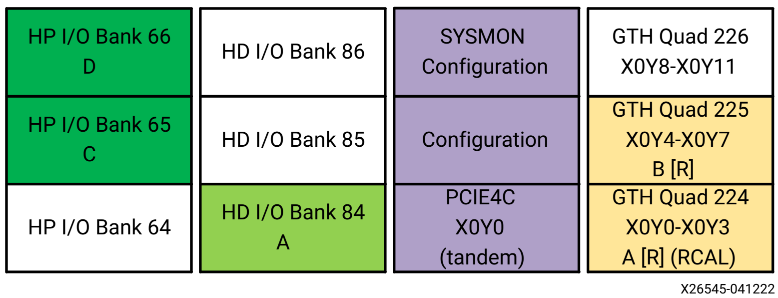

Figure 1-69: **XCAU10P Banks in UBVA368 Package**

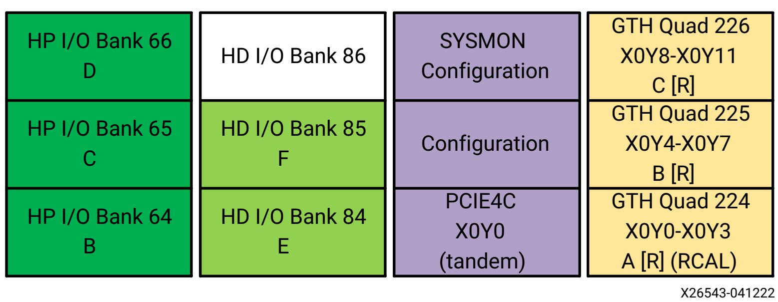

Figure 1-70: **XCAU10P and XAAU10P Banks in SBVB484 Package**

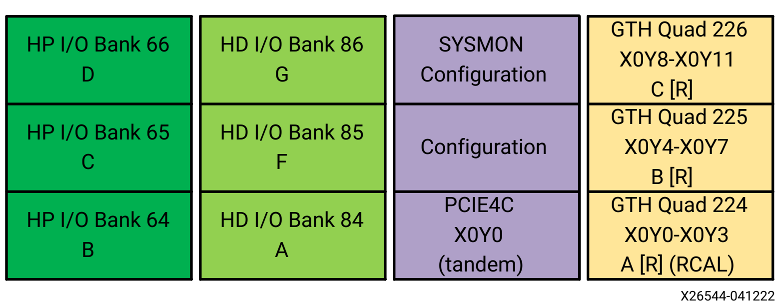

Figure 1-71: **XCAU10P and XAAU10P Banks in FFVB676 Package**

XCAU15P and XAAU15P Bank Diagrams

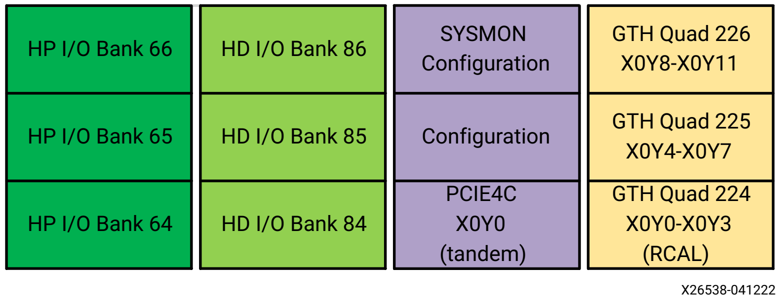

Figure 1-72: **XCAU15P and XAAU15P Banks**

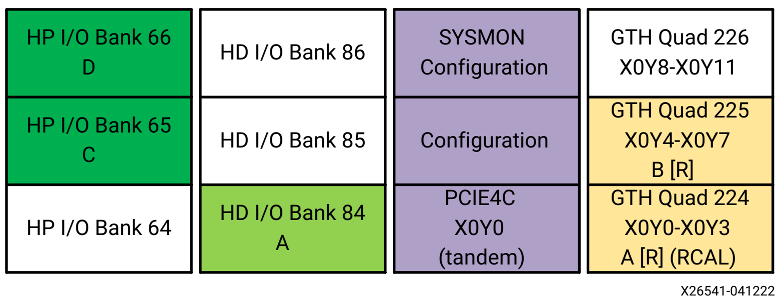

Figure 1-73: **XCAU15P Banks in UBVA368 Package**

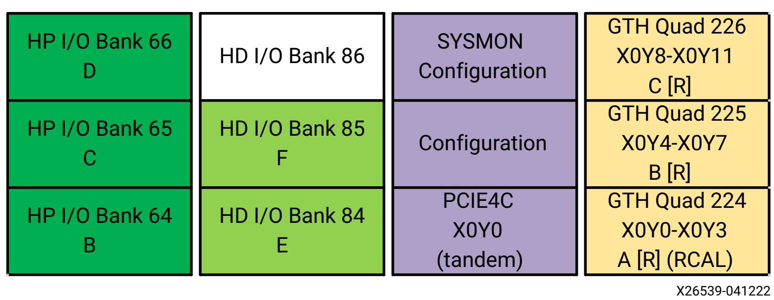

Figure 1-74: **XCAU15P and XAAU15P Banks in SBVB484 Package**

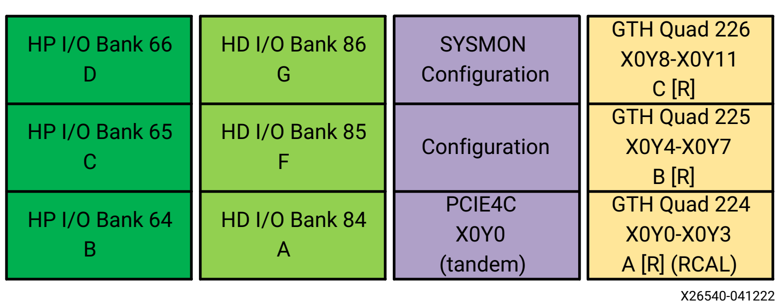

Figure 1-75: **XCAU15P and XAAU15P Banks in FFVB676 Package**

XCAU20P Bank Diagrams

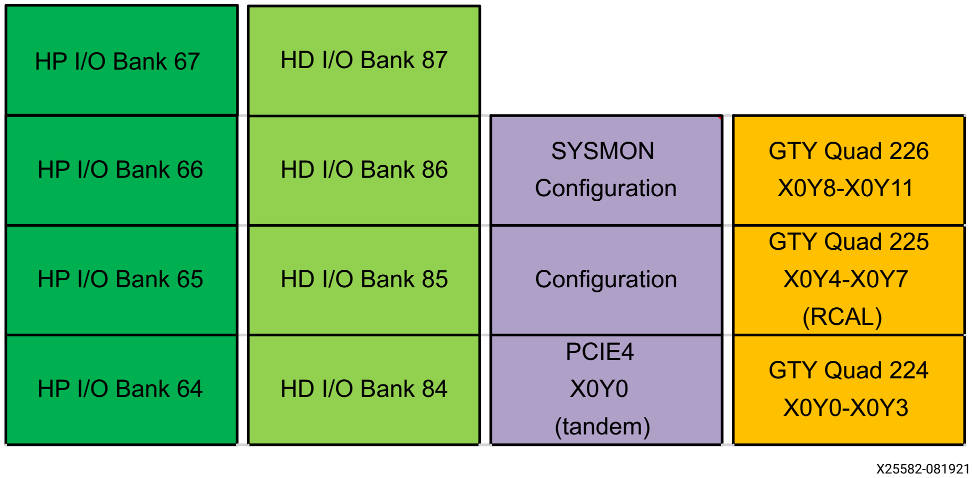

Figure 1-76: **XCAU20P Banks**

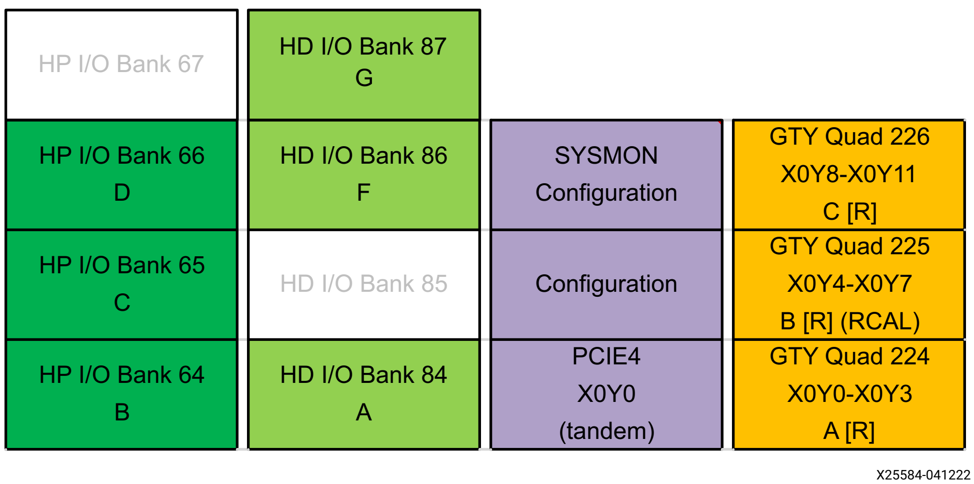

Figure 1-77: **XCAU20P Banks in FFVB676 Package**

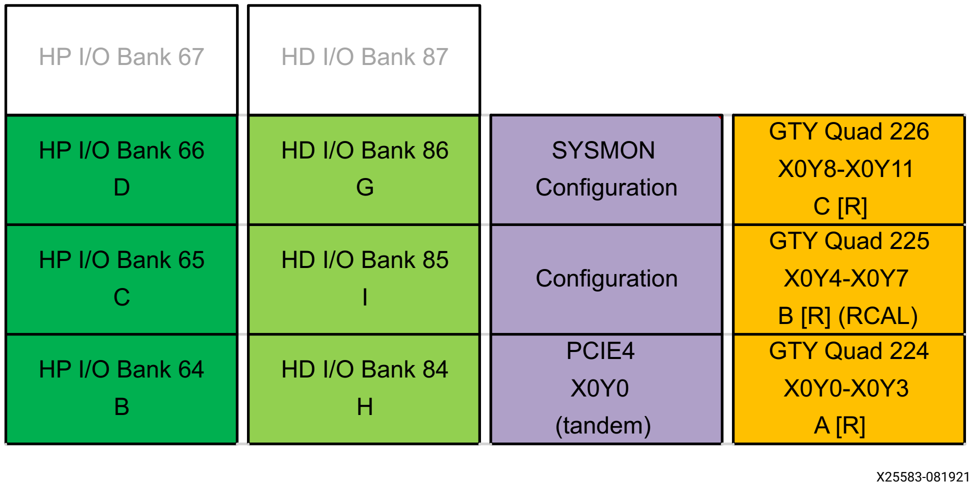

Figure 1-78: **XCAU20P Banks in SFVB784 Package**

XCAU25P Bank Diagrams

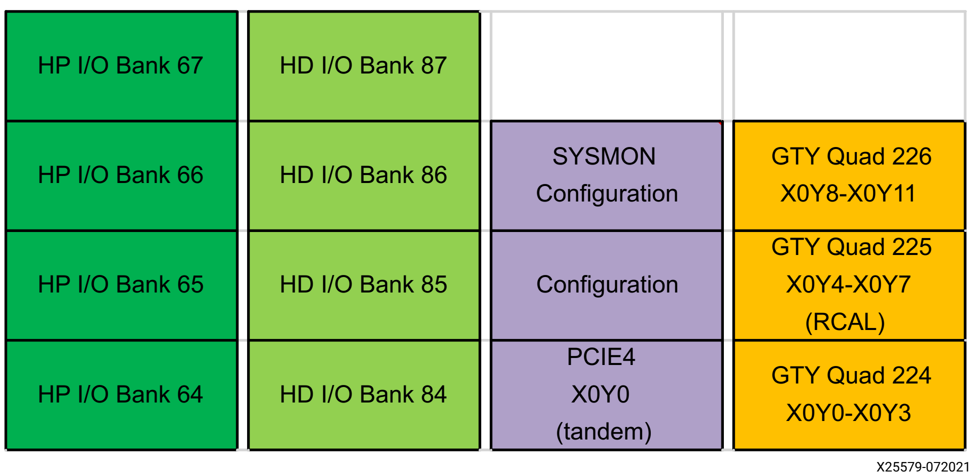

Figure 1-79: **XCAU25P Banks**

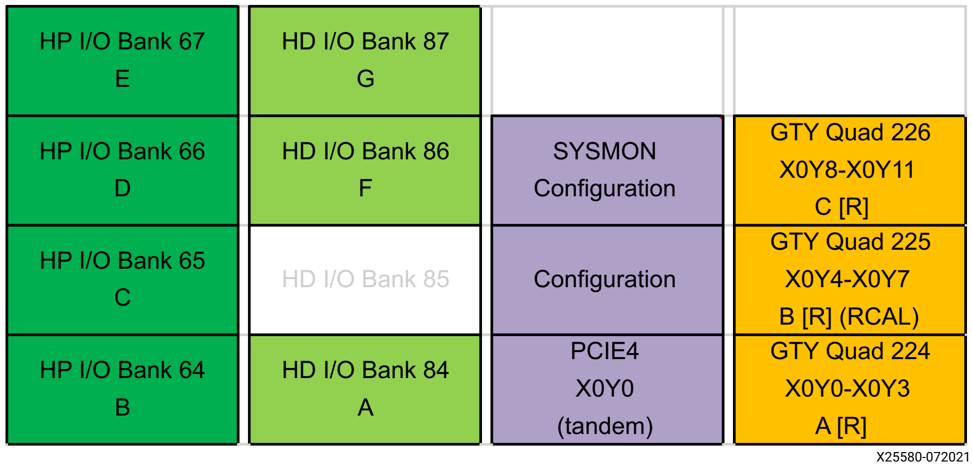

Figure 1-80: **XCAU25P Banks in FFVB676 Package**

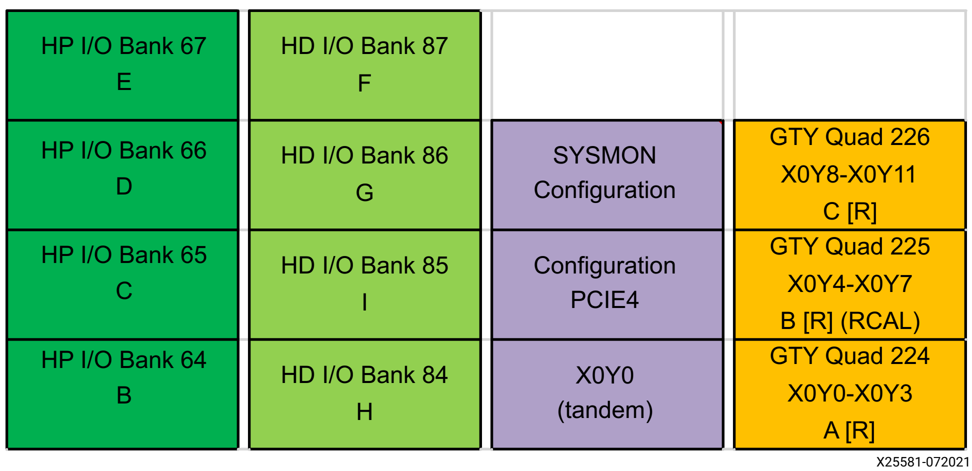

Figure 1-81: **XCAU25P Banks in SFVB784 Package**

XCKU3P Bank Diagrams

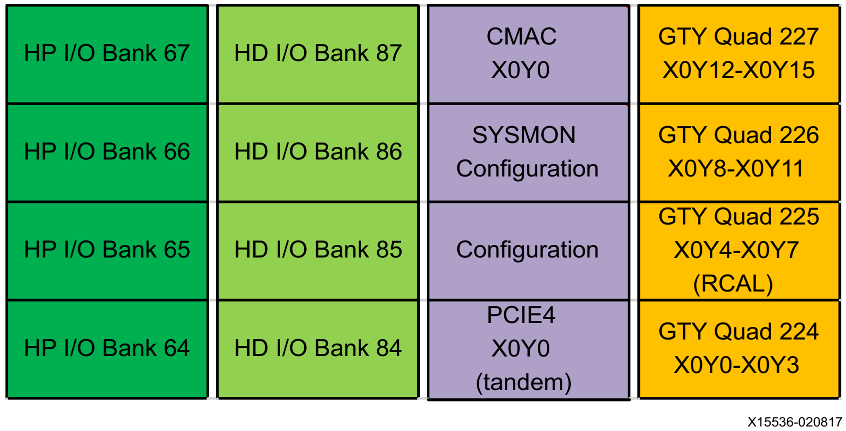

Figure 1-82: **XCKU3P Banks**

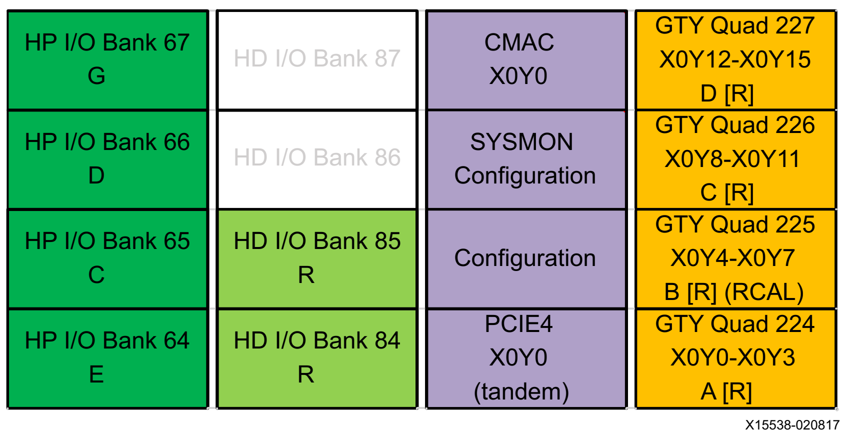

Figure 1-83: **XCKU3P Banks in FFVA676 Package**

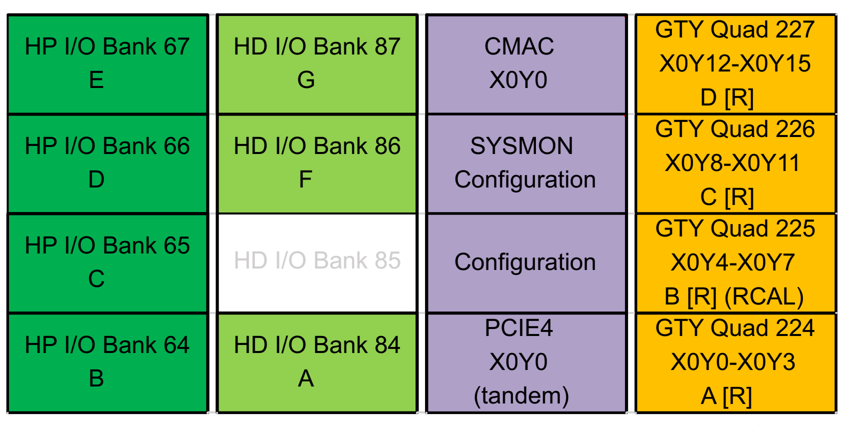

Figure 1-84: **XCKU3P Banks in FFVB676 Package**

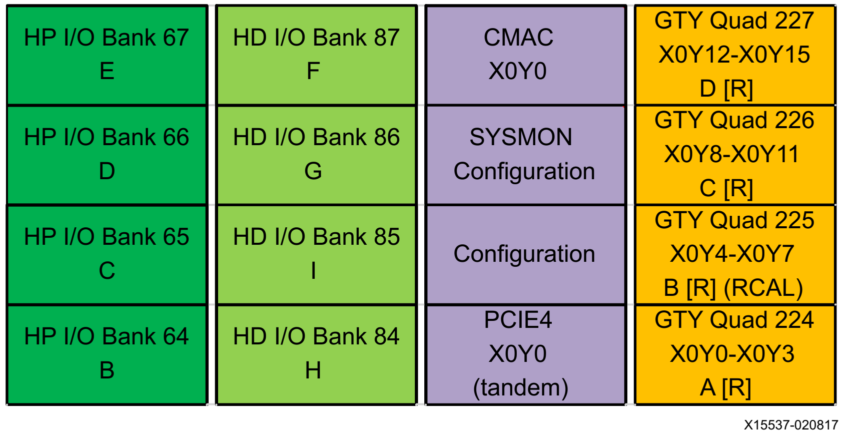

Figure 1-85: **XCKU3P Banks in SFVB784 Package**

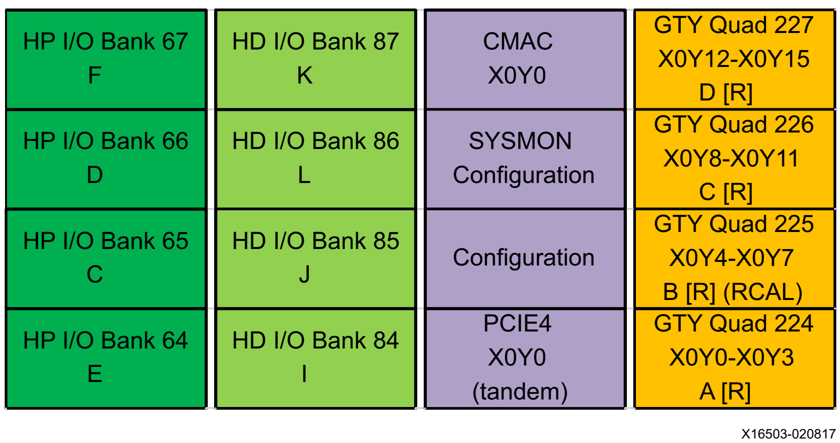

Figure 1-86: **XCKU3P Banks in FFVD900 Package**

XCKU5P and XQKU5P Bank Diagrams

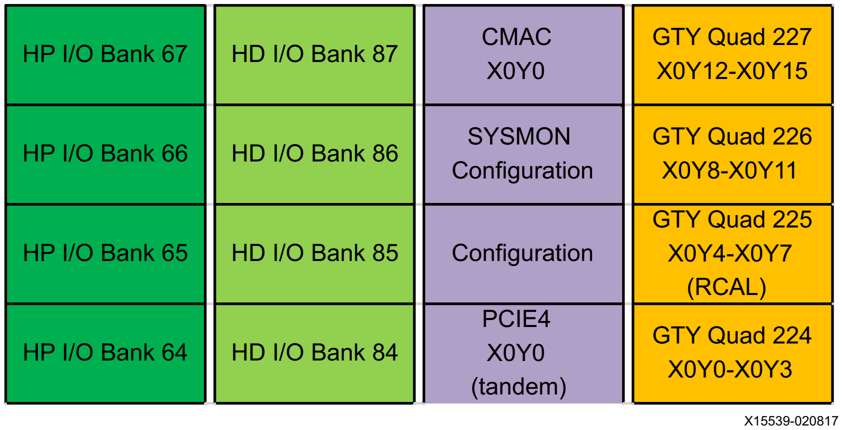

Figure 1-87: **XCKU5P and XQKU5P Banks**

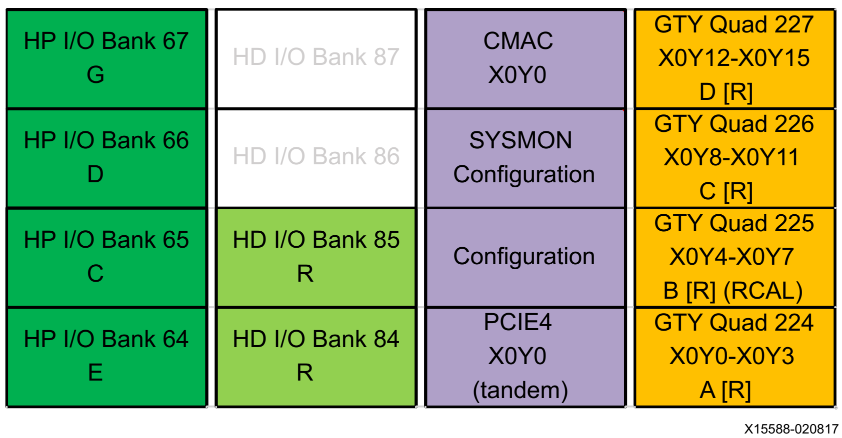

Figure 1-88: **XCKU5P Banks in FFVA676 Package**

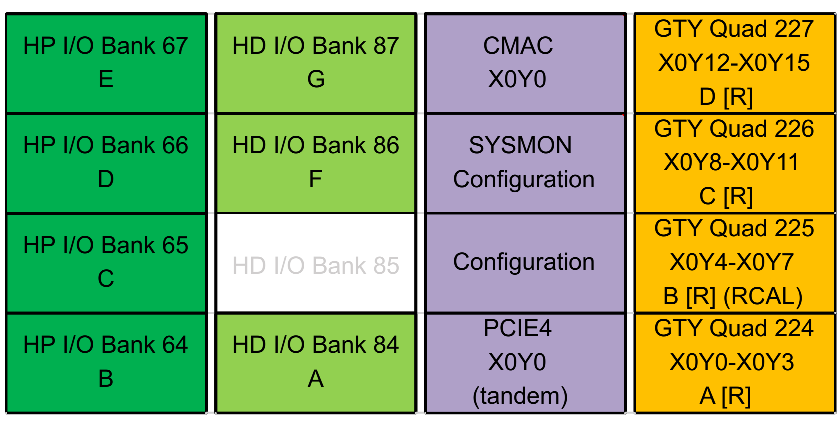

Figure 1-89: **XCKU5P Banks in FFVB676 Package and XQKU5P Banks in FFRB676 Package**

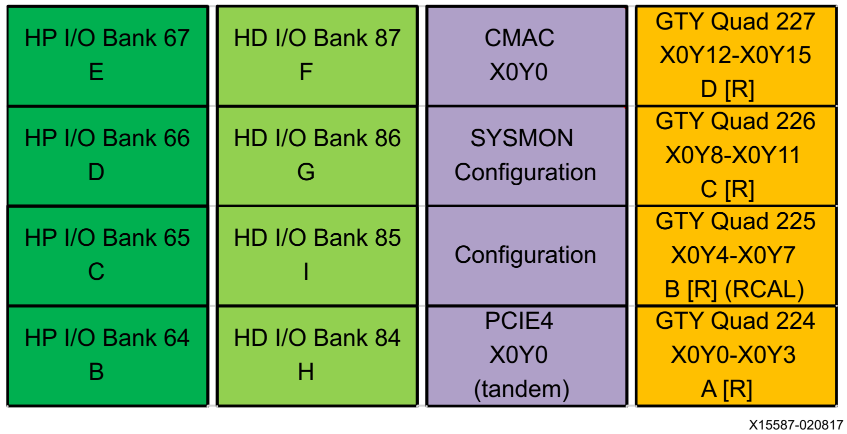

Figure 1-90: **XCKU5P Banks in SFVB784 Package and XQKU5P Banks in SFRB784 Package**

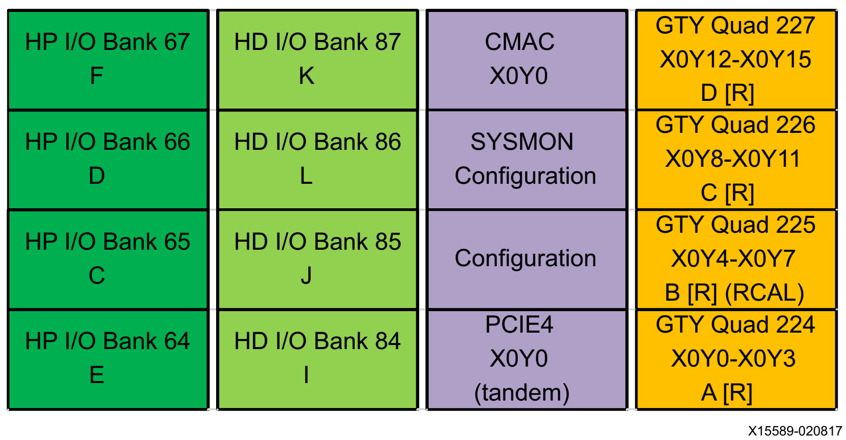

Figure 1-91: **XCKU5P Banks in FFVD900 Package**

XCKU9P Bank Diagrams

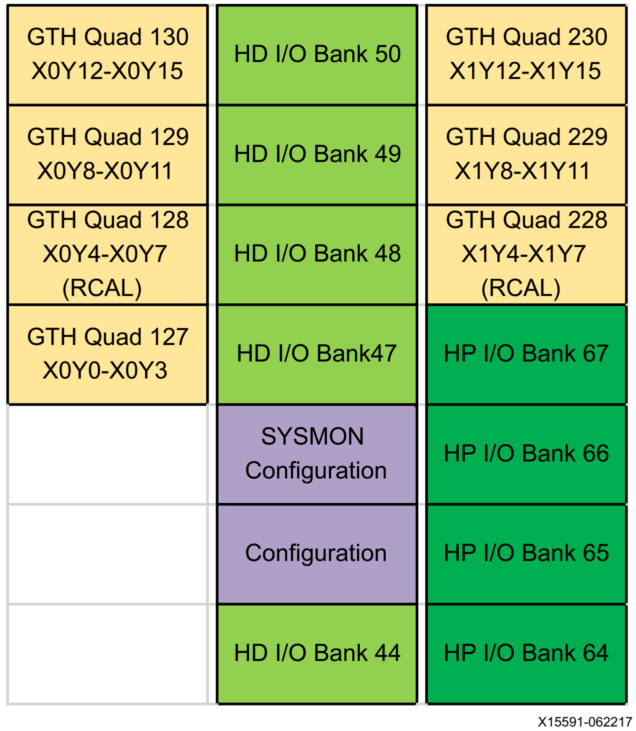

Figure 1-92: **XCKU9P Banks**

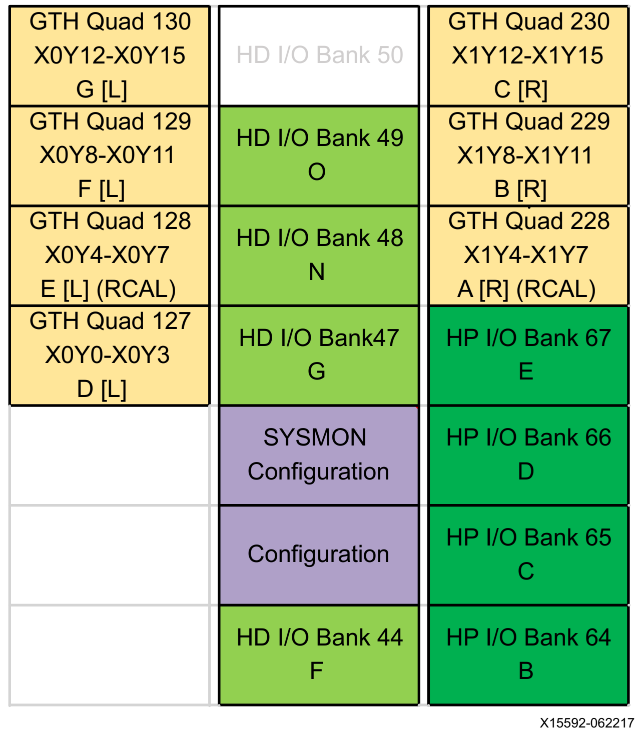

Figure 1-93: **XCKU9P Banks in FFVE900 Package**

XCKU11P Bank Diagrams

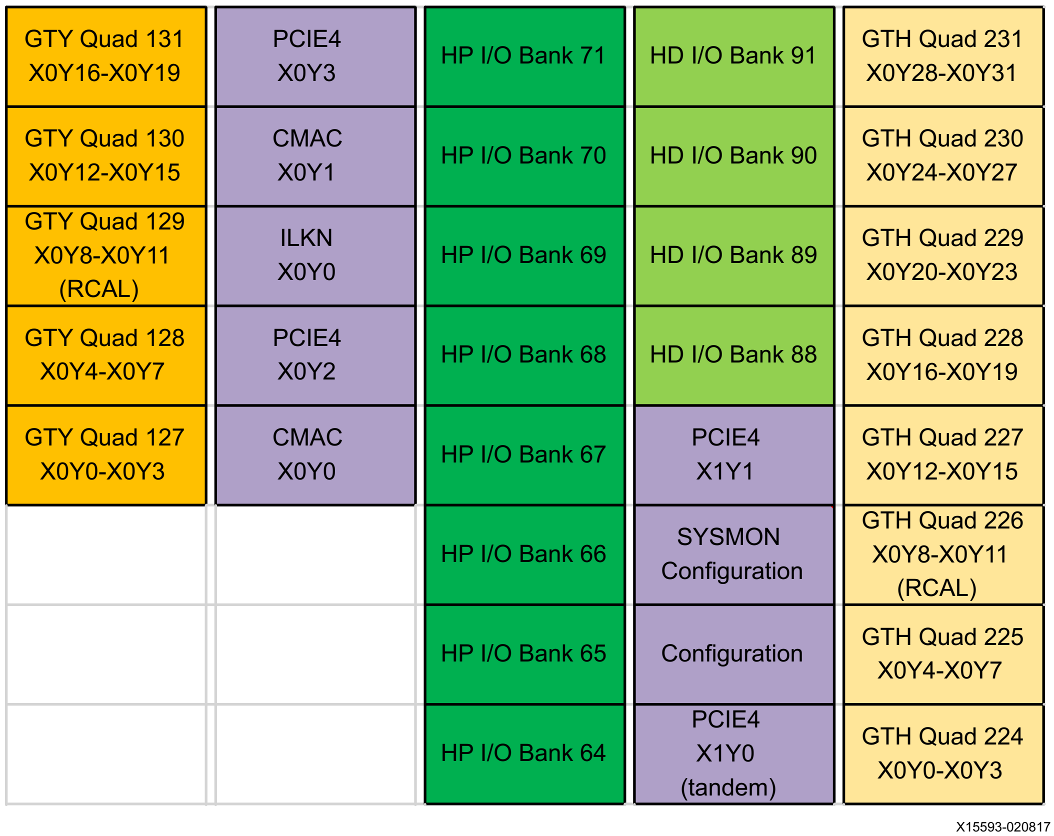

Figure 1-94: **XCKU11P Banks**

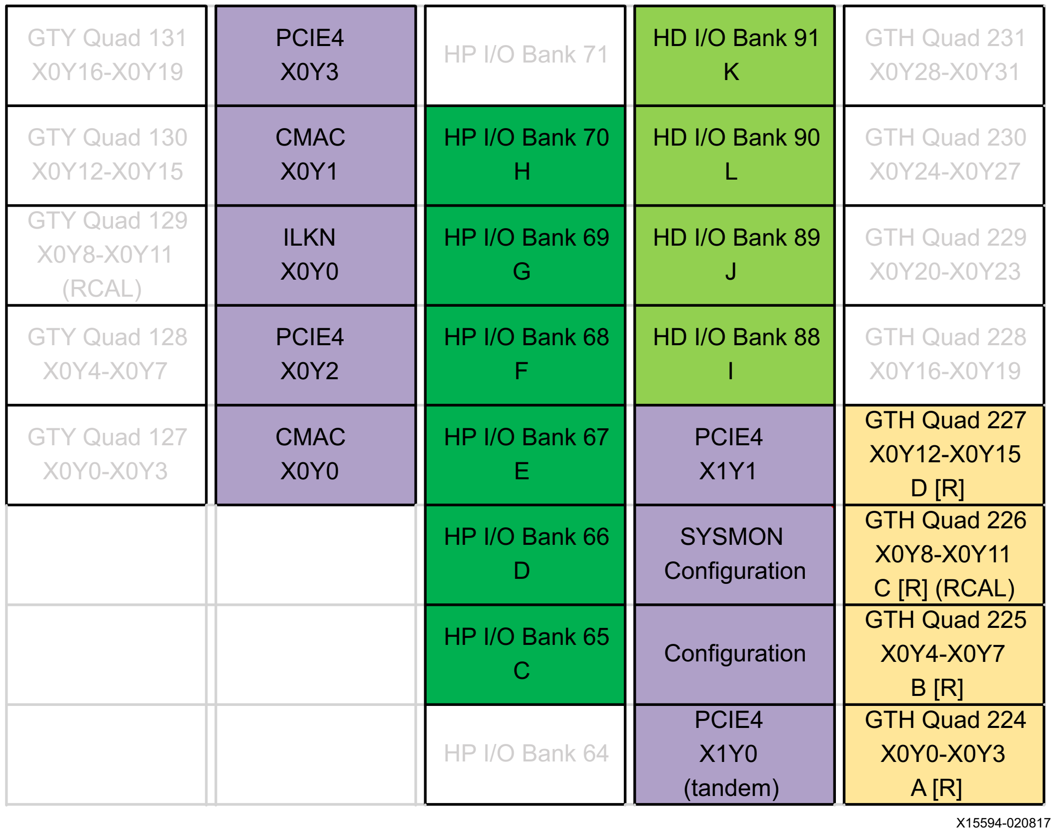

Figure 1-95: **XCKU11P Banks in FFVD900 Package**

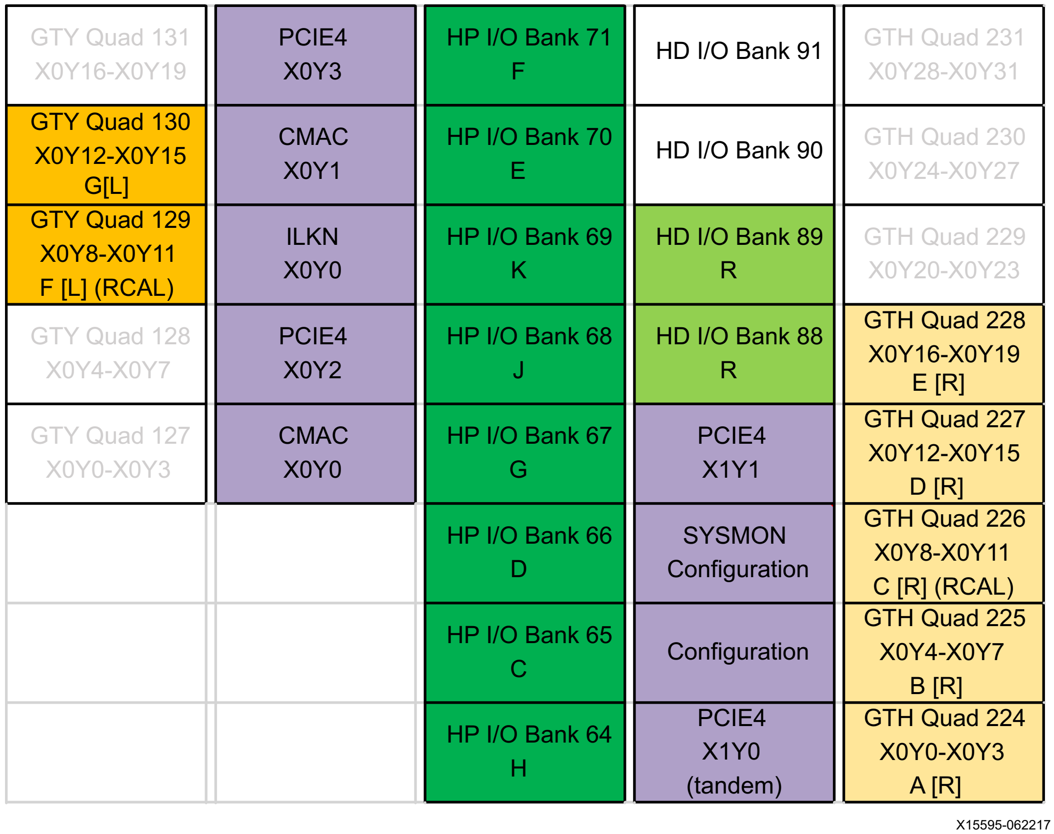

Figure 1-96: **XCKU11P Banks in FFVA1156 Package**

GTY Quad 131 X0Y16-X0Y19 M [L]	PCIE4 X0Y3	HP I/O Bank 71 R	HD I/O Bank 91 N	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y12-X0Y15 L [L]	CMAC X0Y1	HP I/O Bank 70 S	HD I/O Bank 90 O	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y8-X0Y11 K [L] (RCAL)	ILKN X0Y0	HP I/O Bank 69 T	HD I/O Bank 89 P	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y4-X0Y7 J [L]	PCIE4 X0Y2	HP I/O Bank 68 G	HD I/O Bank 88 Q	GTH Quad 228 X0Y16-X0Y19 E [RN]
GTY Quad 127 X0Y0-X0Y3 I [L]	CMAC X0Y0	HP I/O Bank 67 F	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [RS]
		HP I/O Bank 66 E	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
		HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
		HP I/O Bank 64 D	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-97: **XCKU11P Banks in FFVE1517 Package**

XCKU13P Bank Diagrams

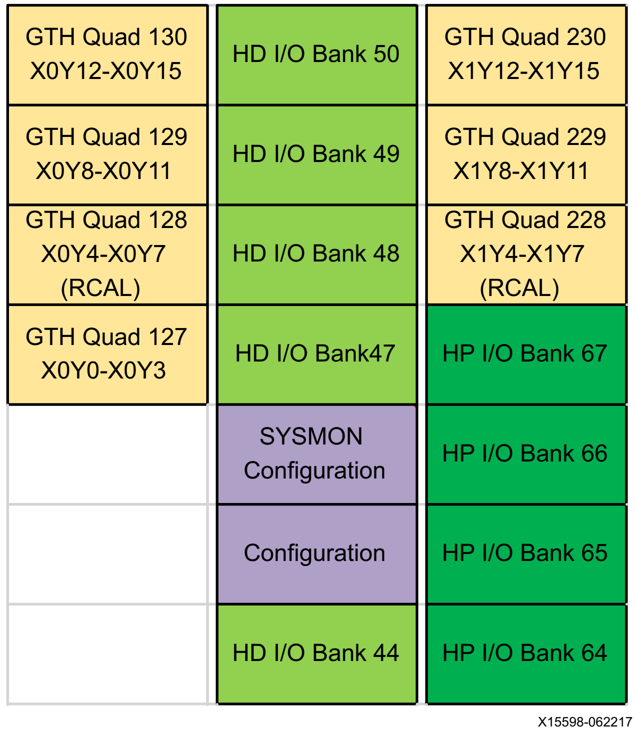

Figure 1-98: **XCKU13P Banks**

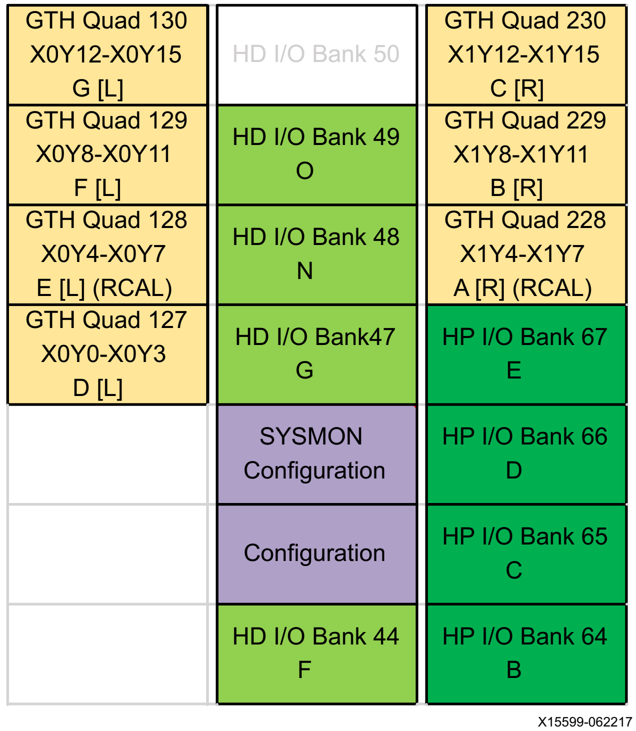

Figure 1-99: **XCKU13P Banks in FFVE900 Package**

XCKU15P and XQKU15P Bank Diagrams

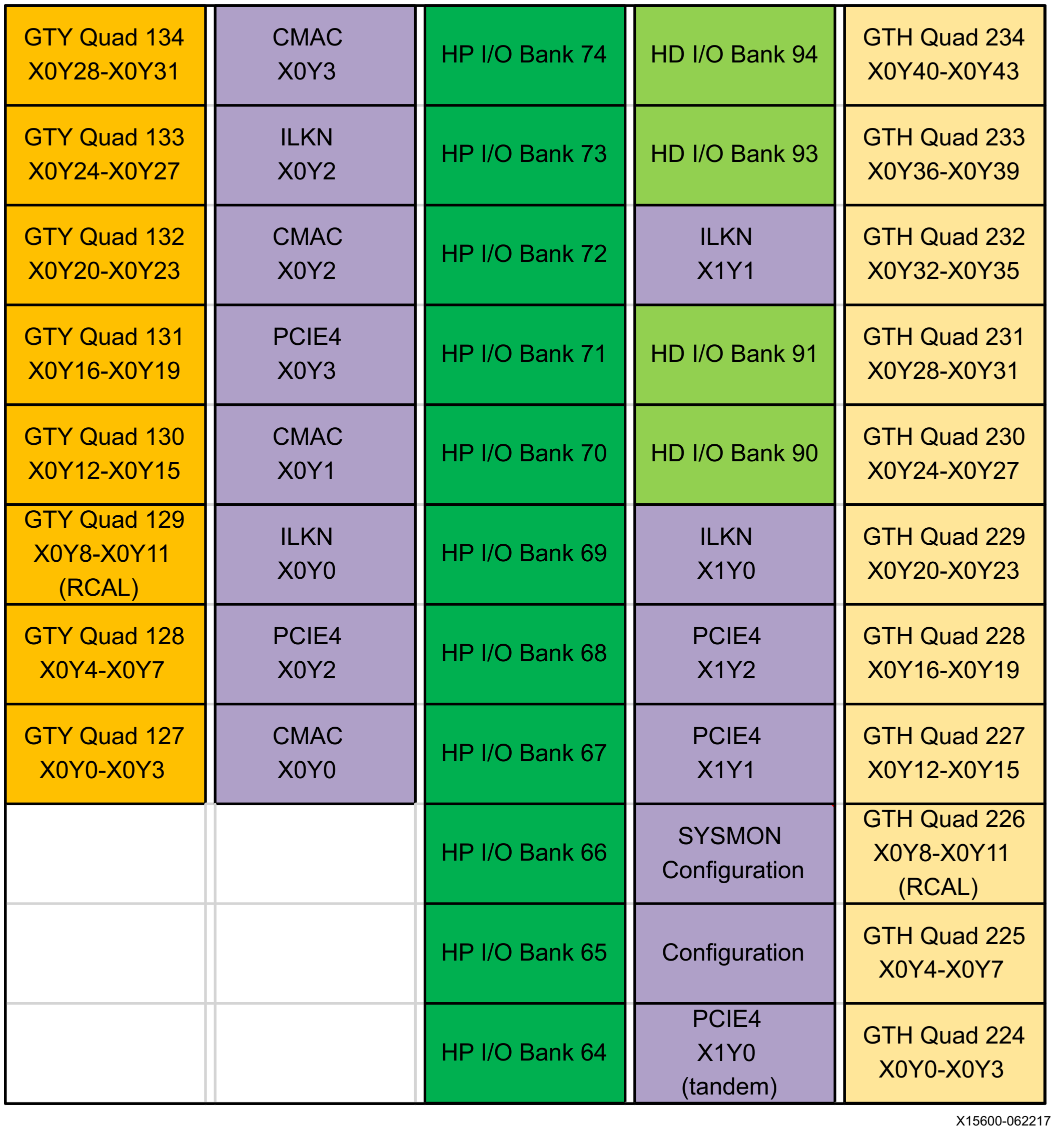

Figure 1-100: **XCKU15P and XQKU15P Banks**

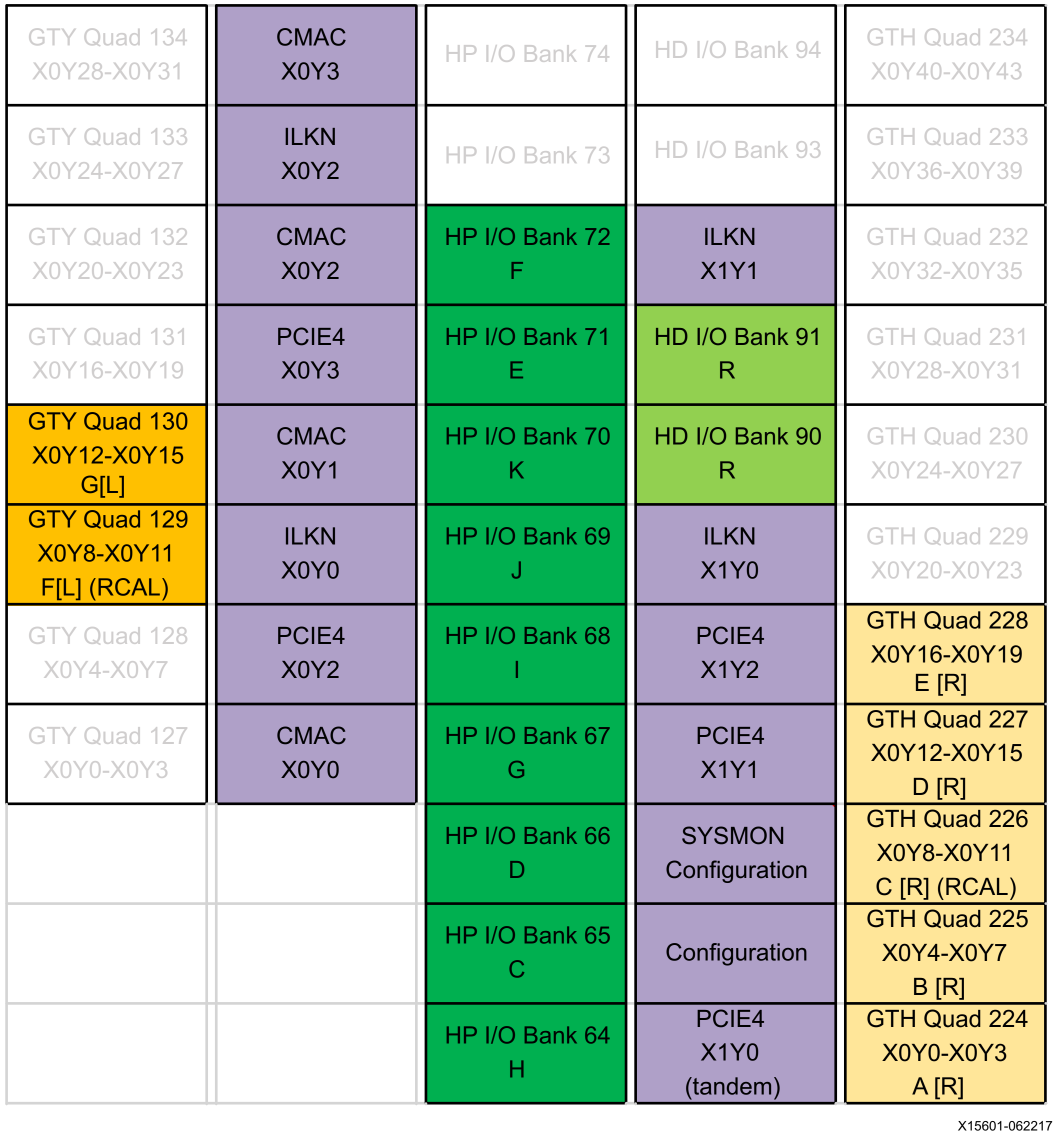

Figure 1-101: **XCKU15P Banks in FFVA1156 Package and XQKU15P in FFRA1156 Package**

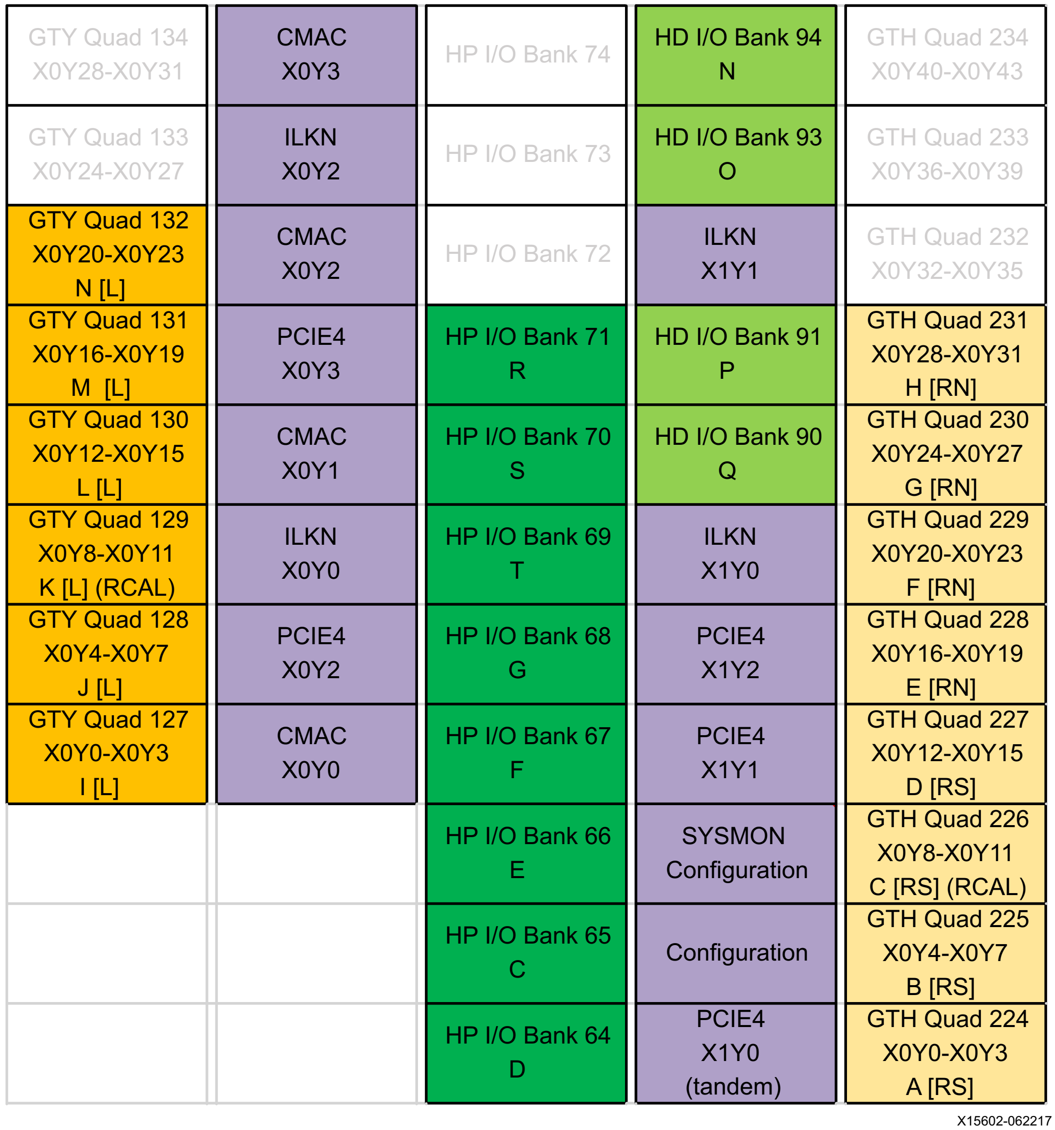

Figure 1-102: **XCKU15P Banks in FFVE1517 Package and XQKU15P Banks in FFRE1517 Package**

GTY Quad 134 X0Y28-X0Y31 S [LN]	CMAC X0Y3	HP I/O Bank 74	HD I/O Bank 94 N	GTH Quad 234 X0Y40-X0Y43 K [RN]
GTY Quad 133 X0Y24-X0Y27 R [LN]	ILKN X0Y2	HP I/O Bank 73	HD I/O Bank 93 O	GTH Quad 233 X0Y36-X0Y39 J [RN]
GTY Quad 132 X0Y20-X0Y23 Q [LN]	CMAC X0Y2	HP I/O Bank 72 R	ILKN X1Y1	GTH Quad 232 X0Y32-X0Y35 I [RN]
GTY Quad 131 X0Y16-X0Y19 P [LN]	PCIE4 X0Y3	HP I/O Bank 71 S	HD I/O Bank 91 P	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y12-X0Y15 O [LS]	CMAC X0Y1	HP I/O Bank 70 T	HD I/O Bank 90 Q	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y8-X0Y11 N [LS] (RCAL)	ILKN X0Y0	HP I/O Bank 69	ILKN X1Y0	GTH Quad 229 X0Y20-X0Y23 F [RS]
GTY Quad 128 X0Y4-X0Y7 M [LS]	PCIE4 X0Y2	HP I/O Bank 68 G	PCIE4 X1Y2	GTH Quad 228 X0Y16-X0Y19 E [RS]
GTY Quad 127 X0Y0-X0Y3 L [LS]	CMAC X0Y0	HP I/O Bank 67 F	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [RS]
		HP I/O Bank 66 E	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
		HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
		HP I/O Bank 64 D	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-103: **XCKU15P Banks in FFVA1760 Package**

GTY Quad 134 X0Y28-X0Y31	CMAC X0Y3	HP I/O Bank 74 R	HD I/O Bank 94 N	GTH Quad 234 X0Y40-X0Y43
GTY Quad 133 X0Y24-X0Y27	ILKN X0Y2	HP I/O Bank 73 S	HD I/O Bank 93 O	GTH Quad 233 X0Y36-X0Y39
GTY Quad 132 X0Y20-X0Y23 N [L]	CMAC X0Y2	HP I/O Bank 72 T	ILKN X1Y1	GTH Quad 232 X0Y32-X0Y35
GTY Quad 131 X0Y16-X0Y19 M [L]	PCIE4 X0Y3	HP I/O Bank 71 U	HD I/O Bank 91 P	GTH Quad 231 X0Y28-X0Y31 H [RN]
GTY Quad 130 X0Y12-X0Y15 L [L]	CMAC X0Y1	HP I/O Bank 70 V	HD I/O Bank 90 Q	GTH Quad 230 X0Y24-X0Y27 G [RN]
GTY Quad 129 X0Y8-X0Y11 K [L] (RCAL)	ILKN X0Y0	HP I/O Bank 69 H	ILKN X1Y0	GTH Quad 229 X0Y20-X0Y23 F [RN]
GTY Quad 128 X0Y4-X0Y7 J [L]	PCIE4 X0Y2	HP I/O Bank 68 G	PCIE4 X1Y2	GTH Quad 228 X0Y16-X0Y19 E [RN]
GTY Quad 127 X0Y0-X0Y3 I [L]	CMAC X0Y0	HP I/O Bank 67 F	PCIE4 X1Y1	GTH Quad 227 X0Y12-X0Y15 D [RS]
		HP I/O Bank 66 E	SYSMON Configuration	GTH Quad 226 X0Y8-X0Y11 C [RS] (RCAL)
		HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y4-X0Y7 B [RS]
		HP I/O Bank 64 D	PCIE4 X1Y0 (tandem)	GTH Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-104: **XCKU15P Banks in FFVE1760 Package**

XCKU19P Bank Diagrams

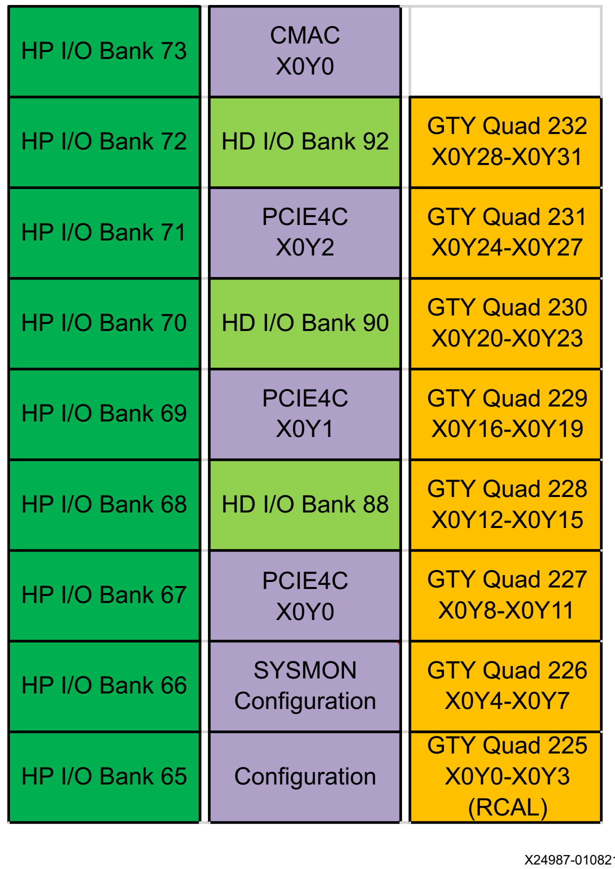

Figure 1-105: **XCKU19P Banks**

IMPORTANT: *Tandem configuration is not supported for any PCIE4C instance in XCKU19P banks.*

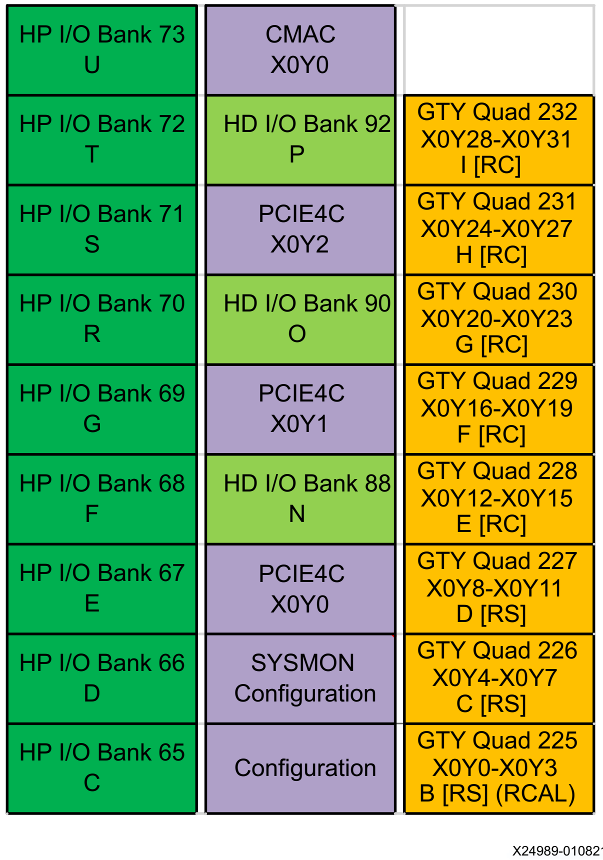

Figure 1-106: **XCKU19P Banks in FFVJ1760 Package**

IMPORTANT: *Tandem configuration is not supported for any PCIE4C instance in XCKU19P banks.*

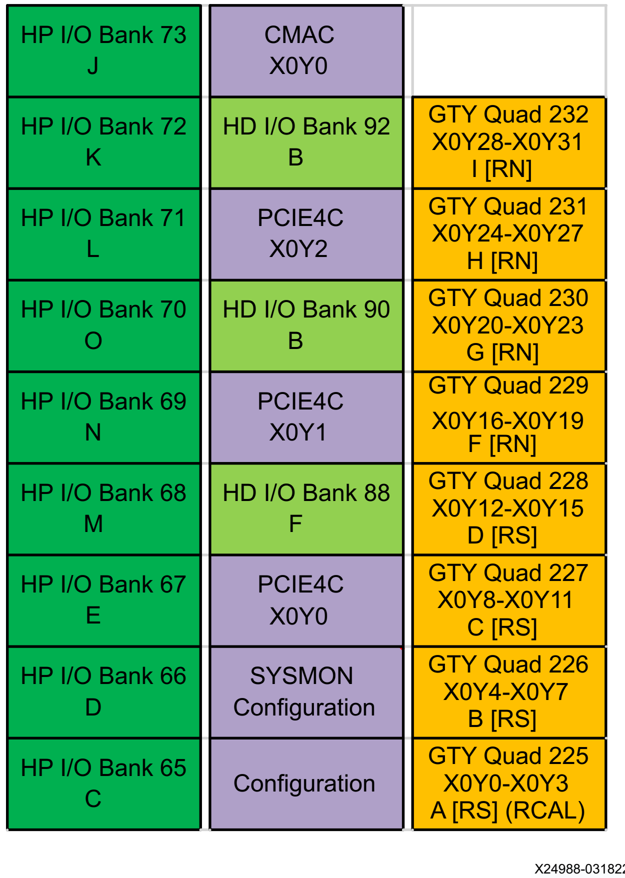

Figure 1-107: **XCKU19P Banks in FFVB2104 Package**

IMPORTANT: *Tandem configuration is not supported for any PCIE4C instance in XCKU19P banks.*

XCVU3P and XQVU3P Bank Diagrams

GTY Quad 128 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68	ILKN X1Y2	GTY Quad 228 X1Y16-X1Y19
GTY Quad 127 X0Y12-X0Y15	PCIE4 X0Y1	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y1	GTY Quad 227 X1Y12-X1Y15
GTY Quad 126 X0Y8-X0Y11 (RCAL)	CMAC X0Y1	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11 (RCAL)
GTY Quad 125 X0Y4-X0Y7	ILKN X0Y0	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTY Quad 225 X1Y4-X1Y7
GTY Quad 124 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 44	HP I/O Bank 64	PCIE4 X1Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3

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Figure 1-108: **XCVU3P and XQVU3P Banks**

GTY Quad 128 X0Y16-X0Y19 J [L]	CMAC X0Y2	HP I/O Bank 48 K	HP I/O Bank 68 F	ILKN X1Y2	GTY Quad 228 X1Y16-X1Y19 E [R]
GTY Quad 127 X0Y12-X0Y15 I [L]	PCIE4 X0Y1	HP I/O Bank 47 J	HP I/O Bank 67 E	ILKN X1Y1	GTY Quad 227 X1Y12-X1Y15 D [R]
GTY Quad 126 X0Y8-X0Y11 H [L] (RCAL)	CMAC X0Y1	HP I/O Bank 46 I	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11 C [R] (RCAL)
GTY Quad 125 X0Y4-X0Y7 G [L]	ILKN X0Y0	HP I/O Bank 45 H	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y4-X1Y7 B [R]
GTY Quad 124 X0Y0-X0Y3 F [L]	CMAC X0Y0	HP I/O Bank 44 G	HP I/O Bank 64 B	PCIE4 X1Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3 A [R]

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Figure 1-109: **XCVU3P Banks in FFVC1517 Package and XQVU3P Banks in FFRC1517 Package**

XCVU5P Bank Diagrams

GTY Quad 133 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y5	GTY Quad 233 X1Y36-X1Y39
GTY Quad 132 X0Y32-X0Y35	PCIE4 X0Y3	HP I/O Bank 52	HP I/O Bank 72	ILKN X1Y4	GTY Quad 232 X1Y32-X1Y35
GTY Quad 131 X0Y28-X0Y31 (RCAL)	CMAC X0Y4	HP I/O Bank 51	HP I/O Bank 71	SYSMON Configuration	GTY Quad 231 X1Y28-X1Y31 (RCAL)
GTY Quad 130 X0Y24-X0Y27	ILKN X0Y3	HP I/O Bank 50	HP I/O Bank 70	Configuration	GTY Quad 230 X1Y24-X1Y27
GTY Quad 129 X0Y20-X0Y23	CMAC X0Y3	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y2	GTY Quad 229 X1Y20-X1Y23
SLR Crossing					
GTY Quad 128 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 48	HP I/O Bank 68	ILKN X1Y2	GTY Quad 228 X1Y16-X1Y19
GTY Quad 127 X0Y12-X0Y15	PCIE4 X0Y1	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y1	GTY Quad 227 X1Y12-X1Y15
GTY Quad 126 X0Y8-X0Y11 (RCAL)	CMAC X0Y1	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y1 (RCAL)
GTY Quad 125 X0Y4-X0Y7	ILKN X0Y0	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTY Quad 225 X1Y4-X1Y7
GTY Quad 124 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 44	HP I/O Bank 64	PCIE4 X1Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3

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Figure 1-110: **XCVU5P Banks**

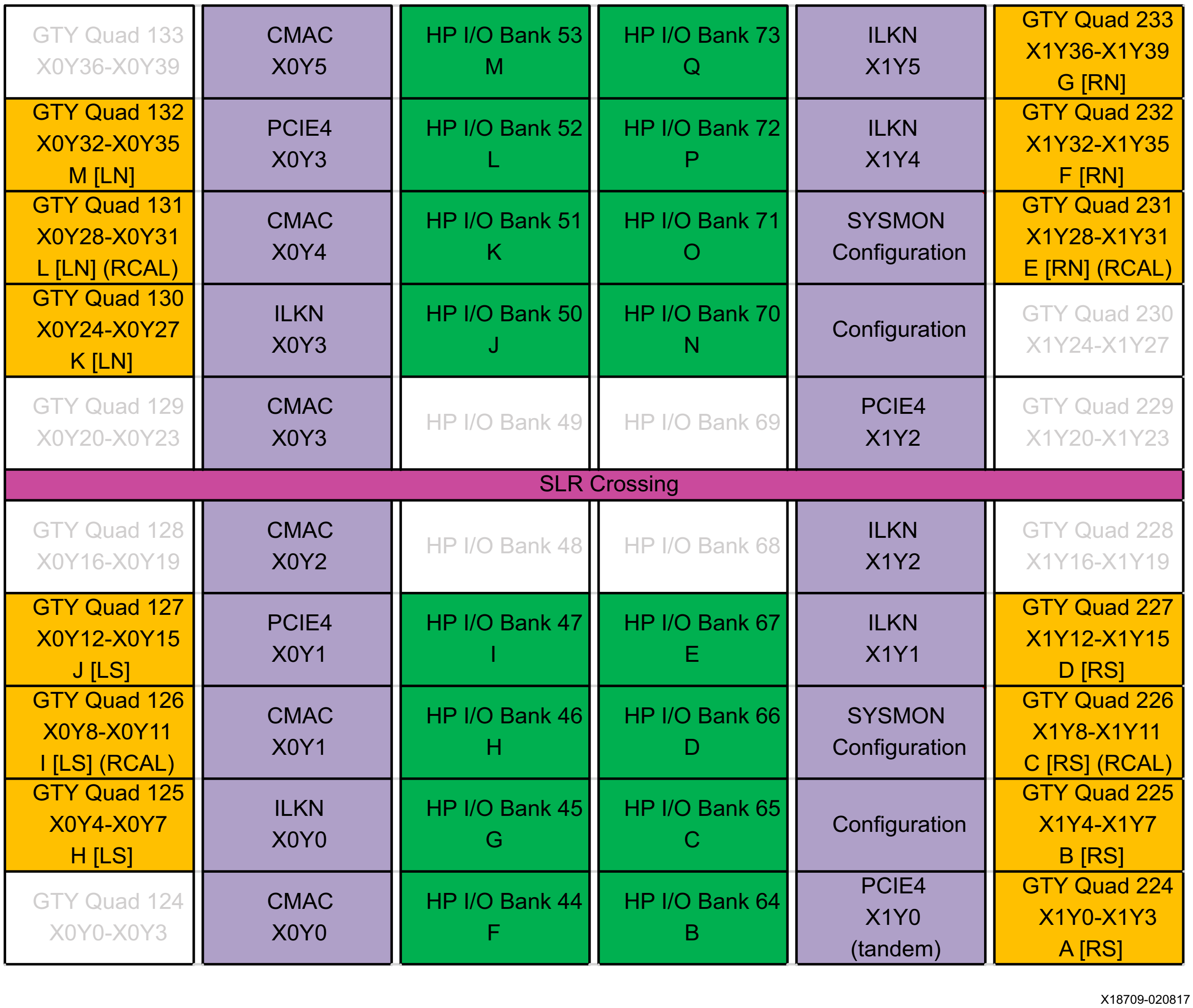

Figure 1-111: **XCVU5P Banks in FLVA2104 Package**

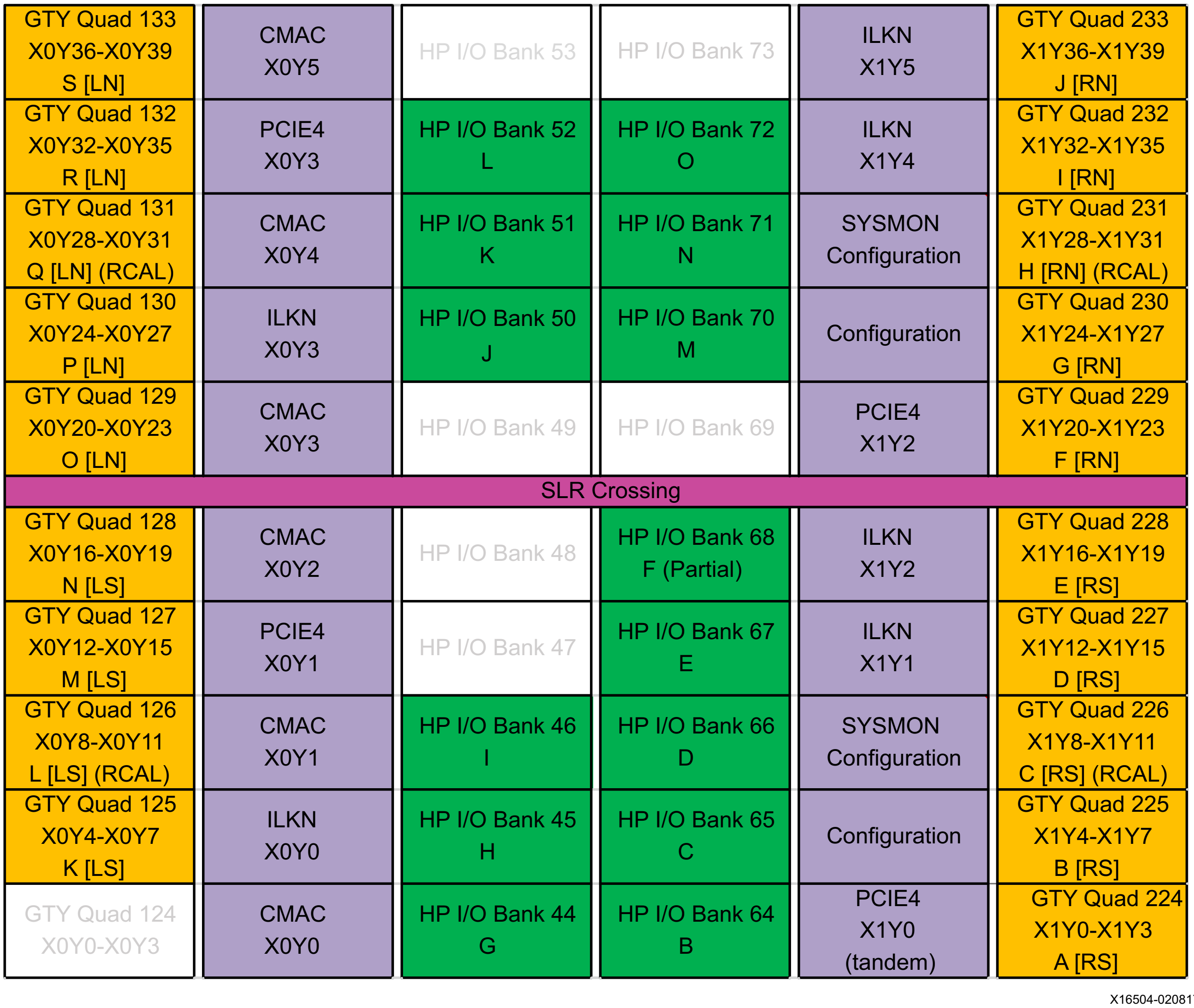

Figure 1-112: **XCVU5P Banks in FLVB2104 Package**

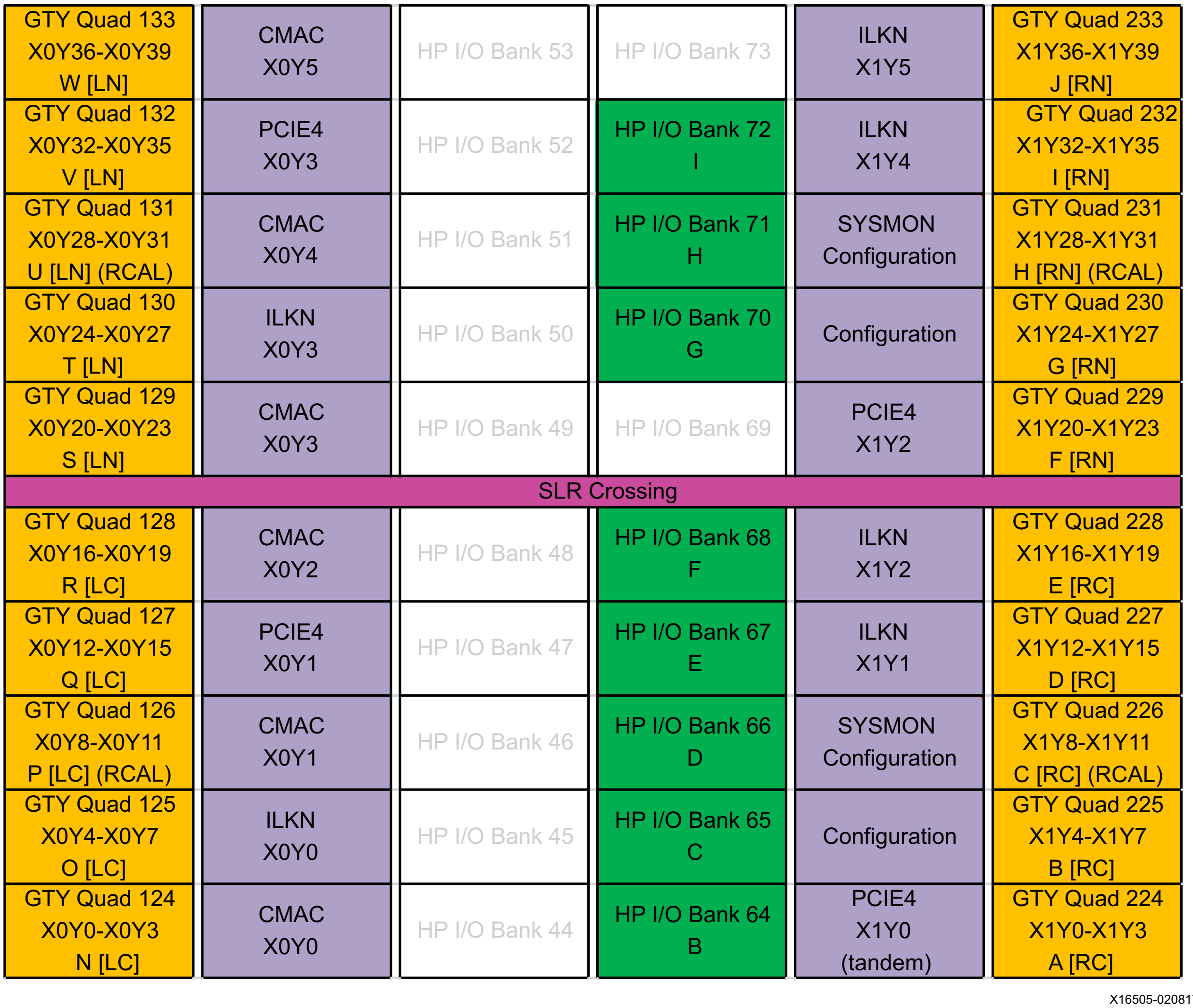

Figure 1-113: **XCVU5P Banks in FLVC2104 Package**

XCVU7P and XQVU7P Bank Diagrams

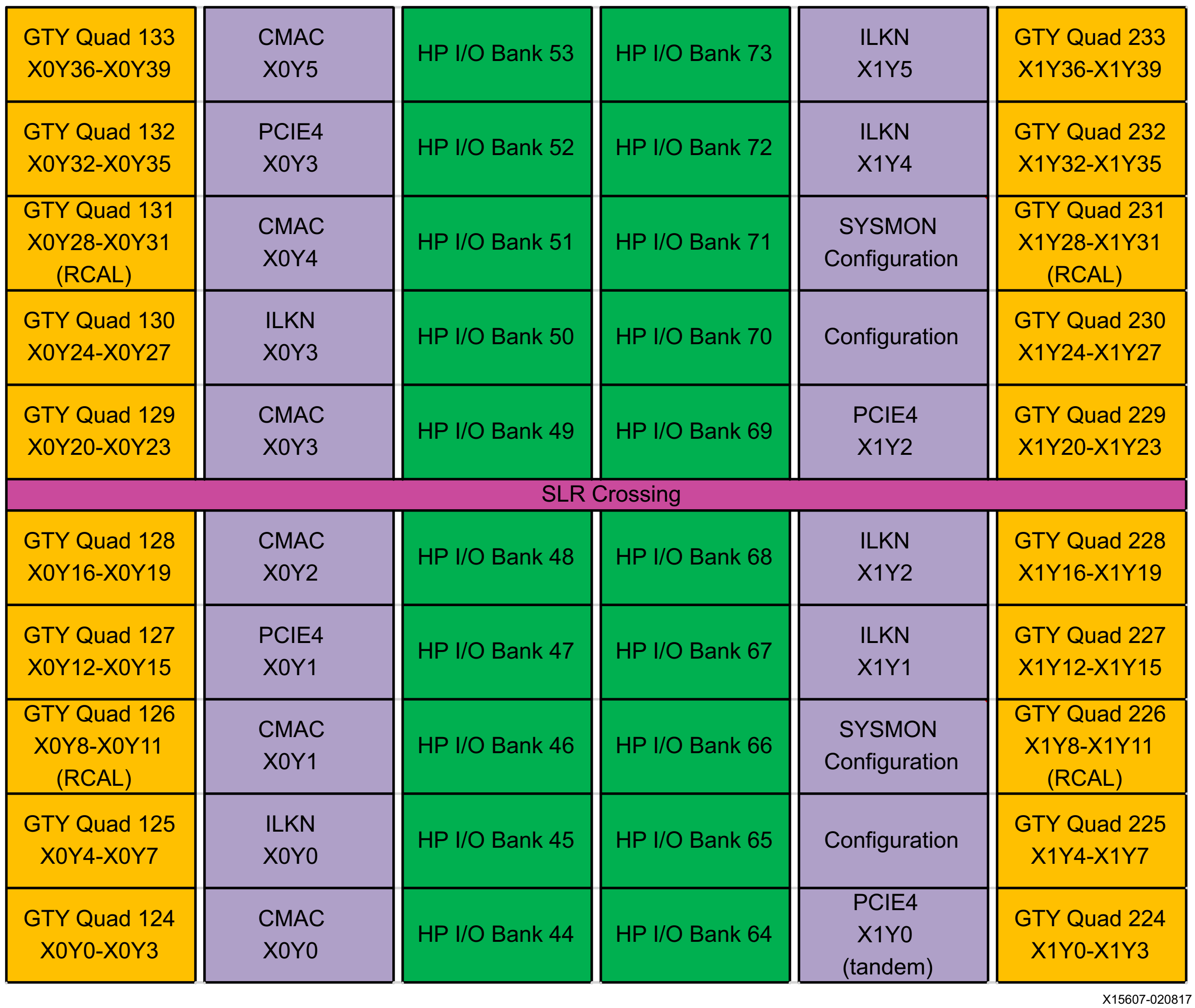

Figure 1-114: **XCVU7P and XQVU7P Banks**

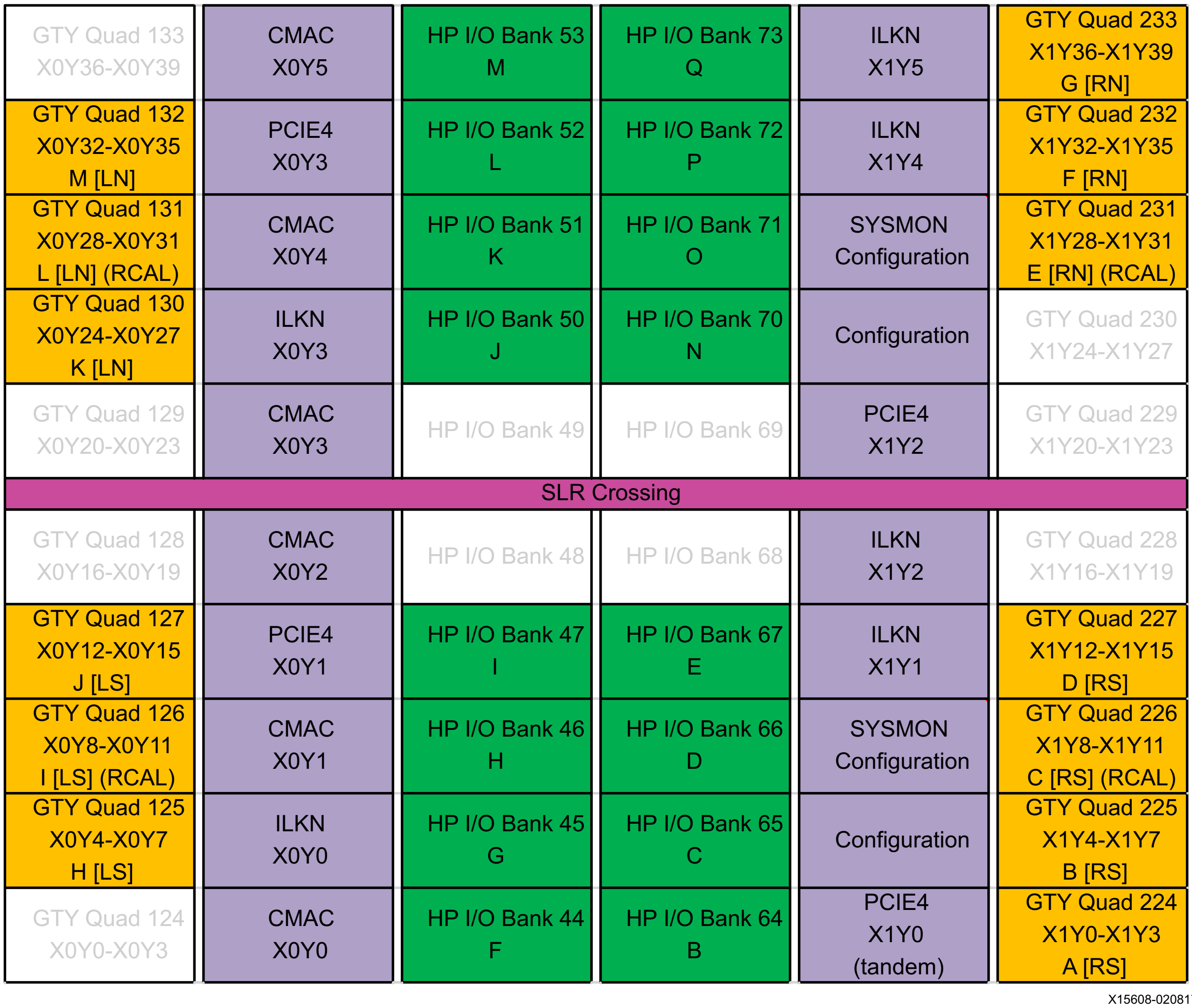

Figure 1-115: **XCVU7P Banks in FLVA2104 Package and XQVU7P in FLRA2104 Package**

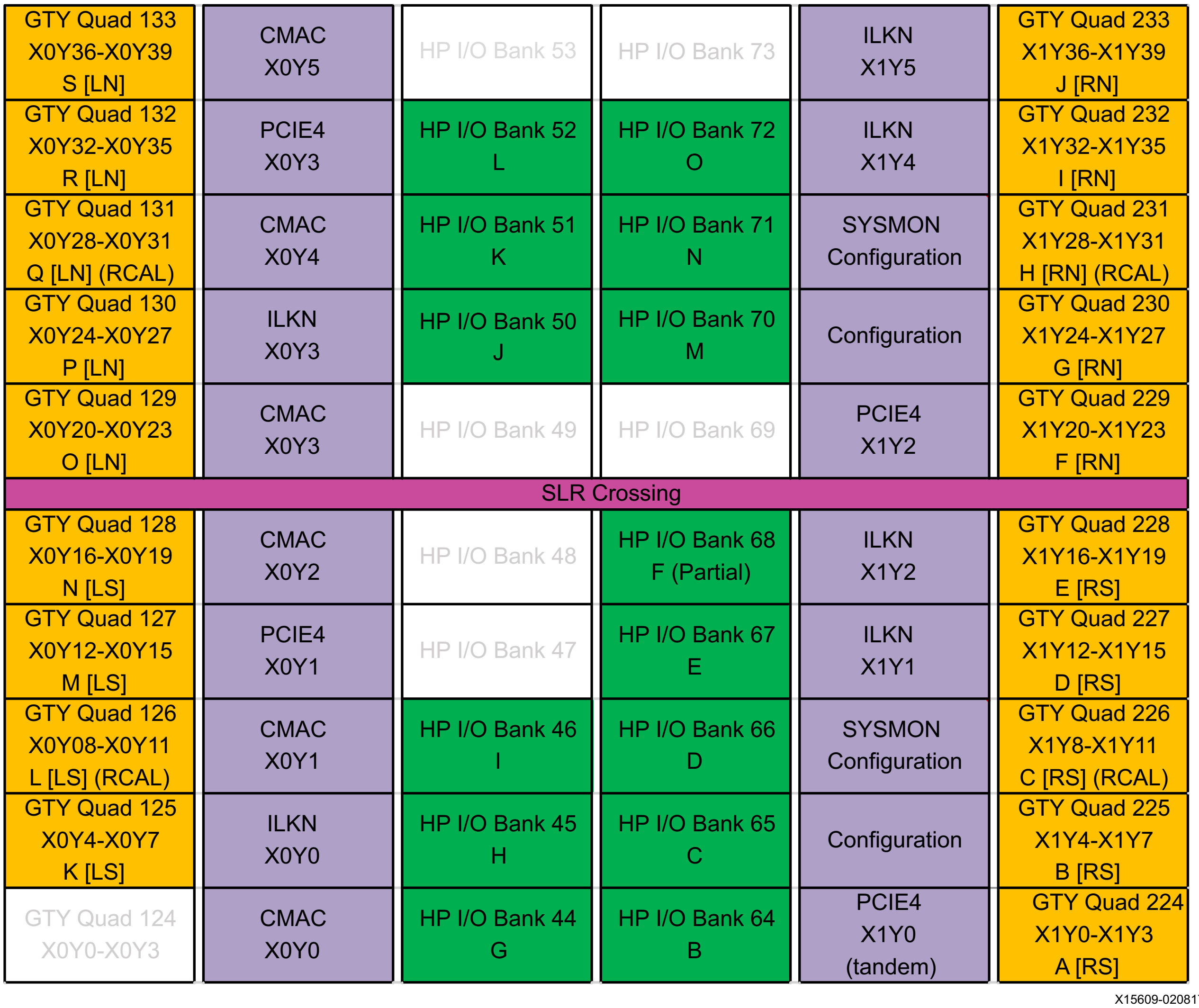

Figure 1-116: **XCVU7P Banks in FLVB2104 Package and XQVU7P in FLRB2104 Package**

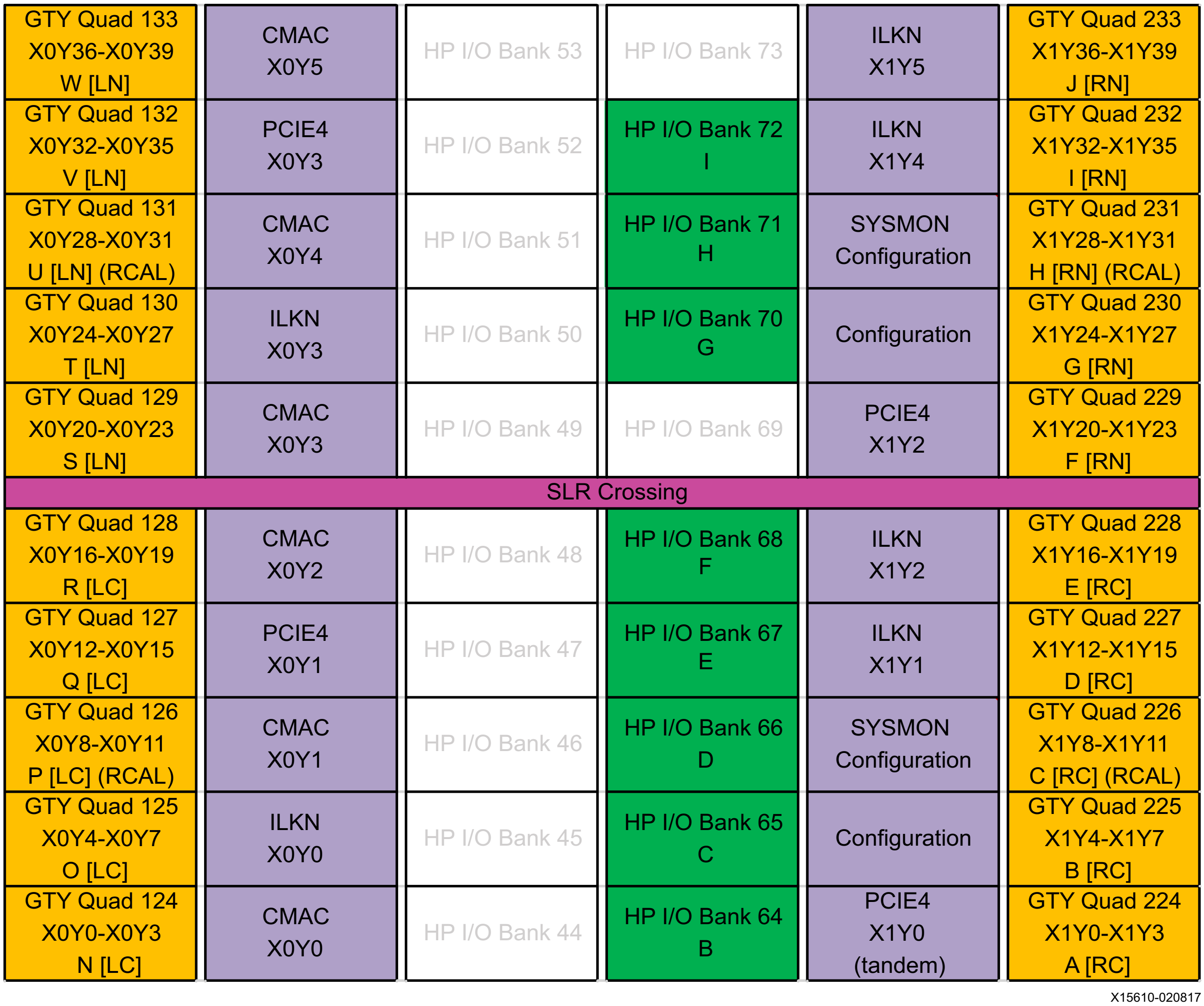

Figure 1-117: **XCVU7P Banks in FLVC2104 Package**

XCVU9P Bank Diagrams

GTY Quad 133 X0Y56-X0Y59	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y8	GTY Quad 233 X1Y56-X1Y59
GTY Quad 132 X0Y52-X0Y55	PCIE4 X0Y5	HP I/O Bank 52	HP I/O Bank 72	ILKN X1Y7	GTY Quad 232 X1Y52-X1Y55
GTY Quad 131 X0Y48-X0Y51 (RCAL)	CMAC X0Y7	HP I/O Bank 51	HP I/O Bank 71	SYSMON Configuration	GTY Quad 231 X1Y48-X1Y51 (RCAL)
GTY Quad 130 X0Y44-X0Y47	ILKN X0Y6	HP I/O Bank 50	HP I/O Bank 70	Configuration	GTY Quad 230 X1Y44-X1Y47
GTY Quad 129 X0Y40-X0Y43	CMAC X0Y6	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y4	GTY Quad 229 X1Y40-X1Y43
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68	ILKN X1Y5	GTY Quad 228 X1Y36-X1Y39
GTY Quad 127 X0Y32-X0Y35	PCIE4 X0Y3	HP I/O Bank 47	HP I/O Bank 67	ILKN X1Y4	GTY Quad 227 X1Y32-X1Y35
GTY Quad 126 X0Y28-X0Y31 (RCAL)	CMAC X0Y4	HP I/O Bank 46	HP I/O Bank 66	SYSMON Configuration	GTY Quad 226 X1Y28-X1Y31 (RCAL)
GTY Quad 125 X0Y24-X0Y27	ILKN X0Y3	HP I/O Bank 45	HP I/O Bank 65	Configuration	GTY Quad 225 X1Y24-X1Y27
GTY Quad 124 X0Y20-X0Y23	CMAC X0Y3	HP I/O Bank 44	HP I/O Bank 64	PCIE4 X1Y2 (tandem)	GTY Quad 224 X1Y20-X1Y23
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	ILKN X1Y2	GTY Quad 223 X1Y16-X1Y19
GTY Quad 122 X0Y12-X0Y15	PCIE4 X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y1	GTY Quad 222 X1Y12-X1Y15
GTY Quad 121 X0Y8-X0Y11 (RCAL)	CMAC X0Y1	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTY Quad 221 X1Y8-X1Y11 (RCAL)
GTY Quad 120 X0Y4-X0Y7	ILKN X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTY Quad 220 X1Y4-X1Y7
GTY Quad 119 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 39	HP I/O Bank 59	PCIE4 X1Y0	GTY Quad 219 X1Y0-X1Y3

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Figure 1-118: **XCVU9P Banks**

GTY Quad 133 X0Y56-X0Y59	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73 Q	ILKN X1Y8	GTY Quad 233 X1Y56-X1Y59 G [RN]
GTY Quad 132 X0Y52-X0Y55	PCIE4 X0Y5	HP I/O Bank 52	HP I/O Bank 72 P	ILKN X1Y7	GTY Quad 232 X1Y52-X1Y55 F [RN]
GTY Quad 131 X0Y48-X0Y51 (RCAL)	CMAC X0Y7	HP I/O Bank 51	HP I/O Bank 71 O	SYSMON Configuration	GTY Quad 231 X1Y48-X1Y51 E [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47	ILKN X0Y6	HP I/O Bank 50	HP I/O Bank 70 N	Configuration	GTY Quad 230 X1Y44-X1Y47
GTY Quad 129 X0Y40-X0Y43	CMAC X0Y6	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y4	GTY Quad 229 X1Y40-X1Y43
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 48 M	HP I/O Bank 68	ILKN X1Y5	GTY Quad 228 X1Y36-X1Y39
GTY Quad 127 X0Y32-X0Y35 M [LN]	PCIE4 X0Y3	HP I/O Bank 47 L	HP I/O Bank 67 E	ILKN X1Y4	GTY Quad 227 X1Y32-X1Y35 D [RS]
GTY Quad 126 X0Y28-X0Y31 L [LN] (RCAL)	CMAC X0Y4	HP I/O Bank 46 K	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y28-X1Y31 C [RS] (RCAL)
GTY Quad 125 X0Y24-X0Y27 K [LN]	ILKN X0Y3	HP I/O Bank 45 J	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y24-X1Y27 B [RS]
GTY Quad 124 X0Y20-X0Y23	CMAC X0Y3	HP I/O Bank 44	HP I/O Bank 64 B	PCIE4 X1Y2 (tandem)	GTY Quad 224 X1Y20-X1Y23 A [RS]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43 I	HP I/O Bank 63	ILKN X1Y2	GTY Quad 223 X1Y16-X1Y19
GTY Quad 122 X0Y12-X0Y15 J [LS]	PCIE4 X0Y1	HP I/O Bank 42 H	HP I/O Bank 62	ILKN X1Y1	GTY Quad 222 X1Y12-X1Y15
GTY Quad 121 X0Y8-X0Y11 I [LS] (RCAL)	CMAC X0Y1	HP I/O Bank 41 G	HP I/O Bank 61	SYSMON Configuration	GTY Quad 221 X1Y8-X1Y11 (RCAL)
GTY Quad 120 X0Y4-X0Y7 H [LS]	ILKN X0Y0	HP I/O Bank 40 F	HP I/O Bank 60	Configuration	GTY Quad 220 X1Y4-X1Y7
GTY Quad 119 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 39	HP I/O Bank 59	PCIE4 X1Y0	GTY Quad 219 X1Y0-X1Y3

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Figure 1-119: **XCVU9P Banks in FLGA2104 Package**

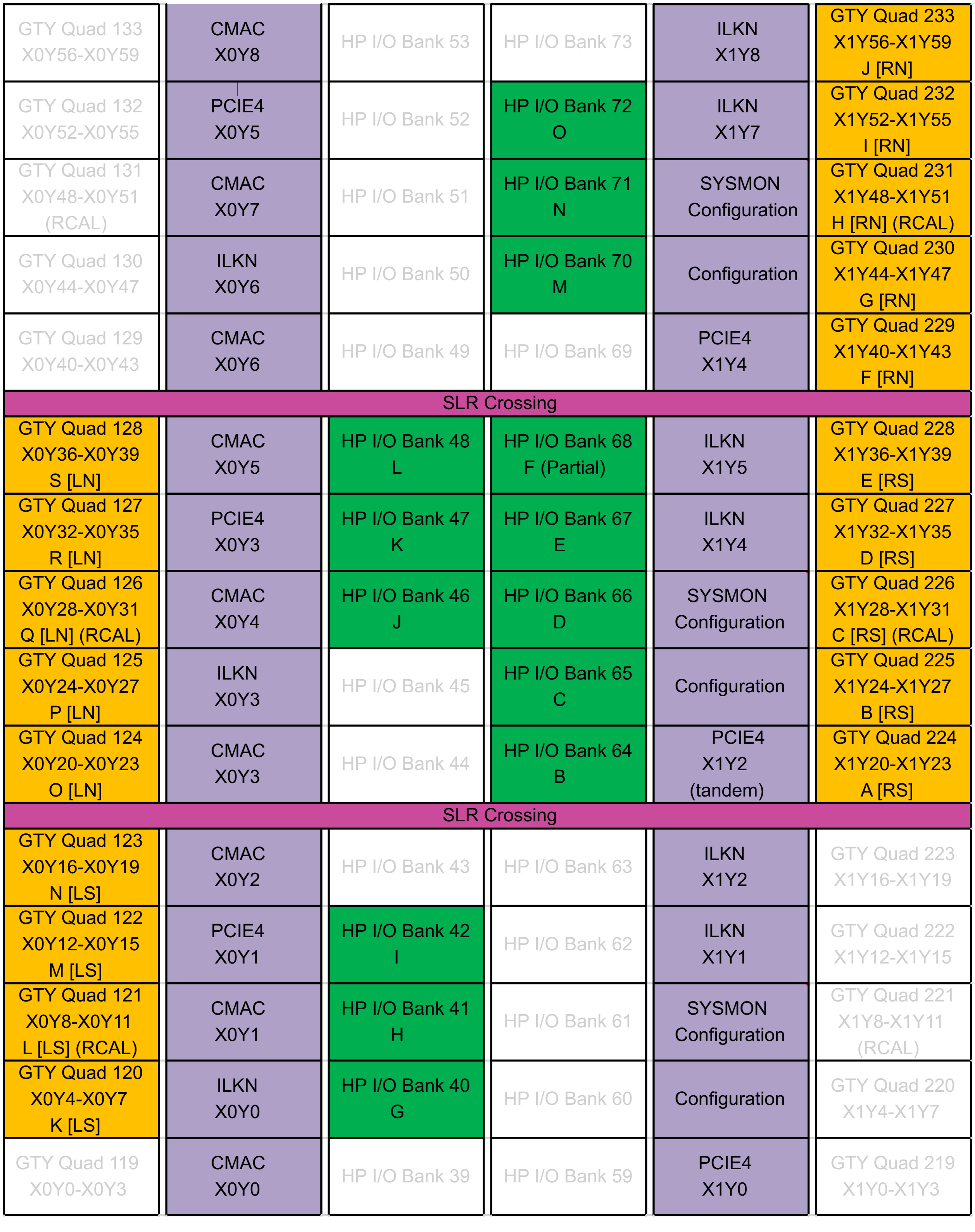

Figure 1-120: **XCVU9P Banks in FLGB2104 Package**

GTY Quad 133 X0Y56-X0Y59 W [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y8	GTY Quad 233 X1Y56-X1Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55 V [LN]	PCIE4 X0Y5	HP I/O Bank 52	HP I/O Bank 72 I	ILKN X1Y7	GTY Quad 232 X1Y52-X1Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 U [LN] (RCAL)	CMAC X0Y7	HP I/O Bank 51	HP I/O Bank 71 H	SYSMON Configuration	GTY Quad 231 X1Y48-X1Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47 T [LN]	ILKN X0Y6	HP I/O Bank 50	HP I/O Bank 70 G	Configuration	GTY Quad 230 X1Y44-X1Y47 G [RN]
GTY Quad 129 X0Y40-X0Y43 S [LN]	CMAC X0Y6	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y4	GTY Quad 229 X1Y40-X1Y43 F [RN]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39 R [LC]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 F	ILKN X1Y5	GTY Quad 228 X1Y36-X1Y39 E [RC]
GTY Quad 127 X0Y32-X0Y35 Q [LC]	PCIE4 X0Y3	HP I/O Bank 47	HP I/O Bank 67 E	ILKN X1Y4	GTY Quad 227 X1Y32-X1Y35 D [RC]
GTY Quad 126 X0Y28-X0Y31 P [LC] (RCAL)	CMAC X0Y4	HP I/O Bank 46	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y28-X1Y31 C [RC] (RCAL)
GTY Quad 125 X0Y24-X0Y27 O [LC]	ILKN X0Y3	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y24-X1Y27 B [RC]
GTY Quad 124 X0Y20-X0Y23 N [LC]	CMAC X0Y3	HP I/O Bank 44	HP I/O Bank 64 B	PCIE4 X1Y2 (tandem)	GTY Quad 224 X1Y20-X1Y23 A [RC]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	ILKN X1Y2	GTY Quad 223 X1Y16-X1Y19
GTY Quad 122 X0Y12-X0Y15 Z [LS]	PCIE4 X0Y1	HP I/O Bank 42	HP I/O Bank 62	ILKN X1Y1	GTY Quad 222 X1Y12-X1Y15 M [RS]
GTY Quad 121 X0Y8-X0Y11 Y [LS] (RCAL)	CMAC X0Y1	HP I/O Bank 41	HP I/O Bank 61	SYSMON Configuration	GTY Quad 221 X1Y8-X1Y11 L [RS] (RCAL)
GTY Quad 120 X0Y4-X0Y7 X [LS]	ILKN X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTY Quad 220 X1Y4-X1Y7 K [RS]
GTY Quad 119 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 39	HP I/O Bank 59	PCIE4 X1Y0	GTY Quad 219 X1Y0-X1Y3

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Figure 1-121: **XCVU9P Banks in FLGC2104 Package**

GTY Quad 133 X0Y56-X0Y59	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y8	GTY Quad 233 X1Y56-X1Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55	PCIE4 X0Y5	HP I/O Bank 52	HP I/O Bank 72 O	ILKN X1Y7	GTY Quad 232 X1Y52-X1Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 S [LN] (RCAL)	CMAC X0Y7	HP I/O Bank 51	HP I/O Bank 71 N	SYSMON Configuration	GTY Quad 231 X1Y48-X1Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47	ILKN X0Y6	HP I/O Bank 50	HP I/O Bank 70 M	Configuration	GTY Quad 230 X1Y44-X1Y47 G [RN]
GTY Quad 129 X0Y40-X0Y43	CMAC X0Y6	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y4	GTY Quad 229 X1Y40-X1Y43 F [RN]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39	CMAC X0Y5	HP I/O Bank 48 L	HP I/O Bank 68	ILKN X1Y5	GTY Quad 228 X1Y36-X1Y39 E [RS]
GTY Quad 127 X0Y32-X0Y35 R [LN]	PCIE4 X0Y3	HP I/O Bank 47 K	HP I/O Bank 67 E	ILKN X1Y4	GTY Quad 227 X1Y32-X1Y35 D [RS]
GTY Quad 126 X0Y28-X0Y31 Q [LN] (RCAL)	CMAC X0Y4	HP I/O Bank 46 J	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y28-X1Y31 C [RS] (RCAL)
GTY Quad 125 X0Y24-X0Y27 P [LN]	ILKN X0Y3	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y24-X1Y27 B [RS]
GTY Quad 124 X0Y20-X0Y23 O [LN]	CMAC X0Y3	HP I/O Bank 44	HP I/O Bank 64 B	PCIE4 X1Y2 (tandem)	GTY Quad 224 X1Y20-X1Y23 A [RS]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19 N [LS]	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63	ILKN X1Y2	GTY Quad 223 X1Y16-X1Y19
GTY Quad 122 X0Y12-X0Y15 M [LS]	PCIE4 X0Y1	HP I/O Bank 42 H	HP I/O Bank 62	ILKN X1Y1	GTY Quad 222 X1Y12-X1Y15
GTY Quad 121 X0Y8-X0Y11 L [LS](RCAL)	CMAC X0Y1	HP I/O Bank 41 G	HP I/O Bank 61	SYSMON Configuration	GTY Quad 221 X1Y8-X1Y11
GTY Quad 120 X0Y4-X0Y7 K [LS]	ILKN X0Y0	HP I/O Bank 40 F	HP I/O Bank 60	Configuration	GTY Quad 220 X1Y4-X1Y7
GTY Quad 119 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 39	HP I/O Bank 59	PCIE4 X1Y0	GTY Quad 219 X1Y0-X1Y3

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Figure 1-122: **XCVU9P Banks in FSGD2104 Package**

GTY Quad 133 X0Y56-X0Y59 Z [LN]	CMAC X0Y8	HP I/O Bank 53	HP I/O Bank 73	ILKN X1Y8	GTY Quad 233 X1Y56-X1Y59 J [RN]
GTY Quad 132 X0Y52-X0Y55 Y [LN]	PCIE4 X0Y5	HP I/O Bank 52	HP I/O Bank 72 K	ILKN X1Y7	GTY Quad 232 X1Y52-X1Y55 I [RN]
GTY Quad 131 X0Y48-X0Y51 X [LN] (RCAL)	CMAC X0Y7	HP I/O Bank 51	HP I/O Bank 71 J	SYSMON Configuration	GTY Quad 231 X1Y48-X1Y51 H [RN] (RCAL)
GTY Quad 130 X0Y44-X0Y47 W [LUC]	ILKN X0Y6	HP I/O Bank 50	HP I/O Bank 70 I	Configuration	GTY Quad 230 X1Y44-X1Y47 G [RUC]
GTY Quad 129 X0Y40-X0Y43 V [LUC]	CMAC X0Y6	HP I/O Bank 49	HP I/O Bank 69	PCIE4 X1Y4	GTY Quad 229 X1Y40-X1Y43 F [RUC]
SLR Crossing					
GTY Quad 128 X0Y36-X0Y39 U [LUC]	CMAC X0Y5	HP I/O Bank 48	HP I/O Bank 68 H (Partial)	ILKN X1Y5	GTY Quad 228 X1Y36-X1Y39 E [RUC]
GTY Quad 127 X0Y32-X0Y35 T [LUC]	PCIE4 X0Y3	HP I/O Bank 47	HP I/O Bank 67 G	ILKN X1Y4	GTY Quad 227 X1Y32-X1Y35 D [RUC]
GTY Quad 126 X0Y28-X0Y31 S [LLC] (RCAL)	CMAC X0Y4	HP I/O Bank 46	HP I/O Bank 66 B (Partial)	SYSMON Configuration	GTY Quad 226 X1Y28-X1Y31 C [RLC] (RCAL)
GTY Quad 125 X0Y24-X0Y27 R [LLC]	ILKN X0Y3	HP I/O Bank 45	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y24-X1Y27 B [RLC]
GTY Quad 124 X0Y20-X0Y23 Q [LLC]	CMAC X0Y3	HP I/O Bank 44	HP I/O Bank 64	PCIE4 X1Y2 (tandem)	GTY Quad 224 X1Y20-X1Y23 A [RLC]
SLR Crossing					
GTY Quad 123 X0Y16-X0Y19 AF [LLC]	CMAC X0Y2	HP I/O Bank 43	HP I/O Bank 63 F	ILKN X1Y2	GTY Quad 223 X1Y16-X1Y19 P [RLC]
GTY Quad 122 X0Y12-X0Y15 AE [LS]	PCIE4 X0Y1	HP I/O Bank 42	HP I/O Bank 62 E	ILKN X1Y1	GTY Quad 222 X1Y12-X1Y15 O [RS]
GTY Quad 121 X0Y8-X0Y11 AD [LS] (RCAL)	CMAC X0Y1	HP I/O Bank 41	HP I/O Bank 61 D	SYSMON Configuration	GTY Quad 221 X1Y8-X1Y11 N [RS] (RCAL)
GTY Quad 120 X0Y4-X0Y7 AC [LS]	ILKN X0Y0	HP I/O Bank 40	HP I/O Bank 60	Configuration	GTY Quad 220 X1Y4-X1Y7 M [RS]
GTY Quad 119 X0Y0-X0Y3 AB [LS]	CMAC X0Y0	HP I/O Bank 39	HP I/O Bank 59	PCIE4 X1Y0	GTY Quad 219 X1Y0-X1Y3 L [RS]

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Figure 1-123: **XCVU9P Banks in FLGA2577 Package**

XCVU11P and XQVU11P Bank Diagrams

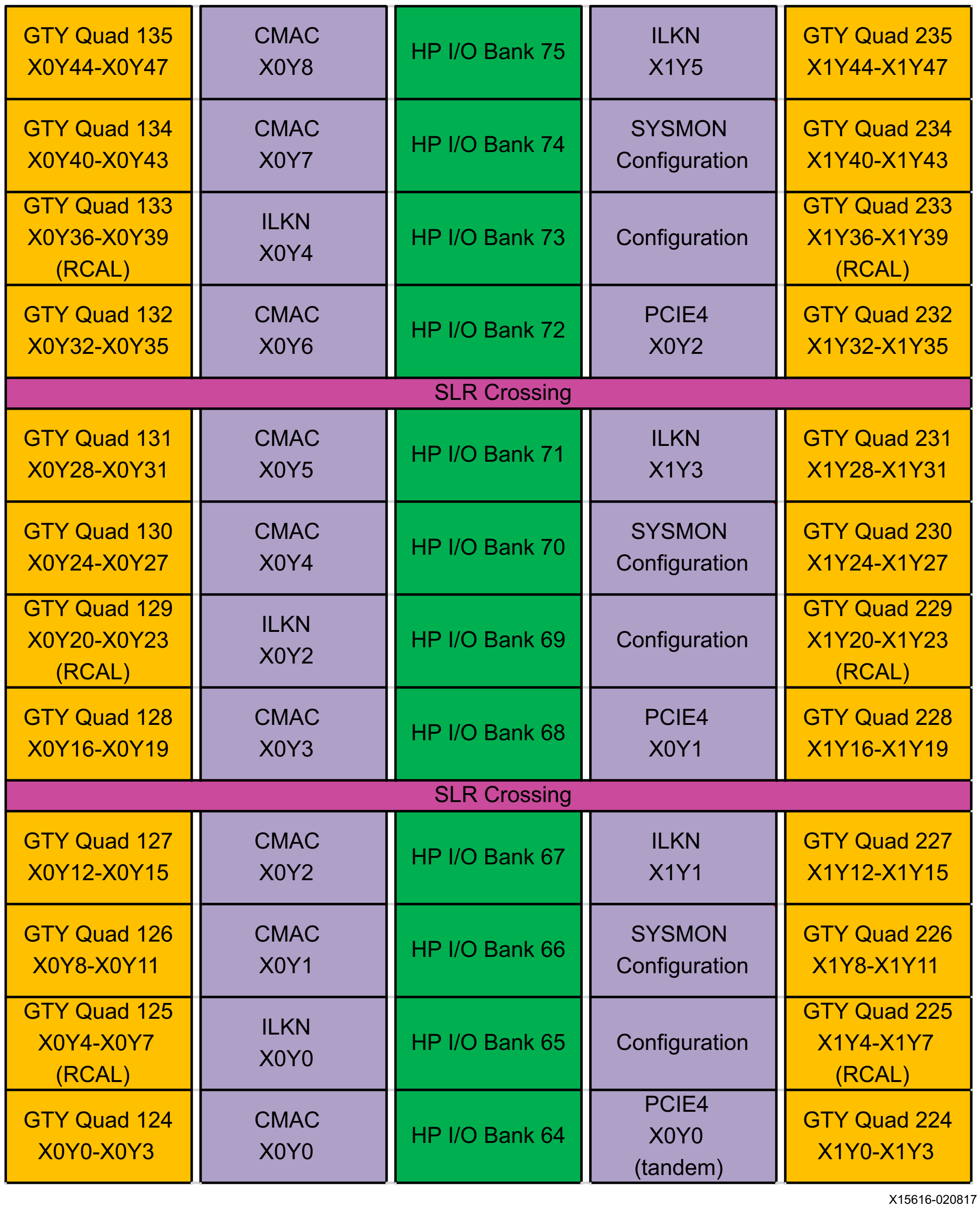

Figure 1-124: **XCVU11P and XQVU11P Banks**

GTY Quad 135 X0Y44-X0Y47	CMAC X0Y8	HP I/O Bank 75 P	ILKN X1Y5	GTY Quad 235 X1Y44-X1Y47
GTY Quad 134 X0Y40-X0Y43	CMAC X0Y7	HP I/O Bank 74 O	SYSMON Configuration	GTY Quad 234 X1Y40-X1Y43
GTY Quad 133 X0Y36-X0Y39 (RCAL)	ILKN X0Y4	HP I/O Bank 73 N	Configuration	GTY Quad 233 X1Y36-X1Y39 J [RN] (RCAL)
GTY Quad 132 X0Y32-X0Y35	CMAC X0Y6	HP I/O Bank 72 M	PCIE4 X0Y2	GTY Quad 232 X1Y32-X1Y35 I [RN]
SLR Crossing				
GTY Quad 131 X0Y28-X0Y31 P [LN]	CMAC X0Y5	HP I/O Bank 71 L	ILKN X1Y3	GTY Quad 231 X1Y28-X1Y31 H [RN]
GTY Quad 130 X0Y24-X0Y27 Q [LN]	CMAC X0Y4	HP I/O Bank 70 K	SYSMON Configuration	GTY Quad 230 X1Y24-X1Y27 G [RN]
GTY Quad 129 X0Y20-X0Y23 N [LN] (RCAL)	ILKN X0Y2	HP I/O Bank 69 J	Configuration	GTY Quad 229 X1Y20-X1Y23 F [RN] (RCAL)
GTY Quad 128 X0Y16-X0Y19	CMAC X0Y3	HP I/O Bank 68 F	PCIE4 X0Y1	GTY Quad 228 X1Y16-X1Y19 E [RS]
SLR Crossing				
GTY Quad 127 X0Y12-X0Y15 M [LS]	CMAC X0Y2	HP I/O Bank 67 E	ILKN X1Y1	GTY Quad 227 X1Y12-X1Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 L [LS]	CMAC X0Y1	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 K [LS] (RCAL)	ILKN X0Y0	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y4-X1Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 64 G	PCIE4 X0Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3 A [RS]

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Figure 1-125: **XCVU11P Banks in FLGF1924 Package**

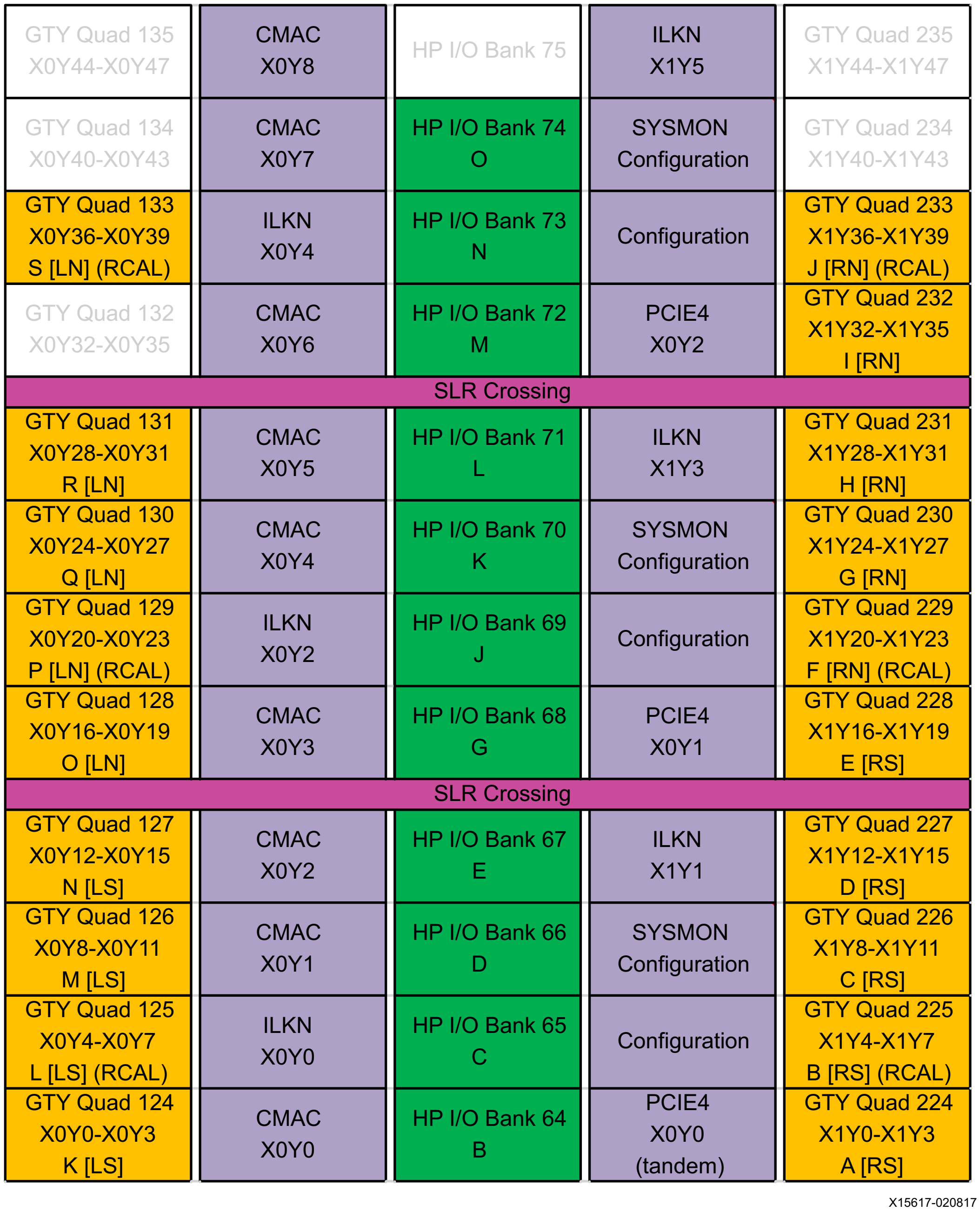

Figure 1-126: **XCVU11P Banks in FLGB2104 Package**

GTY Quad 135 X0Y44-X0Y47 W [LN]	CMAC X0Y8	HP I/O Bank 75	ILKN X1Y5	GTY Quad 235 X1Y44-X1Y47 J [RN]
GTY Quad 134 X0Y40-X0Y43 V [LN]	CMAC X0Y7	HP I/O Bank 74	SYSMON Configuration	GTY Quad 234 X1Y40-X1Y43 I [RN]
GTY Quad 133 X0Y36-X0Y39 U [LN] (RCAL)	ILKN X0Y4	HP I/O Bank 73	Configuration	GTY Quad 233 X1Y36-X1Y39 H [RN] (RCAL)
GTY Quad 132 X0Y32-X0Y35 T [LN]	CMAC X0Y6	HP I/O Bank 72	PCIE4 X0Y2	GTY Quad 232 X1Y32-X1Y35 G [RN]
SLR Crossing				
GTY Quad 131 X0Y28-X0Y31 S [LN]	CMAC X0Y5	HP I/O Bank 71 I	ILKN X1Y3	GTY Quad 231 X1Y28-X1Y31 F [RN]
GTY Quad 130 X0Y24-X0Y27 R [LC]	CMAC X0Y4	HP I/O Bank 70 H	SYSMON Configuration	GTY Quad 230 X1Y24-X1Y27 E [RC]
GTY Quad 129 X0Y20-X0Y23 Q [LC] (RCAL)	ILKN X0Y2	HP I/O Bank 69 G	Configuration	GTY Quad 229 X1Y20-X1Y23 D [RC] (RCAL)
GTY Quad 128 X0Y16-X0Y19 P [LC]	CMAC X0Y3	HP I/O Bank 68 F	PCIE4 X0Y1	GTY Quad 228 X1Y16-X1Y19 C [RC]
SLR Crossing				
GTY Quad 127 X0Y12-X0Y15 O [LC]	CMAC X0Y2	HP I/O Bank 67 E	ILKN X1Y1	GTY Quad 227 X1Y12-X1Y15 B [RC]
GTY Quad 126 X0Y8-X0Y11 N [LC]	CMAC X0Y1	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11 A [RC]
GTY Quad 125 X0Y4-X0Y7 Z [LS] (RCAL)	ILKN X0Y0	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y4-X1Y7 M [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3 Y [LS]	CMAC X0Y0	HP I/O Bank 64 B	PCIE4 X0Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3 L [RS]

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Figure 1-127: **XCVU11P Banks in FLGC2104 Package and XQVU11P Banks in FLRC2104 Package**

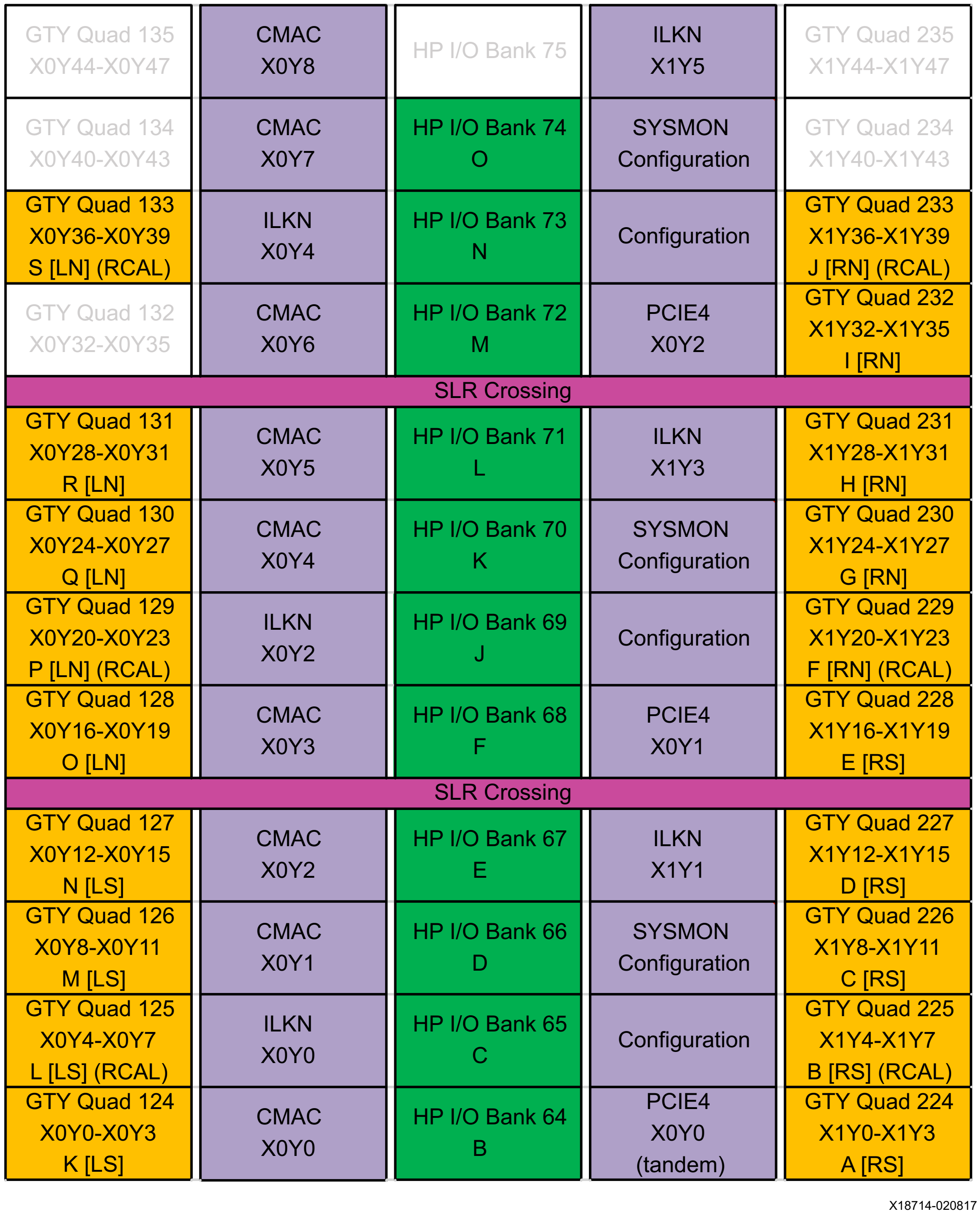

Figure 1-128: **XCVU11P Banks in FSGD2104 Package**

Figure 1-129: **XCVU11P Banks in FLGA2577 Package**

XCVU13P Bank Diagrams

GTY Quad 135 X0Y60-X0Y63	CMAC X0Y11	HP I/O Bank 75	ILKN X1Y7	GTY Quad 235 X1Y60-X1Y63
GTY Quad 134 X0Y56-X0Y59	CMAC X0Y10	HP I/O Bank 74	SYSMON Configuration	GTY Quad 234 X1Y56-X1Y59
GTY Quad 133 X0Y52-X0Y55 (RCAL)	ILKN X0Y6	HP I/O Bank 73	Configuration	GTY Quad 233 X1Y52-X1Y55 (RCAL)
GTY Quad 132 X0Y48-X0Y51	CMAC X0Y9	HP I/O Bank 72	PCIE4 X0Y3	GTY Quad 232 X1Y48-X1Y51
SLR Crossing				
GTY Quad 131 X0Y44-X0Y47	CMAC X0Y8	HP I/O Bank 71	ILKN X1Y5	GTY Quad 231 X1Y44-X1Y47
GTY Quad 130 X0Y40-X0Y43	CMAC X0Y7	HP I/O Bank 70	SYSMON Configuration	GTY Quad 230 X1Y40-X1Y43
GTY Quad 129 X0Y36-X0Y39 (RCAL)	ILKN X0Y4	HP I/O Bank 69	Configuration	GTY Quad 229 X1Y36-X1Y39 (RCAL)
GTY Quad 128 X0Y32-X0Y35	CMAC X0Y6	HP I/O Bank 68	PCIE4 X0Y2	GTY Quad 228 X1Y32-X1Y35
SLR Crossing				
GTY Quad 127 X0Y28-X0Y31	CMAC X0Y5	HP I/O Bank 67	ILKN X1Y3	GTY Quad 227 X1Y28-X1Y31
GTY Quad 126 X0Y24-X0Y27	CMAC X0Y4	HP I/O Bank 66	SYSMON Configuration	GTY Quad 226 X1Y24-X1Y27
GTY Quad 125 X0Y20-X0Y23 (RCAL)	ILKN X0Y2	HP I/O Bank 65	Configuration	GTY Quad 225 X1Y20-X1Y23 (RCAL)
GTY Quad 124 X0Y16-X0Y19	CMAC X0Y3	HP I/O Bank 64	PCIE4 X0Y1 (tandem)	GTY Quad 224 X1Y16-X1Y19
SLR Crossing				
GTY Quad 123 X0Y12-X0Y15	CMAC X0Y2	HP I/O Bank 63	ILKN X1Y1	GTY Quad 223 X1Y12-X1Y15
GTY Quad 122 X0Y8-X0Y11	CMAC X0Y1	HP I/O Bank 62	SYSMON Configuration	GTY Quad 222 X1Y8-X1Y11
GTY Quad 121 X0Y4-X0Y7 (RCAL)	ILKN X0Y0	HP I/O Bank 61	Configuration	GTY Quad 221 X1Y4-X1Y7 (RCAL)
GTY Quad 120 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 60	PCIE4 X0Y0	GTY Quad 220 X1Y0-X1Y3

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Figure 1-130: **XCVU13P Banks**

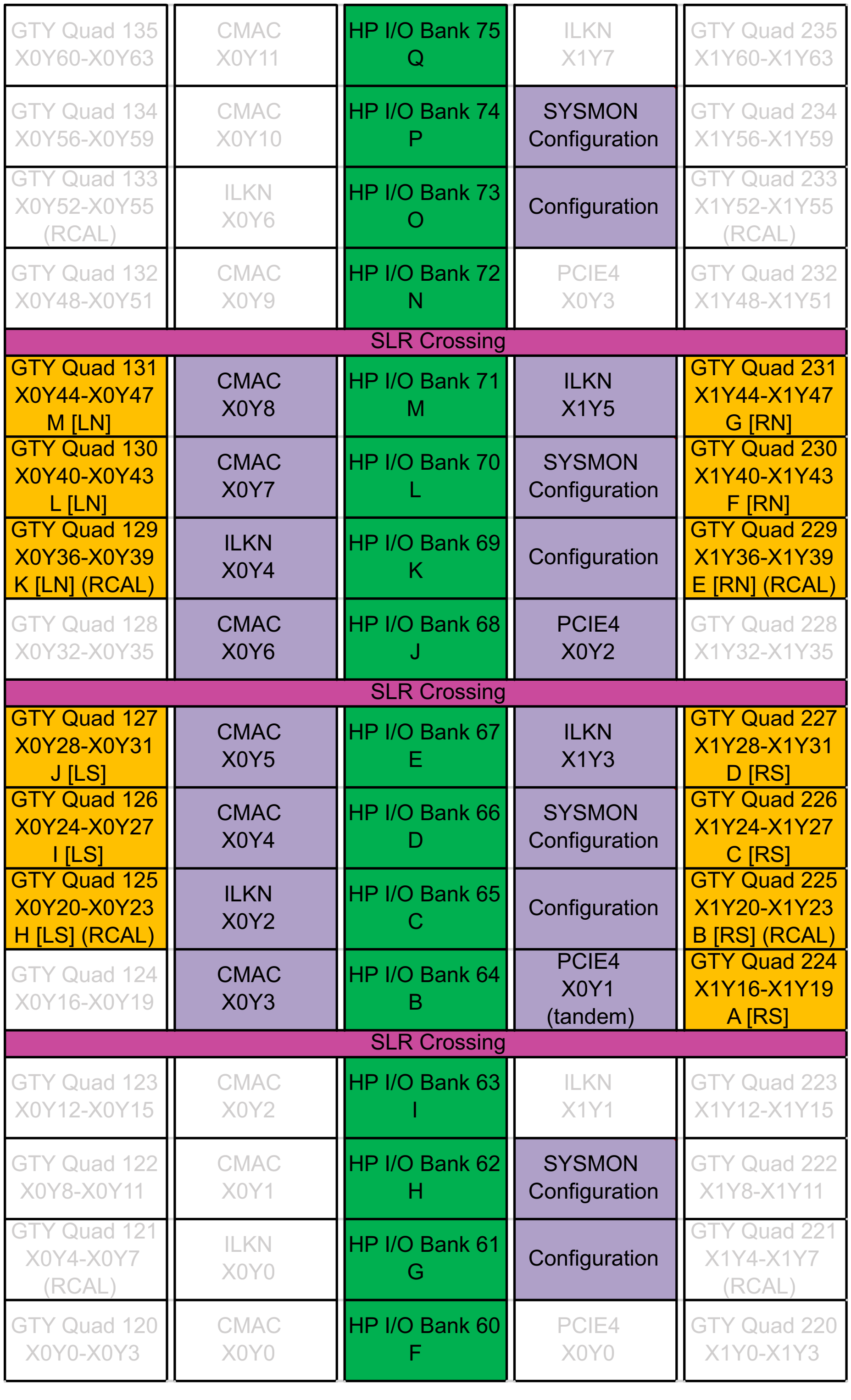

Figure 1-131: **XCVU13P Banks in FHGA2104 Package**

GTY Quad 135 X0Y60-X0Y63	CMAC X0Y11	HP I/O Bank 75	ILKN X1Y7	GTY Quad 235 X1Y60-X1Y63
GTY Quad 134 X0Y56-X0Y59	CMAC X0Y10	HP I/O Bank 74 O	SYSMON Configuration	GTY Quad 234 X1Y56-X1Y59
GTY Quad 133 X0Y52-X0Y55 S [LN] (RCAL)	ILKN X0Y6	HP I/O Bank 73 N	Configuration	GTY Quad 233 X1Y52-X1Y55 J [RN] (RCAL)
GTY Quad 132 X0Y48-X0Y51	CMAC X0Y9	HP I/O Bank 72 M	PCIE4 X0Y3	GTY Quad 232 X1Y48-X1Y51 I [RN]
SLR Crossing				
GTY Quad 131 X0Y44-X0Y47 R [LN]	CMAC X0Y8	HP I/O Bank 71 L	ILKN X1Y5	GTY Quad 231 X1Y44-X1Y47 H [RN]
GTY Quad 130 X0Y40-X0Y43 Q [LN]	CMAC X0Y7	HP I/O Bank 70 K	SYSMON Configuration	GTY Quad 230 X1Y40-X1Y43 G [RN]
GTY Quad 129 X0Y36-X0Y39 P [LN] (RCAL)	ILKN X0Y4	HP I/O Bank 69 J	Configuration	GTY Quad 229 X1Y36-X1Y39 F [RN] (RCAL)
GTY Quad 128 X0Y32-X0Y35 O [LN]	CMAC X0Y6	HP I/O Bank 68 F (Partial)	PCIE4 X0Y2	GTY Quad 228 X1Y32-X1Y35 E [RS]
SLR Crossing				
GTY Quad 127 X0Y28-X0Y31 N [LS]	CMAC X0Y5	HP I/O Bank 67 E	ILKN X1Y3	GTY Quad 227 X1Y28-X1Y31 D [RS]
GTY Quad 126 X0Y24-X0Y27 M [LS]	CMAC X0Y4	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y24-X1Y27 C [RS]
GTY Quad 125 X0Y20-X0Y23 L [LS] (RCAL)	ILKN X0Y2	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y20-X1Y23 B [RS] (RCAL)
GTY Quad 124 X0Y16-X0Y19 K [LS]	CMAC X0Y3	HP I/O Bank 64 B	PCIE4 X0Y1 (tandem)	GTY Quad 224 X1Y16-X1Y19 A [RS]
SLR Crossing				
GTY Quad 123 X0Y12-X0Y15	CMAC X0Y2	HP I/O Bank 63 I	ILKN X1Y1	GTY Quad 223 X1Y12-X1Y15
GTY Quad 122 X0Y8-X0Y11	CMAC X0Y1	HP I/O Bank 62 H	SYSMON Configuration	GTY Quad 222 X1Y8-X1Y11
GTY Quad 121 X0Y4-X0Y7 (RCAL)	ILKN X0Y0	HP I/O Bank 61 G	Configuration	GTY Quad 221 X1Y4-X1Y7 (RCAL)
GTY Quad 120 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 60 F	PCIE4 X0Y0	GTY Quad 220 X1Y0-X1Y3

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Figure 1-132: **XCVU13P Banks in FHGB2104 Package**

GTY Quad 135 X0Y60-X0Y63	CMAC X0Y11	HP I/O Bank 75	ILKN X1Y7	GTY Quad 235 X1Y60-X1Y63
GTY Quad 134 X0Y56-X0Y59	CMAC X0Y10	HP I/O Bank 74	SYSMON Configuration	GTY Quad 234 X1Y56-X1Y59
GTY Quad 133 X0Y52-X0Y55 W [LN] (RCAL)	ILKN X0Y6	HP I/O Bank 73	Configuration	GTY Quad 233 X1Y52-X1Y55 J [RN] (RCAL)
GTY Quad 132 X0Y48-X0Y51 V [LN]	CMAC X0Y9	HP I/O Bank 72	PCIE4 X0Y3	GTY Quad 232 X1Y48-X1Y51 I [RN]
SLR Crossing				
GTY Quad 131 X0Y44-X0Y47 U [LN]	CMAC X0Y8	HP I/O Bank 71 I	ILKN X1Y5	GTY Quad 231 X1Y44-X1Y47 H [RN]
GTY Quad 130 X0Y40-X0Y43 T [LN]	CMAC X0Y7	HP I/O Bank 70 H	SYSMON Configuration	GTY Quad 230 X1Y40-X1Y43 G [RN]
GTY Quad 129 X0Y36-X0Y39 S [LN] (RCAL)	ILKN X0Y4	HP I/O Bank 69 G	Configuration	GTY Quad 229 X1Y36-X1Y39 F [RN] (RCAL)
GTY Quad 128 X0Y32-X0Y35 R [LC]	CMAC X0Y6	HP I/O Bank 68 F	PCIE4 X0Y2	GTY Quad 228 X1Y32-X1Y35 E [RC]
SLR Crossing				
GTY Quad 127 X0Y28-X0Y31 Q [LC]	CMAC X0Y5	HP I/O Bank 67 E	ILKN X1Y3	GTY Quad 227 X1Y28-X1Y31 D [RC]
GTY Quad 126 X0Y24-X0Y27 P [LC]	CMAC X0Y4	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y24-X1Y27 C [RC]
GTY Quad 125 X0Y20-X0Y23 O [LC] (RCAL)	ILKN X0Y2	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y20-X1Y23 B [RC] (RCAL)
GTY Quad 124 X0Y16-X0Y19 N [LC]	CMAC X0Y3	HP I/O Bank 64 B	PCIE4 X0Y1 (tandem)	GTY Quad 224 X1Y16-X1Y19 A [RC]
SLR Crossing				
GTY Quad 123 X0Y12-X0Y15 Z [LS]	CMAC X0Y2	HP I/O Bank 63	ILKN X1Y1	GTY Quad 223 X1Y12-X1Y15 M [RS]
GTY Quad 122 X0Y8-X0Y11 Y [LS]	CMAC X0Y1	HP I/O Bank 62	SYSMON Configuration	GTY Quad 222 X1Y8-X1Y11 L [RS]
GTY Quad 121 X0Y4-X0Y7 X [LS] (RCAL)	ILKN X0Y0	HP I/O Bank 61	Configuration	GTY Quad 221 X1Y4-X1Y7 K [RS] (RCAL)
GTY Quad 120 X0Y0-X0Y3	CMAC X0Y0	HP I/O Bank 60	PCIE4 X0Y0	GTY Quad 220 X1Y0-X1Y3

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Figure 1-133: **XCVU13P Banks in FHGC2104 Package**

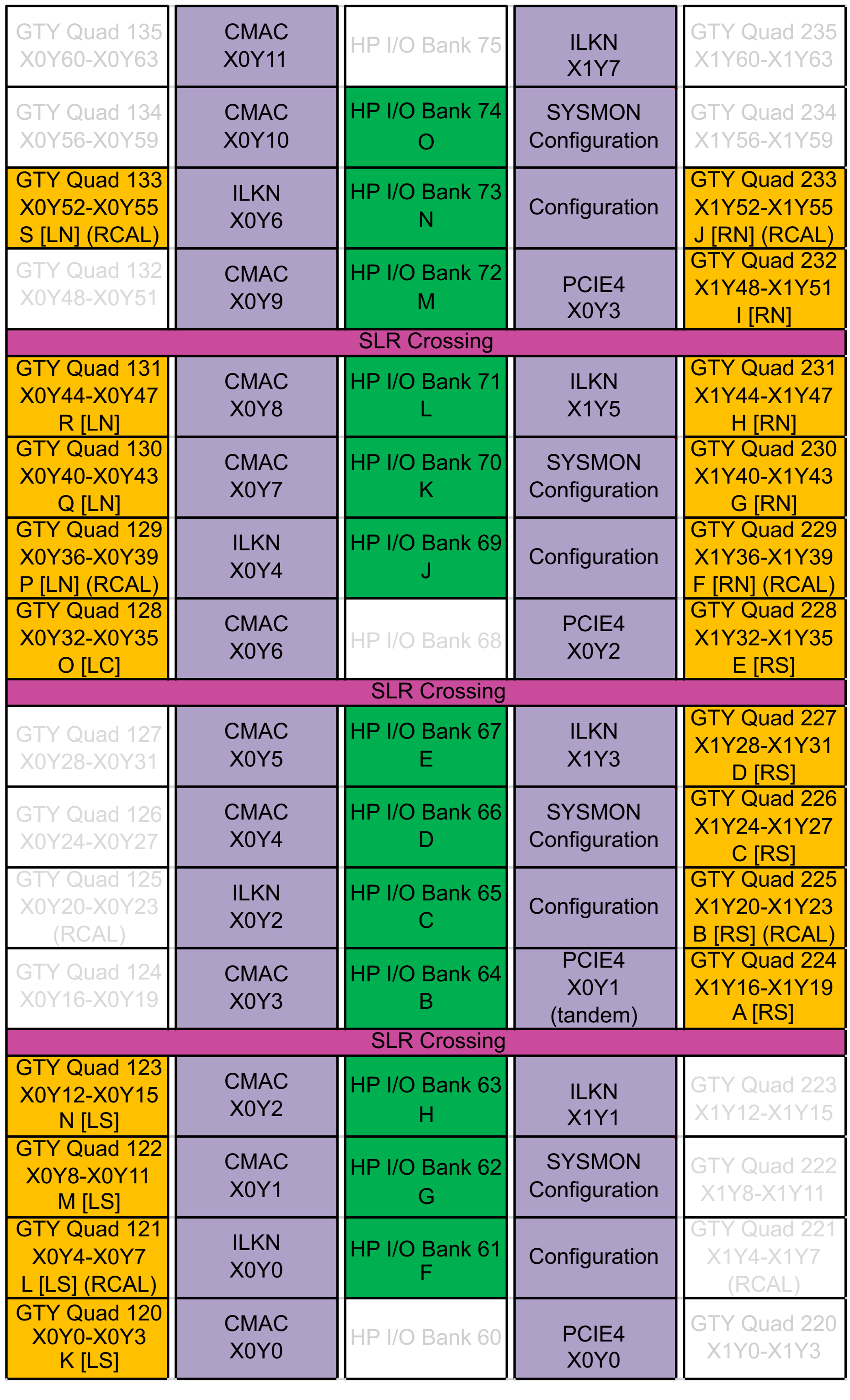

Figure 1-134: **XCVU13P Banks in FIGD2104 Package**

GTY Quad 135 X0Y60-X0Y63 AA [LN]	CMAC X0Y11	HP I/O Bank 75 K	ILKN X1Y7	GTY Quad 235 X1Y60-X1Y63 K [RN]
GTY Quad 134 X0Y56-X0Y59 Z [LN]	CMAC X0Y10	HP I/O Bank 74 J	SYSMON Configuration	GTY Quad 234 X1Y56-X1Y59 J [RN]
GTY Quad 133 X0Y52-X0Y55 Y [LN] (RCAL)	ILKN X0Y6	HP I/O Bank 73 I	Configuration	GTY Quad 233 X1Y52-X1Y55 I [RN] (RCAL)
GTY Quad 132 X0Y48-X0Y51 X [LN]	CMAC X0Y9	HP I/O Bank 72	PCIE4 X0Y3	GTY Quad 232 X1Y48-X1Y51 H [RN]
SLR Crossing				
GTY Quad 131 X0Y44-X0Y47 W [LUC]	CMAC X0Y8	HP I/O Bank 71 H (Partial)	ILKN X1Y5	GTY Quad 231 X1Y44-X1Y47 G [RUC]
GTY Quad 130 X0Y40-X0Y43 V [LUC]	CMAC X0Y7	HP I/O Bank 70 G	SYSMON Configuration	GTY Quad 230 X1Y40-X1Y43 F [RUC]
GTY Quad 129 X0Y36-X0Y39 U [LUC] (RCAL)	ILKN X0Y4	HP I/O Bank 69	Configuration	GTY Quad 229 X1Y36-X1Y39 E [RUC] (RCAL)
GTY Quad 128 X0Y32-X0Y35 T [LUC]	CMAC X0Y6	HP I/O Bank 68	PCIE4 X0Y2	GTY Quad 228 X1Y32-X1Y35 D [RUC]
SLR Crossing				
GTY Quad 127 X0Y28-X0Y31 S [LLC]	CMAC X0Y5	HP I/O Bank 67	ILKN X1Y3	GTY Quad 227 X1Y28-X1Y31 C [RLC]
GTY Quad 126 X0Y24-X0Y27 R [LLC]	CMAC X0Y4	HP I/O Bank 66 B (Partial)	SYSMON Configuration	GTY Quad 226 X1Y24-X1Y27 B [RLC]
GTY Quad 125 X0Y20-X0Y23 Q [LLC] (RCAL)	ILKN X0Y2	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y20-X1Y23 A [RLC] (RCAL)
GTY Quad 124 X0Y16-X0Y19 AF [LLC]	CMAC X0Y3	HP I/O Bank 64	PCIE4 X0Y1 (tandem)	GTY Quad 224 X1Y16-X1Y19 P [RLC]
SLR Crossing				
GTY Quad 123 X0Y12-X0Y15 AE [LS]	CMAC X0Y2	HP I/O Bank 63 F	ILKN X1Y1	GTY Quad 223 X1Y12-X1Y15 O [RS]
GTY Quad 122 X0Y8-X0Y11 AD [LS]	CMAC X0Y1	HP I/O Bank 62 E	SYSMON Configuration	GTY Quad 222 X1Y8-X1Y11 N [RS]
GTY Quad 121 X0Y4-X0Y7 AC [LS] (RCAL)	ILKN X0Y0	HP I/O Bank 61 D	Configuration	GTY Quad 221 X1Y4-X1Y7 M [RS] (RCAL)
GTY Quad 120 X0Y0-X0Y3 AB [LS]	CMAC X0Y0	HP I/O Bank 60	PCIE4 X0Y0	GTY Quad 220 X1Y0-X1Y3 L [RS]

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Figure 1-135: **XCVU13P Banks in FLGA2577 and FSGA2577 Packages**

XCVU19P Bank Diagrams

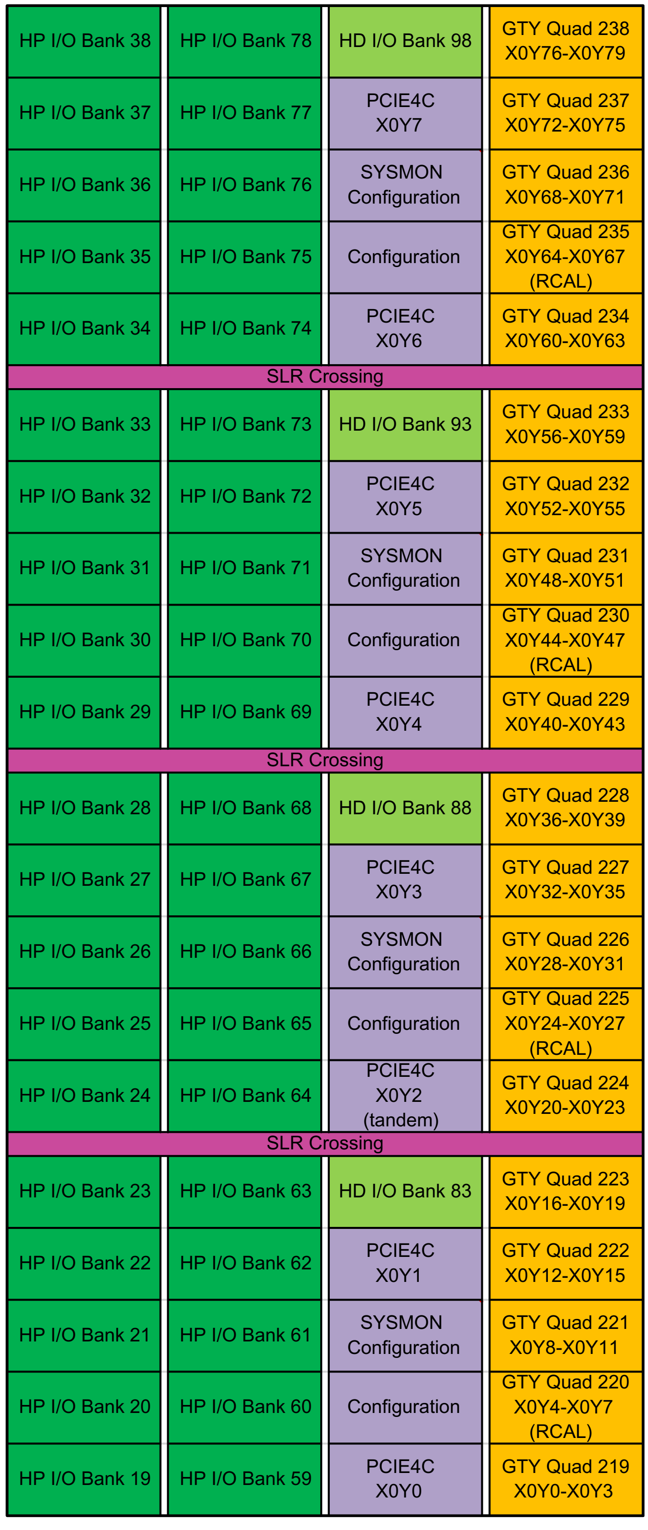

Figure 1-136: **XCVU19P Banks**

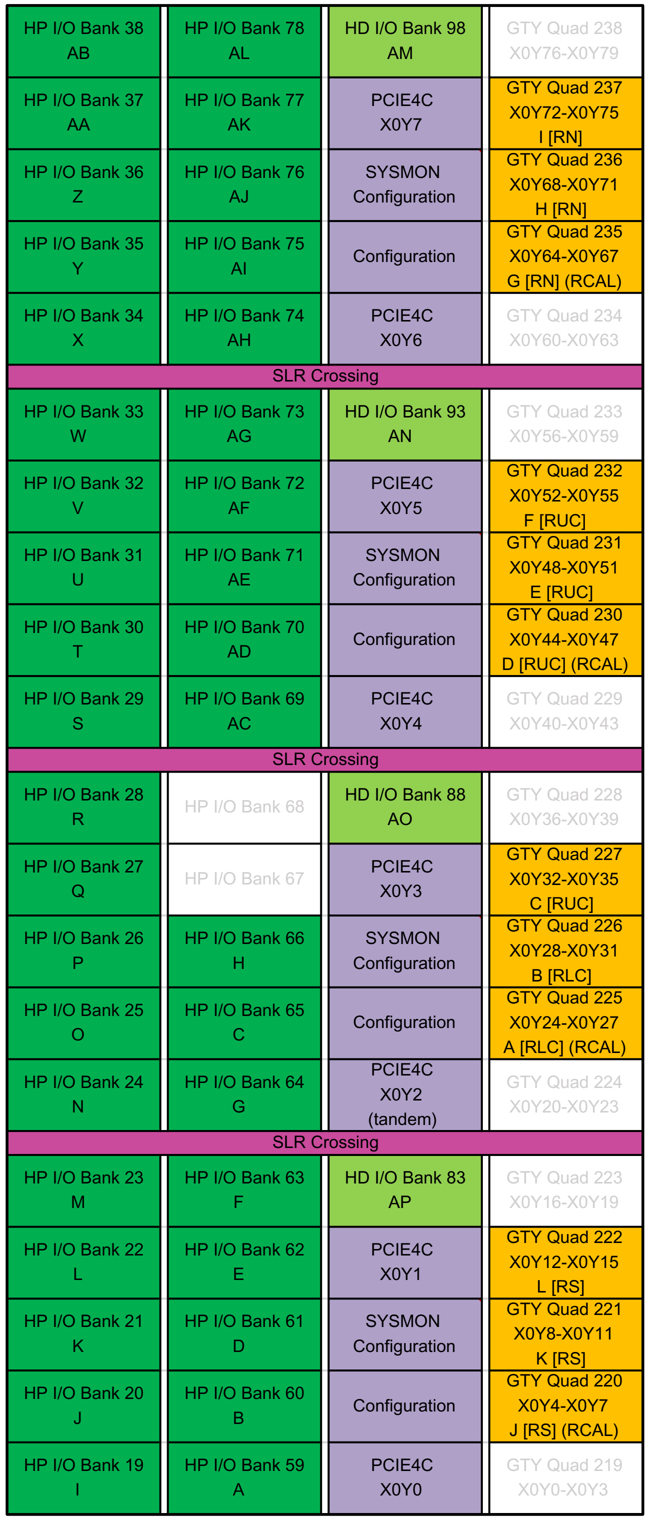

Figure 1-137: **XCVU19P Banks in FSVA3824 Package**

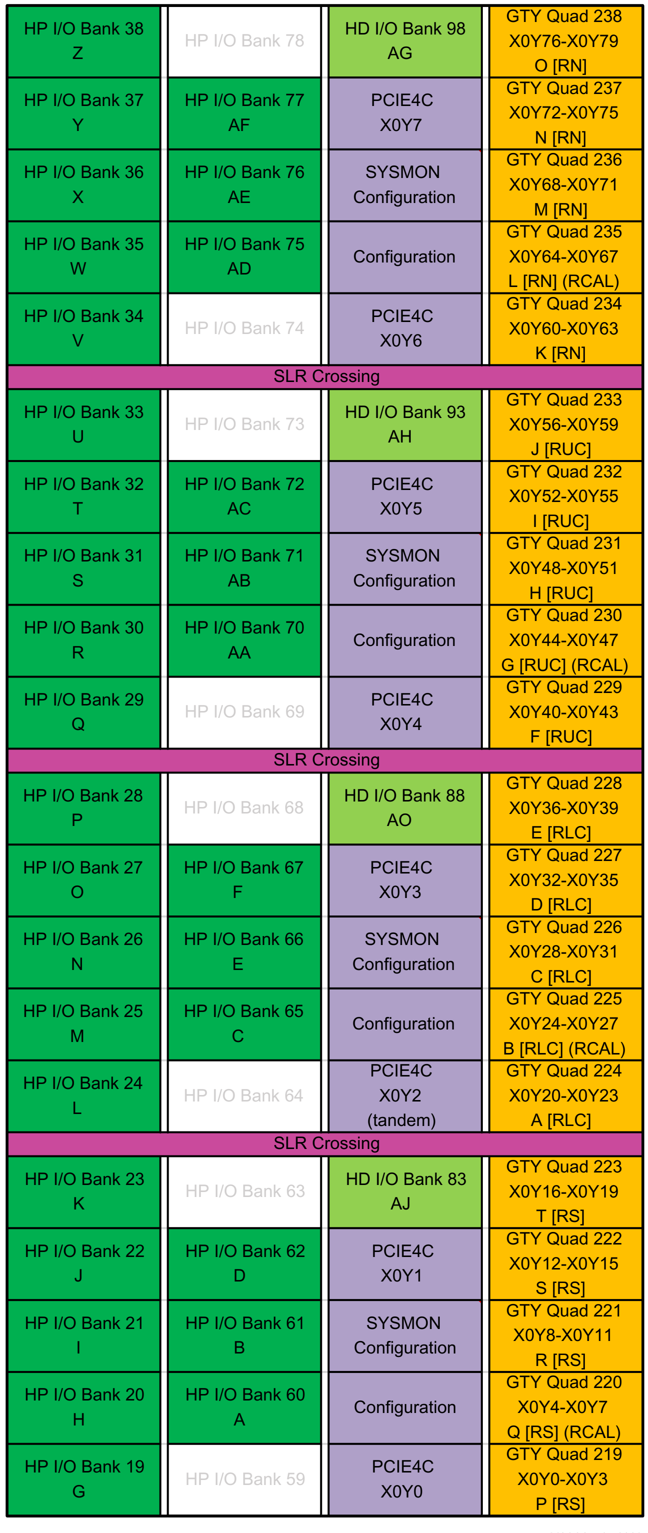

Figure 1-138: **XCVU19P Banks in FSVB3824 Package**

XCVU23P Bank Diagrams

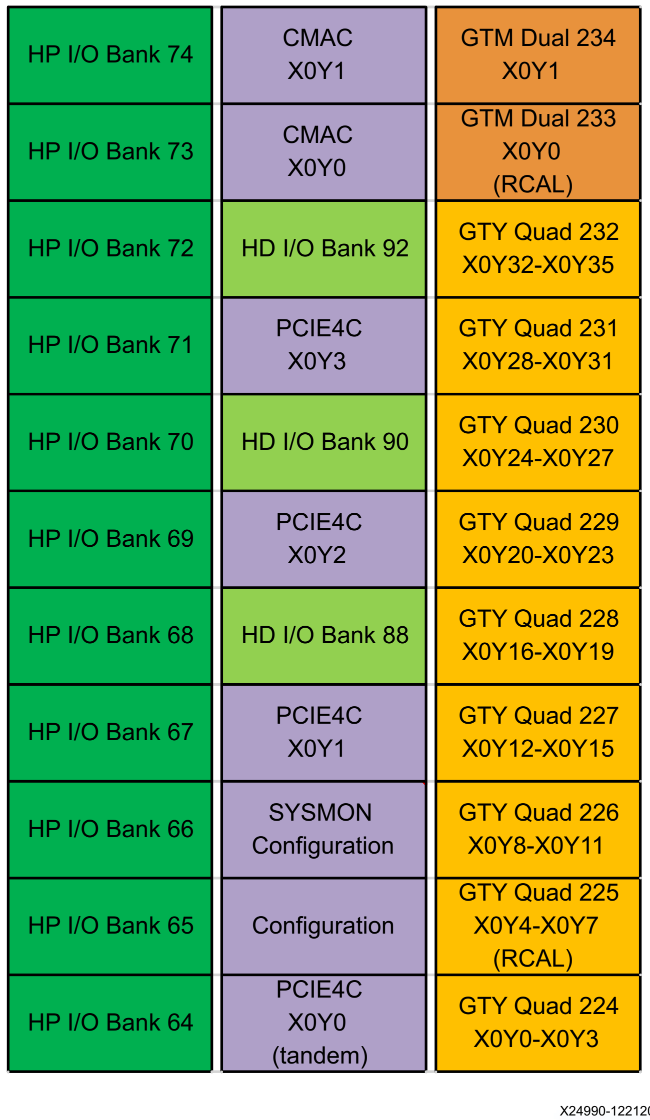

Figure 1-139: **XCVU23P Banks**

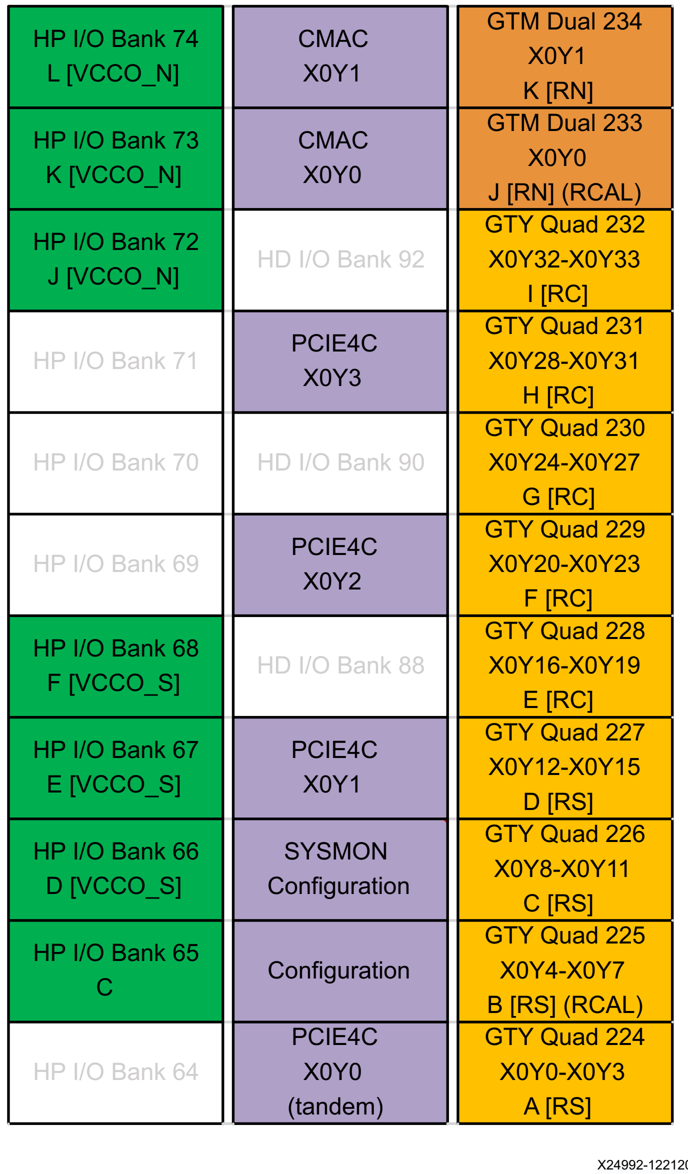

Figure 1-140: **XCVU23P Banks in VSVA1365 Package**

Note: Banks with a common V_{CCO} (such as VCCO_S or VCCO_N) should be tied to a common on-board power supply voltage.

HP I/O Bank 74 V	CMAC X0Y1	GTM Dual 234 X0Y1 K [RN]
HP I/O Bank 73 U	CMAC X0Y0	GTM Dual 233 X0Y0 J [RN] (RCAL)
HP I/O Bank 72 T	HD I/O Bank 92 P	GTY Quad 232 X0Y32-X0Y33 I [RC]
HP I/O Bank 71 S	PCIE4C X0Y3	GTY Quad 231 X0Y28-X0Y31 H [RC]
HP I/O Bank 70 R	HD I/O Bank 90 O	GTY Quad 230 X0Y24-X0Y27 G [RC]
HP I/O Bank 69 G	PCIE4C X0Y2	GTY Quad 229 X0Y20-X0Y23 F [RC]
HP I/O Bank 68 F	HD I/O Bank 88 N	GTY Quad 228 X0Y16-X0Y19 E [RC]
HP I/O Bank 67 E	PCIE4C X0Y1	GTY Quad 227 X0Y12-X0Y15 D [RS]
HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X0Y8-X0Y11 C [RS]
HP I/O Bank 65 C	Configuration	GTY Quad 225 X0Y4-X0Y7 B [RS] (RCAL)
HP I/O Bank 64 B	PCIE4C X0Y0 (tandem)	GTY Quad 224 X0Y0-X0Y3 A [RS]

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Figure 1-141: **XCVU23P Banks in FSVJ1760 Package**

XCVU27P Bank Diagrams

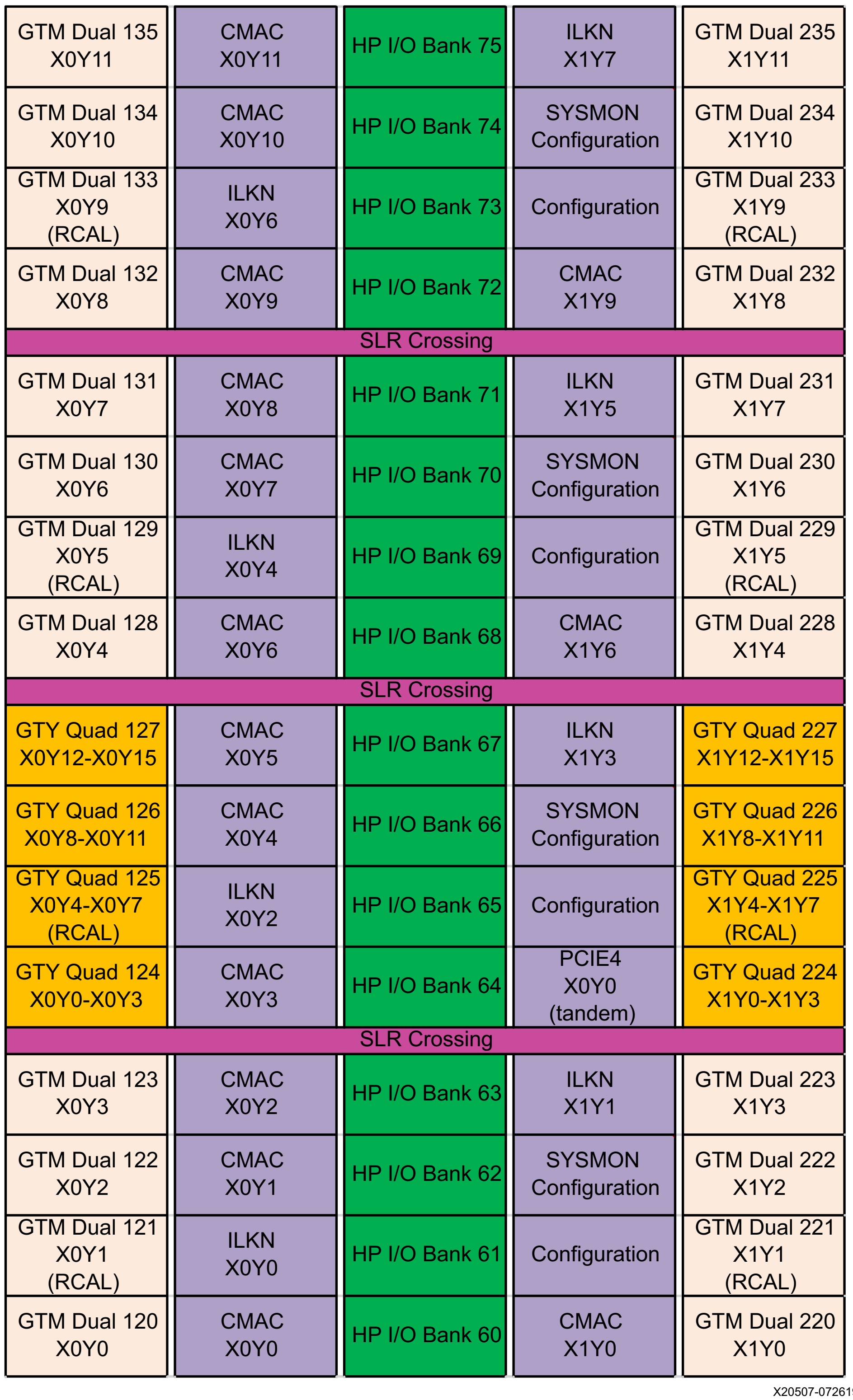

Figure 1-142: **XCVU27P Banks**

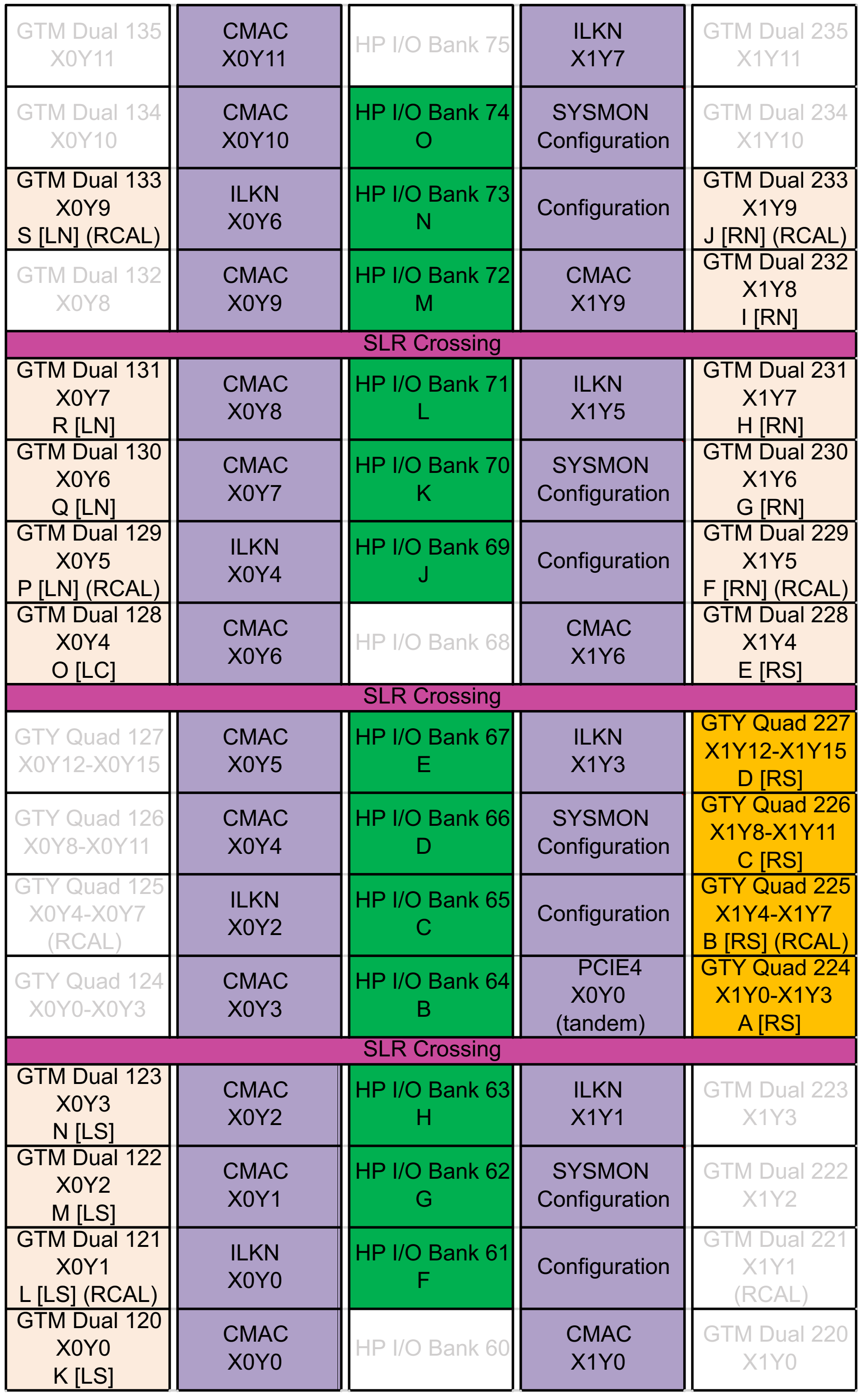

Figure 1-143: **XCVU27P Banks in FIGD2104 Package**

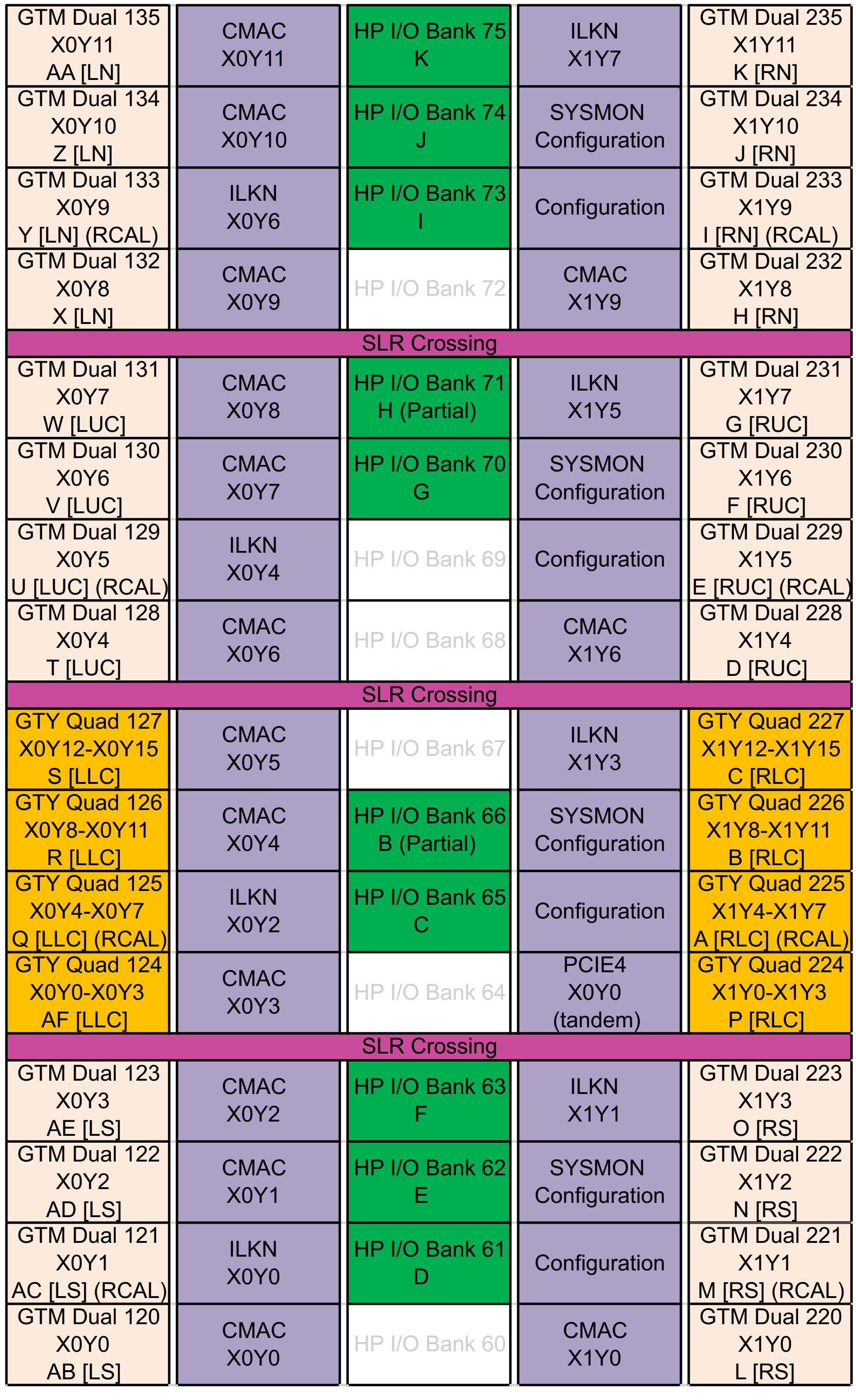

Figure 1-144: **XCVU27P Banks in FSGA2577 Package**

XCVU29P Bank Diagrams

GTM Dual 135 X0Y11	CMAC X0Y11	HP I/O Bank 75	ILKN X1Y7	GTM Dual 235 X1Y11
GTM Dual 134 X0Y10	CMAC X0Y10	HP I/O Bank 74	SYSMON Configuration	GTM Dual 234 X1Y10
GTM Dual 133 X0Y9 (RCAL)	ILKN X0Y6	HP I/O Bank 73	Configuration	GTM Dual 233 X1Y9 (RCAL)
GTM Dual 132 X0Y8	CMAC X0Y9	HP I/O Bank 72	CMAC X1Y9	GTM Dual 232 X1Y8
SLR Crossing				
GTM Dual 131 X0Y7	CMAC X0Y8	HP I/O Bank 71	ILKN X1Y5	GTM Dual 231 X1Y7
GTM Dual 130 X0Y6	CMAC X0Y7	HP I/O Bank 70	SYSMON Configuration	GTM Dual 230 X1Y6
GTM Dual 129 X0Y5 (RCAL)	ILKN X0Y4	HP I/O Bank 69	Configuration	GTM Dual 229 X1Y5 (RCAL)
GTM Dual 128 X0Y4	CMAC X0Y6	HP I/O Bank 68	CMAC X1Y6	GTM Dual 228 X1Y4
SLR Crossing				
GTY Quad 127 X0Y12-X0Y15	CMAC X0Y5	HP I/O Bank 67	ILKN X1Y3	GTY Quad 227 X1Y12-X1Y15
GTY Quad 126 X0Y8-X0Y11	CMAC X0Y4	HP I/O Bank 66	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11
GTY Quad 125 X0Y4-X0Y7 (RCAL)	ILKN X0Y2	HP I/O Bank 65	Configuration	GTY Quad 225 X1Y4-X1Y7 (RCAL)
GTY Quad 124 X0Y0-X0Y3	CMAC X0Y3	HP I/O Bank 64	PCIE4 X0Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3
SLR Crossing				
GTM Dual 123 X0Y3	CMAC X0Y2	HP I/O Bank 63	ILKN X1Y1	GTM Dual 223 X1Y3
GTM Dual 122 X0Y2	CMAC X0Y1	HP I/O Bank 62	SYSMON Configuration	GTM Dual 222 X1Y2
GTM Dual 121 X0Y1 (RCAL)	ILKN X0Y0	HP I/O Bank 61	Configuration	GTM Dual 221 X1Y1 (RCAL)
GTM Dual 120 X0Y0	CMAC X0Y0	HP I/O Bank 60	CMAC X1Y0	GTM Dual 220 X1Y0

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Figure 1-145: **XCVU29P Banks**

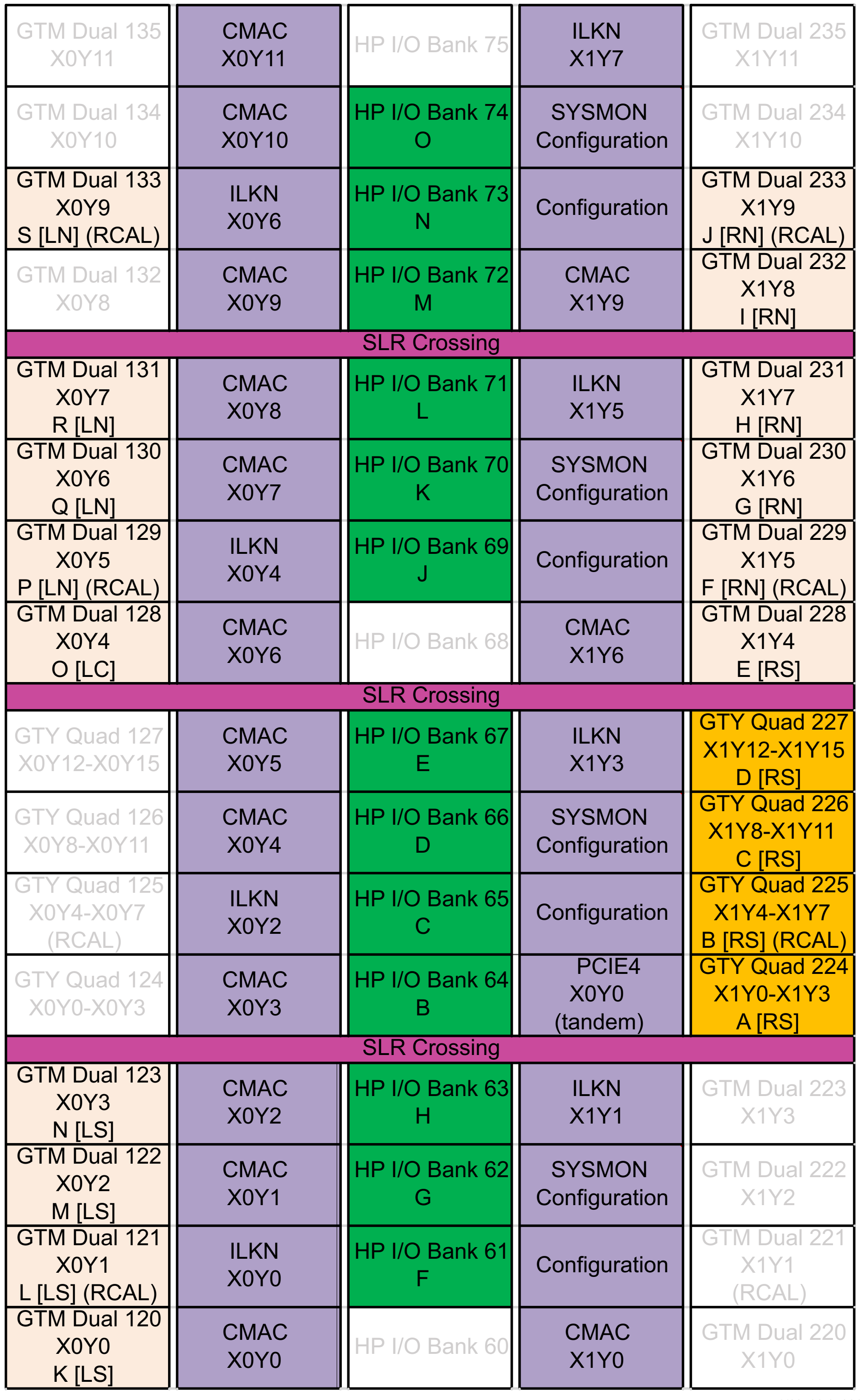

Figure 1-146: **XCVU29P Banks in FIGD2104 Package**

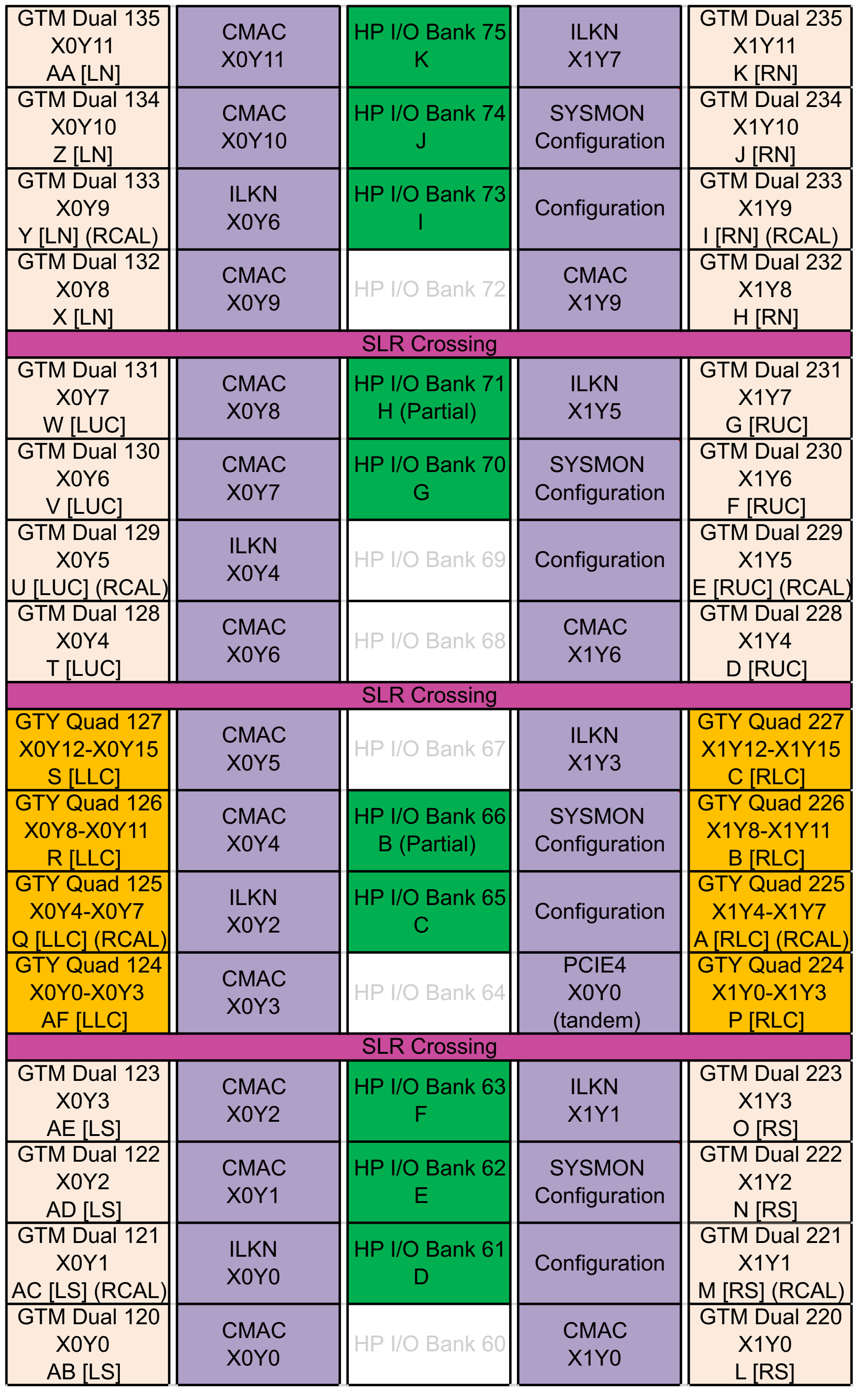

Figure 1-147: **XCVU29P Banks in FSGA2577 Package**

XCVU31P Bank Diagrams

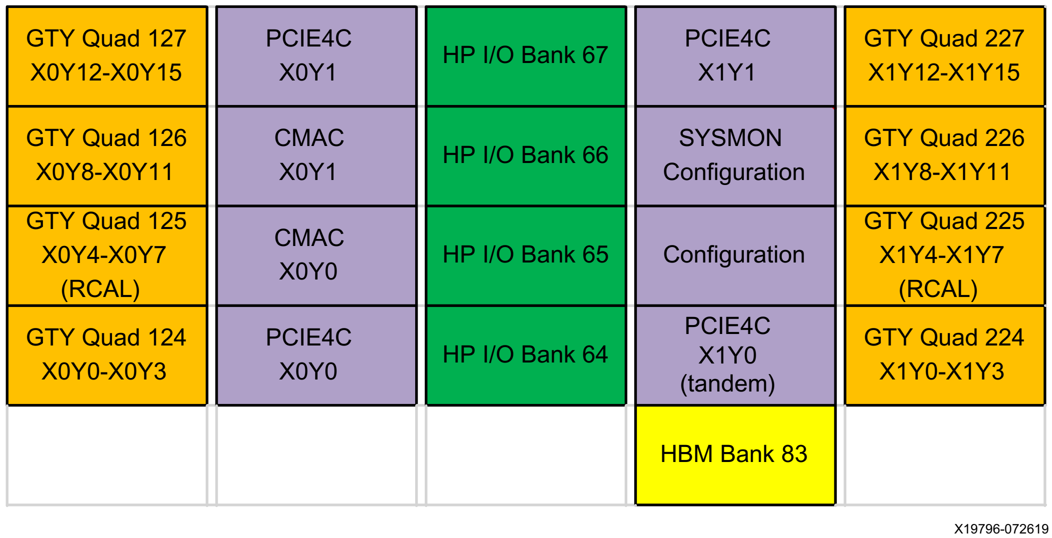

Figure 1-148: **XCVU31P Banks**

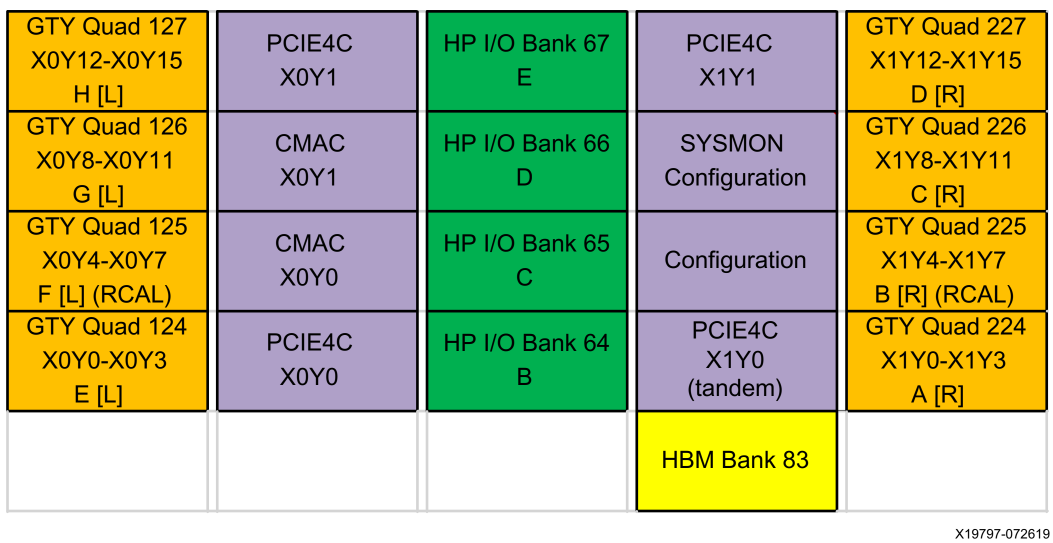

Figure 1-149: **XCVU31P Banks in FSVH1924 Package**

XCVU33P Bank Diagrams

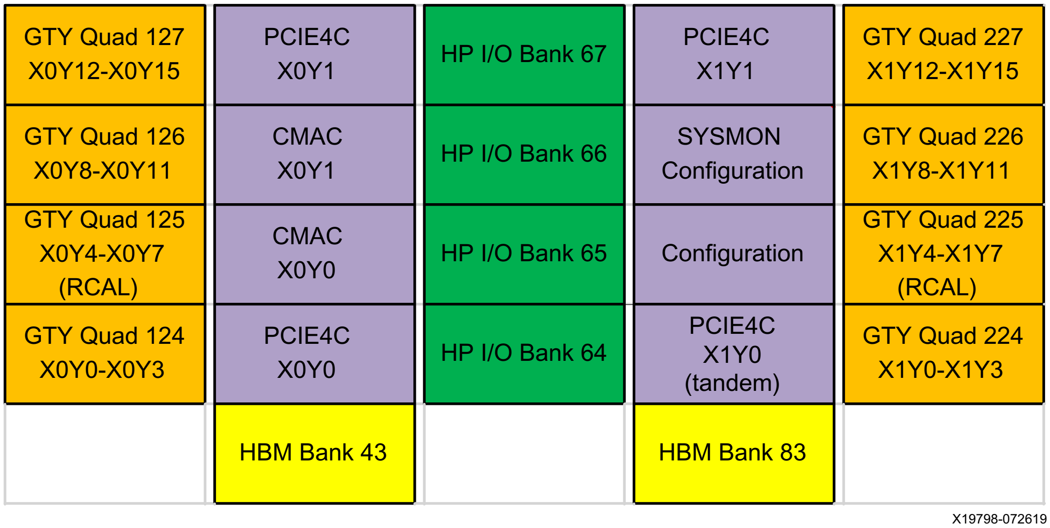

Figure 1-150: **XCVU33P Banks**

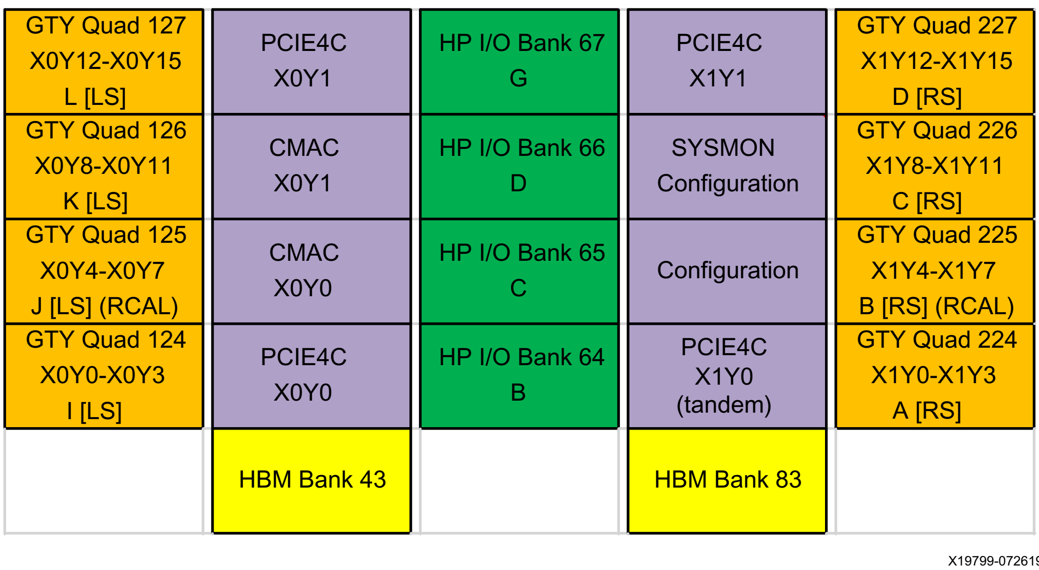

Figure 1-151: **XCVU33P Banks in FSVH2104 Package**

XCVU35P and XCVU45P Bank Diagrams

Figure 1-152: **XCVU35P and XCVU45P Banks**

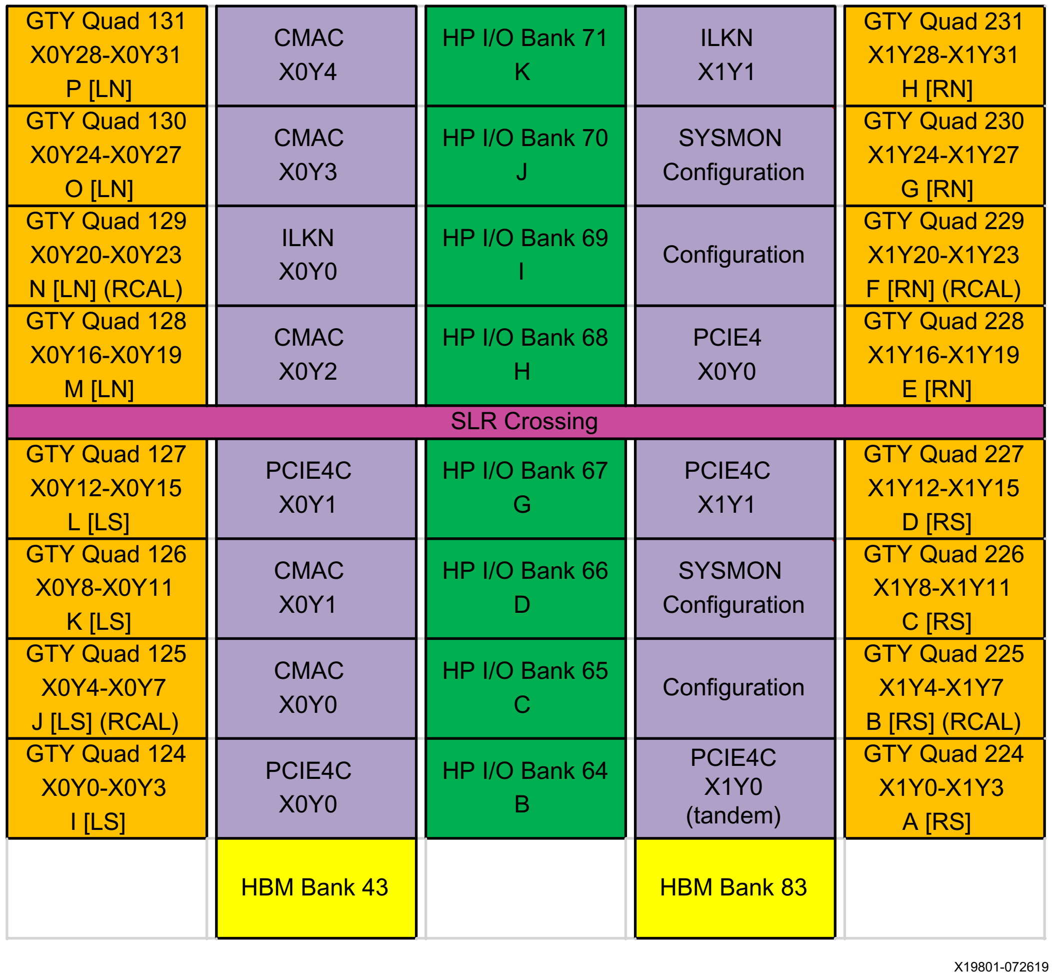

Figure 1-153: **XCVU35P and XCVU45P Banks in FSVH2104 Package**

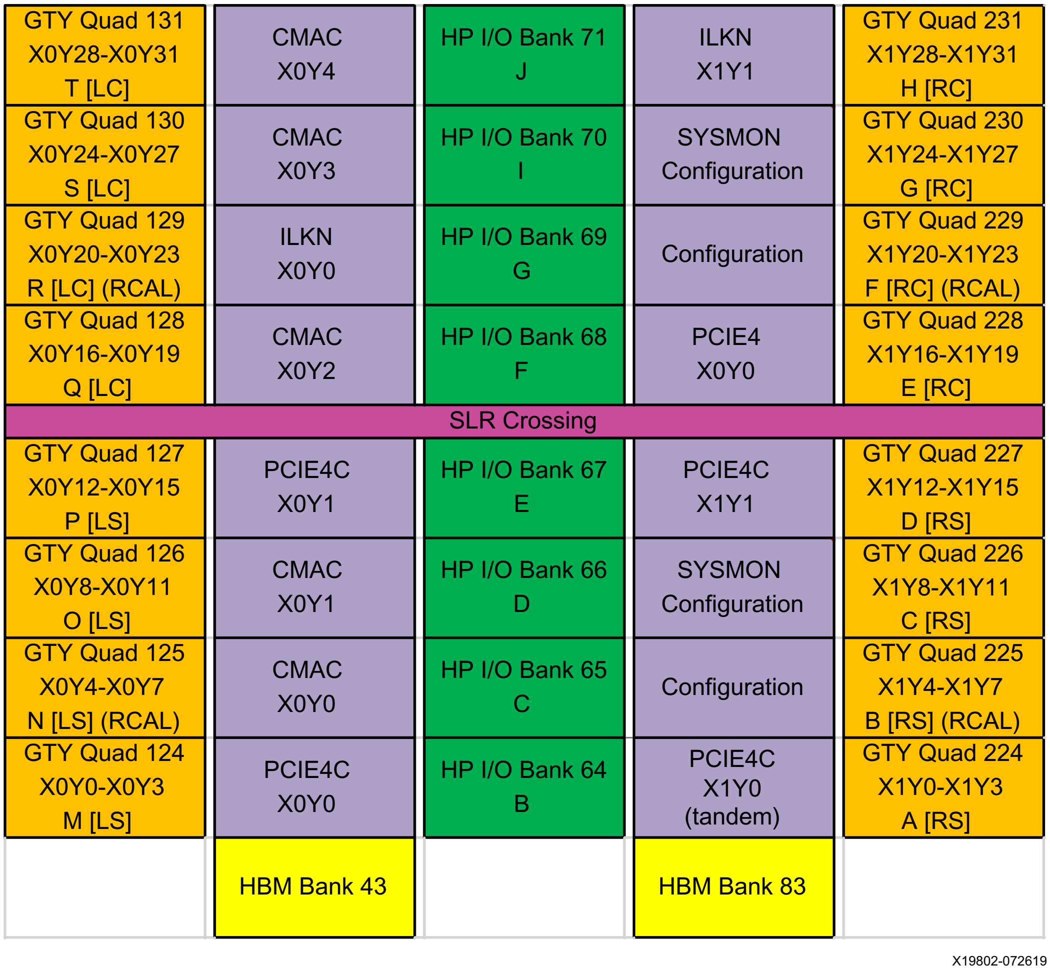

Figure 1-154: **XCVU35P and XCVU45P Banks in FSVH2892 Package**

XCVU37P and XCVU47P Bank Diagrams

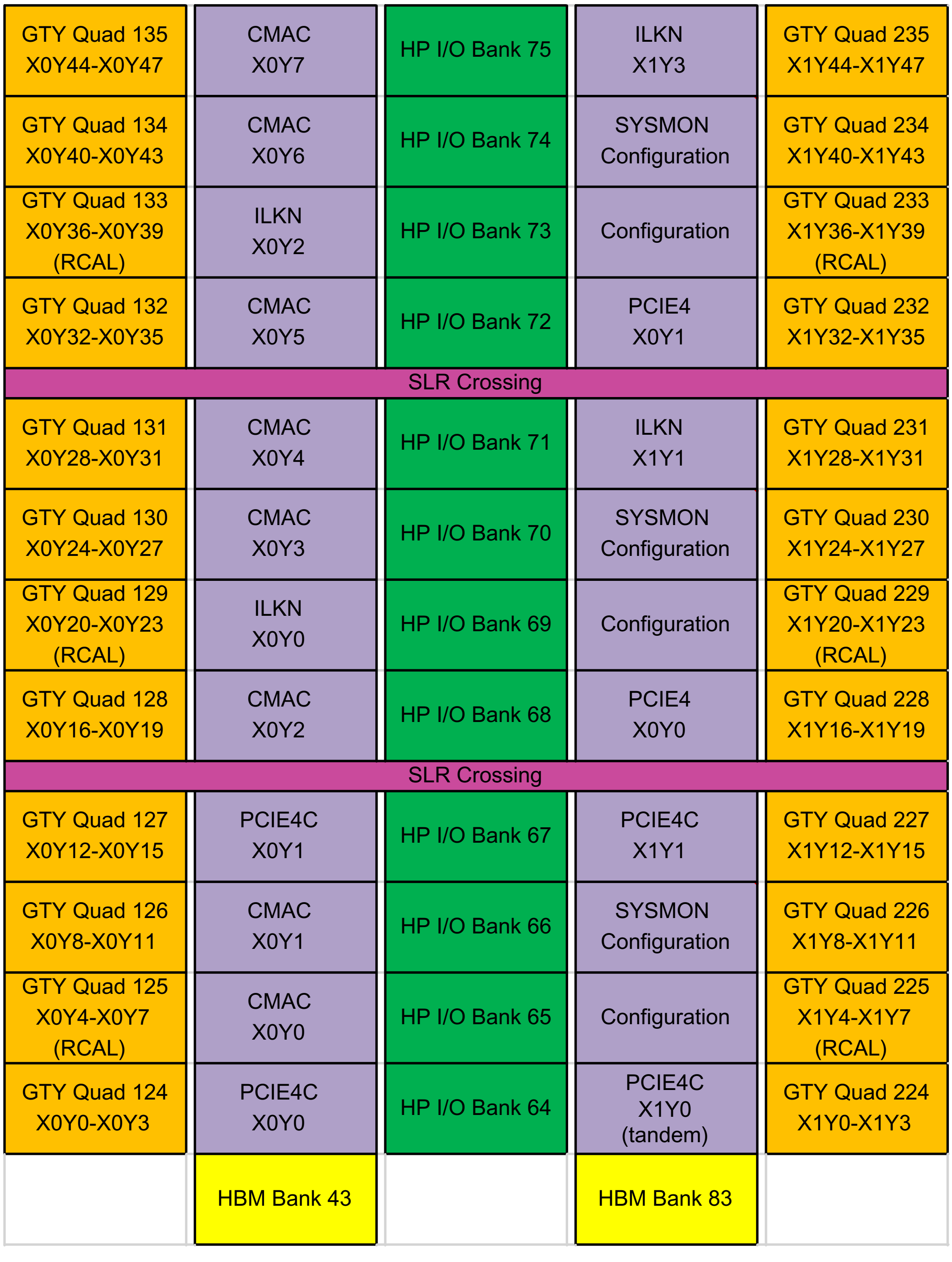

Figure 1-155: **XCVU37P and XCVU47P Banks**

GTY Quad 135 X0Y44-X0Y47 X [LN]	CMAC X0Y7	HP I/O Bank 75 N	ILKN X1Y3	GTY Quad 235 X1Y44-X1Y47 L [RN]
GTY Quad 134 X0Y40-X0Y43 W [LN]	CMAC X0Y6	HP I/O Bank 74 M	SYSMON Configuration	GTY Quad 234 X1Y40-X1Y43 K [RN]
GTY Quad 133 X0Y36-X0Y39 V [LN] (RCAL)	ILKN X0Y2	HP I/O Bank 73 L	Configuration	GTY Quad 233 X1Y36-X1Y39 J [RN] (RCAL)
GTY Quad 132 X0Y32-X0Y35 U [LN]	CMAC X0Y5	HP I/O Bank 72 K	PCIE4 X0Y1	GTY Quad 232 X1Y32-X1Y35 I [RN]
		SLR Crossing		
GTY Quad 131 X0Y28-X0Y31 T [LC]	CMAC X0Y4	HP I/O Bank 71 J	ILKN X1Y1	GTY Quad 231 X1Y28-X1Y31 H [RC]
GTY Quad 130 X0Y24-X0Y27 S [LC]	CMAC X0Y3	HP I/O Bank 70 I	SYSMON Configuration	GTY Quad 230 X1Y24-X1Y27 G [RC]
GTY Quad 129 X0Y20-X0Y23 R [LC] (RCAL)	ILKN X0Y0	HP I/O Bank 69 G	Configuration	GTY Quad 229 X1Y20-X1Y23 F [RC] (RCAL)
GTY Quad 128 X0Y16-X0Y19 Q [LC]	CMAC X0Y2	HP I/O Bank 68 F	PCIE4 X0Y0	GTY Quad 228 X1Y16-X1Y19 E [RC]
		SLR Crossing		
GTY Quad 127 X0Y12-X0Y15 P [LS]	PCIE4C X0Y1	HP I/O Bank 67 E	PCIE4C X1Y1	GTY Quad 227 X1Y12-X1Y15 D [RS]
GTY Quad 126 X0Y8-X0Y11 O [LS]	CMAC X0Y1	HP I/O Bank 66 D	SYSMON Configuration	GTY Quad 226 X1Y8-X1Y11 C [RS]
GTY Quad 125 X0Y4-X0Y7 N [LS] (RCAL)	CMAC X0Y0	HP I/O Bank 65 C	Configuration	GTY Quad 225 X1Y4-X1Y7 B [RS] (RCAL)
GTY Quad 124 X0Y0-X0Y3 M [LS]	PCIE4C X0Y0	HP I/O Bank 64 B	PCIE4C X1Y0 (tandem)	GTY Quad 224 X1Y0-X1Y3 A [RS]
	HBM Bank 43		HBM Bank 83	

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Figure 1-156: **XCVU37P and XCVU47P Banks in FSVH2892 Package**

XCVU57P Bank Diagrams

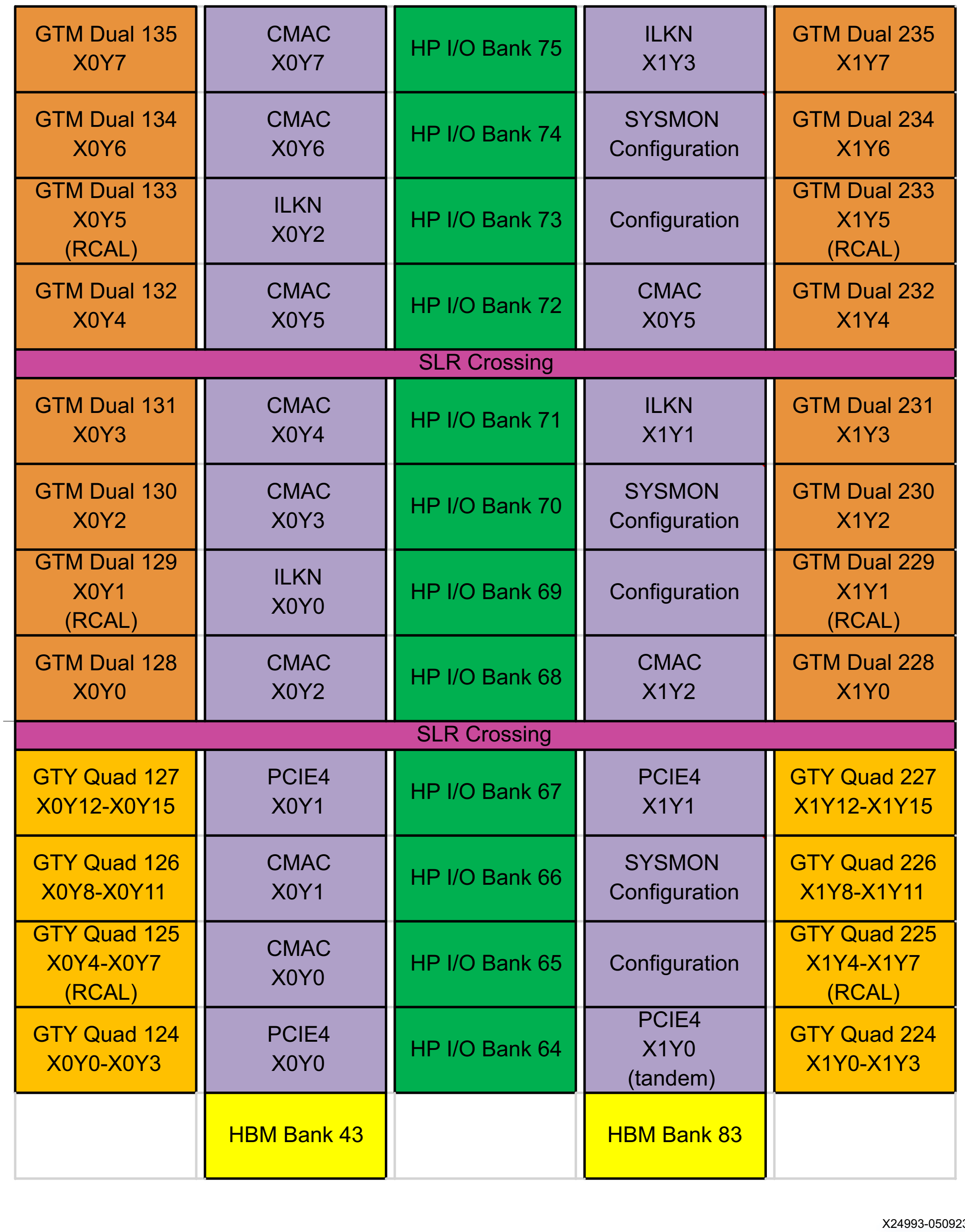


Figure 1-157: **XCVU57P Banks**

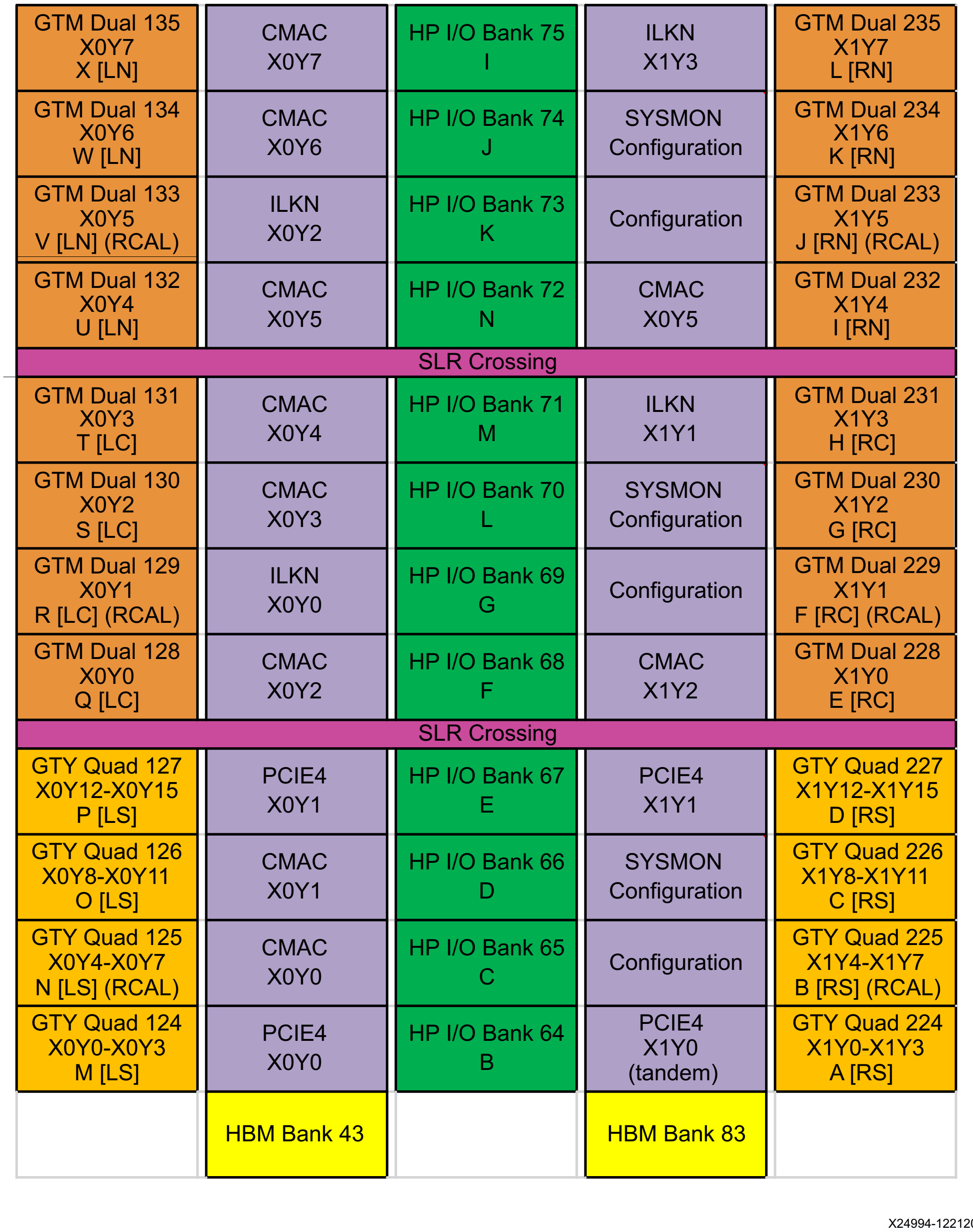


Figure 1-158: **XCVU57P Banks in FSVK2892 Package**

XCSU10P Bank Diagrams

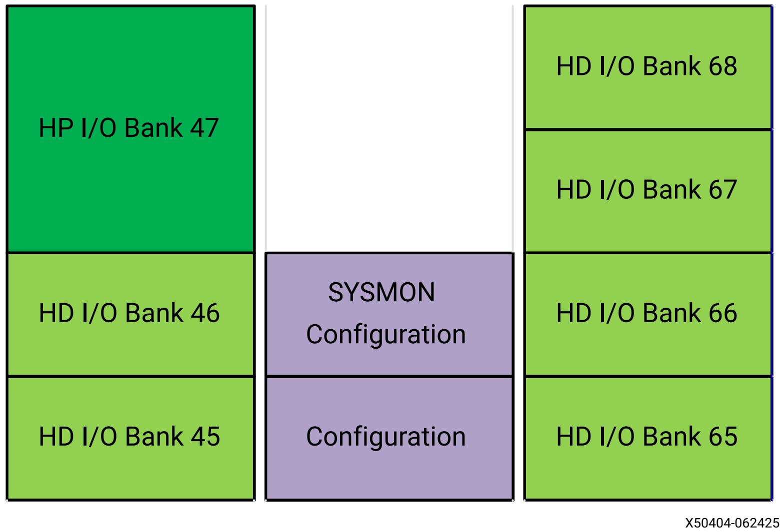


Figure 1-159: **XCSU10P Banks**

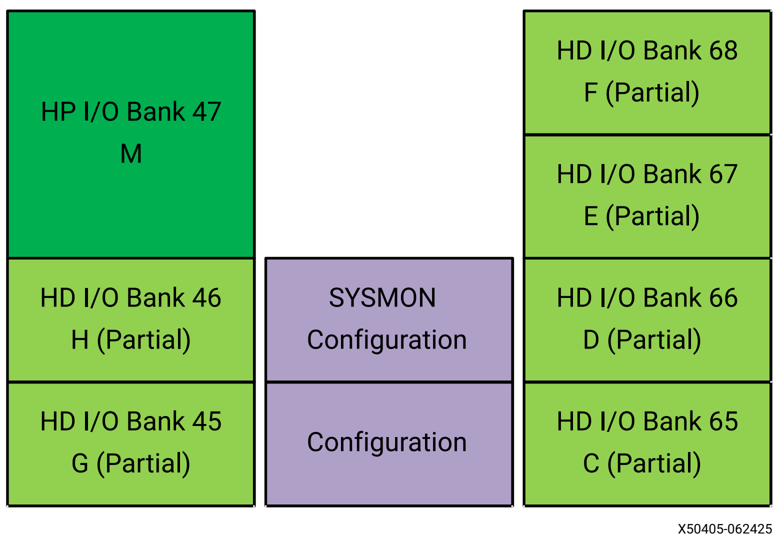


Figure 1-160: **XCSU10P Banks in CMVA361 Package**

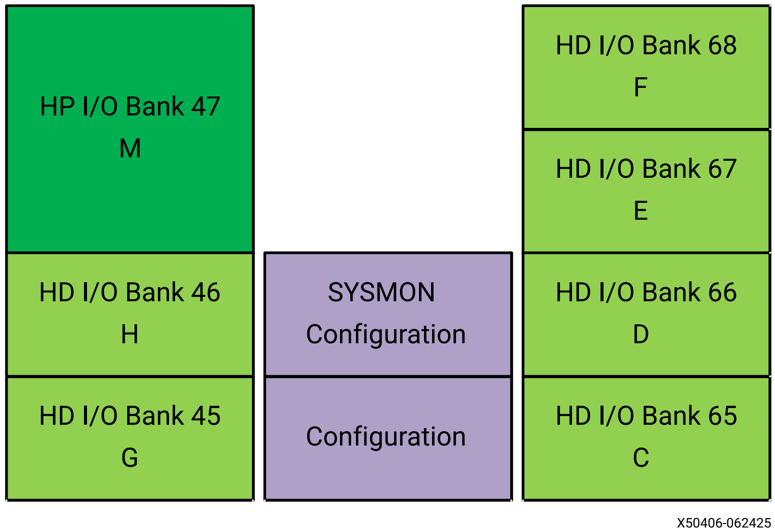


Figure 1-161: **XCSU10P Banks in CMVA529 Package**

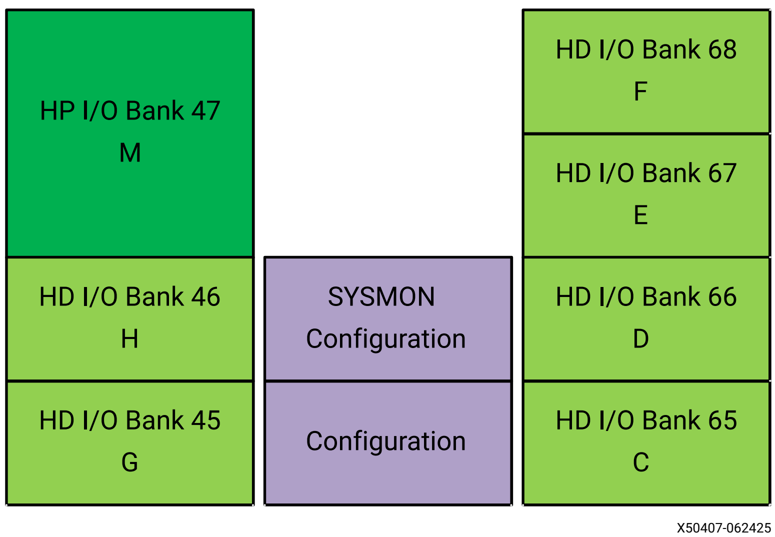


Figure 1-162: **XCSU10P Banks in SBVB625 Package**

XCSU25P Bank Diagrams

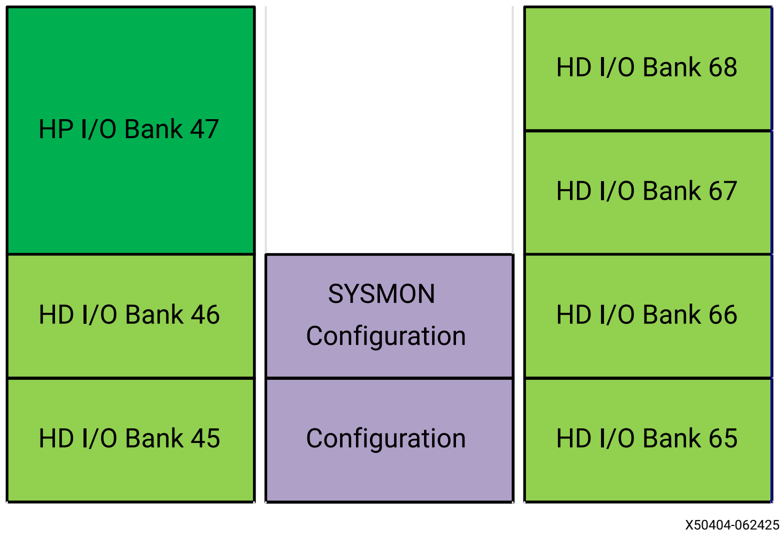


Figure 1-163: **XCSU25P Banks**

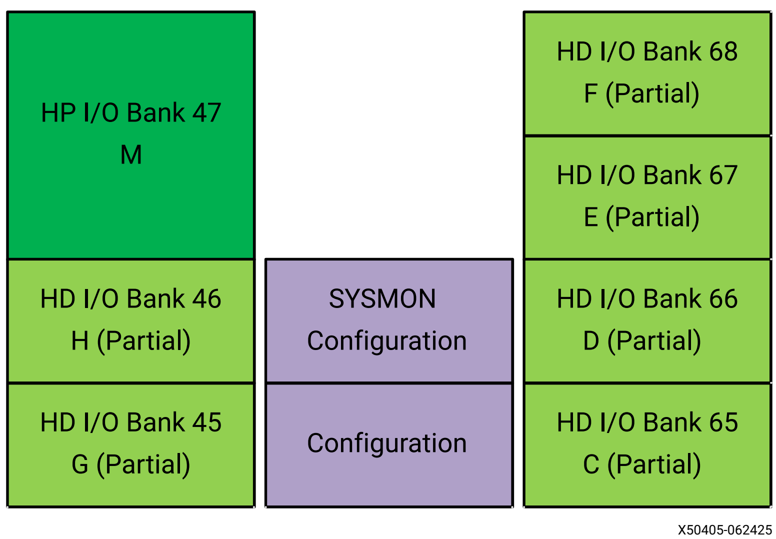


Figure 1-164: **XCSU25P Banks in CMVA361 Package**

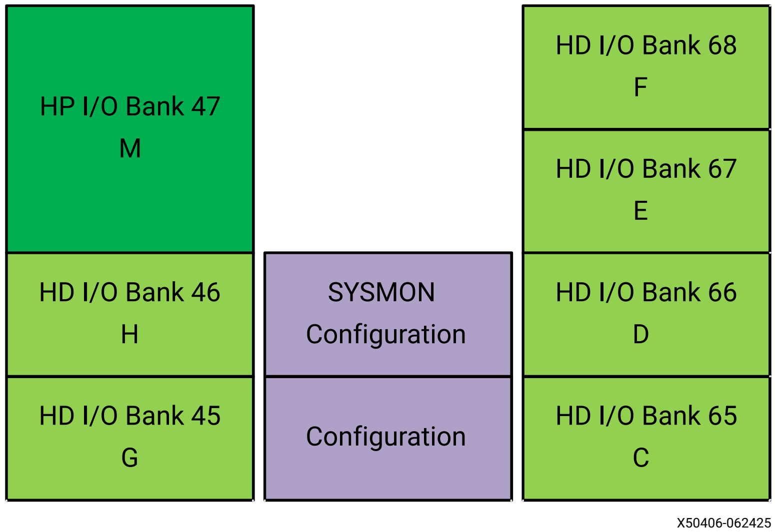


Figure 1-165: **XCSU25P Banks in CMVA529 Package**

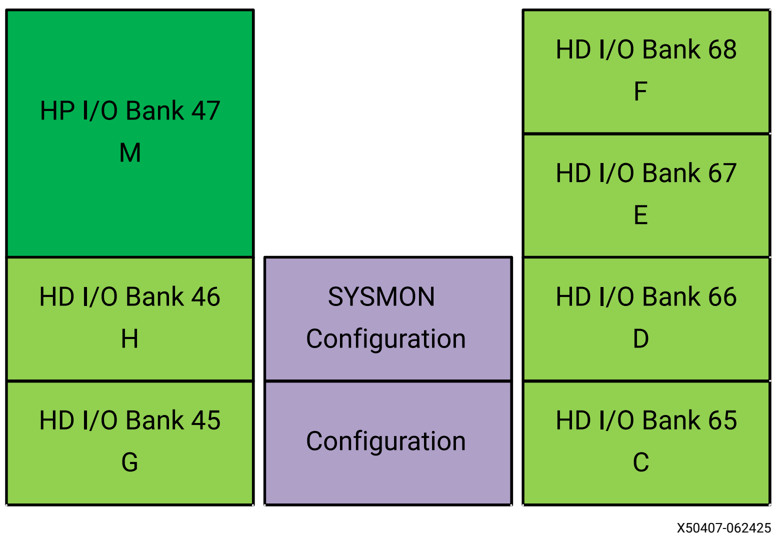


Figure 1-166: **XCSU25P Banks in SBVB625 Package**

XCSU35P Bank Diagrams

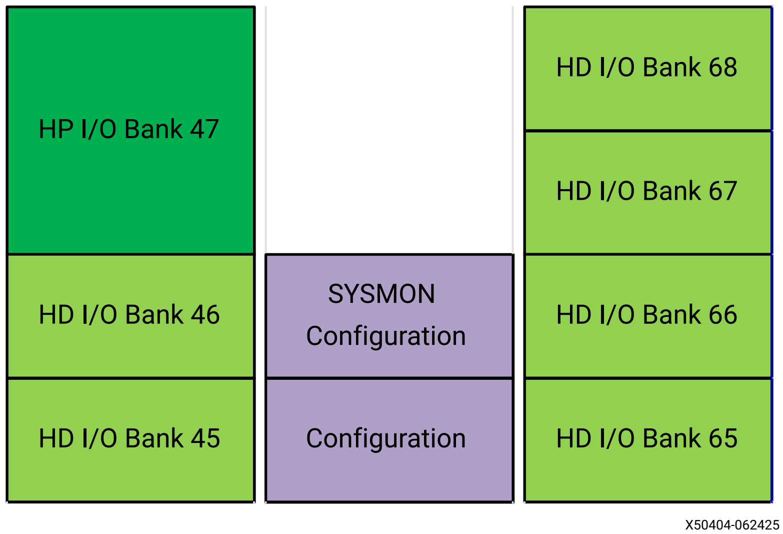


Figure 1-167: **XCSU35P Banks**

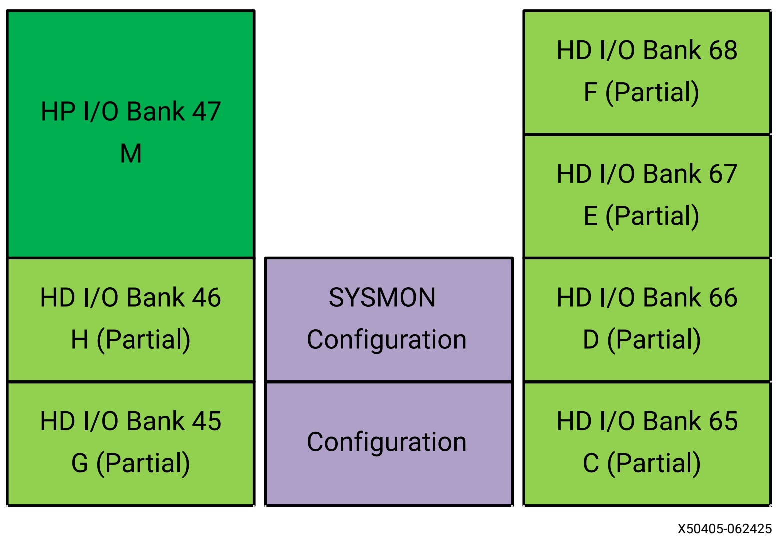


Figure 1-168: **XCSU35P Banks in CMVA361 Package**

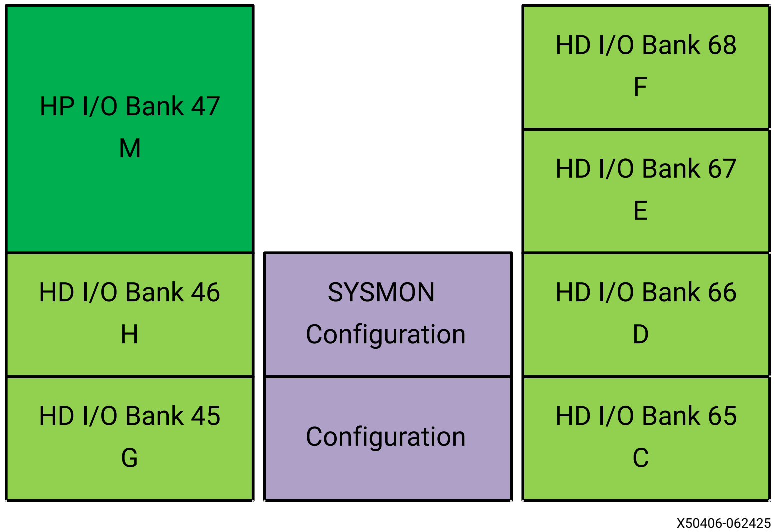


Figure 1-169: **XCSU35P Banks in CMVA529 Package**

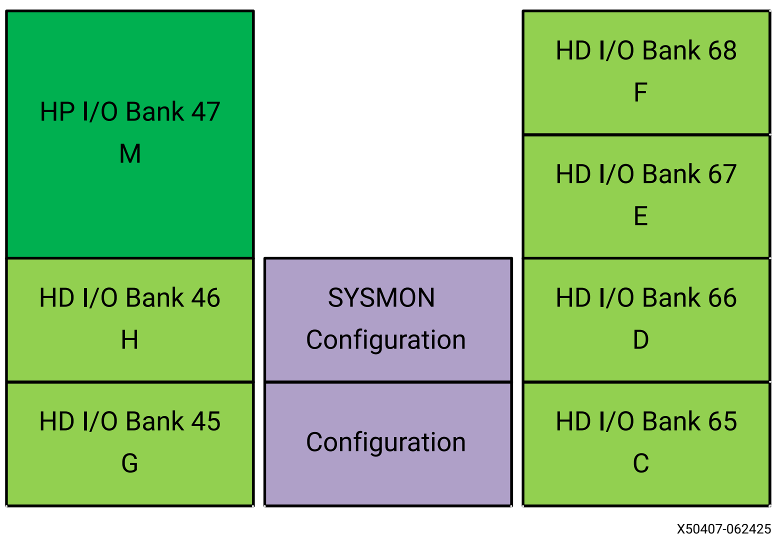


Figure 1-170: **XCSU35P Banks in SBVB625 Package**

Package Files

About ASCII Package Files

The ASCII package files for each package include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor in fixed-width fonts. The information in each of the files includes:

- Device/Package name (*family-device-package*), with date and time of creation
- Seven columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3 split into upper (U) and lower (L) halves. For more information on the memory byte group, see the *UltraScale Architecture FPGAs Memory IP Product Guide* (PG150).
  - Bank—Bank number.
  - I/O Type—CONFIG, HD, HR, HP, or GT (GTH, GTY, or GTM) depending on the I/O type. For more information on the I/O type, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
  - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
  - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.

Package Specifications Designations

Package specifications are designated as evaluation only, engineering sample, or production. Each designation is defined as follows.

Evaluation Only

These package specifications are based on initial device specifications, package routability analysis and mechanical package construction. Package specifications with this designation are not stable and package pinouts are likely to change and these specifications should only be used for initial system level design feasibility.

Engineering Sample

These package specifications are based on a released package design and validated with ES engineering sample (ES) devices. Package specifications with this designation are considered stable, however some pinout and mechanical specifications might change prior to the production release of the particular device. Package pinouts with this designation are to be used for PCB and Vivado™ designs using ES devices.

Production

These package specifications are released coincident with production release of a particular device. Customers receive formal notification of any subsequent changes.

ASCII Pinout Files

Links to the ASCII pinout information by device/package are listed in Table 2-1. The pinouts of XQ devices are identical to the pinouts of their equivalent XC devices in footprint compatible package. Links in this table to XQ devices open the XC version of the pinout file. For example, the link to RBA676-XQKU040 opens the FBVA676-XCKU040 pinout file.

Download all available Kintex UltraScale, Kintex UltraScale+, Artix UltraScale+, Spartan UltraScale+, Virtex UltraScale, and Virtex UltraScale+ FPGA package/device/pinout files in the Package File Portal.

Note: All package files are ASCII files in TXT and CSV file format. Only the available files listed in Table 2-1 are linked and consolidated in this ZIP file.

IMPORTANT: *With the exception of InFO packages (package names begin with U), all packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC, and the third digit in the package name is Q (for example: FFQA1156).*

Table 2-1: **Package/Device Pinout Files**

Package	Device			
FCVA289	XCAU7P Engineering Sample	XAAU7P ES		
CMVA361	XCSU10P Production	XCSU25P Production	XCSU35P Production	
UBVA368	XCAU10P Engineering Sample	XCAU15P Engineering Sample		
SBVB484	XCAU10P Production	XCAU15P Production	XAAU10P Production	XAAU15P Production
SBVC484	XCAU7P Engineering Sample	XAAU7P Engineering Sample		
CMVA529	XCSU10P Production	XCSU25P Production	XCSU35P Production	
SBVB625	XCSU10P Production	XCSU25P Production	XCSU35P Production	
FBVA676	XCKU035 Production	XCKU040 Production		
FFVA676	XCKU3P Production	XCKU5P Production		

Table 2-1: **Package/Device Pinout Files *(Cont'd)***

Package	Device						
FFVB676	XCAU10P Production	XCAU15P Production	XCAU20P Production	XCAU25P Production	XCKU3P Production	XCKU5P Production	
FFRB676	XQKU5P Production						
RBA676	XQKU040 Production						
SFVA784	XCKU035 Production	XCKU040 Production					
SFVB784	XCAU20P Production	XCAU25P Production	XCKU3P Production	XCKU5P Production			
SFRB784	XQKU5P Production						
FBVA900	XCKU035 Production	XCKU040 Production					
FFVD900	XCKU3P Production	XCKU5P Production	XCKU11P Production				
FFVE900	XCKU9P Production	XCKU13P Production					
FFVA1156	XCKU025 Production	XCKU035 Production	XCKU040 Production	XCKU060 Production	XCKU095 Production	XCKU11P Production	XCKU15P Production
FFRA1156	XQKU15P Production						
RFA1156	XQKU040 Production	XQKU060 Production	XQKU095 Production				
VSVA1365	XCVU23P Production						
FFVA1517	XCKU060 Production						
FLVA1517	XCKU085 Production	XCKU115 Production					
FFVC1517	XCKU095 Production	XCVU065 Production	XCVU080 Production	XCVU095 Production	XCVU3P Production		
FFRC1517	XQVU3P Production						
FFVD1517	XCVU080 Production	XCVU095 Production					

Table 2-1: **Package/Device Pinout Files *(Cont'd)***

Package	Device			
FLVD1517	XCKU115 Production	XCVU125 Production		
FFVE1517	XCKU11P Production	XCKU15P Production		
FFRE1517	XQKU15P Production			
RLD1517	XQKU115 Production			
FFVA1760	XCKU15P Production			
FFVB1760	XCKU095 Production	XCVU080 Production	XCVU095 Production	
FLVB1760	XCKU085 Production	XCKU115 Production	XCVU125 Production	
FFVE1760	XCKU15P Production			
FFVJ1760	XCVU19P Production			
FSVJ1760	XCVU23P Production			
FLVD1924	XCKU115 Production			
FLVF1924	XCKU085 Production	XCKU115 Production		
FLGF1924	XCVU11P Production			
RLF1924	XQKU115 Production			
FSVH1924	XCVU31P Production			
FFVA2104	XCVU080 Production	XCVU095 Production		
FLVA2104	XCKU115 Production	XCVU125 Production	XCVU5P Production	XCVU7P Production
FLRA2104	XQVU7P Production			

Table 2-1: **Package/Device Pinout Files *(Cont'd)***

Package	Device			
FLGA2104	XCVU9P Production			
FHGA2104	XCVU13P Production			
FFVB2104	XCKU095 Production	XCVU080 Production	XCVU095 Production	XCKU19P Production
FLVB2104	XCKU115 Production	XCVU125 Production	XCVU5P Production	XCVU7P Production
FLRB2104	XQVU7P Production			
FLGB2104	XCVU160 Production	XCVU190 Production	XCVU9P Production	XCVU11P Production
FHGB2104	XCVU13P Production			
FFVC2104	XCVU095 Production			
FLVC2104	XCVU125 Production	XCVU5P Production	XCVU7P Production	
FLGC2104	XCVU160 Production	XCVU190 Production	XCVU9P Production	XCVU11P Production
FLRC2104	XQVU11P Production			
FHGC2104	XCVU13P Production			
FIGD2104	XCVU13P Production	XCVU27P Production	XCVU29P Production	
FSGD2104	XCVU9P Production	XCVU11P Production		
FSVH2104	XCVU33P Production	XCVU35P Production	XCVU45P Production	
FLGB2377	XCVU440 Production			
FLGA2577	XCVU190 Production	XCVU9P Production	XCVU11P Production	XCVU13P Production
FSGA2577	XCVU13P Production	XCVU27P Production	XCVU29P Production	

Table 2-1: **Package/Device Pinout Files *(Cont'd)***

Package	Device		
FLGA2892	XCVU440 Production		
FSVH2892	XCVU35P Production	XCVU37P Production	XCVU47P Production
FSVK2892	XCVU57P Production		
FSVA3824	XCVU19P Production		
FSVB3824	XCVU19P Production		

Chapter 3

Device Diagrams

Summary

The diagrams in this chapter show a top-view perspective of the package pinout of each UltraScale and UltraScale+ device/package combination. Table 3-1 through Table 3-4 contain cross references to the device diagrams. The I/O-bank diagram shows the location of each user I/O and GTH/GTY transceiver and the respective bank or GT quad. The configuration-power diagram shows the location of every power pin and dedicated as well as multi-function configuration pin in the package. See Package Specifications Designations in Chapter 2 for definitions of Evaluation Only, Engineering Sample, and Production device diagrams.

IMPORTANT: *All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC, and the third digit in the package name is Q (for example: FFQA1156).*

Table 3-1: **Cross-Reference to Kintex UltraScale and XQ Kintex UltraScale Device Diagrams by Package**

Package	Footprint Compatible Devices					Package Status
FBVA676	XCKU035 page 212	XCKU040 page 212				Production
RBA676	XQKU040 page 212					Production
SFVA784	XCKU035 page 214	XCKU040 page 214				Production
FBVA900	XCKU035 page 216	XCKU040 page 216				Production
FFVA1156	XCKU025 page 218	XCKU035 page 220	XCKU040 page 222	XCKU060 page 224	XCKU095 page 226	Production
RFA1156	XQKU040 page 222	XQKU060 page 224	XQKU095 page 226			Production
FFVA1517	XCKU060 page 228					Production

Table 3-1: **Cross-Reference to Kintex UltraScale and XQ Kintex UltraScale Device Diagrams by Package *(Cont'd)***

Package	Footprint Compatible Devices			Package Status
FLVA1517	XCKU085 page 230	XCKU115 page 230		Production
FFVC1517	XCKU095 page 232			Production
FLVD1517	XCKU115 page 234			Production
RLD1517	XQKU115 page 234			Production
FFVB1760	XCKU095 page 236			Production
FLVB1760	XCKU085 page 238	XCKU115 page 240		Production
FLVD1924	XCKU115 page 242			Production
FLVF1924	XCKU085 page 244	XCKU115 page 246		Production
RLF1924	XQKU115 page 246			Production
FLVA2104	XCKU115 page 248			Production
FFVB2104	XCKU095 page 250			Production
FLVB2104	XCKU115 page 252			Production

Table 3-2: **Cross-Reference to Virtex UltraScale Device Diagrams by Package**

Package	Footprint Compatible Devices			Package Status
FFVC1517	XCVU065 page 254	XCVU080 page 256	XCVU095 page 256	Production
FFVD1517	XCVU080 page 258	XCVU095 page 258		Production
FLVD1517	XCVU125 page 260			Production
FFVB1760	XCVU080 page 262	XCVU095 page 262		Production
FLVB1760	XCVU125 page 264			Production
FFVA2104	XCVU080 page 266	XCVU095 page 266		Production
FLVA2104	XCVU125 page 268			Production
FFVB2104	XCVU080 page 270	XCVU095 page 270		Production
FLVB2104	XCVU125 page 272			Production
FLGB2104	XCVU160 page 274	XCVU190 page 274		Production
FFVC2104	XCVU095 page 276			Production
FLVC2104	XCVU125 page 278			Production
FLGC2104	XCVU160 page 280	XCVU190 page 280		Production
FLGB2377	XCVU440 page 282			Production
FLGA2577	XCVU190 page 284			Production
FLGA2892	XCVU440 page 286			Production

Table 3-3: **Cross-Reference to Kintex UltraScale+ and XQ Kintex UltraScale+ Device Diagrams by Package**

Package	Footprint Compatible Devices			Package Status
FFVA676	XCKU3P page 309	XCKU5P page 309		Production
FFVB676	XCKU3P page 311	XCKU5P page 311		Production
FFRB676	XQKU5P page 311			Production
SFVB784	XCKU3P page 313	XCKU5P page 313		Production
SFRB784	XQKU5P page 313			Production
FFVD900	XCKU3P page 315	XCKU5P page 315	XCKU11P page 317	Production
FFVE900	XCKU9P page 319	XCKU13P page 321		Production
FFVA1156	XCKU11P page 323	XCKU15P page 325		Production
FFRA1156	XQKU15P page 325			Production
FFVE1517	XCKU11P page 327	XCKU15P page 329		Production
FFRE1517	XQKU15P page 329			Production
FFVA1760	XCKU15P page 331			Production
FFVE1760	XCKU15P page 333			Production
FFVJ1760	XCKU19P page 335			Production
FFVB2104	XCKU19P page 337			Production

Table 3-4: **Cross-Reference to Virtex UltraScale+ and XQ Virtex UltraScale+ Device Diagrams by Package**

Package	Footprint Compatible Devices			Package Status
VSVA1365	XCVU23P page 404			Production
FFVC1517	XCVU3P page 340			Production
FFRC1517	XQVU3P page 340			Production
FSVJ1760	XCVU23P page 342			Production
FLGF1924	XCVU11P page 344			Production
FSVH1924	XCVU31P page 346			Production
FLVA2104	XCVU5P page 348	XCVU7P page 348		Production
FFRA2104	XQVU7P page 348			Production
FLGA2104	XCVU9P page 350			Production
FHGA2104	XCVU13P page 352			Production
FLVB2104	XCVU5P page 354	XCVU7P page 354		Production
FLRB2104	XQVU7P page 354			Production
FLGB2104	XCVU9P page 356	XCVU11P page 358		Production
FHGB2104	XCVU13P page 360			Production
FLVC2104	XCVU5P page 362	XCVU7P page 362		Production
FLGC2104	XCVU9P page 364	XCVU11P page 366		Production
FLRC2104	XQVU11P page 366			Production
FHGC2104	XCVU13P page 368			Production

Table 3-4: **Cross-Reference to Virtex UltraScale+ and XQ Virtex UltraScale+ Device Diagrams by Package *(Cont'd)***

Package	Footprint Compatible Devices				Package Status
FSGD2104	XCVU9P page 370	XCVU11P page 372			Production
FIGD2104	XCVU13P page 374				Production
FIGD2104	XCVU27P page 376	XCVU29P page 378			Production
FSVH2104	XCVU33P page 380	XCVU35P page 382	XCVU45P page 382		Production
FLGA2577	XCVU9P page 384	XCVU11P page 386	XCVU13P page 388		Production
FSGA2577	XCVU13P page 388				Production
FSGA2577	XCVU27P page 390	XCVU29P page 392			Production
FSVH2892	XCVU35P page 394	XCVU37P page 396	XCVU45P page 394	XCVU47P page 396	Production
FSVK2892	XCVU57P page 398				Production
FSVA3824	XCVU19P page 400				Production
FSVB3824	XCVU19P page 402				Production

Table 3-5: **Cross-Reference to Artix UltraScale+ Device Diagrams by Package**

Package	Footprint Compatible Devices				Package Status
FCVA289	XCAU7P page 288	XAAU7P page 288			Production
UBVA368	XCAU10P page 307	XCAU15P page 308			Production
SBVB484	XCAU10P page 299	XCAU15P page 301	XAAU10P page 299	XAAU15P page 301	Production
SBVC484	XCAU7P page 289	XAAU7P page 289			Production
FFVB676	XCAU10P page 291	XCAU15P page 293	XAAU10P page 291	XAAU15P page 293	Production
	XCAU20P page 295	XCAU25P page 297			Production
SFVB784	XCAU20P page 303	XCAU25P page 305			Production

Table 3-6: **Cross-Reference to Spartan UltraScale+ Device Diagrams by Package**

Package	Footprint Compatible Devices			Package Status
CMVA361	XCSU10P page 405	XCSU25P page 406	XCSU35P page 407	Production
CMVA529	XCSU10P page 408	XCSU25P page 409	XCSU35P page 410	Production
SBVB625	XCSU10P page 411	XCSU25P page 412	XCSU35P page 413	Production

FBVA676 Package–XCKU035 and XCKU040 and RBA676 Package–XQKU040

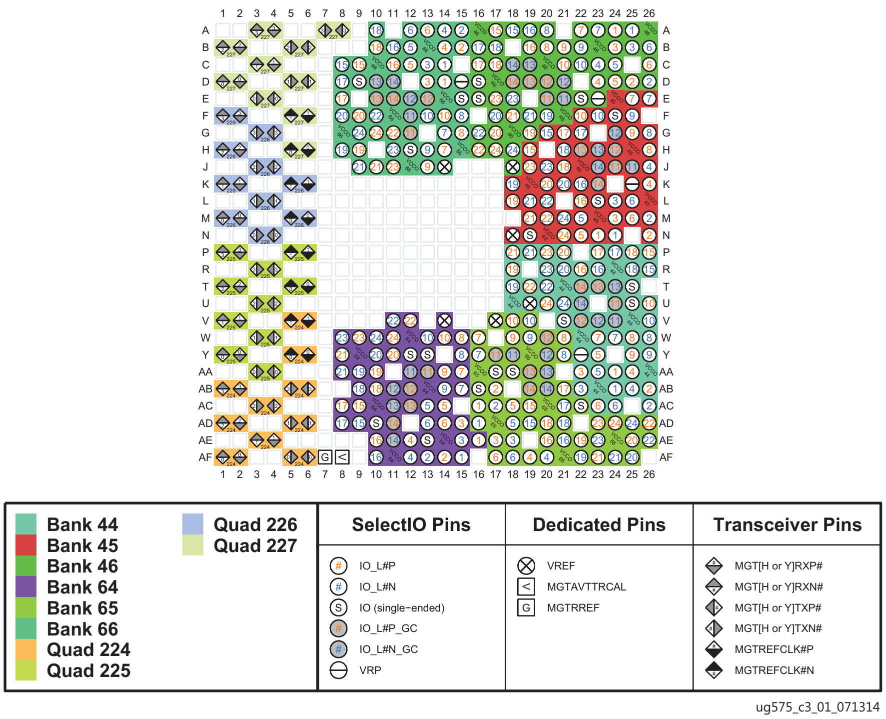
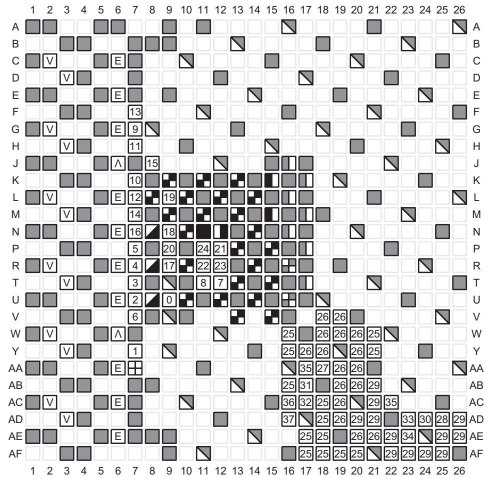


Figure 3-1: **FBVA676 Package—XCKU035 and XCKU040 and RBA676 Package—XQKU040 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-2: **FBVA676 Package—XCKU035 and XCKU040 and RBA676 Package—XQKU040 Configuration/Power Diagram**

SFVA784 (XCKU035 and XCKU040)

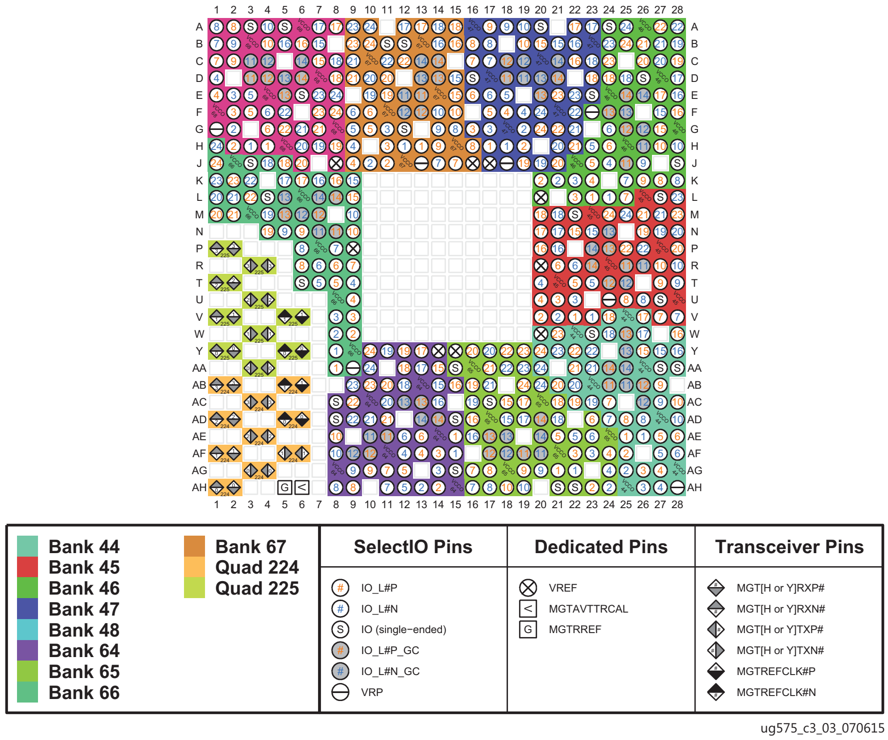
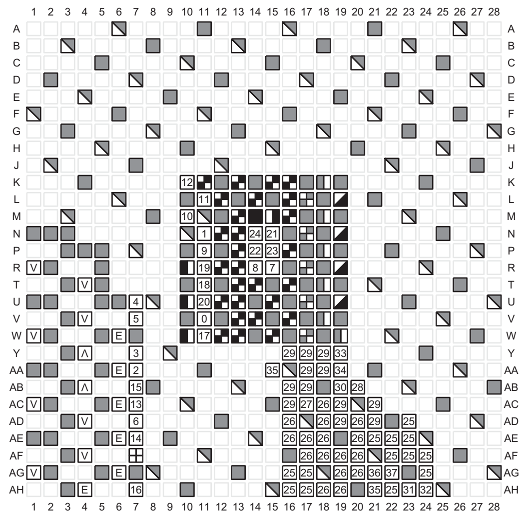


Figure 3-3: **SFVA784 Package—XCKU035 and XCKU040 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi–Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-4: **SFVA784 Package—XCKU035 and XCKU040 Configuration/Power Diagram**

FBVA900 (XCKU035 and XCKU040)

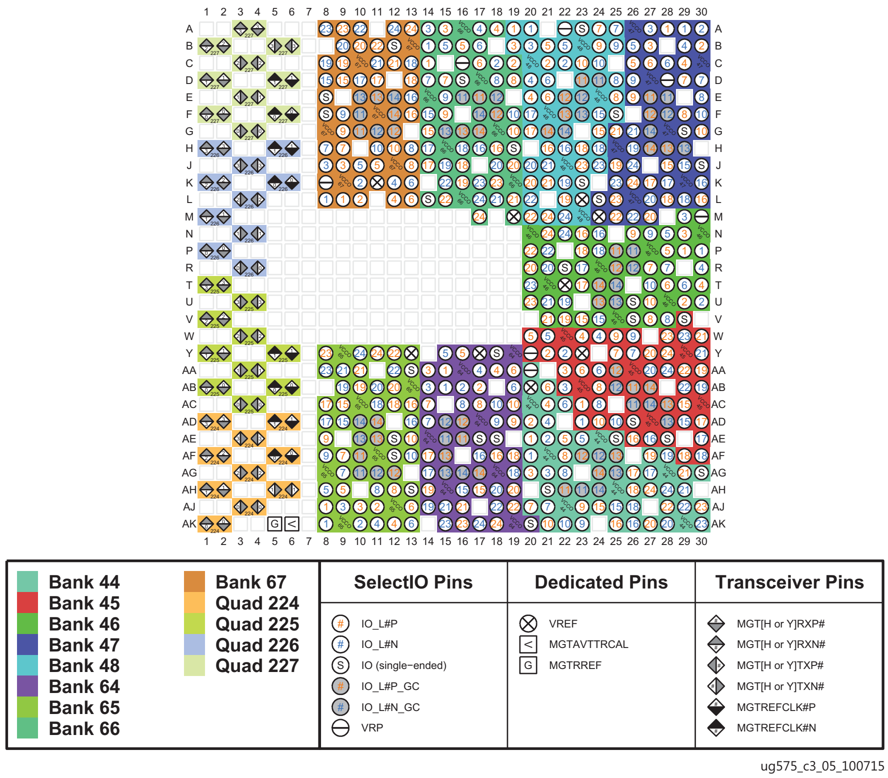
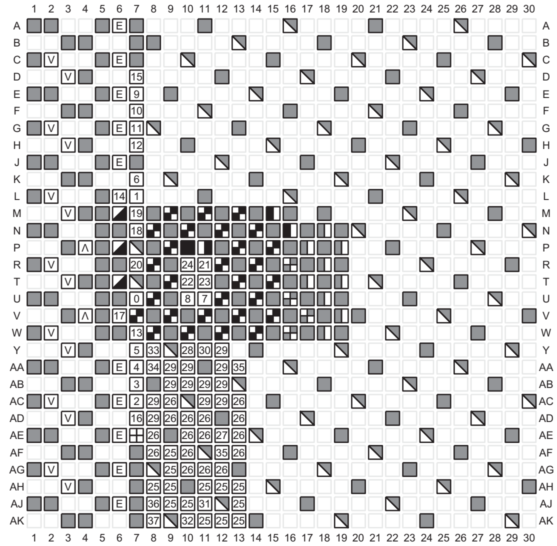


Figure 3-5: **FBVA900 Package—XCKU035 and XCKU040 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-6: **FBVA900 Package—XCKU035 and XCKU040 Configuration/Power Diagram**

FFVA1156 (XCKU025)

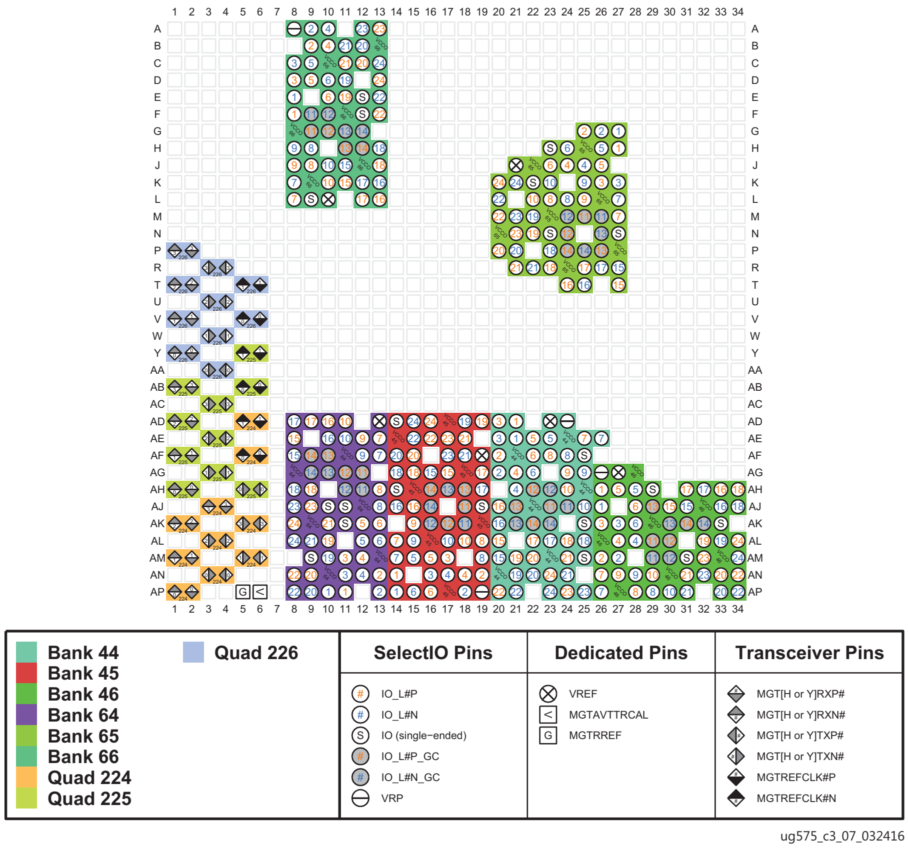
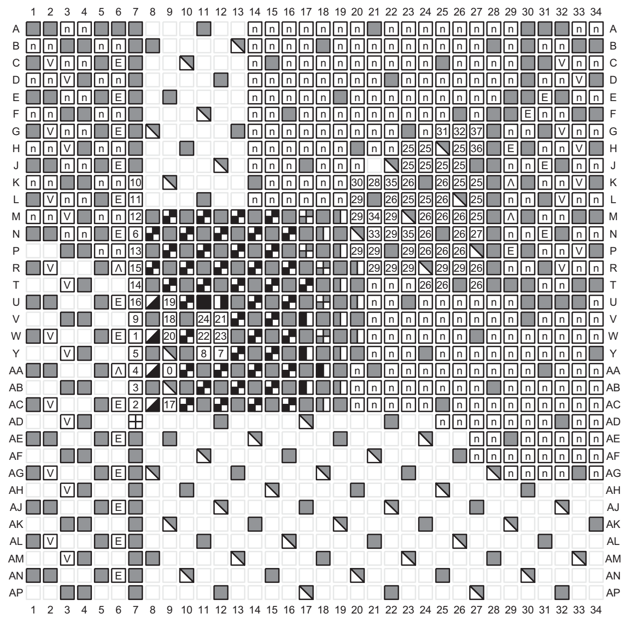


Figure 3-7: **FFVA1156 Package—XCKU025 I/O Bank Diagram**



Power Pins	Dedicated Pins	Multi-Function I/O Pins
GND	0 CCLK_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	28 DOUT_CSO_B
VCCINT	4 D02_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	31 FOE_B
VCCBRAM	7 DXP	32 FWE_FCS2_B
VCCADC	8 DXN	33 I2C_SCLK
GNDADC	9 INIT_B_0	34 I2C_SDA
n NC	10 M0_0	35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0	36 RS0
V MGTAVTT_[R or L]	12 M2_0	37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE	
	14 PROGRAM_B_0	
	15 PUDC_B_0	
	16 RDWR_FCS_B_0	
	17 TCK_0	
	18 TDI_0	
	19 TDO_0	
	20 TMS_0	
	21 VP	
	22 VN	
	23 VREFP	
	24 VREFN	

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Figure 3-8: **FFVA1156 Package—XCKU025 Configuration/Power Diagram**

FFVA1156 (XCKU035)

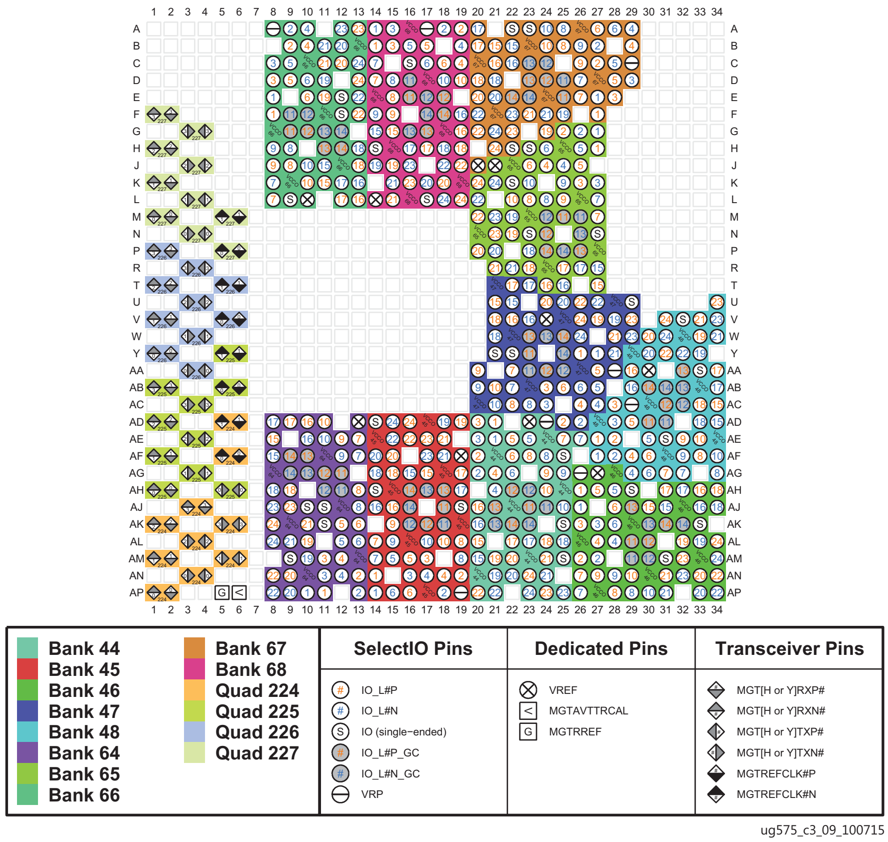


Figure 3-9: **FFVA1156 Package—XCKU035 I/O Bank Diagram**

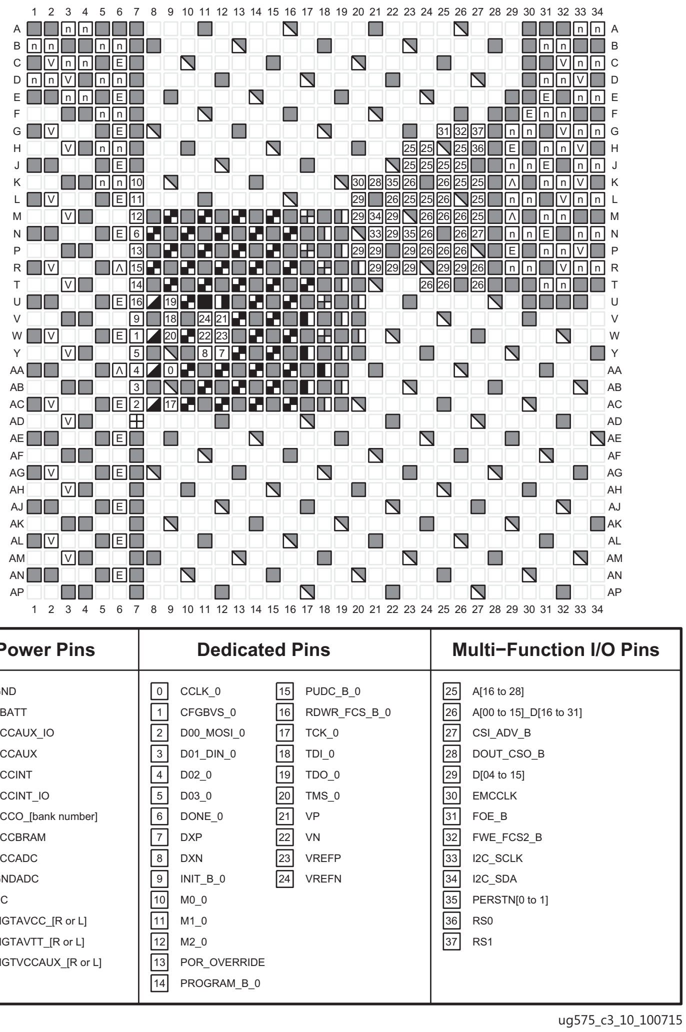


Figure 3-10: **FFVA1156 Package—XCKU035 Configuration/Power Diagram**

FFVA1156 (XCKU040) and RFA1156 (XQKU040)

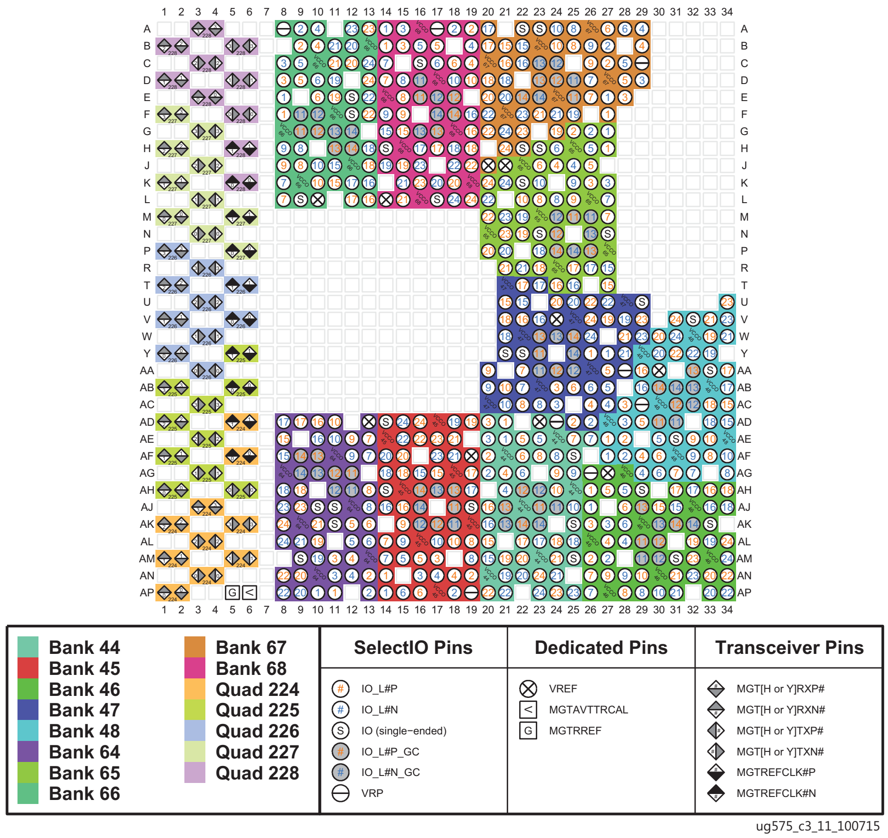
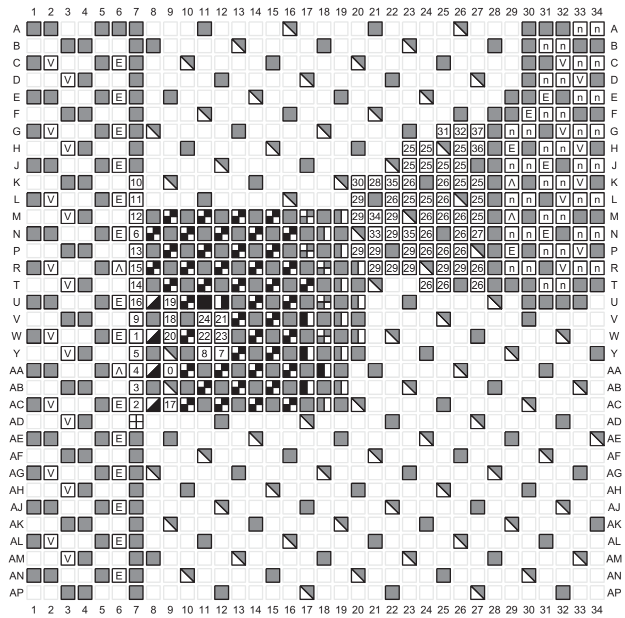


Figure 3-11: **FFVA1156 Package—XCKU040 and RFA1156 Package—XQKU040 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-12: **FFVA1156 Package—XCKU040 and RFA1156 Package—XQKU040 Configuration/Power Diagram**

FFVA1156 (XCKU060) and RFA1156 (XQKU060)

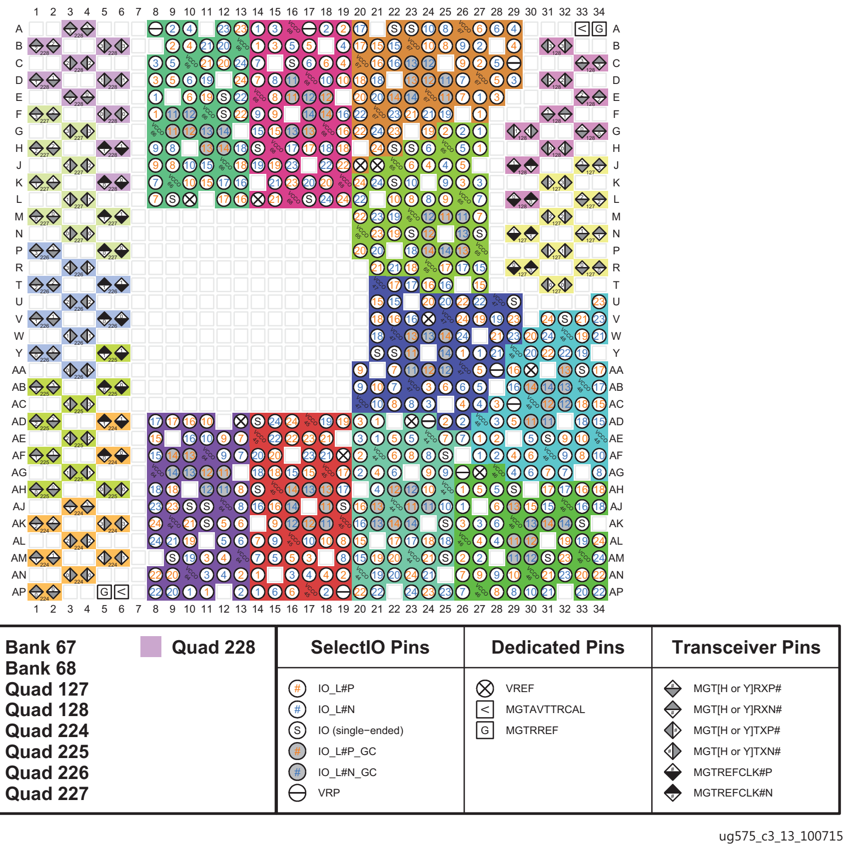
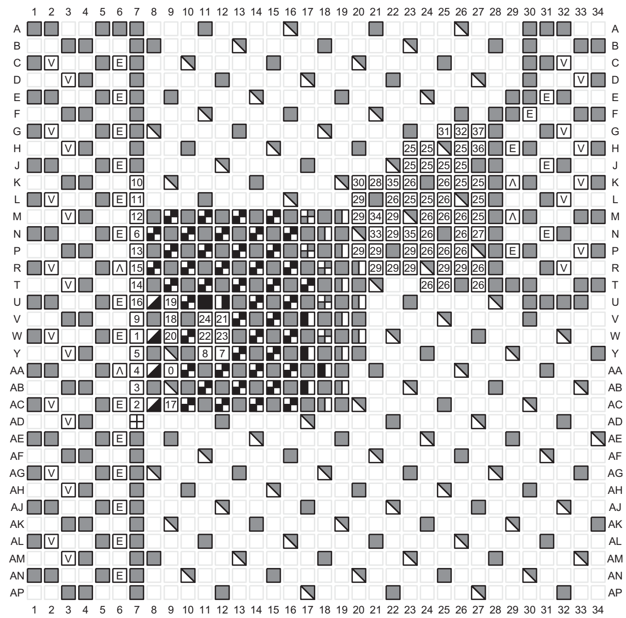


Figure 3-13: **FFVA1156 Package—XCKU060 and RFA1156 Package—XQKU060 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-14: **FFVA1156 Package—XCKU060 and RFA1156 Package—XQKU060 Configuration/Power Diagram**

FFVA1156 (XCKU095) and RFA1156 (XQKU095)

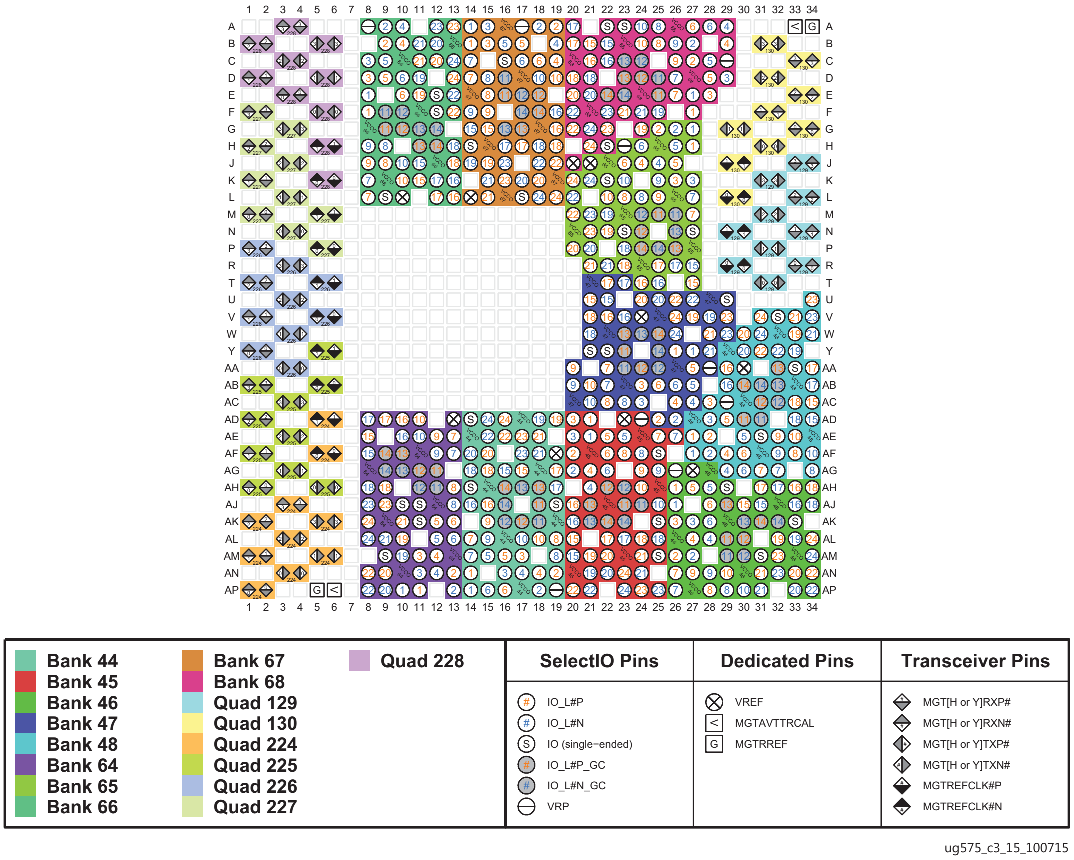
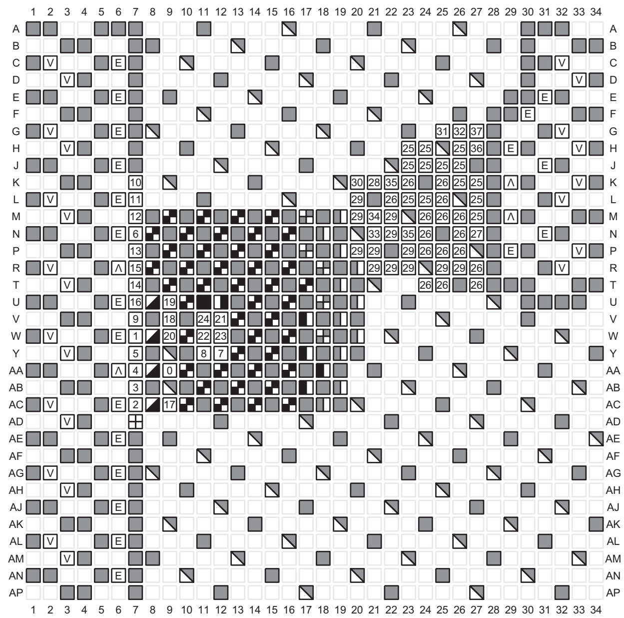


Figure 3-15: **FFVA1156 Package—XCKU095 and RFA1156 Package—XQKU095 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-16: **FFVA1156 Package—XCKU095 and RFA1156 Package—XQKU095 Configuration/Power Diagram**

FFVA1517 (XCKU060)

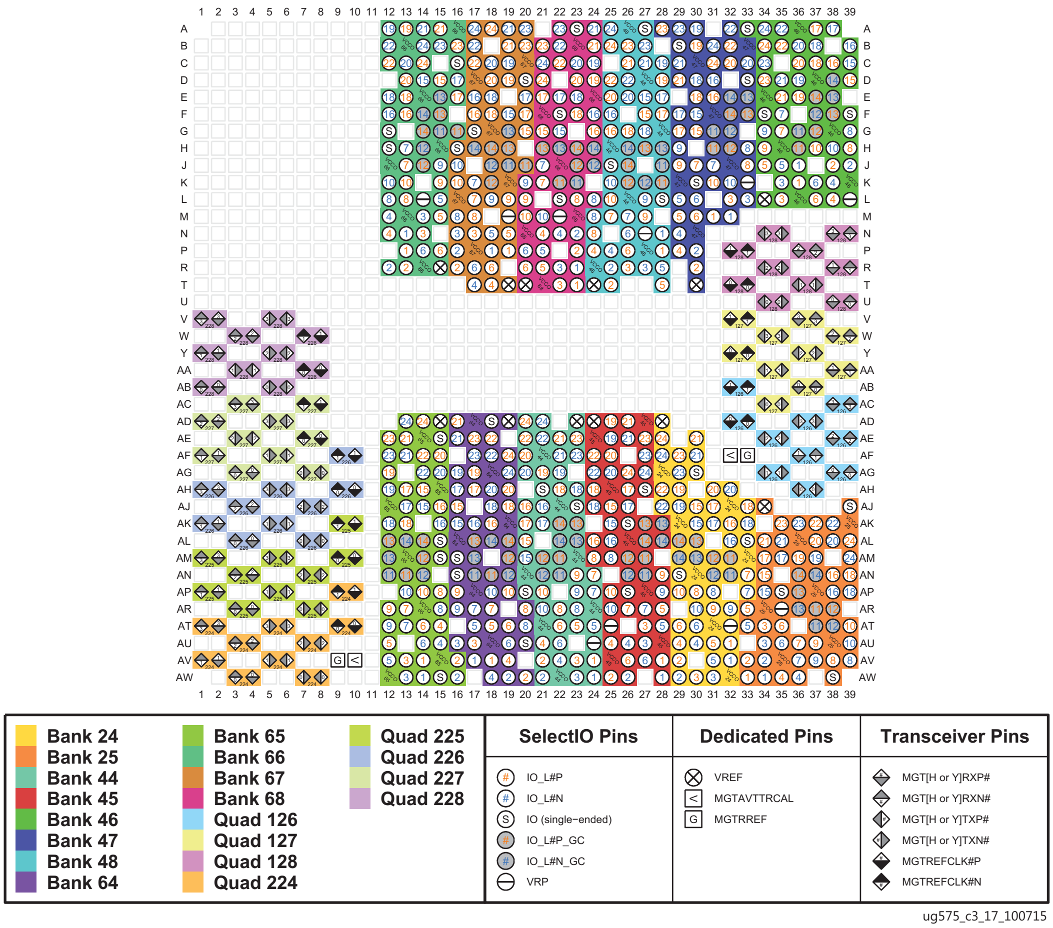


Figure 3-17: **FFVA1517 Package—XCKU060 I/O Bank Diagram**

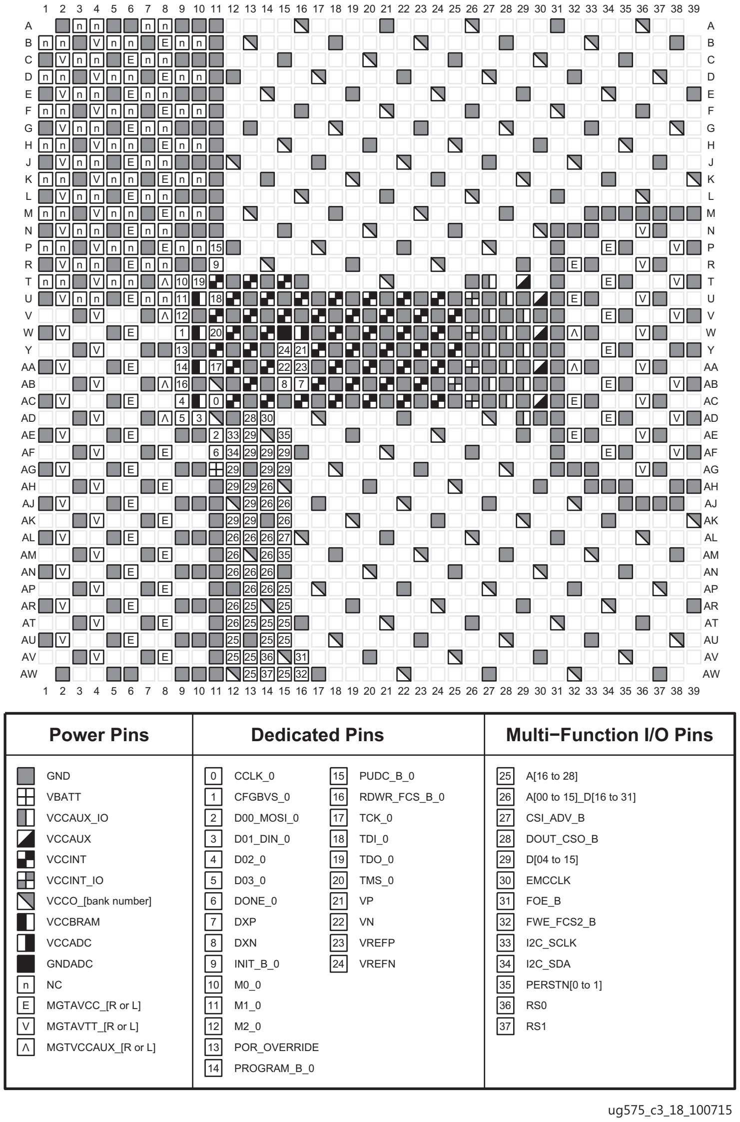


Figure 3-18: **FFVA1517 Package—XCKU060 Configuration/Power Diagram**

FLVA1517 (XCKU085 and XCKU115)

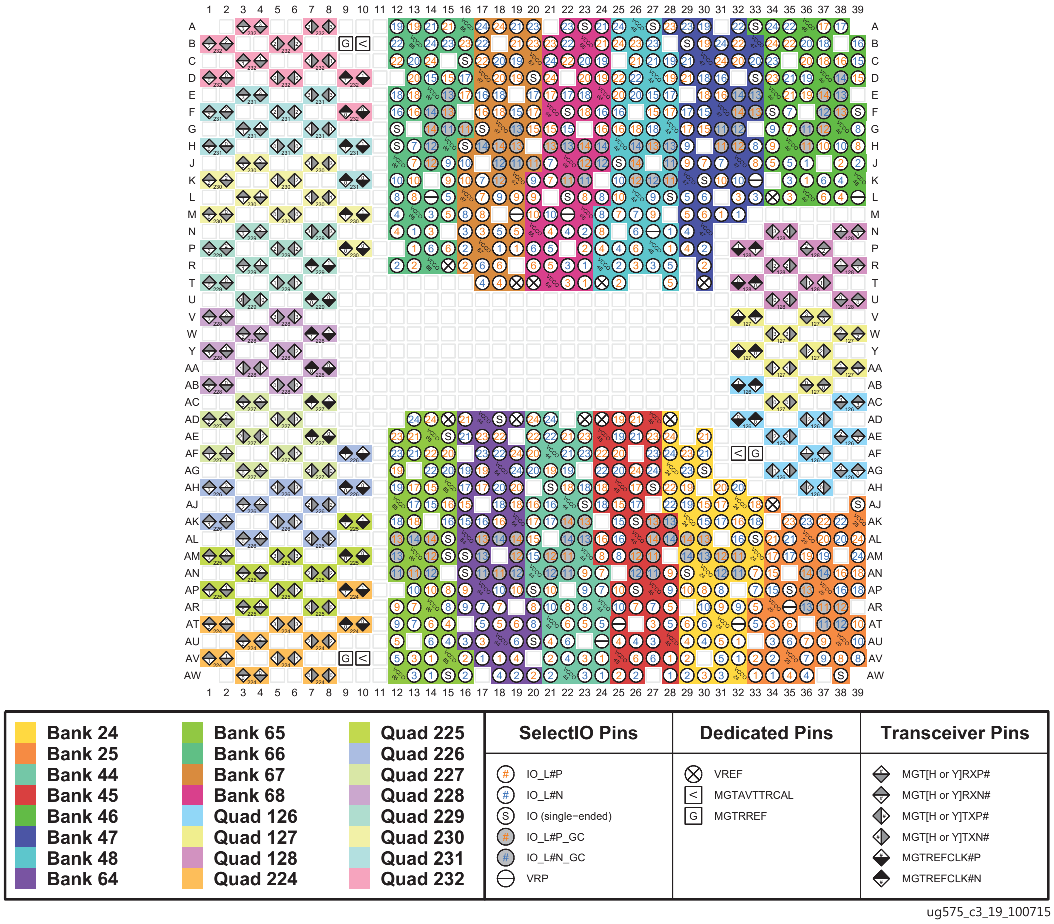


Figure 3-19: **FLVA1517 Package—XCKU085 and XCKU115 I/O Bank Diagram**

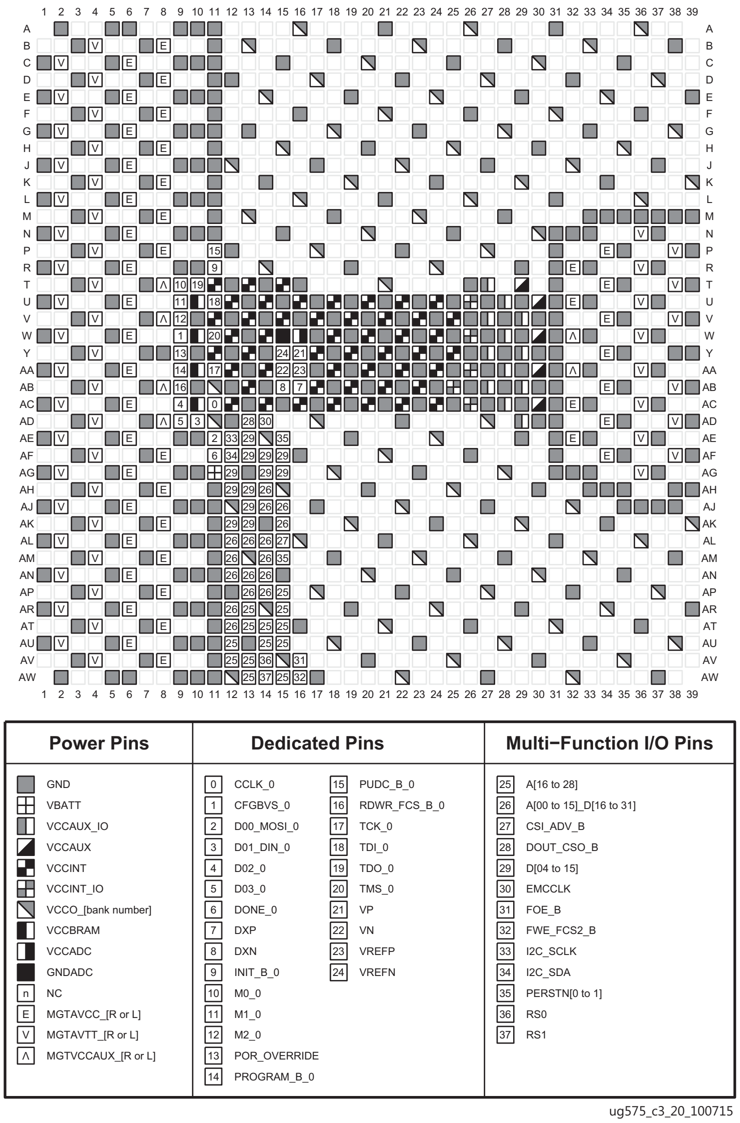


Figure 3-20: **FLVA1517 Package—XCKU085 and XCKU115 Configuration/Power Diagram**

FFVC1517 (XCKU095)

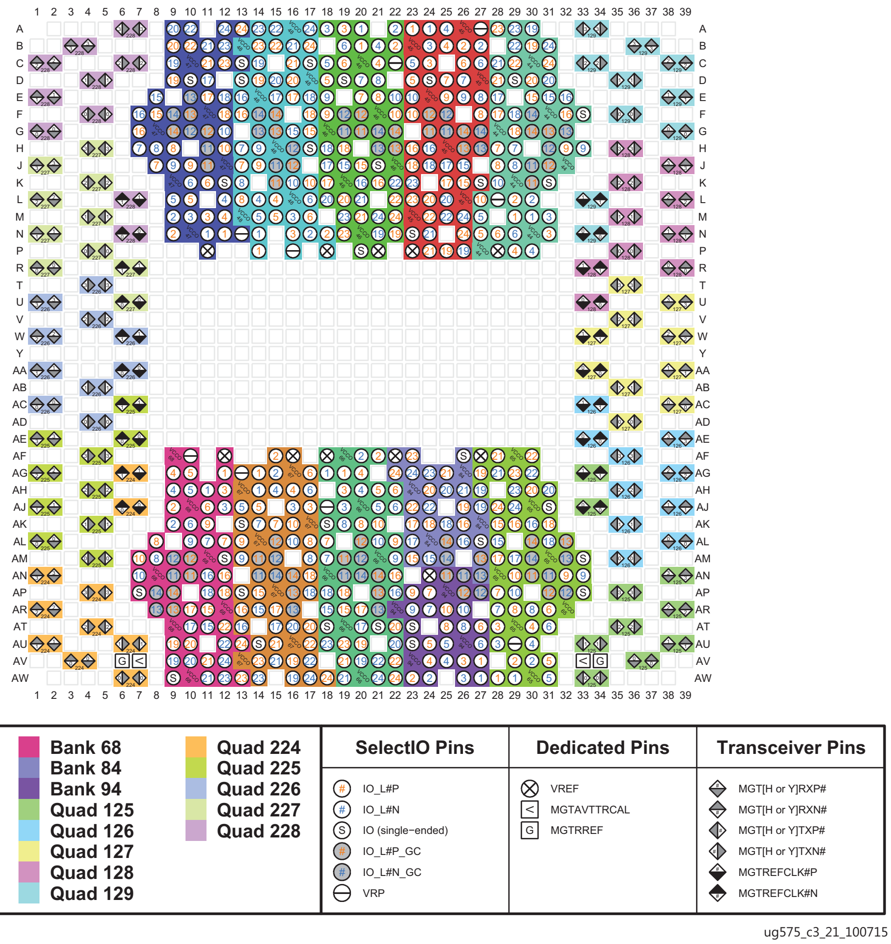


Figure 3-21: **FFVC1517 Package—XCKU095 I/O Bank Diagram**

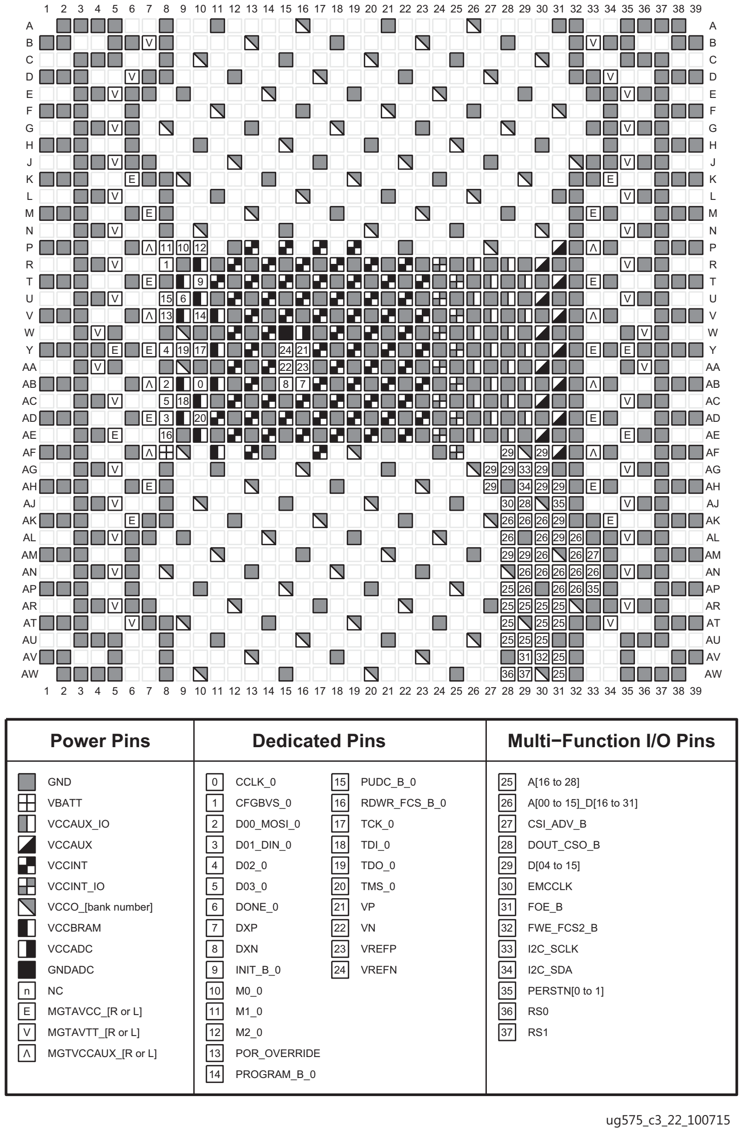


Figure 3-22: **FFVC1517 Package—XCKU095 Configuration/Power Diagram**

FLVD1517 (XCKU115) and RLD1517 (XQKU115)

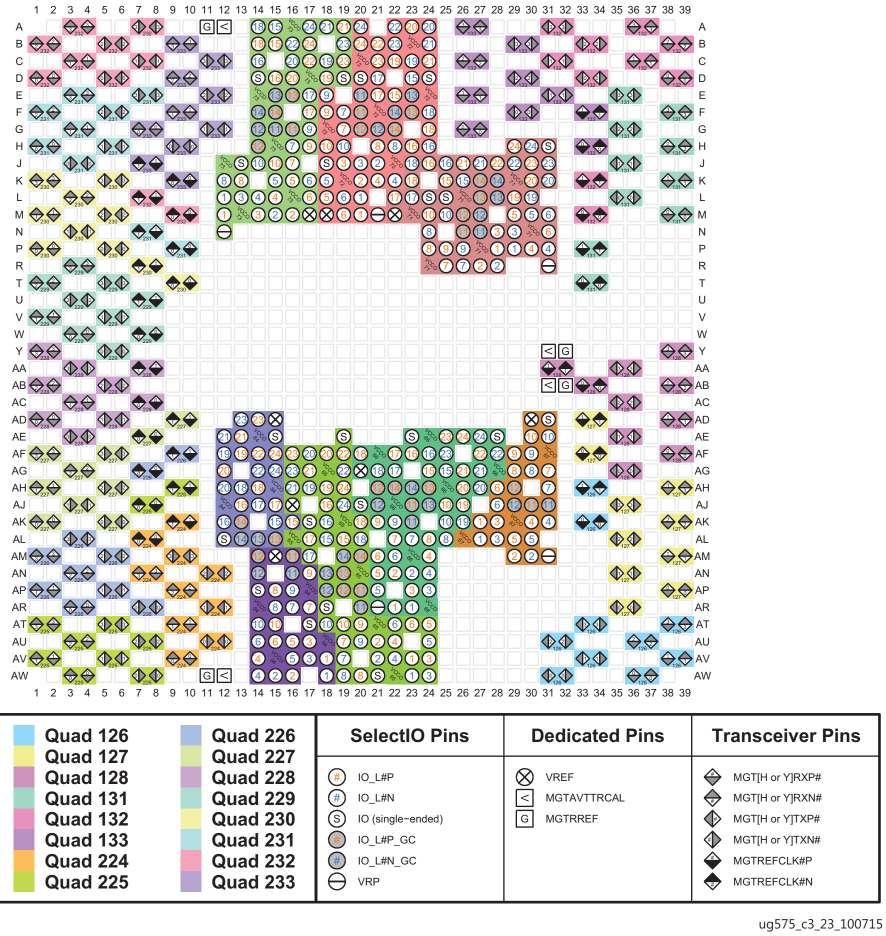


Figure 3-23: **FLVD1517 Package—XCKU115 and RLD1517 Package—XQKU115 I/O Bank Diagram**

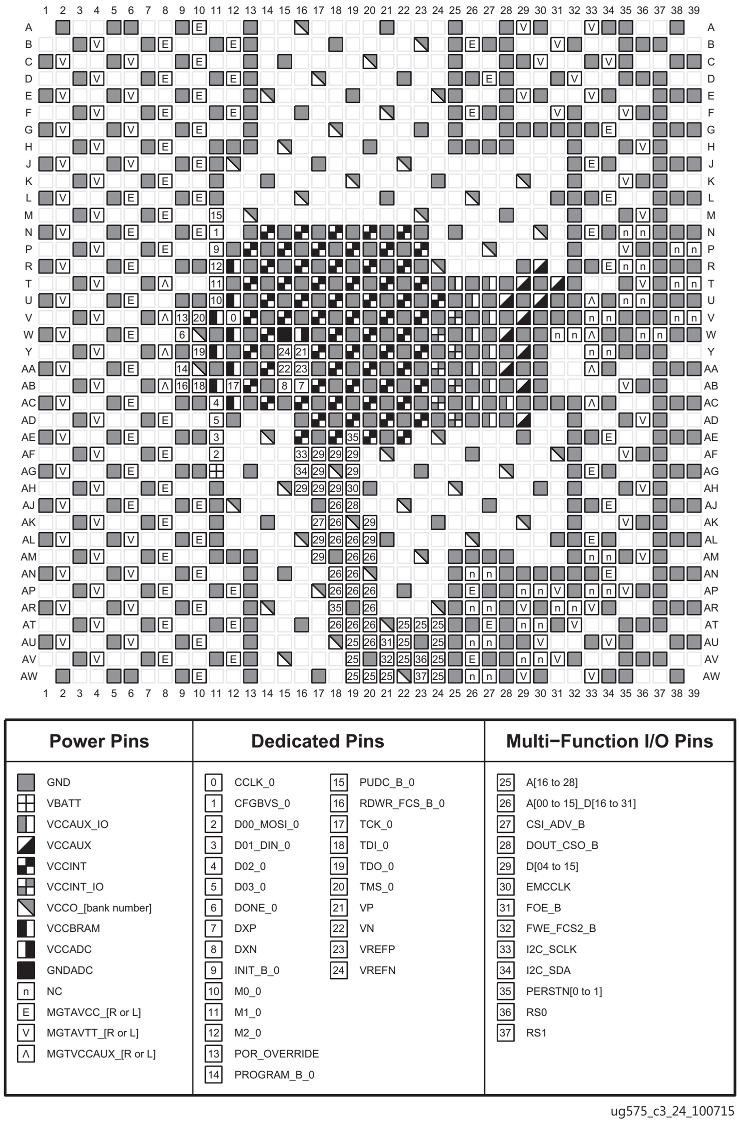


Figure 3-24: **FLVD1517 Package—XCKU115 and RLD1517 Package—XQKU115 Configuration/Power Diagram**

FFVB1760 (XCKU095)

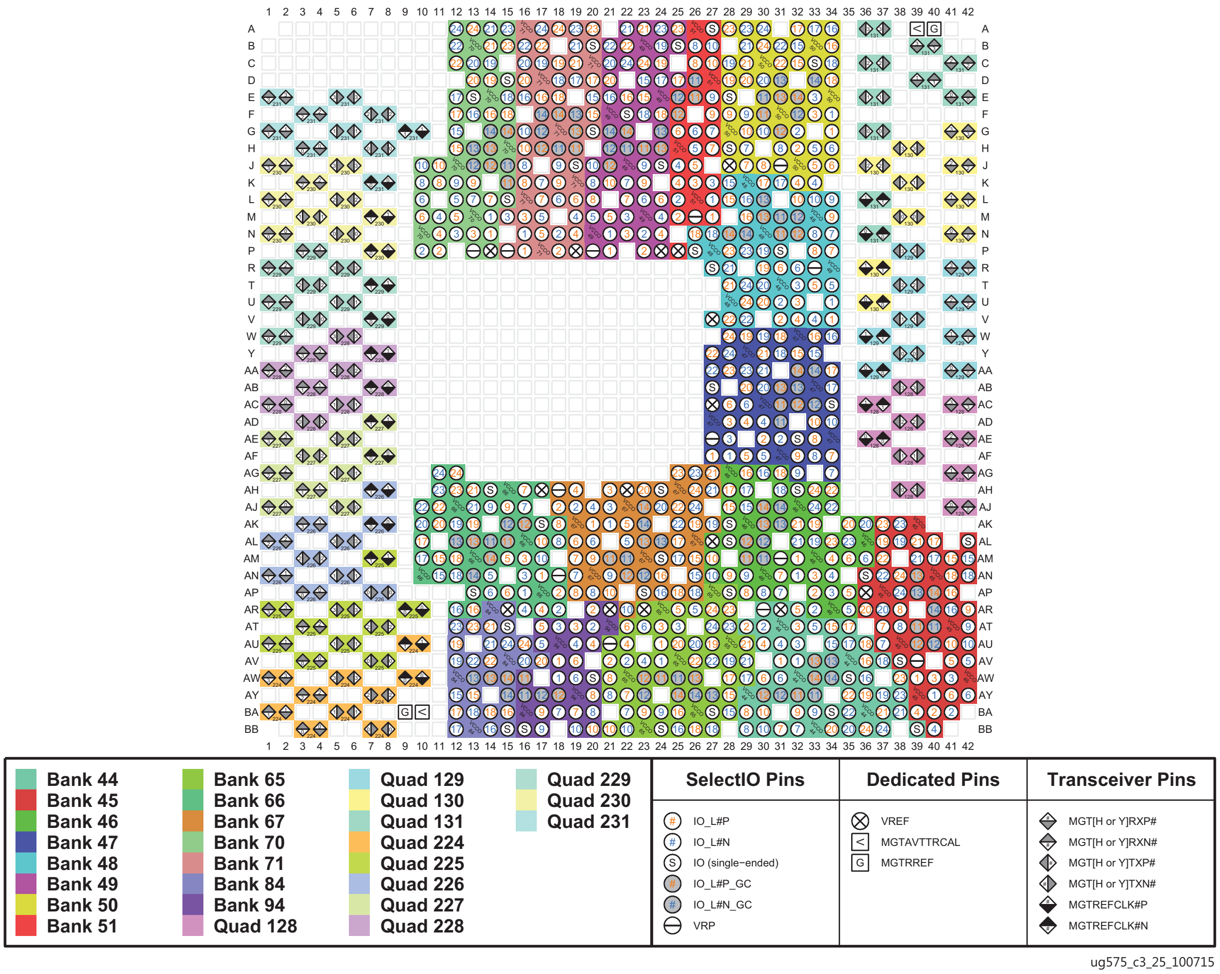


Figure 3-25: **FFVB1760 Package—XCKU095 I/O Bank Diagram**

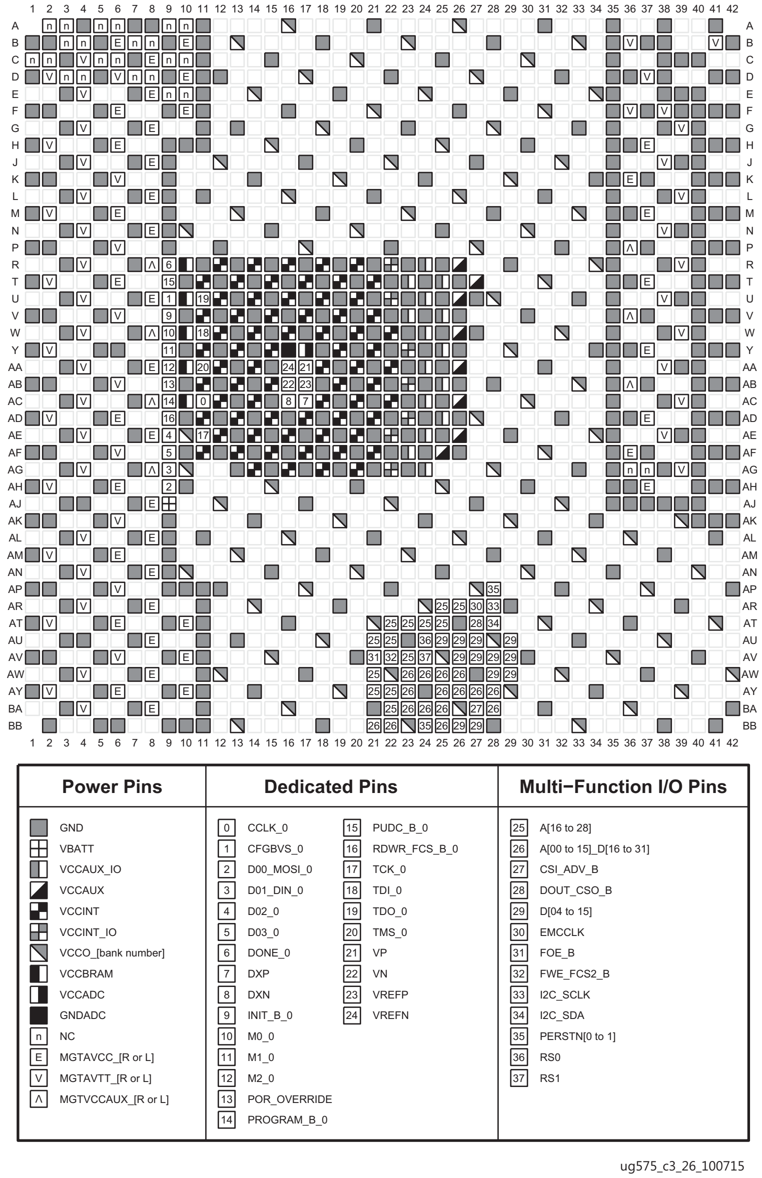


Figure 3-26: **FFVB1760 Package—XCKU095 Configuration/Power Diagram**

FLVB1760 (XCKU085)

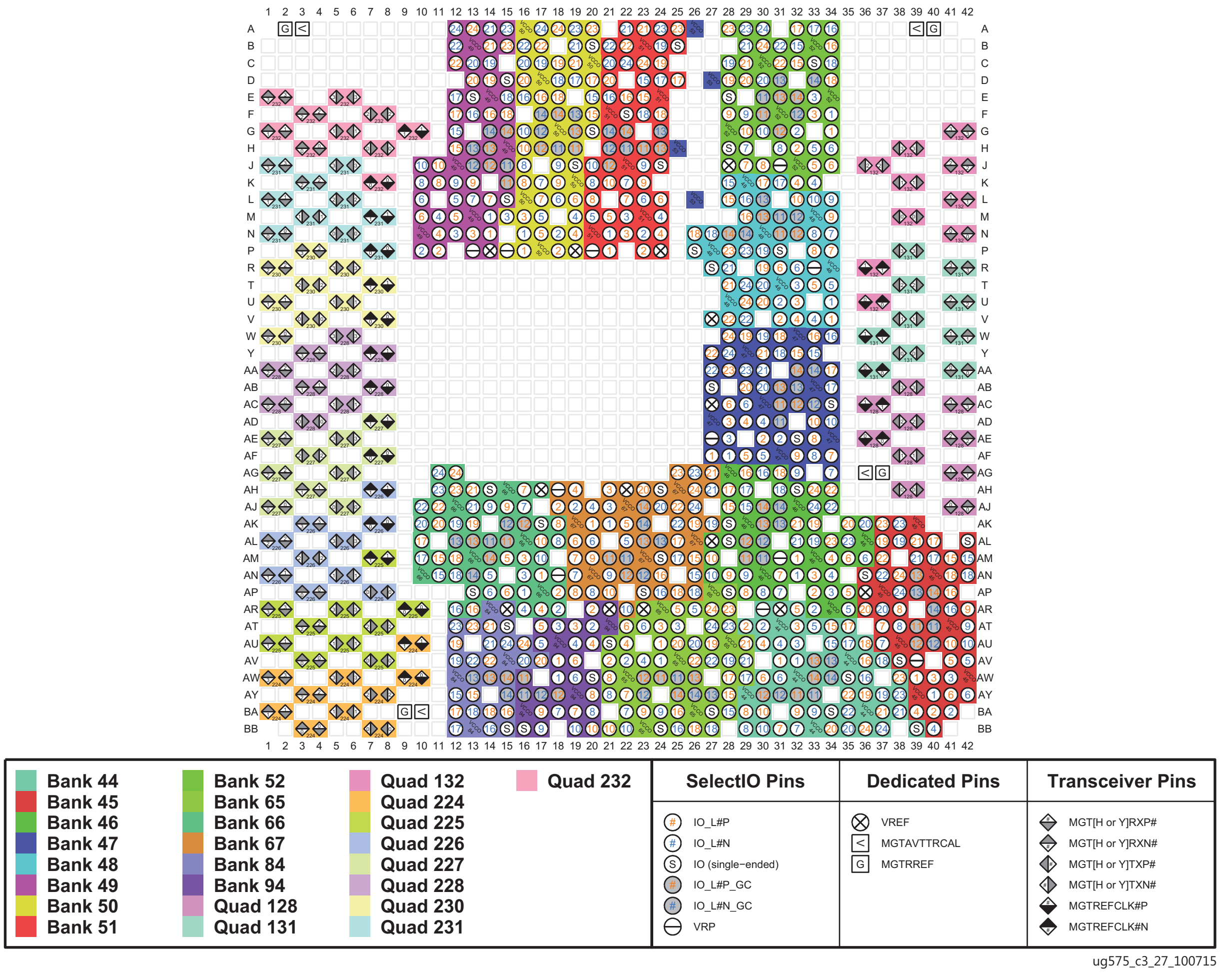


Figure 3-27: **FLVB1760 Package—XCKU085 I/O Bank Diagram**

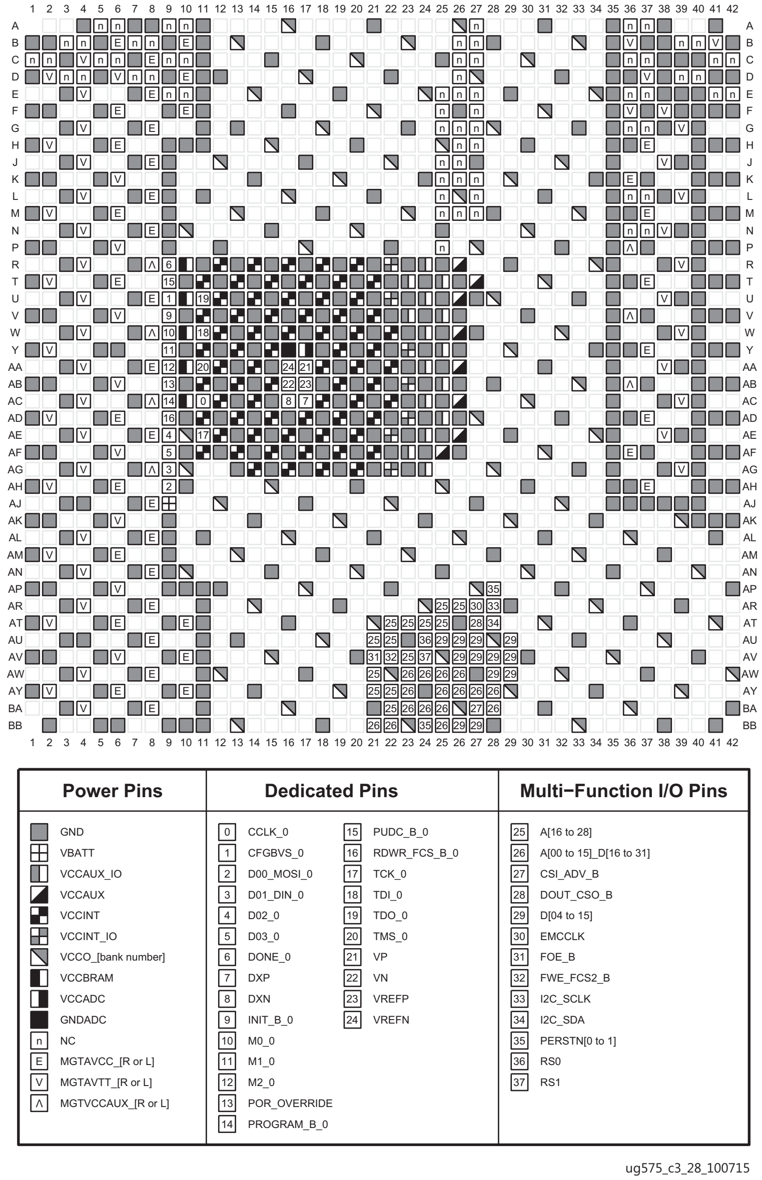


Figure 3-28: **FLVB1760 Package—XCKU085 Configuration/Power Diagram**

FLVB1760 (XCKU115)

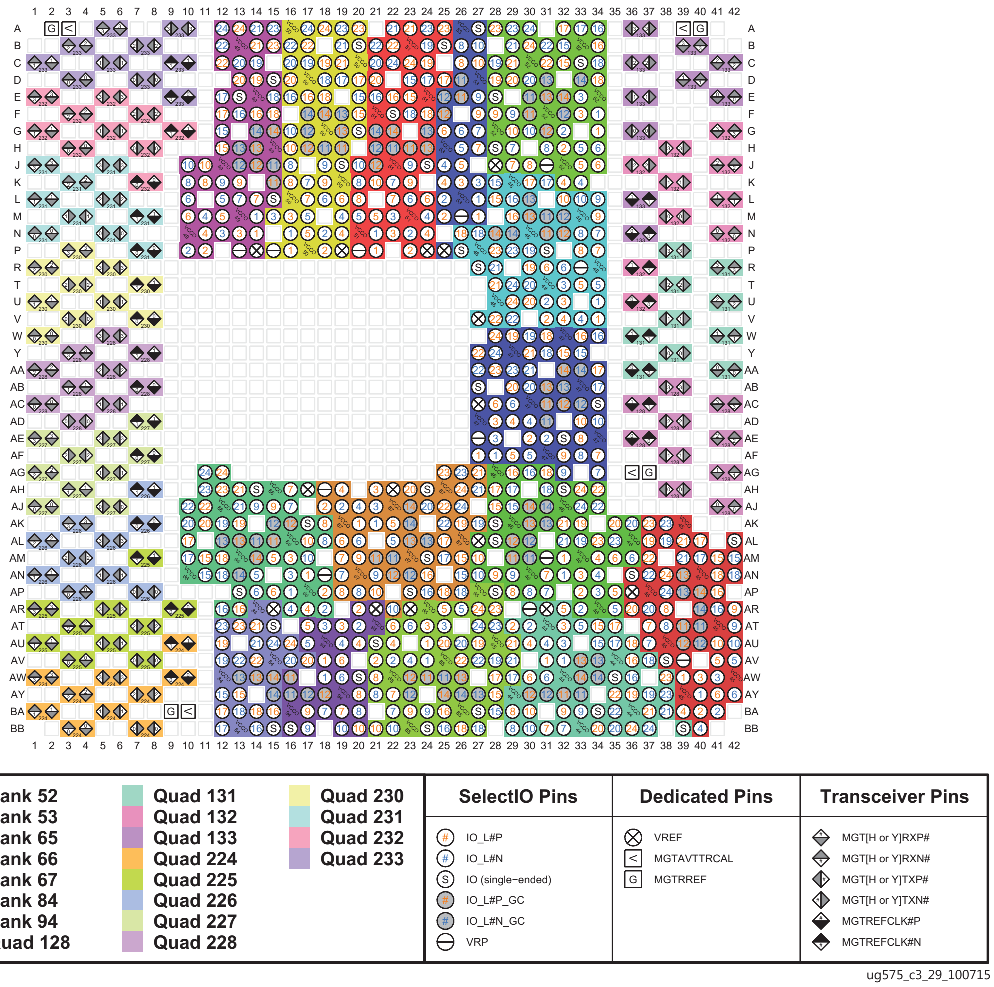
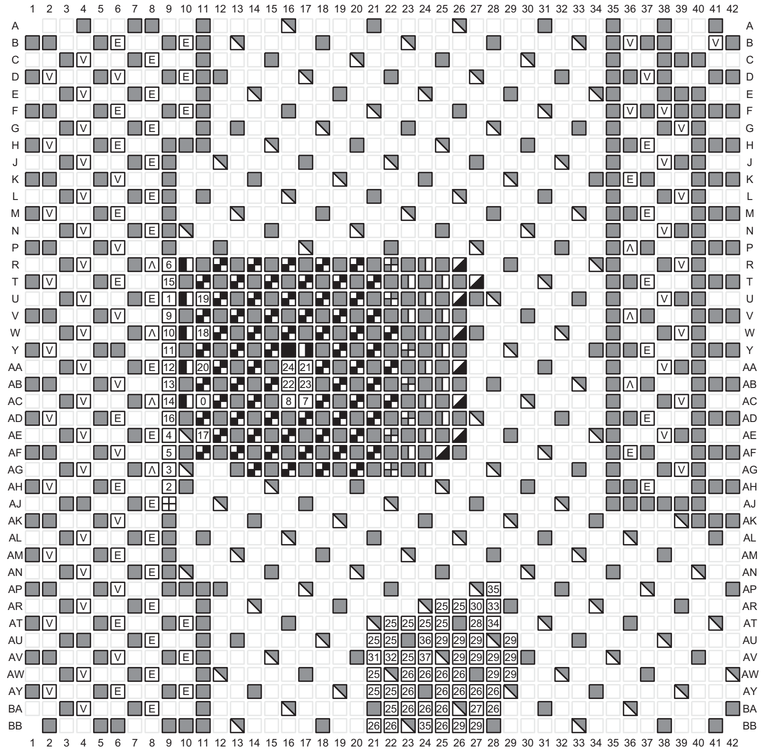


Figure 3-29: **FLVB1760 Package—XCKU115 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi–Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-30: **FLVB1760 Package—XCKU115 Configuration/Power Diagram**

FLVD1924 (XCKU115)

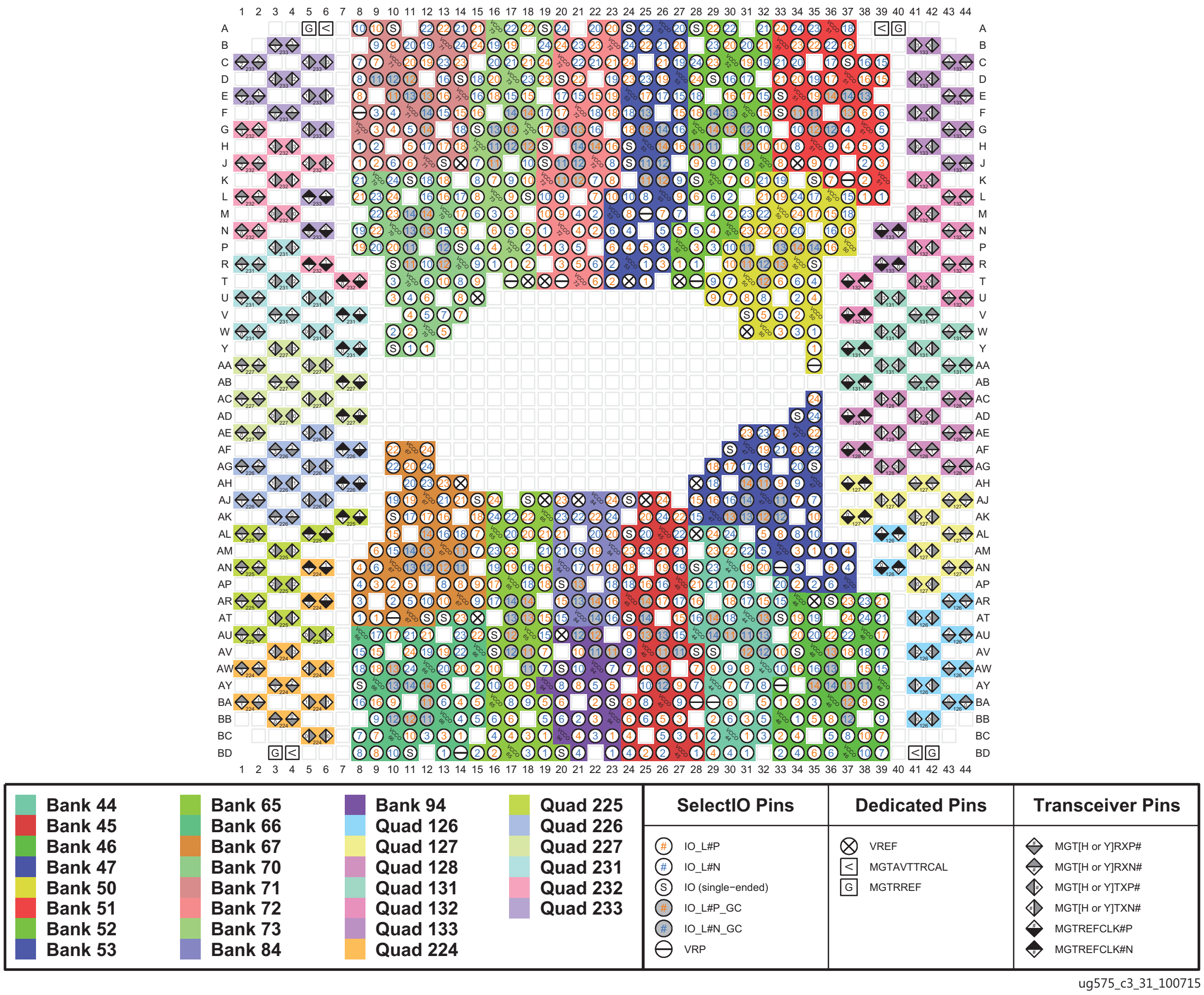
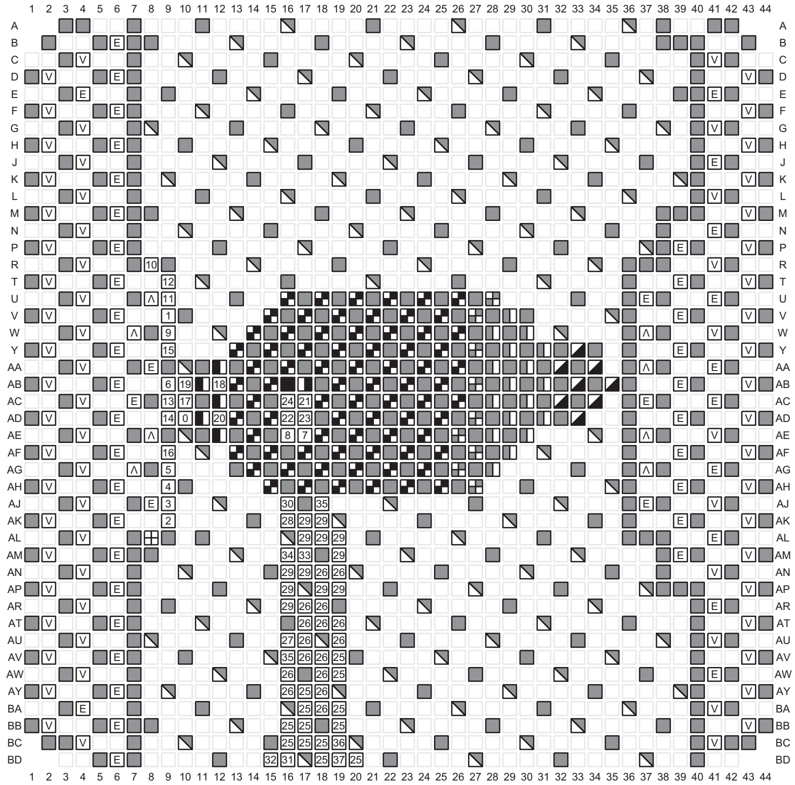


Figure 3-31: **FLVD1924 Package—XCKU115 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-32: **FLVD1924 Package—XCKU115 Configuration/Power Diagram**

FLVF1924 (XCKU085)

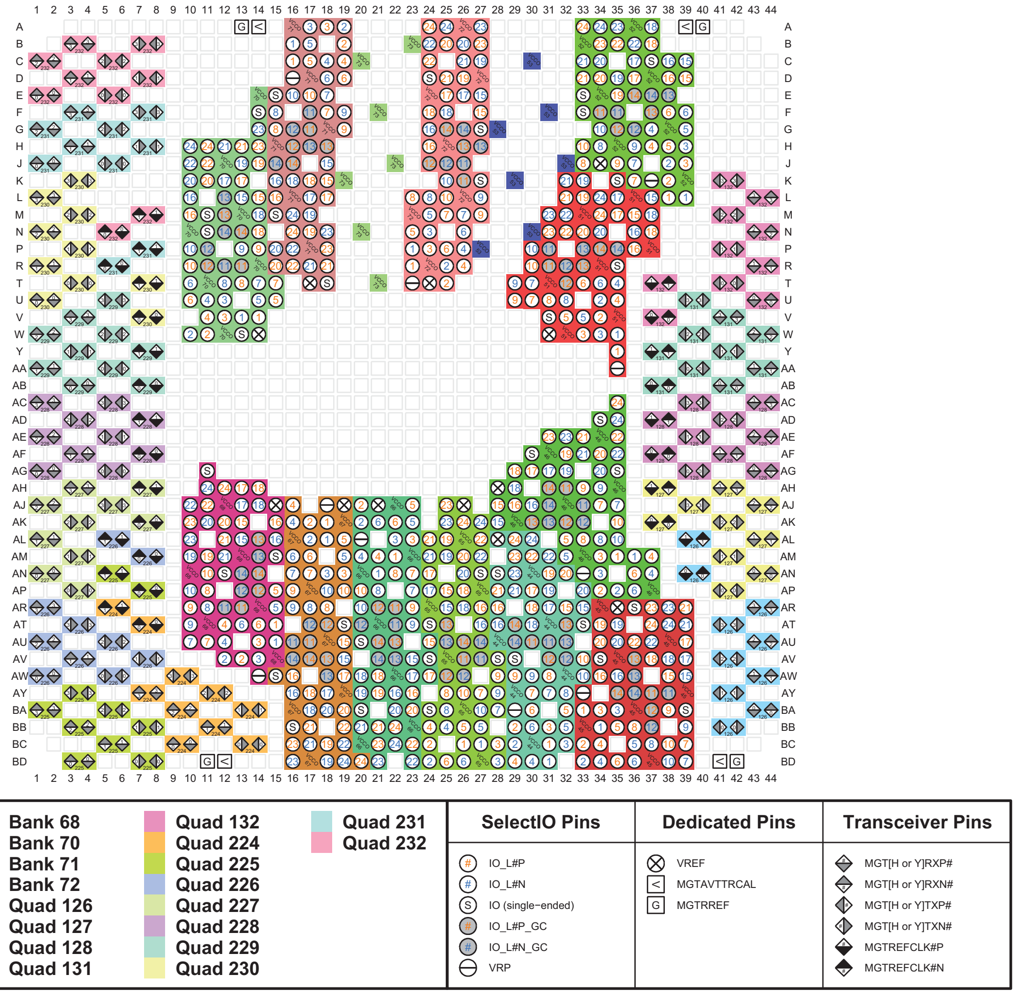

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Figure 3-33: **FLVF1924 Package—XCKU085 I/O Bank Diagram**

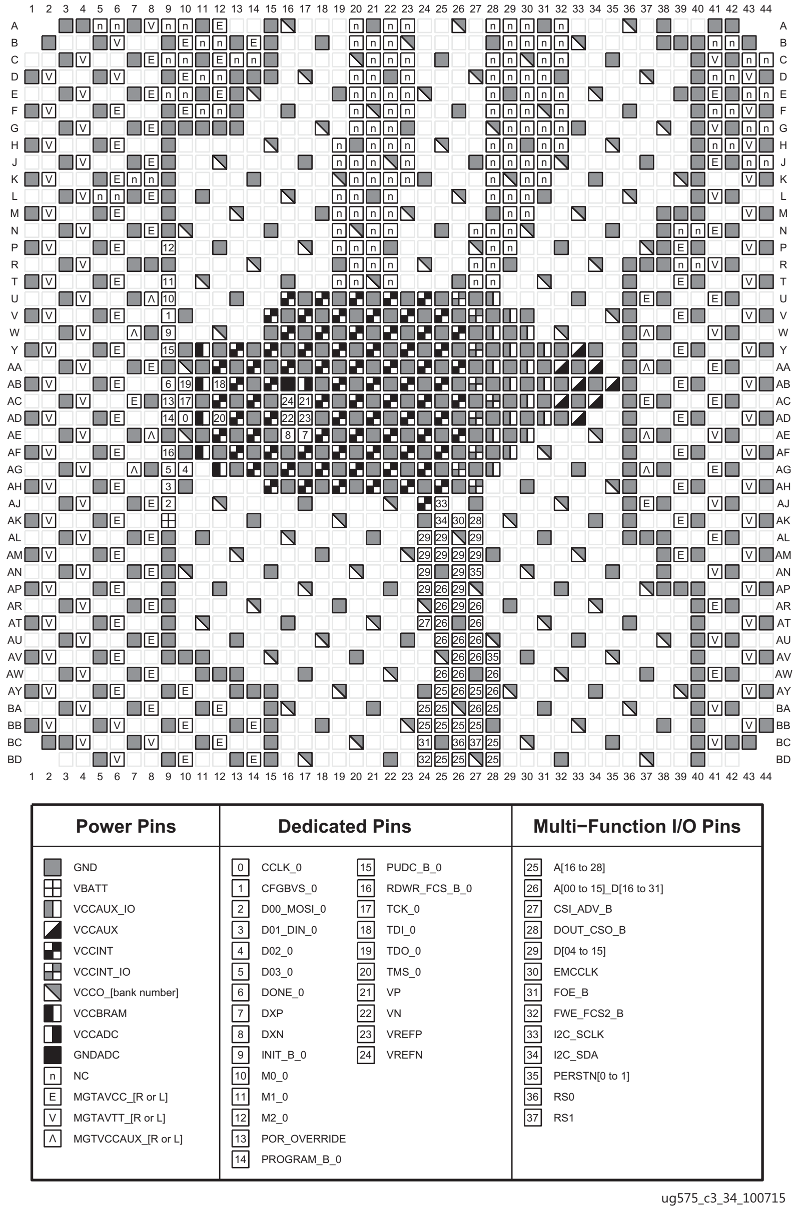


Figure 3-34: **FLVF1924 Package—XCKU085 Configuration/Power Diagram**

FLVF1924 (XCKU115) and RLF1924 (XQKU115)

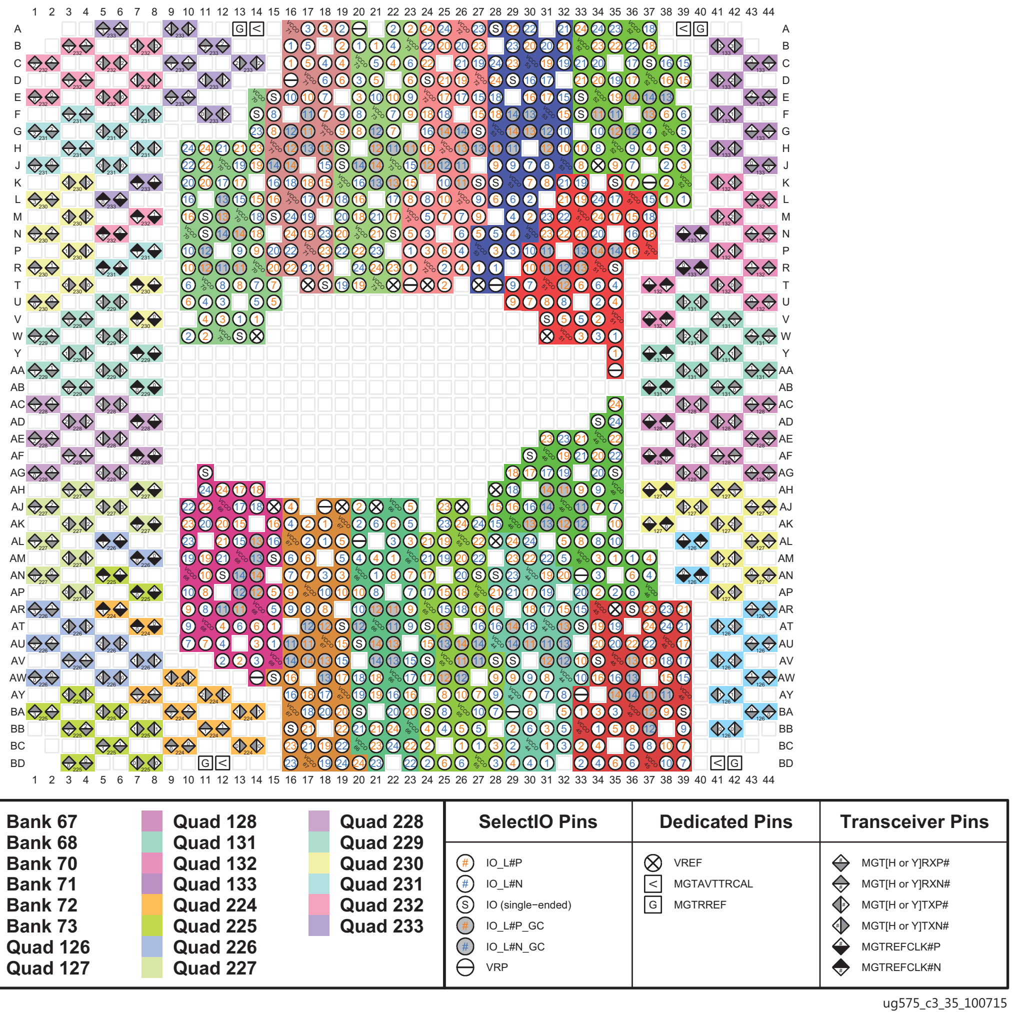


Figure 3-35: **FLVF1924 Package—XCKU115 and RLF1924 Package—XQKU115 I/O Bank Diagram**

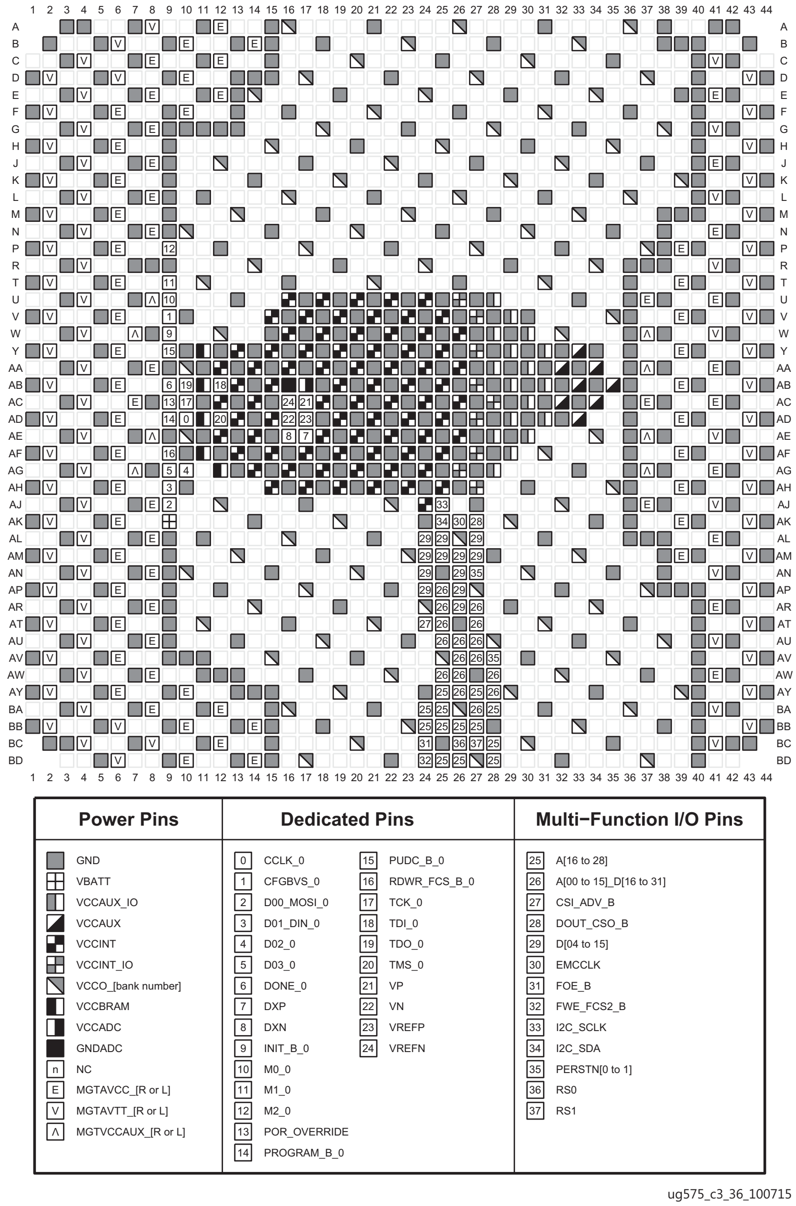


Figure 3-36: **FLVF1924 Package—XCKU115 and RLF1924 Package—XQKU115 Configuration/Power Diagram**

FLVA2104 (XCKU115)

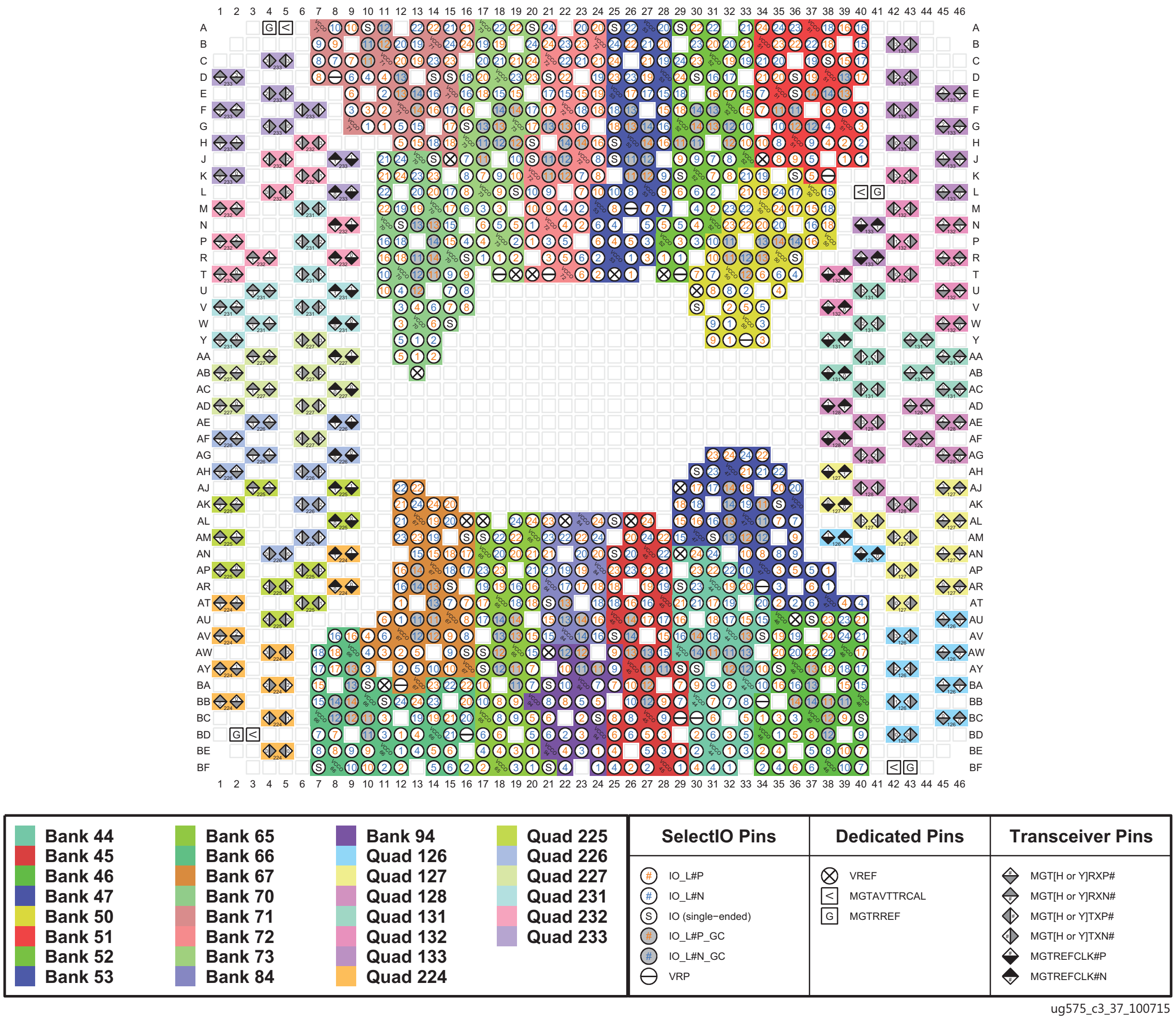


Figure 3-37: **FLVA2104 Package—XCKU115 I/O Bank Diagram**

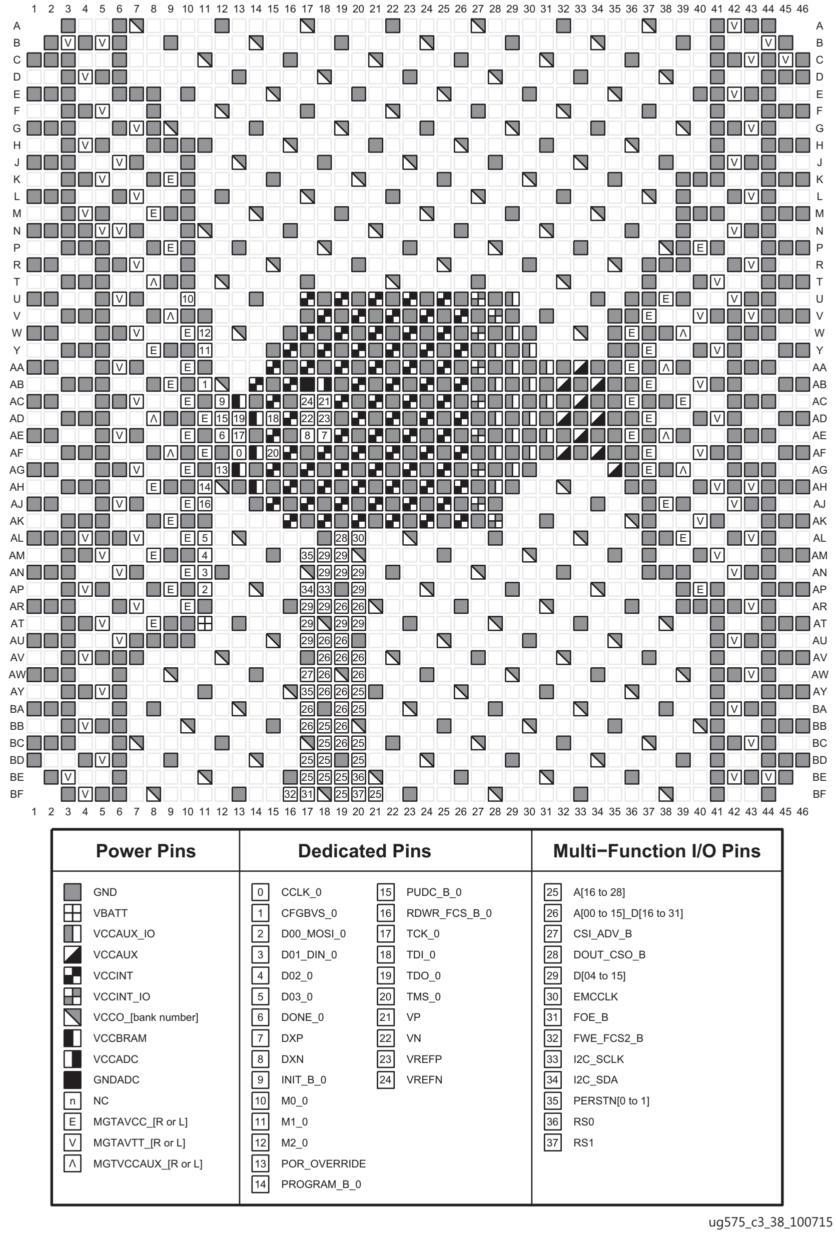


Figure 3-38: **FLVA2104 Package—XCKU115 Configuration/Power Diagram**

FFVB2104 (XCKU095)

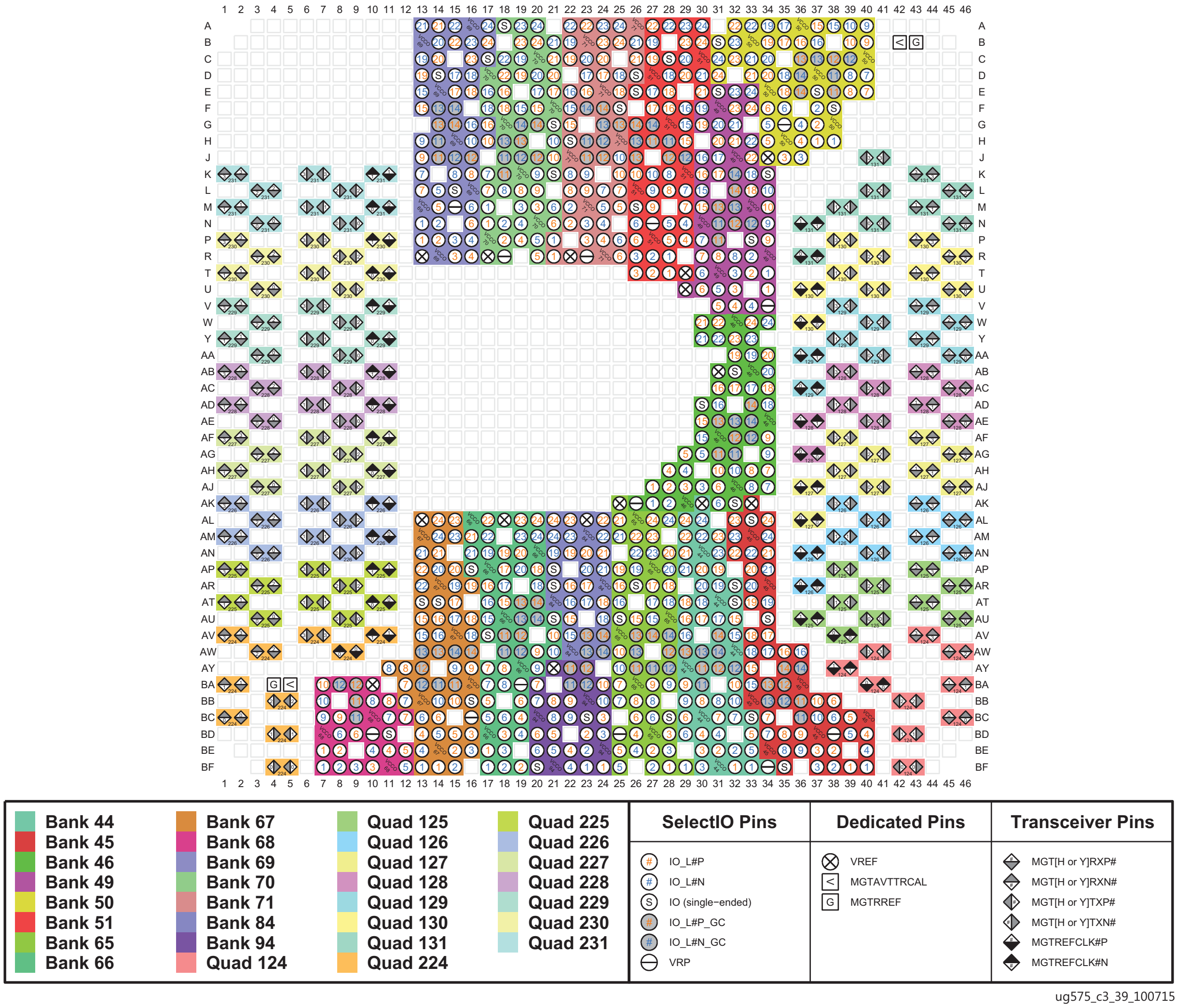


Figure 3-39: **FFVB2104 Package—XCKU095 I/O Bank Diagram**

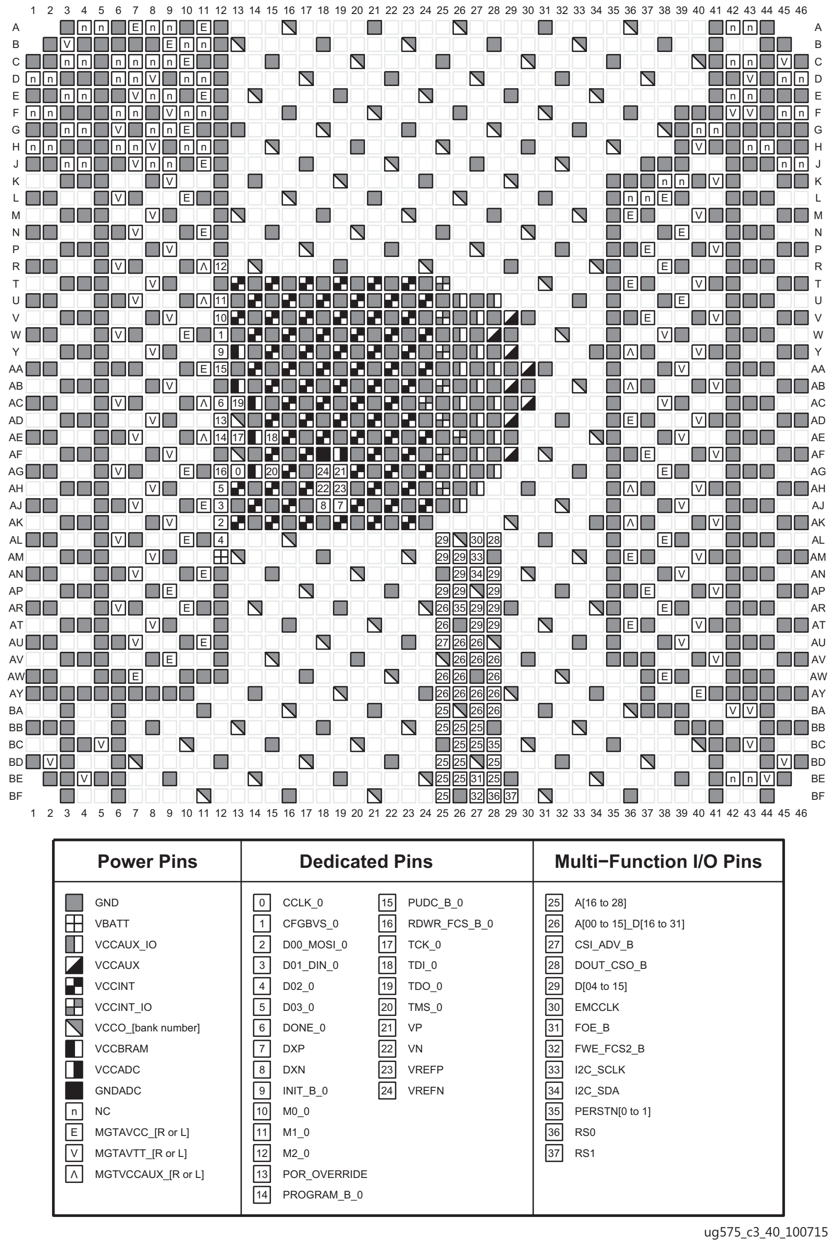


Figure 3-40: **FFVB2104 Package—XCKU095 Configuration/Power Diagram**

FLVB2104 (XCKU115)

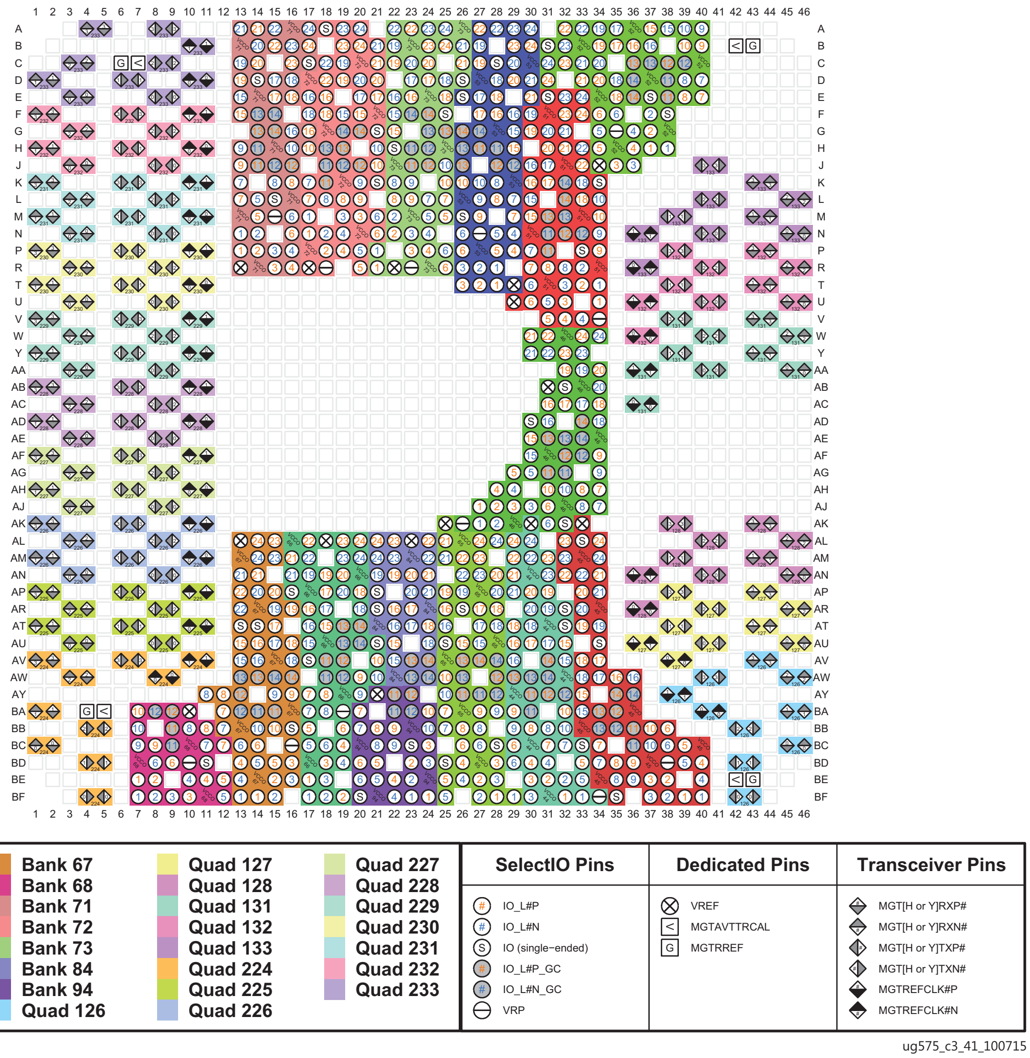


Figure 3-41: **FLVB2104 Package—XCKU115 I/O Bank Diagram**

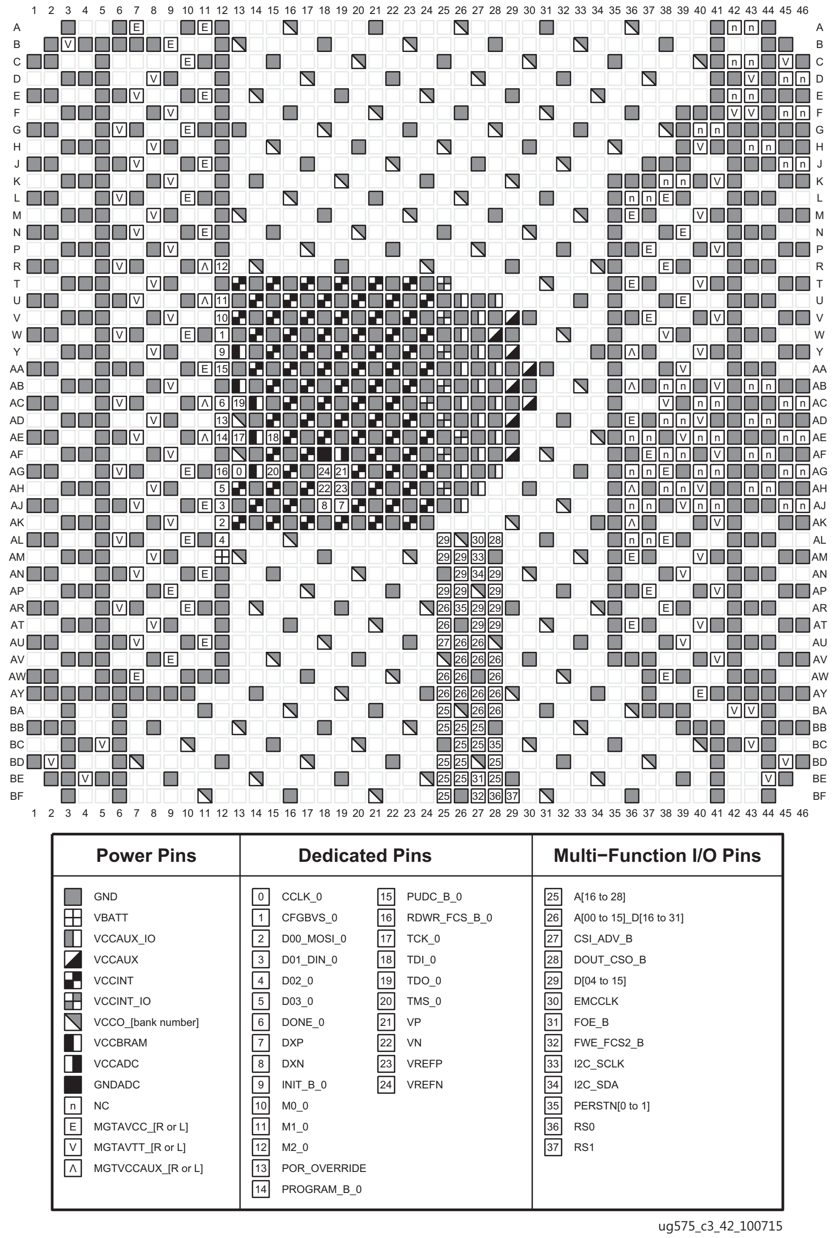
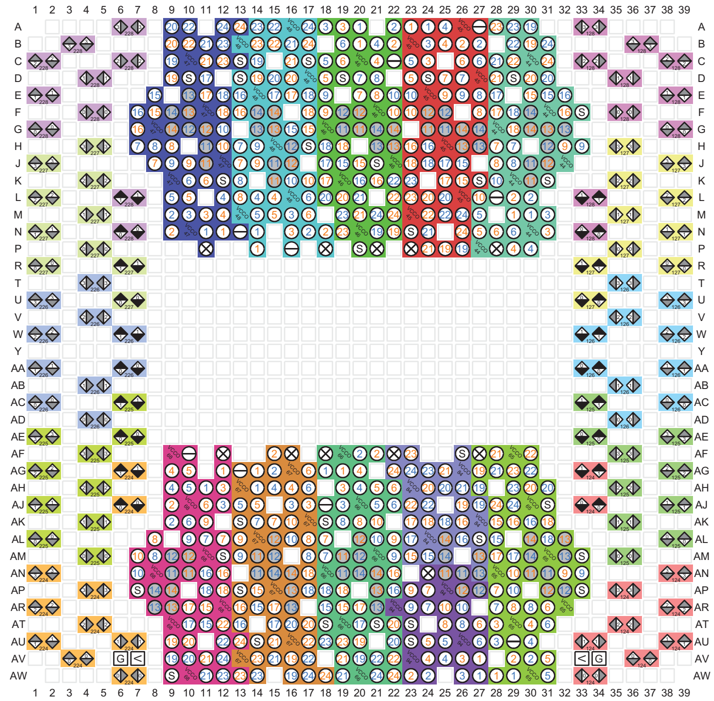


Figure 3-42: **FLVB2104 Package—XCKU115 Configuration/Power Diagram**

FFVC1517 (XCVU065)



Bank 44	Bank 68	Quad 224
Bank 45	Bank 84	Quad 225
Bank 46	Bank 94	Quad 226
Bank 47	Quad 124	Quad 227
Bank 48	Quad 125	Quad 228
Bank 65	Quad 126	
Bank 66	Quad 127	
Bank 67	Quad 128	

SelectIO Pins	Dedicated Pins	Transceiver Pins
IO_L#P	VREF	MGT[H or Y]RXP#
IO_L#N	MGTAVTTRCAL	MGT[H or Y]RXN#
IO (single-ended)	MGTRREF	MGT[H or Y]TXP#
IO_L#P_GC		MGT[H or Y]TXN#
IO_L#N_GC		MGTREFCLK#P
VRP		MGTREFCLK#N

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Figure 3-43: **FFVC1517 Package—XCVU065 I/O Bank Diagram**

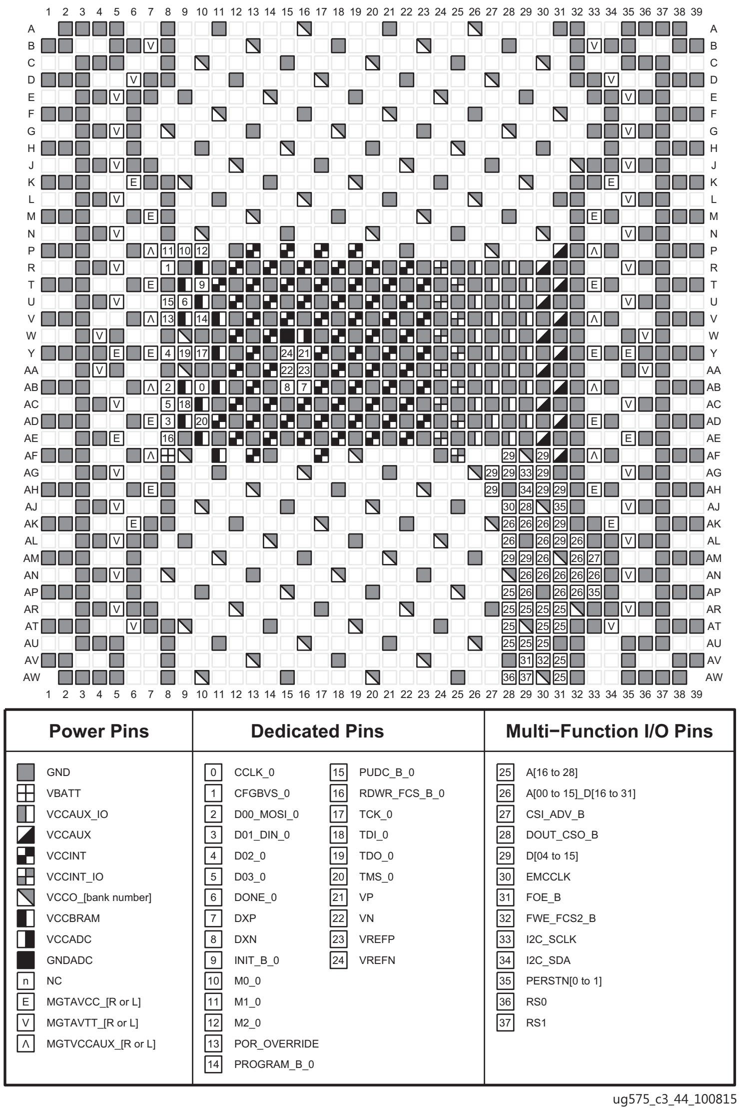

Figure 3-44: **FFVC1517 Package—XCVU065 Configuration/Power Diagram**

FFVC1517 (XCVU080 and XCVU095)

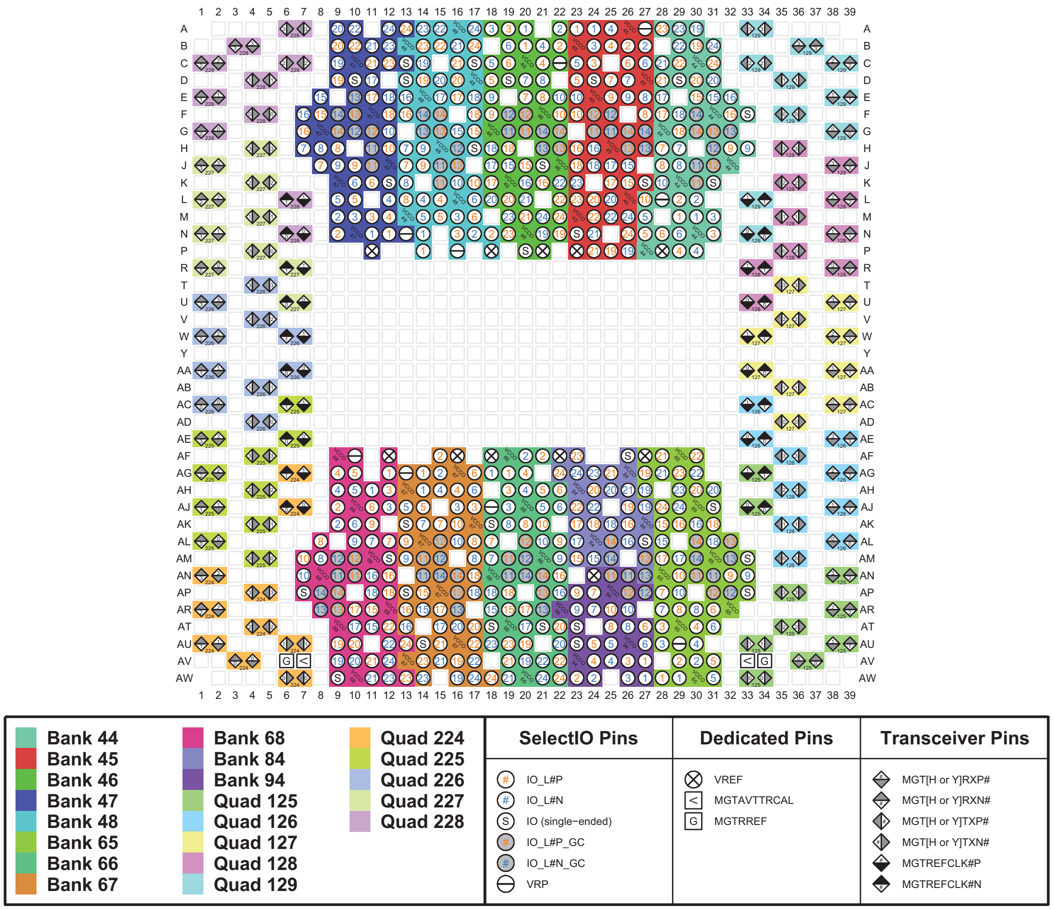

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Figure 3-45: **FFVC1517 Package—XCVU080 and XCVU095 I/O Bank Diagram**

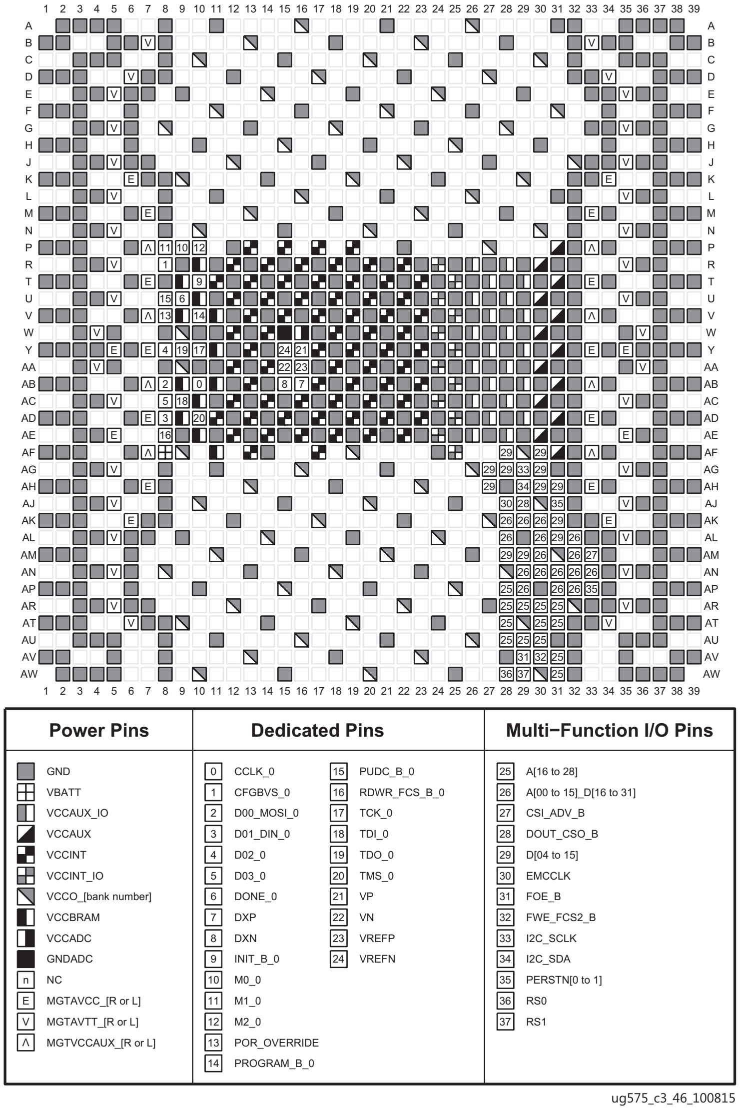

Figure 3-46: **FFVC1517 Package—XCVU080 and XCVU095 Configuration/Power Diagram**

FFVD1517 (XCVU080 and XCVU095)

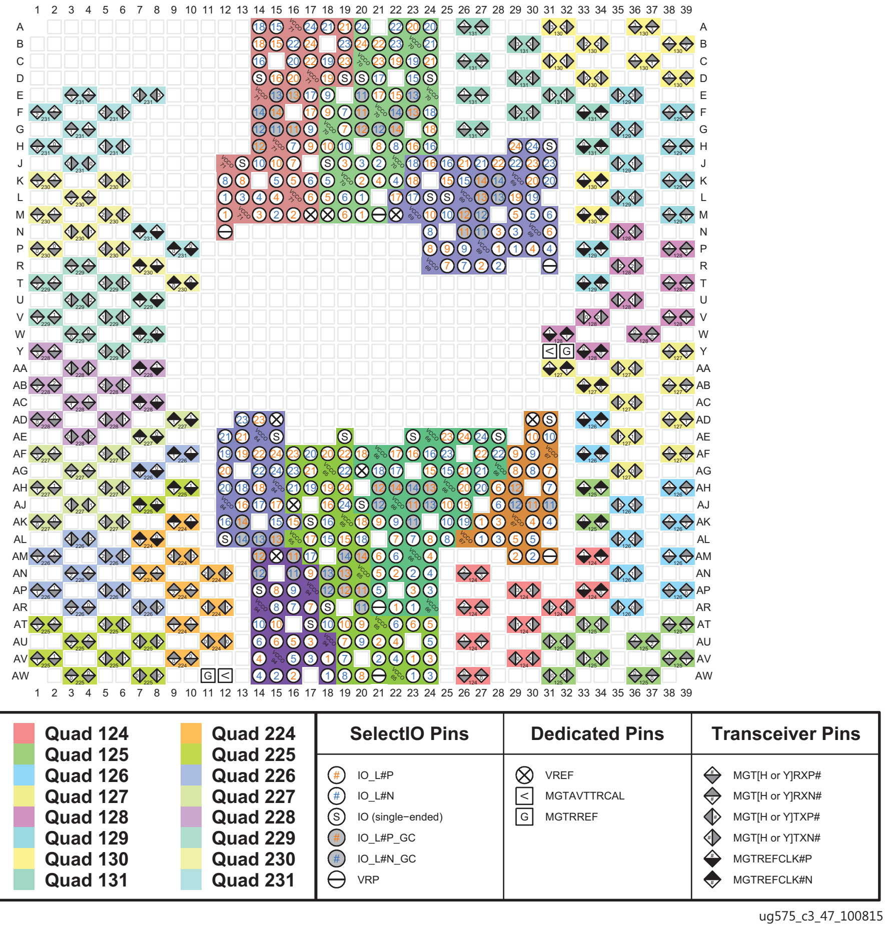

Figure 3-47: **FFVD1517 Package—XCVU080 and XCVU095 I/O Bank Diagram**

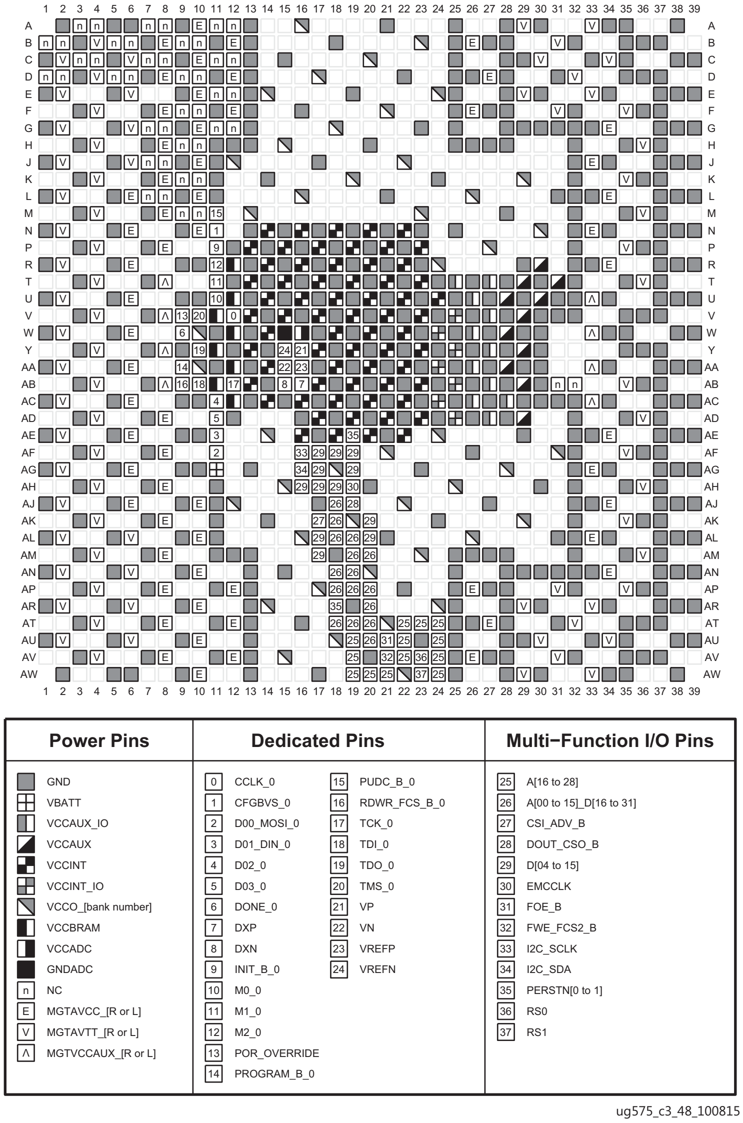

Figure 3-48: **FFVD1517 Package—XCVU080 and XCVU095 Configuration/Power Diagram**

FLVD1517 (XCVU125)

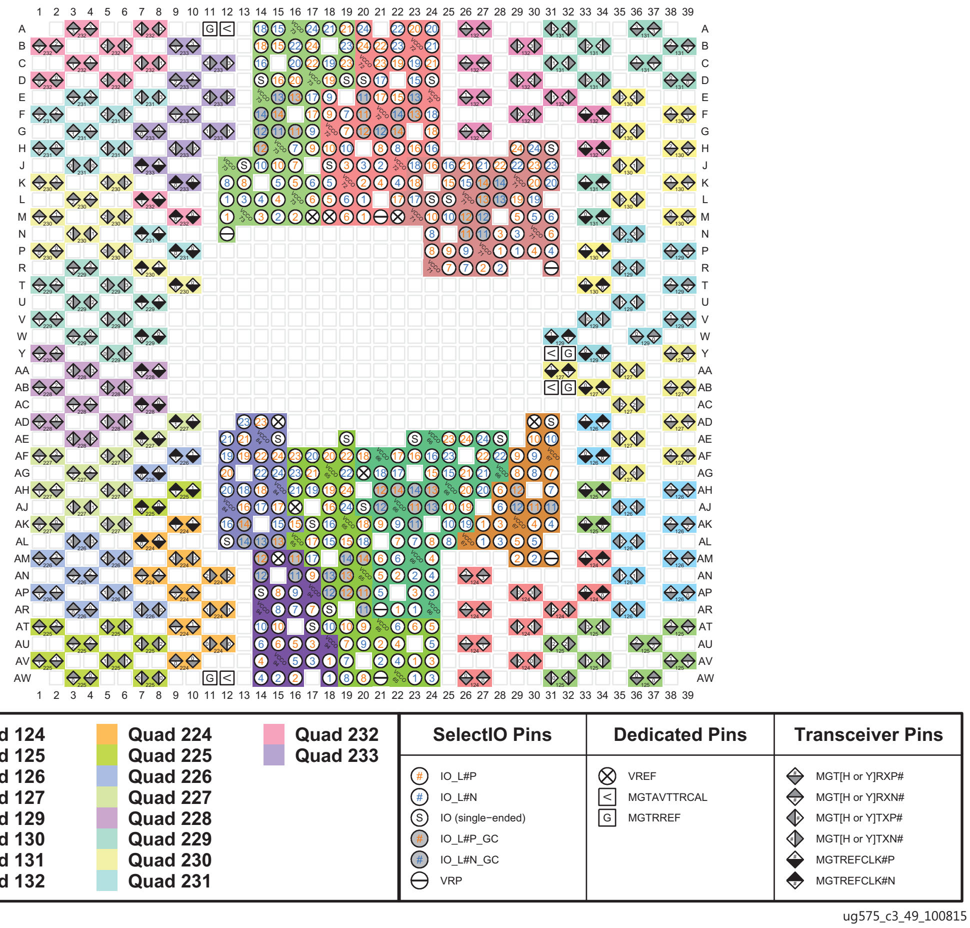

Figure 3-49: **FLVD1517 Package—XCVU125 I/O Bank Diagram**

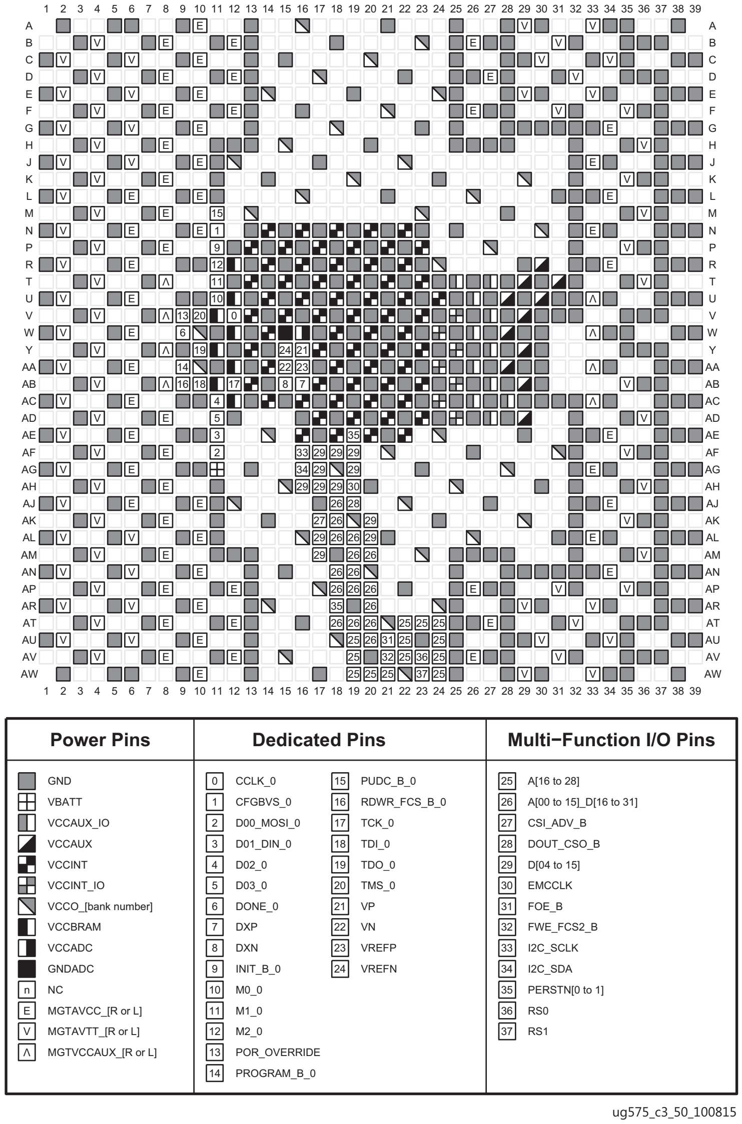

Figure 3-50: **FLVD1517 Package—XCVU125 Configuration/Power Diagram**

FFVB1760 (XCVU080 and XCVU095)

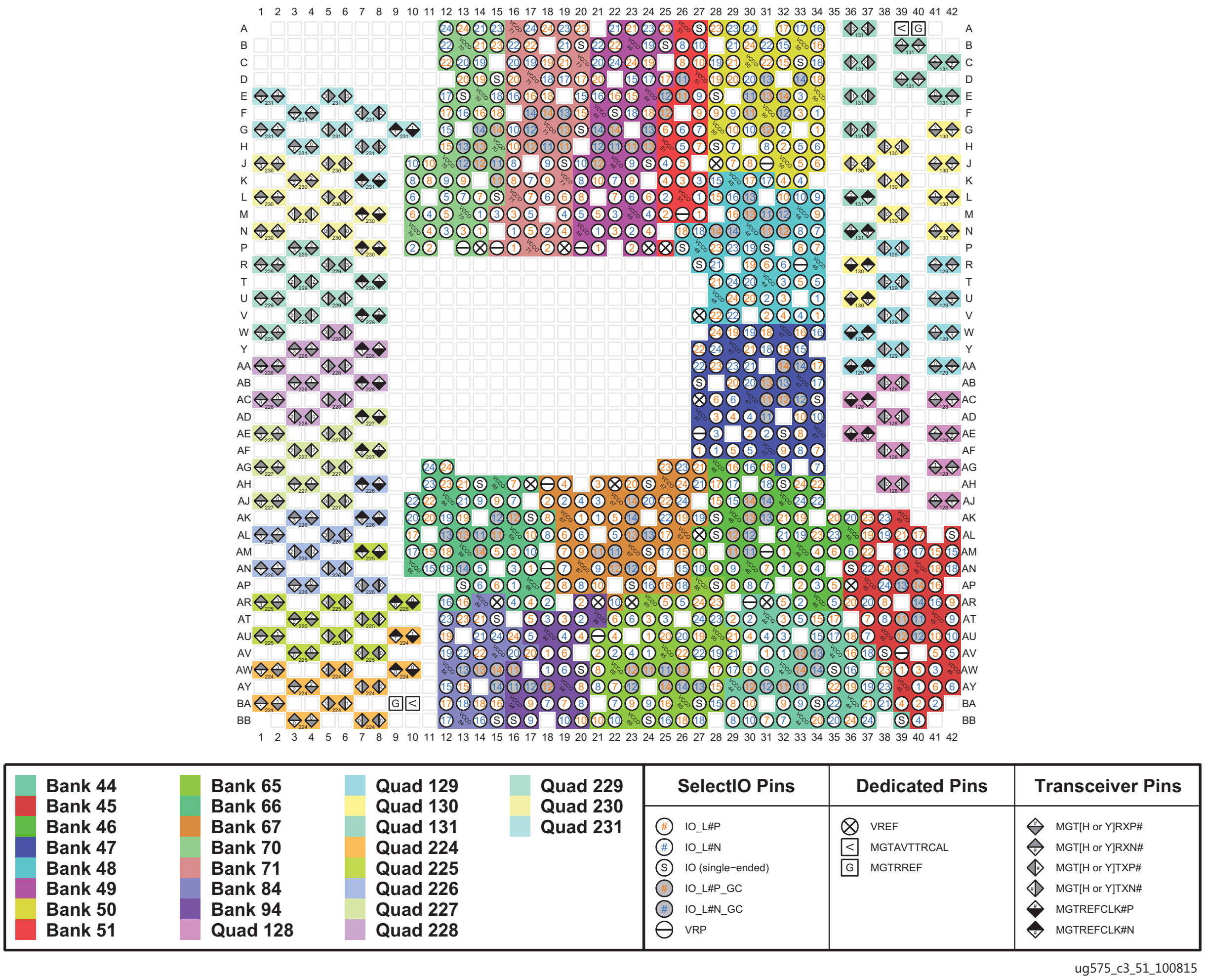

Figure 3-51: **FFVB1760 Package—XCVU080 and XCVU095 I/O Bank Diagram**

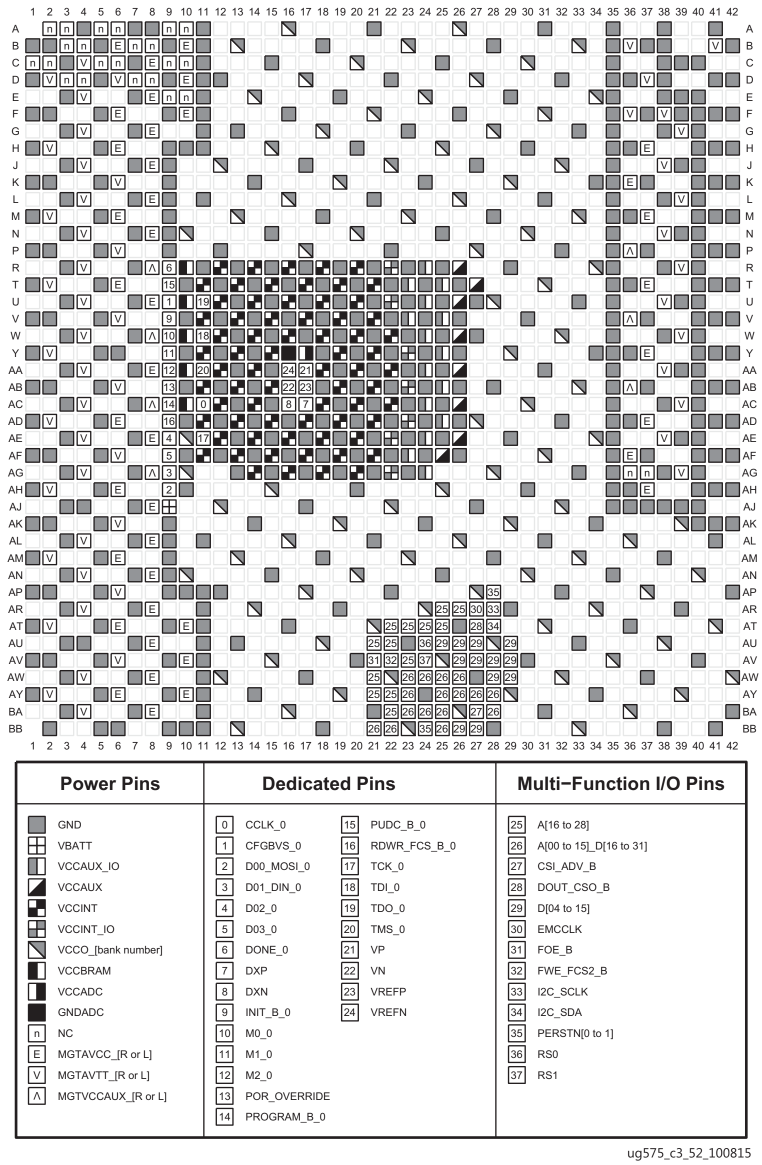

Figure 3-52: **FFVB1760 Package—XCVU080 and XCVU095 Configuration/Power Diagram**

FLVB1760 (XCVU125)

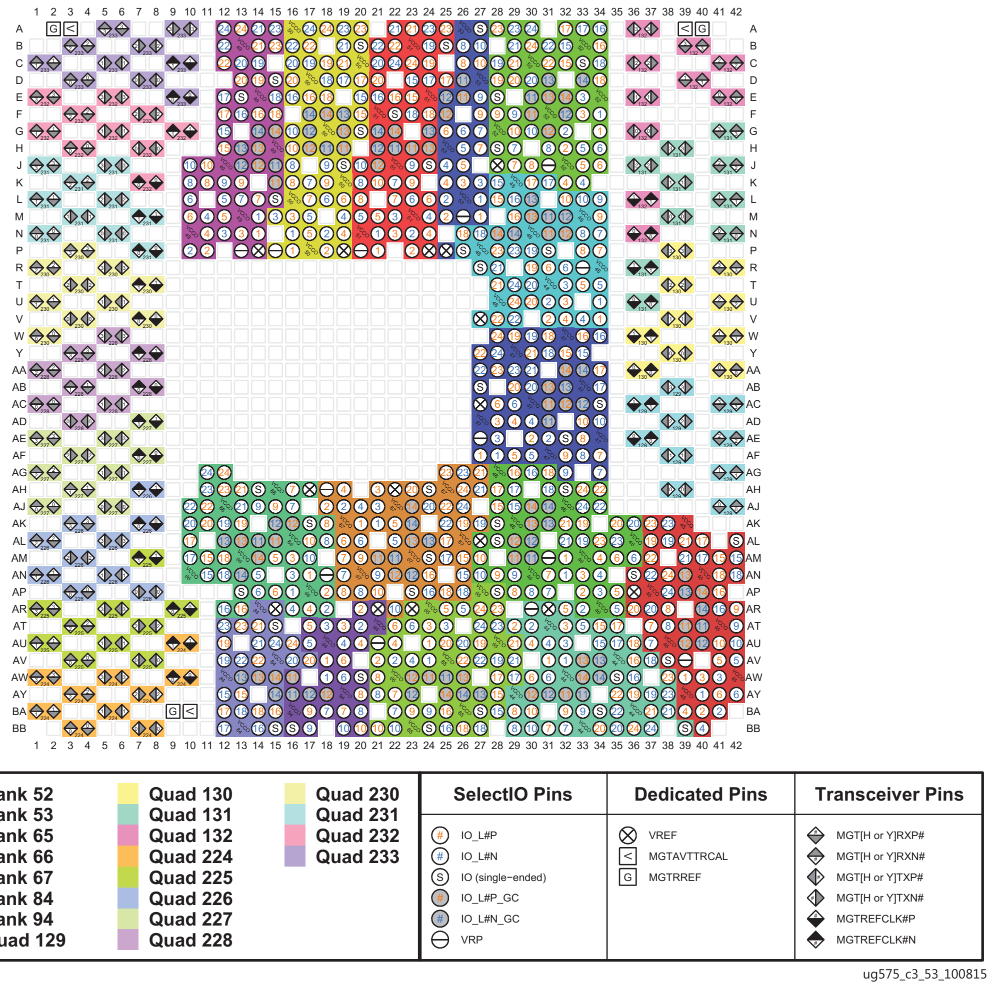

Figure 3-53: **FLVB1760 Package—XCVU125 I/O Bank Diagram**

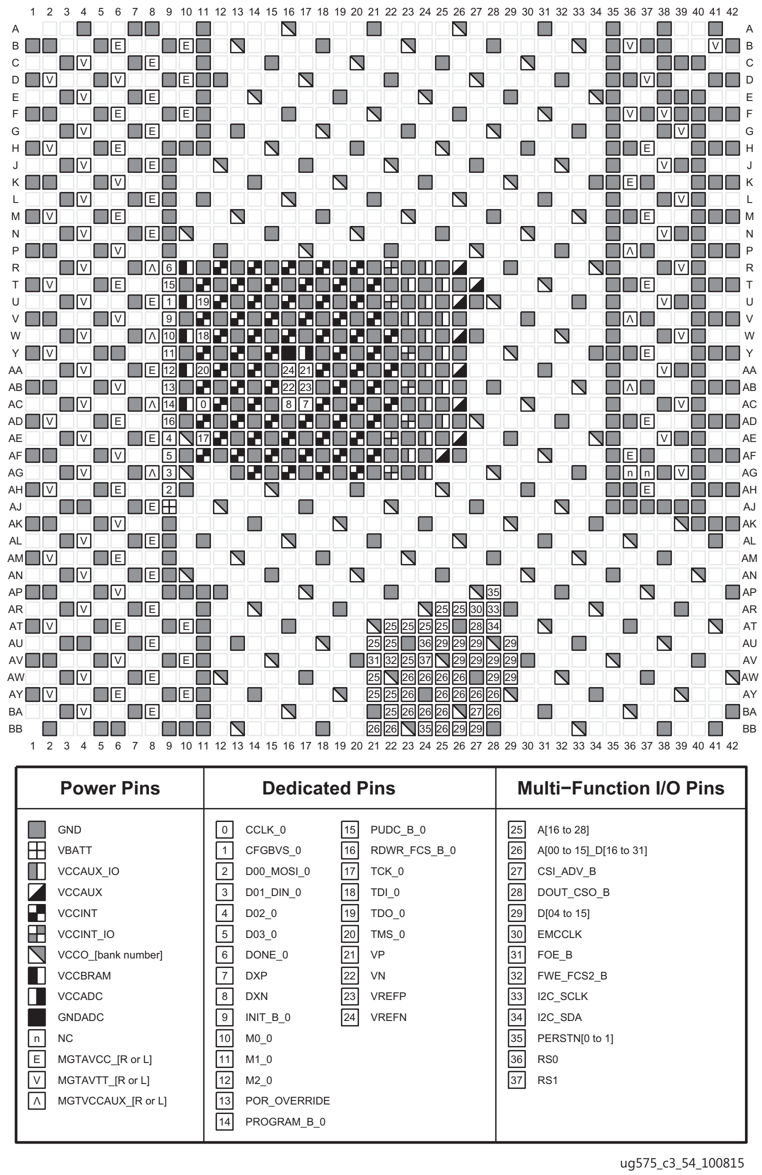

Figure 3-54: **FLVB1760 Package—XCVU125 Configuration/Power Diagram**

FFVA2104 (XCVU080 and XCVU095)

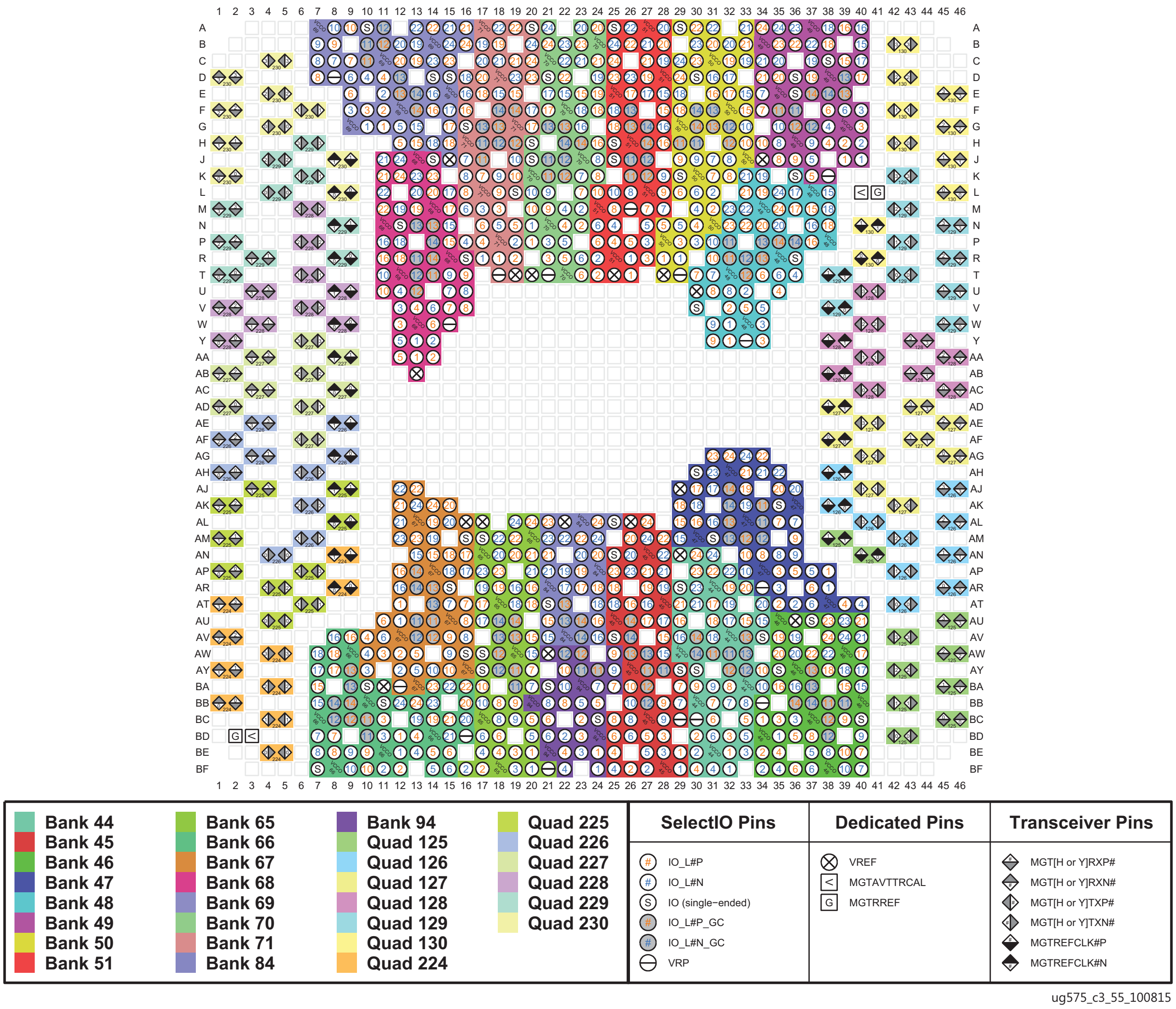

Figure 3-55: **FFVA2104 Package—XCVU080 and XCVU095 I/O Bank Diagram**

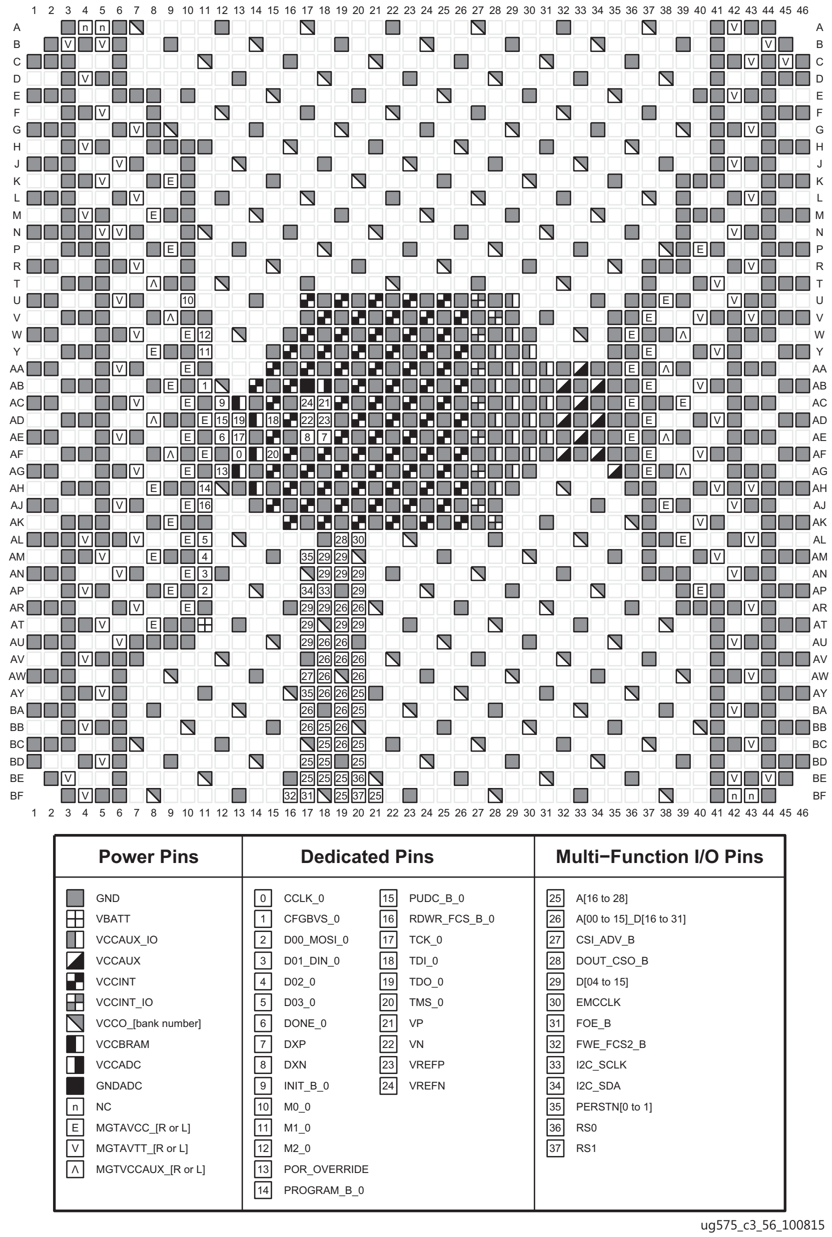

Figure 3-56: **FFVA2104 Package—XCVU080 and XCVU095 Configuration/Power Diagram**

FLVA2104 (XCVU125)

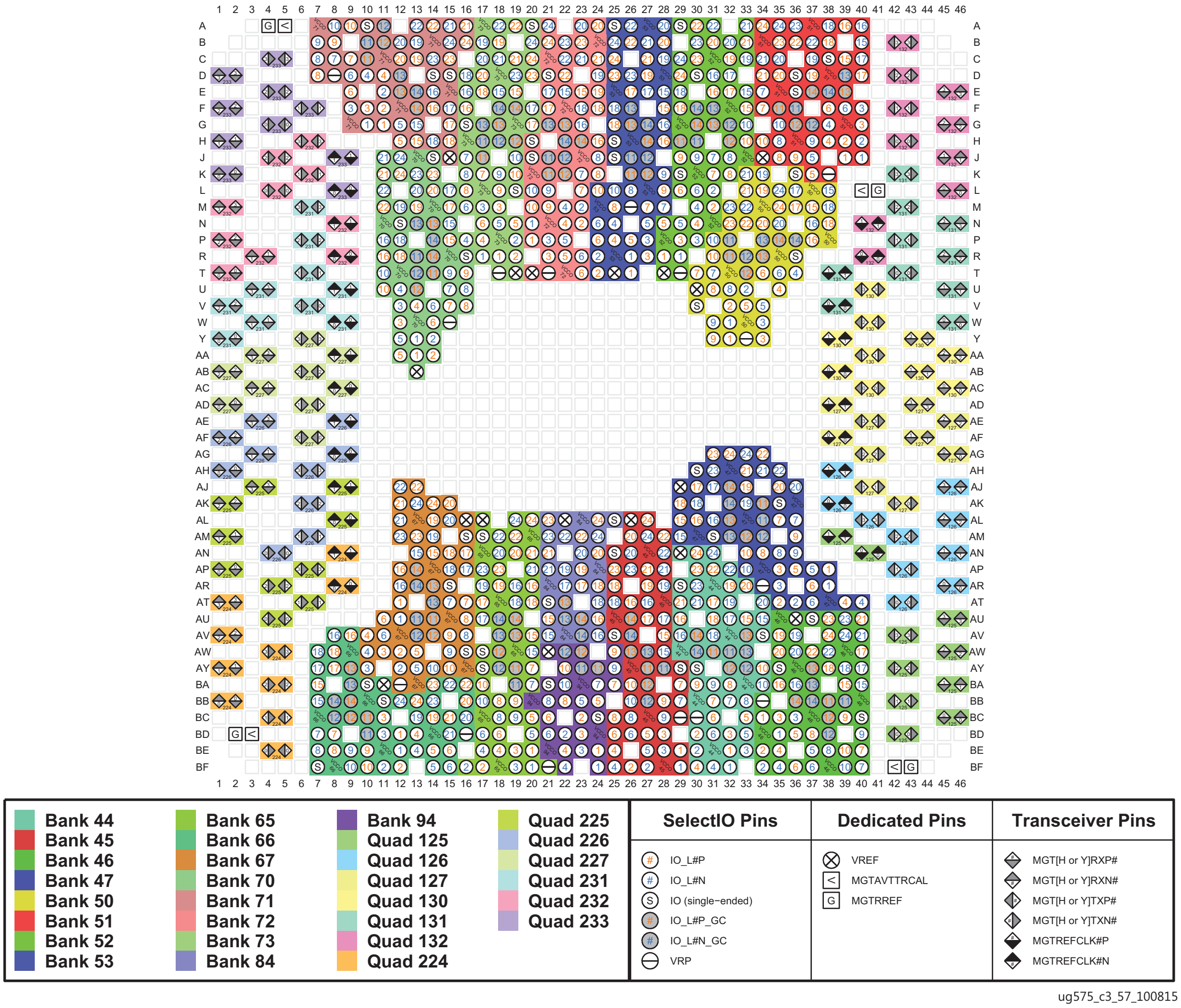

Figure 3-57: **FLVA2104 Package—XCVU125 I/O Bank Diagram**

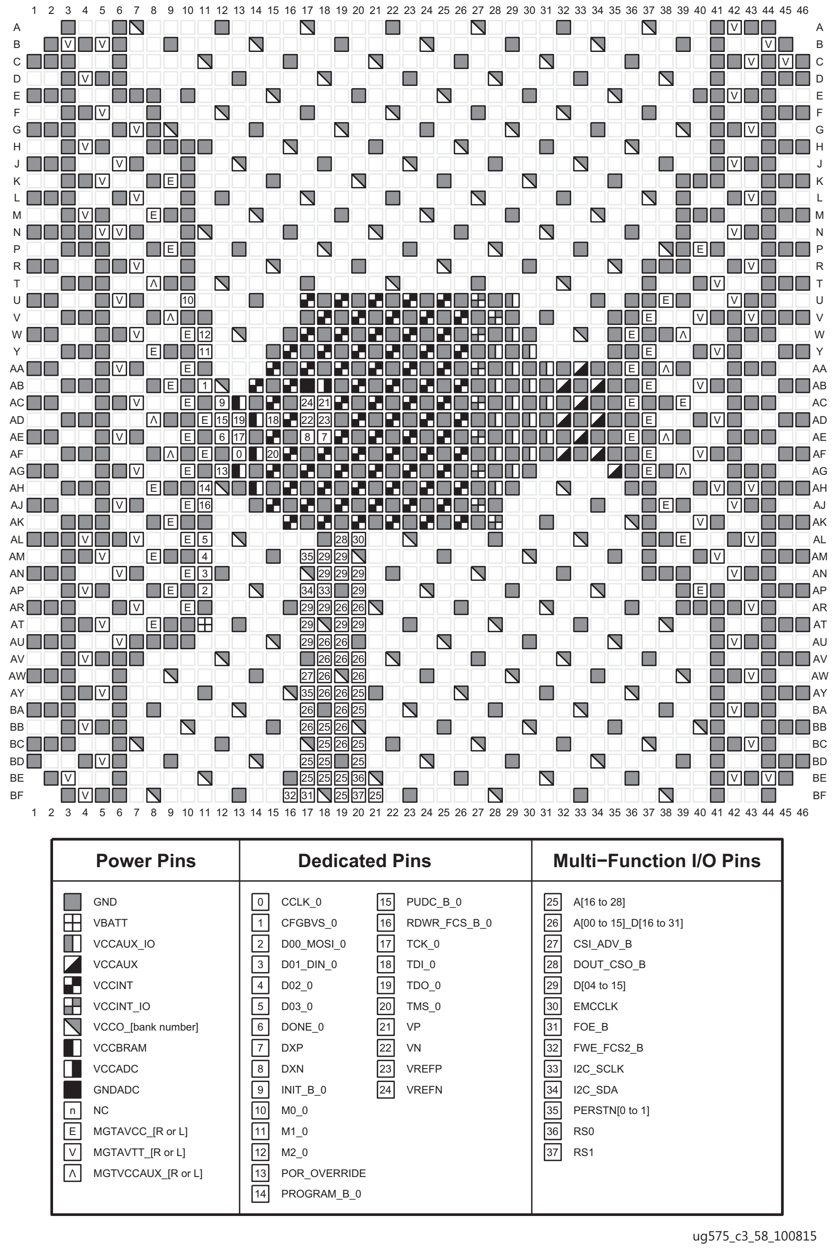

Figure 3-58: **FLVA2104 Package—XCVU125 Configuration/Power Diagram**

FFVB2104 (XCVU080 and XCVU095)

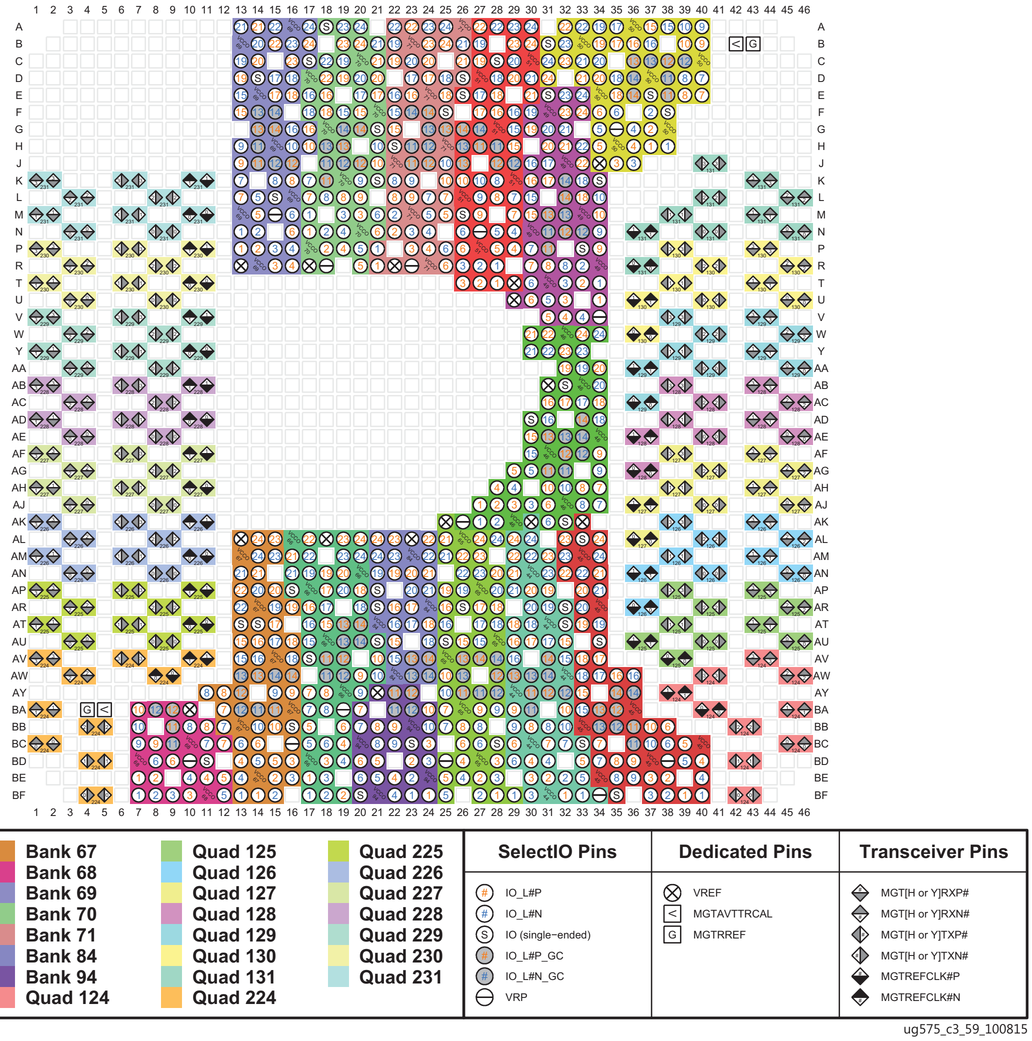

Figure 3-59: **FFVB2104 Package—XCVU080 and XCVU095 I/O Bank Diagram**

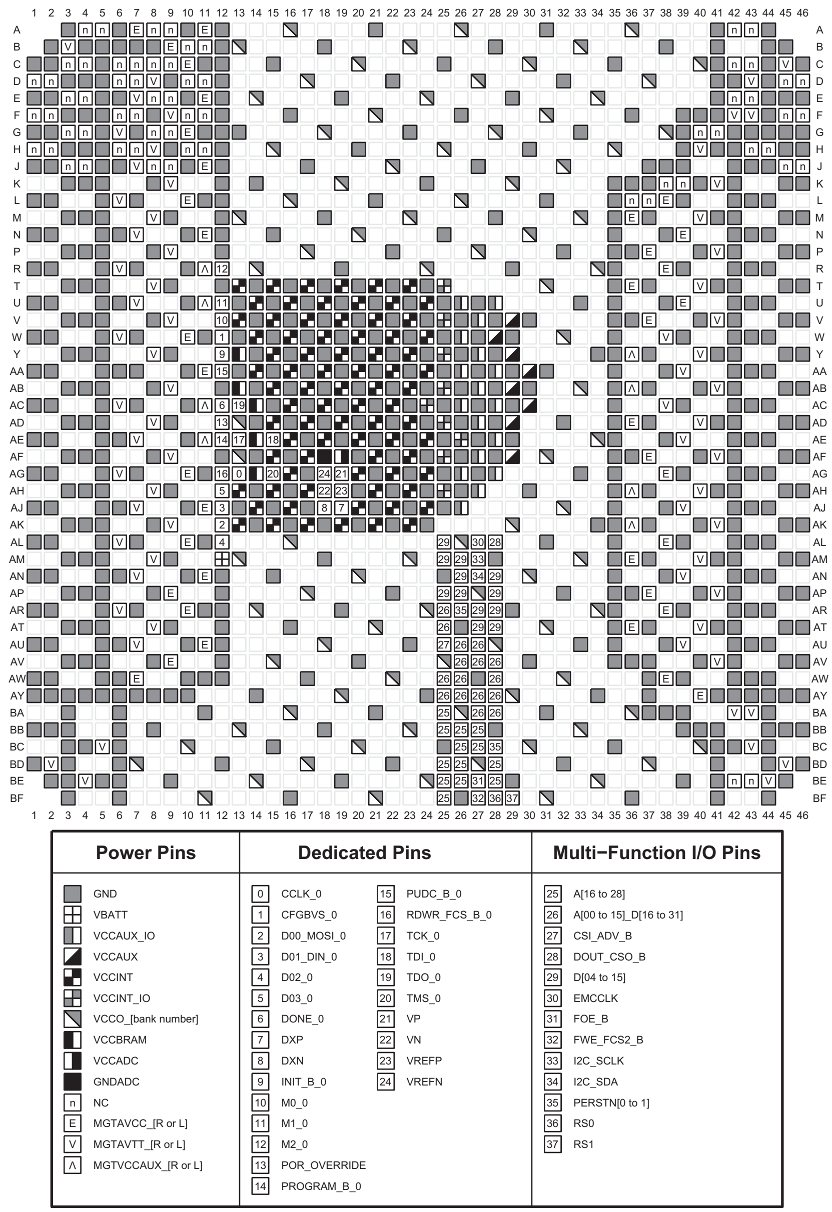

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Figure 3-60: **FFVB2104 Package—XCVU080 and XCVU095 Configuration/Power Diagram**

FLVB2104 (XCVU125)

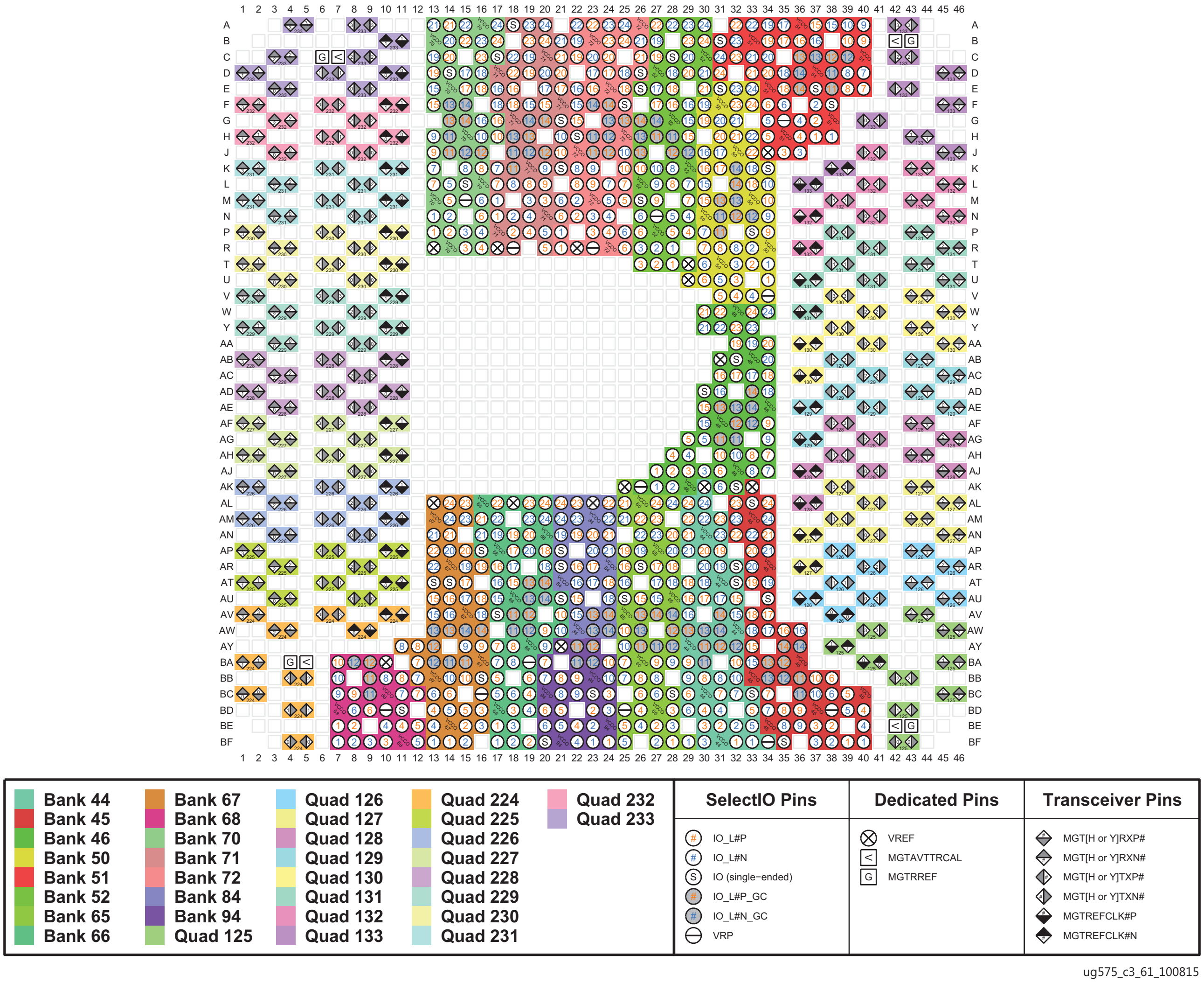


Figure 3-61: **FLVB2104 Package—XCVU125 I/O Bank Diagram**

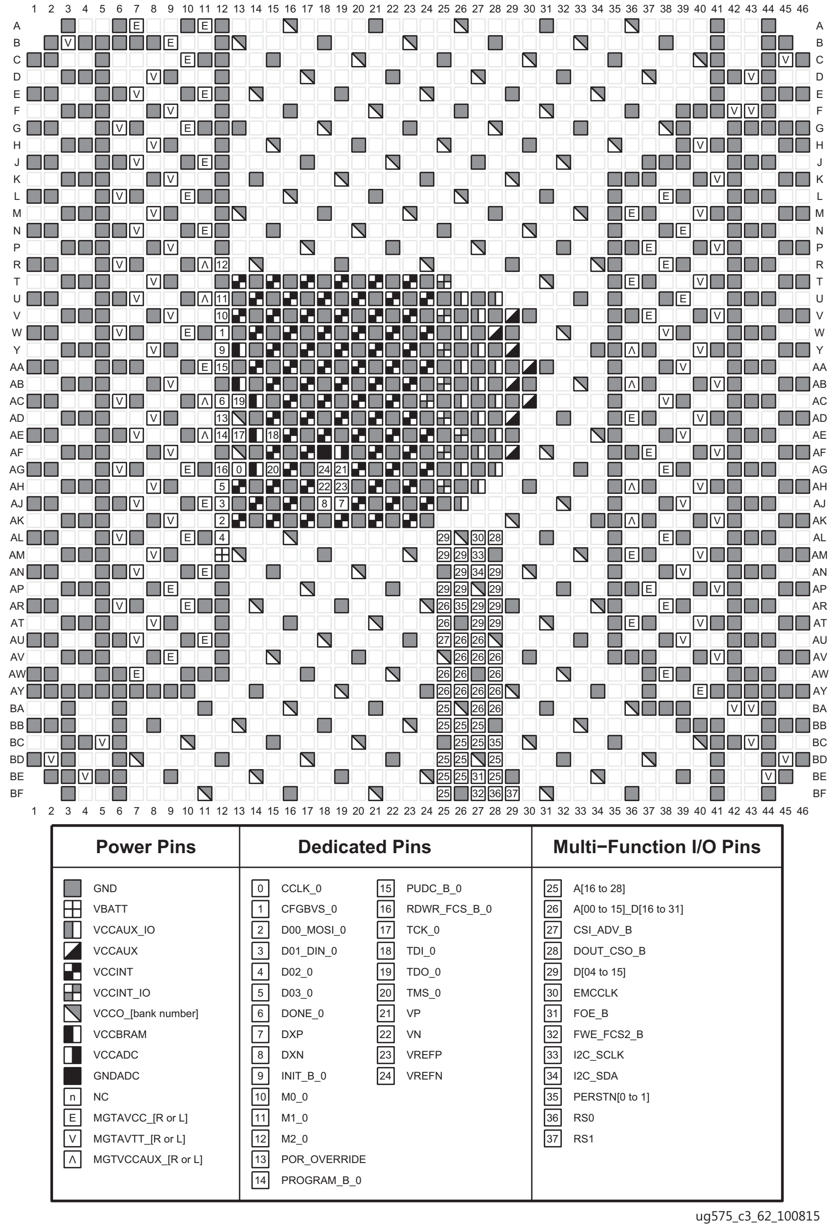


Figure 3-62: **FLVB2104 Package—XCVU125 Configuration/Power Diagram**

FLGB2104 (XCVU160 and XCVU190)

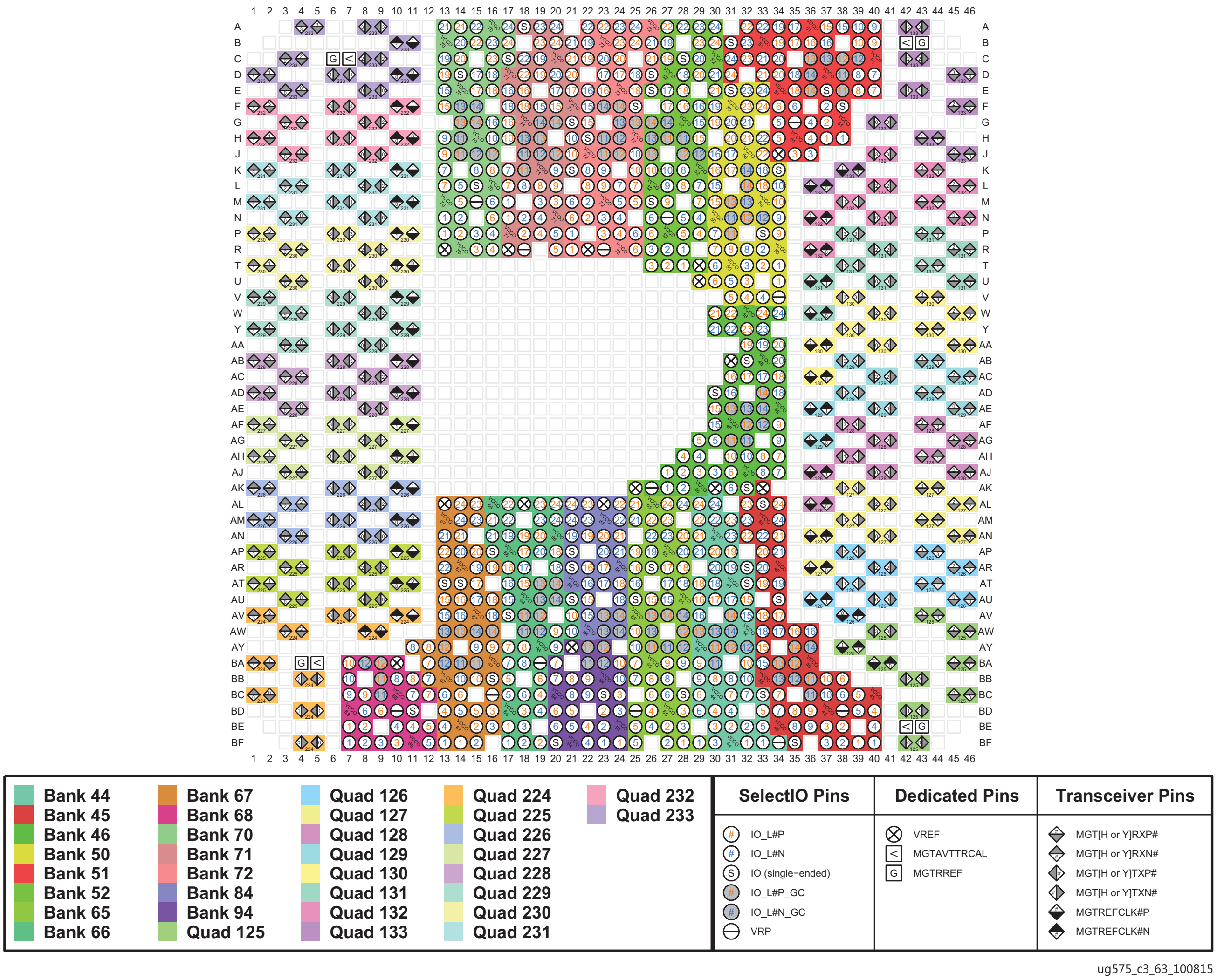


Figure 3-63: **FLGB2104 Package—XCVU160 and XCVU190 I/O Bank Diagram**

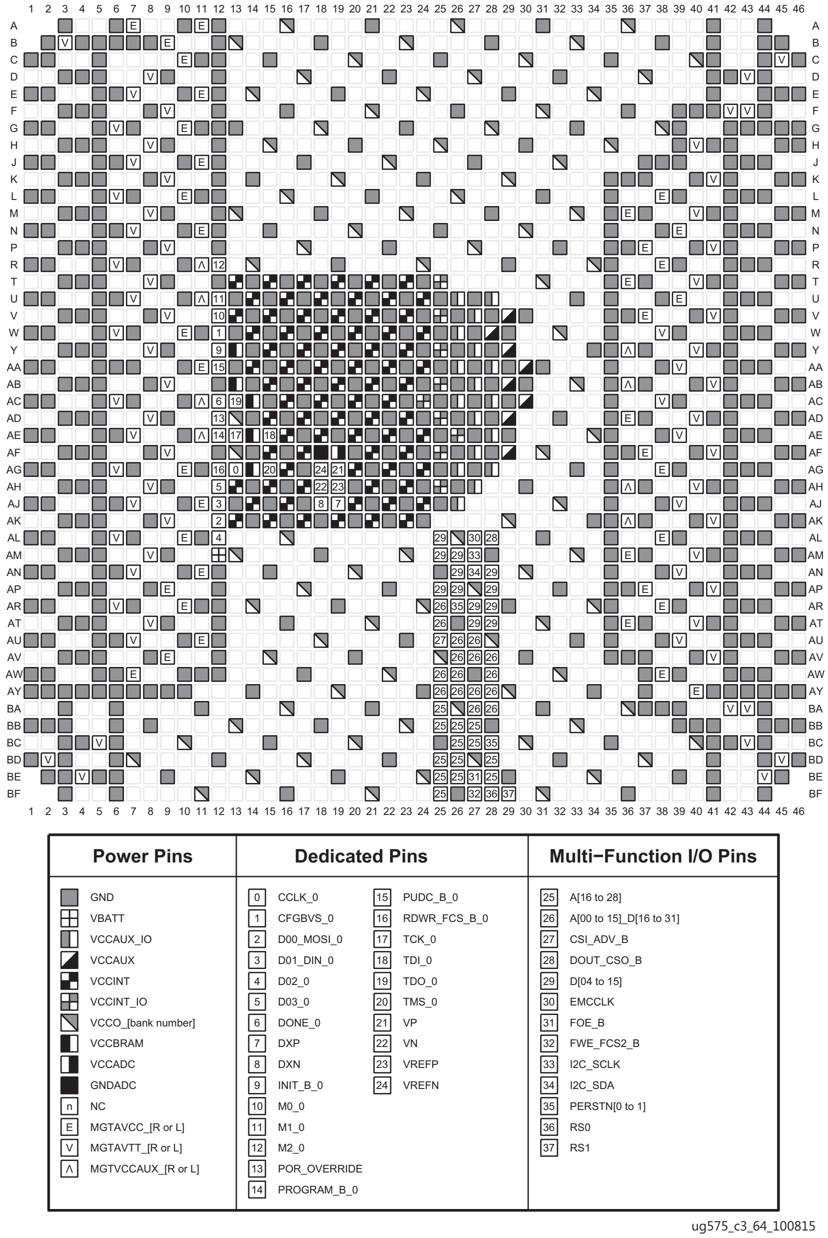


Figure 3-64: **FLGB2104 Package—XCVU160 and XCVU190 Configuration/Power Diagram**

FFVC2104 (XCVU095)

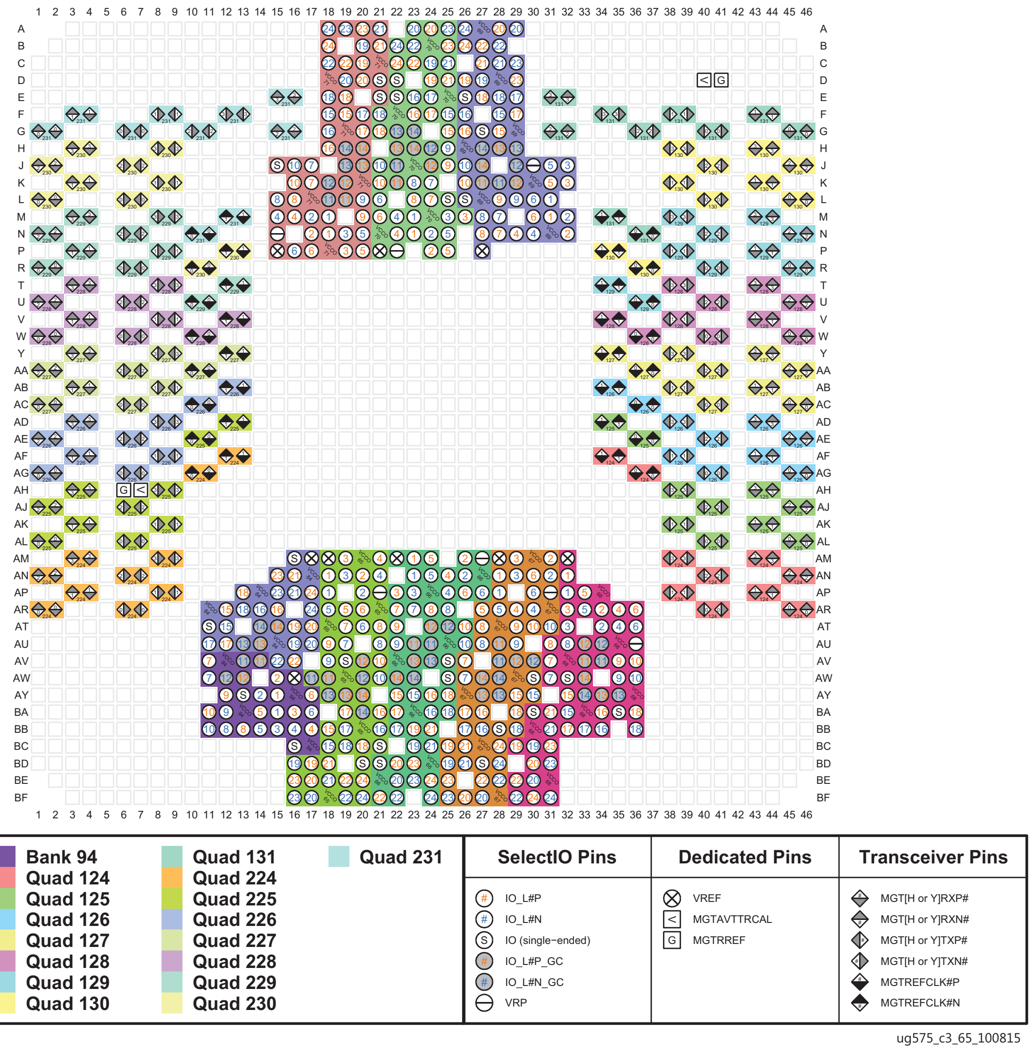
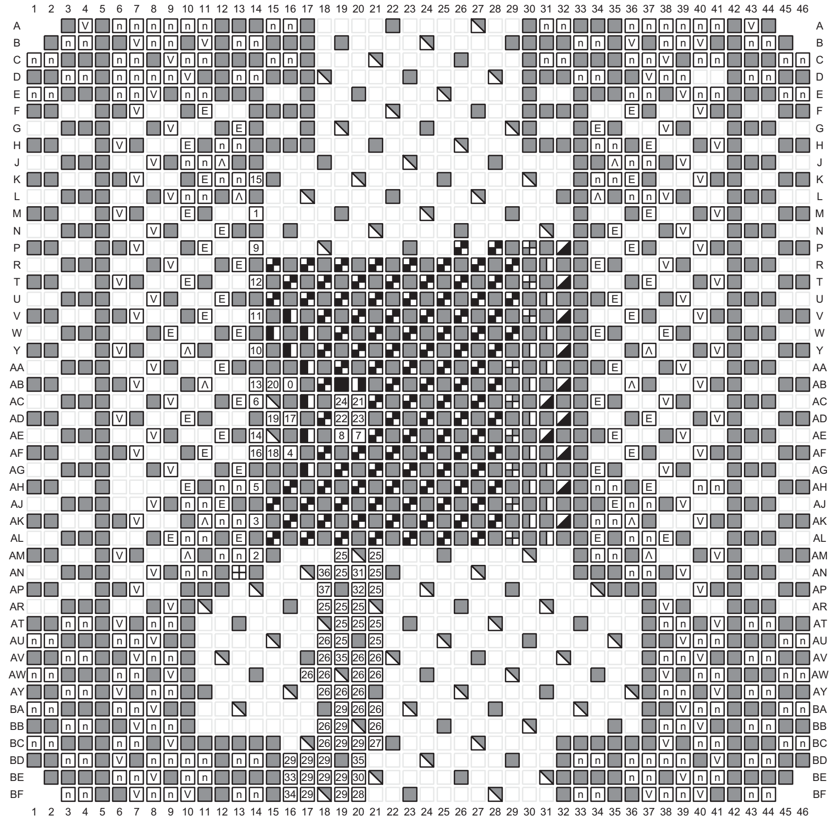


Figure 3-65: **FFVC2104 Package—XCVU095 I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	15 PUDC_B_0	25 A[16 to 28]
VBATT	1 CFGBVS_0	16 RDWR_FCS_B_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	2 D00_MOSI_0	17 TCK_0	27 CSI_ADV_B
VCCAUX	3 D01_DIN_0	18 TDI_0	28 DOUT_CSO_B
VCCINT	4 D02_0	19 TDO_0	29 D[04 to 15]
VCCINT_IO	5 D03_0	20 TMS_0	30 EMCCLK
VCCO_[bank number]	6 DONE_0	21 VP	31 FOE_B
VCCBRAM	7 DXP	22 VN	32 FWE_FCS2_B
VCCADC	8 DXN	23 VREFP	33 I2C_SCLK
GNDADC	9 INIT_B_0	24 VREFN	34 I2C_SDA
n NC	10 M0_0		35 PERSTN[0 to 1]
E MGTAVCC_[R or L]	11 M1_0		36 RS0
V MGTAVTT_[R or L]	12 M2_0		37 RS1
Λ MGTVCCAUX_[R or L]	13 POR_OVERRIDE		
	14 PROGRAM_B_0		

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Figure 3-66: **FFVC2104 Package—XCVU095 Configuration/Power Diagram**

FLVC2104 (XCVU125)

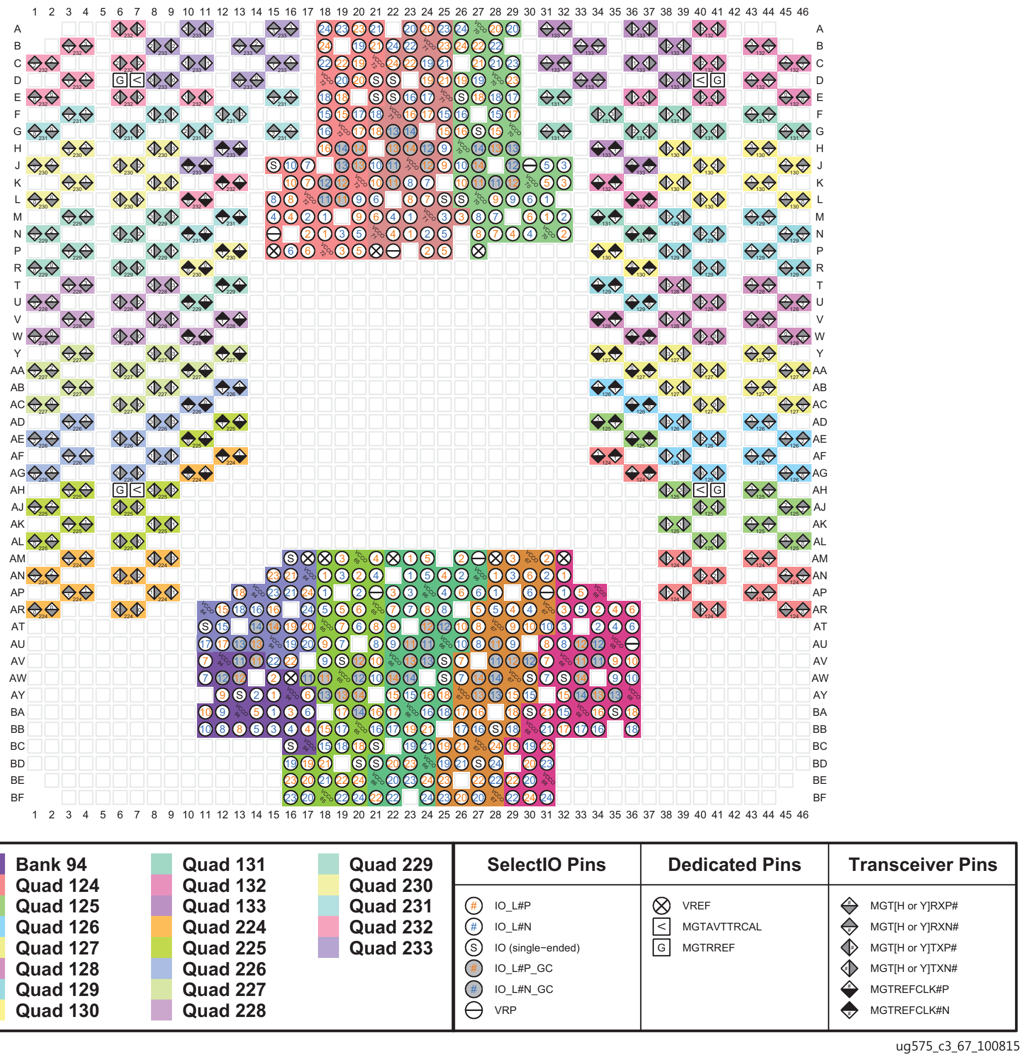


Figure 3-67: **FLVC2104 Package—XCVU125 I/O Bank Diagram**

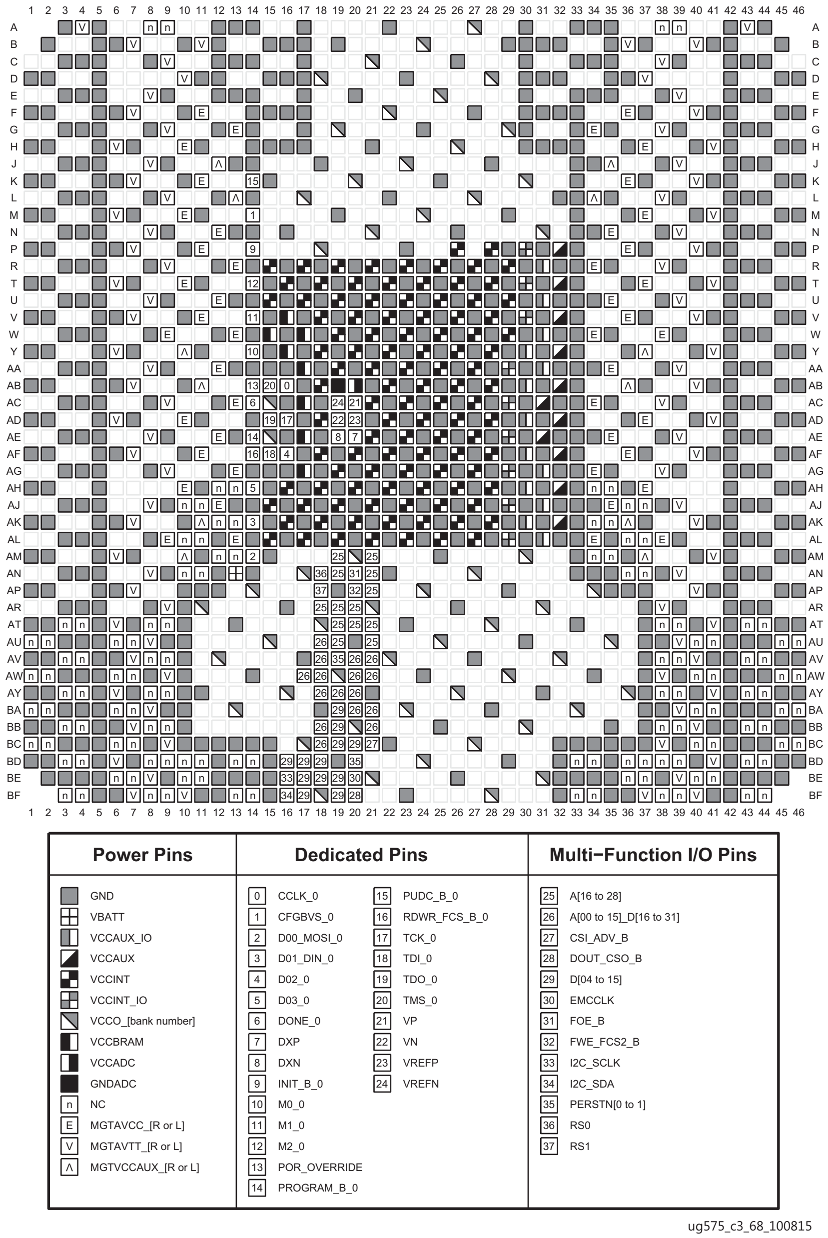


Figure 3-68: **FLVC2104 Package—XCVU125 Configuration/Power Diagram**

FLGC2104 (XCVU160 and XCVU190)

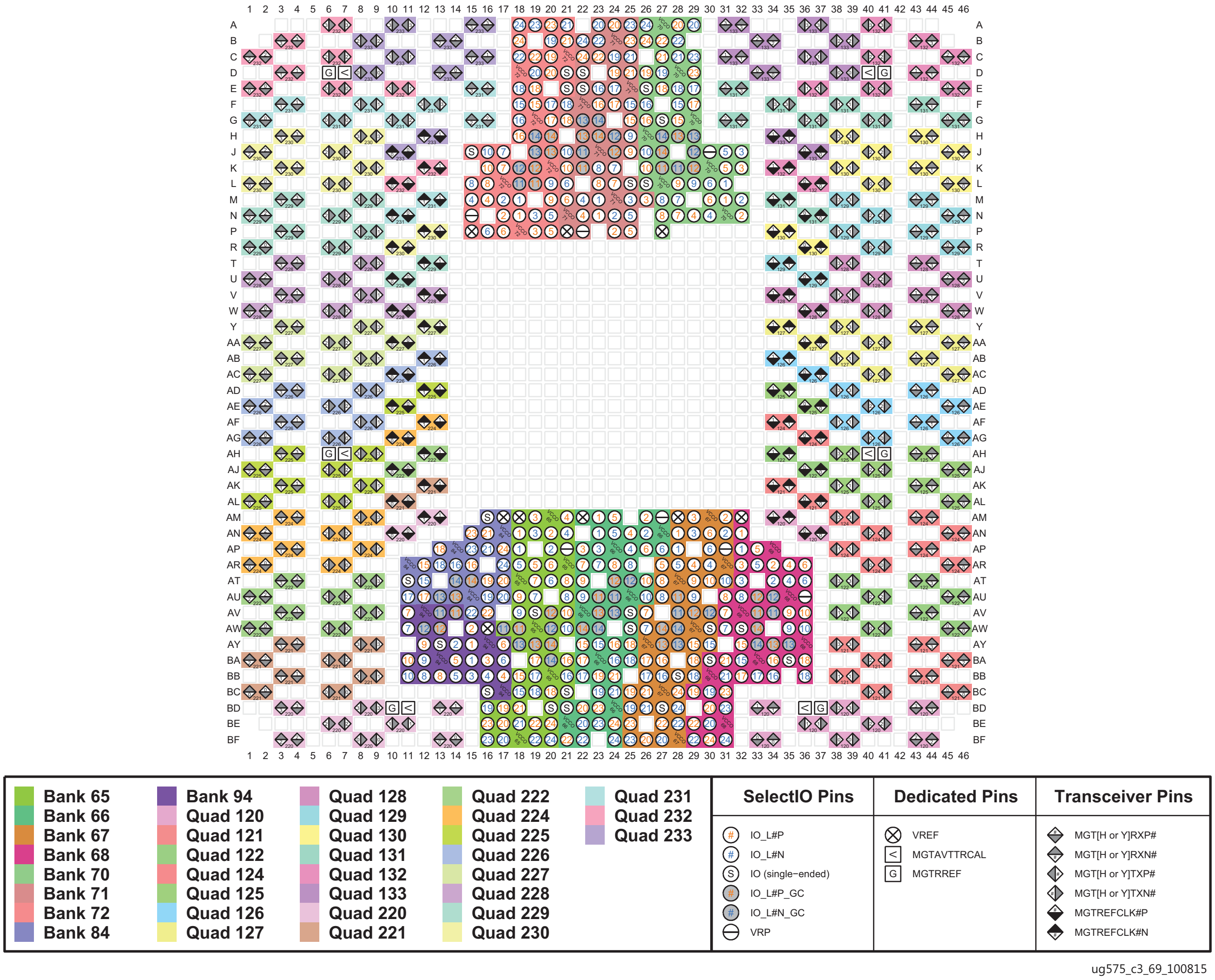


Figure 3-69: **FLGC2104 Package—XCVU160 and XCVU190 I/O Bank Diagram**

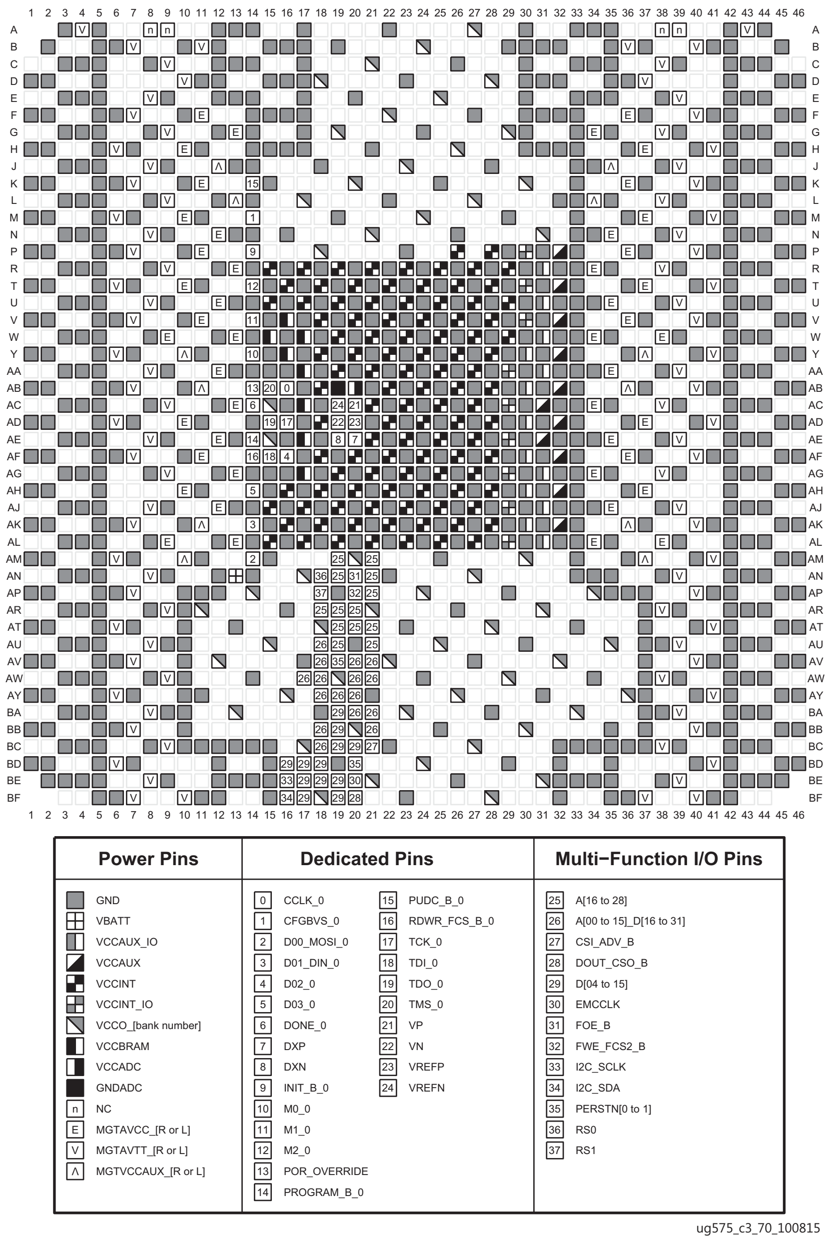


Figure 3-70: **FLGC2104 Package—XCVU160 and XCVU190 Configuration/Power Diagram**

FLGB2377 (XCVU440)

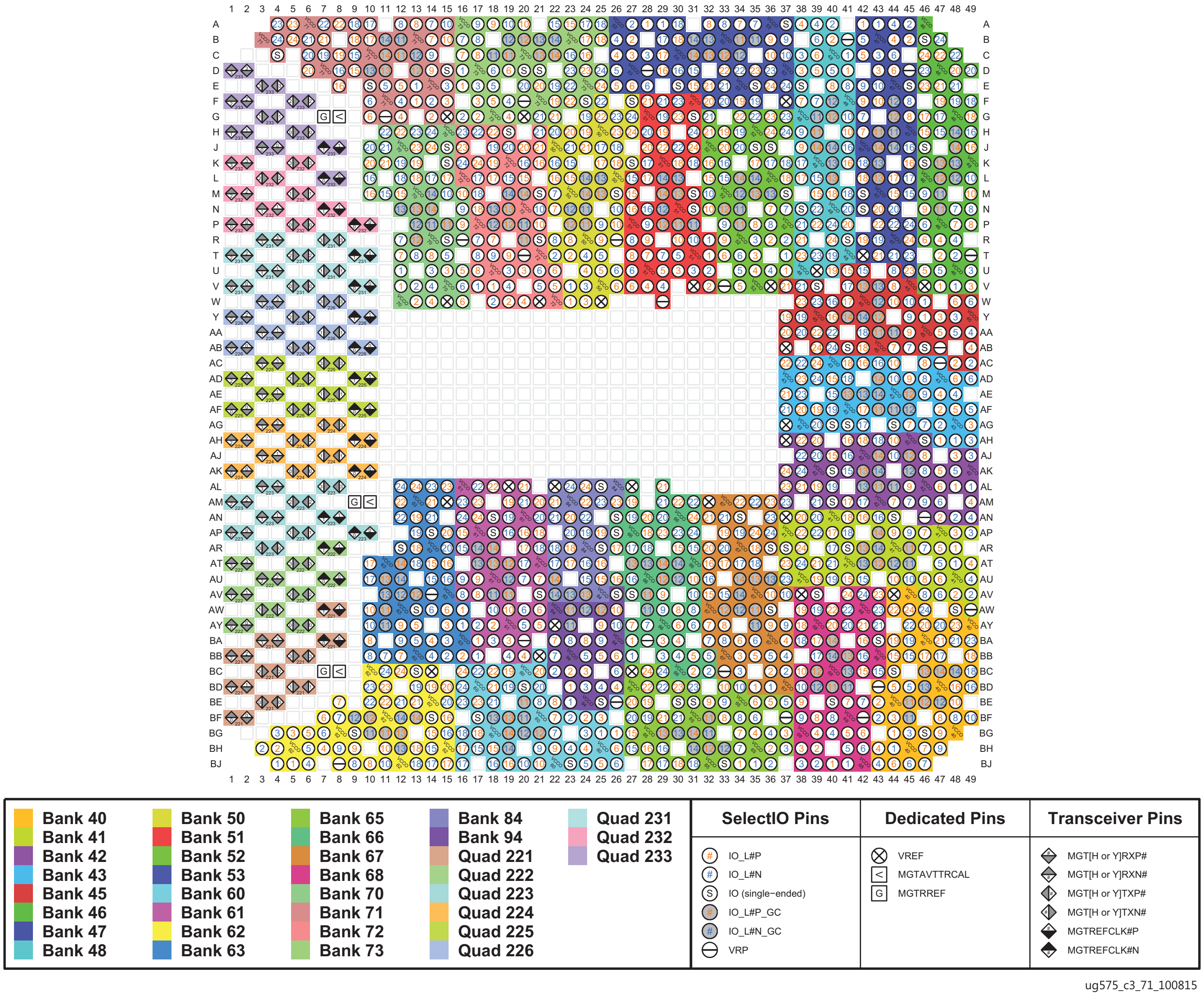


Figure 3-71: **FLGB2377 Package—XCVU440 I/O Bank Diagram**

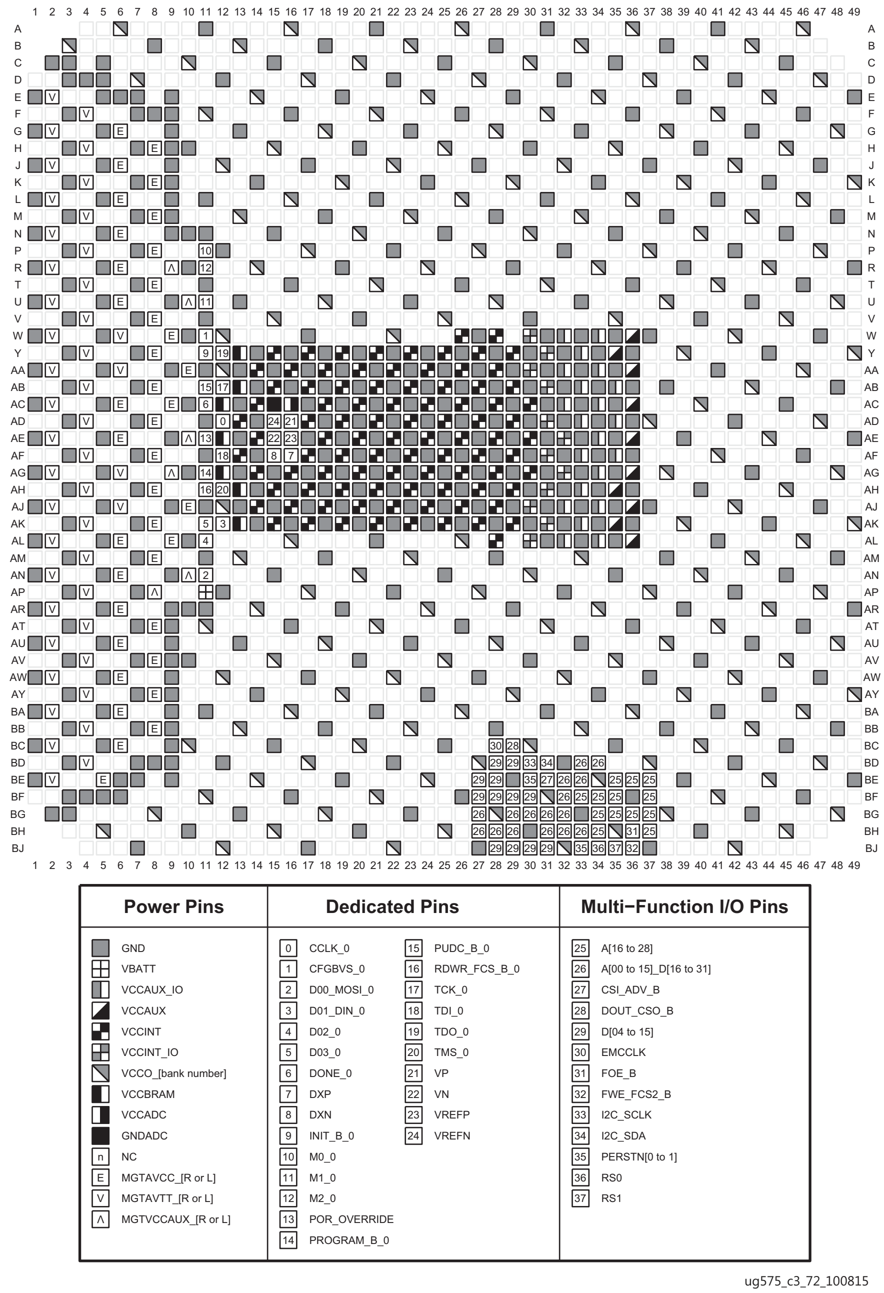


Figure 3-72: **FLGB2377 Package—XCVU440 Configuration/Power Diagram**

FLGA2577 (XCVU190)

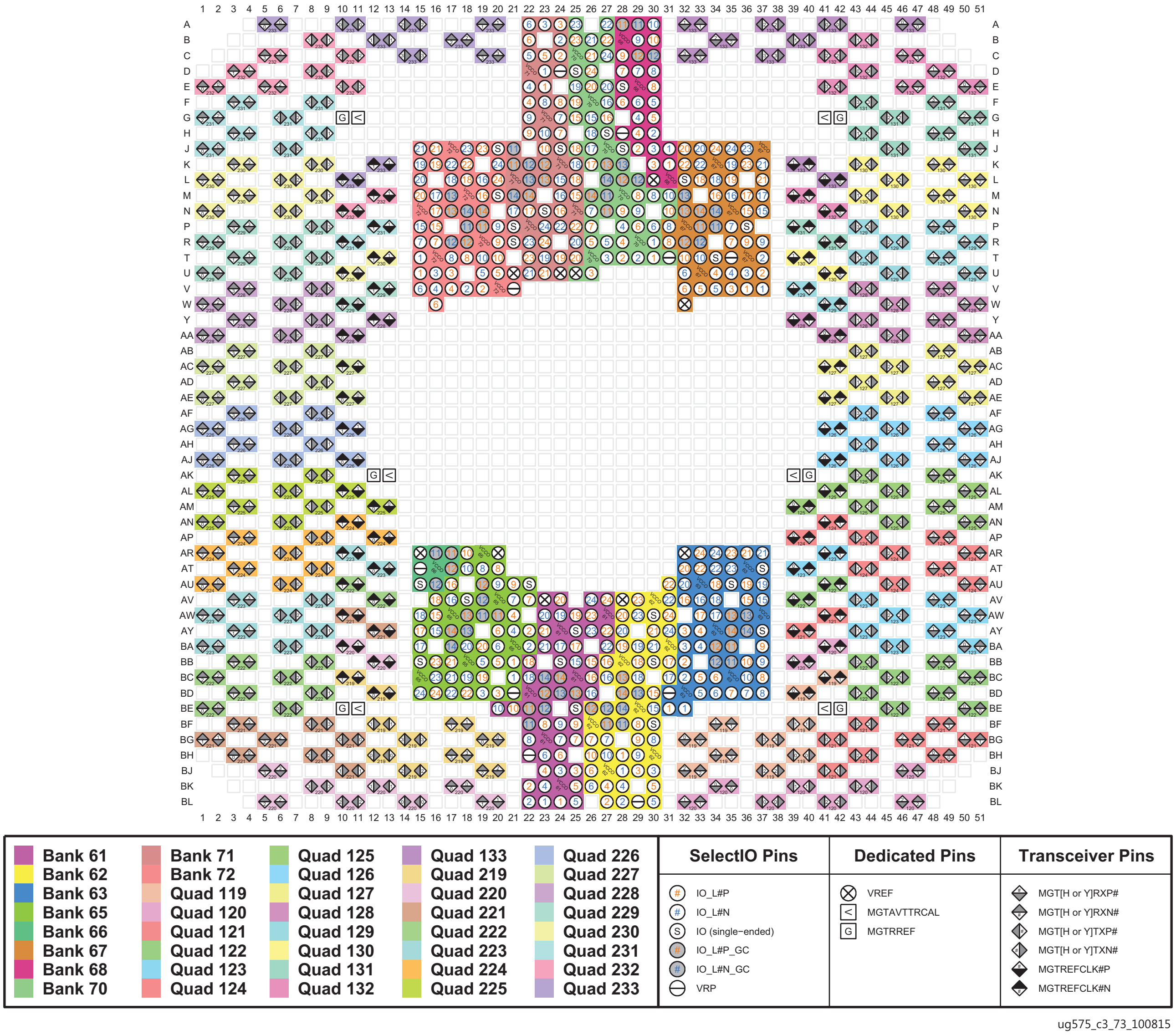


Figure 3-73: **FLGA2577 Package—XCVU190 I/O Bank Diagram**

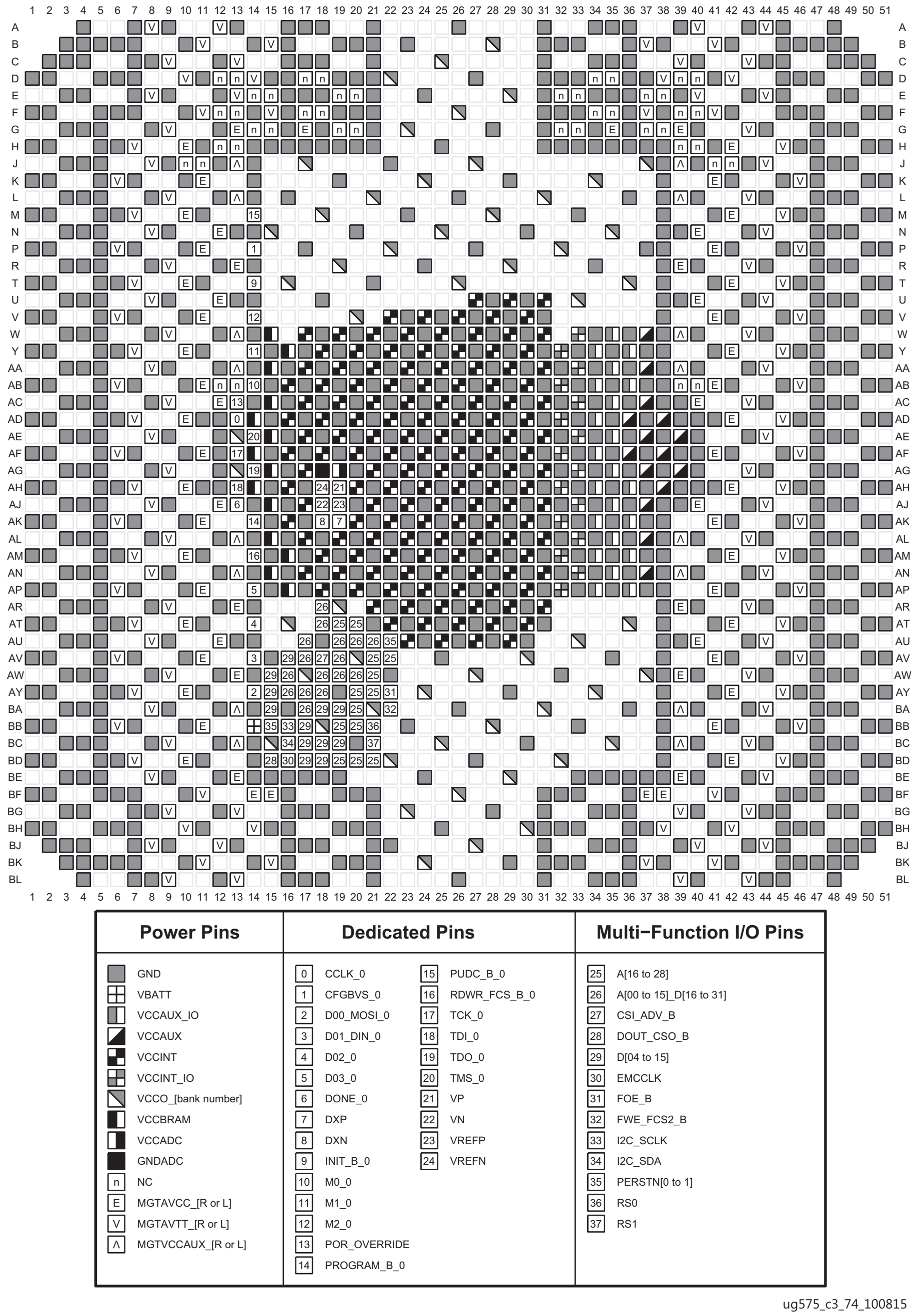


Figure 3-74: **FLGA2577 Package—XCVU190 Configuration/Power Diagram**

FLGA2892 (XCVU440)

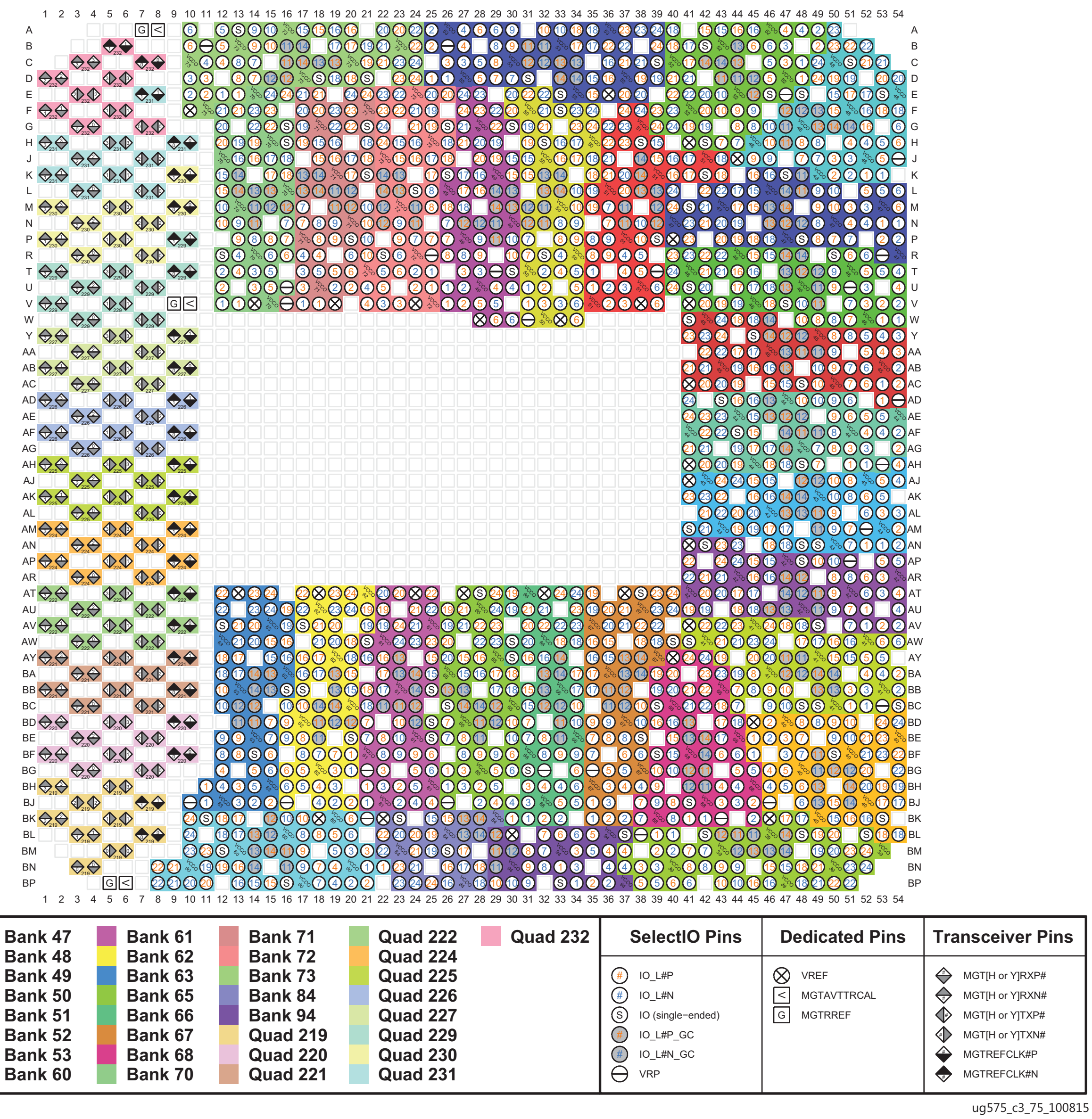


Figure 3-75: **FLGA2892 Package—XCVU440 I/O Bank Diagram**

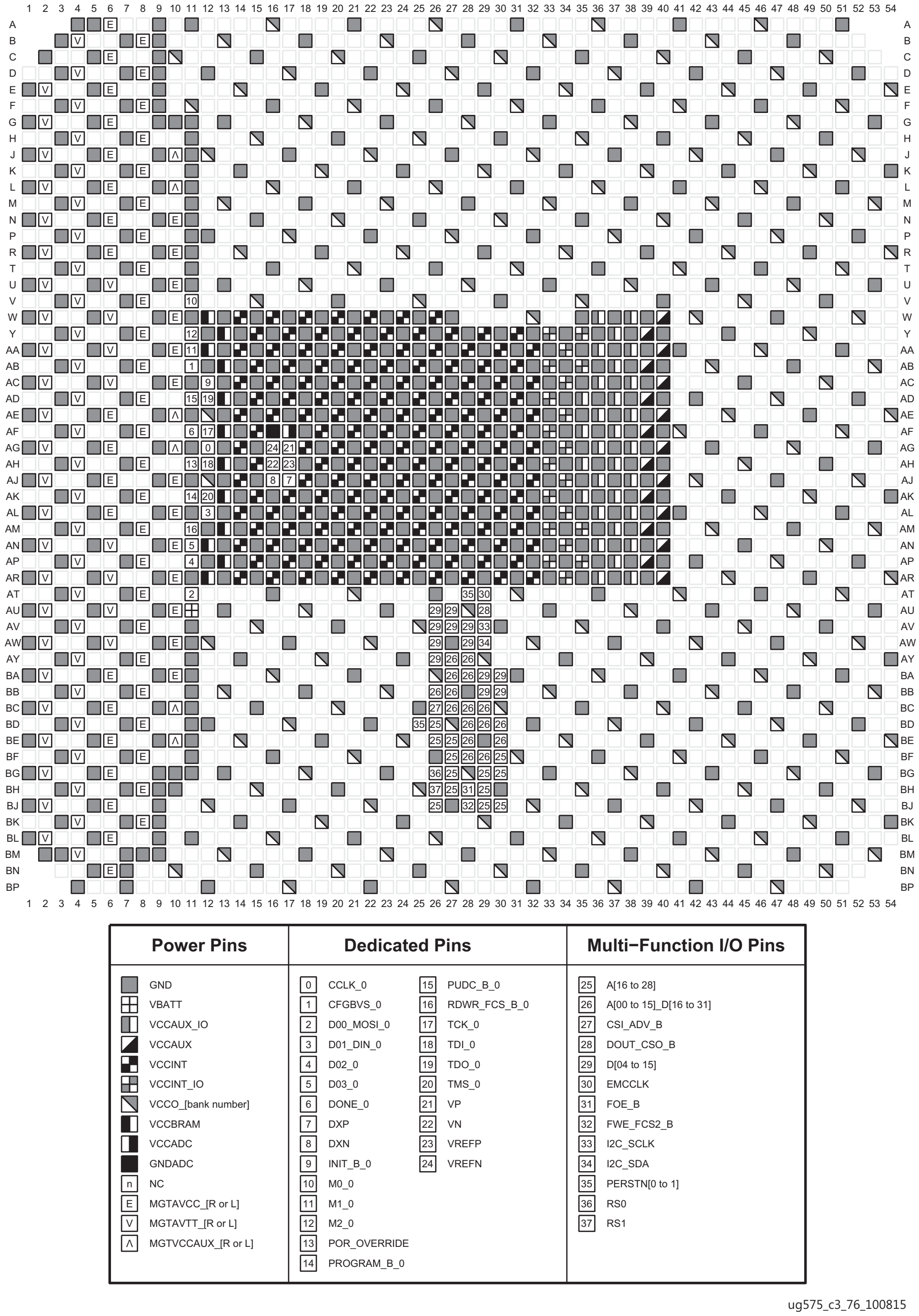


Figure 3-76: **FLGA2892 Package—XCVU440 Configuration/Power Diagram**

FCVA289 (XCAU7P and XAAU7P)

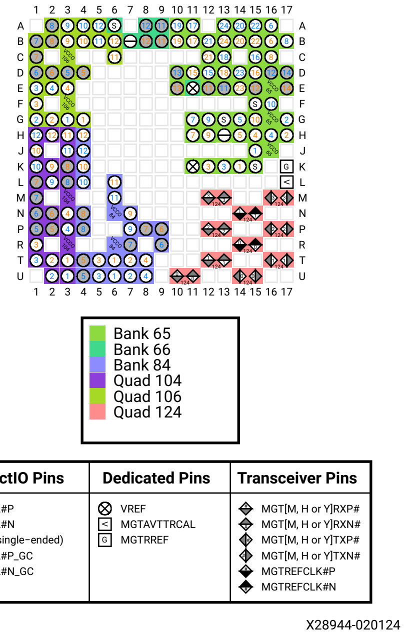


Figure 3-77: **FCVA289 Package—XCAU7P and XAAU7P I/O Bank Diagram**

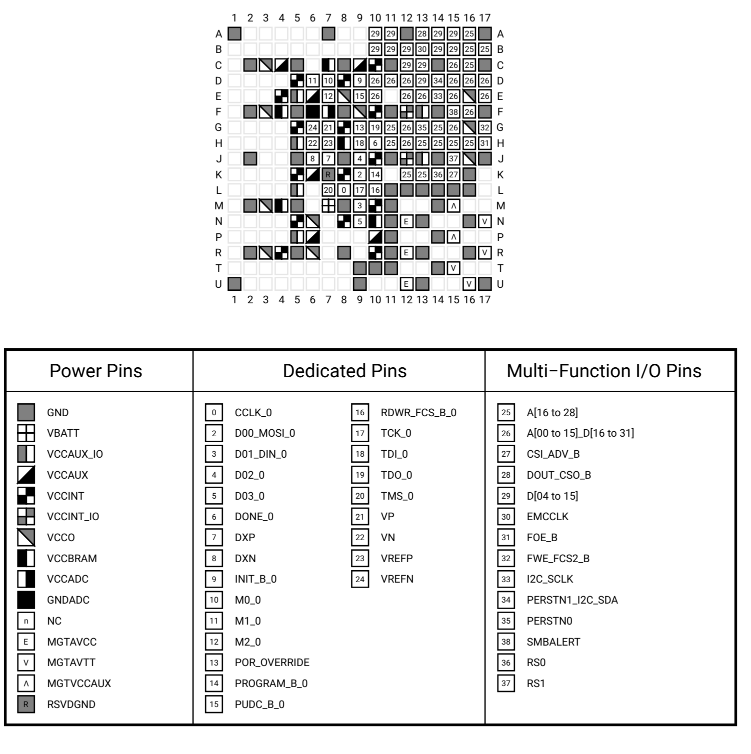
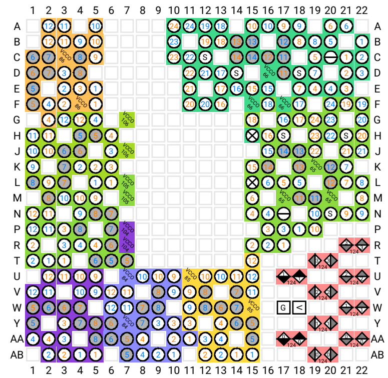


Figure 3-78: **FCVA289 Package— XCAU7P and XAAU7P Configuration/Power Diagram**

SBVC484 (XCAU7P and XAAU7P)

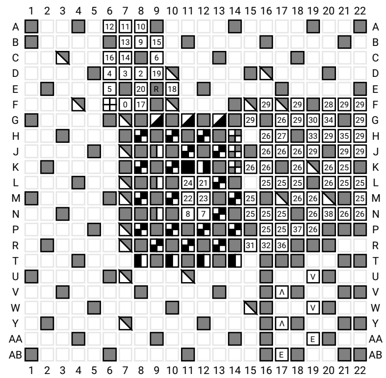


Bank 65	Quad 106
Bank 66	Quad 124
Bank 84	
Bank 85	
Bank 86	
Quad 104	
Quad 105	

SelectIO Pins	Dedicated Pins	Transceiver Pins
IO_L#P	VREF	MGT[M, H or Y]RXP#
IO_L#N	MGTAVTTRCAL	MGT[M, H or Y]RXN#
IO (single-ended)	MGTRREF	MGT[M, H or Y]TXP#
IO_L#P_GC		MGT[M, H or Y]TXN#
IO_L#N_GC		MGTREFCLK#P
VRP		MGTREFCLK#N

X27958-041023

Figure 3-79: **SBVC484 Package—XCAU7P and XAAU7P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

X27959-041023

Figure 3-80: **SBVC484 Package— XCAU7P and XAAU7P Configuration/Power Diagram**

FFVB676 (XCAU10P and XAAU10P)

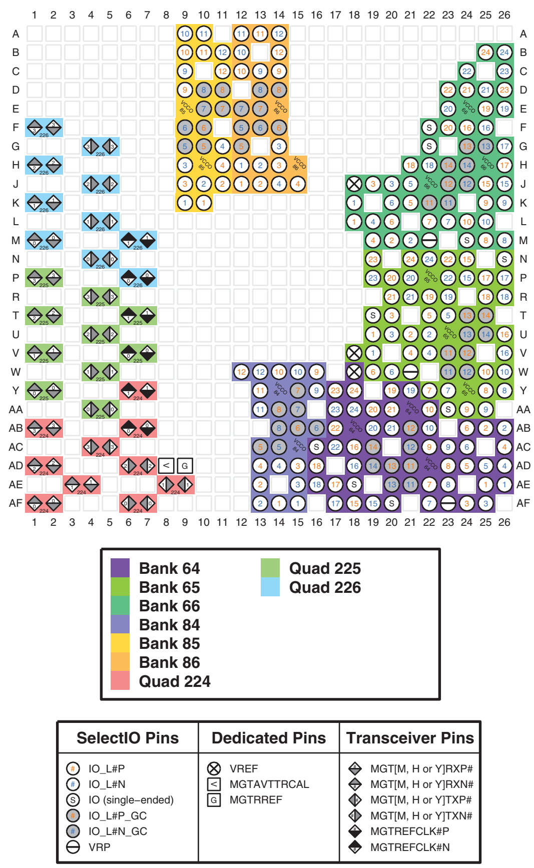
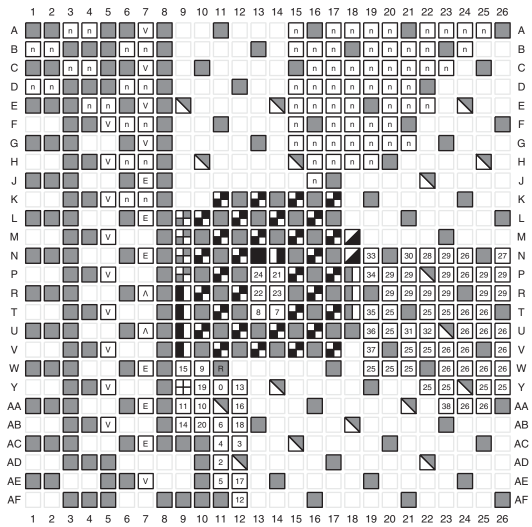


Figure 3-81: **FFVB676 Package—XCAU10P and XAAU10P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi–Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
A MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

Figure 3-82: **FFVB676 Package— XCAU10P and XAAU10P Configuration/Power Diagram**

FFVB676 (XCAU15P and XAAU15P)

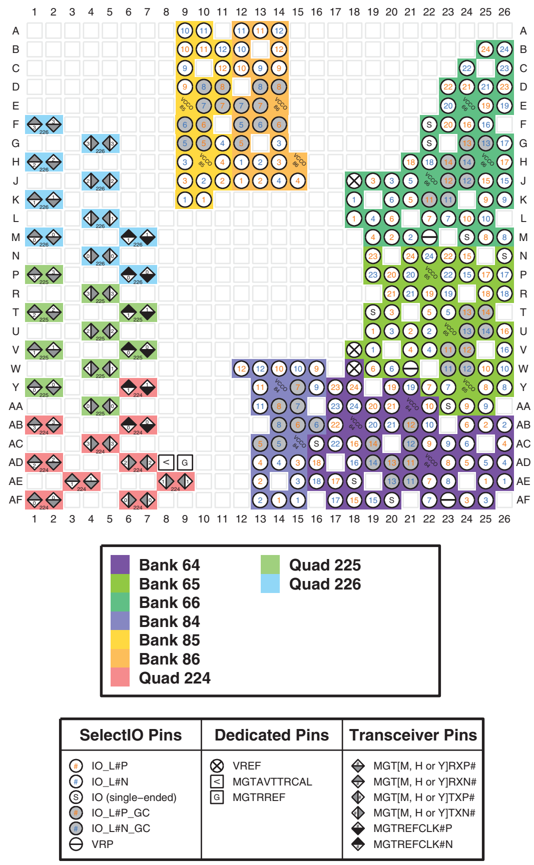
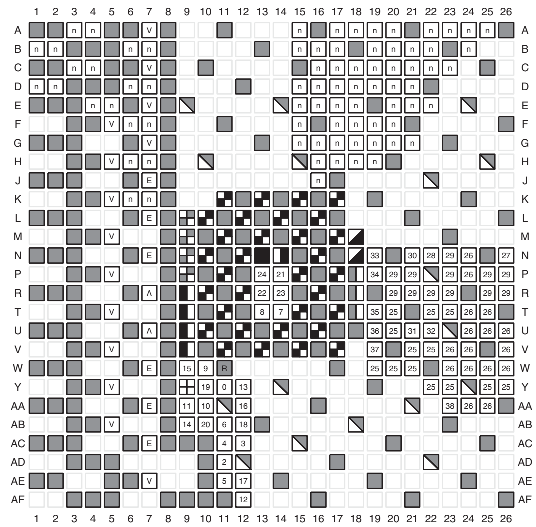


Figure 3-83: **FFVB676 Package—XCAU15P and XAAU15P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi–Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
A MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

Figure 3-84: **FFVB676 Package— XCAU15P and XAAU15P Configuration/Power Diagram**

FFVB676 (XCAU20P)

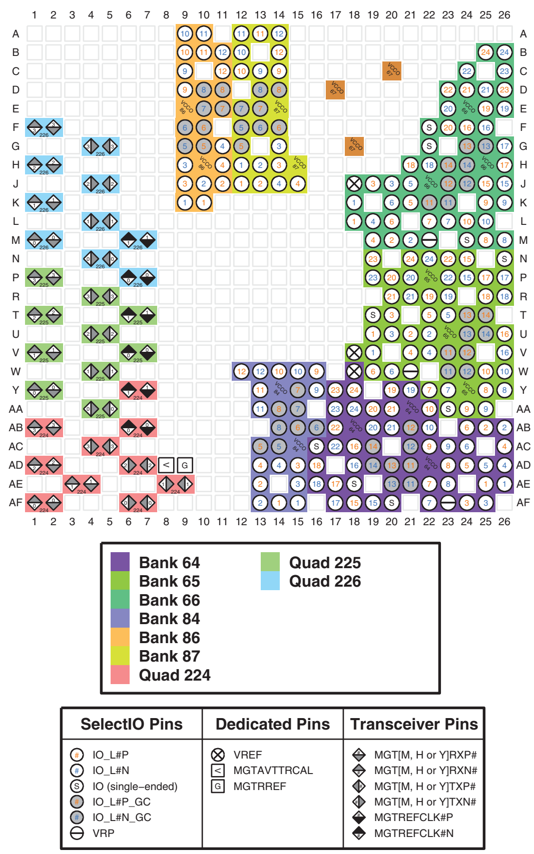
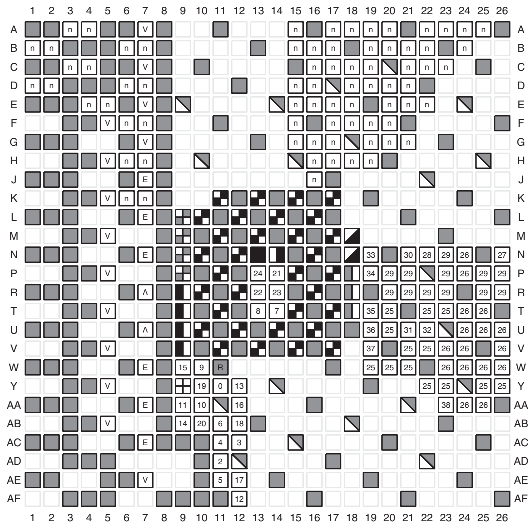


Figure 3-85: **FFVB676 Package—XCAU20P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

Figure 3-86: **FFVB676 Package— XCAU20P Configuration/Power Diagram**

FFVB676 (XCAU25P)

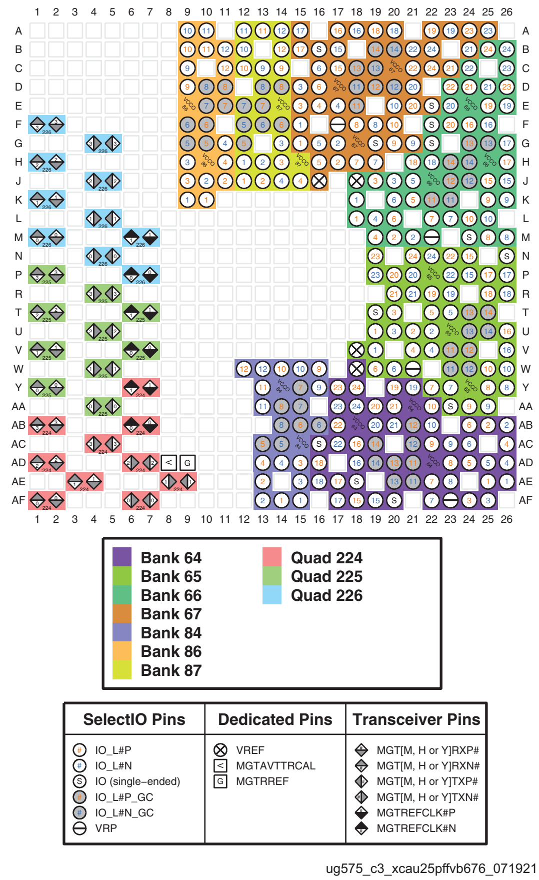
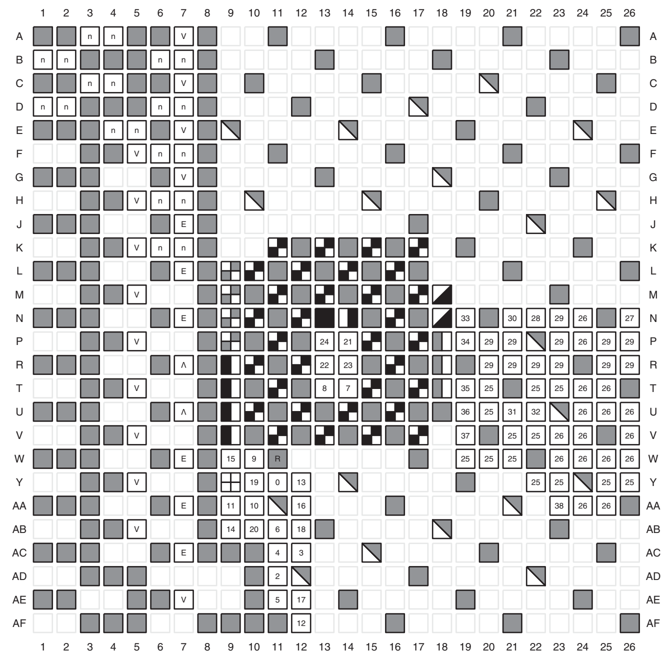


Figure 3-87: **FFVB676 Package—XCAU25P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-88: **FFVB676 Package— XCAU25P Configuration/Power Diagram**

SBVB484 (XCAU10P and XAAU10P)

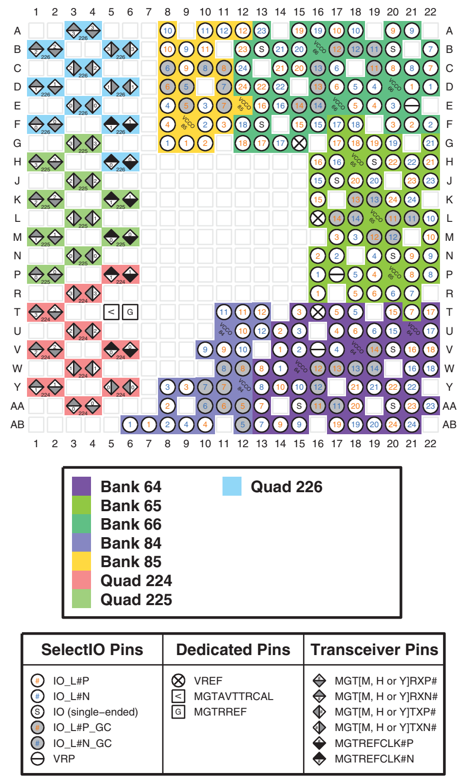
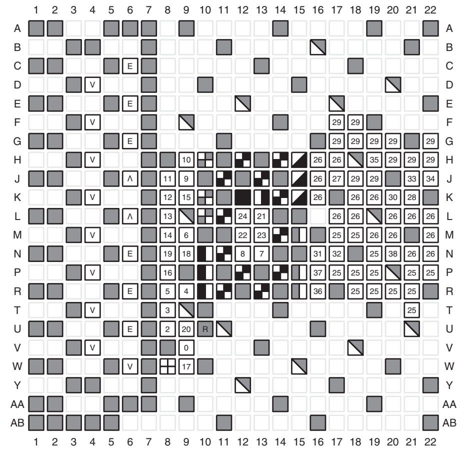


Figure 3-89: **SBVB484 Package—XCAU10P and XAAU10P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

Figure 3-90: **SBVB484 Package— XCAU10P and XAAU10P Configuration/Power Diagram**

SBVB484 (XCAU15P and XAAU15P)

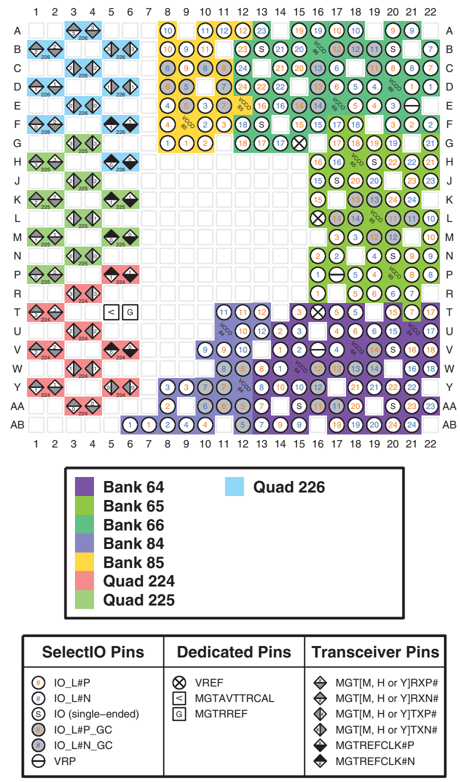


Figure 3-91: **SBVB484 Package—XCAU15P and XAAU15P I/O Bank Diagram**

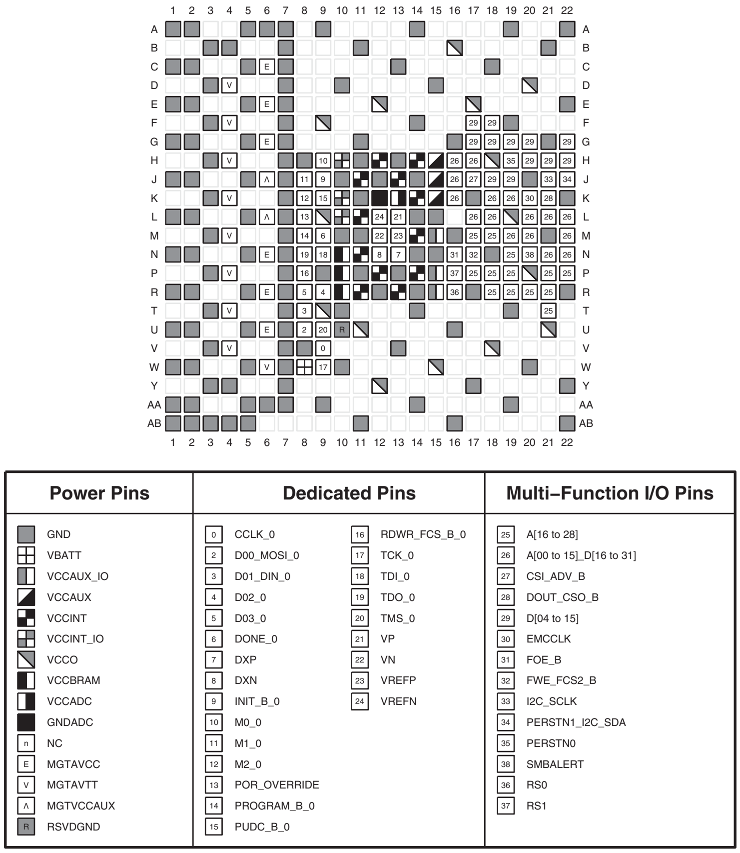


Figure 3-92: **SBVB484 Package— XCAU15P and XAAU15P Configuration/Power Diagram**

SFVB784 (XCAU20P)

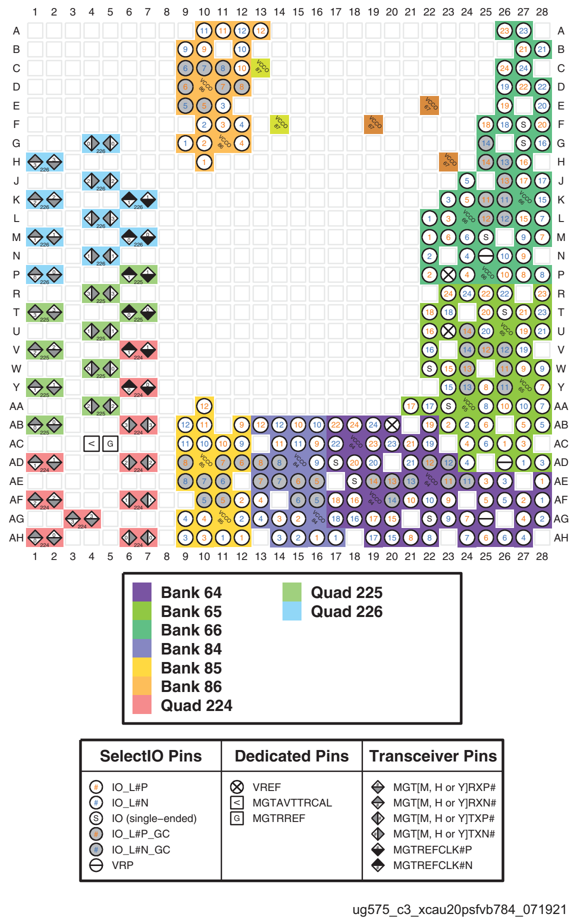
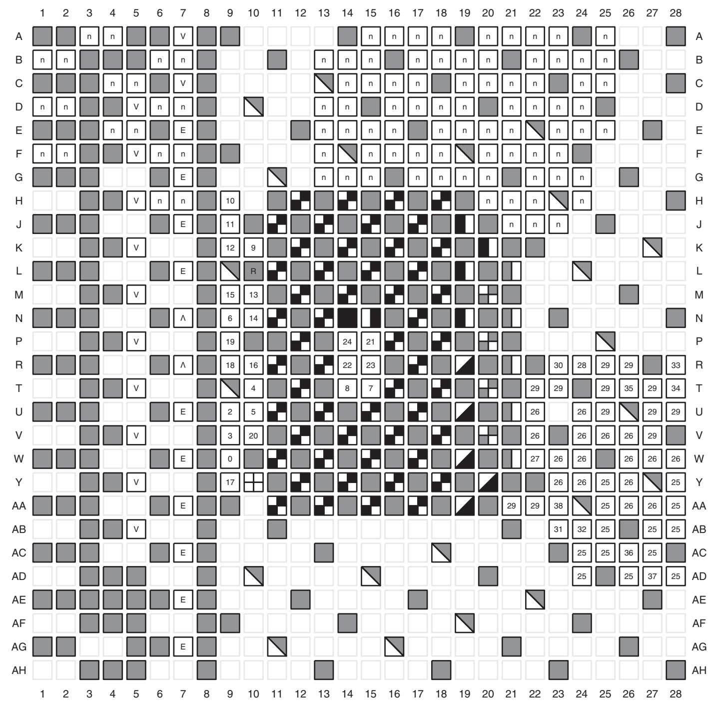


Figure 3-93: **SFVB784 Package—XCAU20P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-94: **SFVB784 Package—XCAU20P Configuration/Power Diagram**

SFVB784 (XCAU25P)

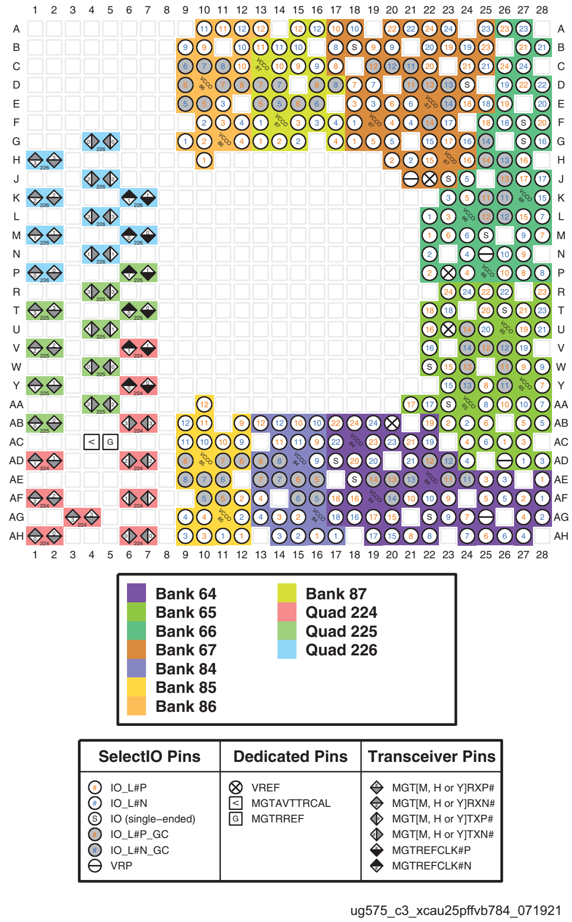
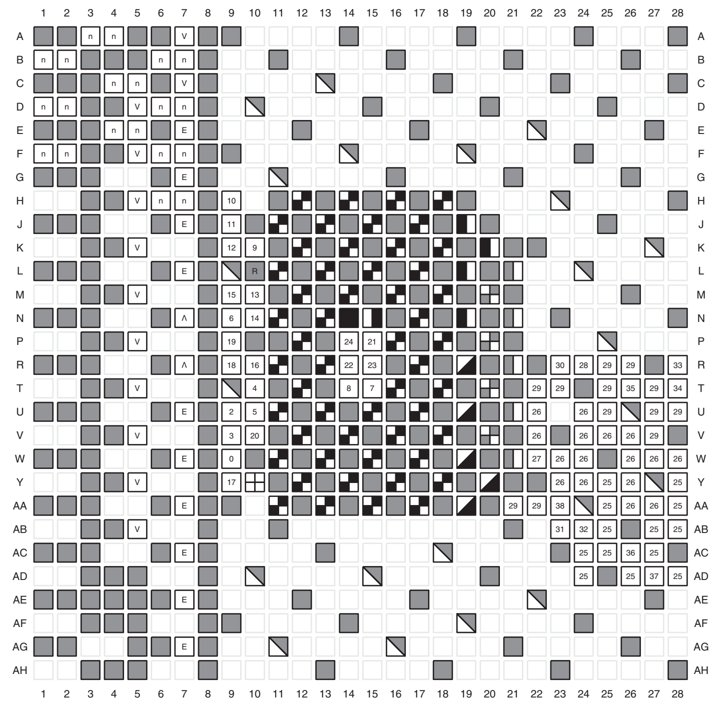


Figure 3-95: **SFVB784 Package—XCAU25P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-96: **SFVB784 Package—XCAU25P Configuration/Power Diagram**

UBVA368 (XCAU10P)

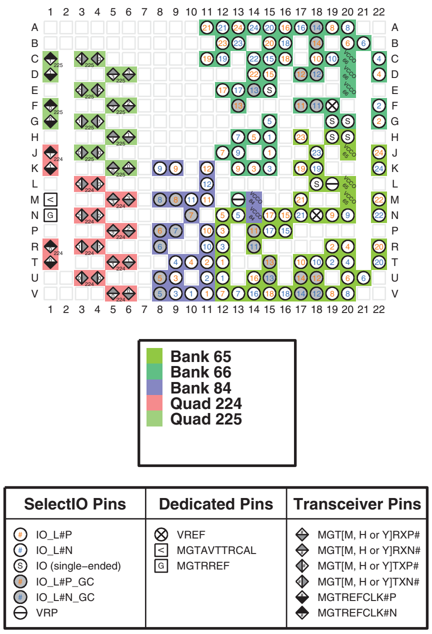


Figure 3-97: **UBVA368 Package—XCAU10P I/O Bank Diagram**

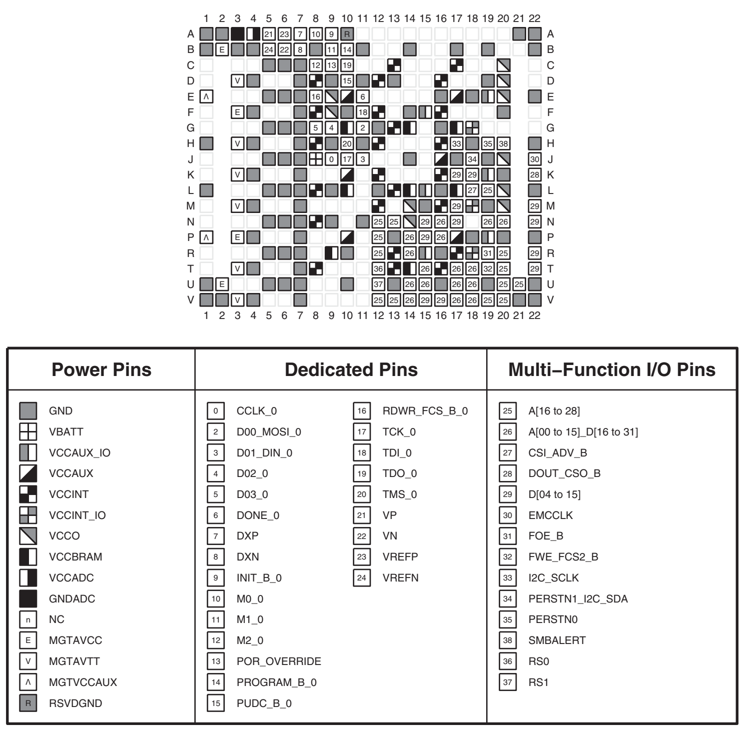


Figure 3-98: **UBVA368 Package— XCAU10P Configuration/Power Diagram**

UBVA368 (XCAU15P)

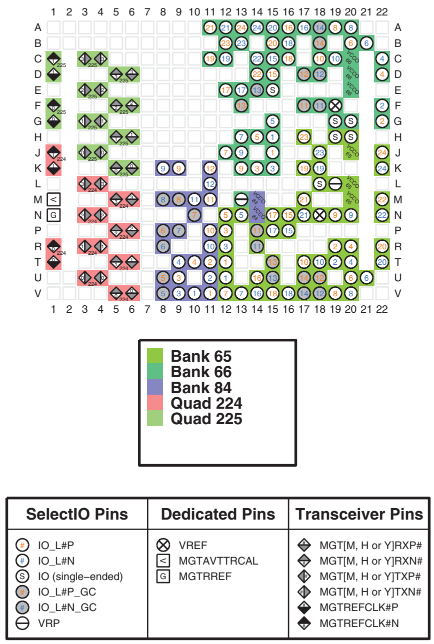


Figure 3-99: **UBVA368 Package—XCAU15P I/O Bank Diagram**

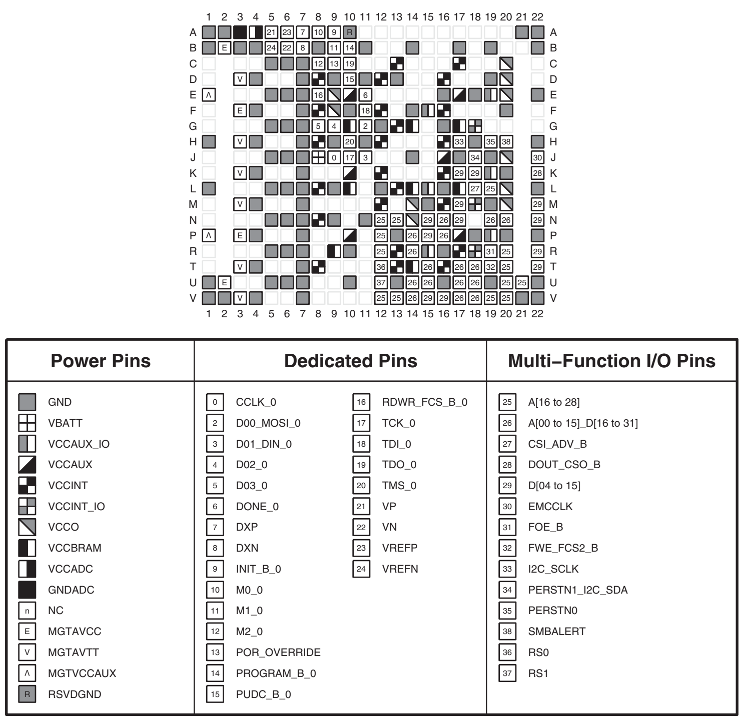


Figure 3-100: **UBVA368 Package— XCAU15P Configuration/Power Diagram**

FFVA676 (XCKU3P and XCKU5P)

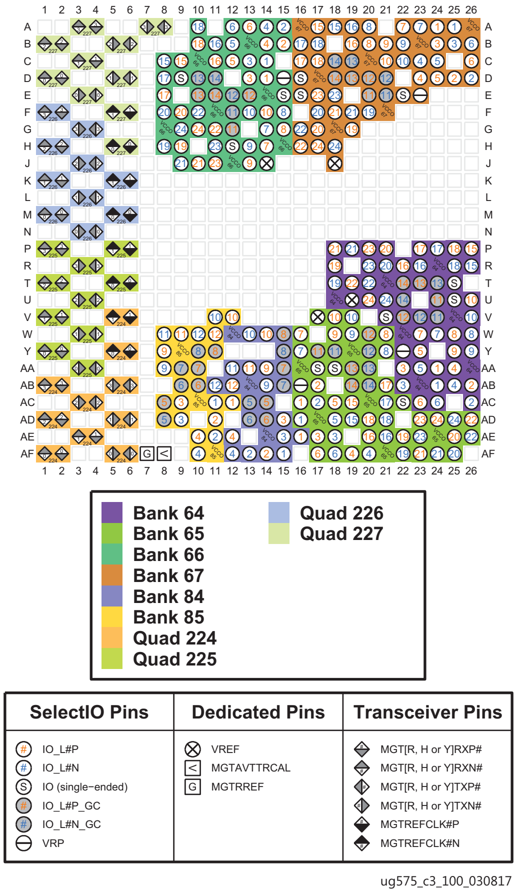


Figure 3-101: **FFVA676 Package—XCKU3P and XCKU5P I/O Bank Diagram**

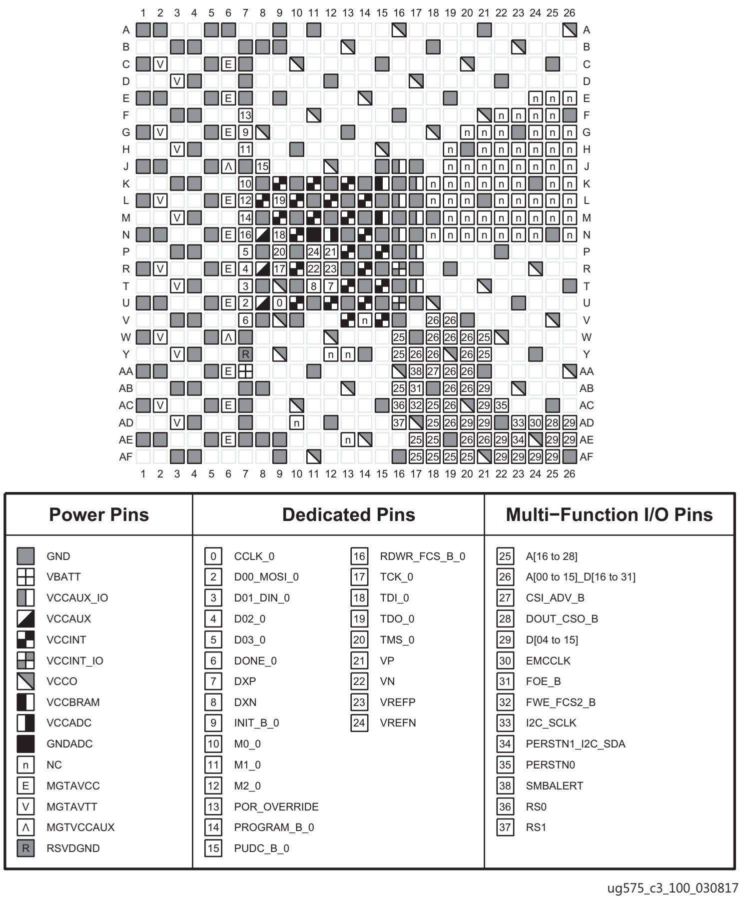


Figure 3-102: **FFVA676 Package—XCKU3P and XCKU5P Configuration/Power Diagram**

FFVB676 (XCKU3P and XCKU5P) and FFRB676 (XQKU5P)

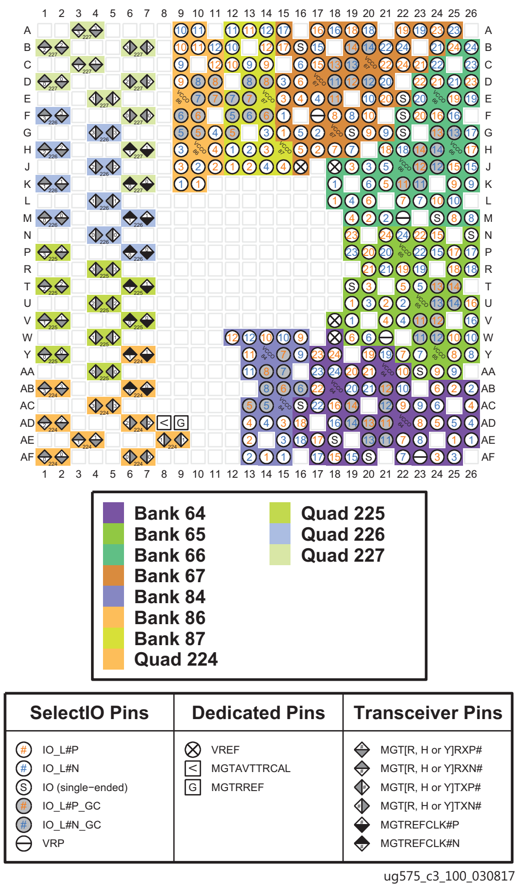
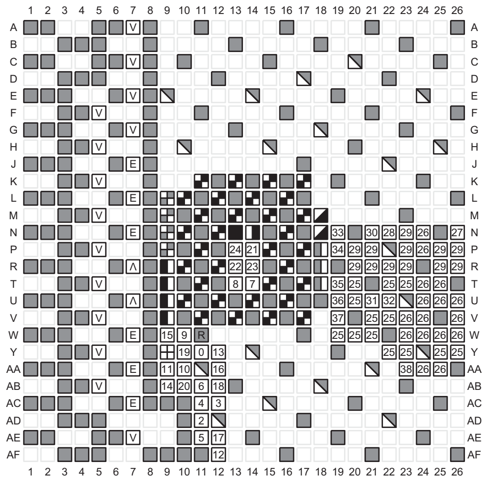


Figure 3-103: **FFVB676 Package—XCKU3P and XCKU5P and FFRB676 Package—XQKU5P I/O Bank Diagram**

Note: VCCAUX_IO pins for the XQ versions of these devices in these packages are split into VCCAUX_HPIO and VCCAUX_HDIO. Refer to the package files for VCCAUX_HPIO and VCCAUX_HDIO pin locations.



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-104: **FFVB676 Package—XCKU3P and XCKU5P and FFRB676 Package—XQKU5P Configuration/Power Diagram**

SFVB784 (XCKU3P and XCKU5P) and SFRB784 (XQKU5P)

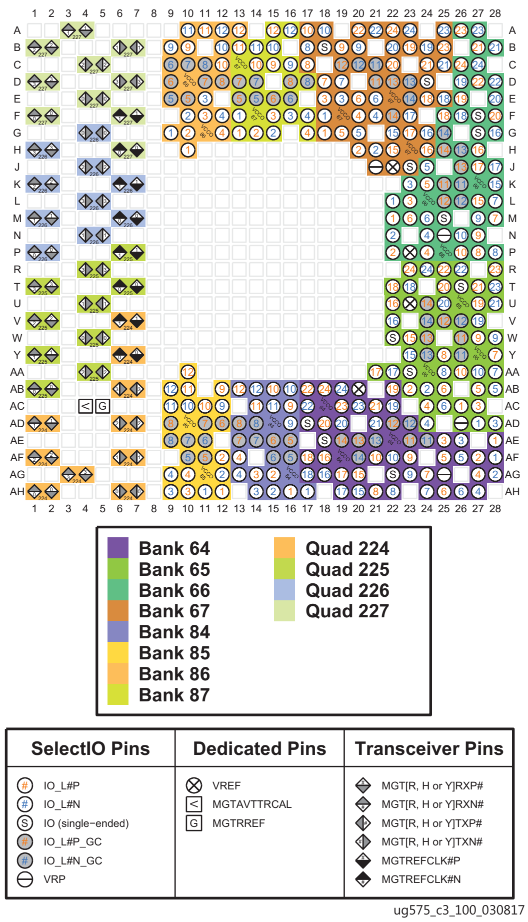
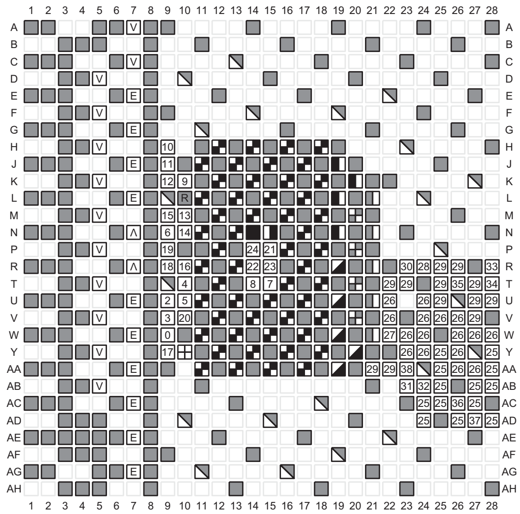


Figure 3-105: **SFVB784 Package—XCKU3P and XCKU5P and SFRB784 Package—XQKU5P I/O Bank Diagram**

Note: VCCAUX_IO pins for the XQ versions of these devices in this package are split into VCCAUX_HPIO and VCCAUX_HDIO. Refer to the package files for VCCAUX_HPIO and VCCAUX_HDIO pin locations.



Power Pins	Dedicated Pins		Multi−Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-106: **SFVB784 Package—XCKU3P and XCKU5P and SFRB784 Package—XQKU5P Configuration/Power Diagram**

FFVD900 (XCKU3P and XCKU5P)

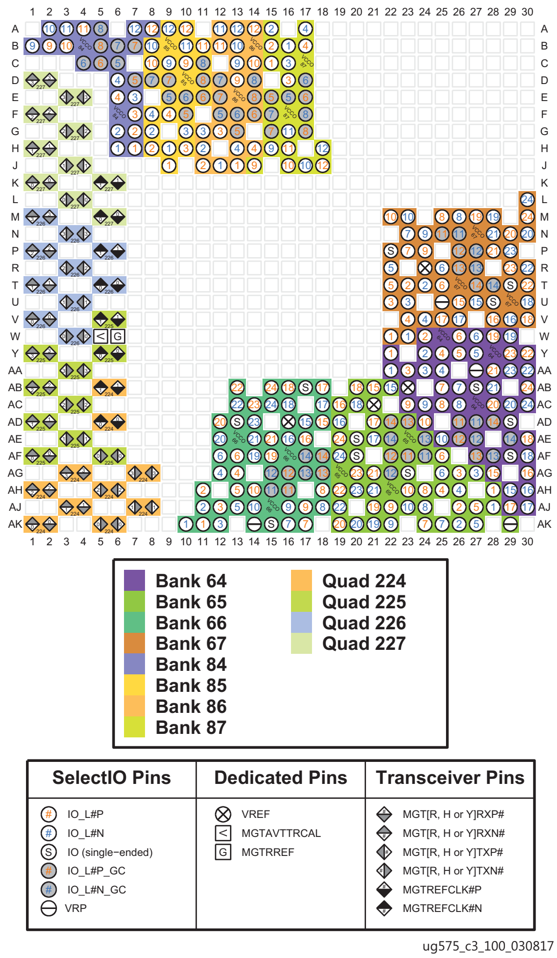
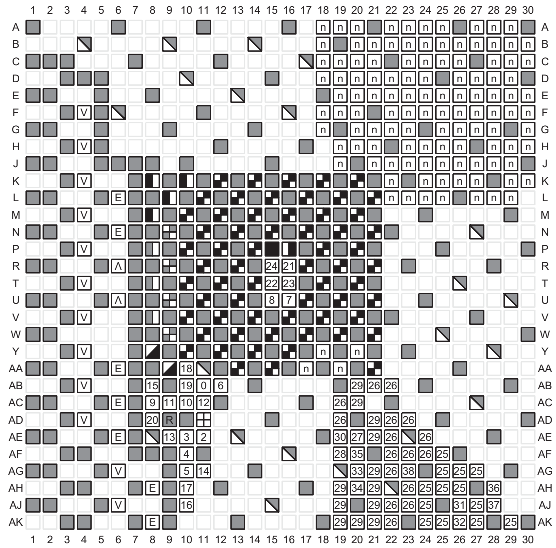


Figure 3-107: **FFVD900 Package—XCKU3P and XCKU5P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-108: **FFVD900 Package—XCKU3P and XCKU5P Configuration/Power Diagram**

FFVD900 (XCKU11P)

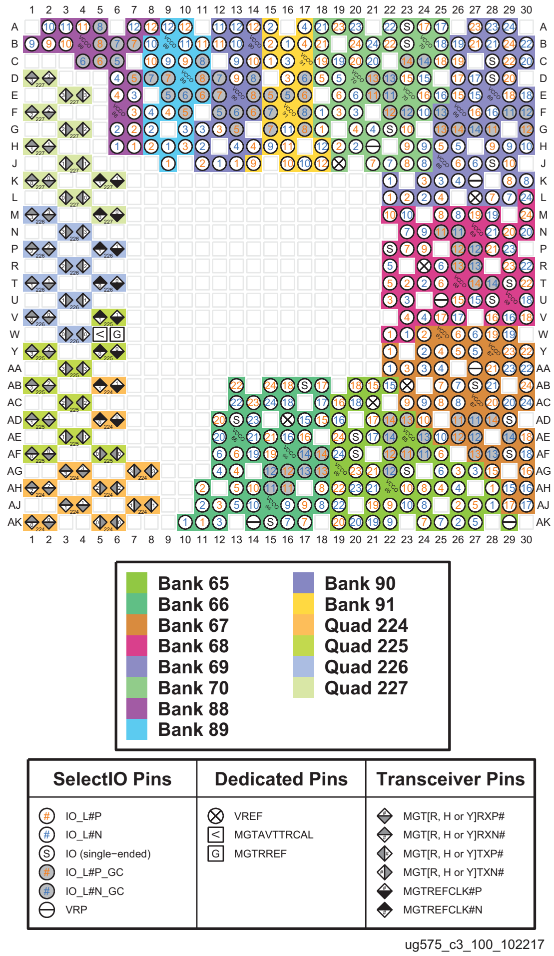


Figure 3-109: **FFVD900 Package—XCKU11P I/O Bank Diagram**

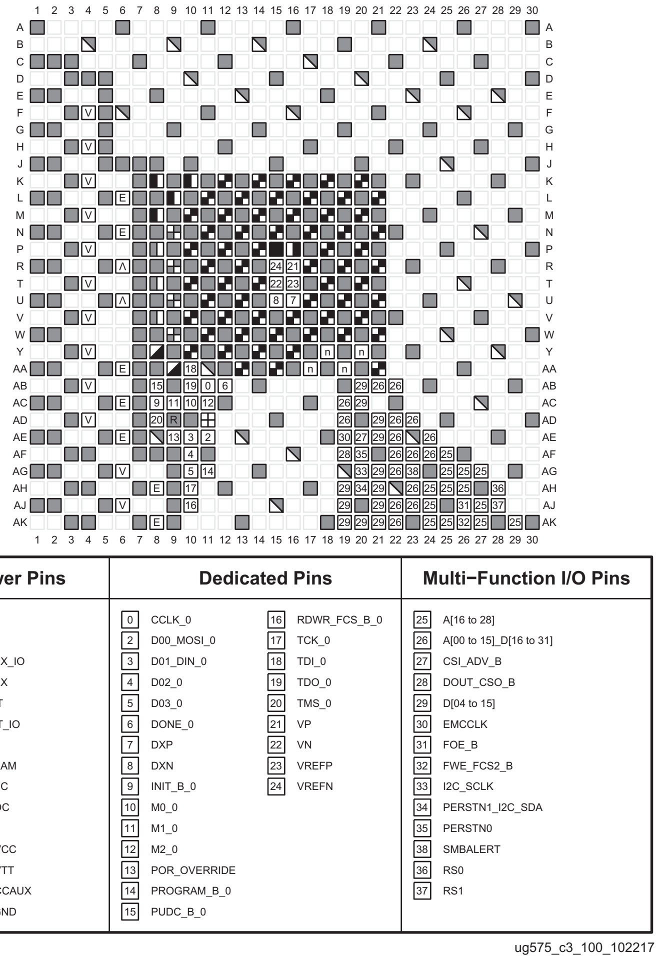


Figure 3-110: **FFVD900 Package—XCKU11P Configuration/Power Diagram**

FFVE900 (XCKU9P)

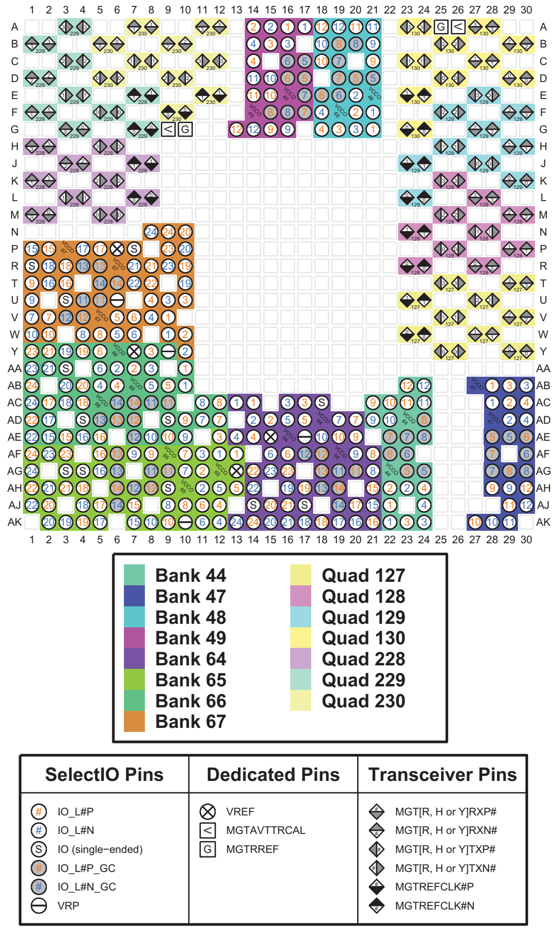


Figure 3-111: **FFVE900 Package—XCKU9P I/O Bank Diagram**

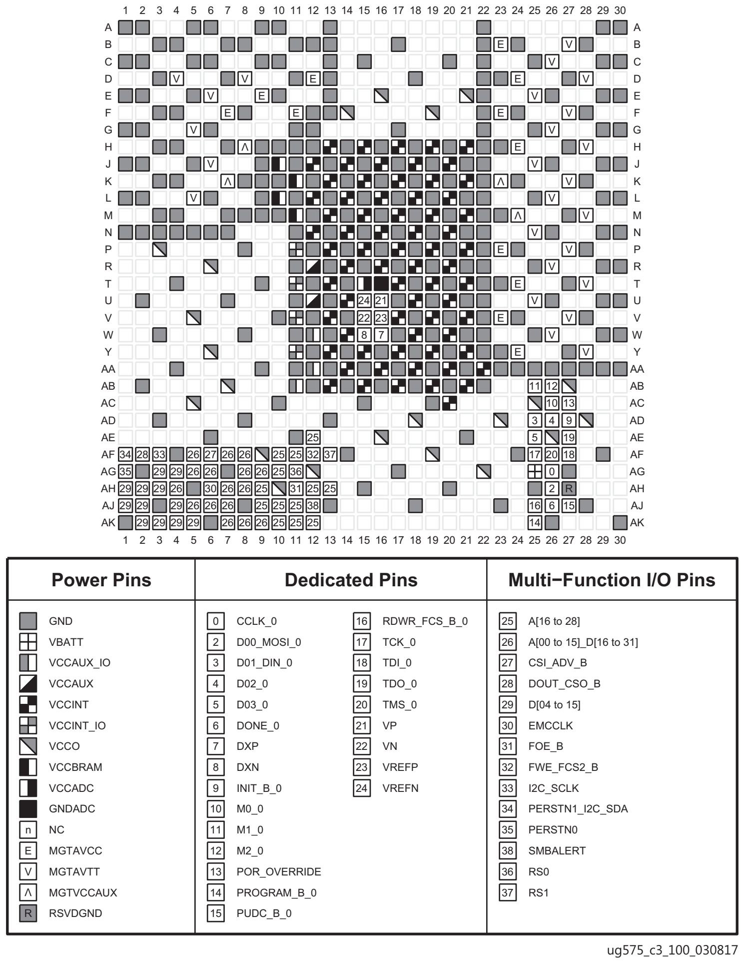


Figure 3-112: **FFVE900 Package—XCKU9P Configuration/Power Diagram**

FFVE900 (XCKU13P)

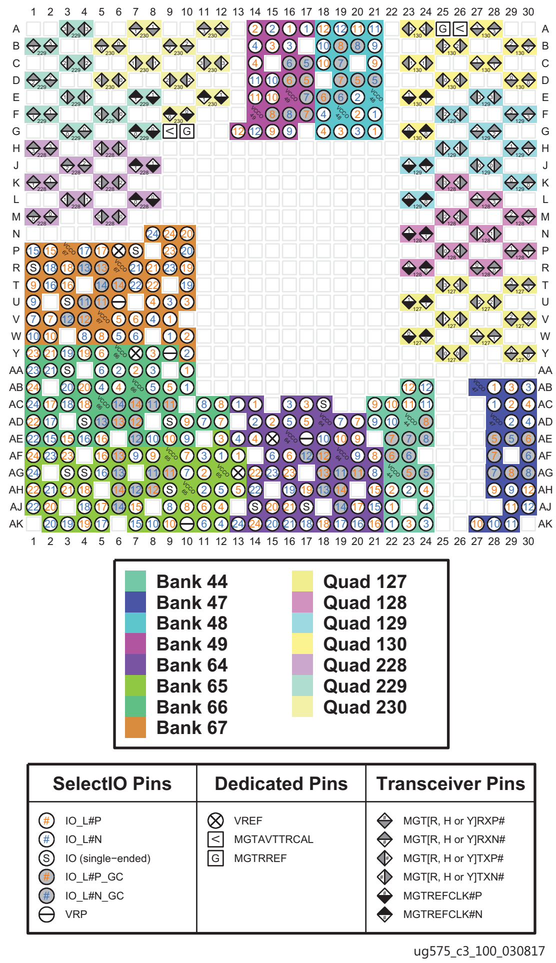


Figure 3-113: **FFVE900 Package—XCKU13P I/O Bank Diagram**

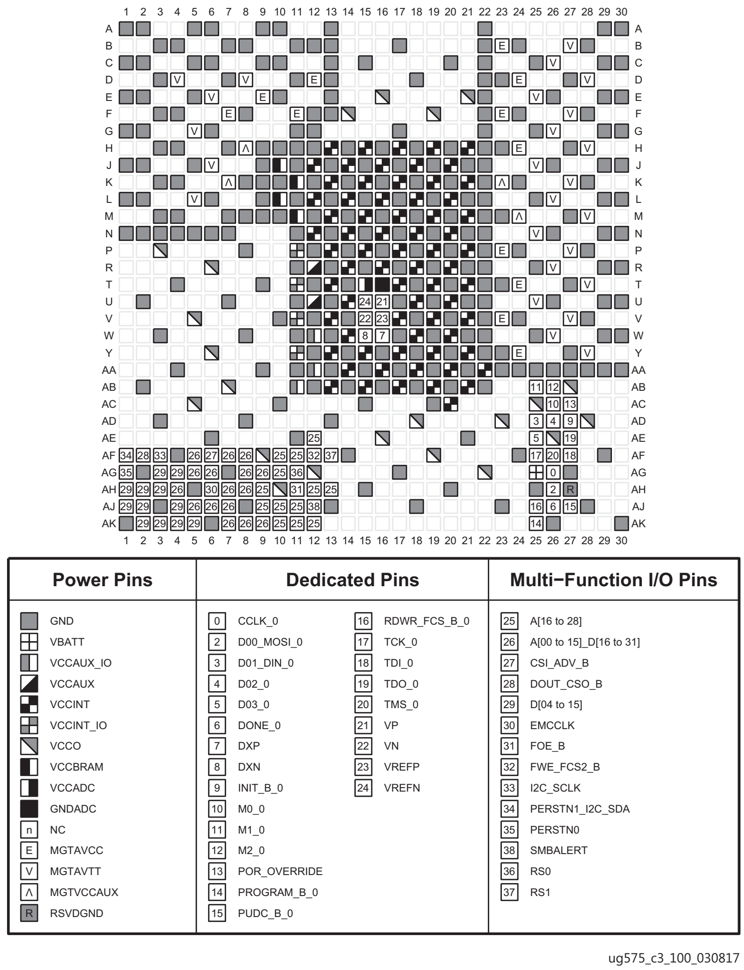


Figure 3-114: **FFVE900 Package—XCKU13P Configuration/Power Diagram**

FFVA1156 (XCKU11P)

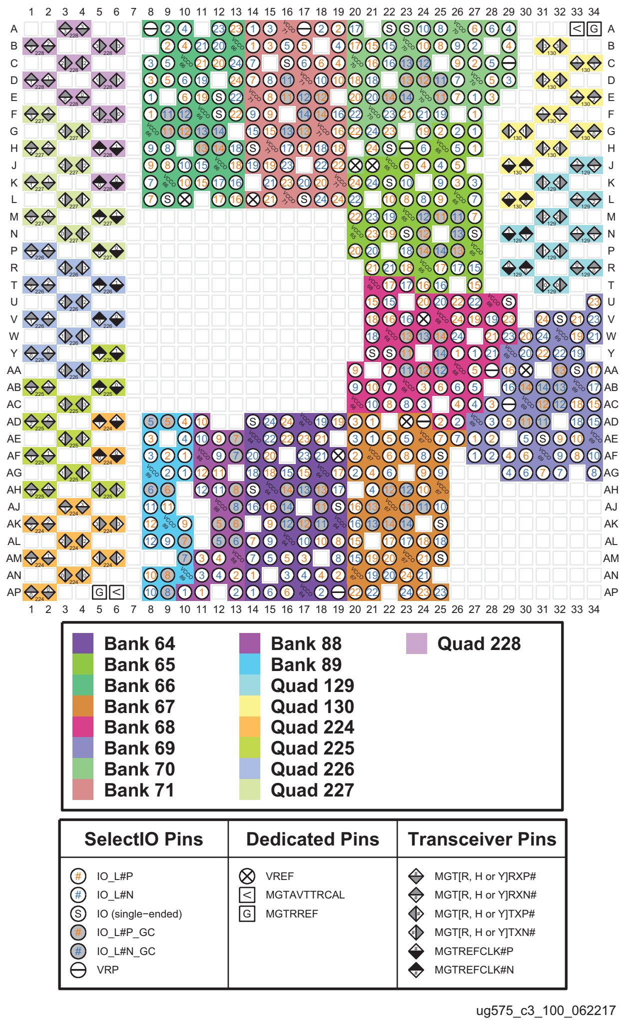


Figure 3-115: **FFVA1156 Package—XCKU11P I/O Bank Diagram**

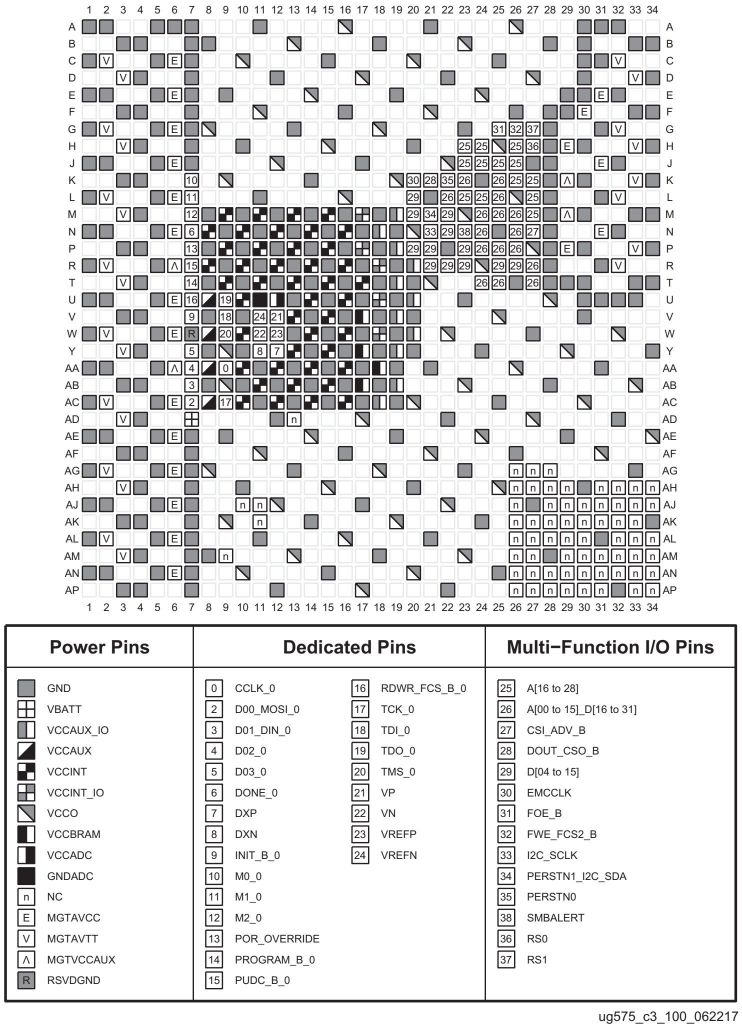


Figure 3-116: **FFVA1156 Package—XCKU11P Configuration/Power Diagram**

FFVA1156 (XCKU15P) and FFRA1156 (XQKU15P)

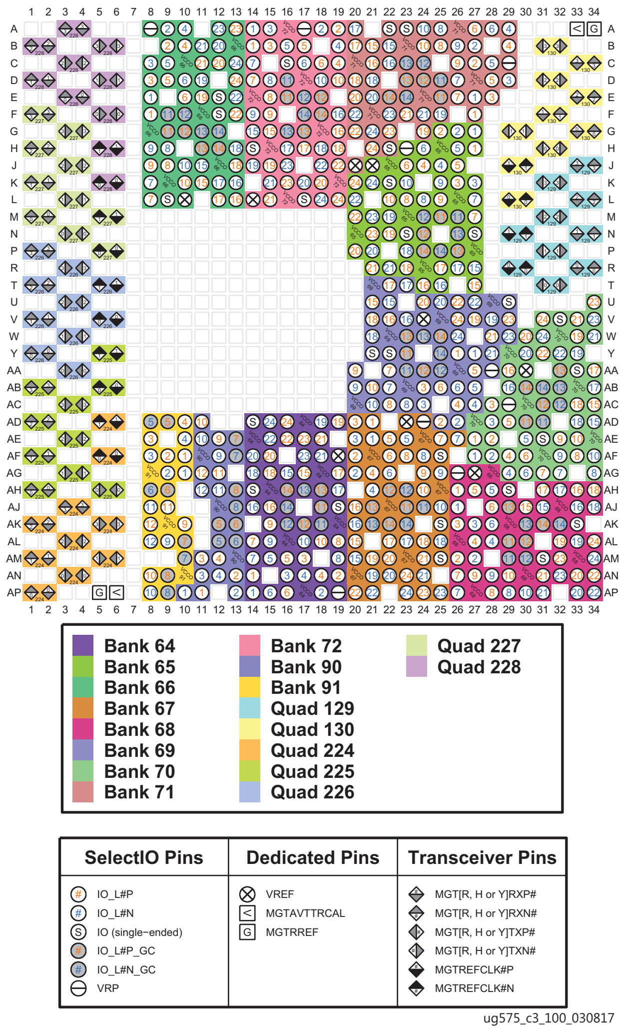
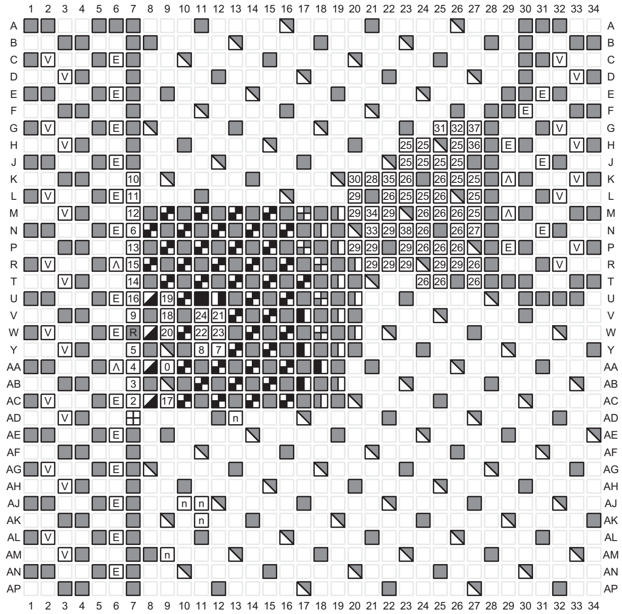


Figure 3-117: **FFVA1156 Package—XCKU15P and FFRA1156 Package—XQKU15P I/O Bank Diagram**

Note: VCCAUX_IO pins for the XQ versions of this device in this package are split into VCCAUX_HPIO and VCCAUX_HDIO. Refer to the package files for VCCAUX_HPIO and VCCAUX_HDIO pin locations.



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-118: **FFVA1156 Package—XCKU15P and FFRA1156 Package—XQKU15P Configuration/Power Diagram**

FFVE1517 (XCKU11P)

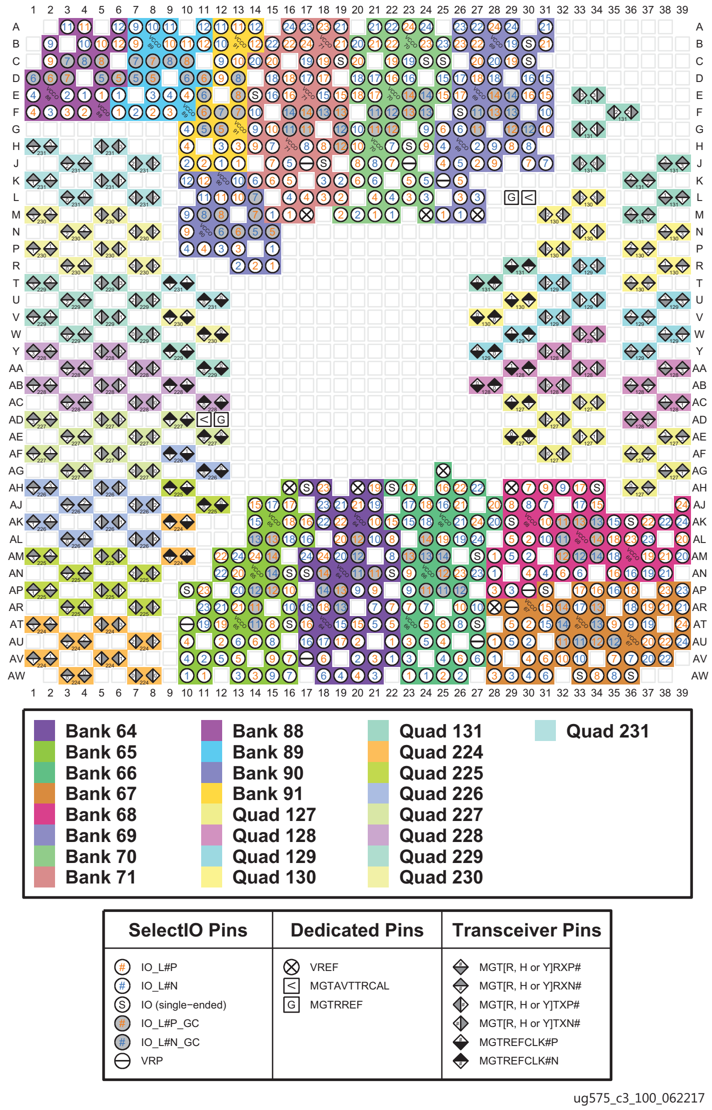


Figure 3-119: **FFVE1517 Package—XCKU11P I/O Bank Diagram**

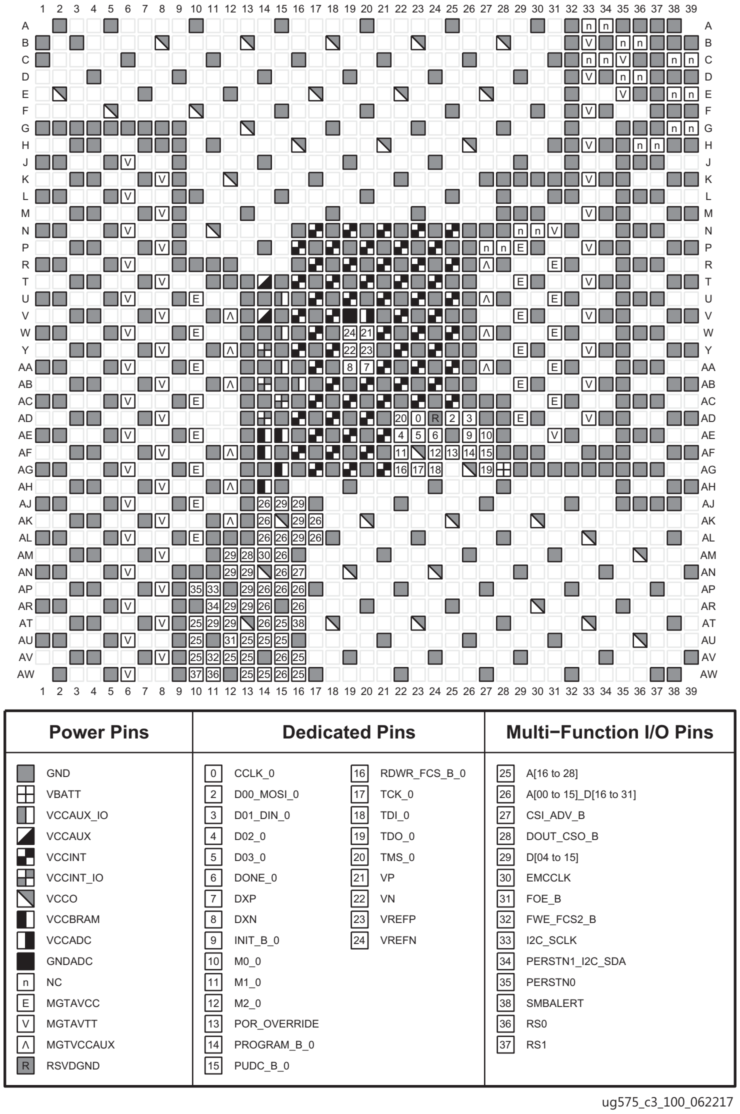


Figure 3-120: **FFVE1517 Package—XCKU11P Configuration/Power Diagram**

FFVE1517 (XCKU15P) and FFRE1517 (XQKU15P)

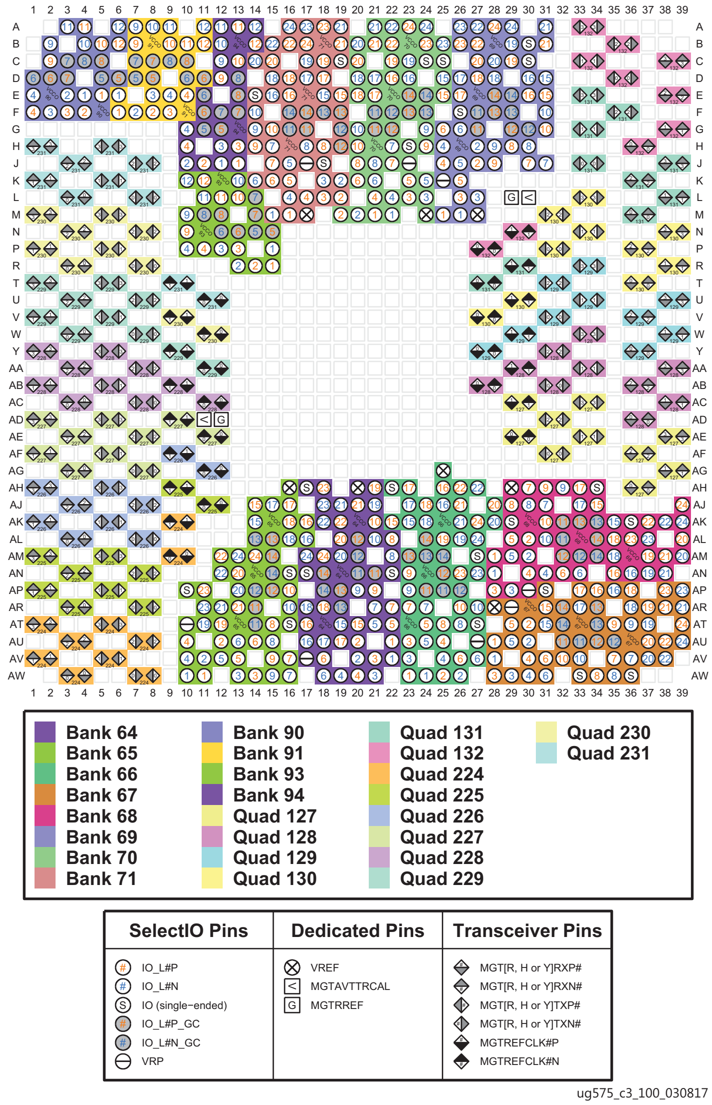


Figure 3-121: **FFVE1517 Package—XCKU15P and FFRE1517 Package—XQKU15P I/O Bank Diagram**

Note: VCCAUX_IO pins for the XQ versions of these devices in these packages are split into VCCAUX_HPIO and VCCAUX_HDIO. Refer to the package files for VCCAUX_HPIO and VCCAUX_HDIO pin locations.

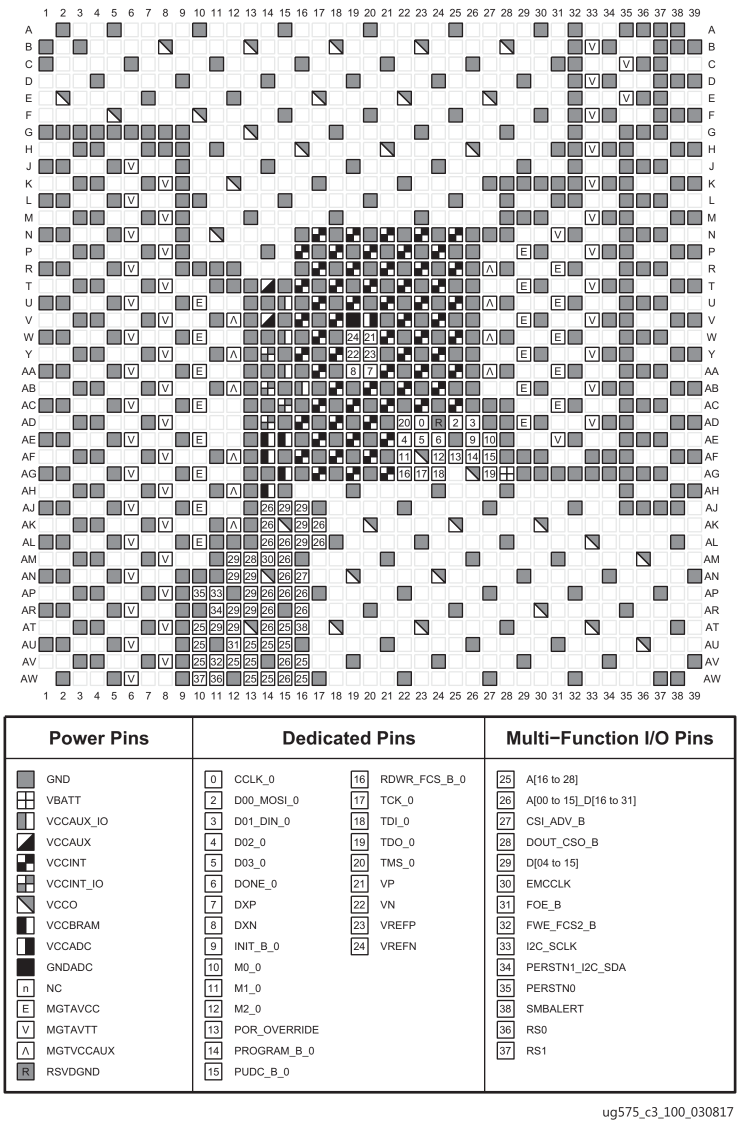


Figure 3-122: **FFVE1517 Package—XCKU15P and FFRE1517 Package—XQKU15P Configuration/Power Diagram**

FFVA1760 (XCKU15P)

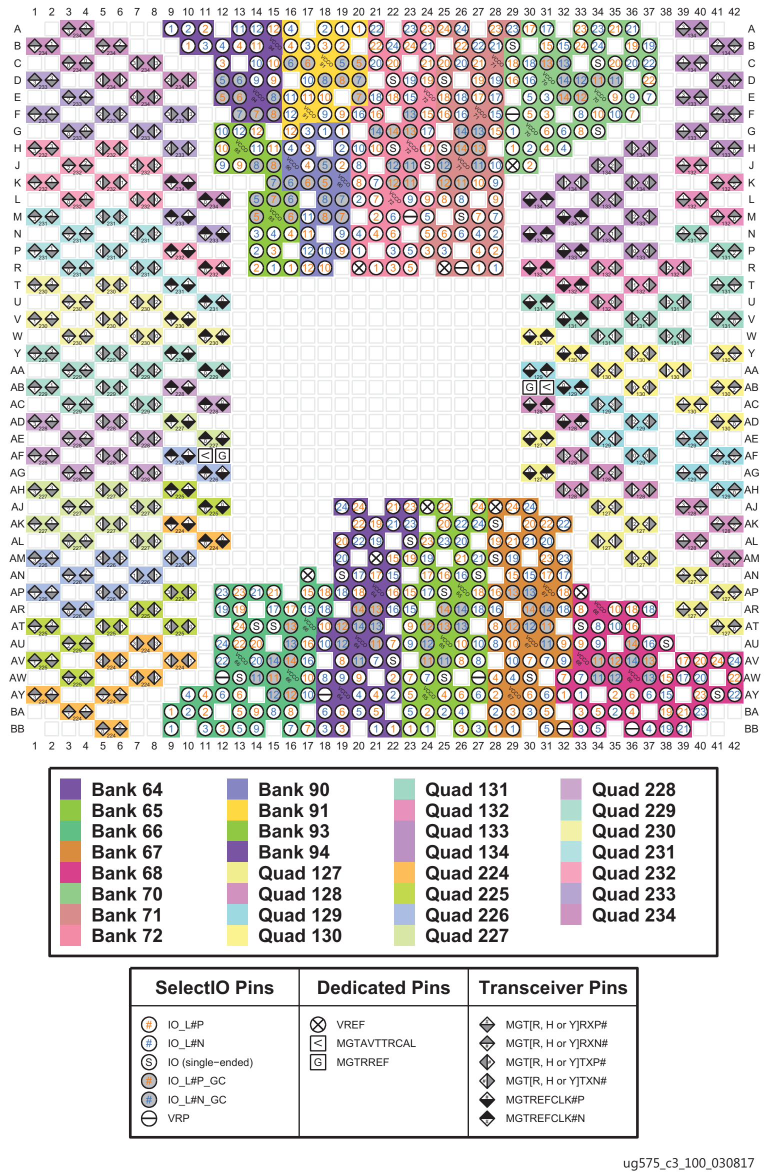


Figure 3-123: **FFVA1760 Package—XCKU15P I/O Bank Diagram**

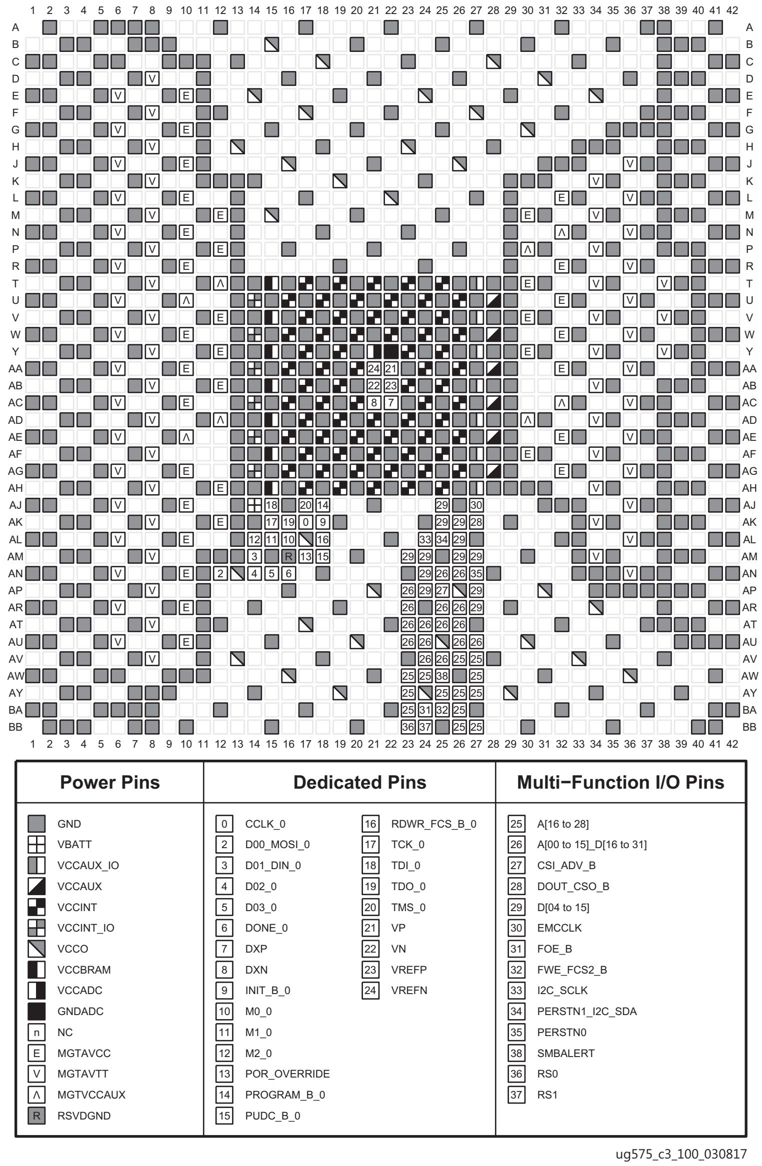


Figure 3-124: **FFVA1760 Package—XCKU15P Configuration/Power Diagram**

FFVE1760 (XCKU15P)

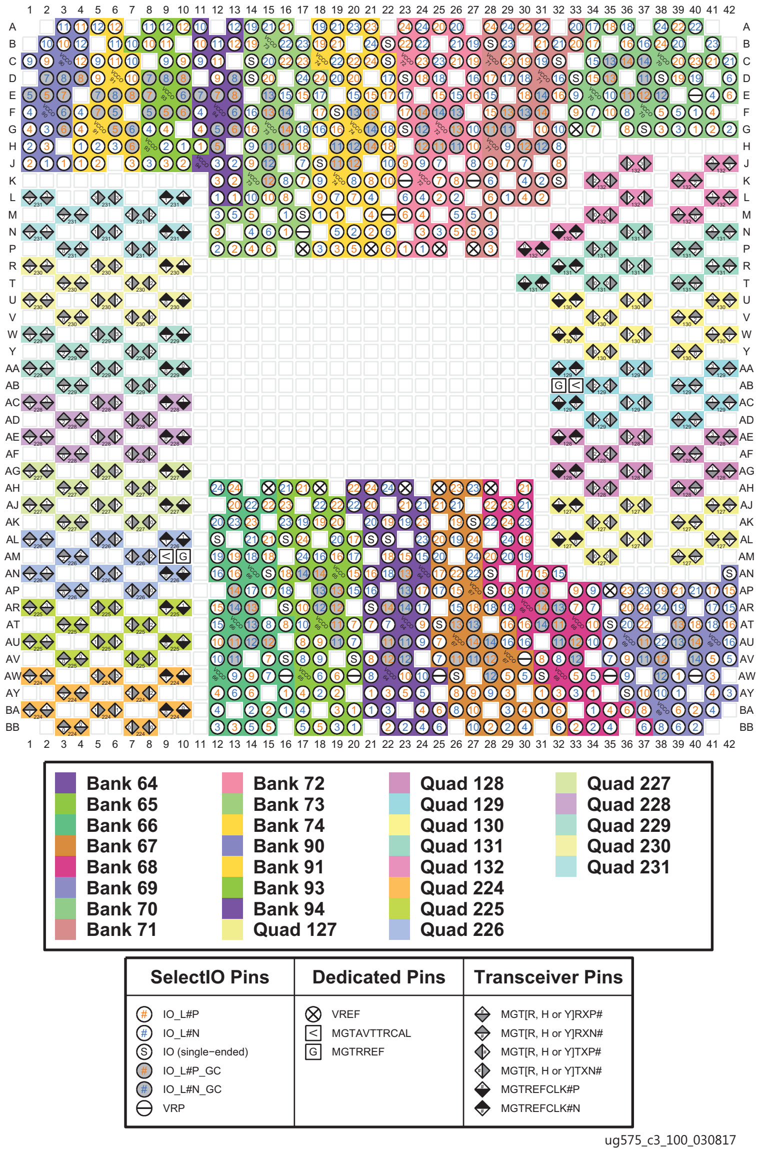


Figure 3-125: **FFVE1760 Package—XCKU15P I/O Bank Diagram**

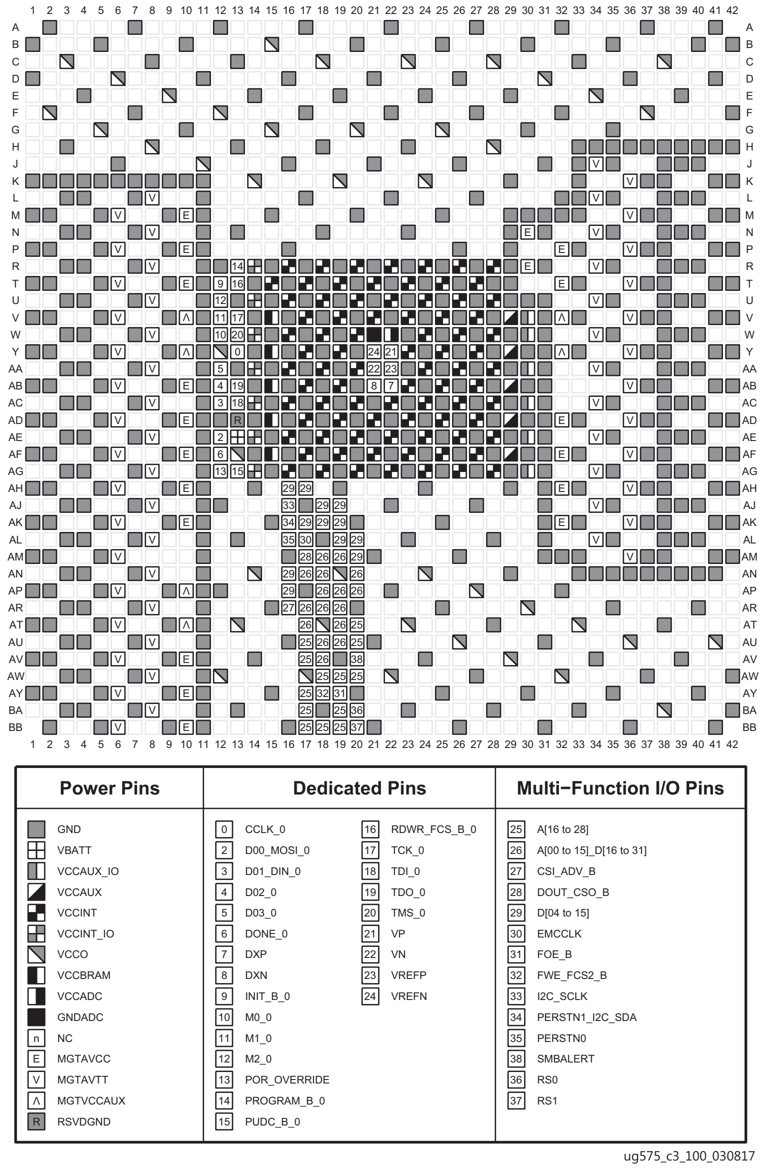


Figure 3-125: **FFVE1760 Package—XCKU15P Configuration/Power Diagram**

FFVJ1760 (XCKU19P)

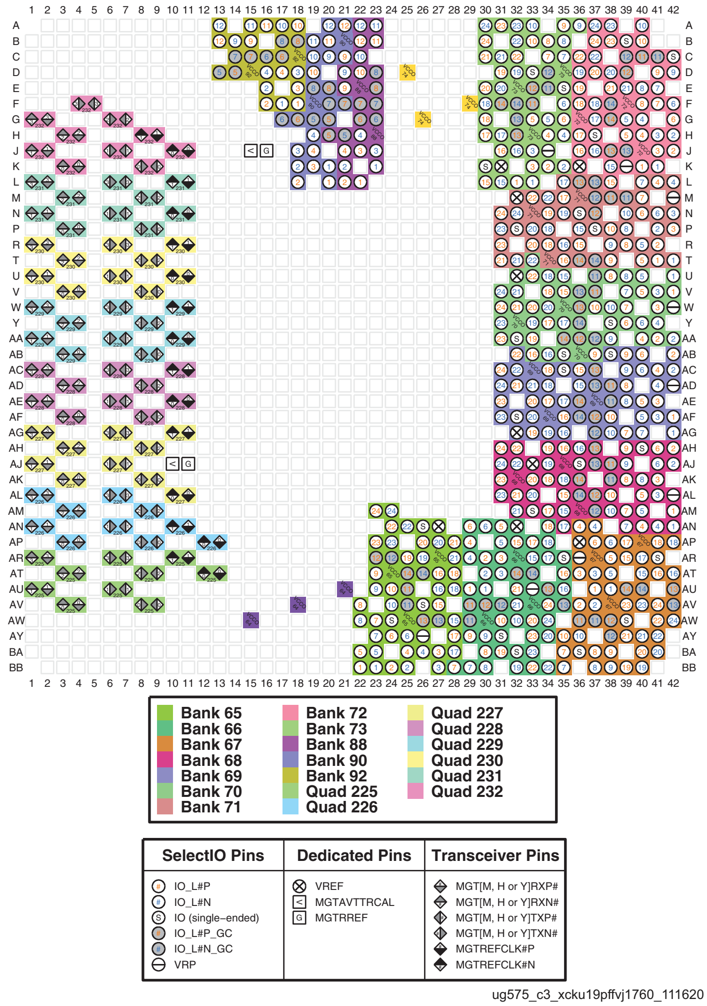


Figure 3-126: **FFVJ1760 Package—XCKU19P I/O Bank Diagram**

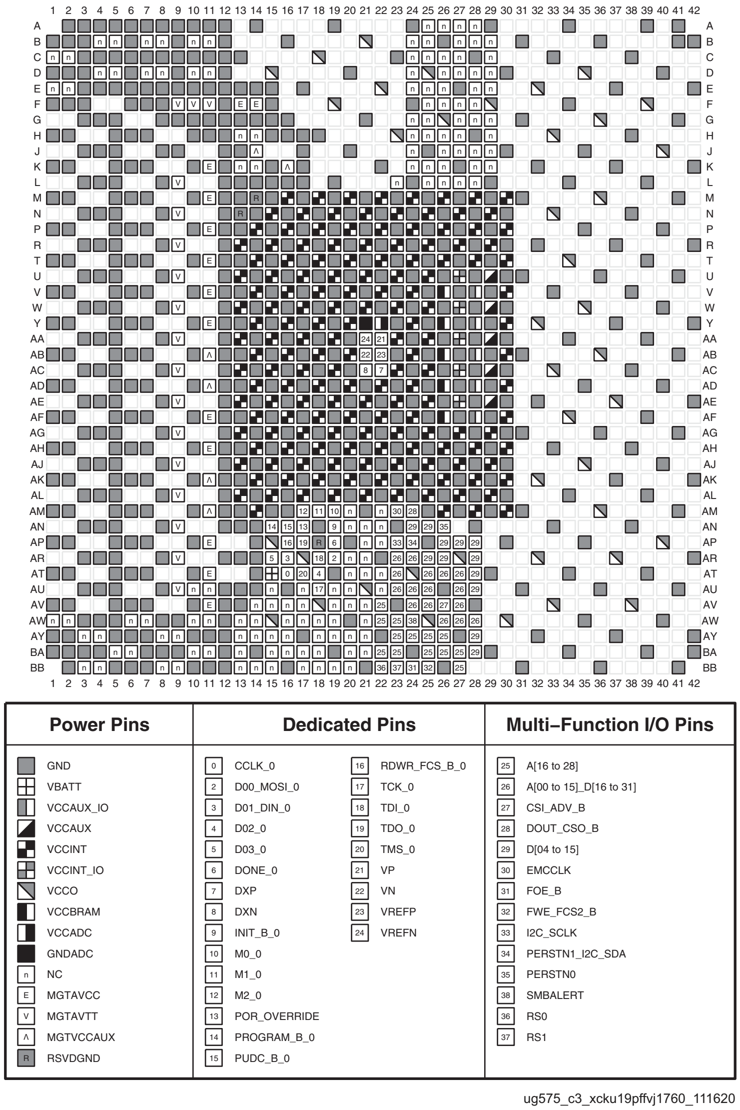


Figure 3-127: **FFVJ1760 Package—XCKU19P Configuration/Power Diagram**

FFVB2104 (XCKU19P)

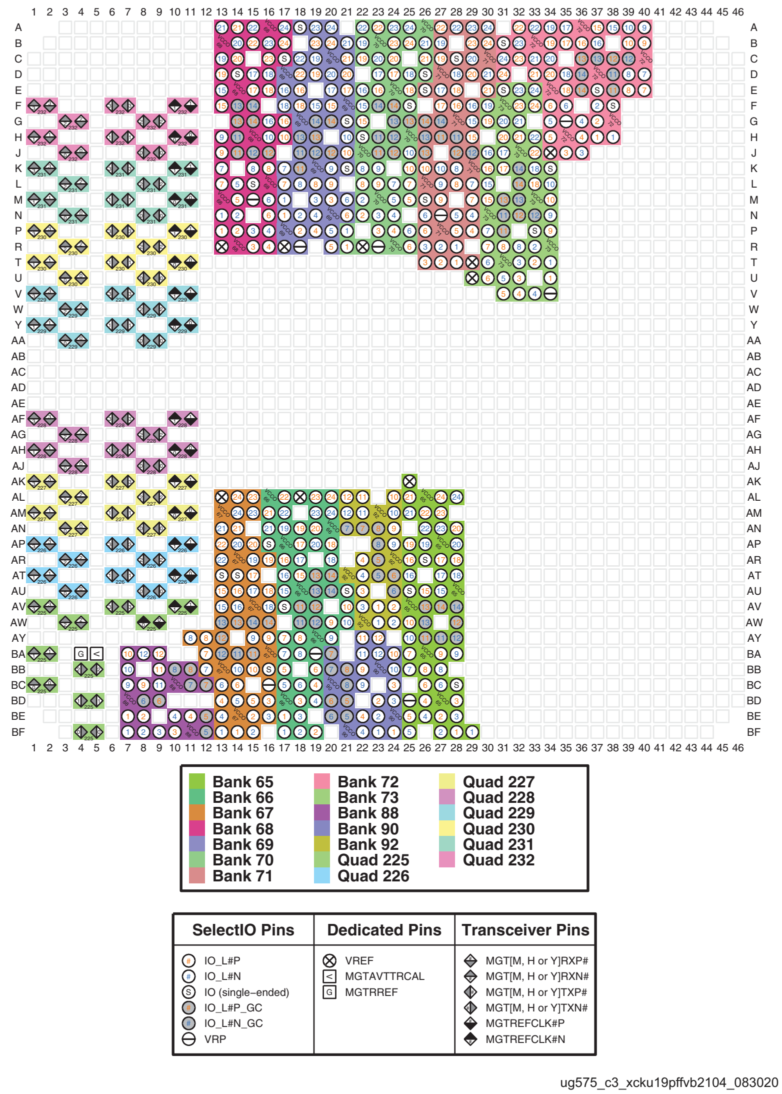


Figure 3-128: **FFVB2104 Package—XCKU19P I/O Bank Diagram**

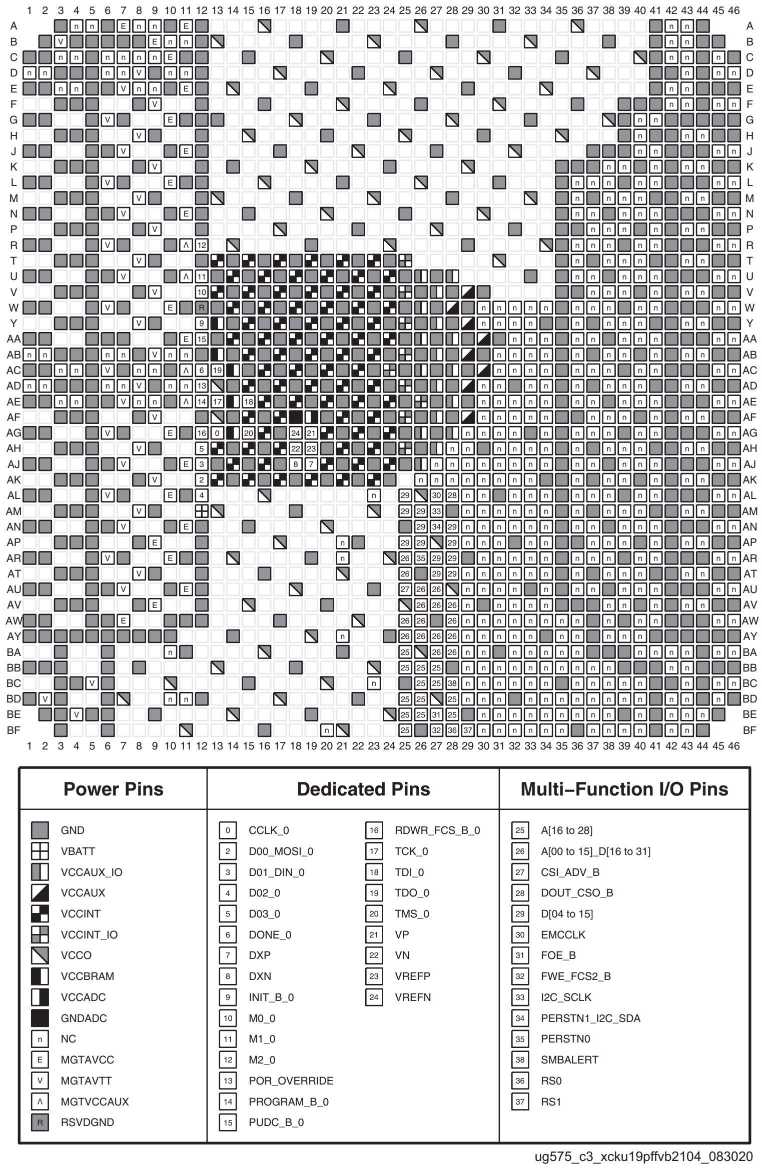


Figure 3-129: **FFVB2104 Package—XCKU19P Configuration/Power Diagram**

FFVC1517 (XCVU3P) and FFRC1517 (XQVU3P)

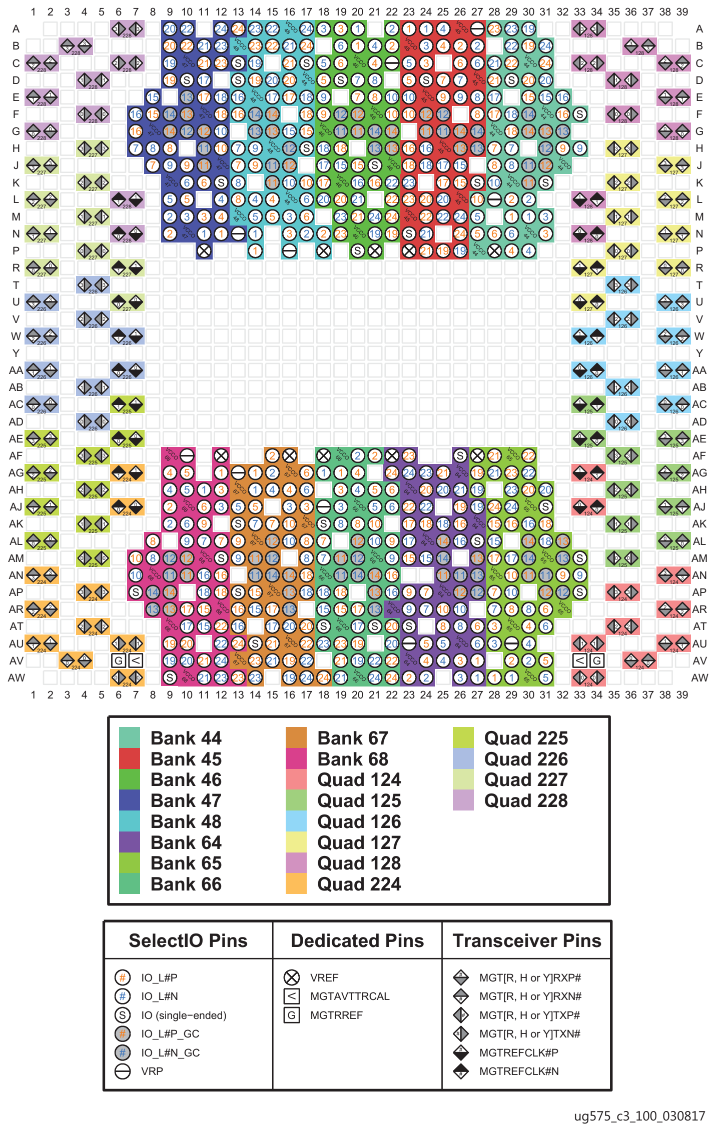


Figure 3-130: **FFVC1517 Package—XCVU3P and FFRC1517 Package—XQVU3P I/O Bank Diagram**

FFVC1517 (XCVU3P) and FFRC1517 (XQVU3P)

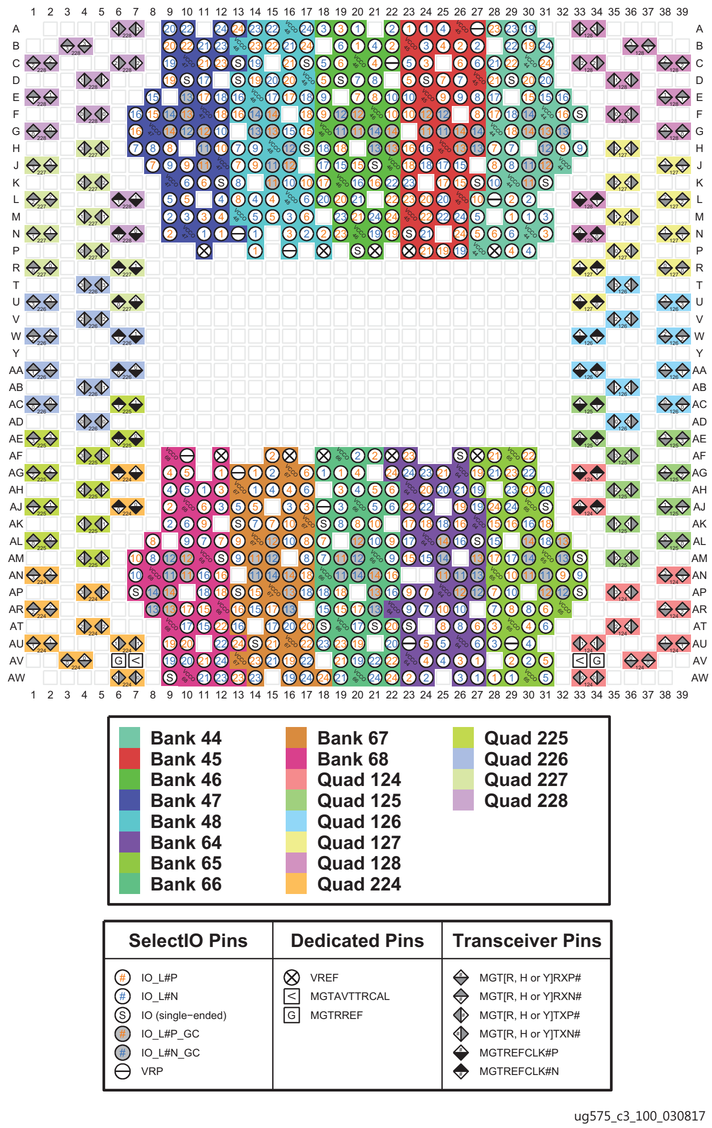


Figure 3-131: **FFVC1517 Package—XCVU3P and FFRC1517 Package—XQVU3P I/O Bank Diagram**

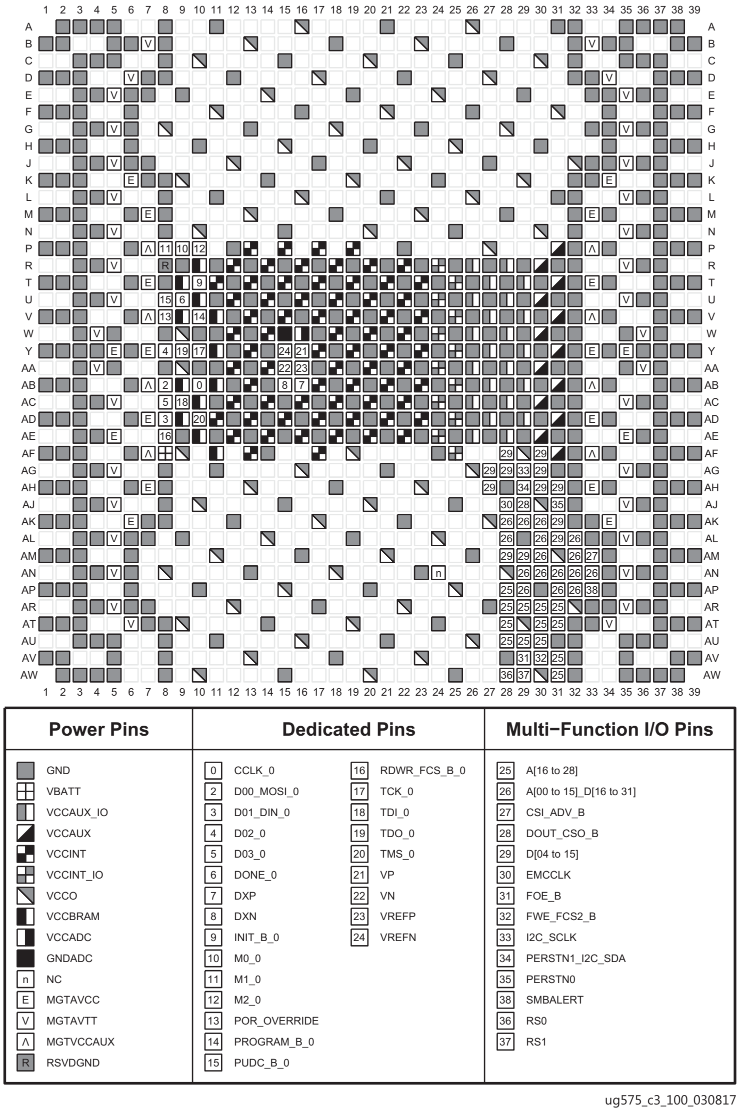


Figure 3-132: **FFVC1517 Package—XCVU3P and FFRC1517 Package—XQVU3P Configuration/Power Diagram**

FSVJ1760 (XCVU23P)

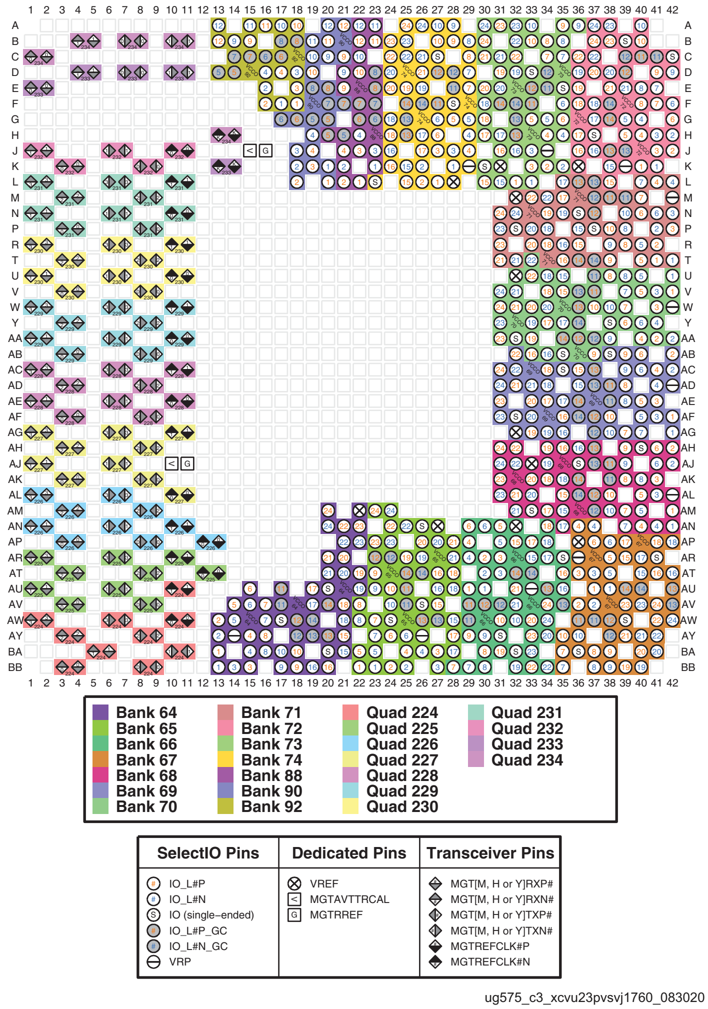


Figure 3-133: **FSVJ1760 Package—XCVU23P I/O Bank Diagram**

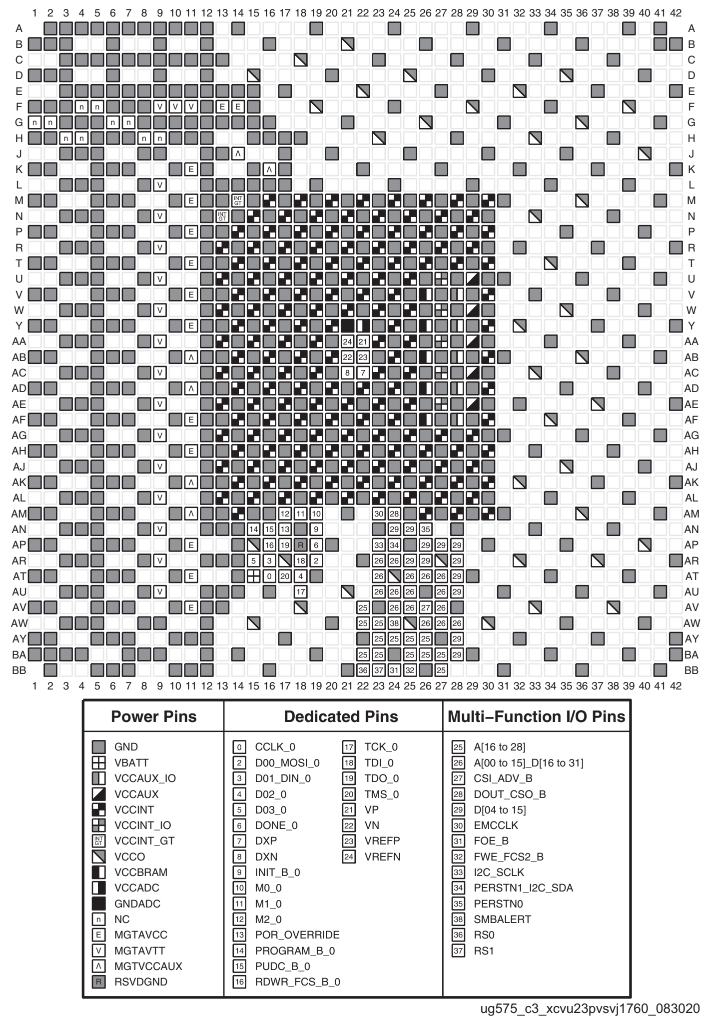


Figure 3-134: **FSVJ1760 Package—XCVU23P Configuration/Power Diagram**

FLGF1924 (XCVU11P)

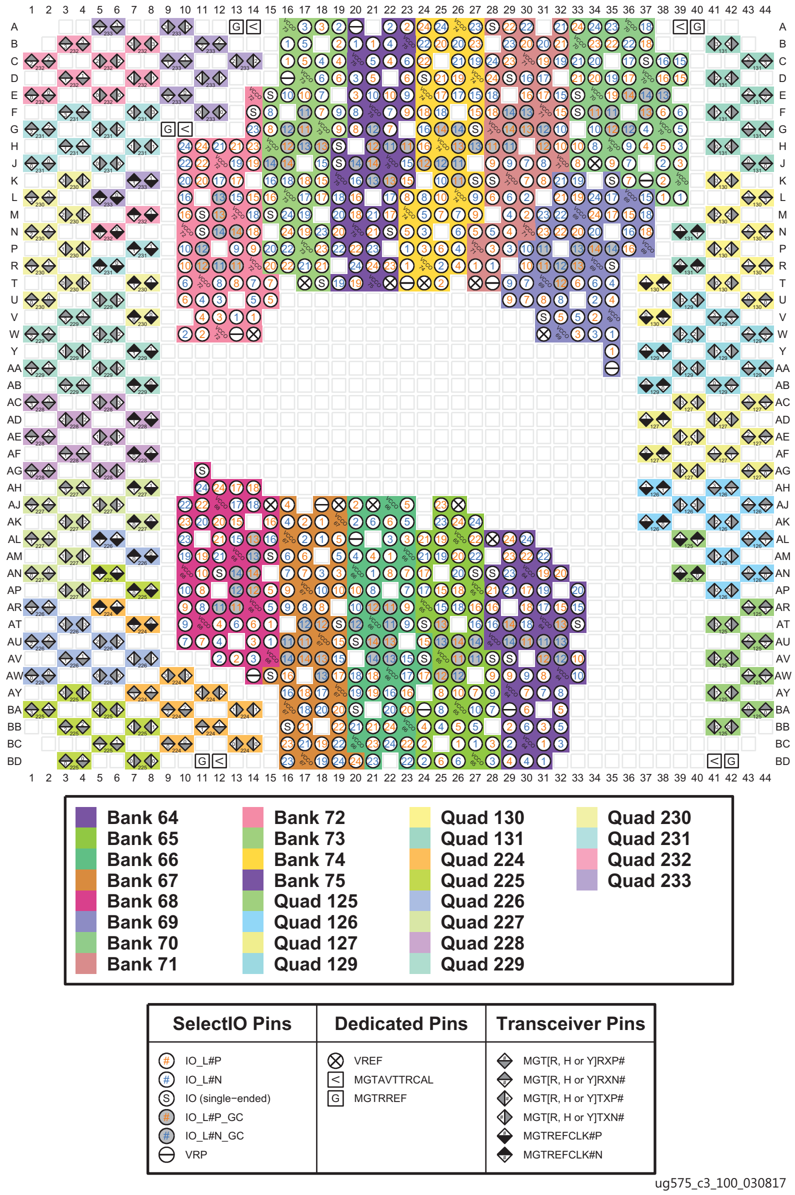


Figure 3-135: **FLGF1924 Package—XCVU11P I/O Bank Diagram**

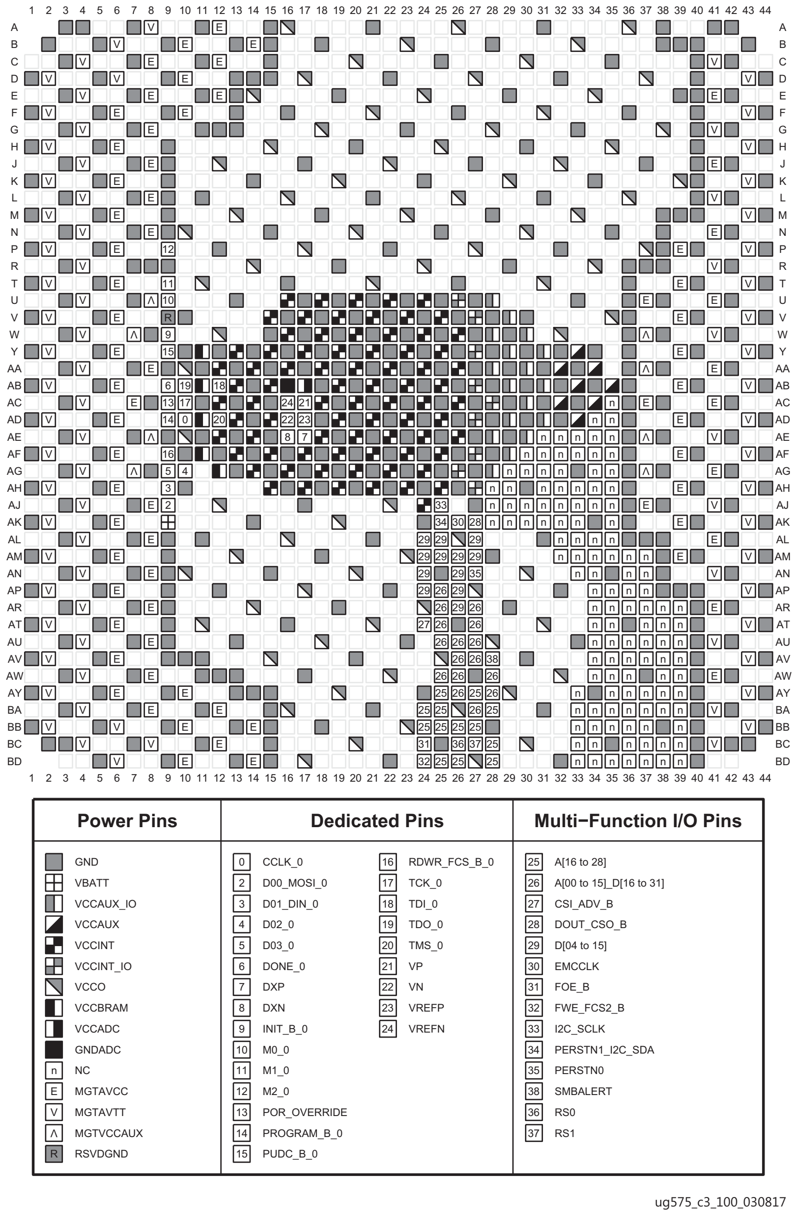


Figure 3-136: **FLGF1924 Package—XCVU11P Configuration/Power Diagram**

FSVH1924 (XCVU31P)

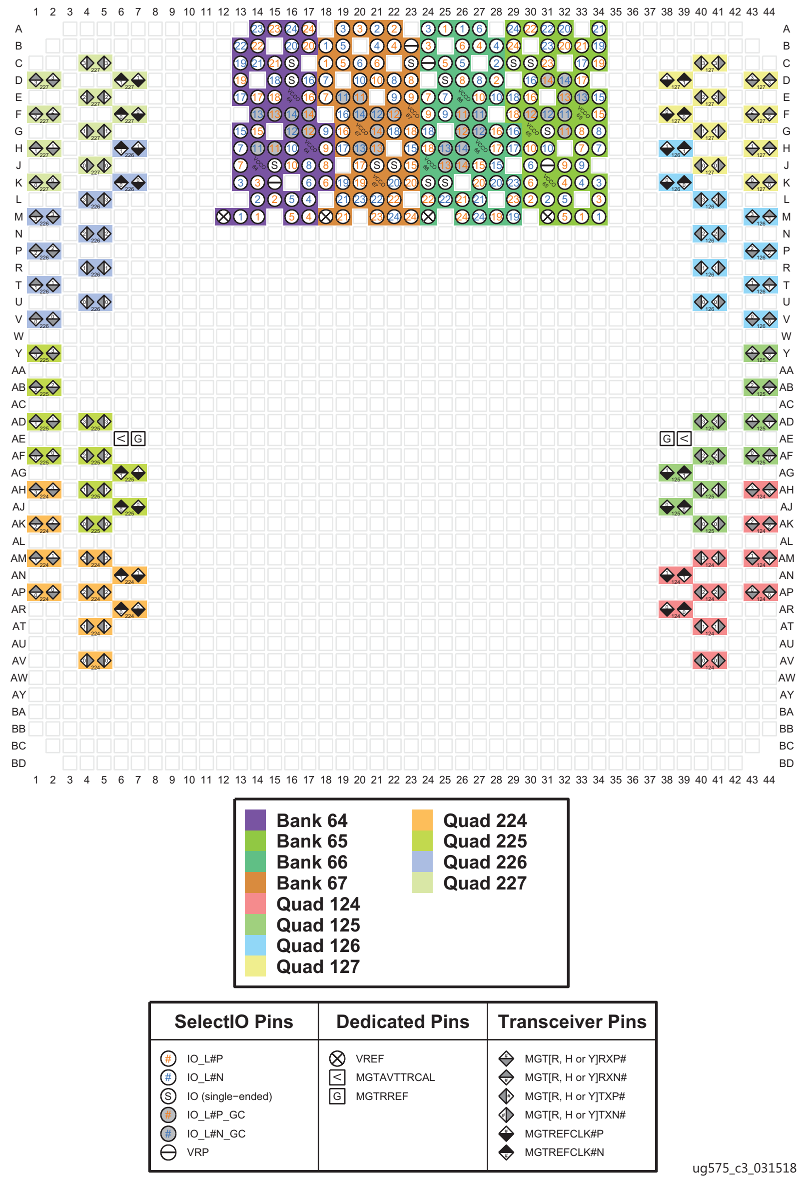
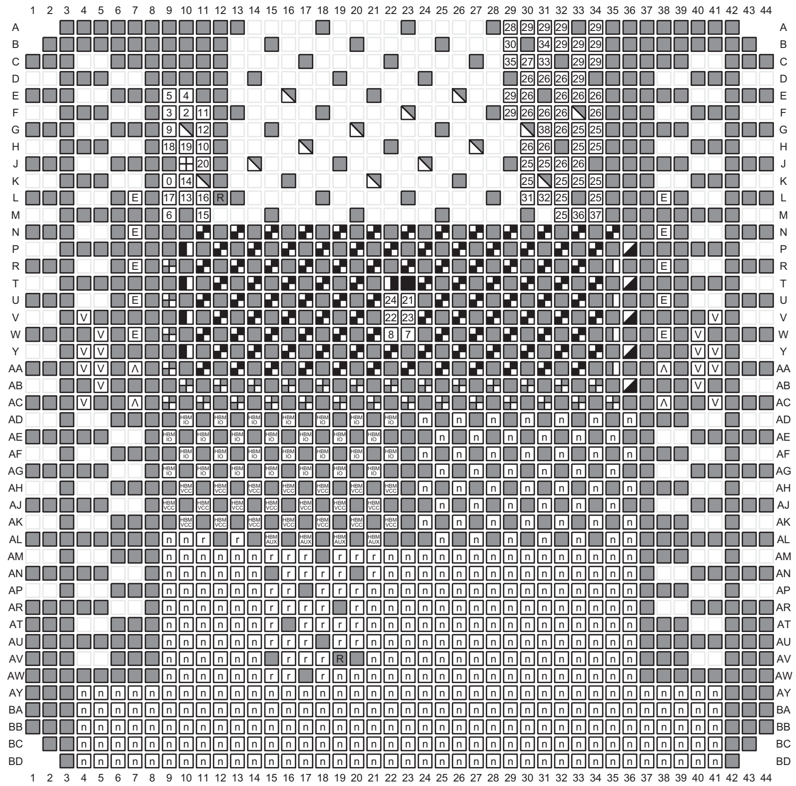


Figure 3-137: **FSVH1924 Package—XCVU31P I/O Bank Diagram**



Power Pins		Dedicated Pins		Multi-Function I/O Pins
GND	E MGTAVCC	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	V MGTAVTT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	Λ MGTVCCAUX	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	HBM AUX VCCAUX_HBM	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	HBM VCC VCC_HBM	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	HBM IO VCC_IO_HBM	6 DONE_0	21 VP	30 EMCCLK
VCCO		7 DXP	22 VN	31 FOE_B
VCCBRAM		8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC		9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC		10 M0_0		34 PERSTN1_I2C_SDA
n NC		11 M1_0		35 PERSTN0
r RSVD		12 M2_0		38 SMBALERT
R RSVDGND		13 POR_OVERRIDE		36 RS0
		14 PROGRAM_B_0		37 RS1
		15 PUDC_B_0		

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Figure 3-138: **FSVH1924 Package—XCVU31P Configuration/Power Diagram**

FLVA2104 (XCVU5P and XCVU7P) and FLRA2104 (XQVU7P)

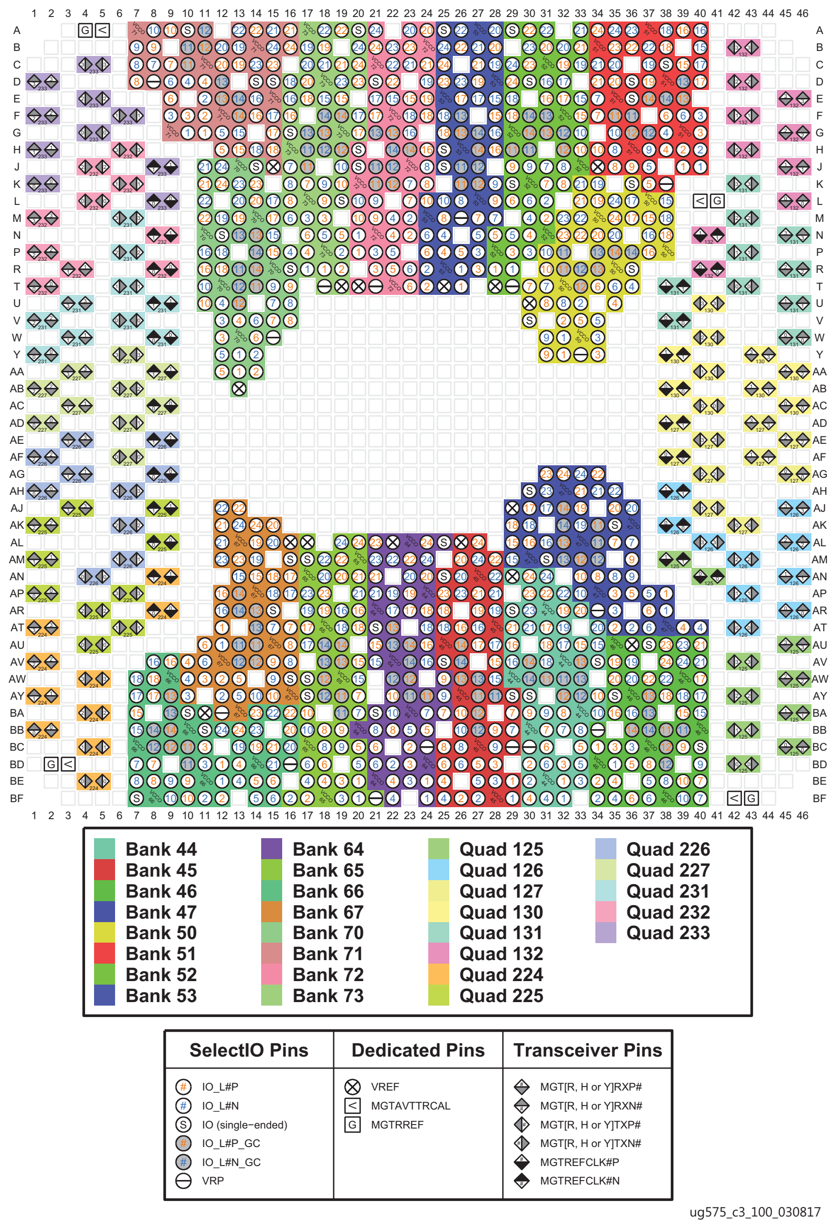

Figure 3-139: **FLVA2104 Package—XCVU5P and XCVU7P and FLRA2104 Package—XQVU7P I/O Bank Diagram**

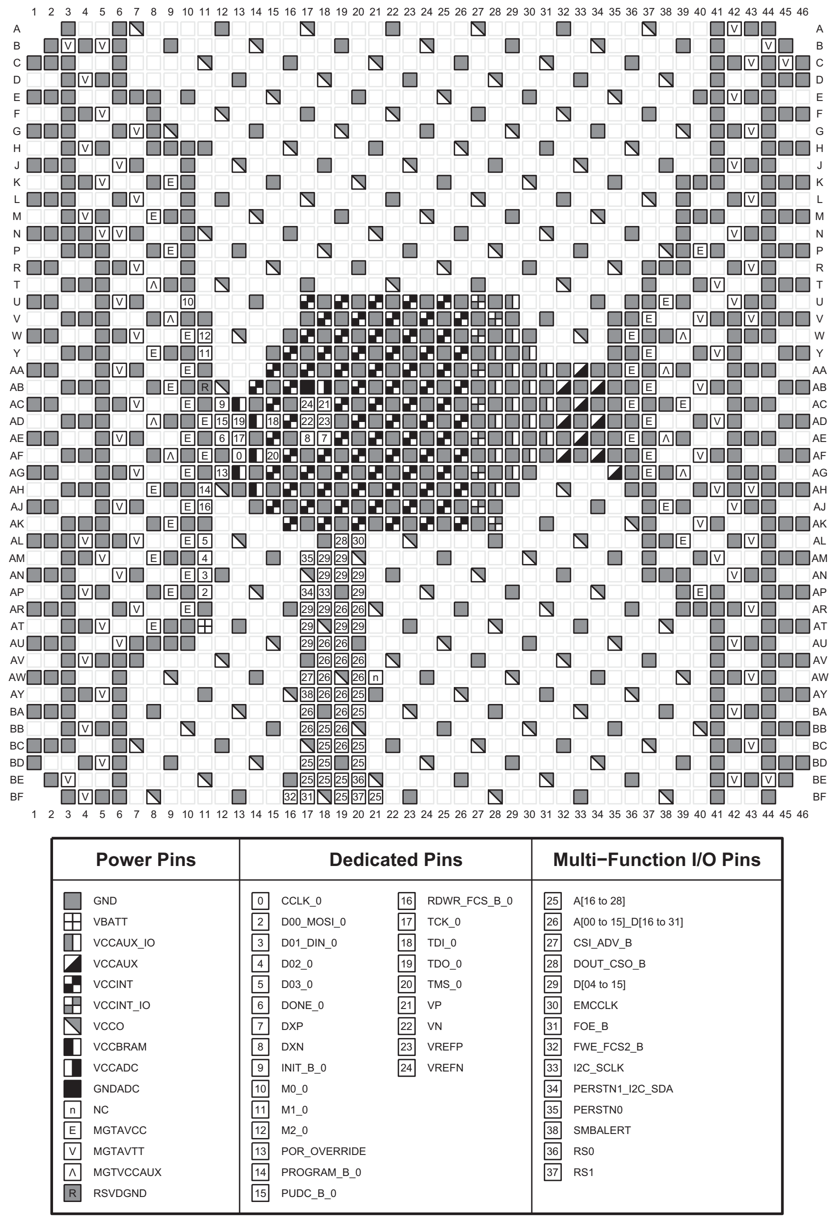

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Figure 3-140: **FLVA2104 Package—XCVU5P and XCVU7P and FLRA2104 Package—XQVU7P Configuration/Power Diagram**

FLGA2104 (XCVU9P)

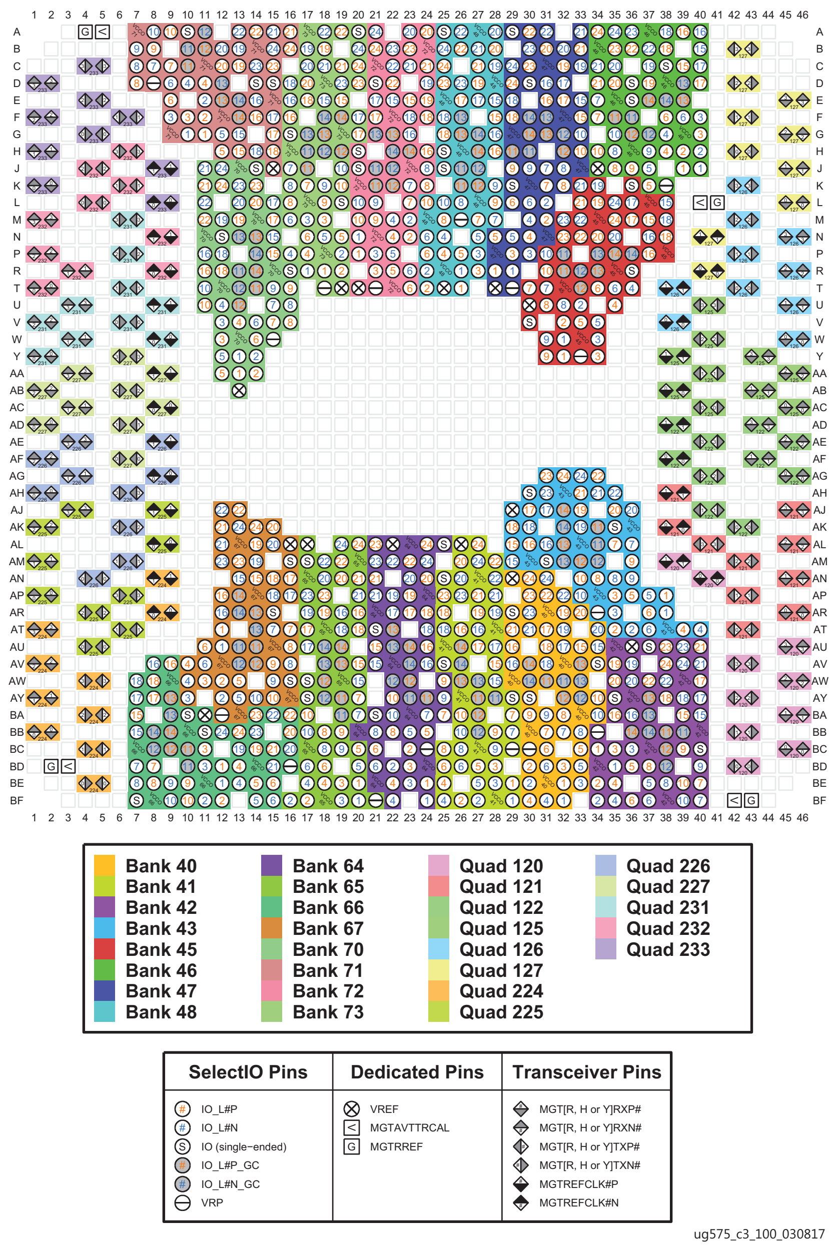


Figure 3-141: **FLGA2104 Package—XCVU9P I/O Bank Diagram**

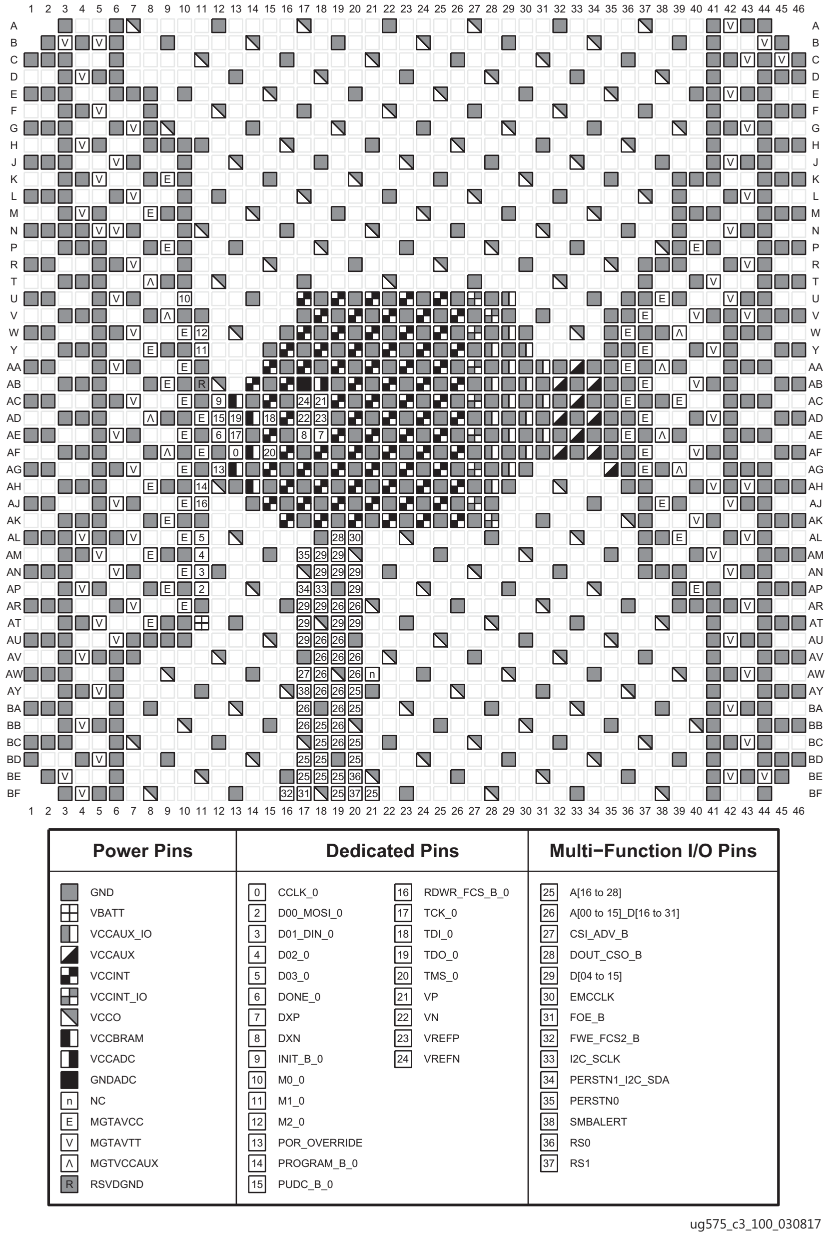


Figure 3-142: **FLGA2104 Package—XCVU9P Configuration/Power Diagram**

FHGA2104 (XCVU13P)

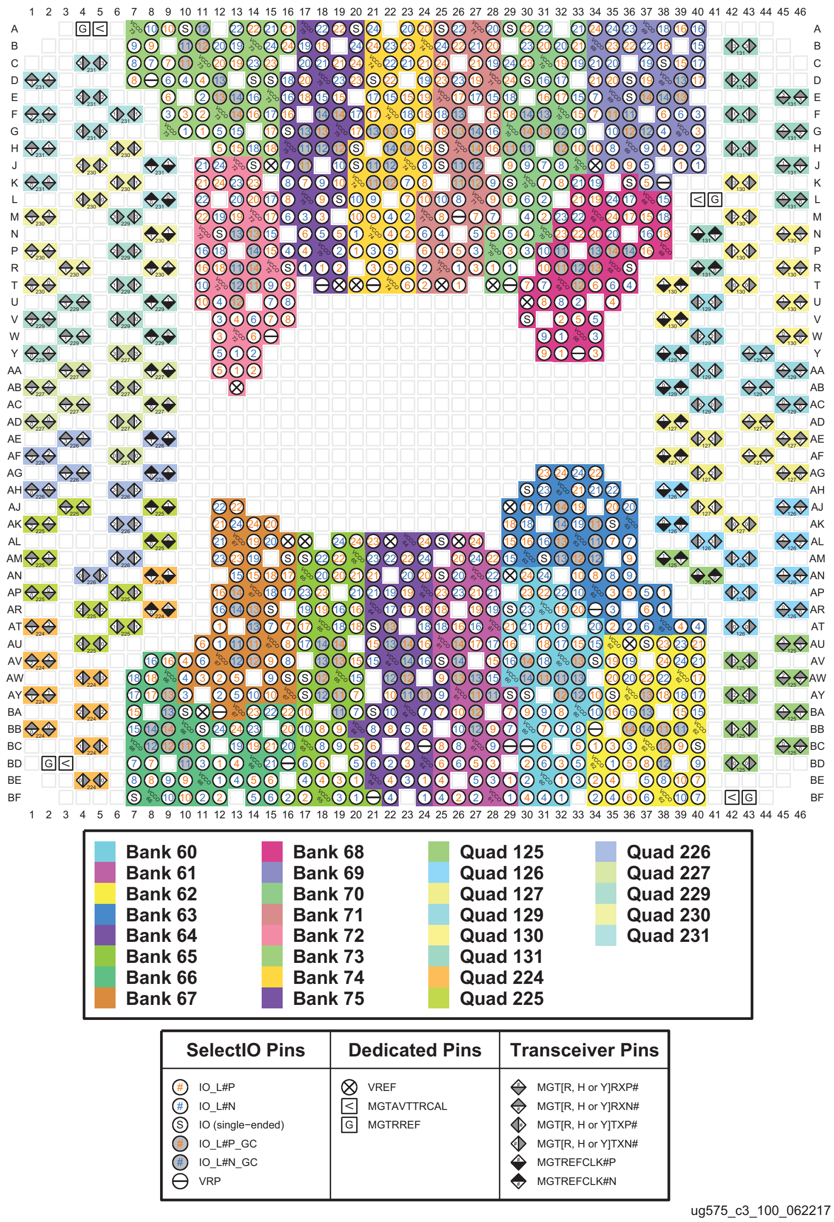


Figure 3-143: **FHGA2104 Package—XCVU13P I/O Bank Diagram**

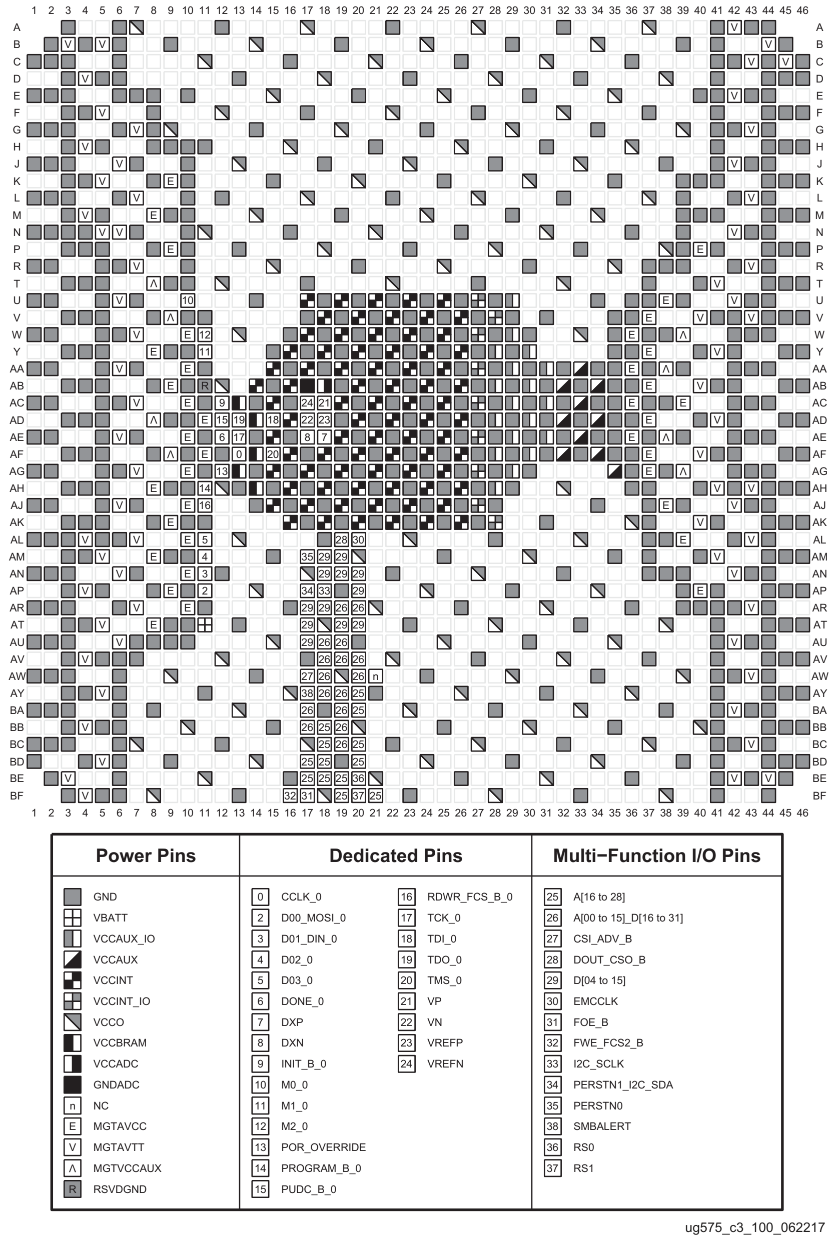


Figure 3-144: **FHGA2104 Package—XCVU13P Configuration/Power Diagram**

FLVB2104 (XCVU5P and XCVU7P) and FLRB2104 (XQVU7P)

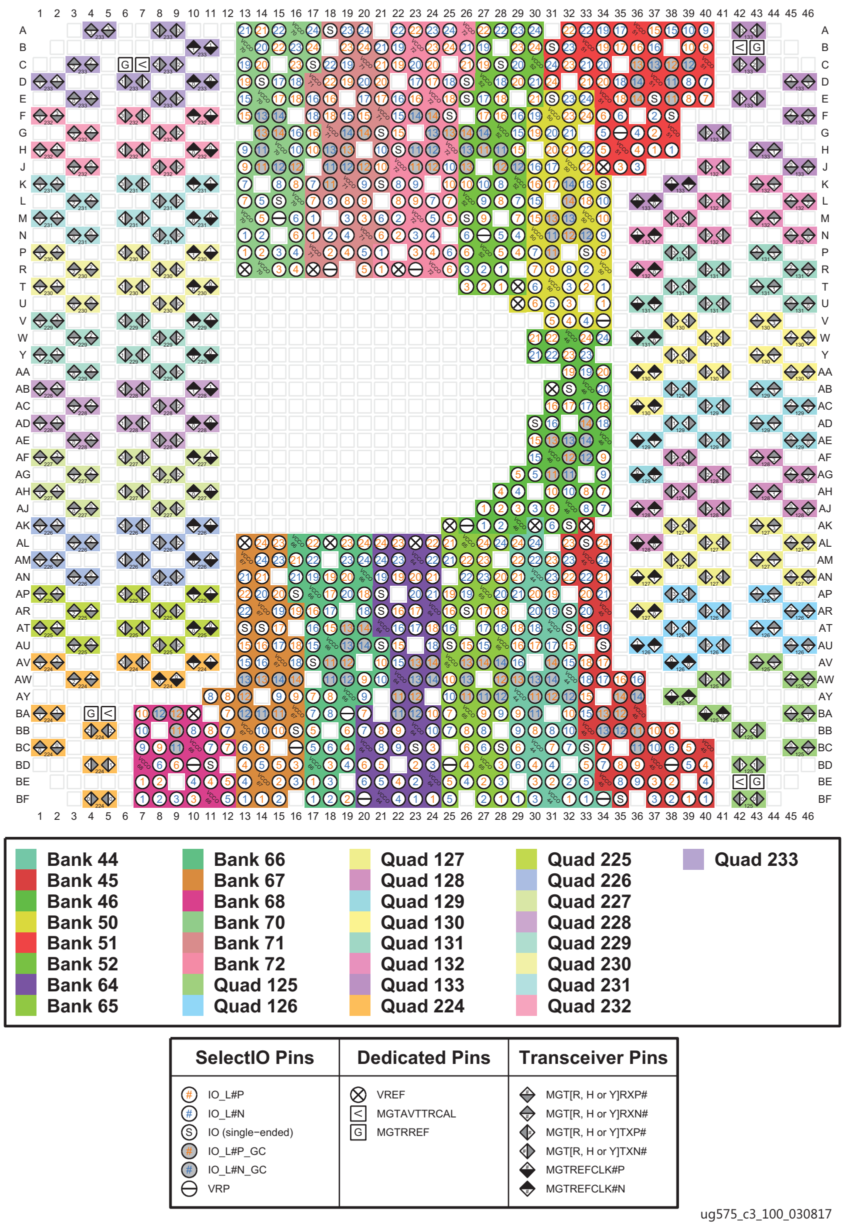
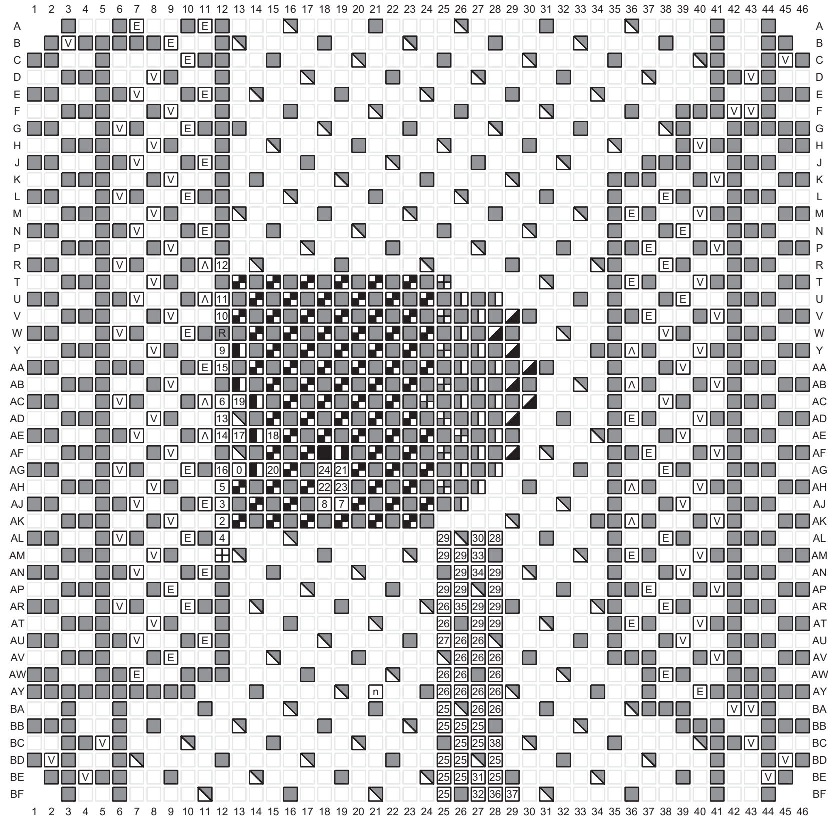


Figure 3-145: **FLVB2104 Package—XCVU5P and XCVU7P and FLRB2104 Package—XQVU7P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-146: **FLVB2104 Package—XCVU5P and XCVU7P and FLRB2104 Package—XQVU7P Configuration/Power Diagram**

FLGB2104 (XCVU9P)

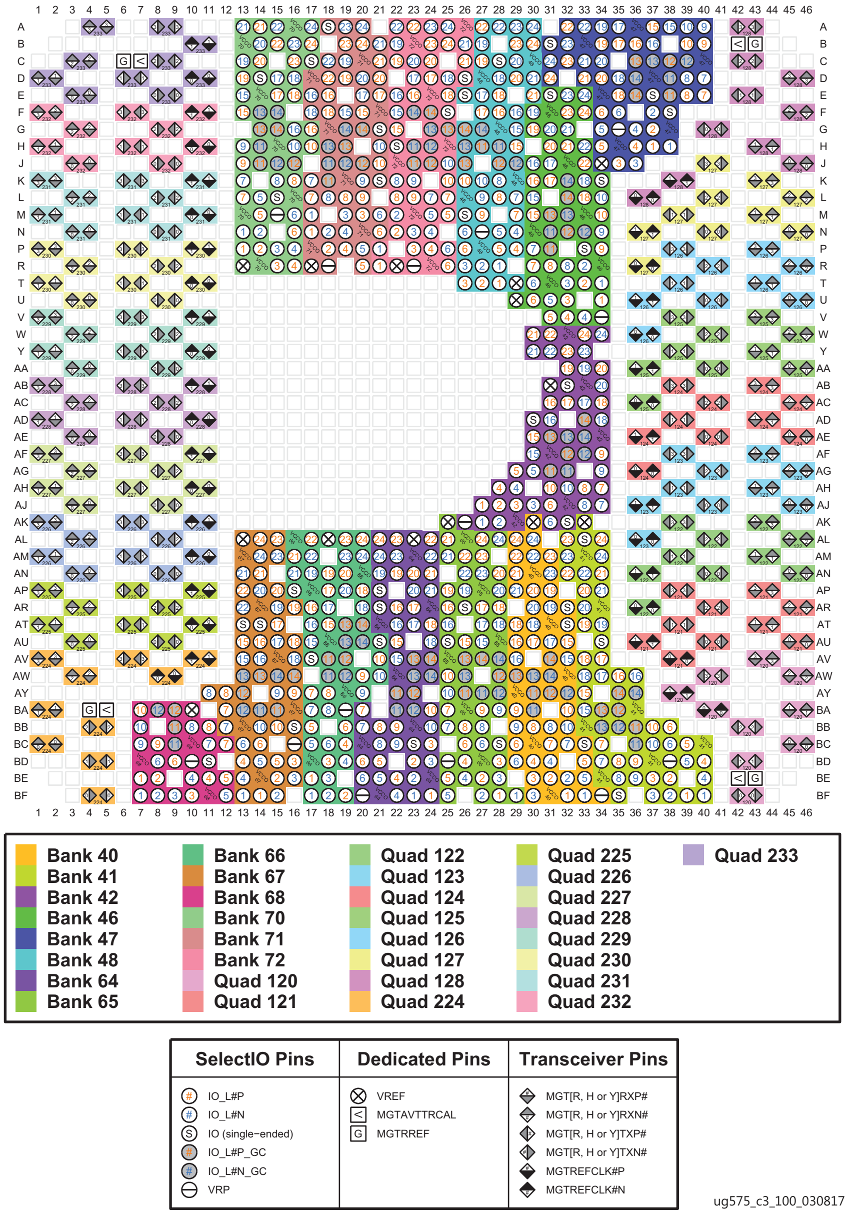


Figure 3-147: **FLGB2104 Package—XCVU9P I/O Bank Diagram**

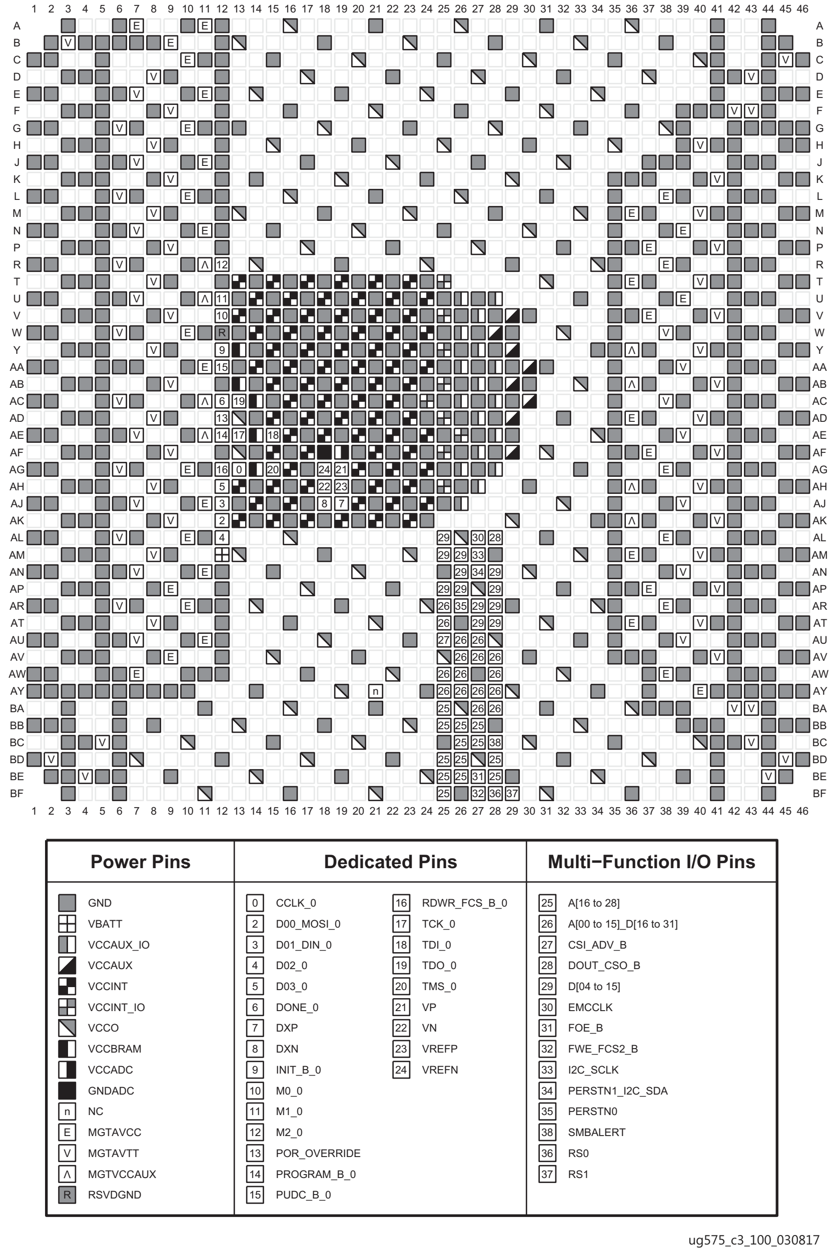


Figure 3-148: **FLGB2104 Package—XCVU9P Configuration/Power Diagram**

FLGB2104 (XCVU11P)

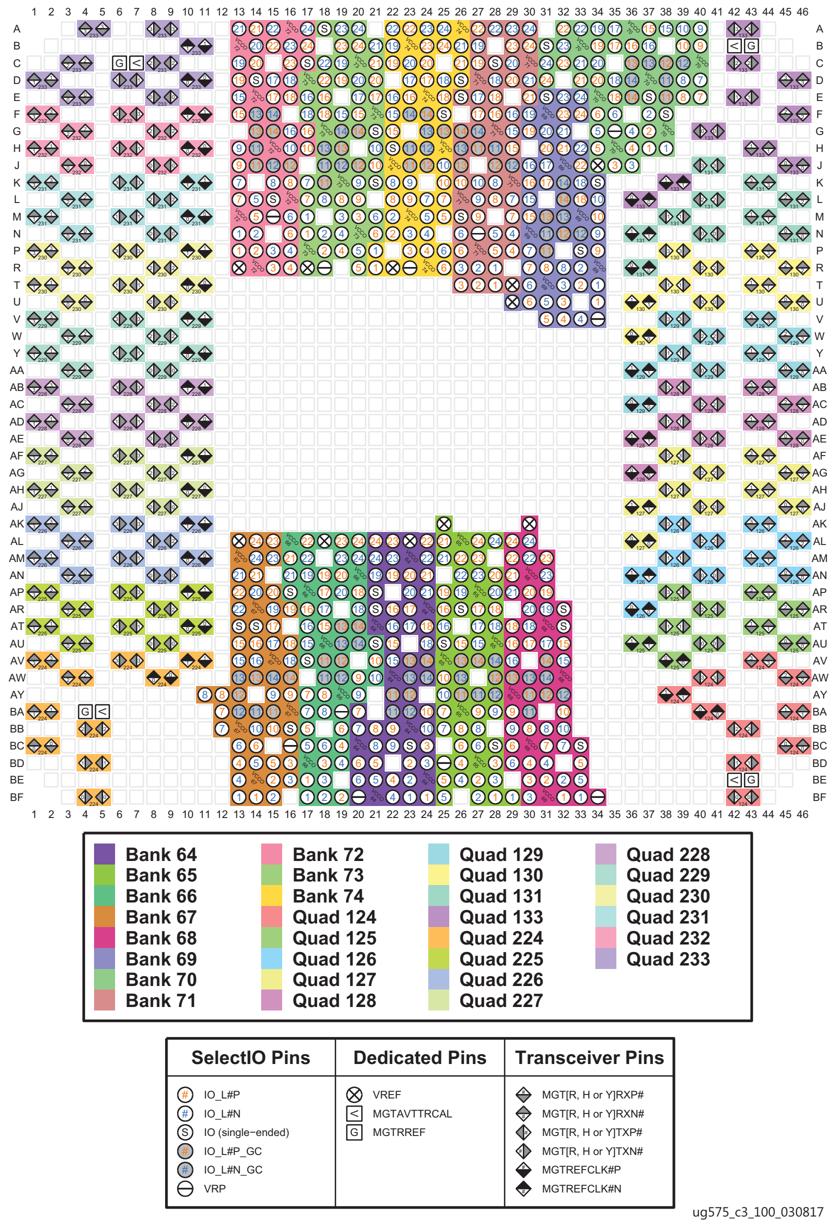


Figure 3-149: **FLGB2104 Package—XCVU11P I/O Bank Diagram**

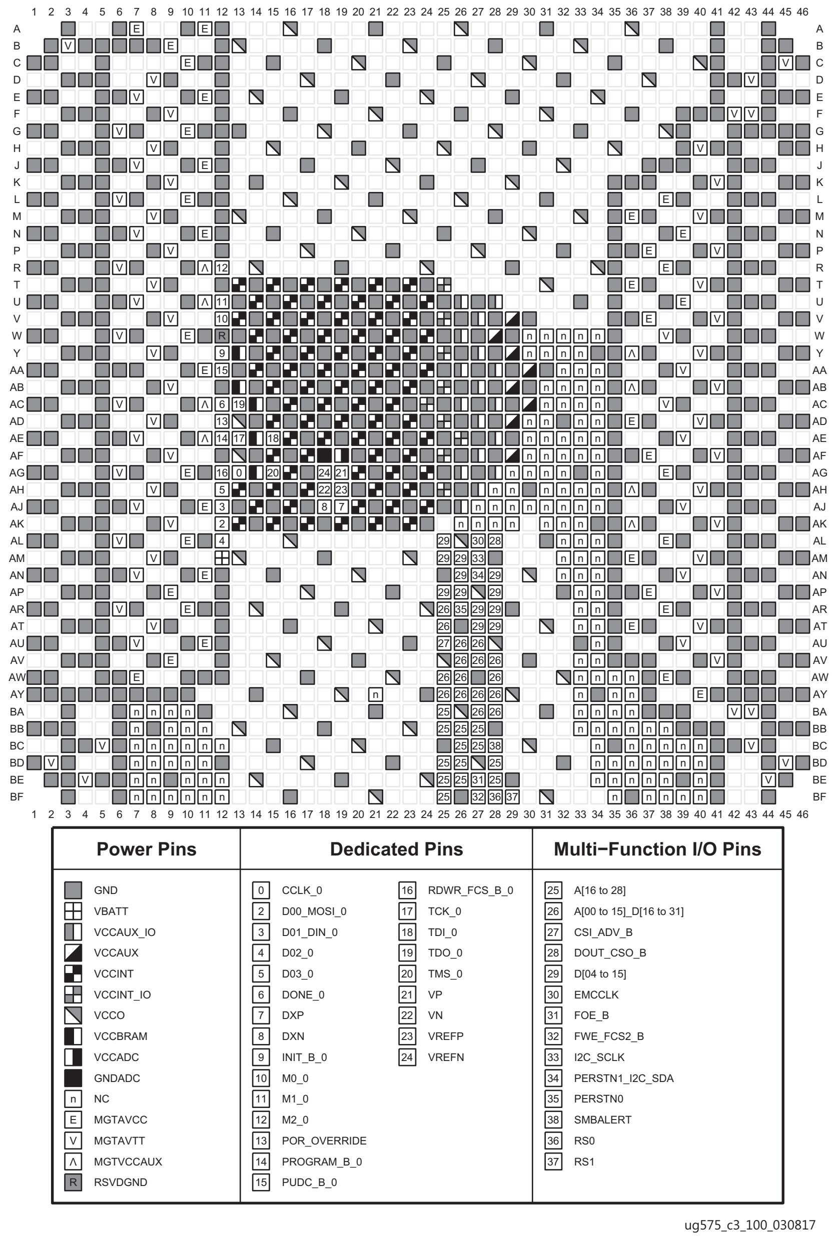


Figure 3-150: **FLGB2104 Package—XCVU11P Configuration/Power Diagram**

FHGB2104 (XCVU13P)

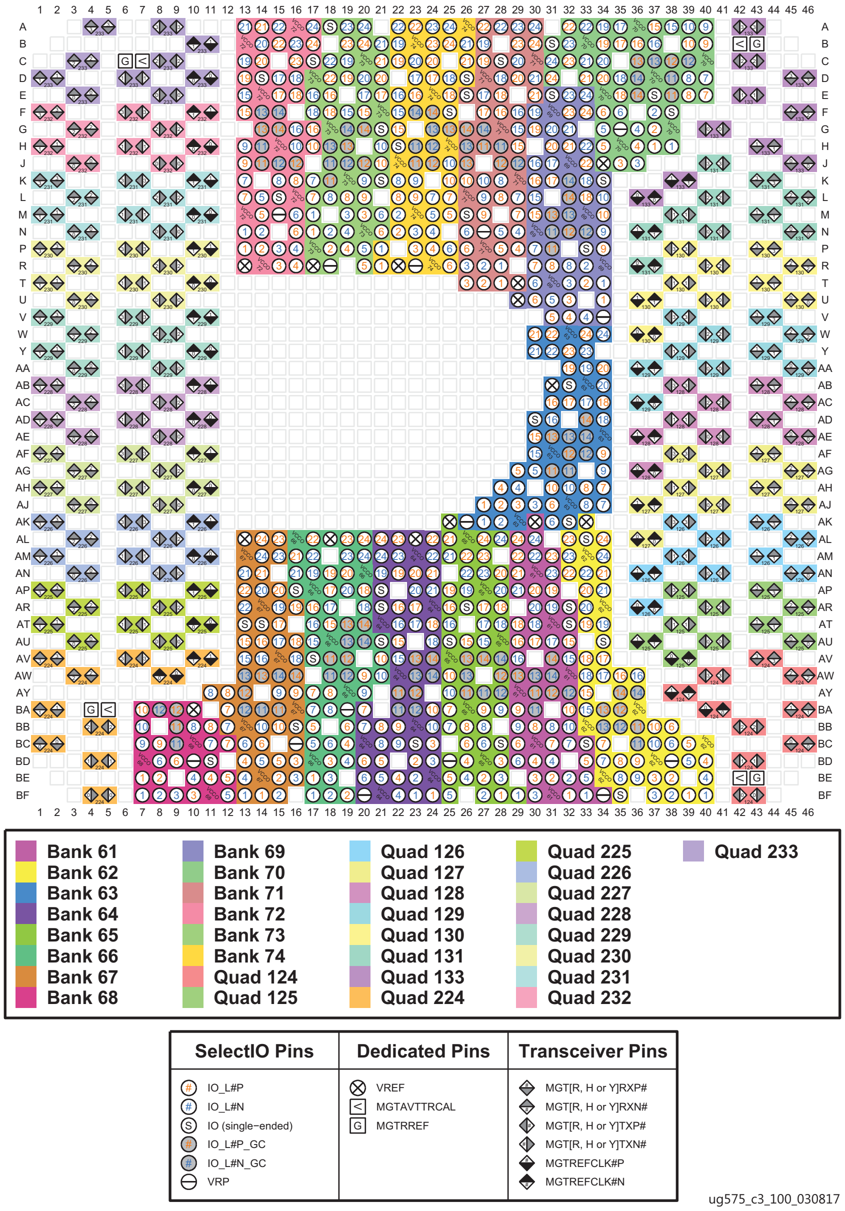
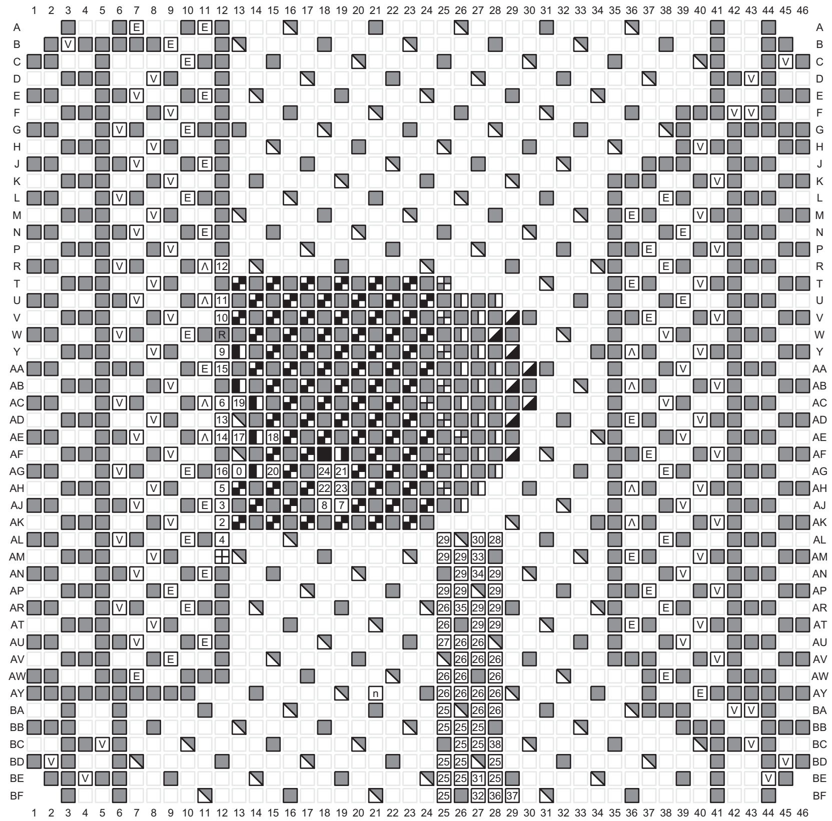


Figure 3-151: **FHGB2104 Package—XCVU13P I/O Bank Diagram**



Power Pins		Dedicated Pins				Multi-Function I/O Pins	
	GND	0	CCLK_0	16	RDWR_FCS_B_0	25	A[16 to 28]
	VBATT	2	D00_MOSI_0	17	TCK_0	26	A[00 to 15]_D[16 to 31]
	VCCAUX_IO	3	D01_DIN_0	18	TDI_0	27	CSI_ADV_B
	VCCAUX	4	D02_0	19	TDO_0	28	DOUT_CSO_B
	VCCINT	5	D03_0	20	TMS_0	29	D[04 to 15]
	VCCINT_IO	6	DONE_0	21	VP	30	EMCCLK
	VCCO	7	DXP	22	VN	31	FOE_B
	VCCBRAM	8	DXN	23	VREFP	32	FWE_FCS2_B
	VCCADC	9	INIT_B_0	24	VREFN	33	I2C_SCLK
	GNDADC	10	M0_0			34	PERSTN1_I2C_SDA
n	NC	11	M1_0			35	PERSTN0
E	MGTAVCC	12	M2_0			38	SMBALERT
V	MGTAVTT	13	POR_OVERRIDE			36	RS0
Λ	MGTVCCAUX	14	PROGRAM_B_0			37	RS1
R	RSVDGND	15	PUDC_B_0				

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Figure 3-152: **FHGB2104 Package—XCVU13P Configuration/Power Diagram**

FLVC2104 (XCVU5P and XCVU7P)

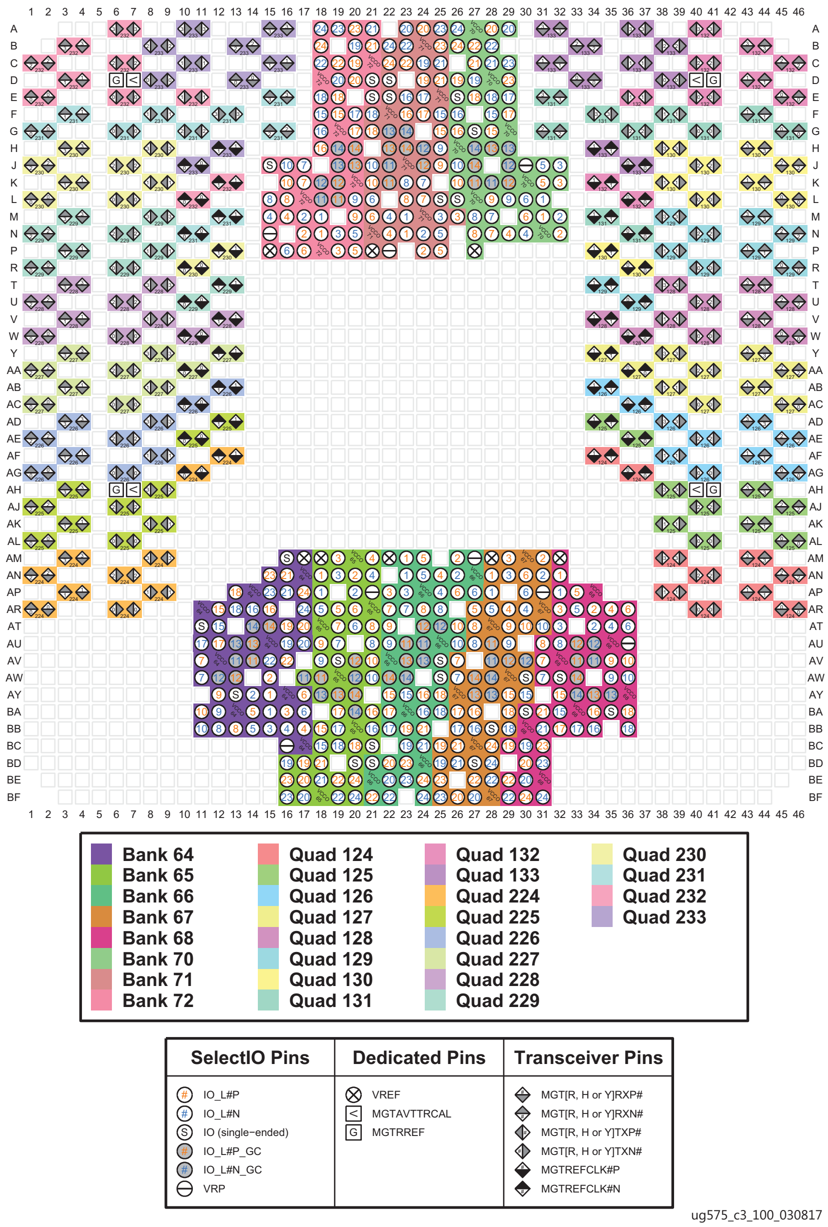


Figure 3-153: **FLVC2104 Package—XCVU5P and XCVU7P I/O Bank Diagram**

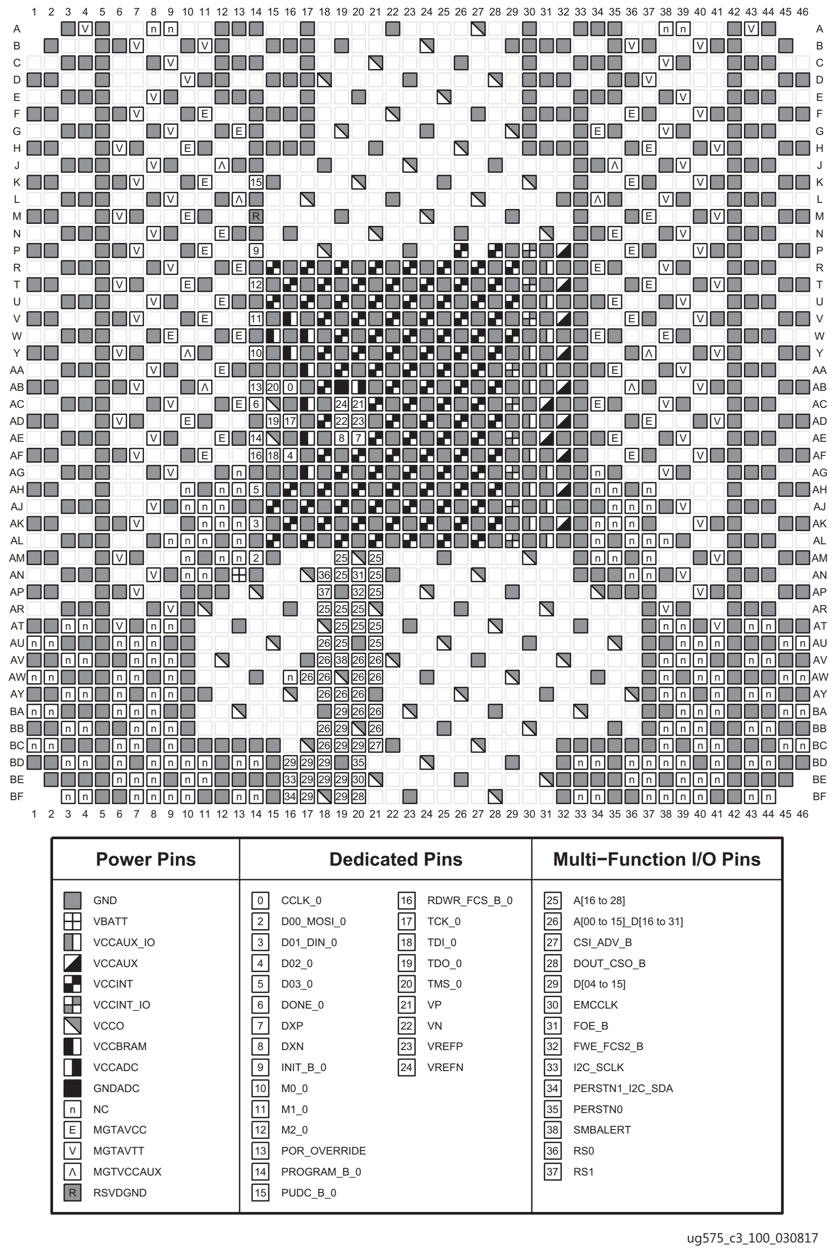


Figure 3-154: **FLVC2104 Package—XCVU5P and XCVU7P Configuration/Power Diagram**

FLGC2104 (XCVU9P)

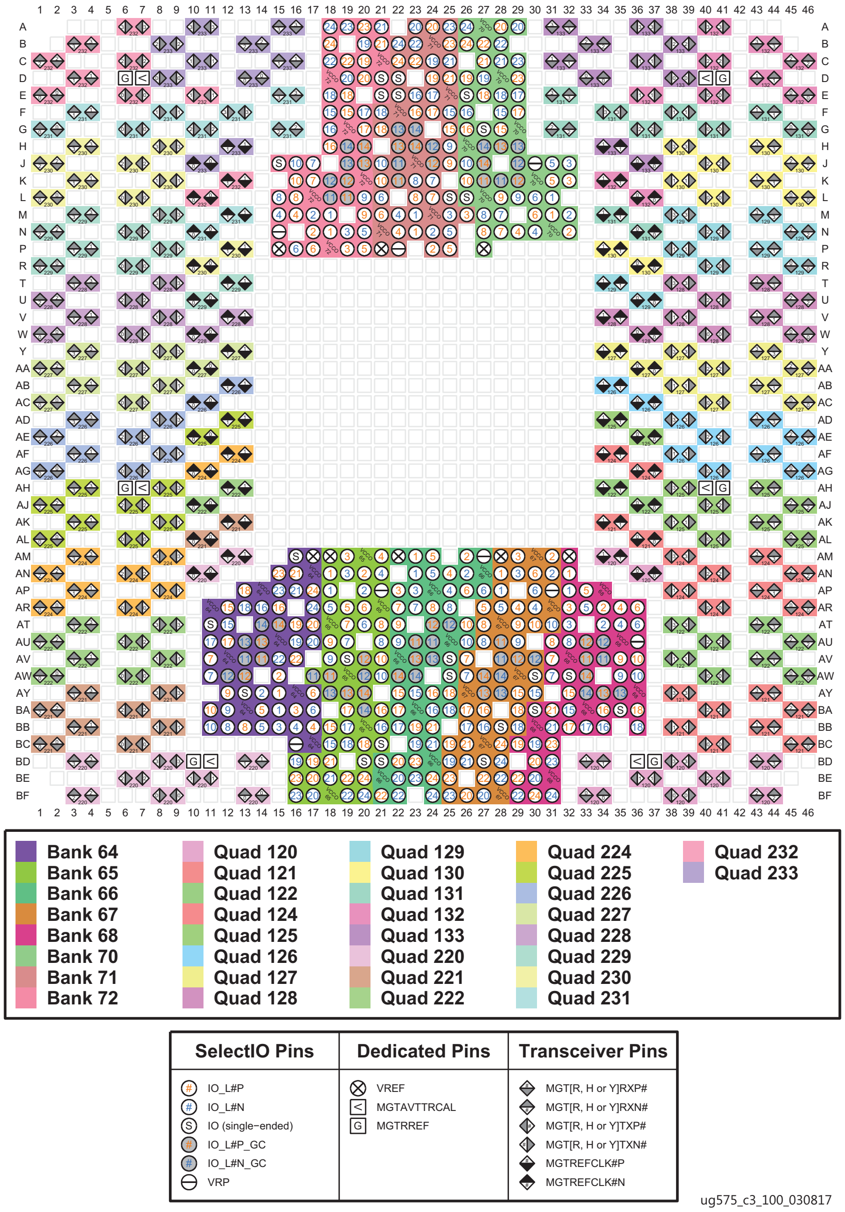


Figure 3-155: **FLGC2104 Package—XCVU9P I/O Bank Diagram**

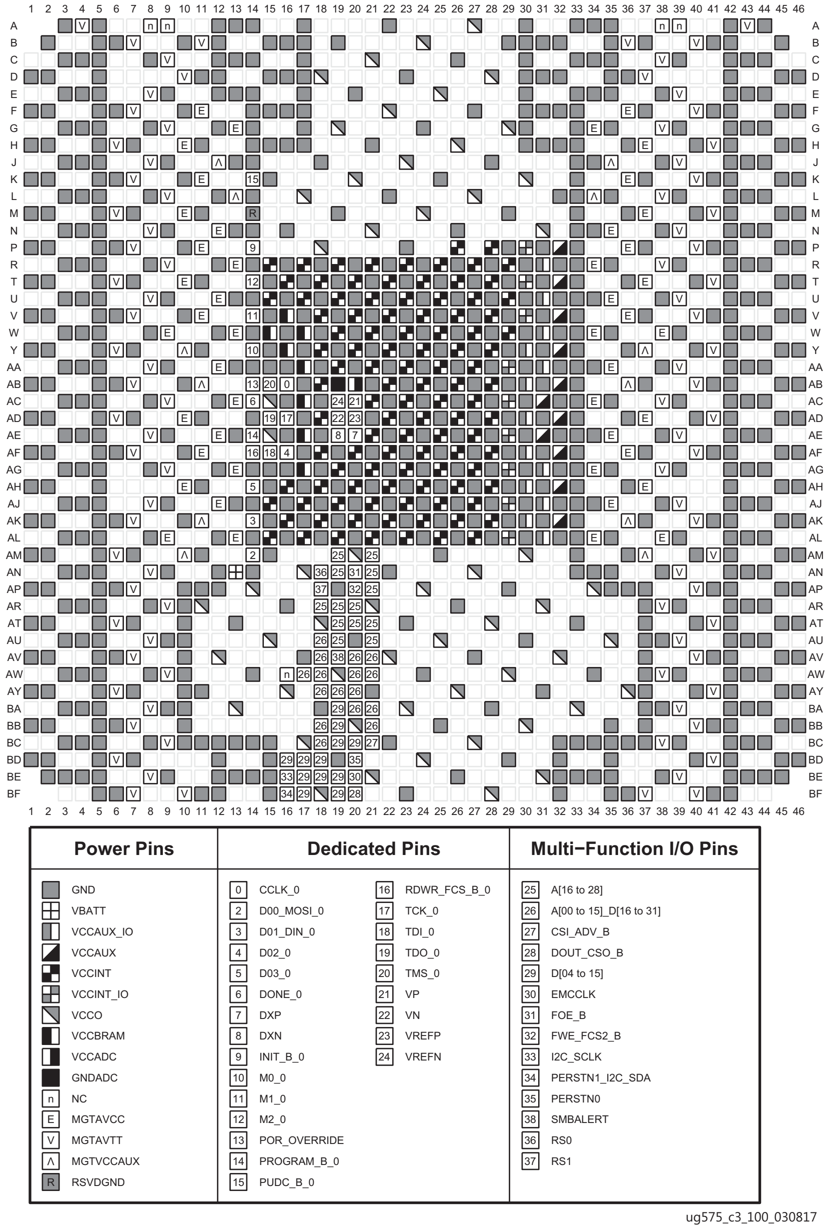


Figure 3-156: **FLGC2104 Package—XCVU9P Configuration/Power Diagram**

FLGC2104 (XCVU11P) and FLRC2104 (XQVU11P)

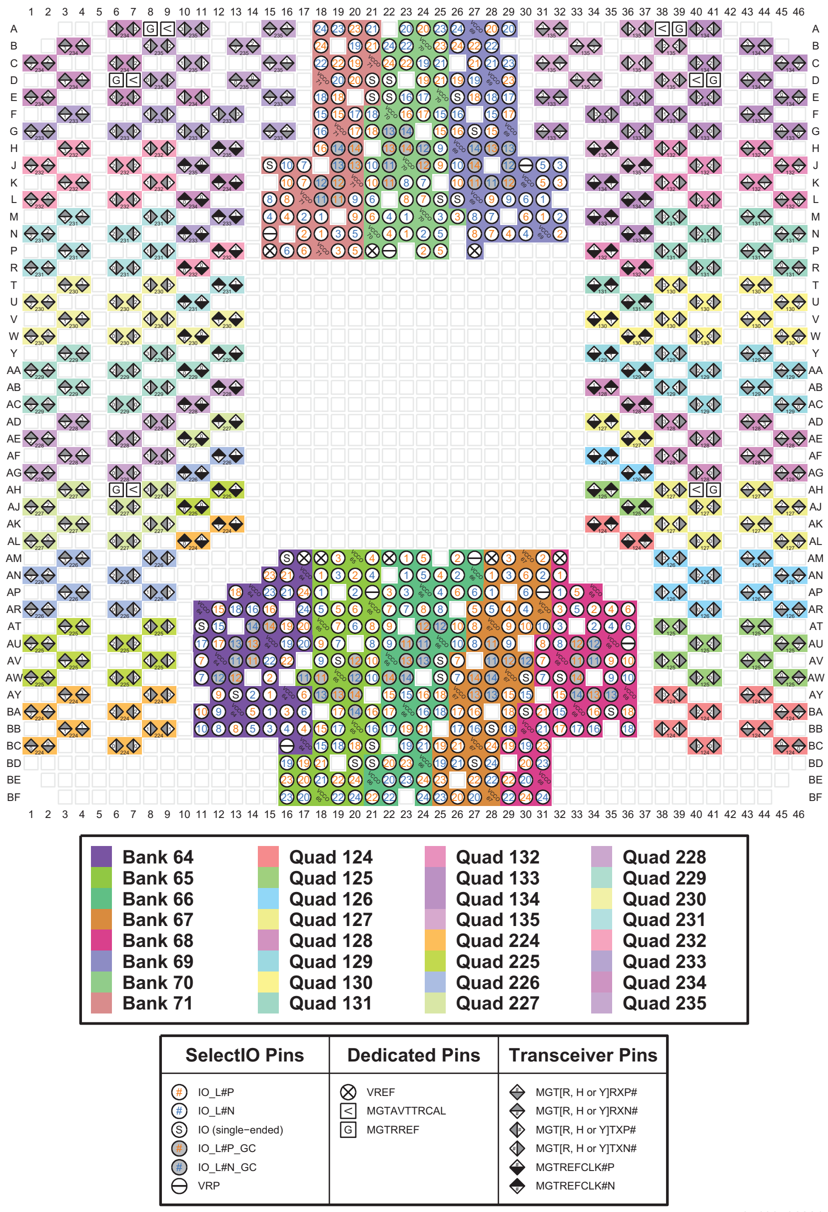


Figure 3-157: **FLGC2104 Package—XCVU11P and FLRC2104 Package—XQVU11P I/O Bank Diagram**

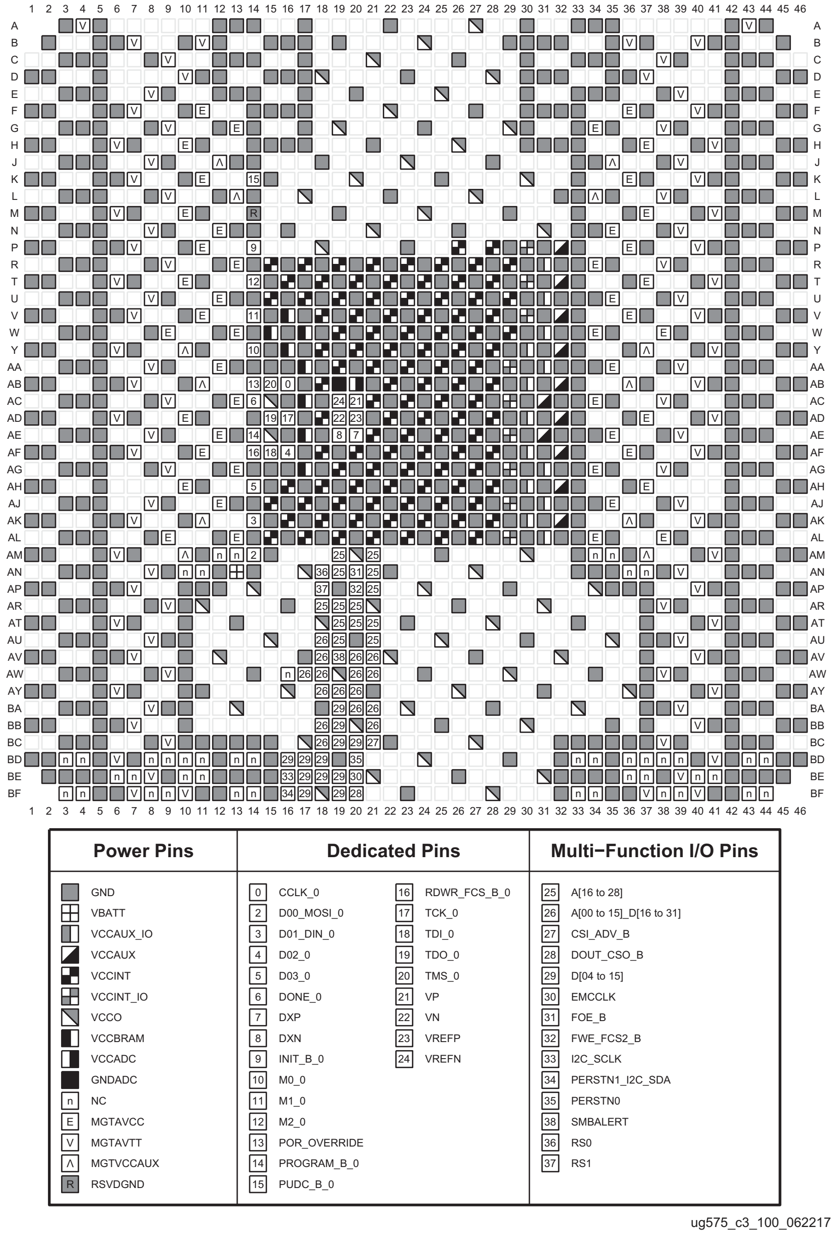


Figure 3-158: **FLGC2104 Package—XCVU11P and FLRC2104 Package—XQVU11P Configuration/Power Diagram**

FHGC2104 (XCVU13P)

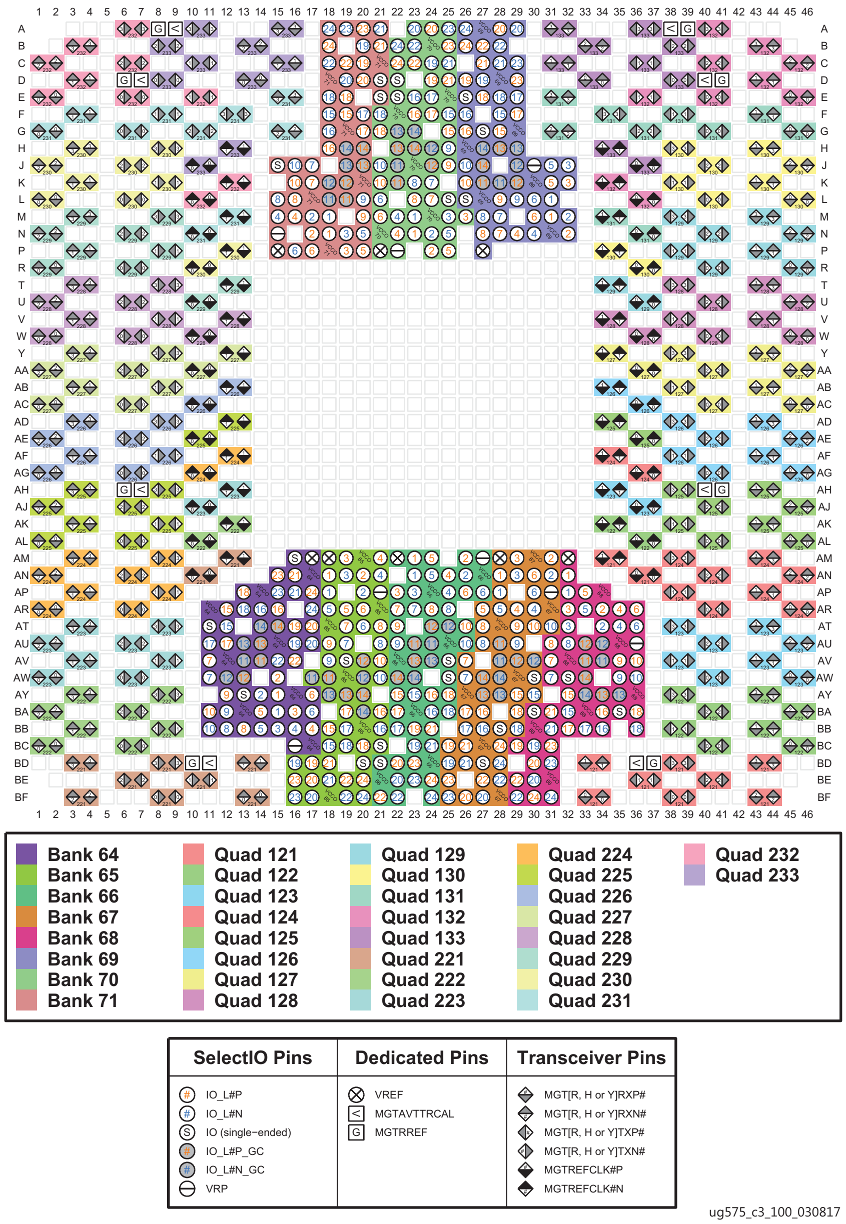


Figure 3-159: **FHGC2104 Package—XCVU13P I/O Bank Diagram**

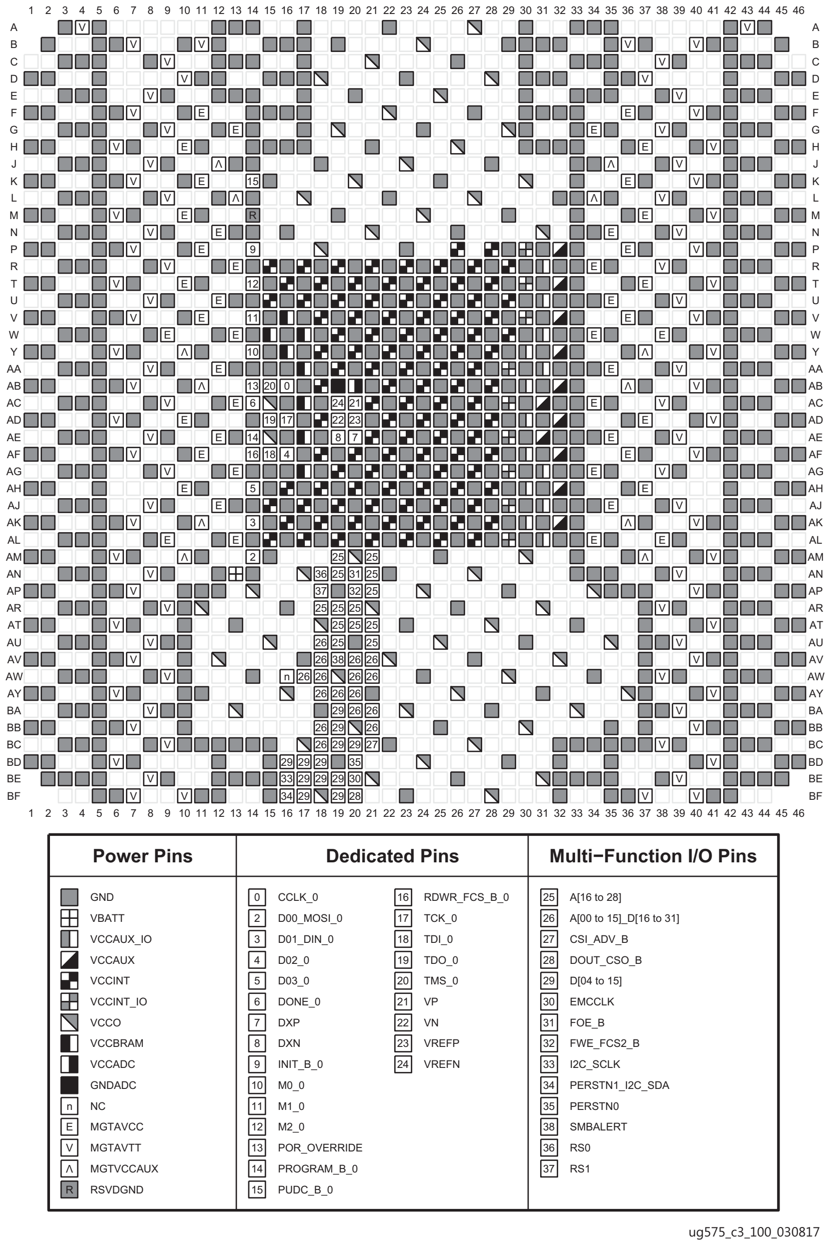


Figure 3-160: **FHGC2104 Package—XCVU13P Configuration/Power Diagram**

FSGD2104 (XCVU9P)

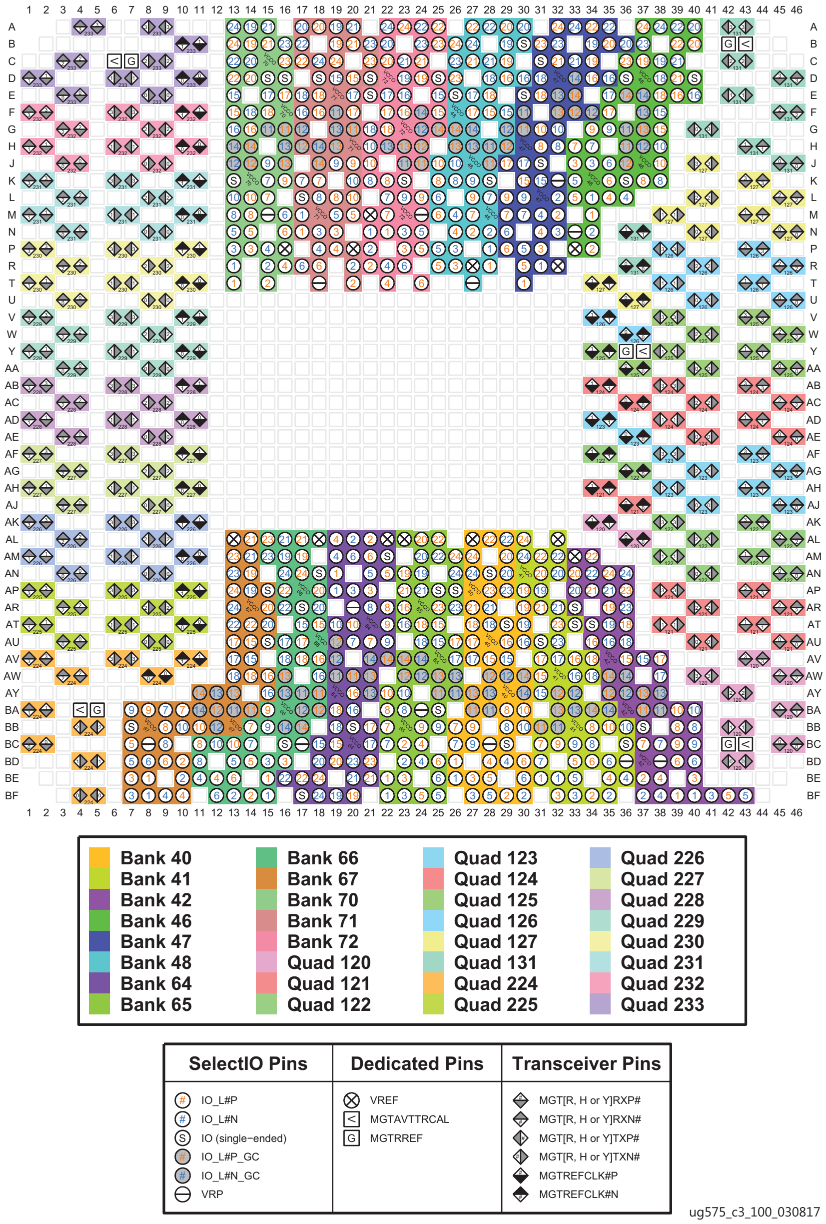


Figure 3-161: **FSGD2104 Package—XCVU9P I/O Bank Diagram**

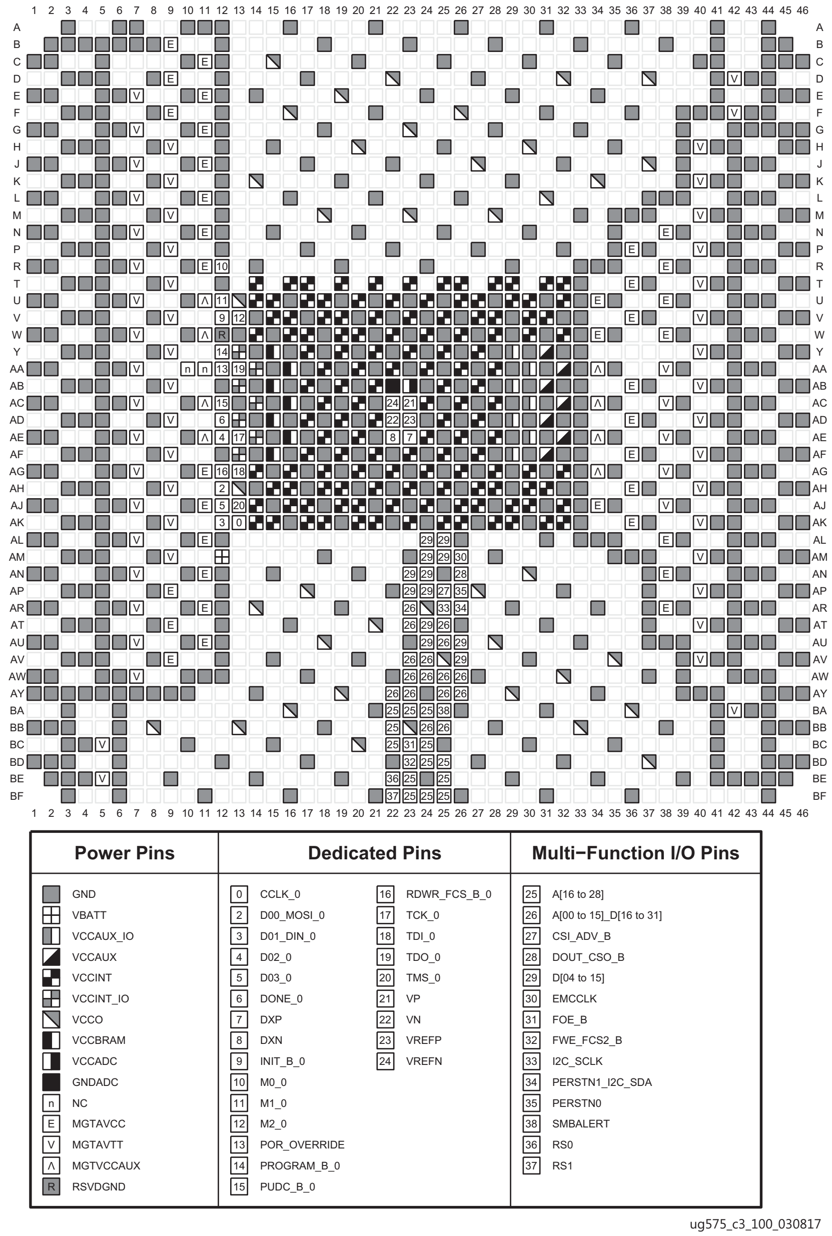


Figure 3-162: **FSGD2104 Package—XCVU9P Configuration/Power Diagram**

FSGD2104 (XCVU11P)

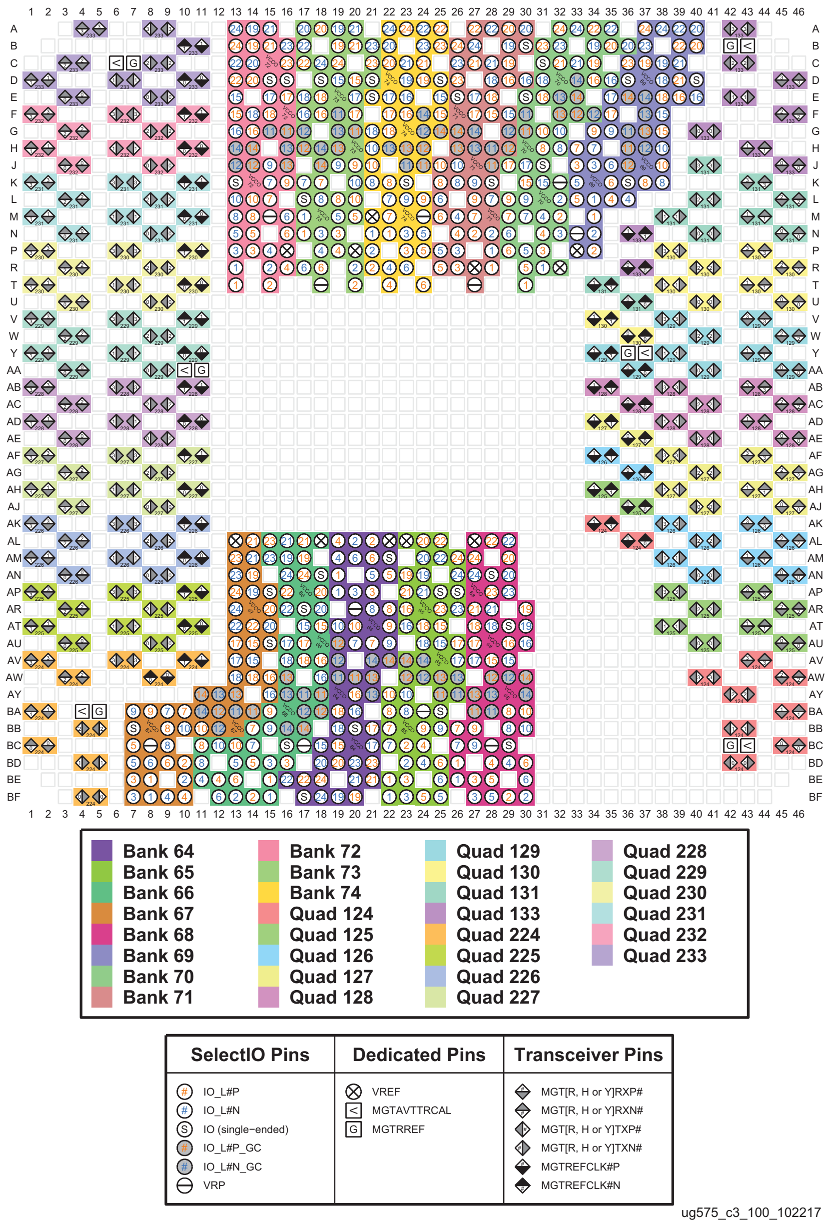
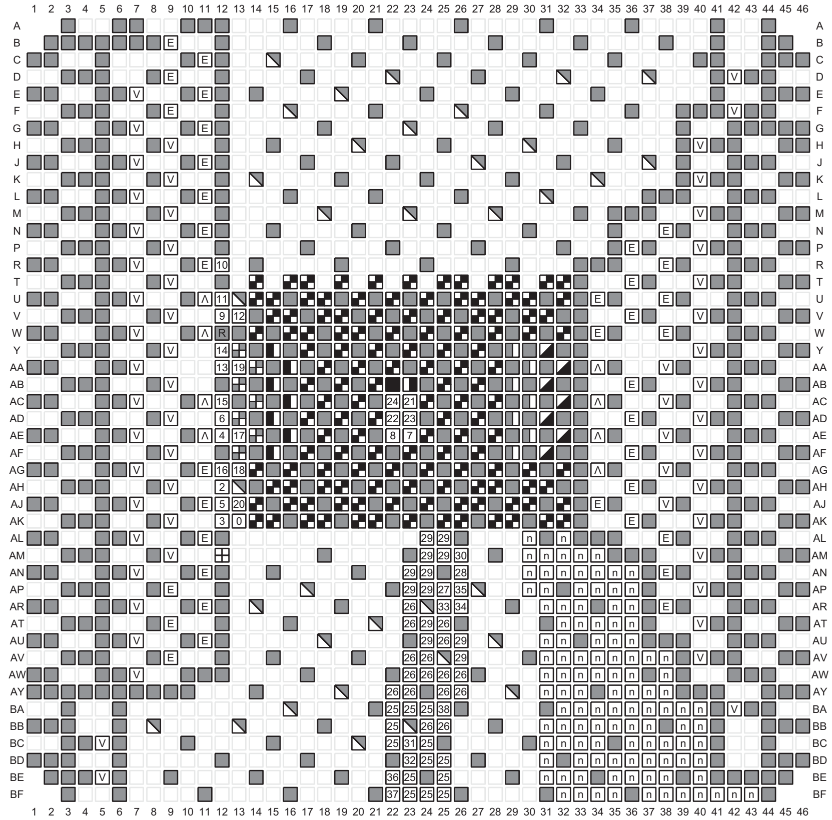


Figure 3-163: **FSGD2104 Package—XCVU11P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-164: **FSGD2104 Package—XCVU11P Configuration/Power Diagram**

FIGD2104 (XCVU13P)

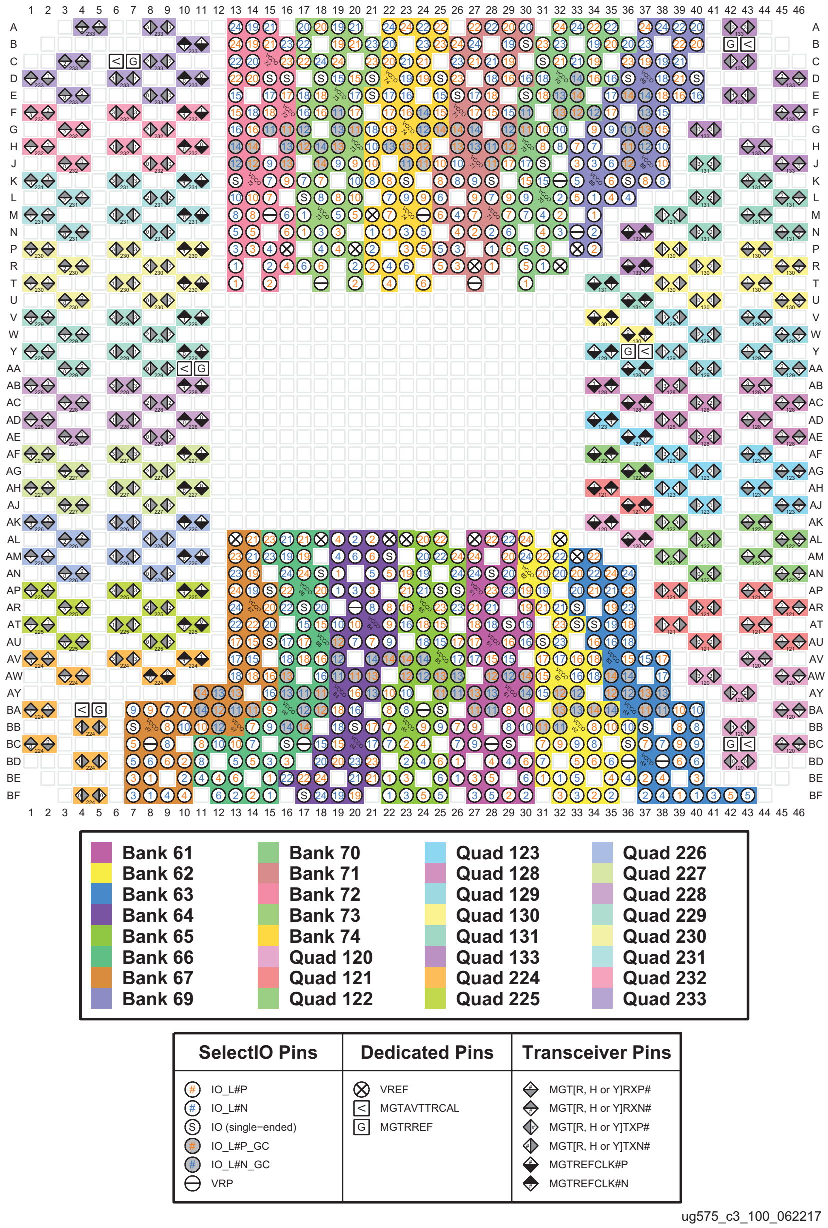
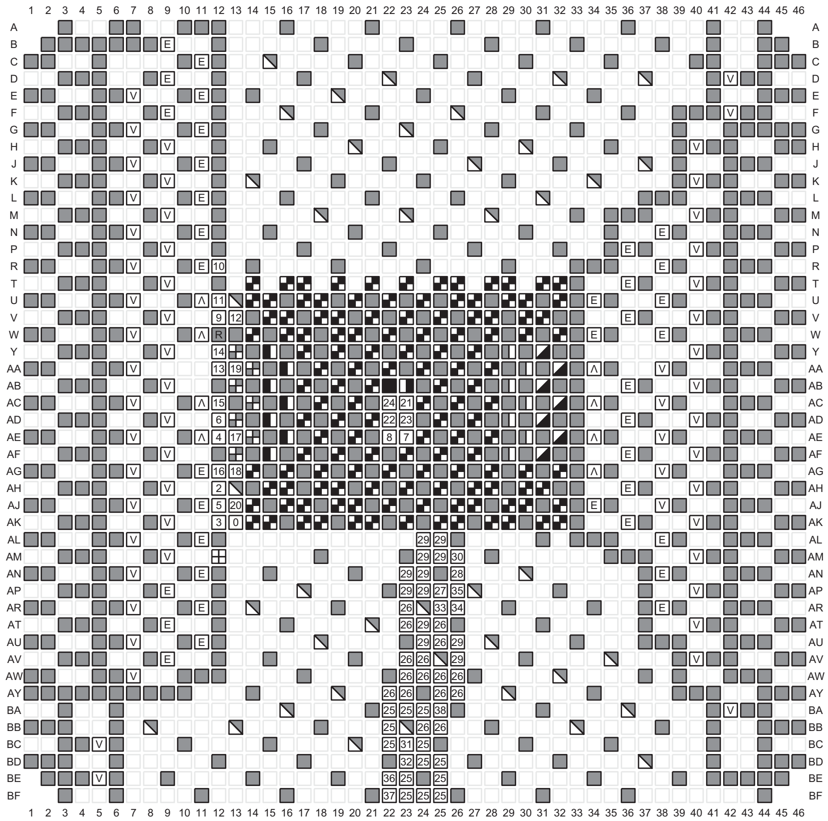


Figure 3-165: **FIGD2104 Package—XCVU13P I/O Bank Diagram**



Power Pins

- GND
- VBATT
- VCCAUX_IO
- VCCAUX
- VCCINT
- VCCINT_IO
- VCCO
- VCCBRAM
- VCCADC
- GNDADC
- n NC
- E MGTAVCC
- V MGTAVTT
- Λ MGTVCCAUX
- R RSVDGND

Dedicated Pins

- 0 CCLK_0
- 2 D00_MOSI_0
- 3 D01_DIN_0
- 4 D02_0
- 5 D03_0
- 6 DONE_0
- 7 DXP
- 8 DXN
- 9 INIT_B_0
- 10 M0_0
- 11 M1_0
- 12 M2_0
- 13 POR_OVERRIDE
- 14 PROGRAM_B_0
- 15 PUDC_B_0
- 16 RDWR_FCS_B_0
- 17 TCK_0
- 18 TDI_0
- 19 TDO_0
- 20 TMS_0
- 21 VP
- 22 VN
- 23 VREFP
- 24 VREFN

Multi−Function I/O Pins

- 25 A[16 to 28]
- 26 A[00 to 15]_D[16 to 31]
- 27 CSI_ADV_B
- 28 DOUT_CSO_B
- 29 D[04 to 15]
- 30 EMCCLK
- 31 FOE_B
- 32 FWE_FCS2_B
- 33 I2C_SCLK
- 34 PERSTN1_I2C_SDA
- 35 PERSTN0
- 38 SMBALERT
- 36 RS0
- 37 RS1

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Figure 3-166: **FIGD2104 Package—XCVU13P Configuration/Power Diagram**

FIGD2104 (XCVU27P)

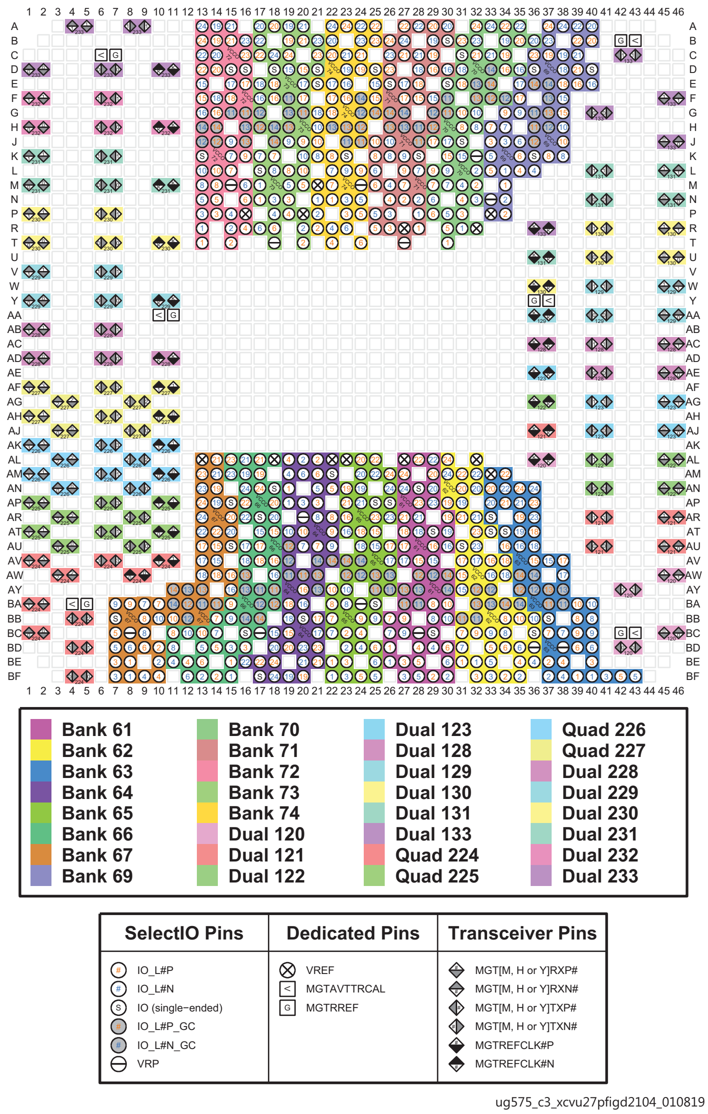


Figure 3-167: **FIGD2104 Package—XCVU27P I/O Bank Diagram**

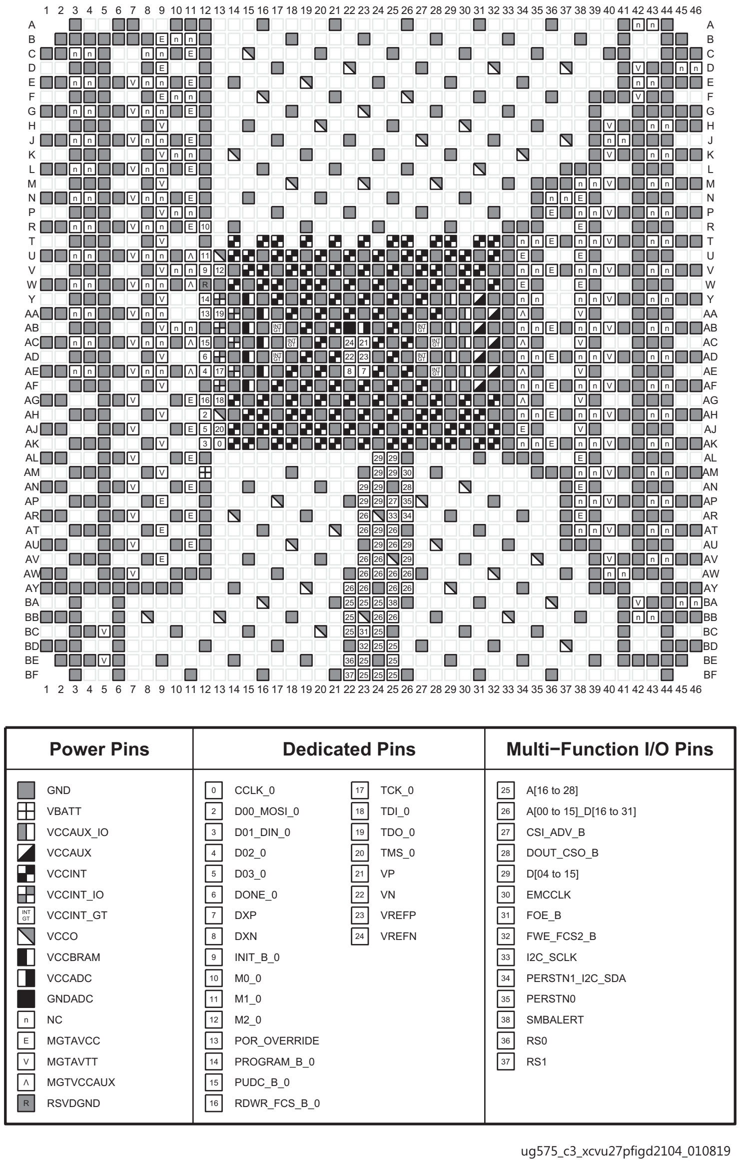


Figure 3-168: **FIGD2104 Package—XCVU27P Configuration/Power Diagram**

FIGD2104 (XCVU29P)

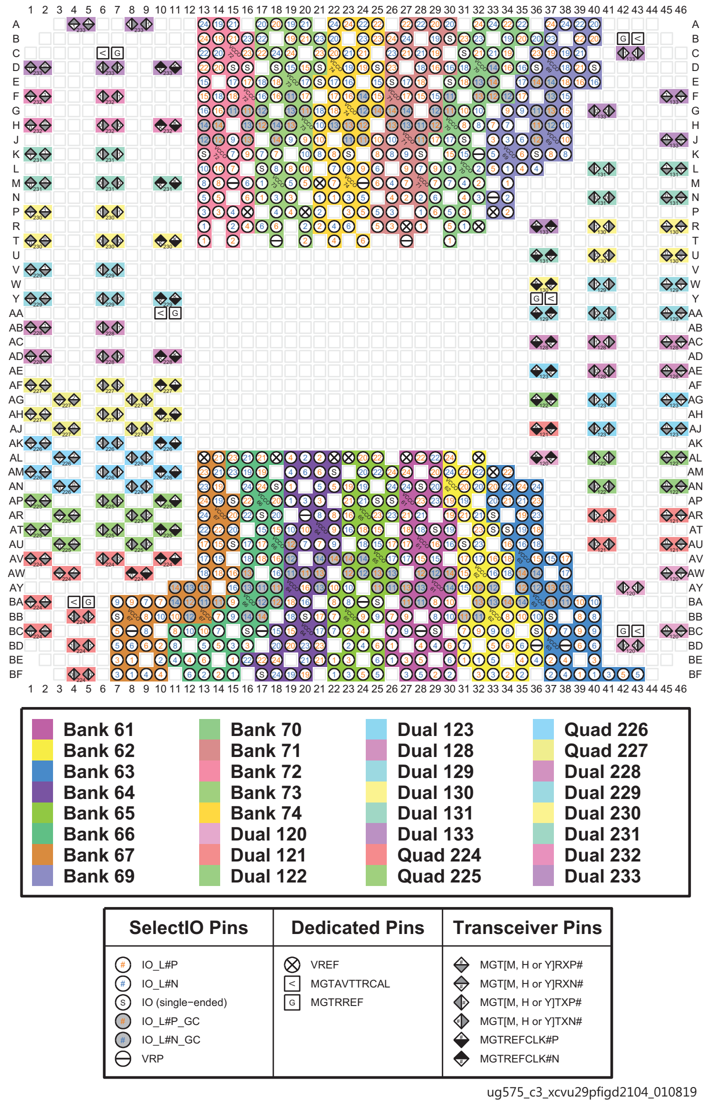


Figure 3-169: **FIGD2104 Package—XCVU29P I/O Bank Diagram**

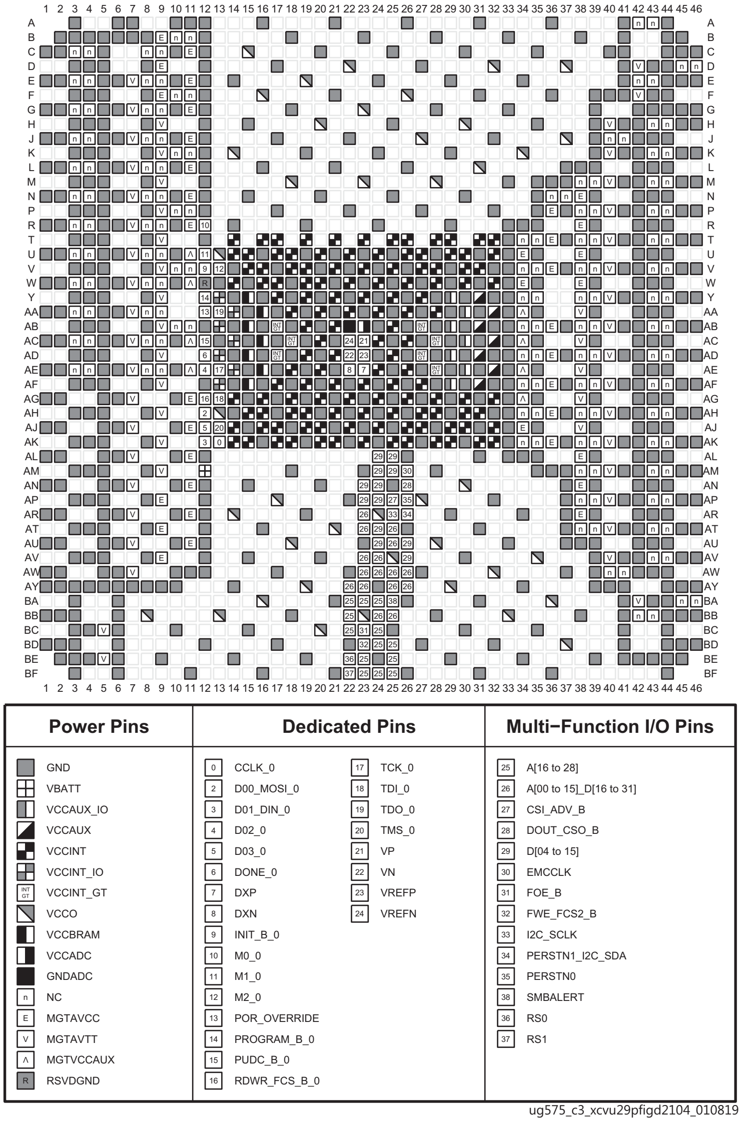


Figure 3-170: **FIGD2104 Package—XCVU29P Configuration/Power Diagram**

FSVH2104 (XCVU33P)

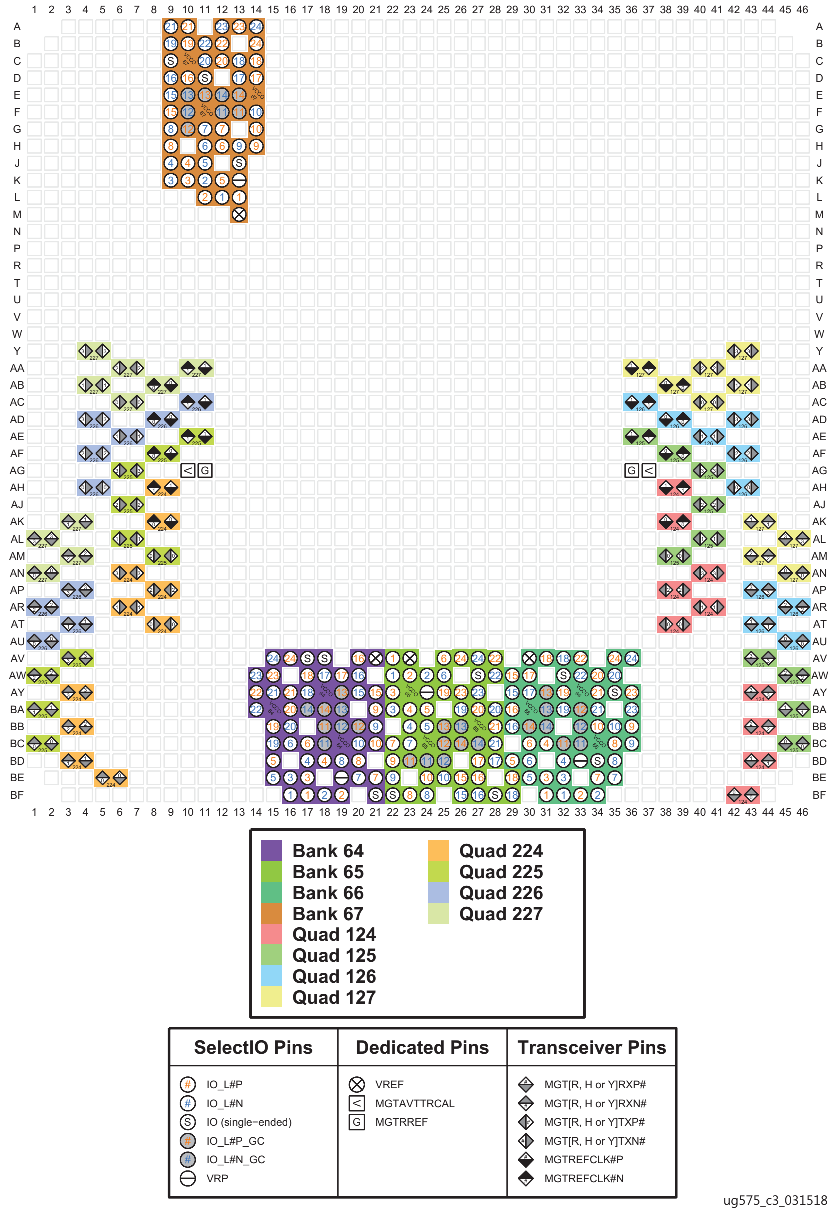
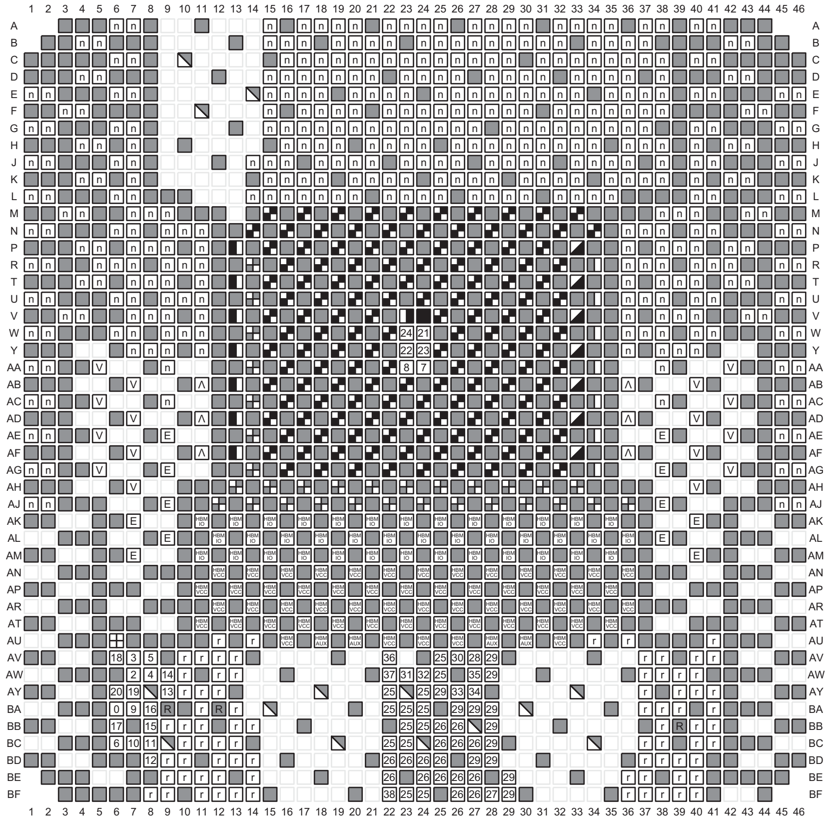


Figure 3-171: **FSVH2104 Package—XCVU33P I/O Bank Diagram**



Power Pins

GND	MGTAVCC
VBATT	MGTAVTT
VCCAUX_IO	MGTVCCAUX
VCCAUX	VCCAUX_HBM
VCCINT	VCC_HBM
VCCINT_IO	VCC_IO_HBM
VCCO	
VCCBRAM	
VCCADC	
GNDADC	
NC	
RSVD	
RSVDGND	

Dedicated Pins

0 CCLK_0	16 RDWR_FCS_B_0
2 D00_MOSI_0	17 TCK_0
3 D01_DIN_0	18 TDI_0
4 D02_0	19 TDO_0
5 D03_0	20 TMS_0
6 DONE_0	21 VP
7 DXP	22 VN
8 DXN	23 VREFP
9 INIT_B_0	24 VREFN
10 M0_0	
11 M1_0	
12 M2_0	
13 POR_OVERRIDE	
14 PROGRAM_B_0	
15 PUDC_B_0	

Multi−Function I/O Pins

- 25 A[16 to 28]
- 26 A[00 to 15]_D[16 to 31]
- 27 CSI_ADV_B
- 28 DOUT_CSO_B
- 29 D[04 to 15]
- 30 EMCCLK
- 31 FOE_B
- 32 FWE_FCS2_B
- 33 I2C_SCLK
- 34 PERSTN1_I2C_SDA
- 35 PERSTN0
- 36 SMBALERT
- 37 RS0
- 38 RS1

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Figure 3-172: **FSVH2104 Package—XCVU33P Configuration/Power Diagram**

FSVH2104 (XCVU35P and XCVU45P)

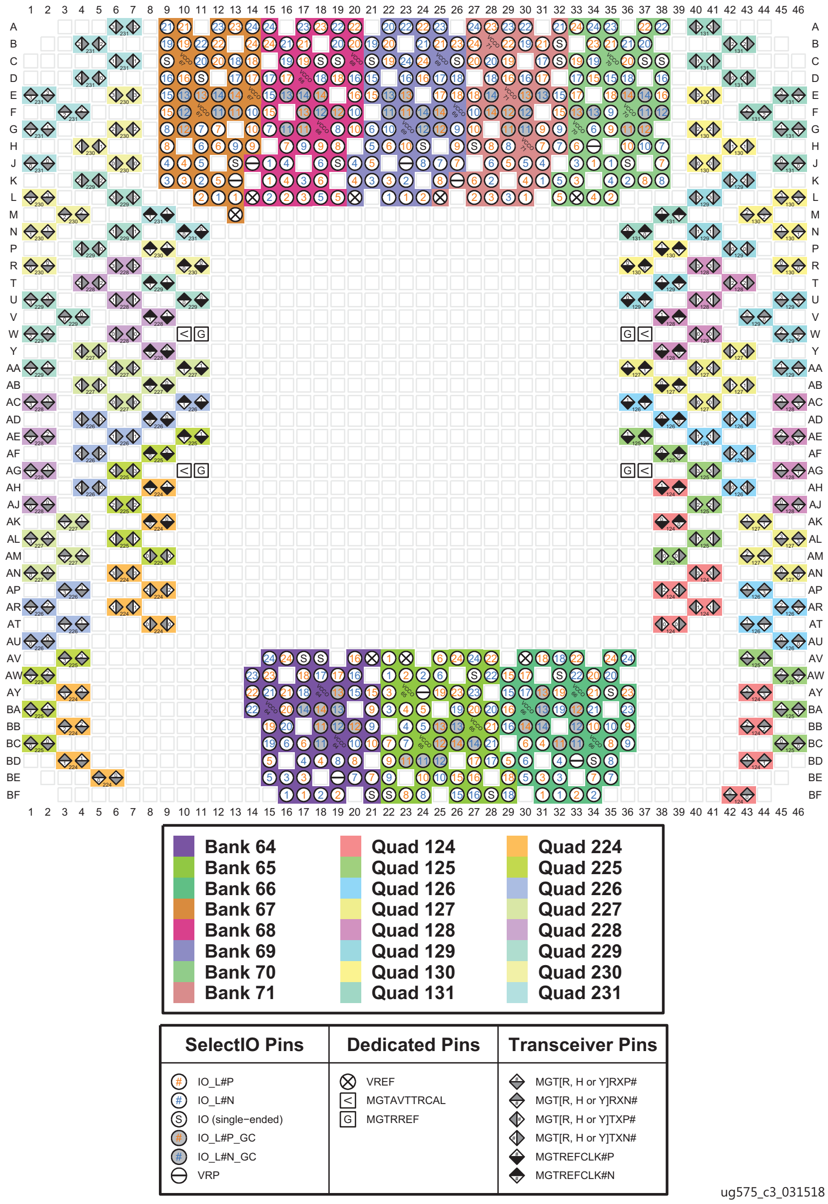


Figure 3-173: **FSVH2104 Package—XCVU35P and XCVU45P I/O Bank Diagram**

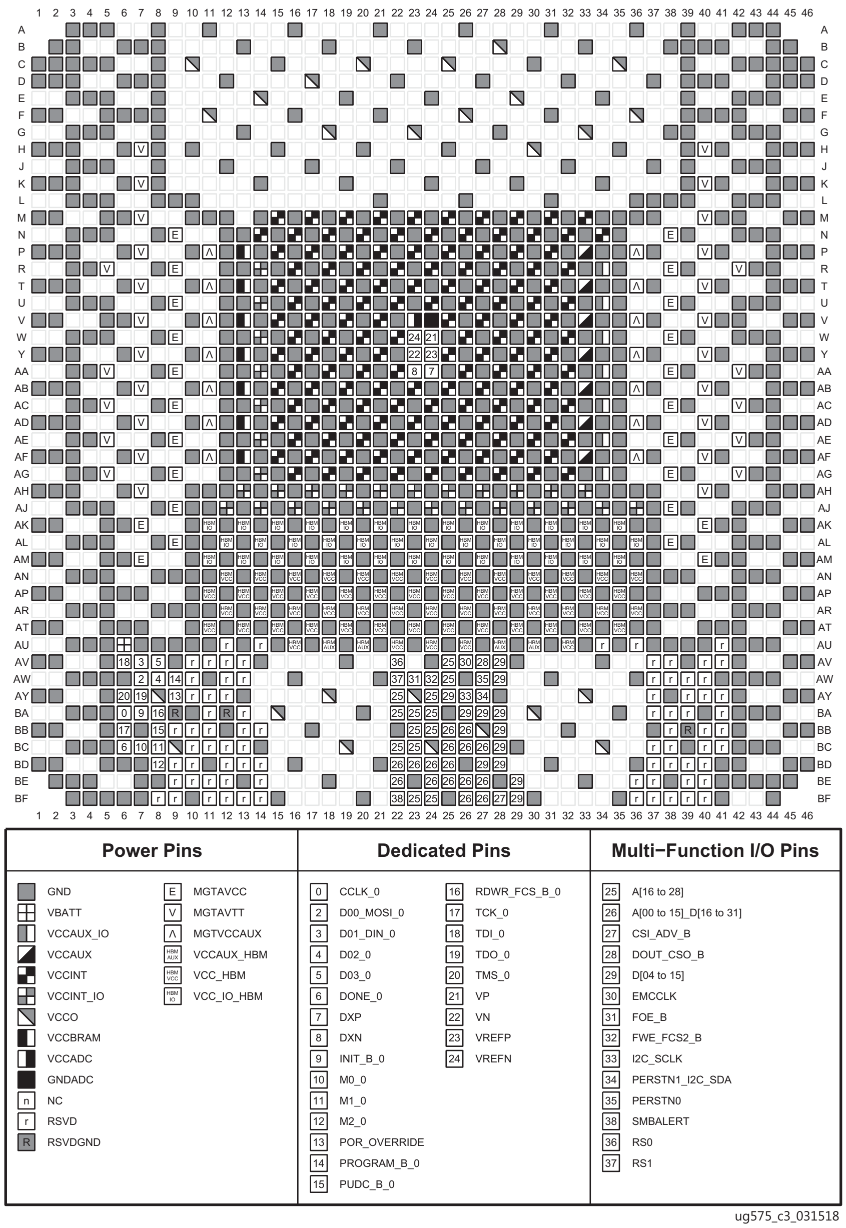


Figure 3-174: **FSVH2104 Package—XCVU35P and XCVU45P Configuration/Power Diagram**

FLGA2577 (XCVU9P)

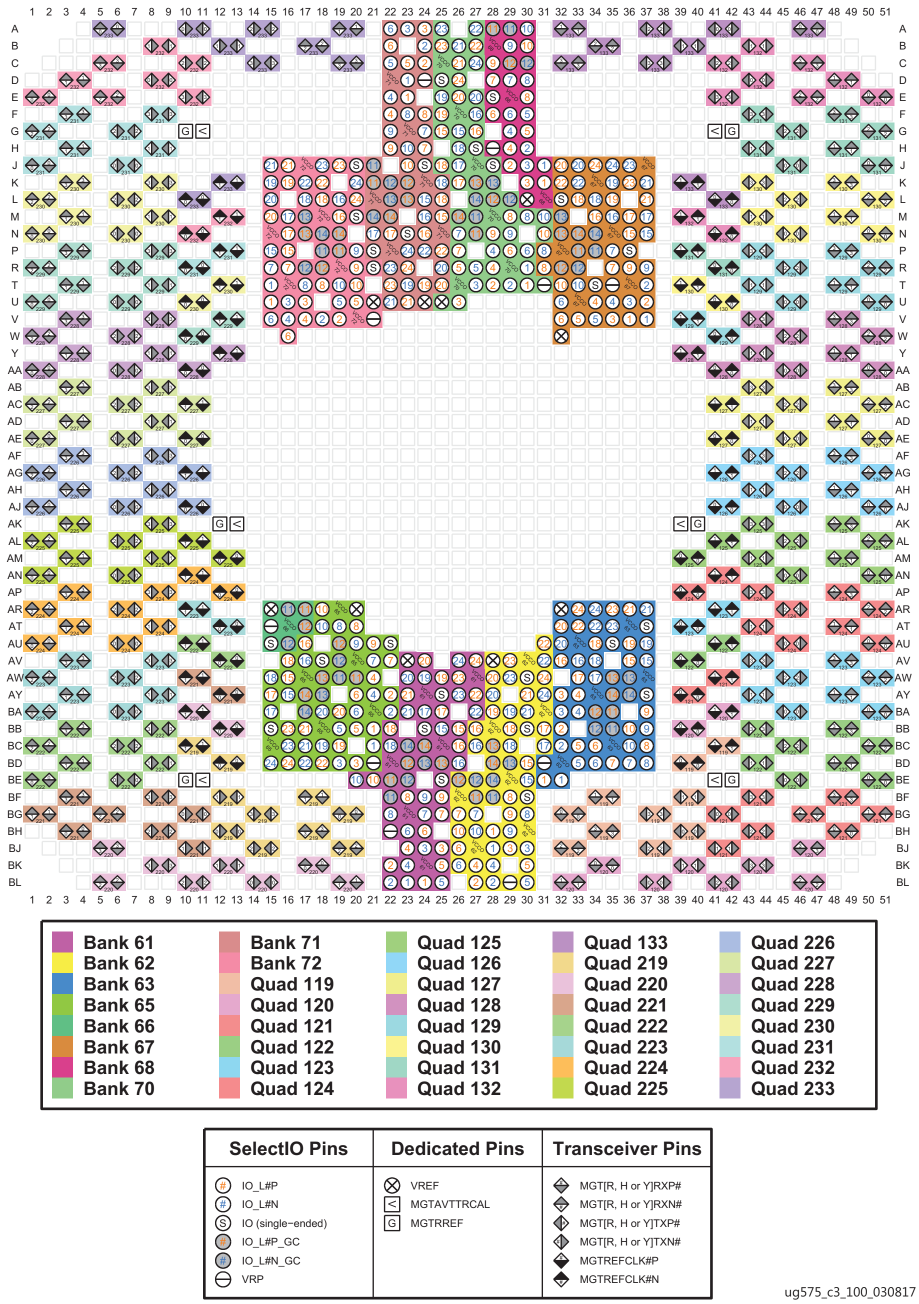


Figure 3-175: **FLGA2577 Package—XCVU9P I/O Bank Diagram**

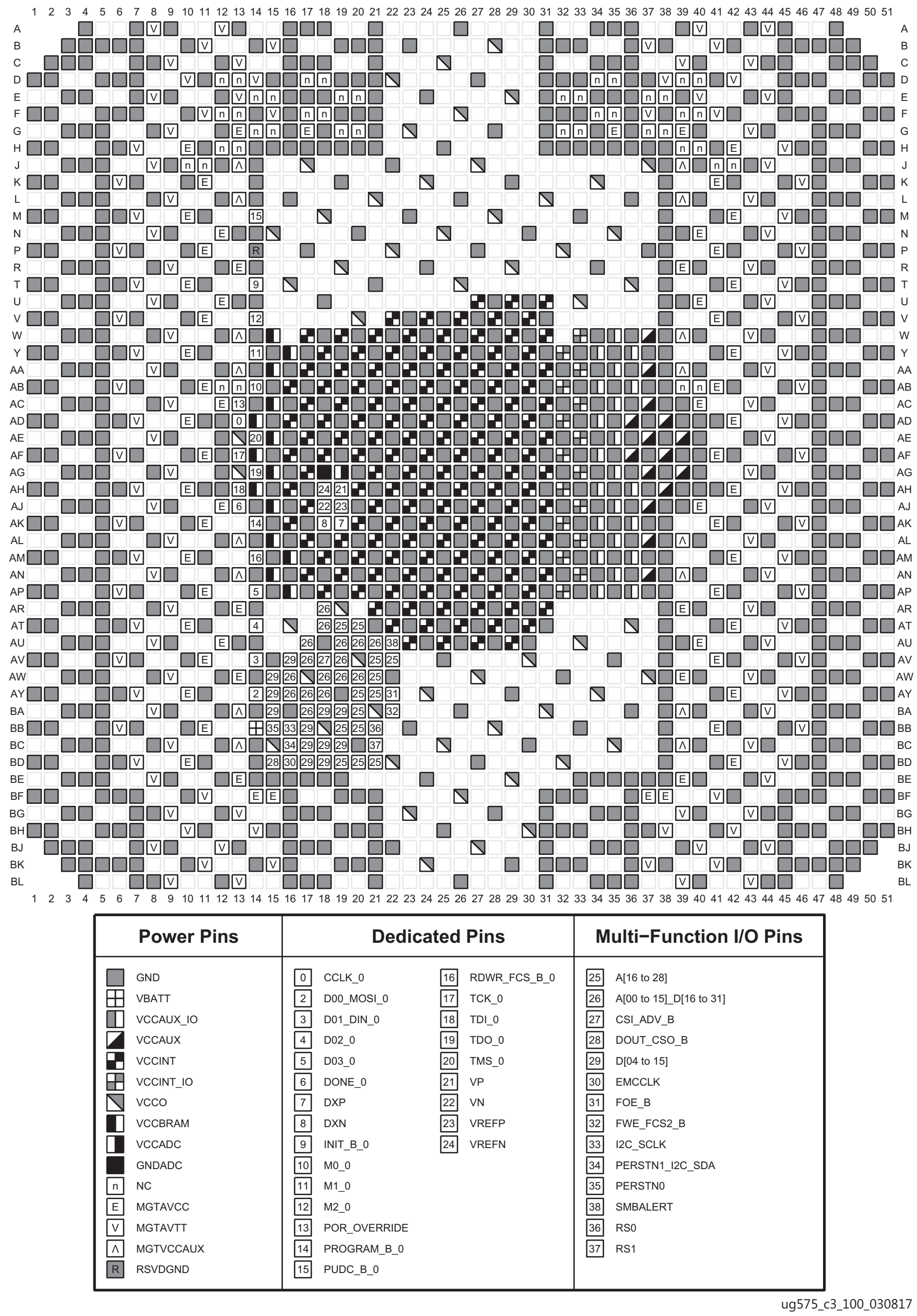


Figure 3-176: **FLGA2577 Package—XCVU9P Configuration/Power Diagram**

FLGA2577 (XCVU11P)

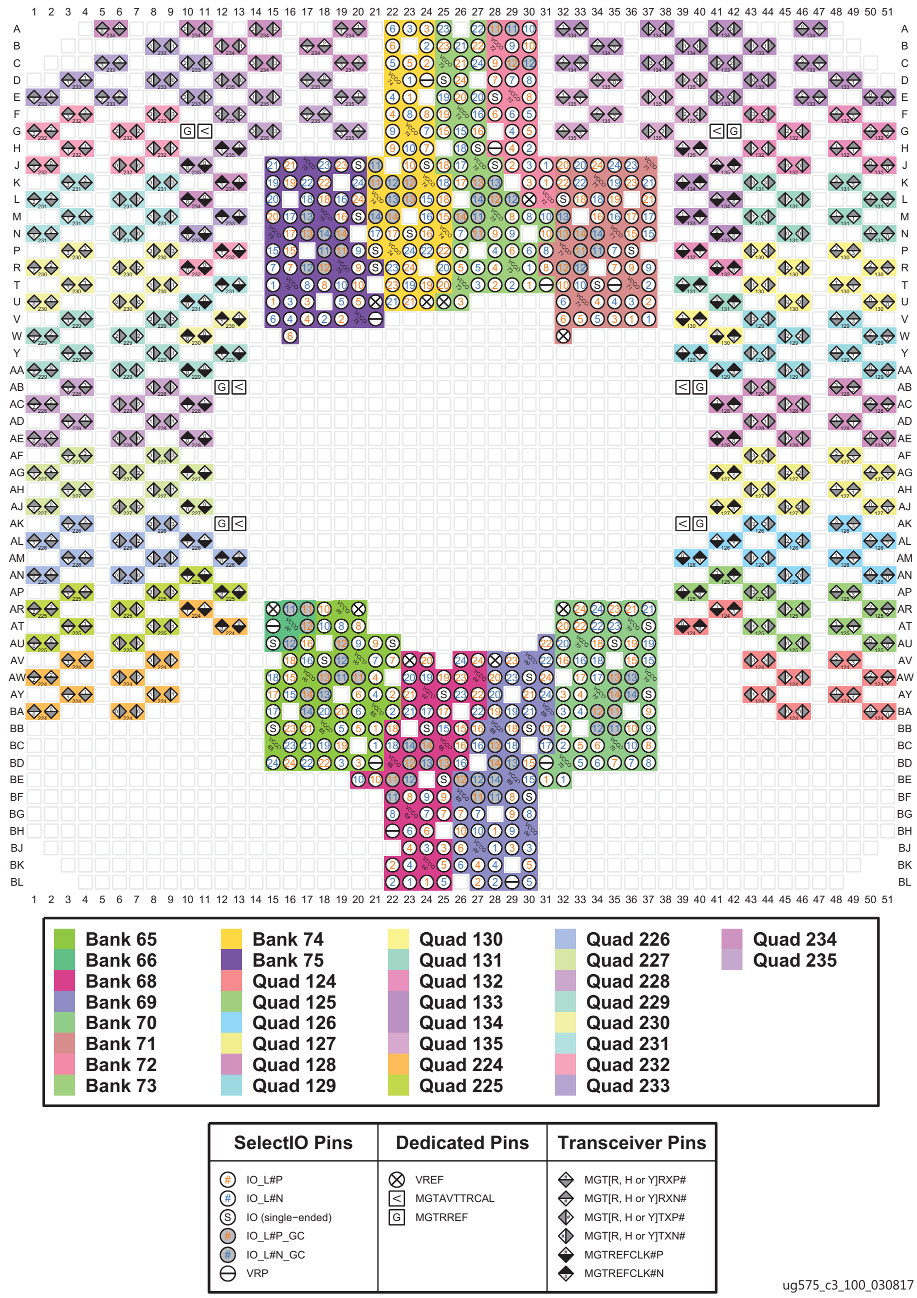


Figure 3-177: **FLGA2577 Package—XCVU11P I/O Bank Diagram**

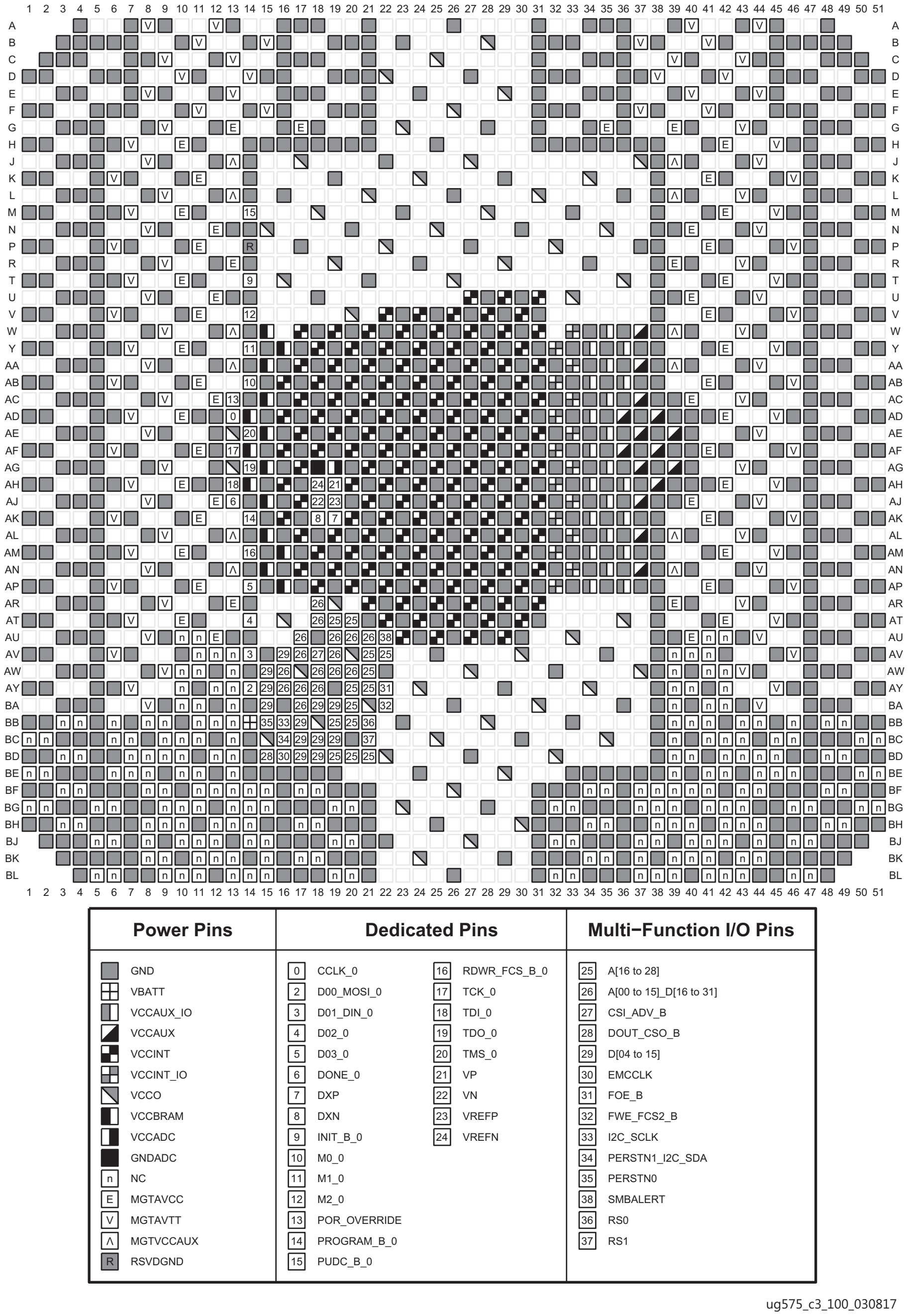


Figure 3-178: **FLGA2577 Package—XCVU11P Configuration/Power Diagram**

FLGA2577 and FSGA2577 (XCVU13P)

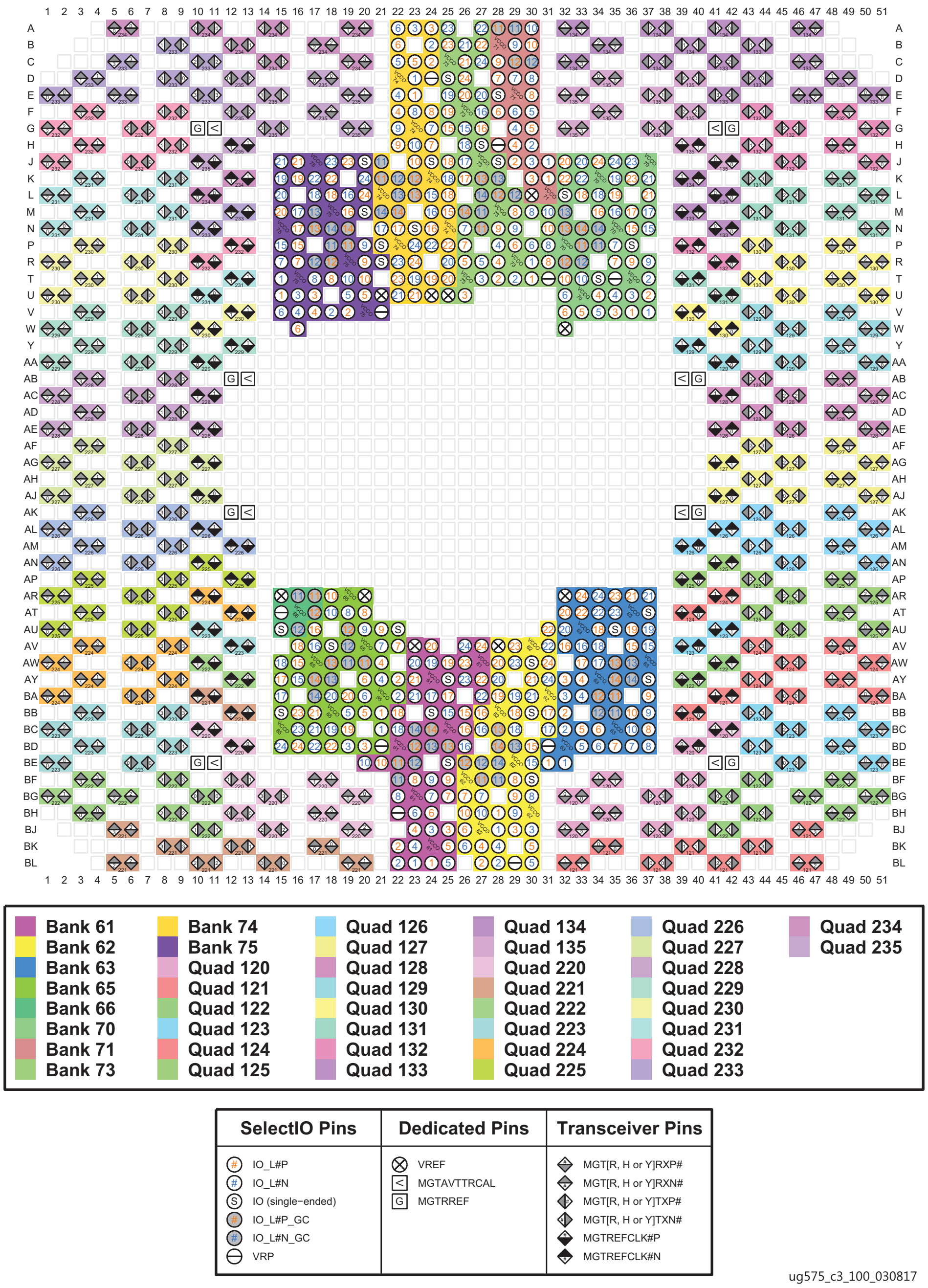


Figure 3-179: **FLGA2577 and FSGA2577 Packages—XCVU13P I/O Bank Diagram**

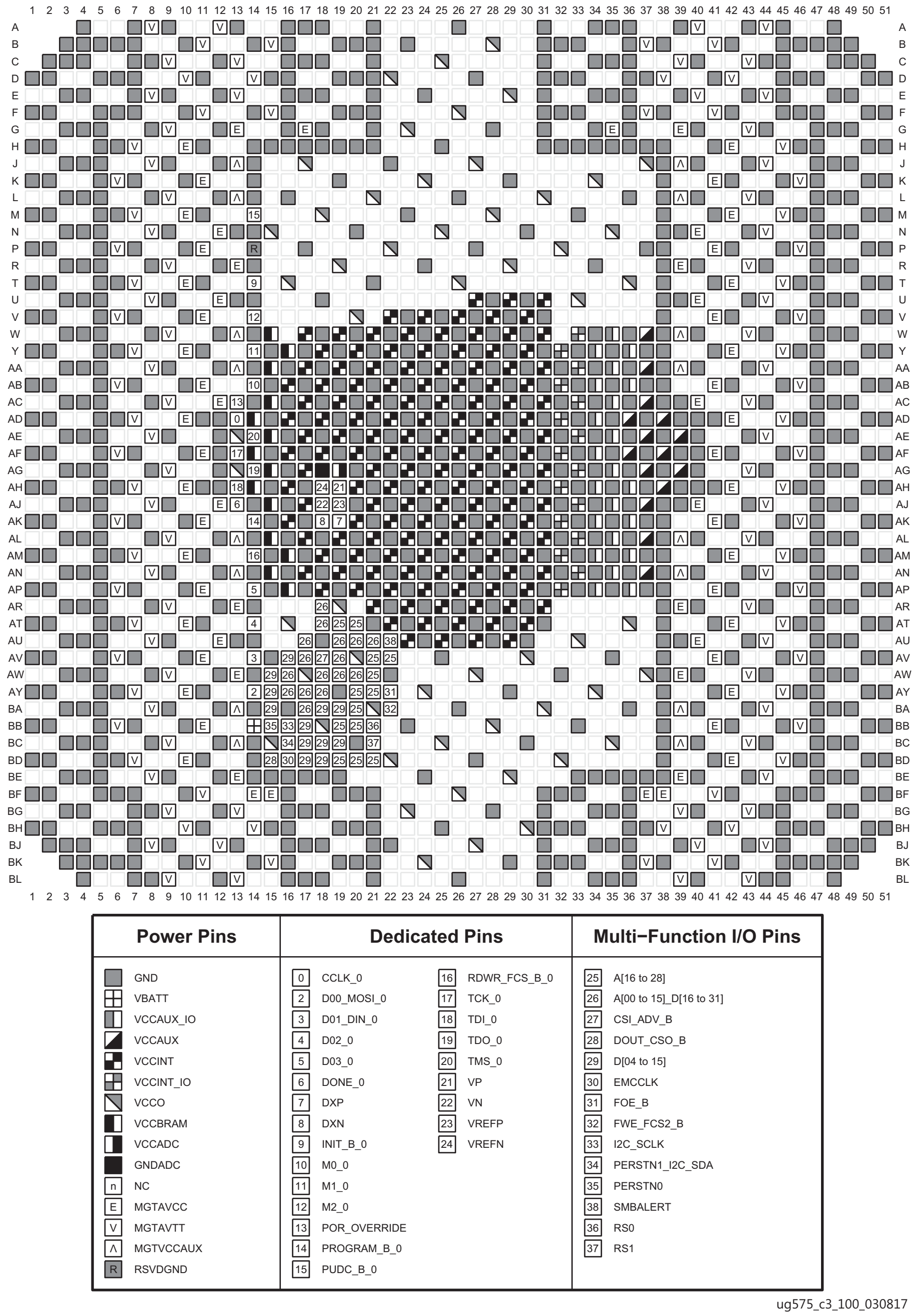


Figure 3-180: **FLGA2577 and FSGA2577 Packages—XCVU13P Configuration/Power Diagram**

FSGA2577 (XCVU27P)

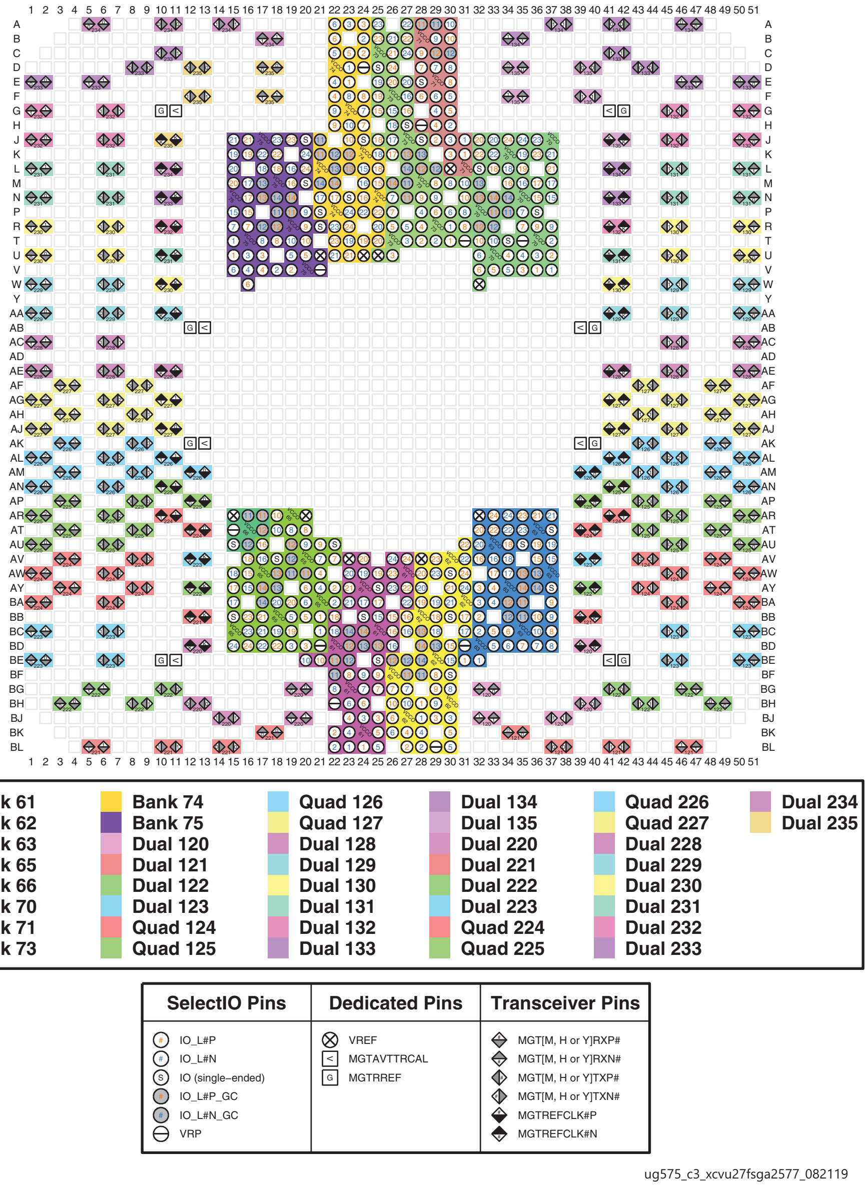


Figure 3-181: **FSGA2577 Package—XCVU27P I/O Bank Diagram**

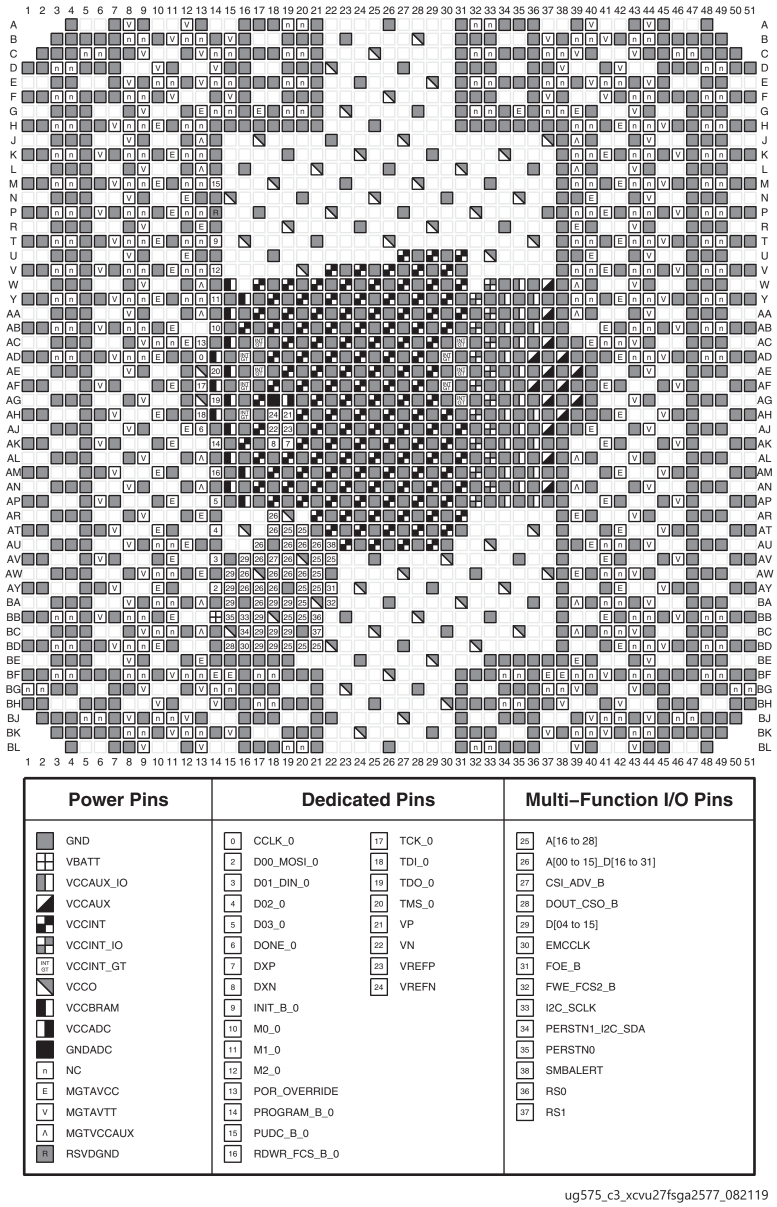


Figure 3-182: **FSGA2577 Package—XCVU27P Configuration/Power Diagram**

FSGA2577 (XCVU29P)

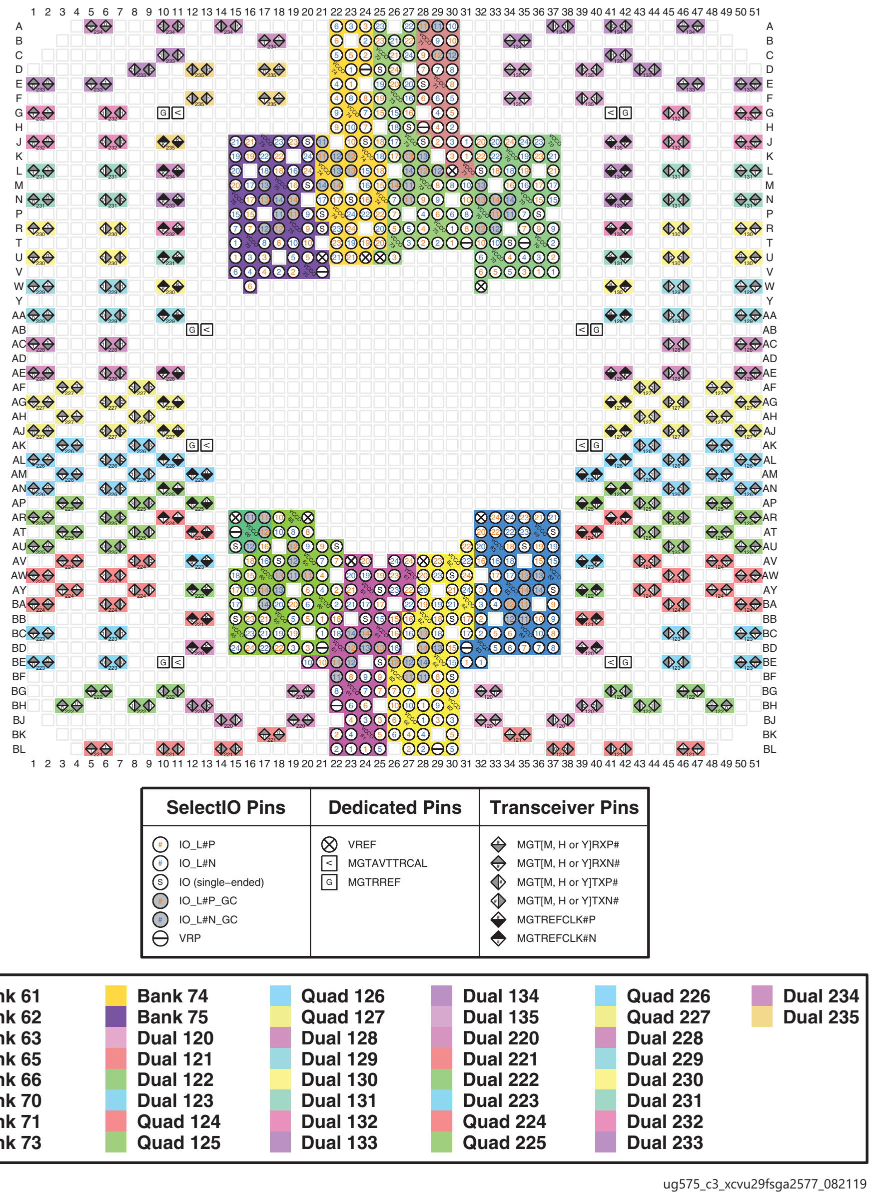


Figure 3-183: **FSGA2577 Package—XCVU29P I/O Bank Diagram**

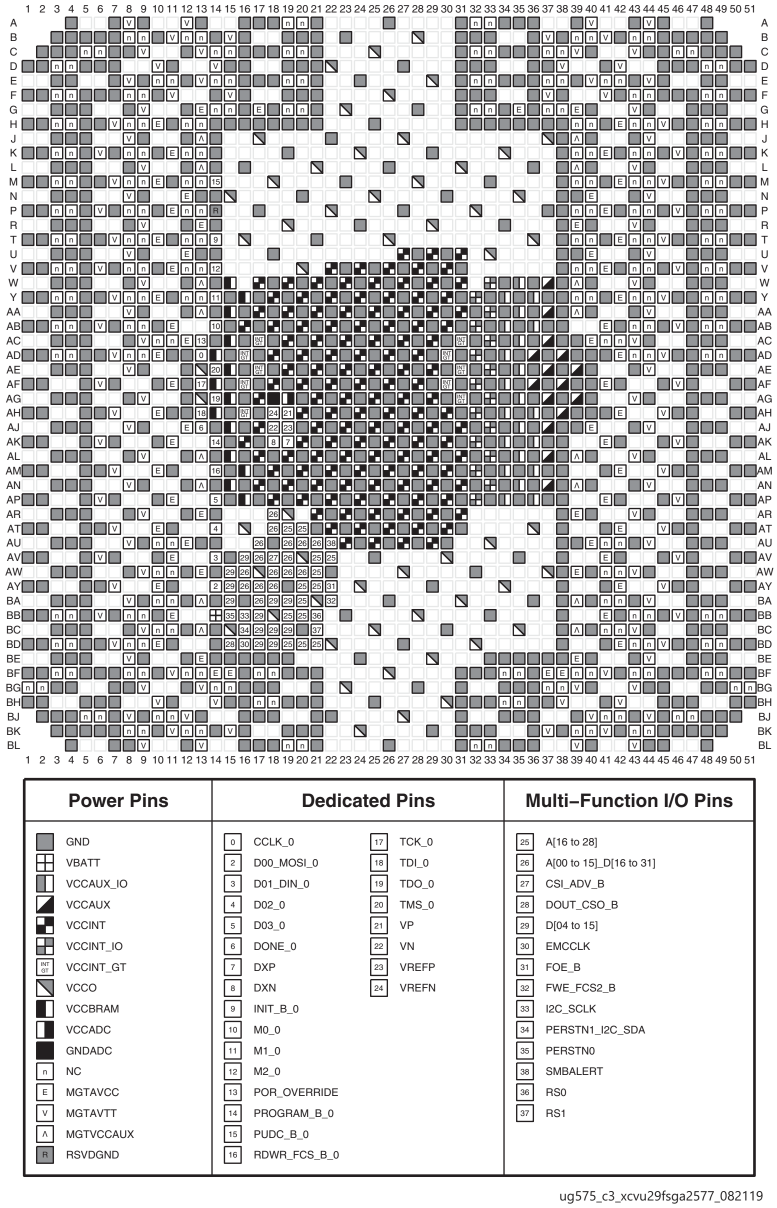


Figure 3-184: **FSGA2577 Package—XCVU29P Configuration/Power Diagram**

FSVH2892 (XCVU35P and XCVU45P)

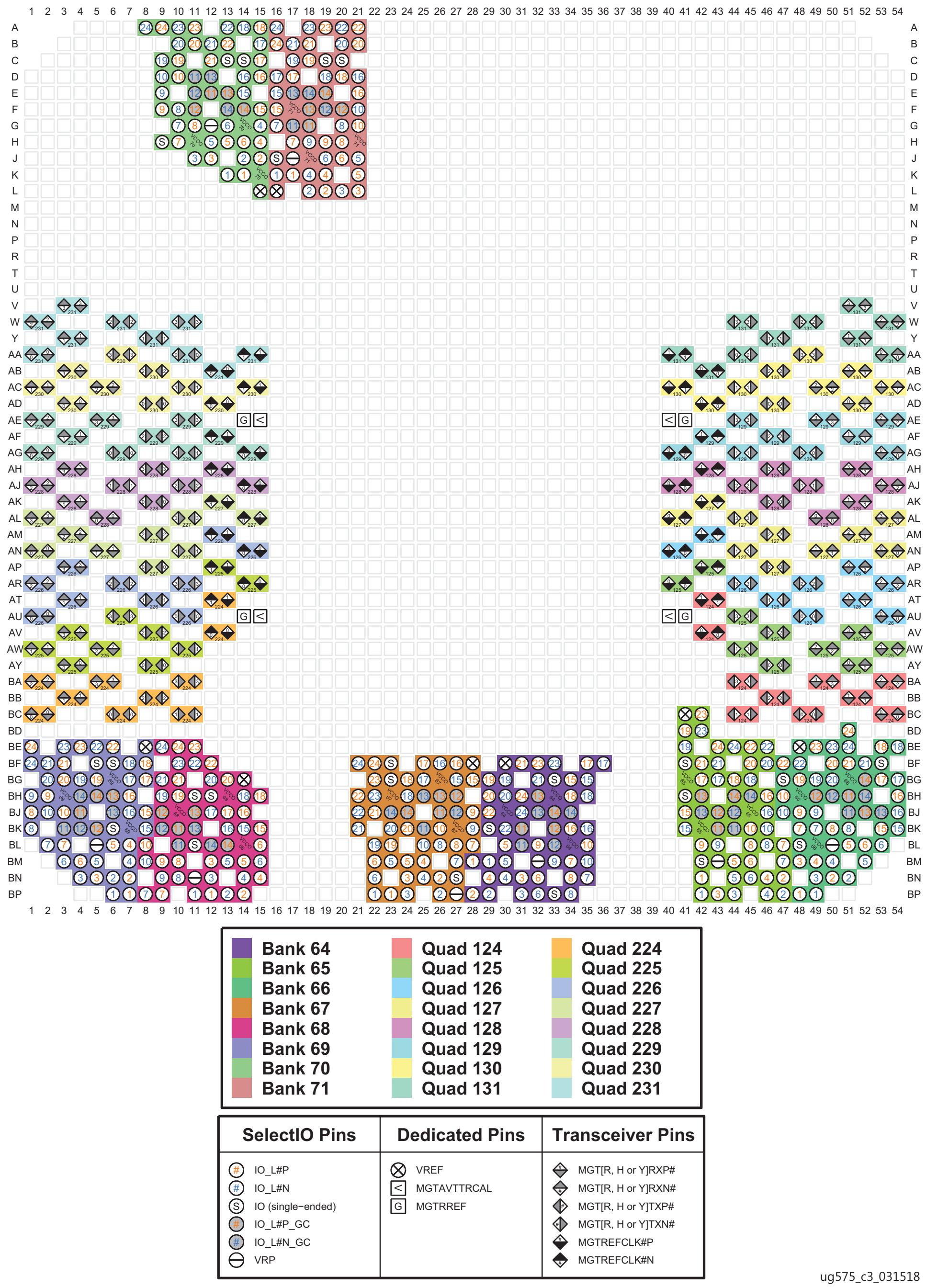


Figure 3-185: **FSVH2892 Package—XCVU35P and XCVU45P I/O Bank Diagram**

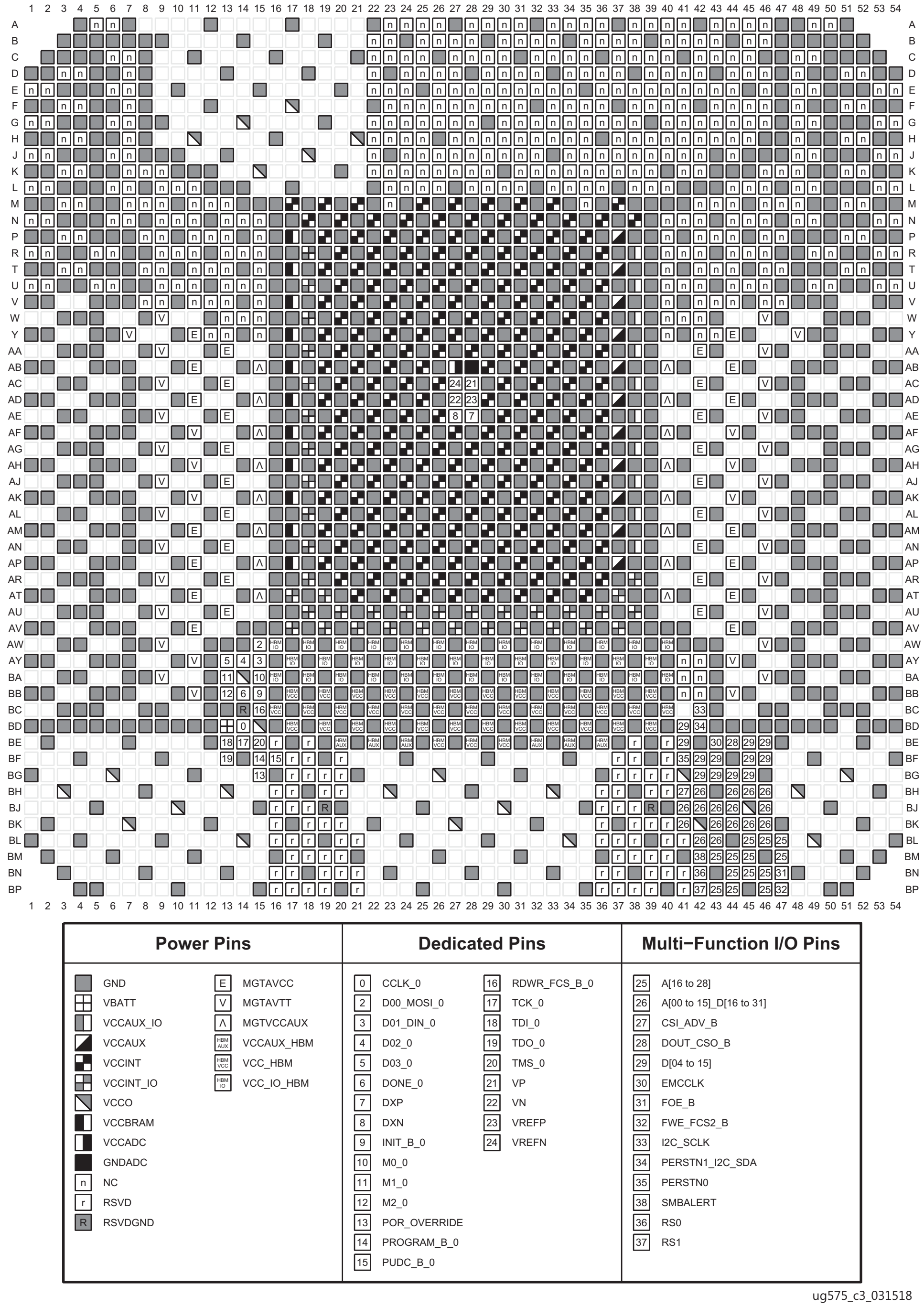


Figure 3-186: **FSVH2892 Package—XCVU35P and XCVU45P Configuration/Power Diagram**

FSVH2892 (XCVU37P and XCVU47P)

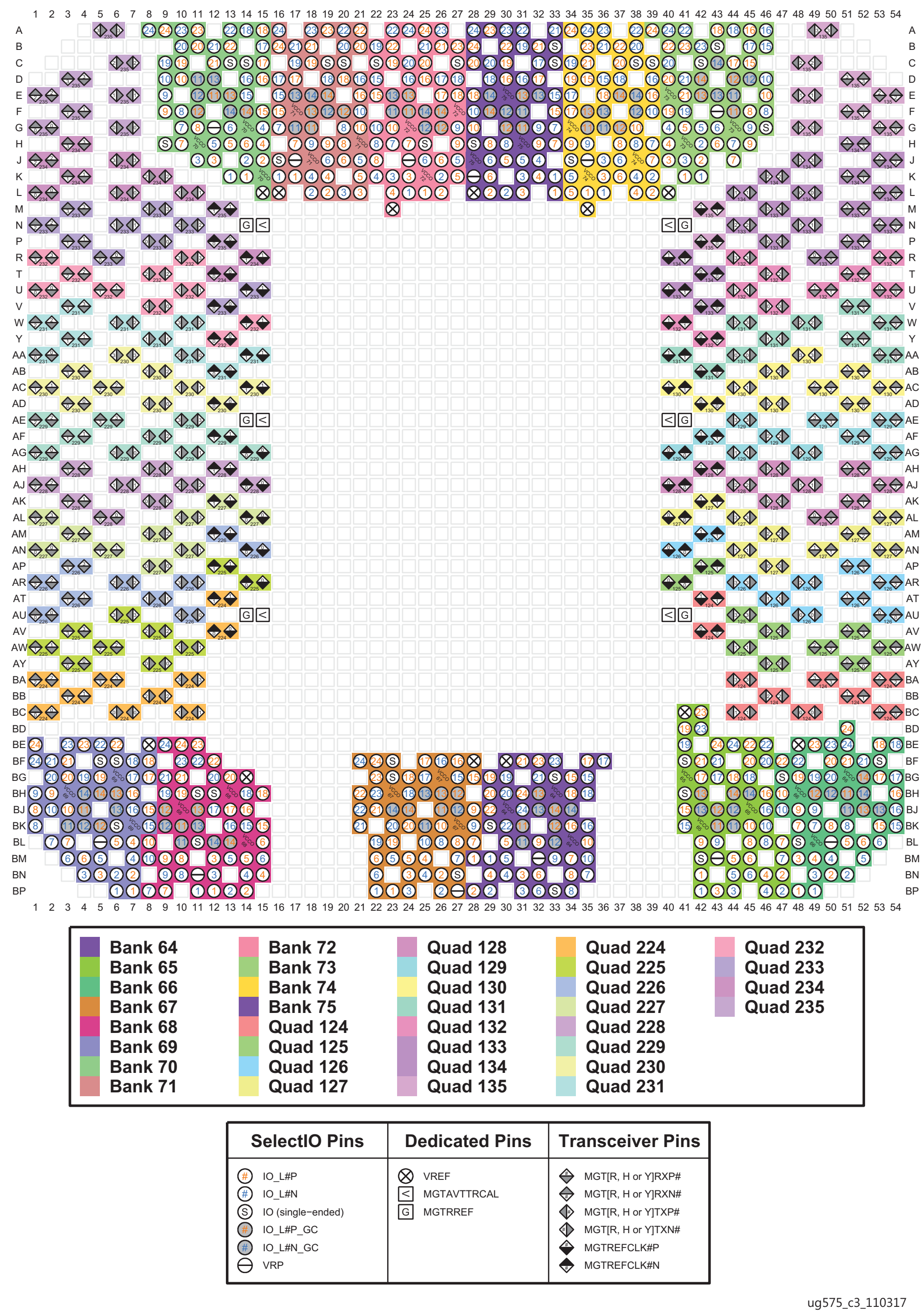


Figure 3-187: **FSVH2892 Package—XCVU37P and XCVU47P I/O Bank Diagram**

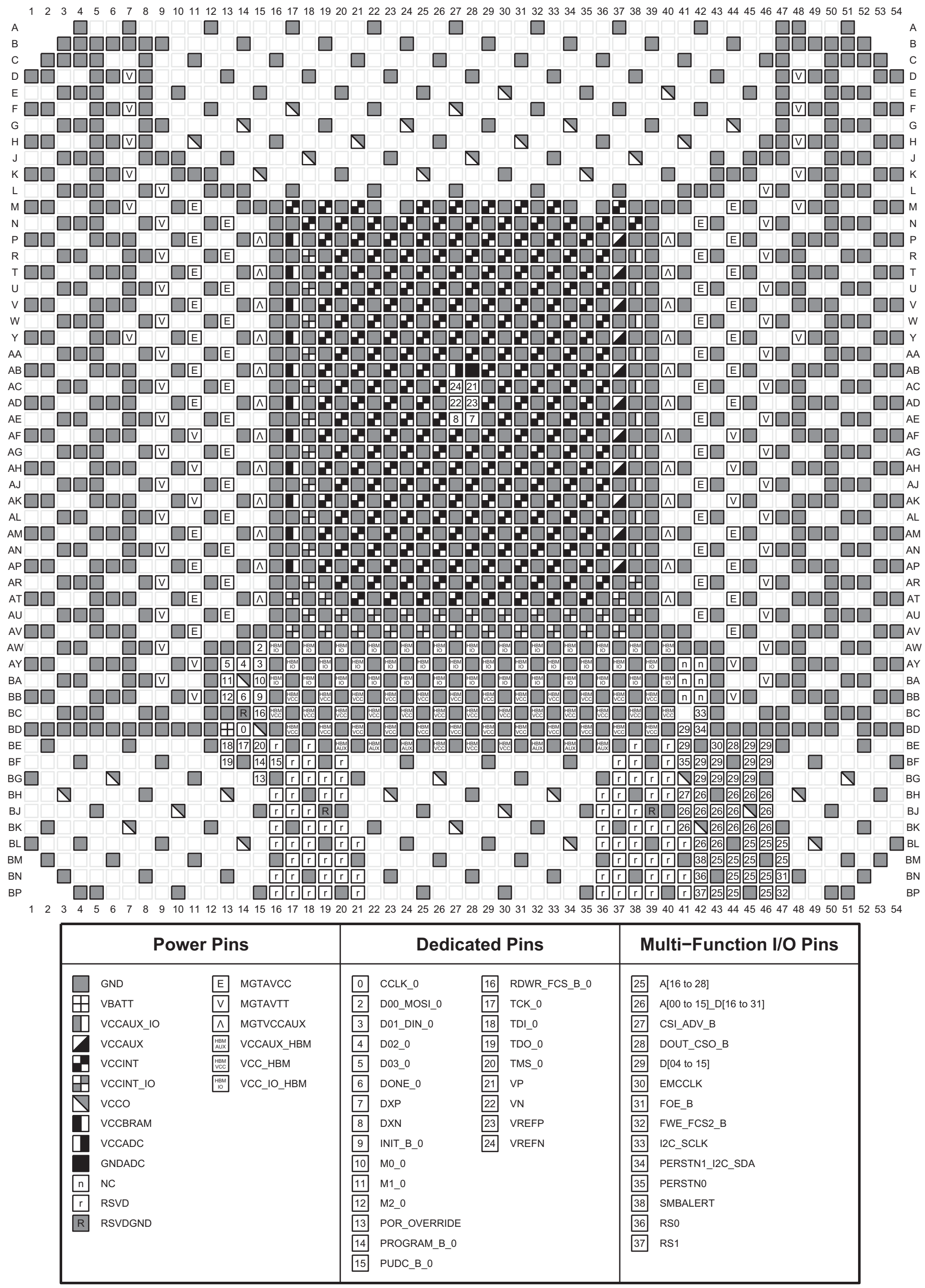


Figure 3-188: **FSVH2892 Package—XCVU37P and XCVU47P Configuration/Power Diagram**

FSVK2892 (XCVU57P)

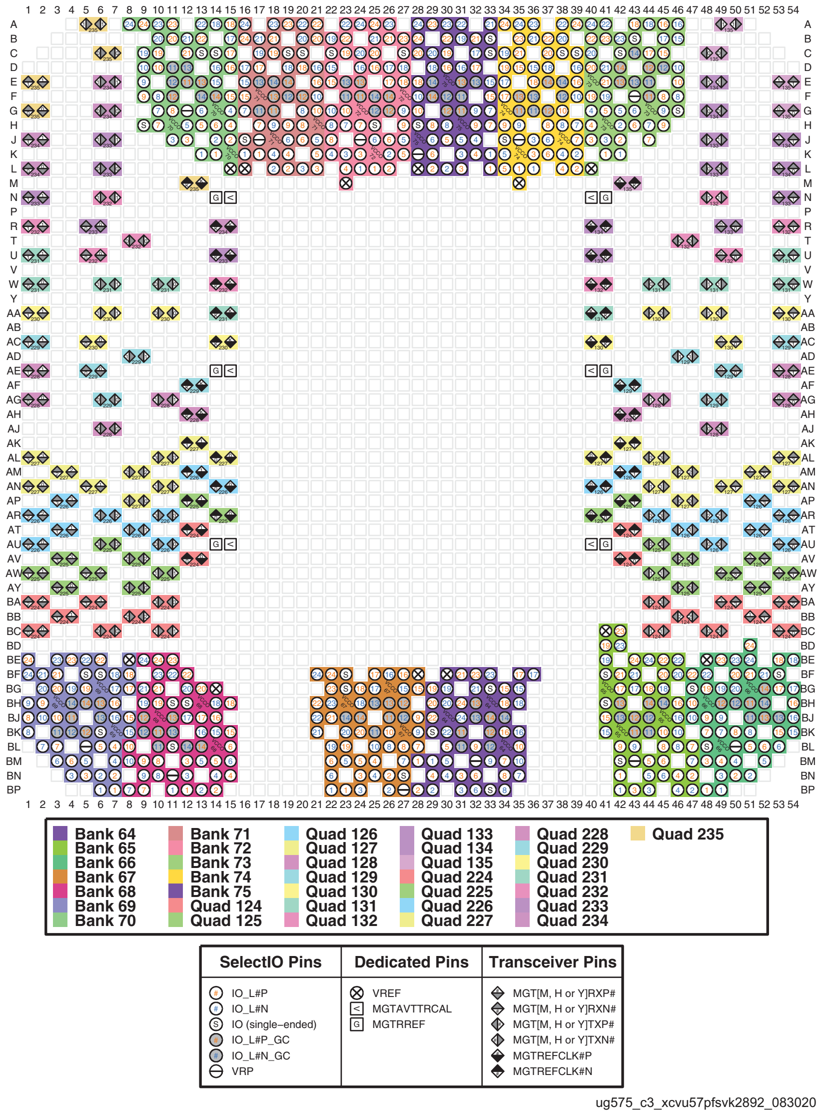


Figure 3-189: **FSVK2892 Package—XCVU57P I/O Bank Diagram**

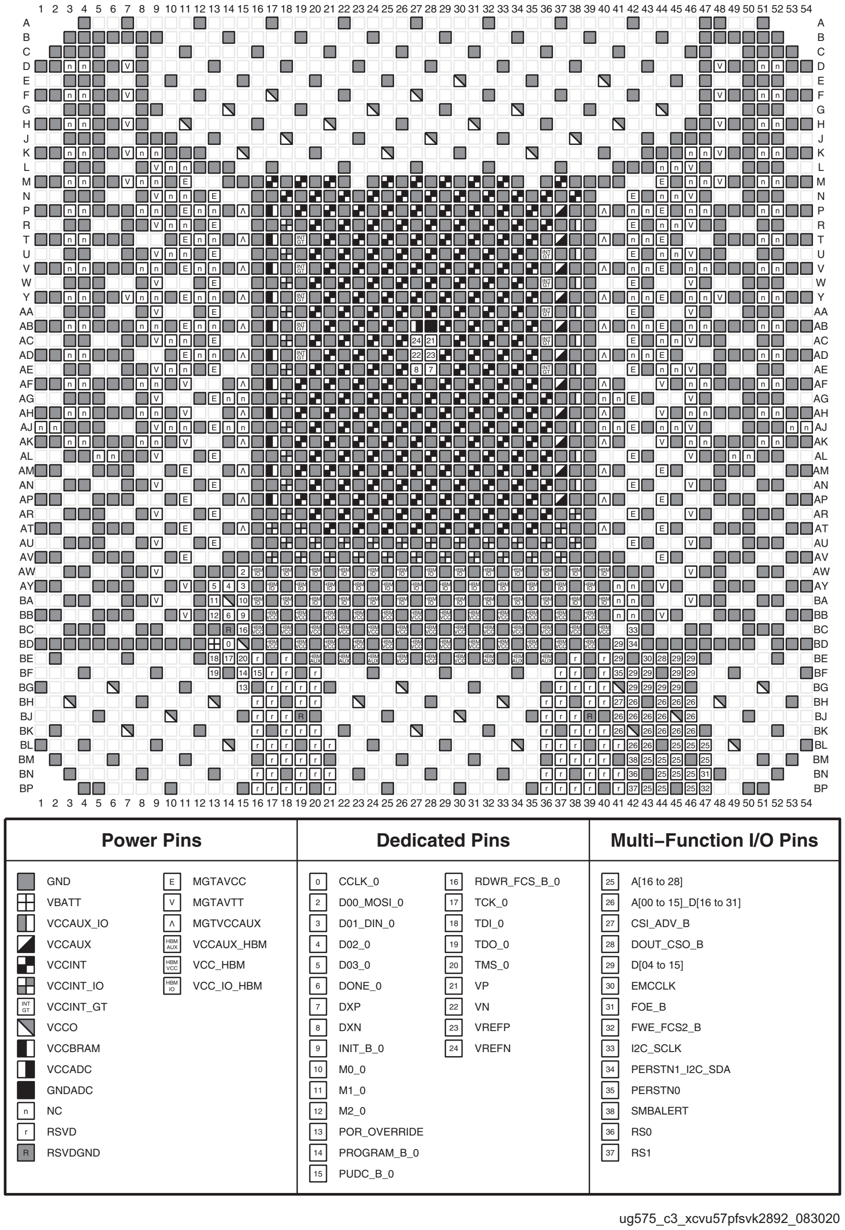


Figure 3-190: **FSVK2892 Package—XCVU57P Configuration/Power Diagram**

FSVA3824 (XCVU19P)

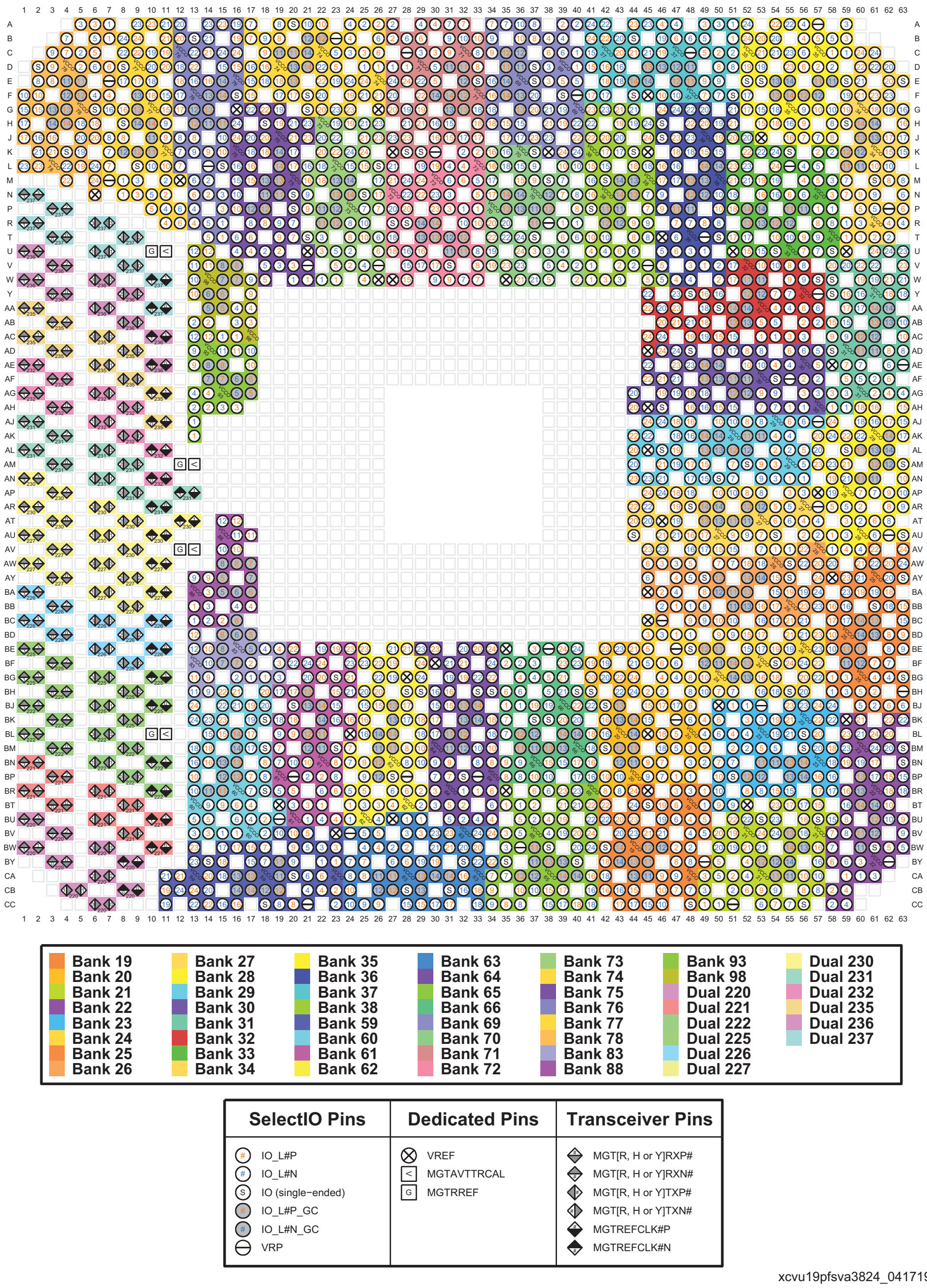
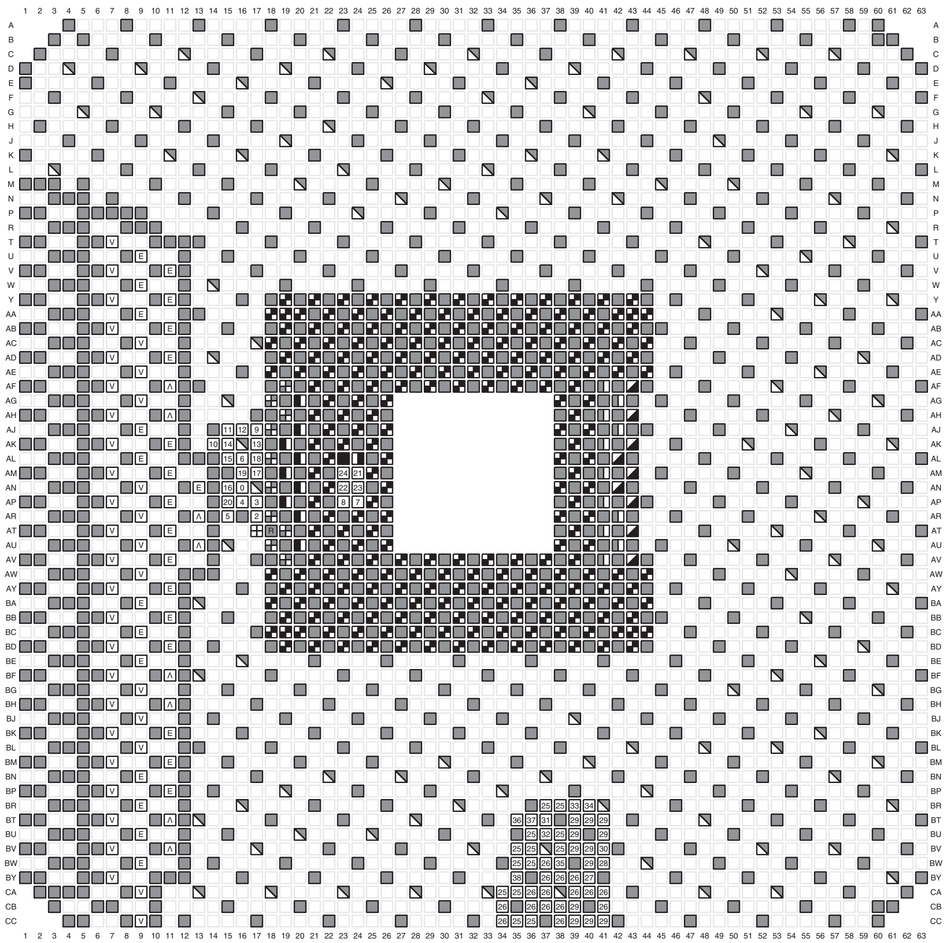


Figure 3-192: **FSVA3824 Package—XCVU19P I/O Bank Diagram**



Power Pins	Dedicated Pins		Multi-Function I/O Pins
GND	0 CCLK_0	16 RDWR_FCS_B_0	25 A[16 to 28]
VBATT	2 D00_MOSI_0	17 TCK_0	26 A[00 to 15]_D[16 to 31]
VCCAUX_IO	3 D01_DIN_0	18 TDI_0	27 CSI_ADV_B
VCCAUX	4 D02_0	19 TDO_0	28 DOUT_CSO_B
VCCINT	5 D03_0	20 TMS_0	29 D[04 to 15]
VCCINT_IO	6 DONE_0	21 VP	30 EMCCLK
VCCO	7 DXP	22 VN	31 FOE_B
VCCBRAM	8 DXN	23 VREFP	32 FWE_FCS2_B
VCCADC	9 INIT_B_0	24 VREFN	33 I2C_SCLK
GNDADC	10 M0_0		34 PERSTN1_I2C_SDA
n NC	11 M1_0		35 PERSTN0
E MGTAVCC	12 M2_0		38 SMBALERT
V MGTAVTT	13 POR_OVERRIDE		36 RS0
Λ MGTVCCAUX	14 PROGRAM_B_0		37 RS1
R RSVDGND	15 PUDC_B_0		

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Figure 3-193: **FSVA3824 Package—XCVU19P Configuration/Power Diagram**

FSVB3824 (XCVU19P)

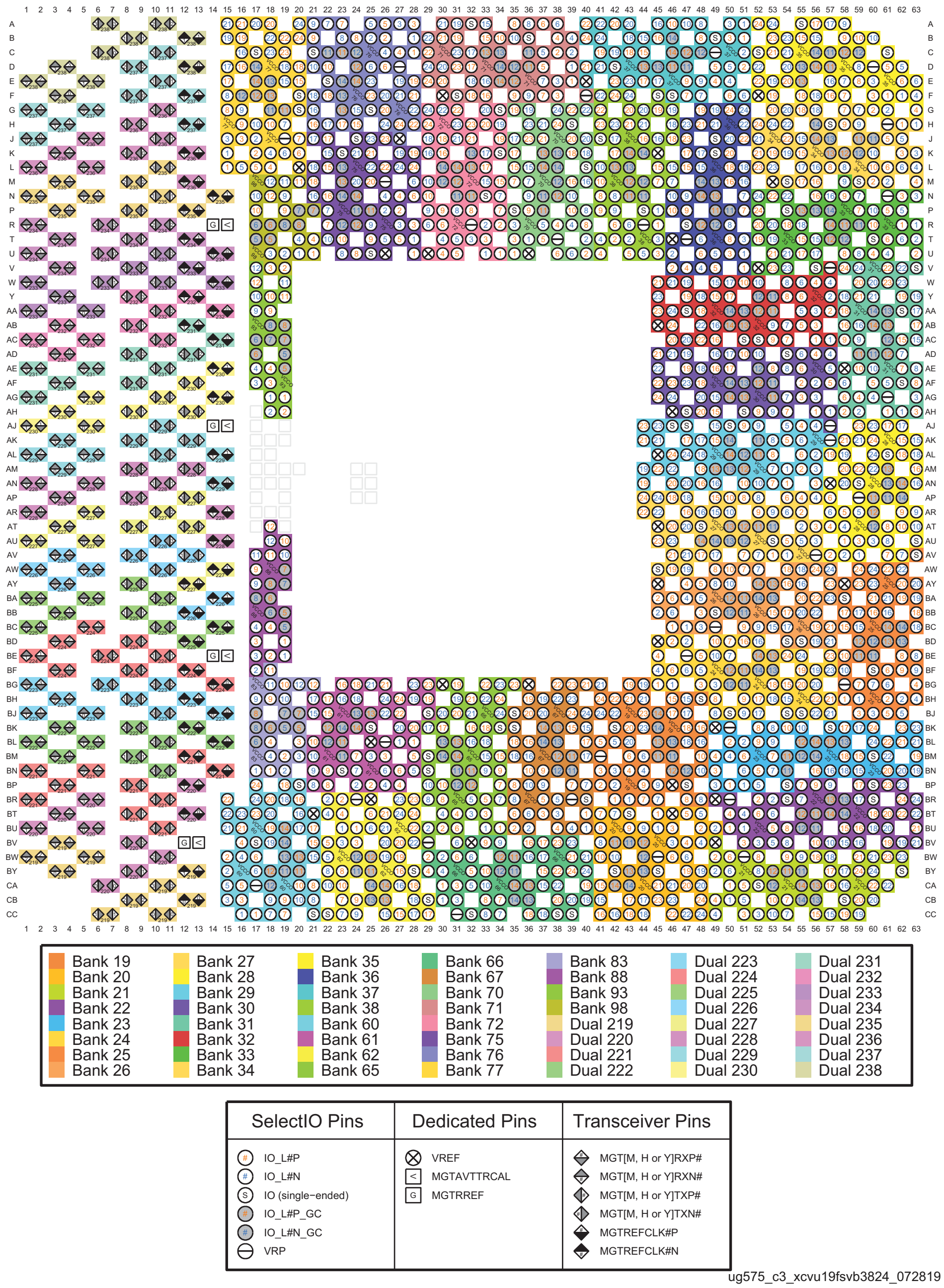


Figure 3-194: **FSVB3824 Package—XCVU19P I/O Bank Diagram**

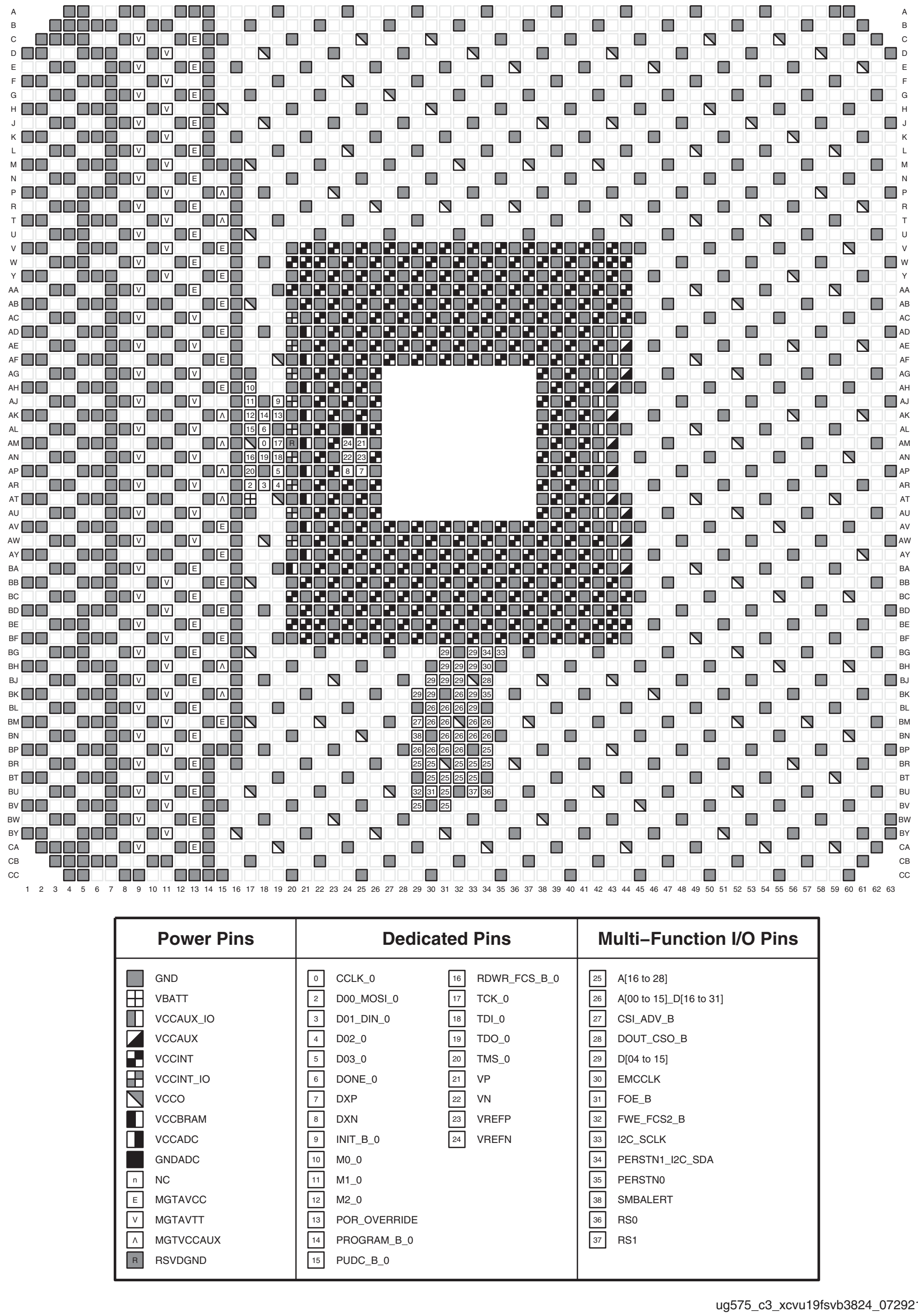


Figure 3-195: **FSVB3824 Package—XCVU19P Configuration/Power Diagram**

VSVA1365 (XCVU23P)

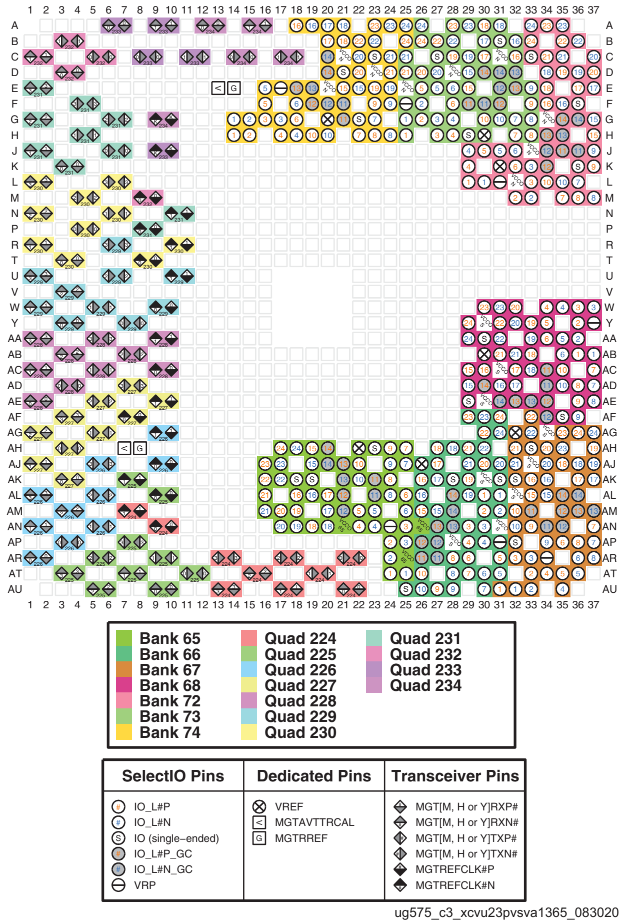


Figure 3-196: **VSVA1365 Package—XCVU23P I/O Bank Diagram**

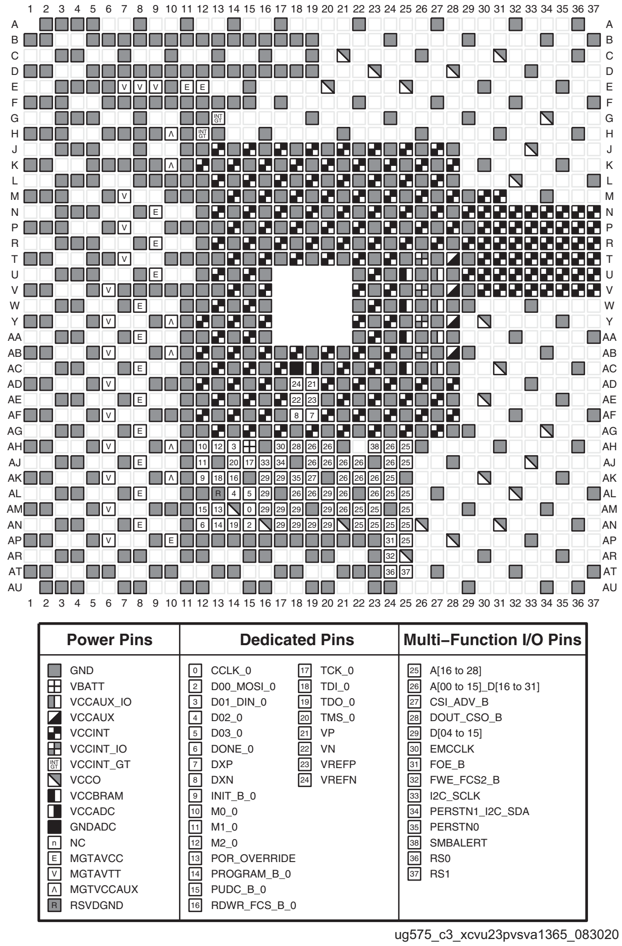


Figure 3-197: **VSVA1365 Package—XCVU23P Configuration/Power Diagram**

CMVA361 (XCSU10P)

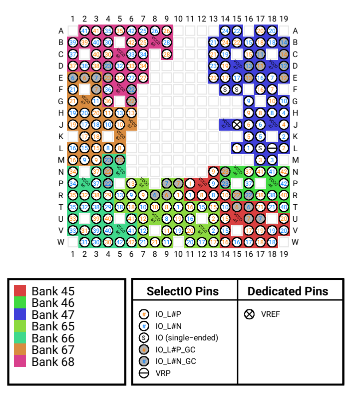


Figure 3-198: **CMVA361 Package—XCSU10P I/O Bank Diagram**

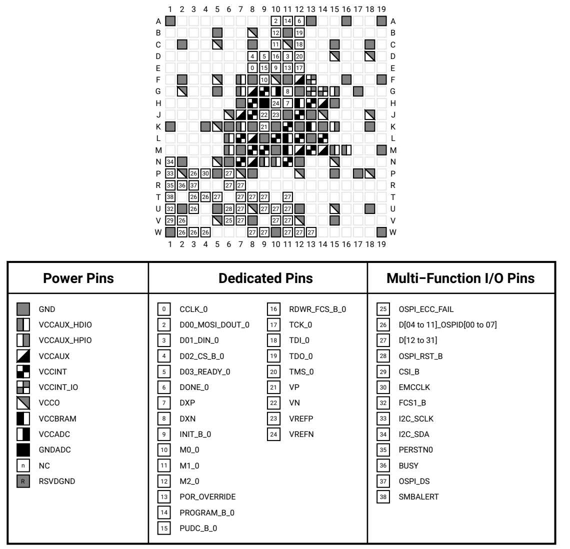


Figure 3-199: **CMVA361 Package—XCSU10P Configuration/Power Diagram**

CMVA361 (XCSU25P)

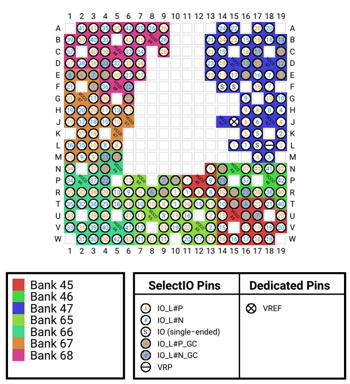


Figure 3-200: **CMVA361 Package—XCSU25P I/O Bank Diagram**

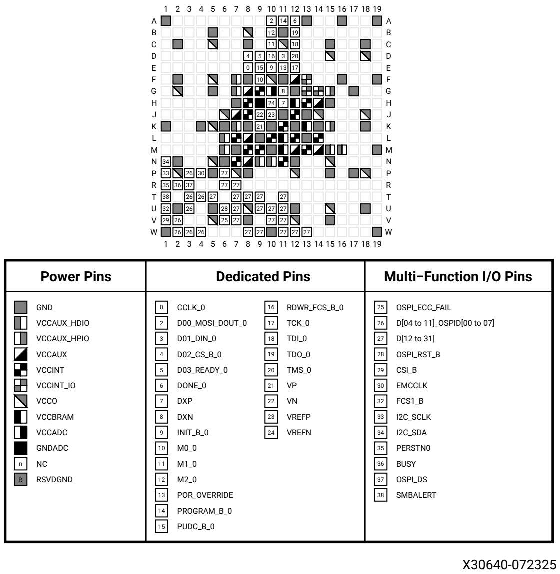


Figure 3-201: **CMVA361 Package—XCSU25P Configuration/Power Diagram**

CMVA361 (XCSU35P)

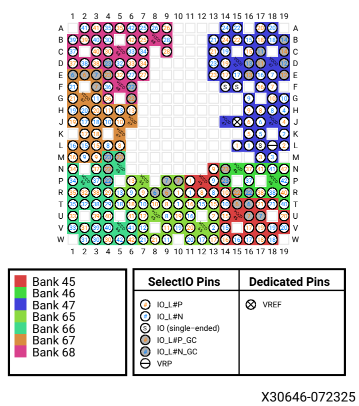


Figure 3-202: **CMVA361 Package—XCSU35P I/O Bank Diagram**

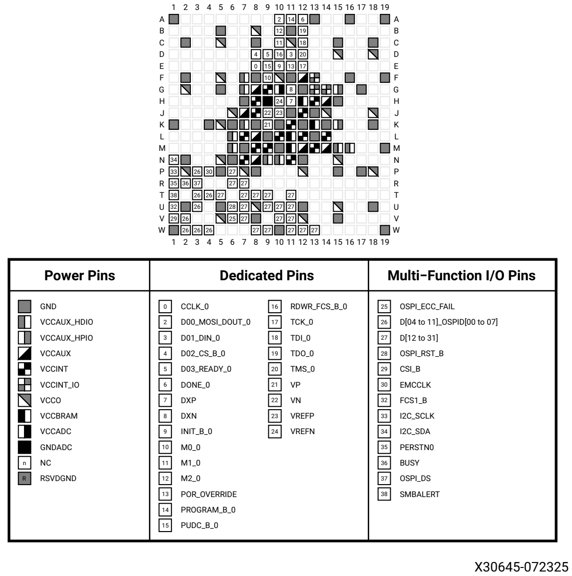


Figure 3-203: **CMVA361 Package—XCSU35P Configuration/Power Diagram**

CMVA529 (XCSU10P)

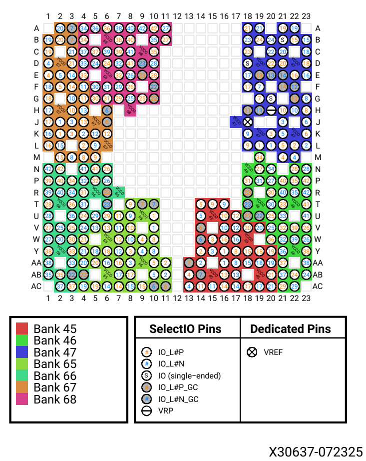


Figure 3-204: **CMVA529 Package—XCSU10P I/O Bank Diagram**

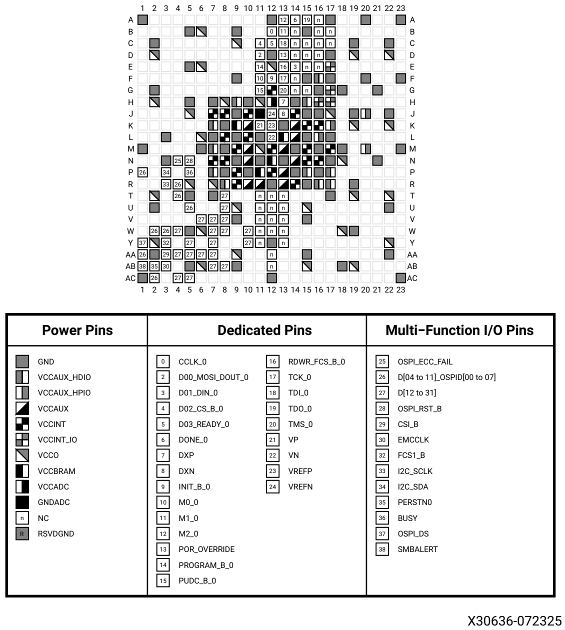


Figure 3-205: **CMVA529 Package—XCSU10P Configuration/Power Diagram**

CMVA529 (XCSU25P)

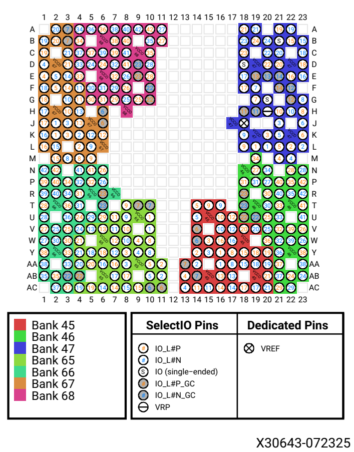


Figure 3-206: **CMVA529 Package—XCSU25P I/O Bank Diagram**

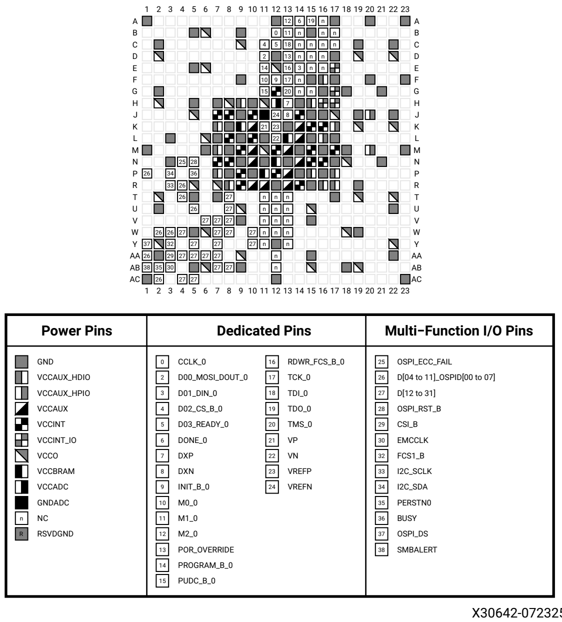


Figure 3-207: **CMVA529 Package—XCSU25P Configuration/Power Diagram**

CMVA529 (XCSU35P)

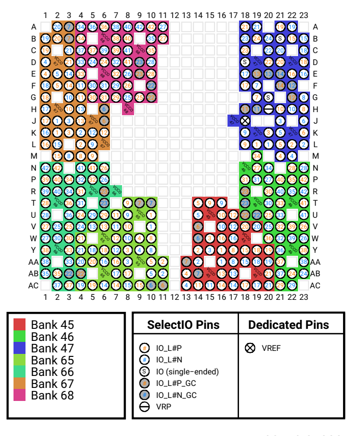


Figure 3-208: **CMVA529 Package—XCSU35P I/O Bank Diagram**

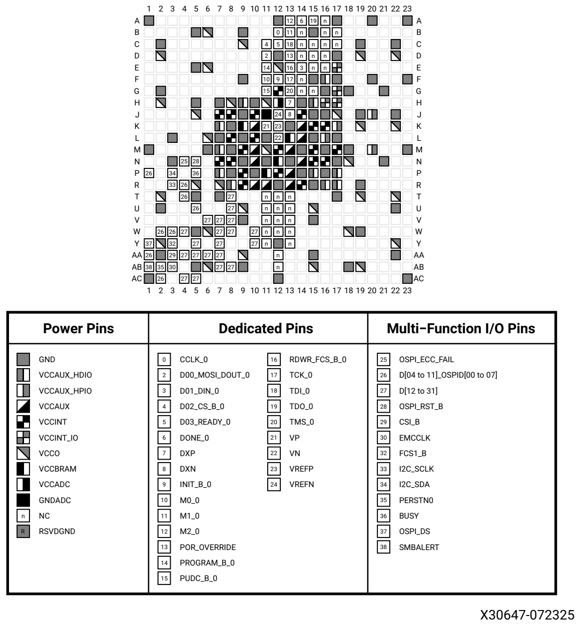


Figure 3-209: **CMVA529 Package—XCSU35P Configuration/Power Diagram**

SBVB625 (XCSU10P)

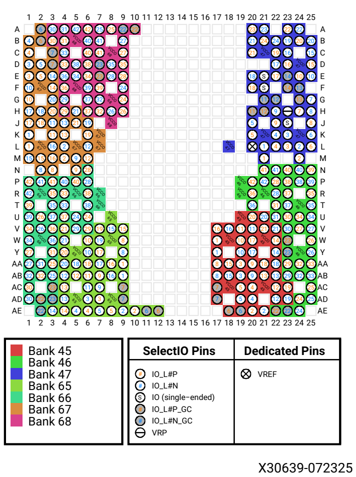


Figure 3-210: **SBVB625 Package—XCSU10P I/O Bank Diagram**

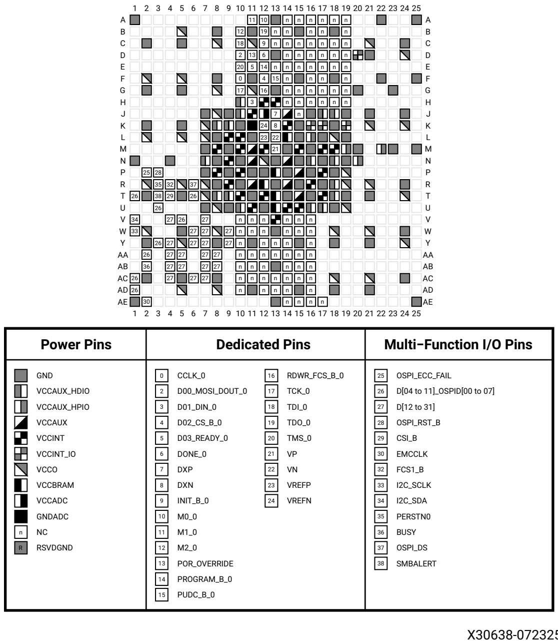


Figure 3-211: **SBVB625 Package—XCSU10P Configuration/Power Diagram**

SBVB625 (XCSU25P)

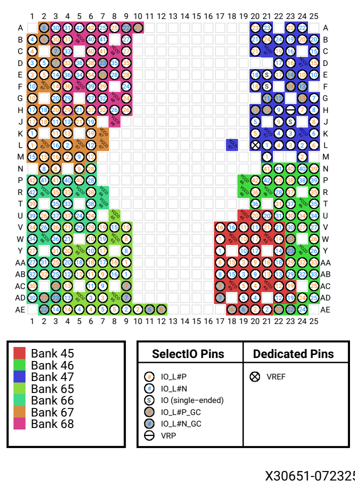


Figure 3-212: **SBVB625 Package—XCSU25P I/O Bank Diagram**

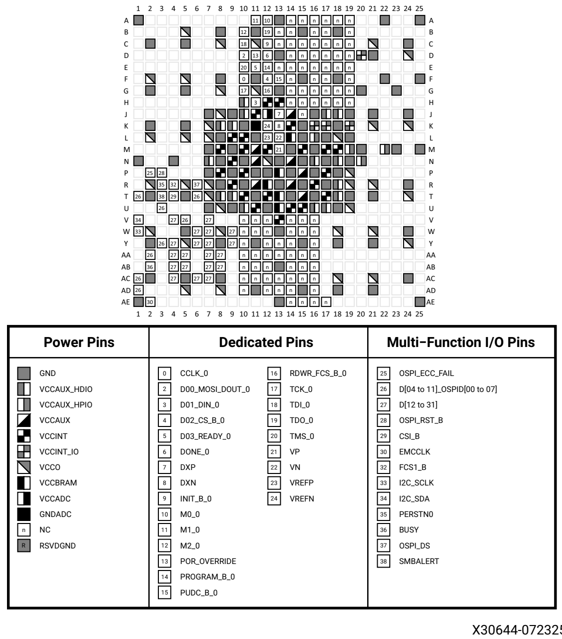


Figure 3-213: **SBVB625 Package—XCSU25P Configuration/Power Diagram**

SBVB625 (XCSU35P)

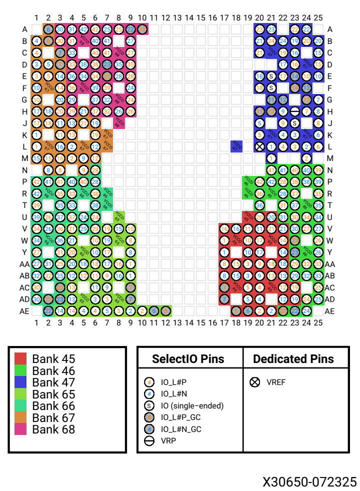


Figure 3-214: **SBVB625 Package—XCSU35P I/O Bank Diagram**

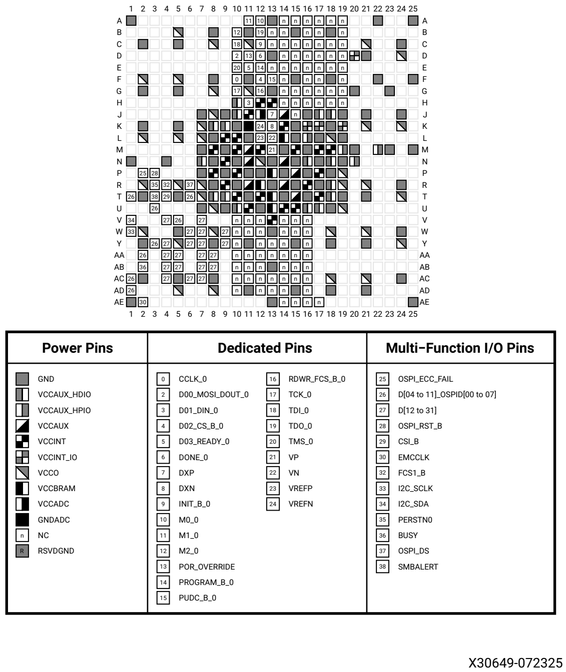


Figure 3-215: **SBVB625 Package—XCSU35P Configuration/Power Diagram**

Chapter 4

Mechanical Drawings

Summary

This chapter provides mechanical drawings (package specifications) of the AMD UltraScale™ and AMD UltraScale+™ device packages. Table 4-1 is a cross-reference to the mechanical drawings by device and package combination.

All AMD Kintex™ and Virtex™ UltraScale+ devices are available in packages with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC and the third digit in the package name replaces the V or G with a Q to delineate the use of eutectic balls on an otherwise XC package. For information on ordering the XQ non-ruggedized eutectic Sn/Pb ball packages, see the XQ UltraScale+ FPGA Ordering Information in the *XQ UltraScale Architecture Data Sheet Overview* (DS895). For the XQ non-ruggedized eutectic Sn/Pb ball packages mechanicals, refer to the XC packages in Table 4-1 because they are built with an XC style package and lid using Pb-free solder inside.

TIP: *For information on materials composition and weight of a device, refer to the material declaration data sheet (MDDS).Click on this link to find the UltraScale and UltraScale+ FPGA Packaging Specifications. In step 2 select the product category: FPGAs and 3D ICs. In step 3, select the product type. In step 4, click on the package specifications selection to find the available MDDS files.*

In Table 4-1, the full Defense-grade XQ ruggedized packages are delineated by an R in the third digit of the package code.

Table 4-1: **Cross-Reference to Mechanical Drawings by Package**

Package	Figure	Device				Package Status
FCVA289	Figure 4-1	XCAU7P	XAAU7P			Production
CMVA361	Figure 4-2	XCSU10P	XCSU25P	XCSU35P		Production
UBVA368	Figure 4-3	XCAU10P	XCAU15P			Production
SBVB484	Figure 4-4	XCAU10P XAAU10P	XCAU15P XAAU10P			Production
SBVC484	Figure 4-5	XCAU7P	XAAU7P			Production
CMVA529	Figure 4-6	XCSU10P	XCSU25P	XCSU35P		Production
SBVB625	Figure 4-7	XCSU10P	XCSU25P	XCSU35P		Production

Table 4-1: **Cross-Reference to Mechanical Drawings by Package *(Cont'd)***

Package	Figure	Device						Package Status
FBVA676	Figure 4-8 Figure 4-9	XCKU035	XCKU040					Production
FFVA676 FFQA676	Figure 4-10	XCKU3P	XCKU5P					Production
FFVB676 FFQB676	Figure 4-10	XCAU10P XAAU10P	XCAU15P XAAU10P	XCAU20P	XCAU25P	XCKU3P	XCKU5P	Production
FFRB676	Figure 4-11	XQKU5P						Production
RBA676	Figure 4-12	XQKU040						Production
SFVA784	Figure 4-13	XCKU035	XCKU040					Production
SFVB784 SFQB784	Figure 4-14	XCAU20P	XCAU25P	XCKU3P	XCKU5P			Production
SFRB784	Figure 4-15	XQKU5P						Production
FBVA900	Figure 4-16 Figure 4-17	XCKU035	XCKU040					Production
FFVD900 FFQD900	Figure 4-18	XCKU3P	XCKU5P	XCKU11P				Production
FFVE900 FFQE900	Figure 4-18	XCKU9P	XCKU13P					Production
FFVA1156 FFQA1156[1]	Figure 4-19	XCKU025	XCKU035	XCKU040				Production
	Figure 4-20	XCKU060	XCKU095	XCKU11P				Production
	Figure 4-21	XCKU15P						Production
FFRA1156	Figure 4-22	XQKU15P						Production
RFA1156	Figure 4-23	XQKU040						Production
	Figure 4-24	XQKU060	XQKU095					Production
VSVA1365	Figure 4-25	XCVU23P						Production
FFVA1517	Figure 4-26	XCKU060						Production
FLVA1517	Figure 4-29	XCKU085	XCKU115					Production
FFVC1517 FFQC1517[1]	Figure 4-26	XCKU095	XCVU065	XCVU080	XCVU095			Production
	Figure 4-27	XCVU3P						Production
FFRC1517	Figure 4-28	XQVU3P						Production
FFVD1517	Figure 4-26	XCVU080	XCVU095					Production
FLVD1517	Figure 4-29	XCKU115	XCVU125					Production
FFVE1517 FFQE1517	Figure 4-27	XCKU11P	XCKU15P					Production
FFRE1517	Figure 4-28	XQKU15P						Production
RLD1517	Figure 4-30	XQKU115						Production

Table 4-1: **Cross-Reference to Mechanical Drawings by Package *(Cont'd)***

Package	Figure	Device			Package Status
FFVA1760 FFQA1760	Figure 4-31	XCKU15P			Production
FFVB1760	Figure 4-32	XCKU095	XCVU080	XCVU095	Production
FLVB1760	Figure 4-33	XCKU085	XCKU115	XCVU125	Production
FFVE1760 FFQE1760	Figure 4-34	XCKU15P			Production
FFVJ1760	Figure 4-35	XCKU19P			Production
FSVJ1760	Figure 4-36	XCVU23P			Production
FLVD1924	Figure 4-37	XCKU115			Production
FLVF1924	Figure 4-37	XCKU085	XCKU115		Production
FLGF1924 FLQF1924	Figure 4-38	XCVU11P			Production
RLF1924	Figure 4-39	XQKU115			Production
FSVH1924 FSQH1924	Figure 4-40	XCVU31P			Production
FFVA2104	Figure 4-41	XCVU080	XCVU095		Production
FHGA2104 FHQA2104	Figure 4-43	XCVU13P			Production
FLVA2104 FLQA2104[1]	Figure 4-45	XCKU115	XCVU125		Production
	Figure 4-46	XCVU5P	XCVU7P		Production
FLRA2104	Figure 4-47	XQVU7P			Production
FLGA2104 FLQA2104	Figure 4-48	XCVU9P			Production
FFVB2104	Figure 4-41	XCKU095	XCVU080	XCVU095	Production
FFVB2104	Figure 4-42	XCKU19P			Production
FHGB2104 FHQB2104	Figure 4-44	XCVU13P			Production
FLVB2104 FLQB2104[1]	Figure 4-45	XCKU115	XCVU125		Production
	Figure 4-46	XCVU5P	XCVU7P		Production
FLRB2104	Figure 4-47	XQVU7P			Production
FLGB2104 FLQB2104[1]	Figure 4-49	XCVU160	XCVU190		Production
	Figure 4-50	XCVU9P	XCVU11P		Production
FFVC2104	Figure 4-52	XCVU095			Production
FHGC2104 FHQC2104	Figure 4-44	XCVU13P			Production

Table 4-1: **Cross-Reference to Mechanical Drawings by Package *(Cont'd)***

Package	Figure	Device			Package Status
FLGC2104 FLQC2104[(1)]	Figure 4-49	XCVU160	XCVU190		Production
	Figure 4-53	XCVU9P			Production
	Figure 4-50	XCVU11P			Production
FLRC2104	Figure 4-51	XQVU11P			Production
FLVC2104 FLQC2104[(1)]	Figure 4-54	XCVU125			Production
	Figure 4-55	XCVU5P	XCVU7P		Production
FIGD2104 FIQD2104[(1)]	Figure 4-56	XCVU13P			Production
	Figure 4-56	XCVU27P	XCVU29P		Production
FSGD2104 FSQD2104	Figure 4-57	XCVU9P			Production
	Figure 4-58	XCVU11P			Production
FSVH2104 FSQH2104	Figure 4-59	XCVU33P			Production
	Figure 4-60	XCVU35P	XCVU45P		Production
FLGB2377	Figure 4-61	XCVU440			Production
FLGA2577 FLQA2577[(1)]	Figure 4-62	XCVU190			Production
	Figure 4-63	XCVU9P	XCVU13P		Production
	Figure 4-64	XCVU11P			Production
FSGA2577 FSQA2577	Figure 4-65	XCVU13P			Production
	Figure 4-65	XCVU27P	XCVU29P		Production
FLGA2892	Figure 4-66	XCVU440			Production
FSVH2892 FSQH2892	Figure 4-67	XCVU35P	XCVU45P		Production
	Figure 4-68	XCVU37P			Production
FSVK2892	Figure 4-69	XCVU57P			Production
FSVA3824	Figure 4-70	XCVU19P			Production
FSVB3824	Figure 4-70	XCVU19P			Production

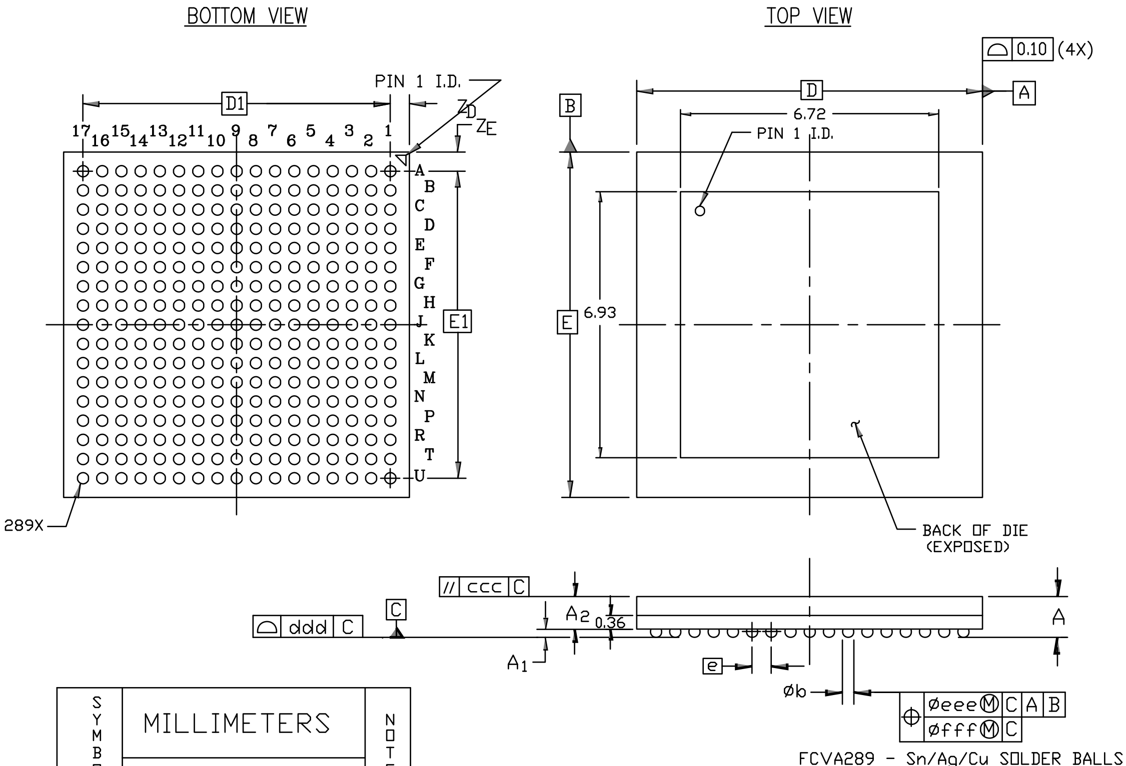
Notes:

1. The XQ devices with non-ruggedized eutectic Sn/Pb ball packages are only available in Kintex and Virtex UltraScale+ devices.

Table 4-2: **Mechanical Drawing Dimension Definitions**

Dimension	Definition
⌓	Bilateral tolerance of package sides with respect to datums A and B
▱	Flatness tolerance of silicon die or package lid top surface
/ /	Bilateral tolerance for parallelism of silicon die or package lid top surface with respect to the seating plane datum C
A	Thickness of package with respect to the seating plane datum C
A_1	Thickness of BGA balls with respect to the seating plane datum C
A_2	Thickness of package body, including stiffener ring or lid and excluding BGA balls, with respect to the seating plane datum C
A_3	Distance from top of silicon die to top of stiffener ring or lid with respect to the seating plane datum C
D/E	Length/width of package with respect to datums A and B
D_1/E_1	Length/width of BGA matrix with respect to datums A and B
e	BGA ball pitch measured at the center of each ball
øb	BGA ball diameter
⌓aaa	Unidirectional upward tolerance with respect to the seating plane datum C
/ / bbb	Bilateral tolerance for parallelism of package surface with respect to the seating plane datum C
øddd	BGA ball position tolerance of diameter ddd with respect to datums A and B perpendicular to the seating plane datum C in which the center of each ball must lie
øeee	BGA ball position tolerance of diameter eee measured with respect to other balls within the BGA matrix in which the center of each ball must lie
M	BGA ball matrix size

FCVA289 Flip-Chip, Chip Scale, BGA (XCAU7P and XAAU7P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	0.96	1.06	1.16	
A_1	0.16	0.21	0.26	
A_2	0.75	0.85	0.95	
D/E	8.90	9.00	9.10	
D_1/E_1	8.00 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc	~	~	0.10	
ddd	~	~	0.08	
eee	~	~	0.15	
fff	~	~	0.05	
Z_D/Z_E	0.35	0.50	0.65	
M	17			2

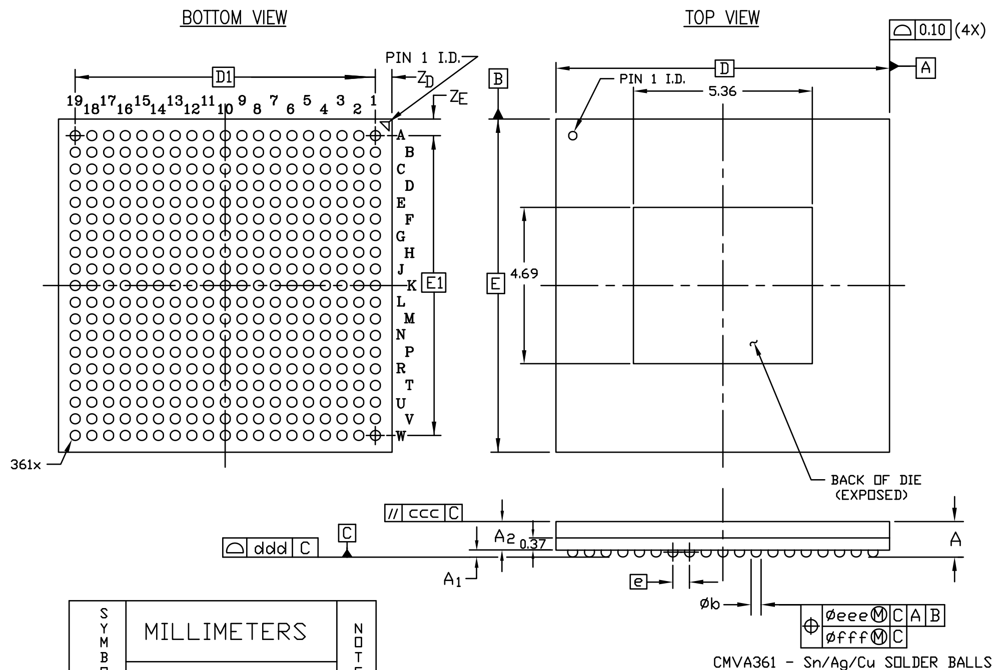
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE

X28943-010224

Figure 4-1: **Package Dimensions for FCVA289 (XCAU7P and XAAU7P)**

CMVA361 Flip-Chip, Chip Scale, BGA (XCSU10P, XCSU25P, XCSU35P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	0.97	1.07	1.17	
A_1	0.16	0.21	0.26	
A_2	0.76	0.86	0.96	
D/E	9.90	10.00	10.10	
D_1/E_1	9.00 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc	~	~	0.10	
ddd	~	~	0.08	
eee	~	~	0.15	
fff	~	~	0.05	
Z_D/Z_E	0.35	0.50	0.65	
M	19			2

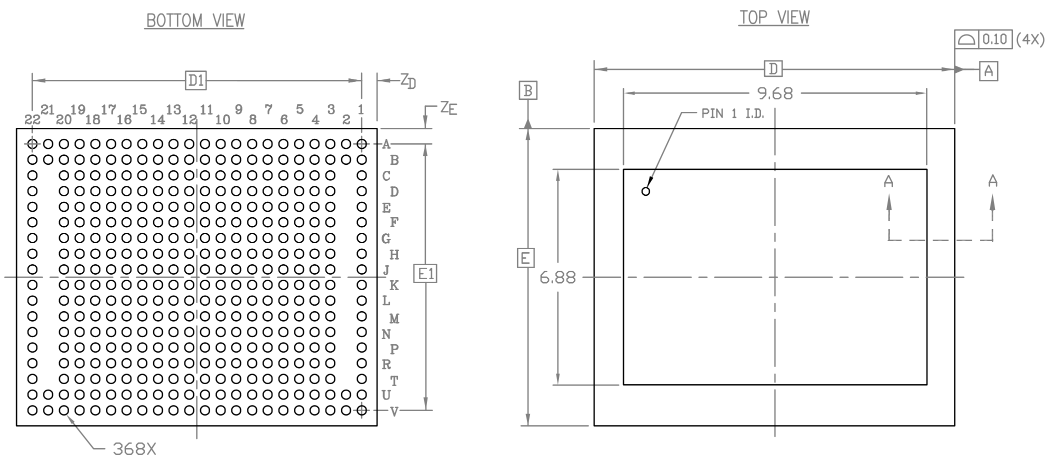
NOTES:

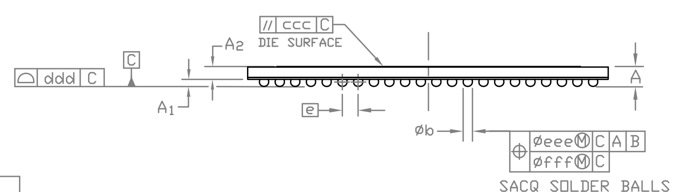
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE

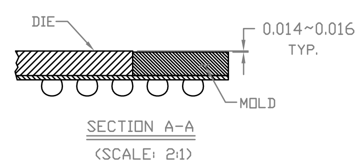
X30290-010825

Figure 4-2: **Package Dimensions for CMVA361 (XCSU10P, XCSU25P, XCSU35P)**

UBVA368 Bare-Die, Flip-Chip, Integrated Fan Out (InFO), BGA (XCAU10P and XCAU15P)







SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	0.596	0.644	0.692	
A_1	0.190	0.235	0.280	
A_2	0.392	0.409	0.426	
D	11.40	11.50	11.60	
E	9.40	9.50	9.60	
D_1	10.50 BSC			
E_1	8.50 BSC			
e	0.50 BSC			
Øb	0.27	0.32	0.37	
ccc	~	~	0.10	
ddd	~	~	0.08	
eee	~	~	0.15	
fff	~	~	0.05	
Z_D/Z_E	0.35	0.50	0.65	
M	22X18			2

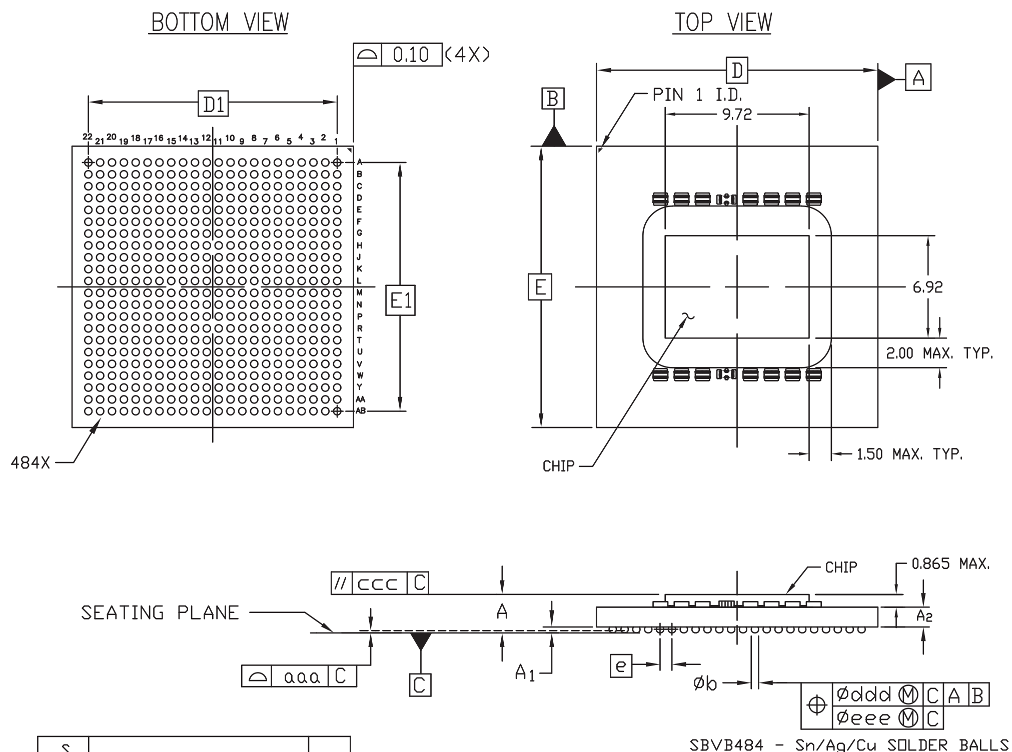
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE

X30289-010825

Figure 4-3: **Package Dimensions for UBVA368 (XCAU10P and XCAU15P)**

SBVB484 Bare-Die, Flip-Chip, Super-Fine Pitch, BGA (XCAU10P, XAAU10P, XCAU15P, and XAAU15P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.39	2.59	2.79	
A_1	0.36	0.40	0.44	
A_2	1.19	1.34	1.49	
D/E	19.00 BASIC			
D1/E1	16.80 BASIC			
e	0.80 BASIC			
ϕb	0.45	0.50	0.55	
aaa	-	-	0.12	
ccc	-	-	0.20	
ddd	-	-	0.15	
eee	-	-	0.08	
M	22			2

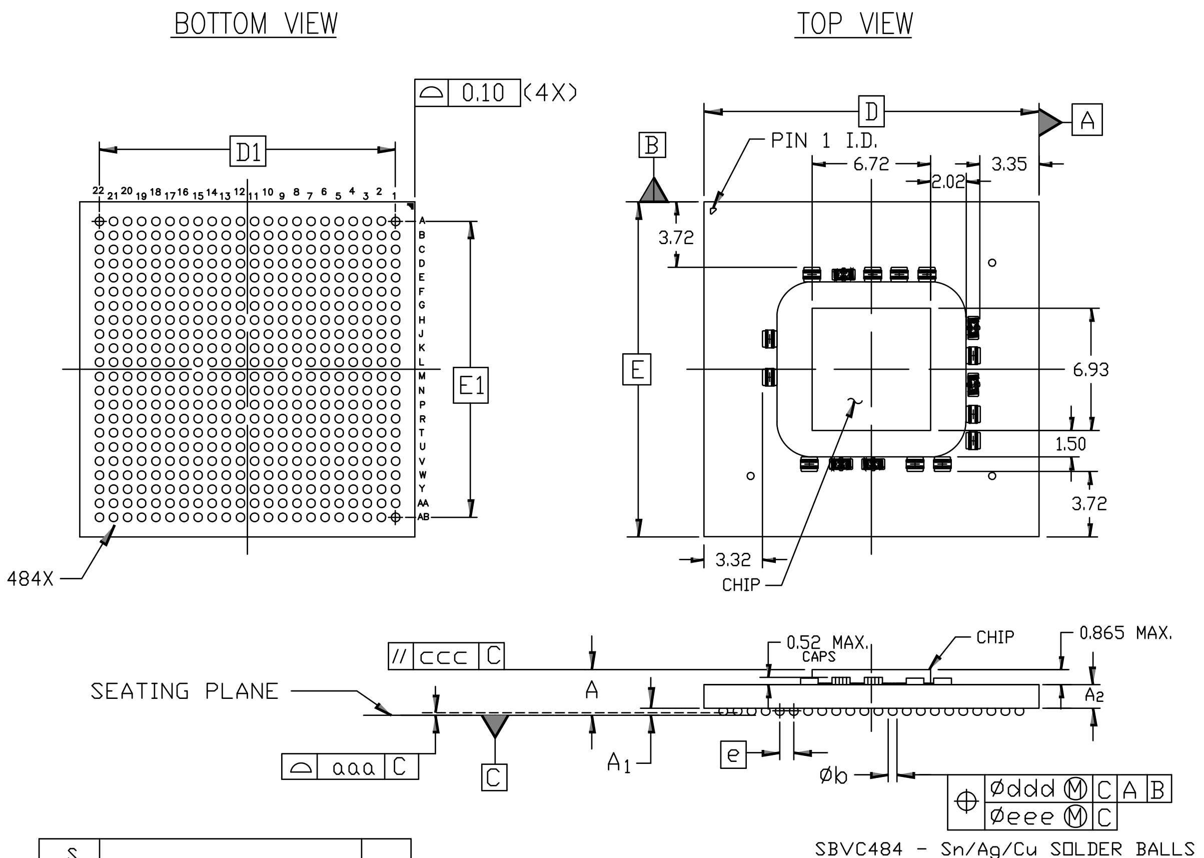
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC M0–216 BAP–2

ug1075_c5_030122

Figure 4-4: **Package Dimensions for SBVB484 (XCAU10P, XAAU10P, XCAU15P, and XAAU15P)**

SBVC484 Bare-Die, Flip-Chip, Super-Fine Pitch, BGA (XCAU7P and XAAU7P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.39	2.59	2.79	
A_1	0.36	0.40	0.44	
A_2	1.19	1.34	1.49	
D/E	19.00 BASIC			
D1/E1	16.80 BASIC			
e	0.80 BASIC			
Øb	0.45	0.50	0.55	
aaa	-	-	0.12	
ccc	-	-	0.20	
ddd	-	-	0.15	
eee	-	-	0.08	
M	22			2

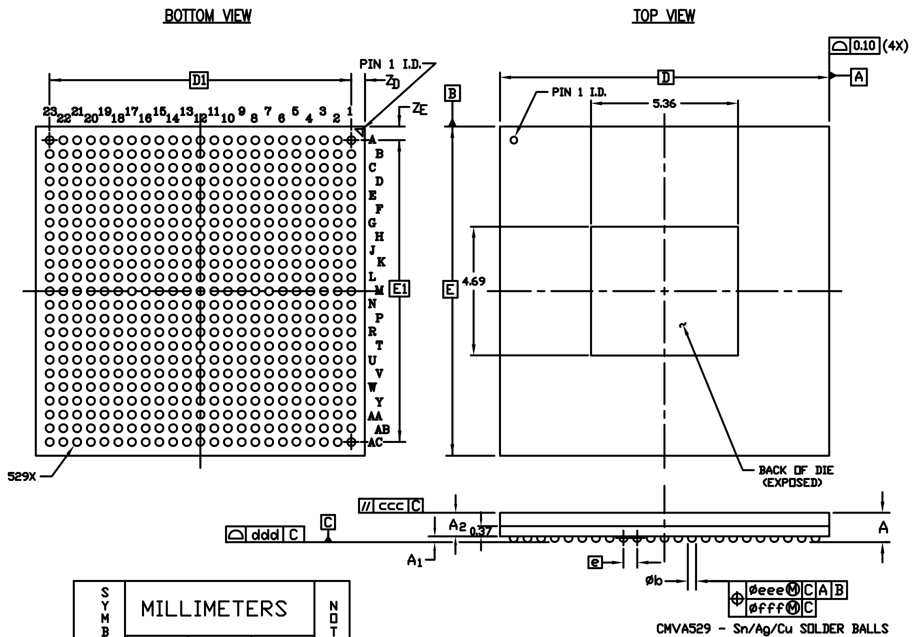
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-216 BAP-2

X27957-041023

Figure 4-5: **Package Dimensions for SBVC484 (XCAU7P and XAAU7P)**

CMVA529 Flip-chip, Chip Scale, BGA (XCSU10P, XCSU25P, XCSU35P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	0.97	1.07	1.17	
A_1	0.16	0.21	0.26	
A_2	0.76	0.86	0.96	
D/E	11.90	12.00	12.10	
D_1/E_1	11.00 BSC			
e	0.50 BSC			
øb	0.25	0.30	0.35	
ccc	—	—	0.10	
ddd	—	—	0.08	
eee	—	—	0.15	
fff	—	—	0.05	
Z_D/Z_E	0.35	0.50	0.65	
M	23			2

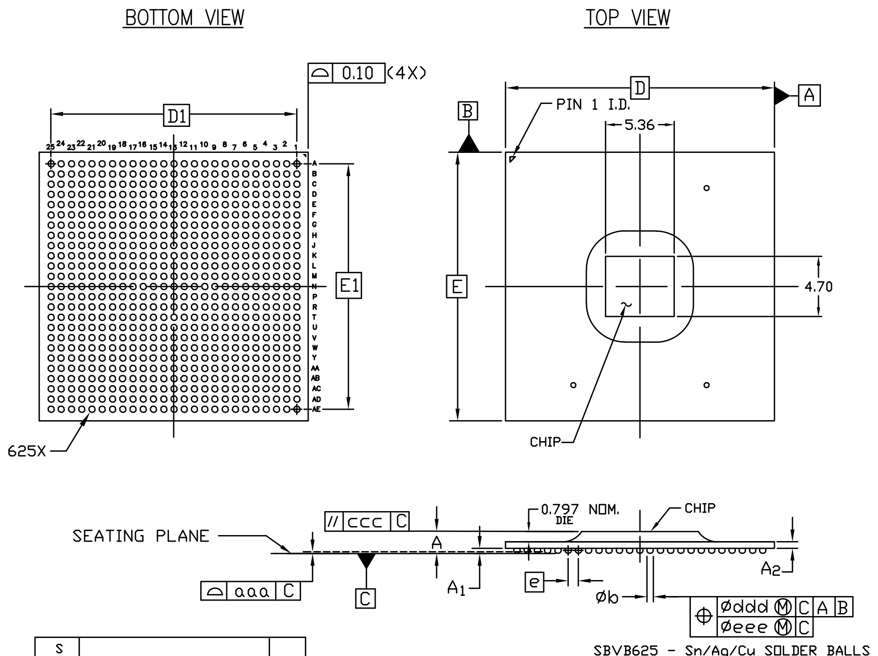
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE

X30291-010825

Figure 4-6: **Package Dimensions for CMVA529 (XCSU10P, XCSU25P, XCSU35P)**

SBVB625 Bare-Die, Flip-Chip, Super-Fine-Pitch, BGA (XCSU10P, XCSU25P, XCSU35P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	1.52	1.72	1.92	
A_1	0.36	0.40	0.44	
A_2	0.372	0.522	0.672	
D/E	21.00 BASIC			
D_1/E_1	19.20 BASIC			
e	0.80 BASIC			
Øb	0.45	0.50	0.55	
aaa	~	~	0.12	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	25			2

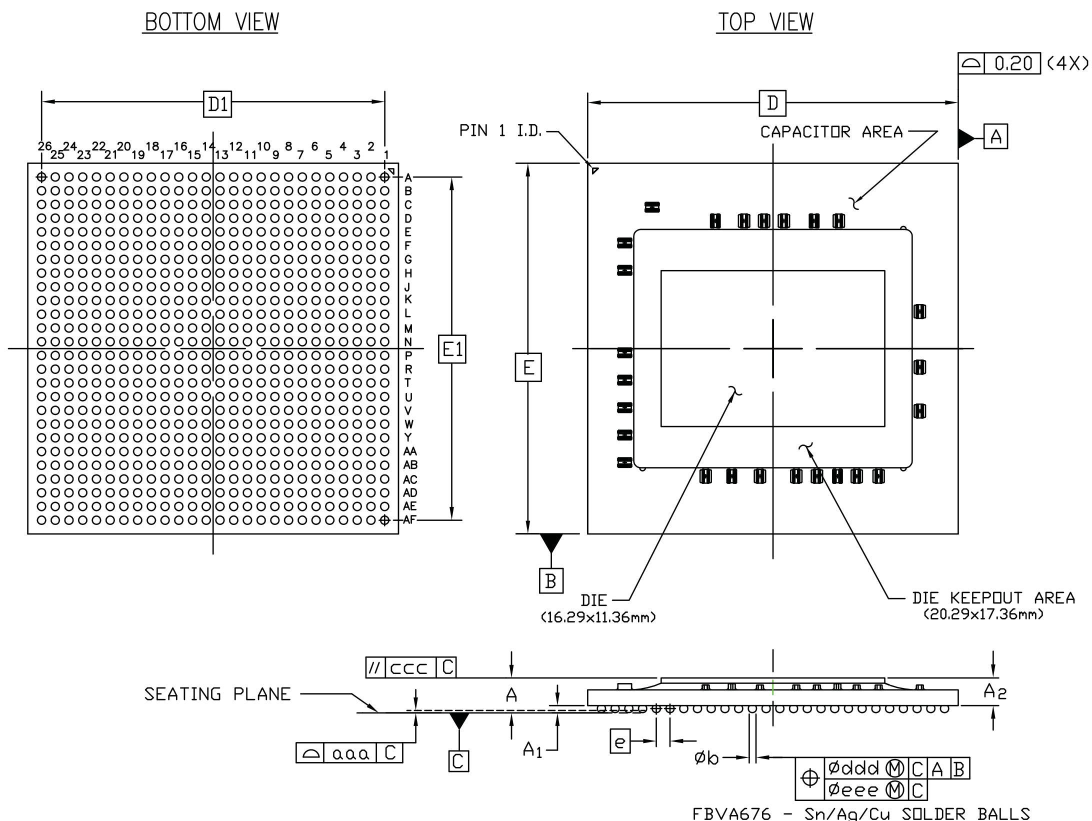
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE

X30292-010825

Figure 4-7: **Package Dimensions for SBVB625 (XCSU10P, XCSU25P, XCSU35P)**

FBVA676 Bare-die Flip-Chip, Fine-Pitch, BGA (XCKU035 and XCKU040)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	2.31	2.51	2.71	
A_1	0.40	0.50	0.60	
A_2	1.81	2.01	2.21	
D/E	27.00 BASIC			
D_1/E_1	25.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M−1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS−034
4. SEE NEXT PAGE FOR CHIP CAPACITOR LOCATION DIMENSIONS

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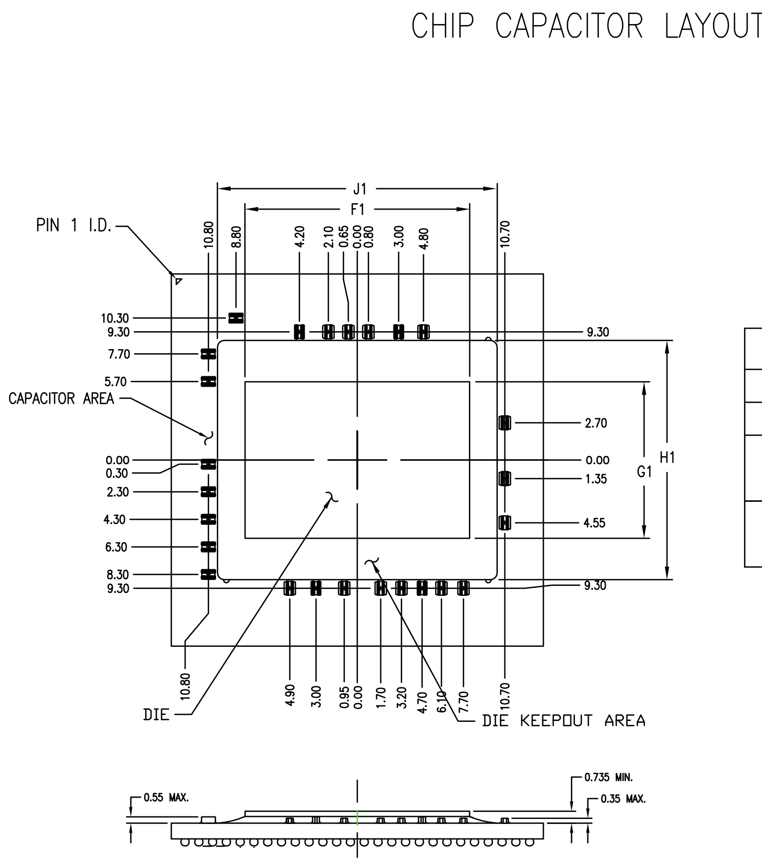
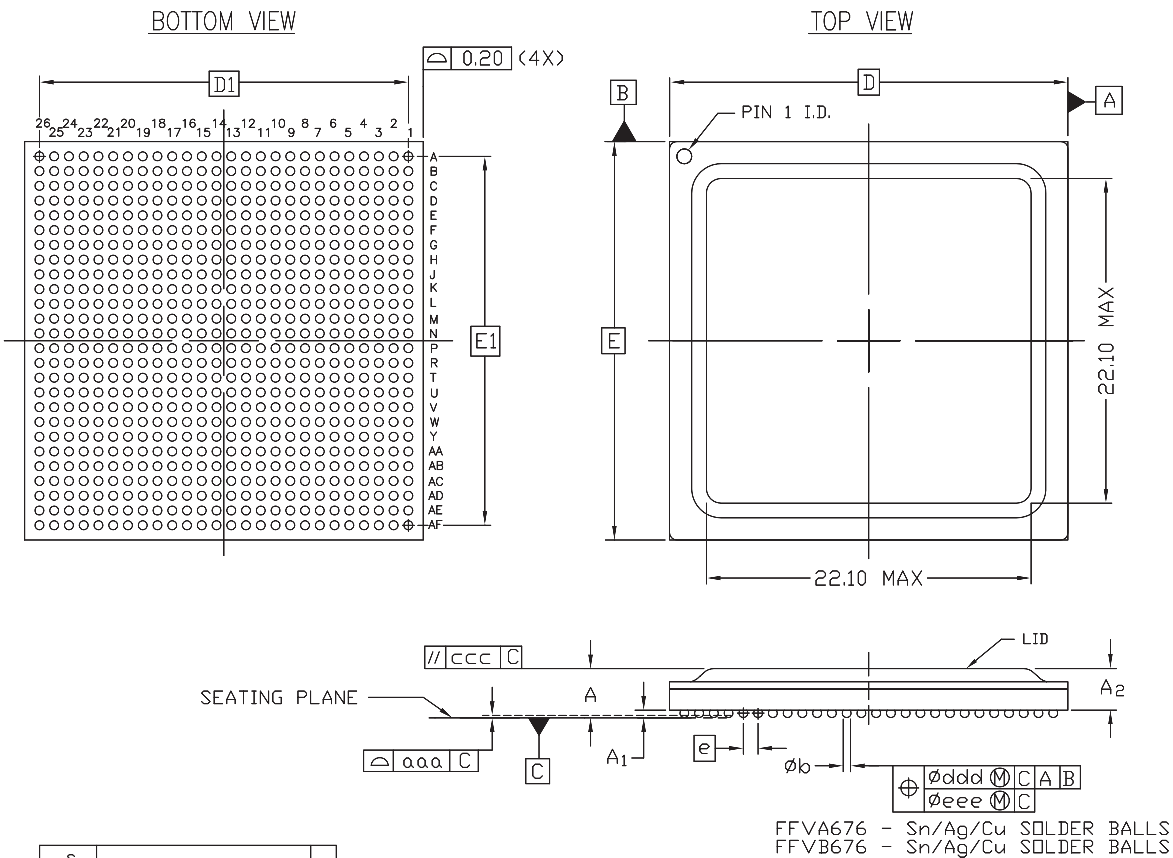
Figure 4-8: **Package Dimensions for FBVA676 (XCKU035 and XCKU040)**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FBVA676	
DEVICE TYPE	KU040	
DIE SIZE (mm)	F1	16.29
	G1	11.36
DIE KEEPOUT AREA (mm)	J1	20.29
	H1	17.36

Figure 4-9: **FBVA676 Package (XCKU035 and XCKU040) Die Dimensions with Capacitor Locations**

FFVA676 and FFVB676 Flip-Chip, Fine-Pitch, BGA (XCAU10P, XAAU10P, XCAU15P, XAAU15P, XCAU20P, XCAU25P, XCKU3P, and XCKU5P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.12	3.31	3.52	
A_1	0.40	0.50	0.60	
A_2	2.61	2.81	3.01	
D/E	27.00 BASIC			
D_1/E_1	25.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	26			2

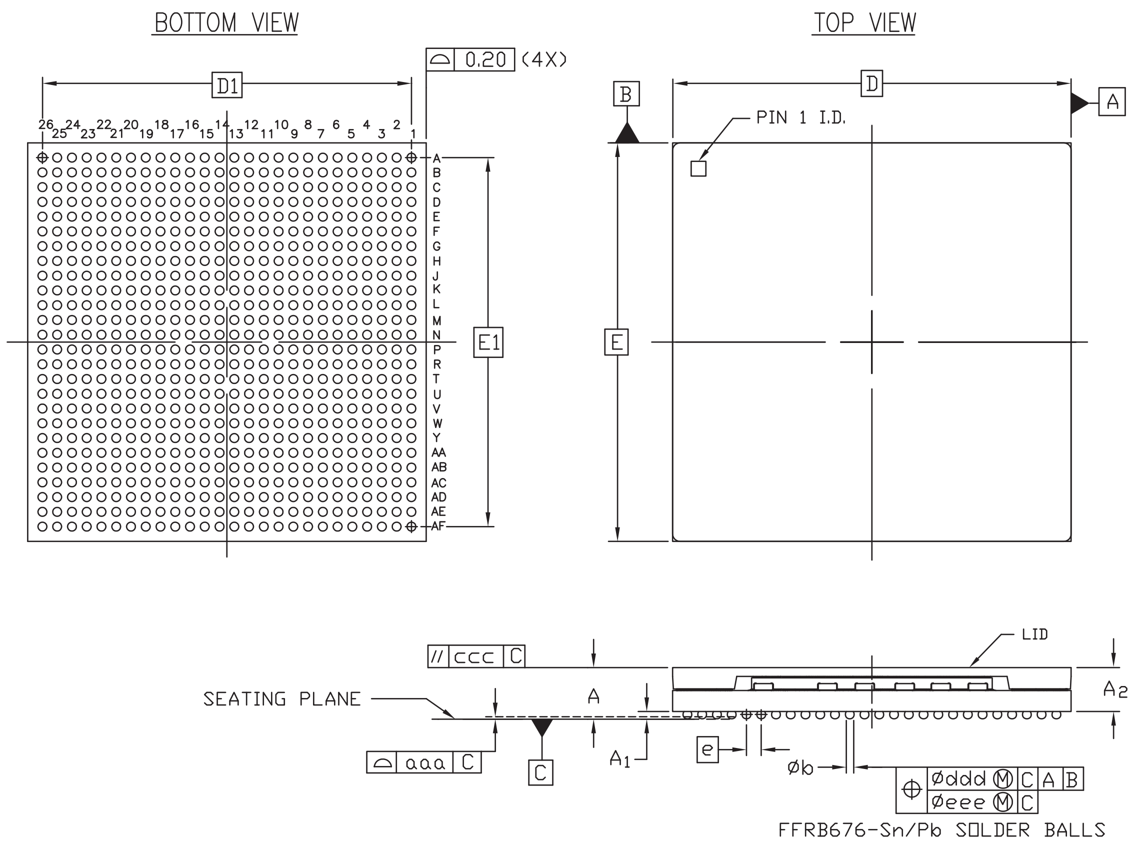
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ug575_c4_ffva676_ffvb676_ku3p_ku5p_041917

Figure 4-10: **Package Dimensions for FFVA676 (XCKU3P and XCKU5P) and FFVB676 (XCAU10P, XAAU10P, XCAU15P, XAAU15P, XCAU20P, and XCAU25P)**

FFRB676 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQKU5P)



SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	3.27	3.47	3.67	
A_1	0.40	0.50	0.60	
A_2	2.77	2.97	3.17	
D/E	27.00 BASIC			
D1/E1	25.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

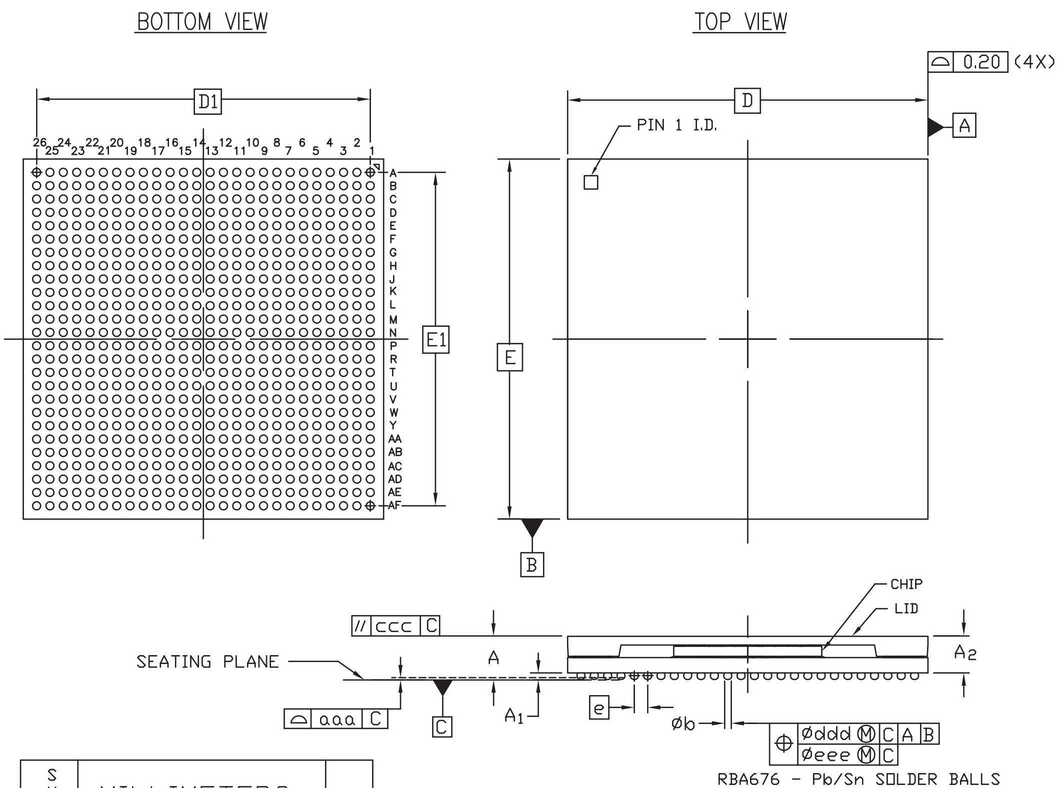
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAL–1

ug575_c4_ffrb676_010819

Figure 4-11: **Package Dimensions for FFRB676 (XQKU5P)**

RBA676 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQKU040)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.04	3.24	3.44	
A_1	0.40	0.50	0.60	
A_2	2.54	2.74	2.94	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	26			2

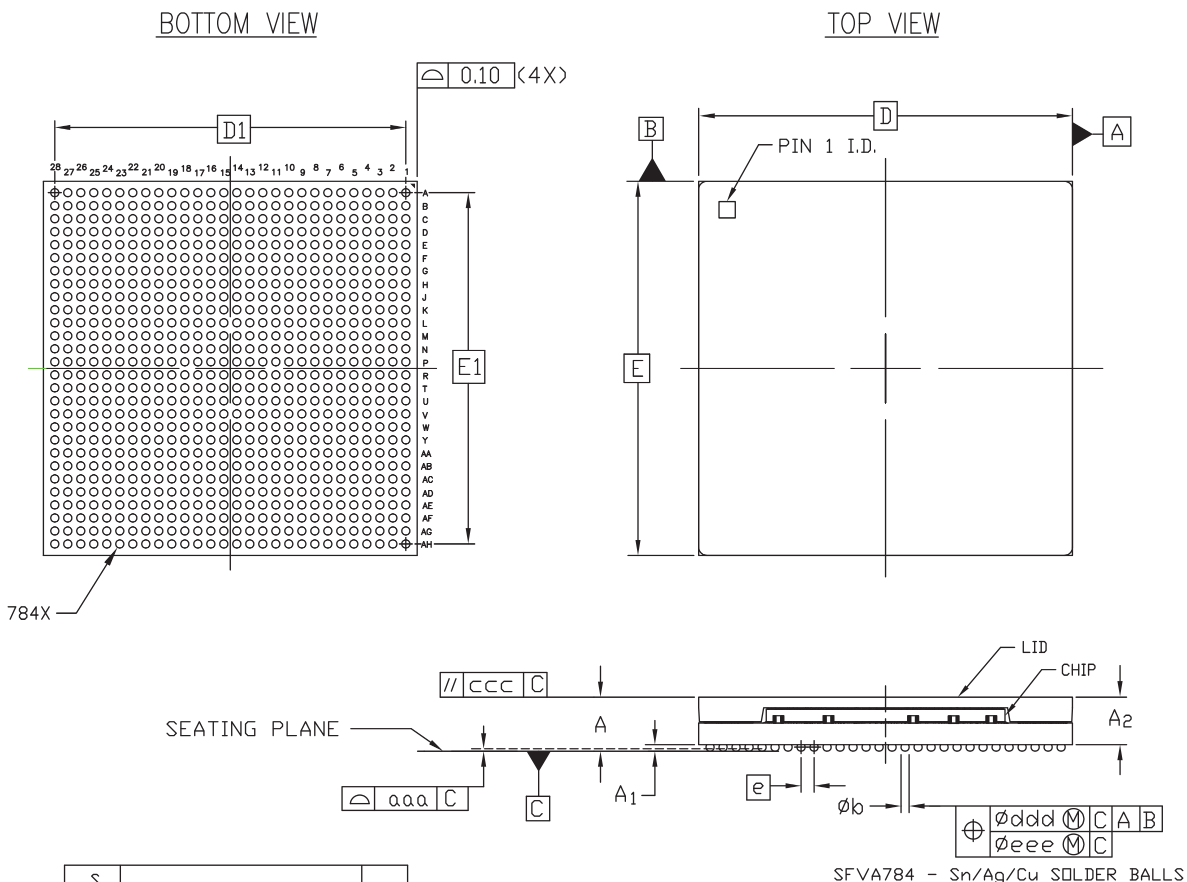
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAL–1

ug575_c4_r1_032417

Figure 4-12: **Package Dimensions for RBA676 (XQKU040)**

SFVA784 Flip-Chip, Super-Fine Pitch, BGA (XCKU035 and XCKU040)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.12	3.32	3.52	
A_1	0.36	0.40	0.44	
A_2	2.72	2.92	3.12	
D/E	23.00 BASIC			
D_1/E_1	21.60 BASIC			
e	0.80 BASIC			
Øb	0.45	0.50	0.55	
aaa	–	–	0.12	
ccc	–	–	0.20	
ddd	–	–	0.15	
eee	–	–	0.08	
M	28			2

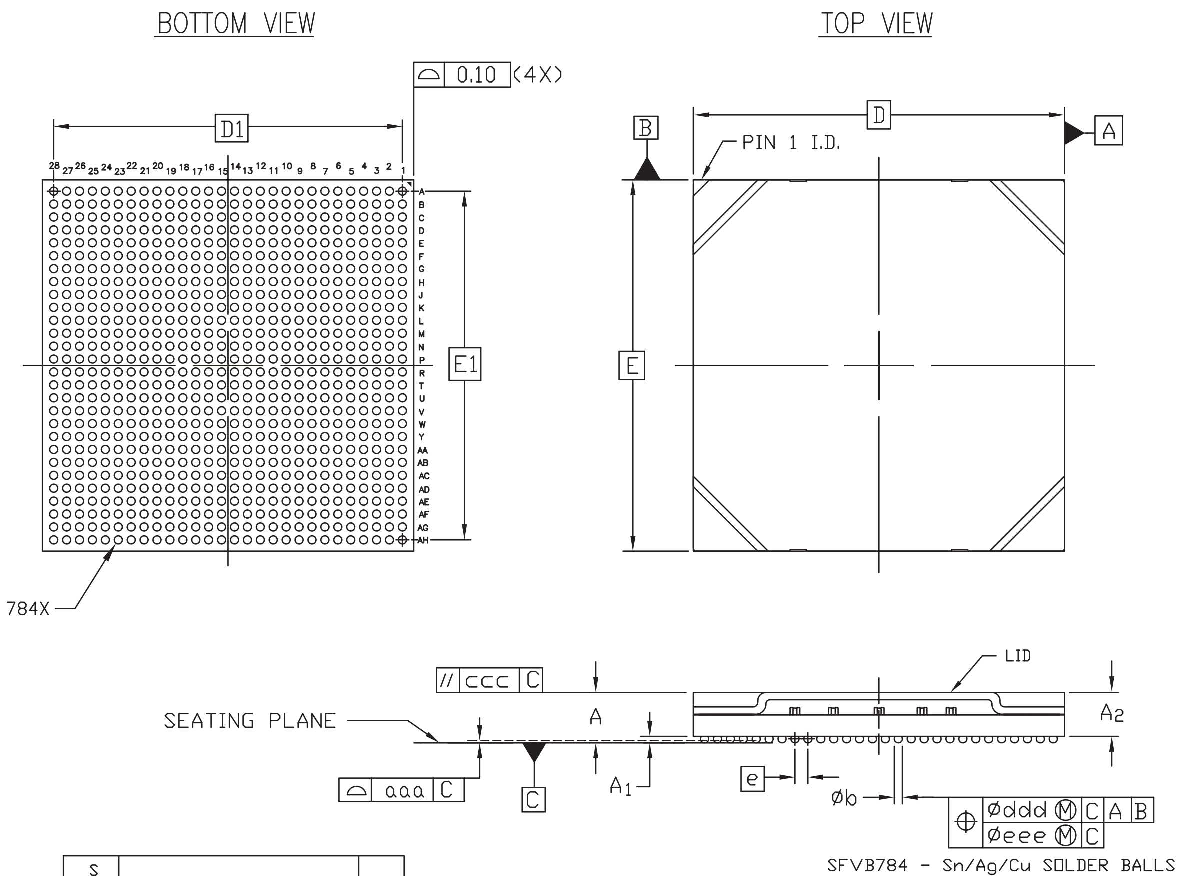
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–216 BAU–1

ug575_c4_23_070615

Figure 4-13: **Package Dimensions for SFVA784 (XCKU035 and XCKU040)**

SFVB784 Flip-Chip, Super-Fine Pitch, BGA (XCAU20P, XCAU25P, XCKU3P, and XCKU5P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	2.92	3.12	3.32	
A_1	0.36	0.40	0.44	
A_2	2.52	2.72	2.92	
D/E	23.00 BASIC			
D_1/E_1	21.60 BASIC			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa	~	~	0.20	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	28			2

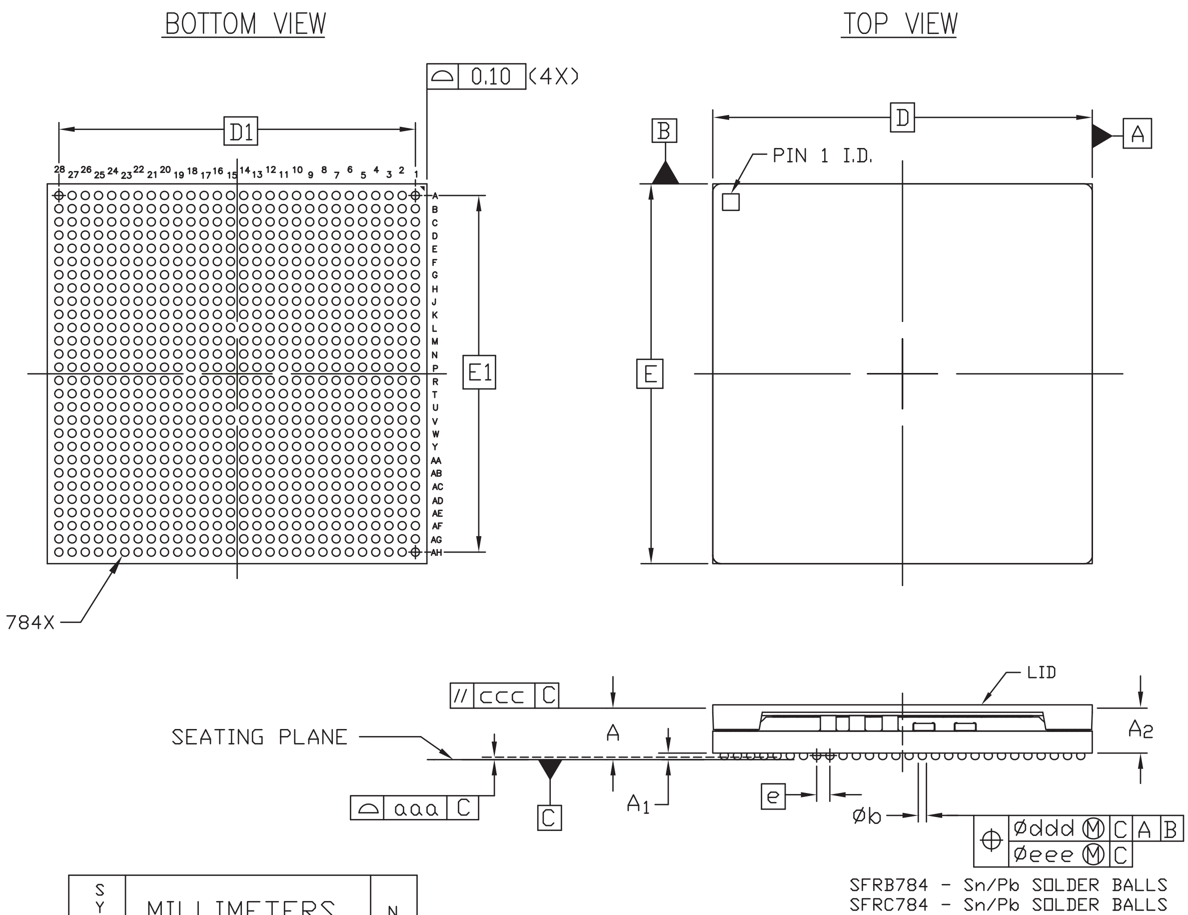
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO-216 BAU-1

ug575_c4_sfvb784_ku3p_ku5p_041917

Figure 4-14: **Package Dimensions for SFVB784 (XCAU20P, XCAU25P, XCKU3P, and XCKU5P)**

SFRB784 Ruggedized Flip-Chip, Super-Fine-Pitch, BGA (XQKU5P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.12	3.32	3.52	
A_1	0.36	0.40	0.44	
A_2	2.72	2.92	3.12	
D/E	23.00 BASIC			
D_1/E_1	21.60 BASIC			
e	0.80 BASIC			
øb	0.45	0.50	0.55	
aaa	~	~	0.20	
ccc	~	~	0.20	
ddd	~	~	0.15	
eee	~	~	0.08	
M	28			2

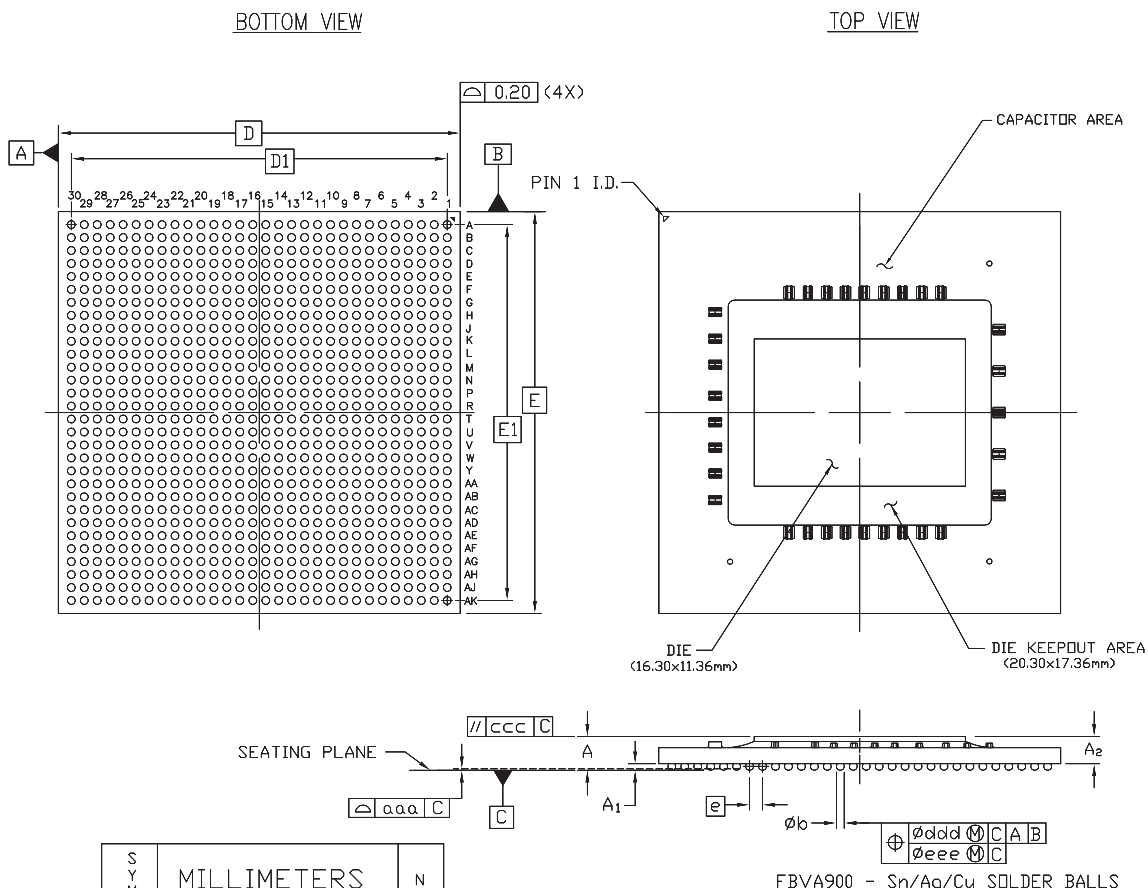
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MO–216 BAU–1

ug575_c4_sfrb784_010719

Figure 4-15: **Package Dimensions for SFRB784 (XQKU5P)**

FBVA900 Bare-die, Flip-Chip, Fine-Pitch, BGA (XCKU035 and XCKU040)



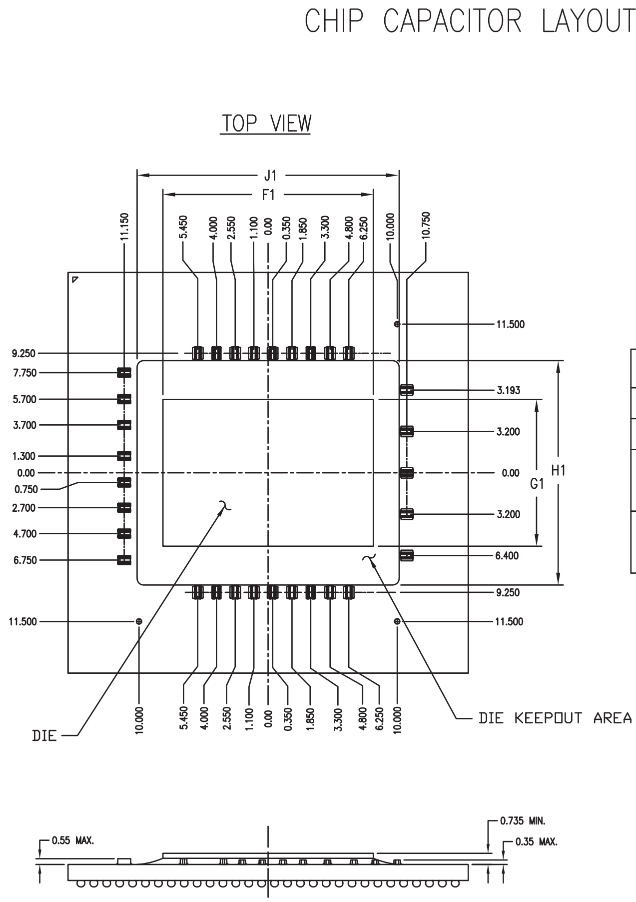
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.40	2.60	2.80	
A_1	0.40	0.50	0.60	
A_2	1.90	2.10	2.30	
D/E	31.00 BASIC			
D_1/E_1	29.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS-034 (DEPOPULATED)
4. SEE NEXT PAGE FOR CHIP CAPACITOR LOCATION DIMENSIONS

ug575_c4_24_041615

Figure 4-16: **Package Dimensions for FBVA900 (XCKU035 and XCKU040)**

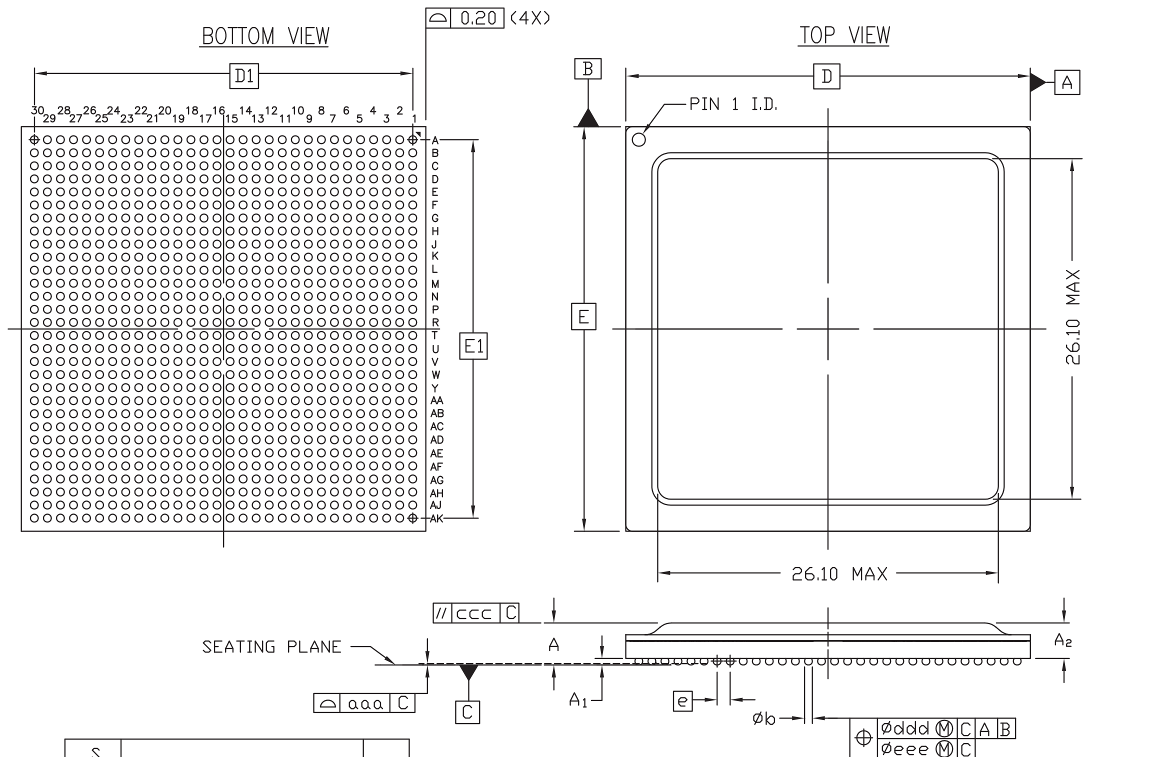


PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FBVA900	
DEVICE TYPE	KU040	
DIE SIZE (mm)	F1	16.30
	G1	11.36
DIE KEEPOUT AREA (mm)	J1	20.30
	H1	17.36

ug575_c4_25_041615

Figure 4-17: **FBVA900 Package (XCKU035 and XCKU040) Die Dimensions with Capacitor Locations**

FFVD900 (XCKU3P, XCKU5P, and XCKU11P) and FFVE900 (XCKU9P and XCKU13P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.02	3.22	3.42	
A_1	0.40	0.50	0.60	
A_2	2.52	2.72	2.92	
D/E	31.00 BASIC			
D_1/E_1	29.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

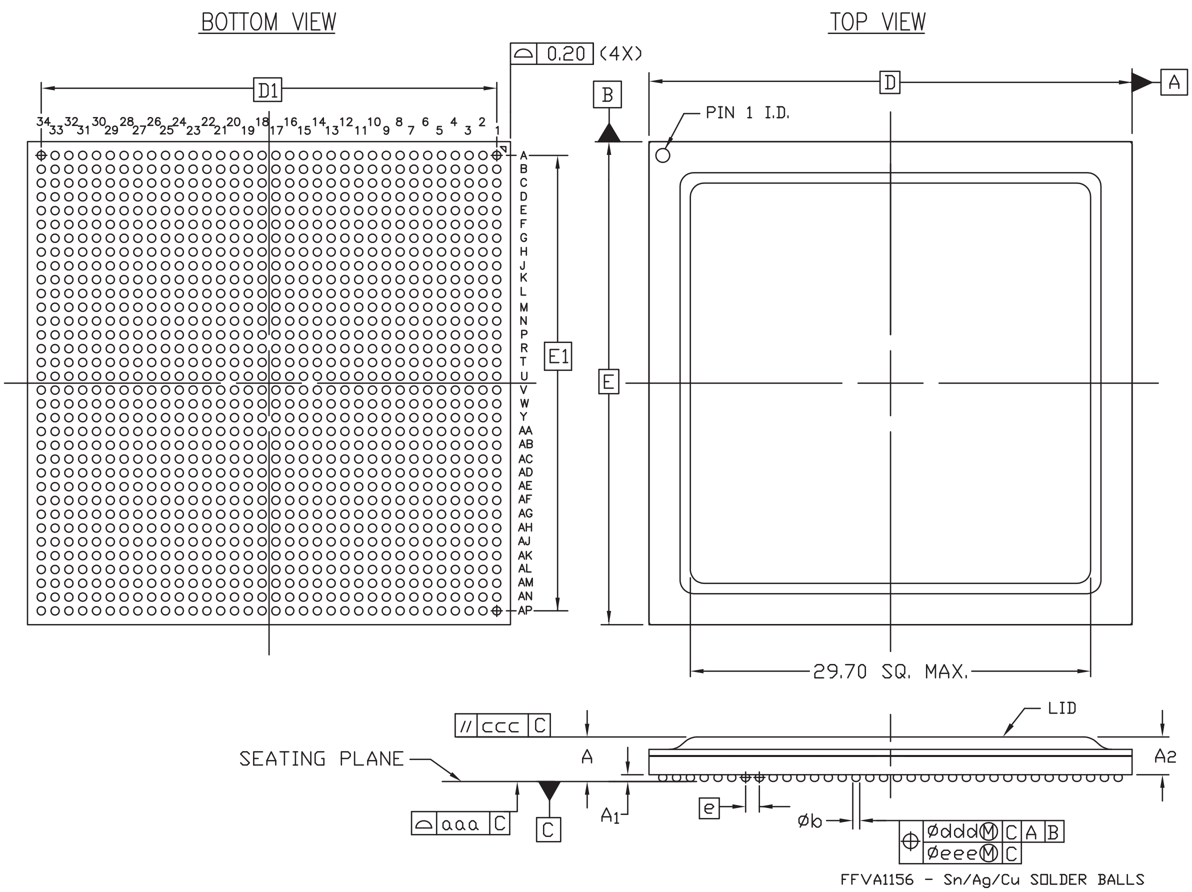
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034 (DEPOPULATED)

ug575_c4_16_072125

Figure 4-18: **Package Dimensions for FFVD900 (XCKU3P, XCKU5P, and XCKU11P) and FFVE900 (XCKU9P and XCKU13P)**

FFVA1156 Flip-Chip, Fine-Pitch, BGA (XCKU025, XCKU035, and XCKU040)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.02	3.22	3.42	
A_1	0.40	0.50	0.60	
A_2	2.52	2.72	2.92	
D/E	35.00 BASIC			
D1/E1	33.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	4
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	34			2

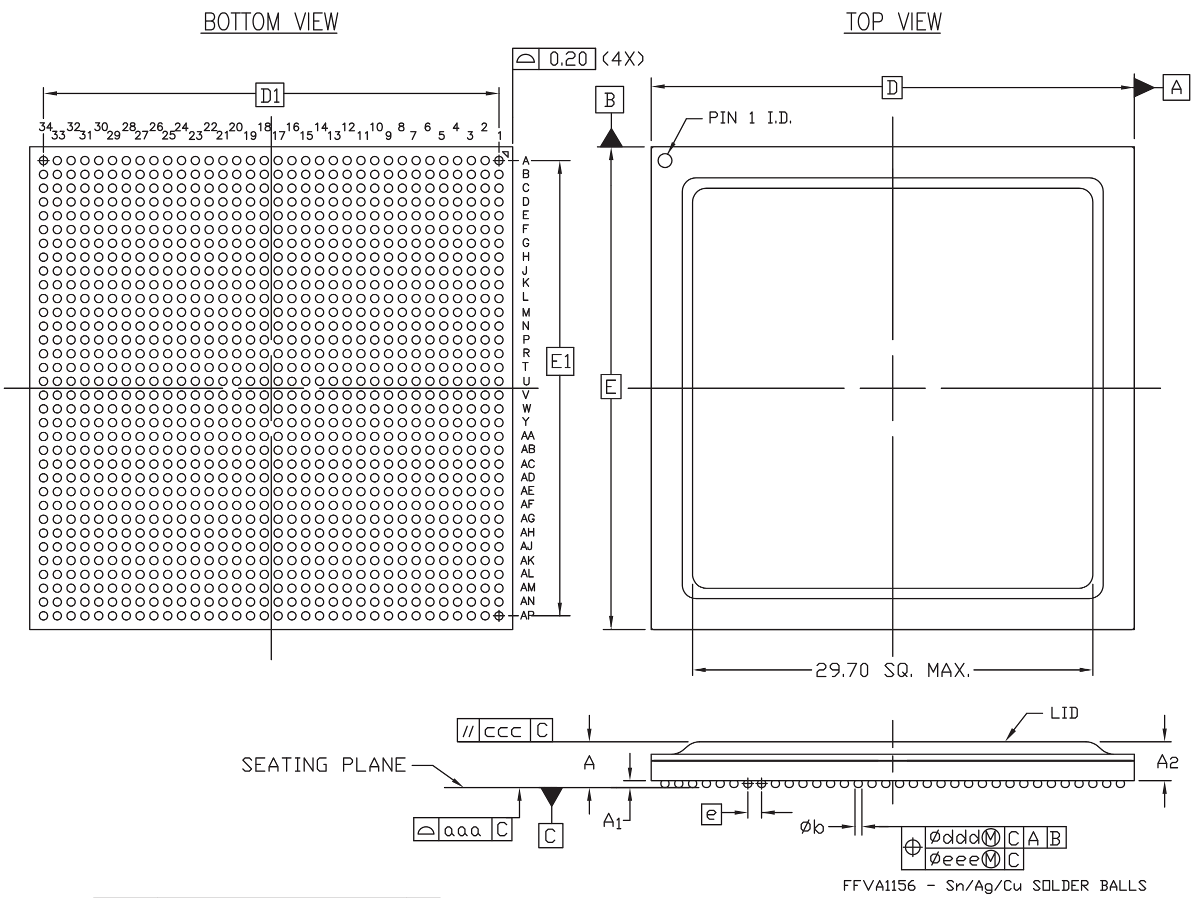
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug575_c4_05_041716

Figure 4-19: **Package Dimensions for FFVA1156 (XCKU025, XCKU035, and XCKU040)**

FFVA1156 Flip-Chip, Fine-Pitch, BGA (XCKU060, XCKU095, and XCKU11P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.11	3.31	3.51	
A_1	0.40	0.50	0.60	
A_2	2.61	2.81	3.01	
D/E	35.00 BASIC			
D1/E1	33.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	-	-	0.20	
ccc	-	-	0.35	
ddd	-	-	0.30	
eee	-	-	0.10	
M	34			2

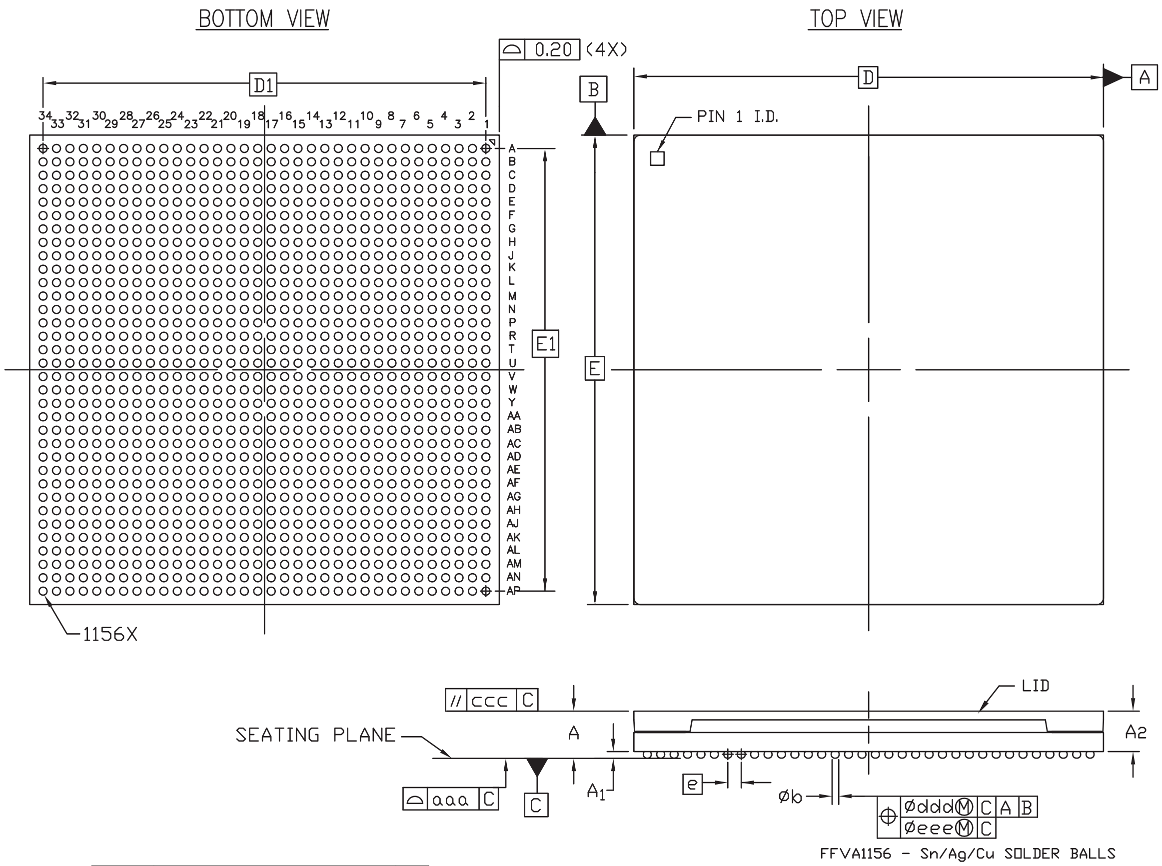
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug575_c4_06_041716

Figure 4-20: **Package Dimensions for FFVA1156 (XCKU060, XCKU095, and XCKU11P)**

FFVA1156 Flip-Chip, Fine-Pitch, BGA (XCKU15P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	35.00 BASIC			
D1/E1	33.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	34			2

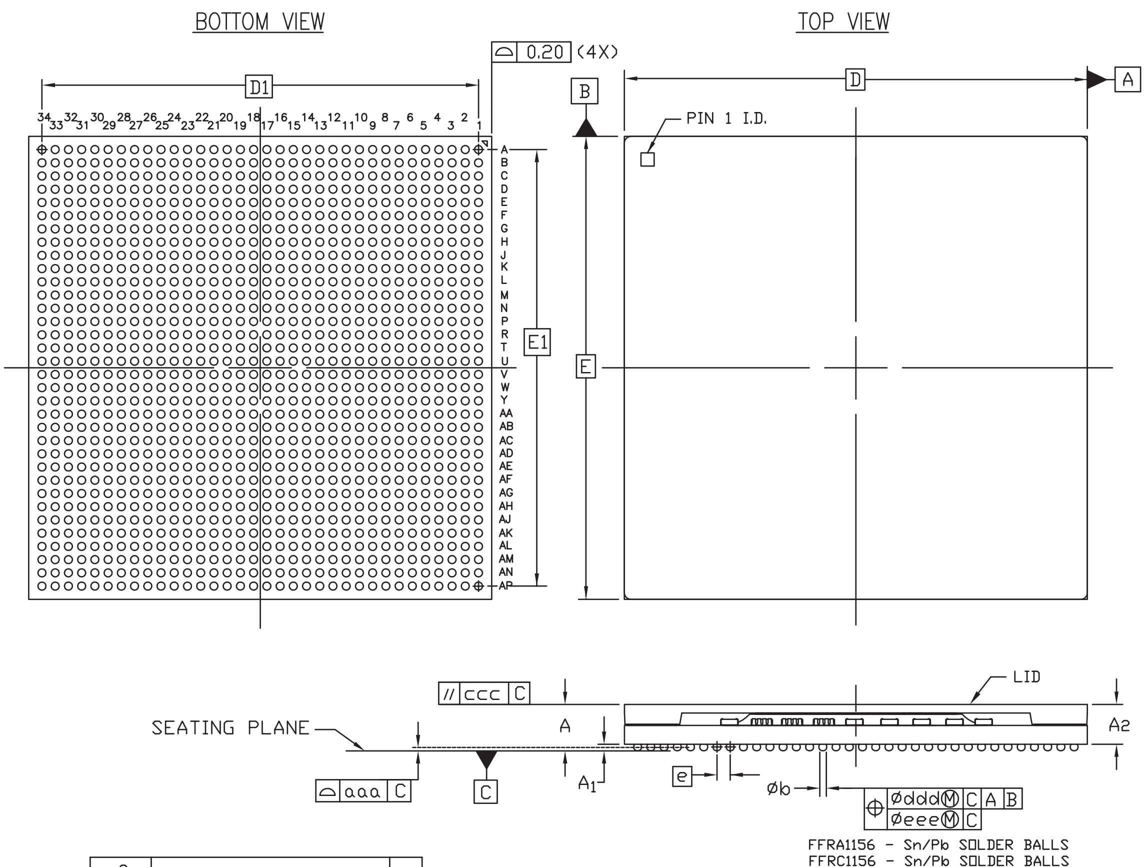
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1

ug575_c4_ffva1156_ku15p_041917

Figure 4-21: **Package Dimensions for FFVA1156 (XCKU15P)**

FFRA1156 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQKU15P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	35.00 BASIC			
D_1/E_1	33.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	34			2

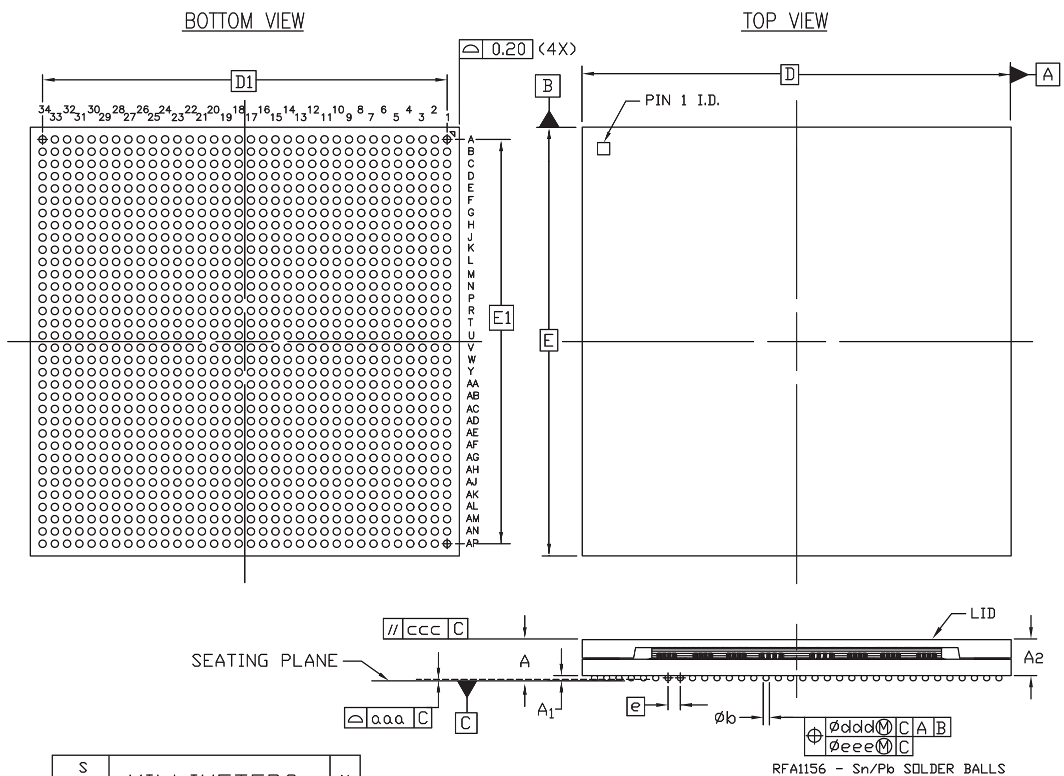
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS-034-AAR-1
4. SEE NEXT PAGE FOR FFRB1156 PACKAGE DIMENSIONS

ug575_c4_ffra1156_010718

Figure 4-22: **Package Dimensions for FFRA1156 (XQKU15P)**

RFA1156 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQKU040)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.22	3.42	3.62	
A_1	0.40	0.50	0.60	
A_2	2.72	2.92	3.12	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	4
aaa	—	—	0.20	
ccc	—	—	0.35	
ddd	—	—	0.30	
eee	—	—	0.10	
M	34			2

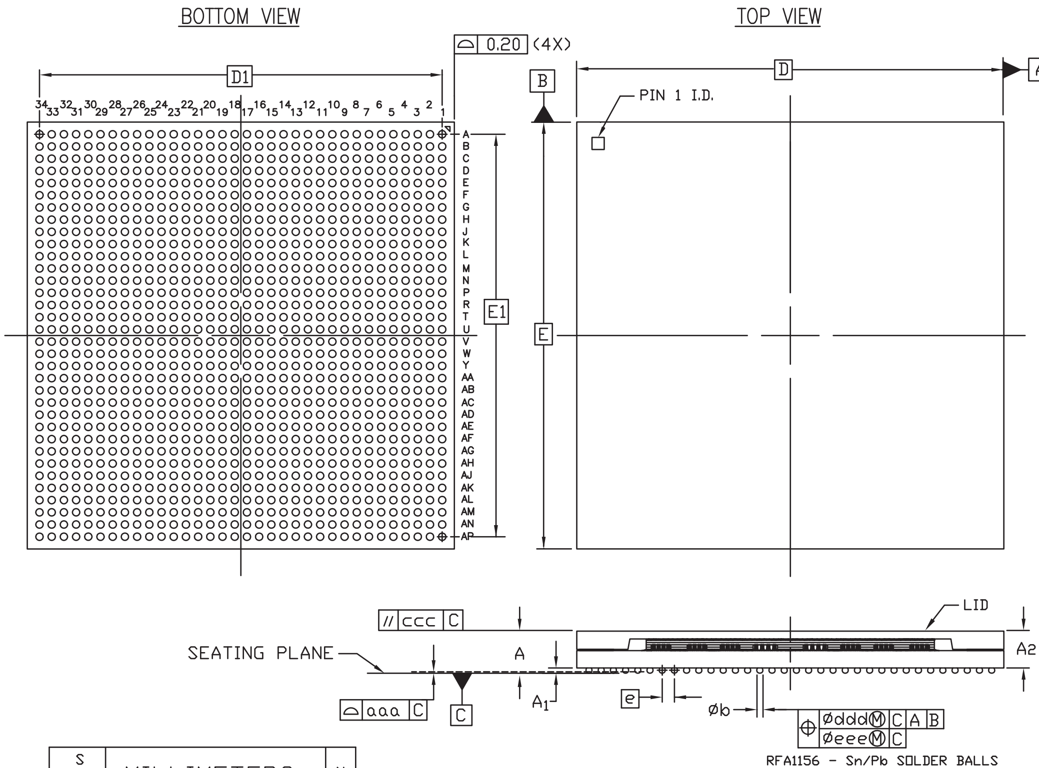
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156

ug575_c4_r2_032417

Figure 4-23: **Package Dimensions for RFA1156 (XQKU040)**

RFA1156 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQKU060 and XQKU095)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.32	3.52	3.72	
A_1	0.40	0.50	0.60	
A_2	2.82	3.02	3.22	
D/E	35.00 BASIC			
D1/E1	33.00 REF			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	4
aaa	-	-	0.20	
ccc	-	-	0.35	
ddd	-	-	0.30	
eee	-	-	0.10	
M	34			2

NOTES:

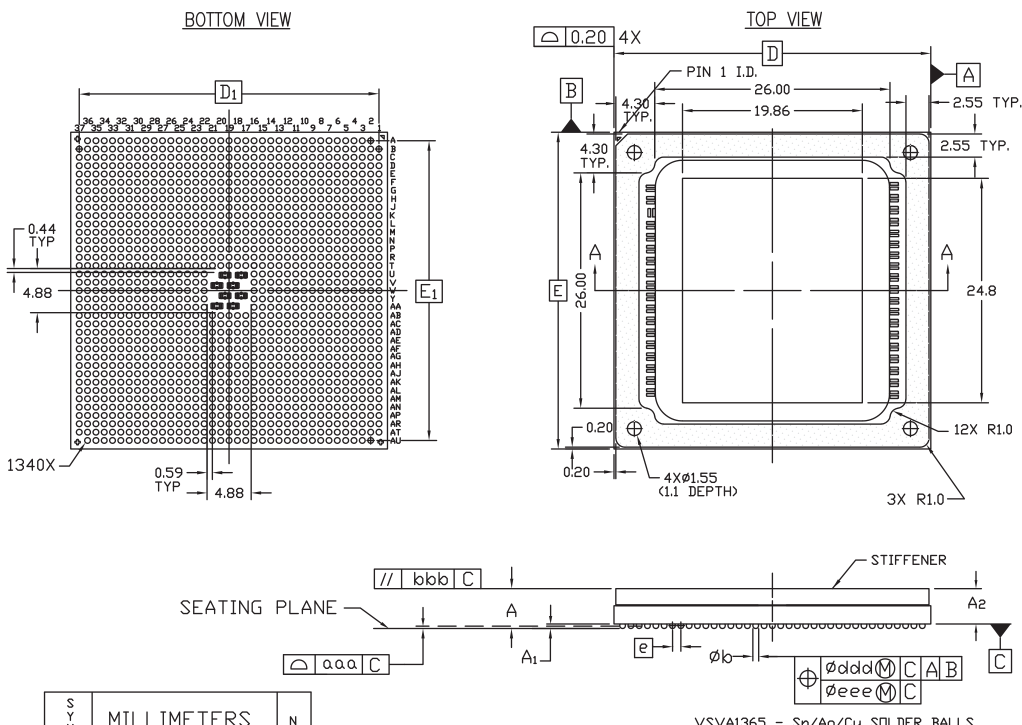
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAR-1
4. ACTUAL SOLDER BALL COUNT = 1156

ug575_c4_r3_032417

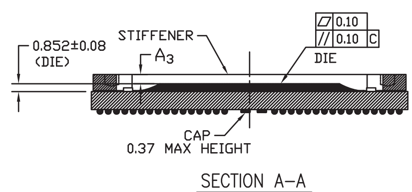
Figure 4-24: **Package Dimensions for RFA1156 (XQKU060 and XQKU095)**

VSVA1365 Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA (XCVU23P)

IMPORTANT: *This package includes land-side capacitors (LSC), a region of the BGA matrix where the BGA balls are replaced with capacitors. The LSC ball grid size for this package is 5 x 5 in terms of the number of BGA balls replaced by capacitors. Therefore, this package has fewer balls than the package name implies (i.e., the package has 5 x 5 = 25 fewer balls than the implied 1365 balls).*



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.20	4.40	4.60	
A_1	0.40	0.50	0.60	
A_2	3.70	3.90	4.10	
A_3	0.94	1.04	1.14	
D/E	35.00 BASIC			
D_1/E_1	33.12 BASIC			
e	0.92 BASIC			
Øb	0.50	0.64	0.70	
aaa	~	~	0.20	
bbb	~	~	0.35	
ddd	~	~	0.25	
eee	~	~	0.10	
M	37			2



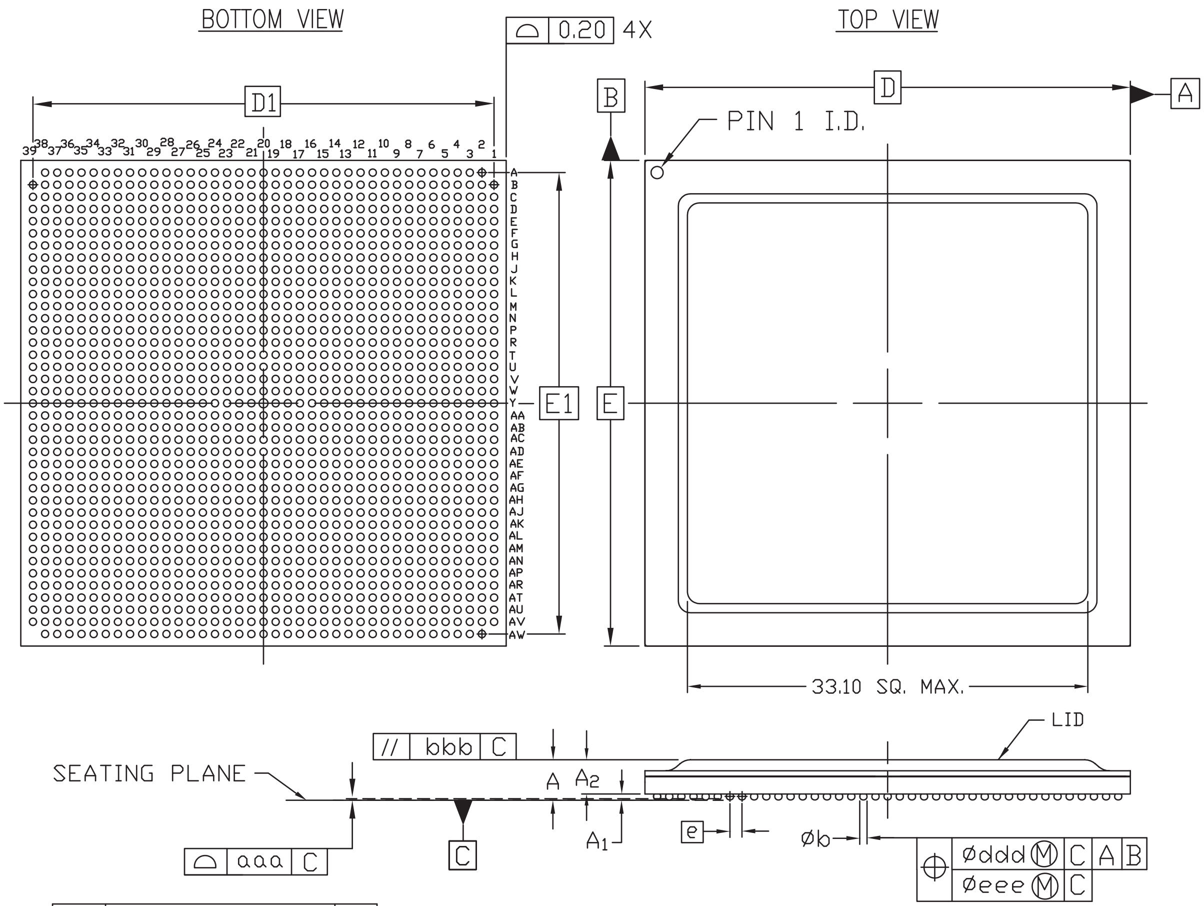
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.

ug575_vsva1365_vu23p_3182022

Figure 4-25: **Package Dimensions for VSVA1365 (XCVU23P)**

FFVA1517, FFVC1517, and FFVD1517 Flip-Chip, Fine-Pitch, BGA (XCKU060, XCKU095, XCVU065, XCVU080, XCVU095)



FFVA1517 - Sn/Ag/Cu SOLDER BALLS
FFVC1517 - Sn/Ag/Cu SOLDER BALLS
FFVD1517 - Sn/Ag/Cu SOLDER BALLS

SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.11	3.31	3.51	
A_1	0.40	0.50	0.60	
A_2	2.61	2.81	3.01	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	-	-	0.20	
bbb	-	-	0.25	
ddd	-	-	0.25	
eee	-	-	0.10	
M		39		2

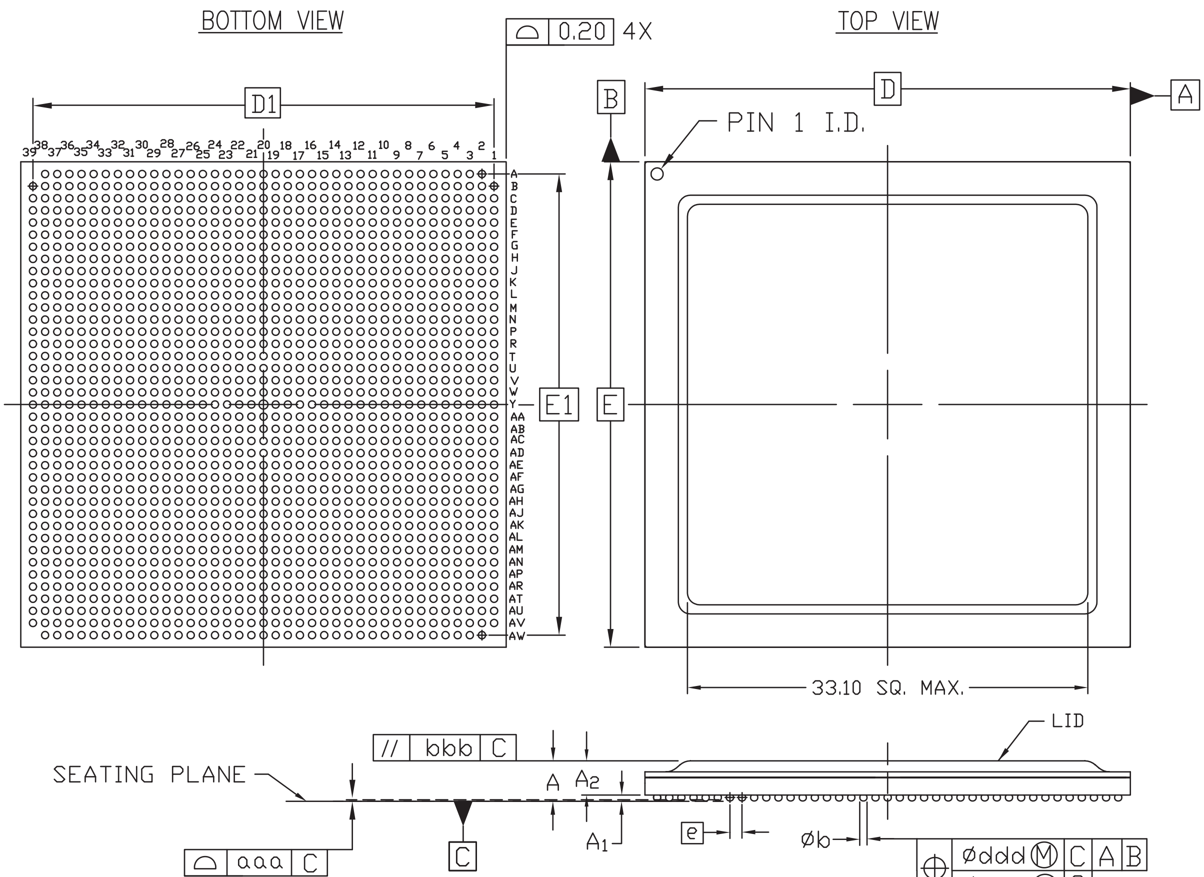
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAU-1 (DEPOPULATED)

ug575_c4_07_041816

Figure 4-26: **Package Dimensions for FFVA1517 (XCKU060), FFVC1517 (XCKU095, XCVU065, XCVU080, and XCVU095) and FFVD1517 (XCVU080 and XCVU095)**

FFVC1517 (XCVU3P) and FFVE1517 (XCKU11P and XCKU15P) Flip-Chip, Fine-Pitch, BGA



FFVC1517 – Sn/Ag/Cu SOLDER BALLS
FFVE1517 – Sn/Ag/Cu SOLDER BALLS

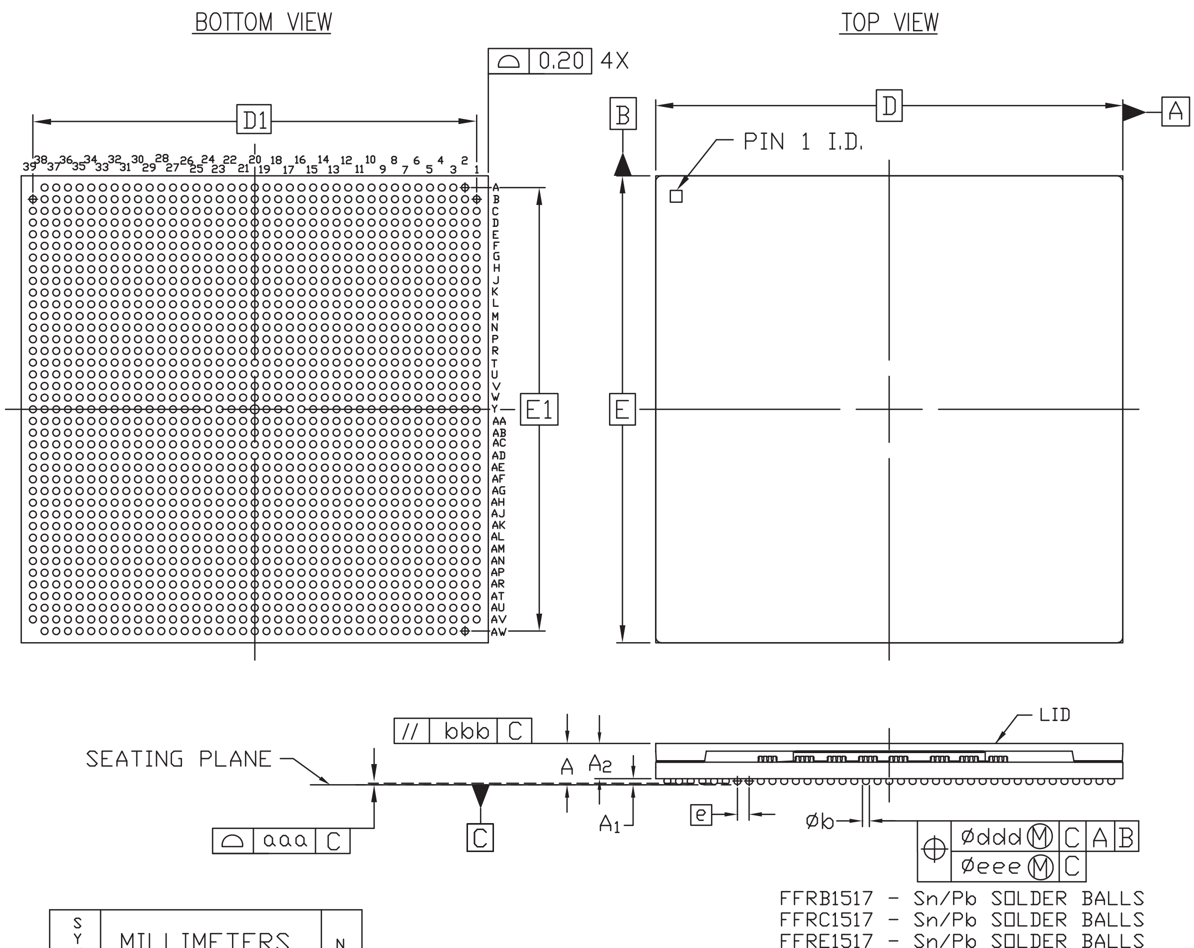
SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.11	3.31	3.51	
A_1	0.40	0.50	0.60	
A_2	2.61	2.81	3.01	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M		39		2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

Figure 4-27: **Package Dimensions for FFVC1517 (XCVU3P) and FFVE1517 (XCKU11P and XCKU15P)**

FFRC1517 (XQVU3P) and FFRE1517 (XQKU15P) Ruggedized Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E		40.00 BASIC		
D_1/E_1		38.00 BASIC		
e		1.00 BASIC		
øb	0.50	0.60	0.70	
aaa	—	—	0.20	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M		39		2

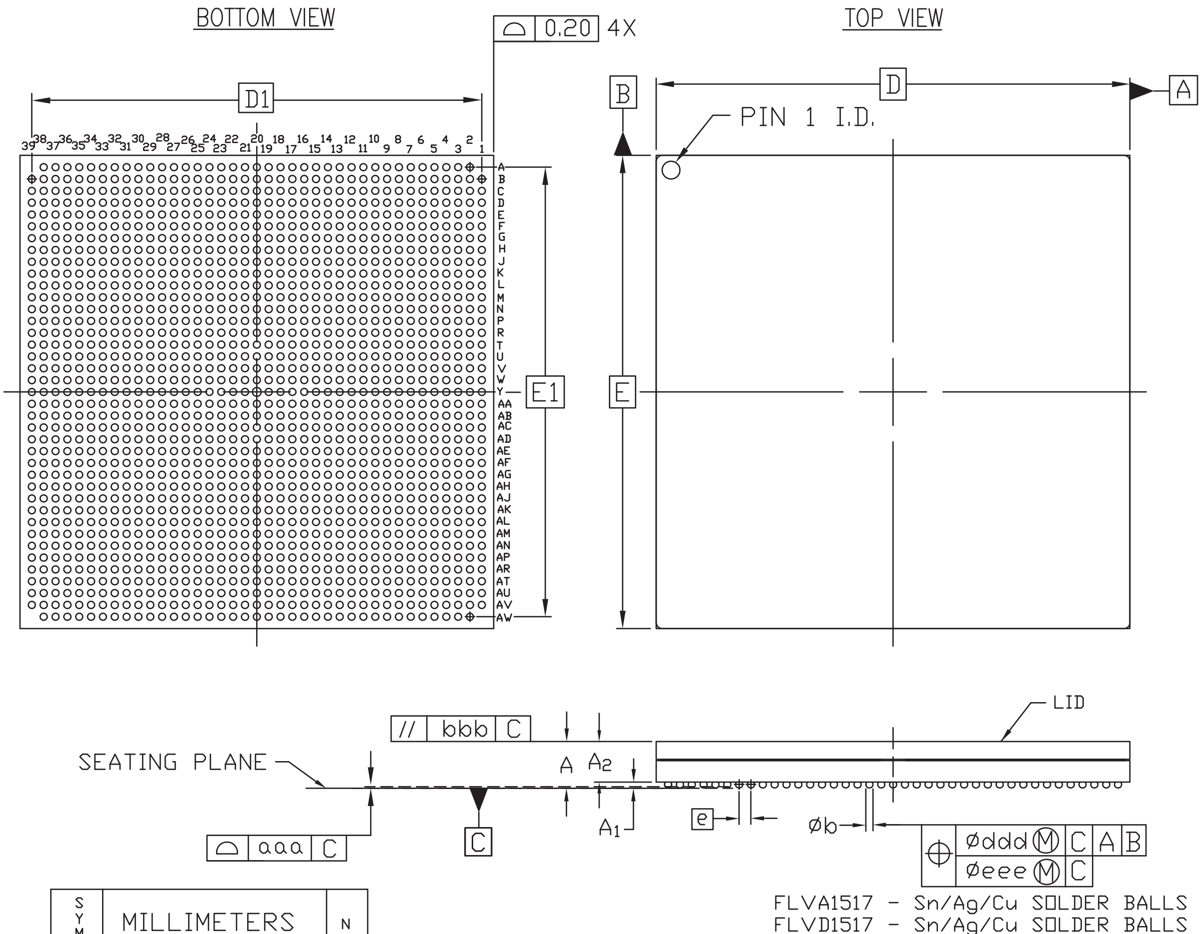
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAU-1 (DEPOPULATED)

ug575_c4_ffrc1517_ffre1517_010719

Figure 4-28: **Package Dimensions for FFRC1517 (XQVU3P) and FFRE1517 (XQKU15P)**

FLVA1517 (XCKU085 and XCKU115) and FLVD1517 (XCKU115 and XCVU125) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.69	3.89	4.09	
A_1	0.40	0.50	0.60	
A_2	3.19	3.39	3.59	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M		39		2

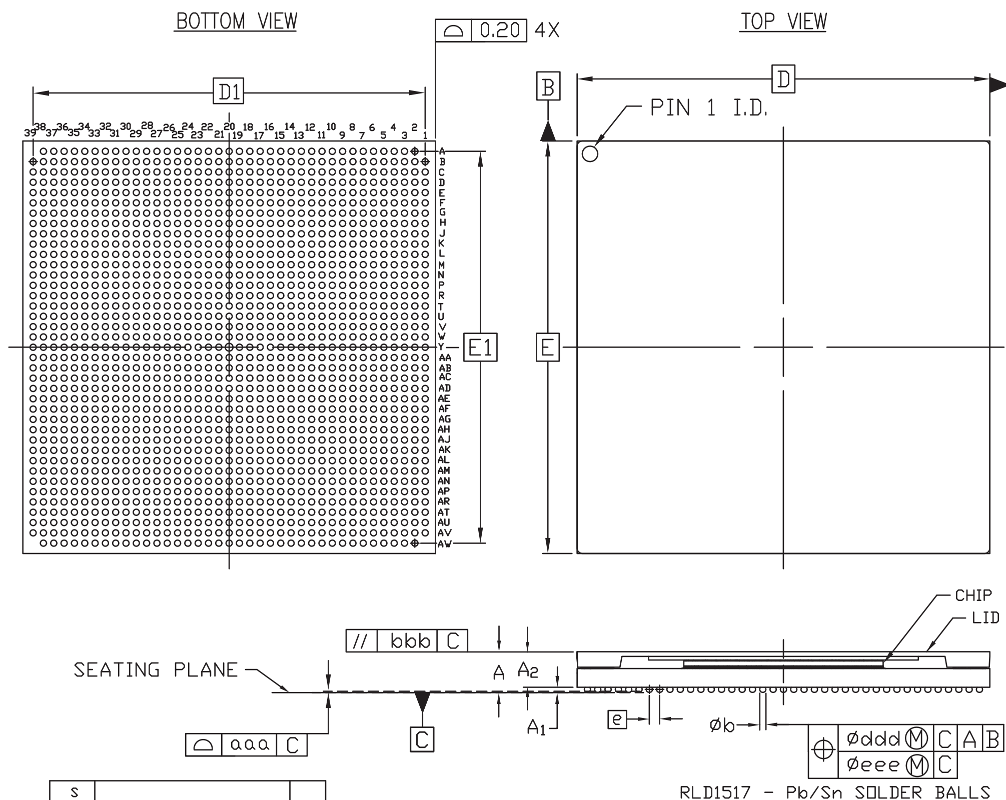
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

ug575_c4_08_010715

Figure 4-29: **Package Dimensions for FLVA1517 (XCKU085 and XCKU115) and FLVD1517 (XCKU115 and XCVU125)**

RLD1517 Ruggedized Flip-Chip, Fine-Pitch, BGA (XQKU115)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.74	3.94	4.14	
A_1	0.40	0.50	0.60	
A_2	3.24	3.44	3.64	
D/E	40.00 BASIC			
D_1/E_1	38.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M		39		2

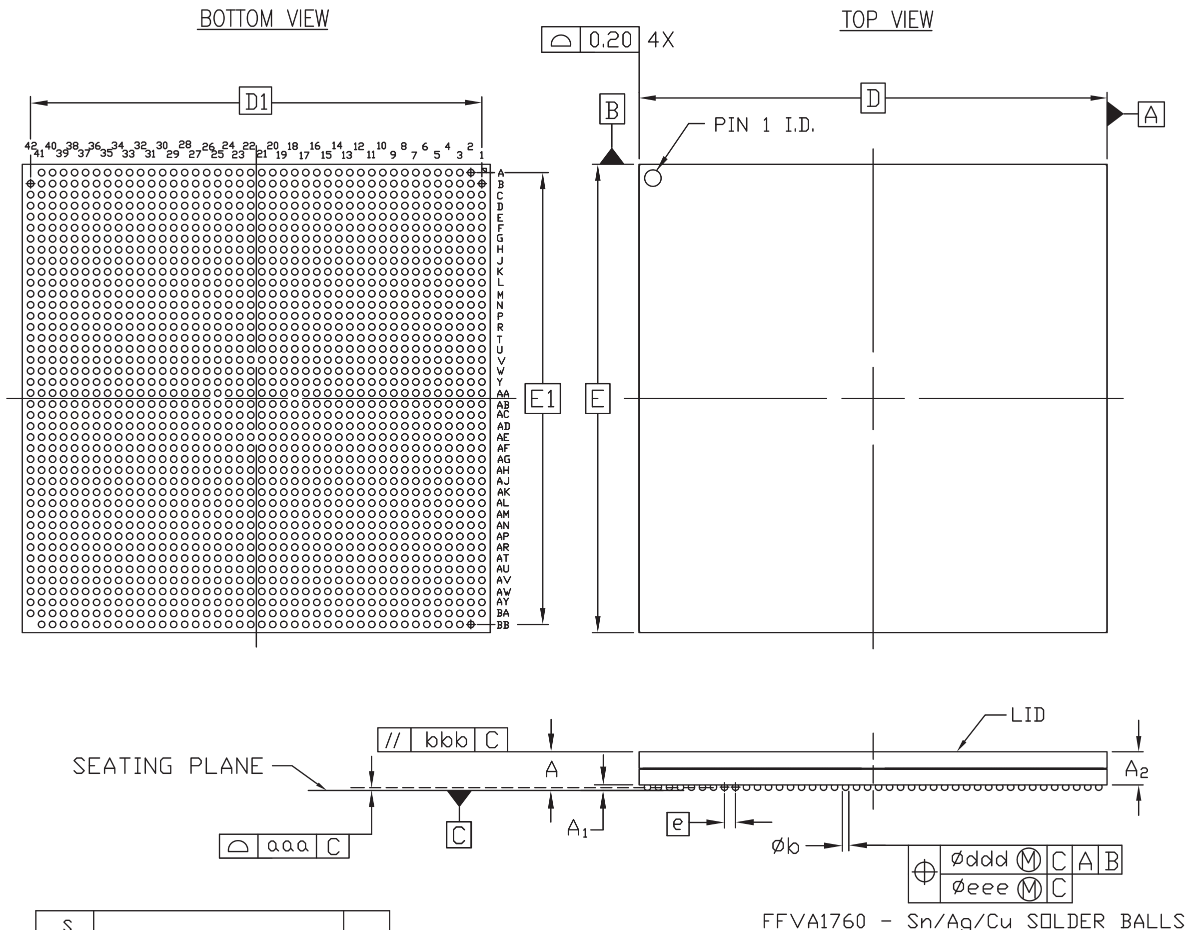
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAU–1 (DEPOPULATED)

ug575_c4_r4_032417

Figure 4-30: **Package Dimensions for RLD1517 (XQKU115)**

FFVA1760 Flip-Chip, Fine-Pitch, BGA (XCKU15P)



SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	-	-	0.20	
bbb	-	-	0.25	
ddd	-	-	0.25	
eee	-	-	0.10	
M	42			2

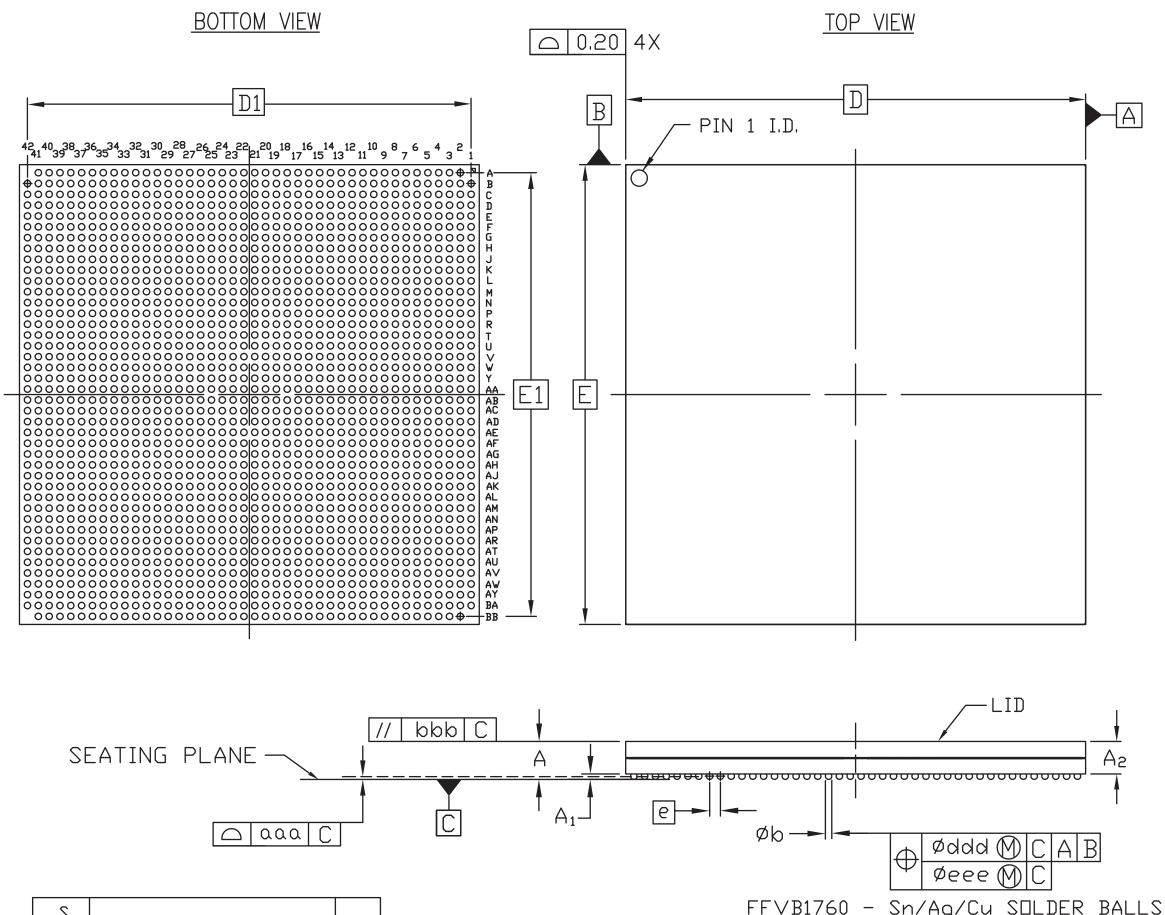
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAV-1 (DEPOPULATED)

ug575_c4_ffva1760_ku15p_041917

Figure 4-31: **Package Dimensions for FFVA1760 (XCKU15P)**

FFVB1760 Flip-Chip, Fine-Pitch, BGA (XCKU095, XCVU080, and XCVU095)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	42.50 BASIC			
D1/E1	41.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	42			2

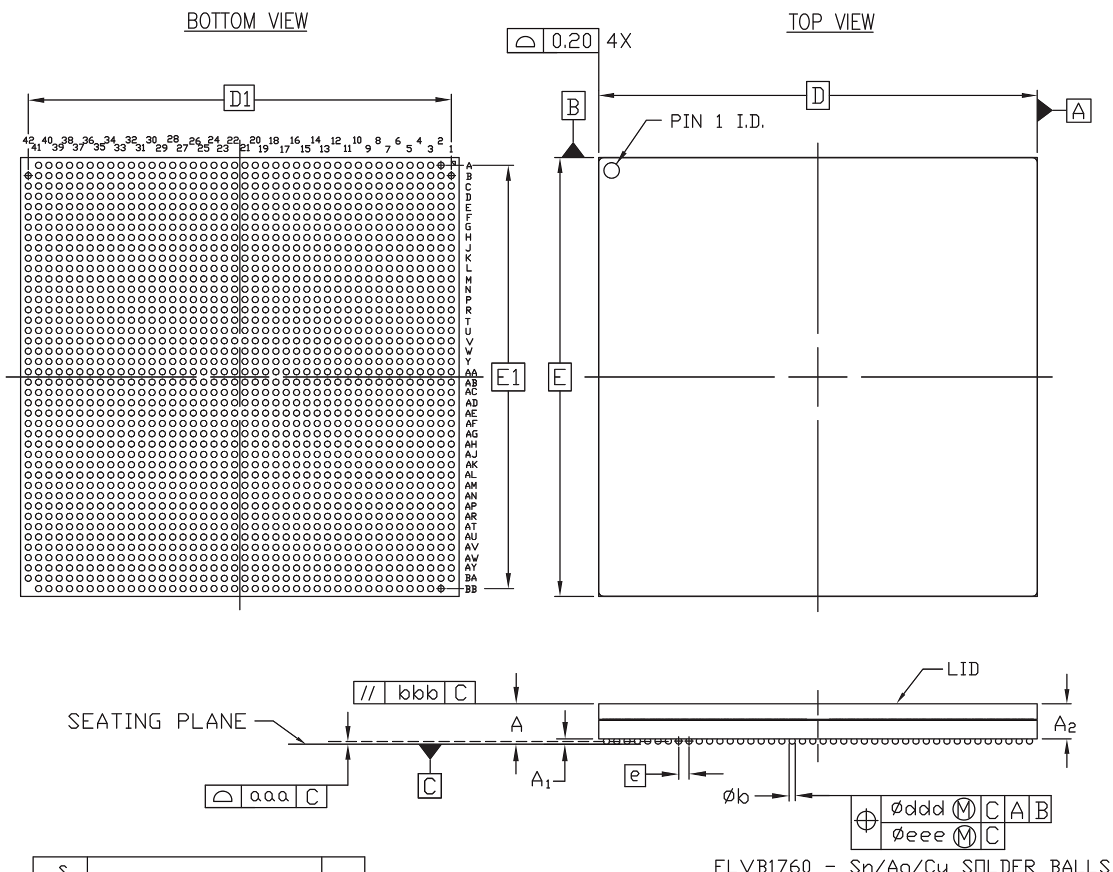
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

ug575_c4_09_041617

Figure 4-32: **Package Dimensions for FFVB1760 (XCKU095, XCVU080, and XCVU095)**

FLVB1760 Flip-Chip, Fine-Pitch, BGA (XCKU085, XCKU115, and XCVU125)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.71	3.91	4.11	
A_1	0.40	0.50	0.60	
A_2	3.21	3.41	3.61	
D/E	42.50 BASIC			
D1/E1	41.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	42			2

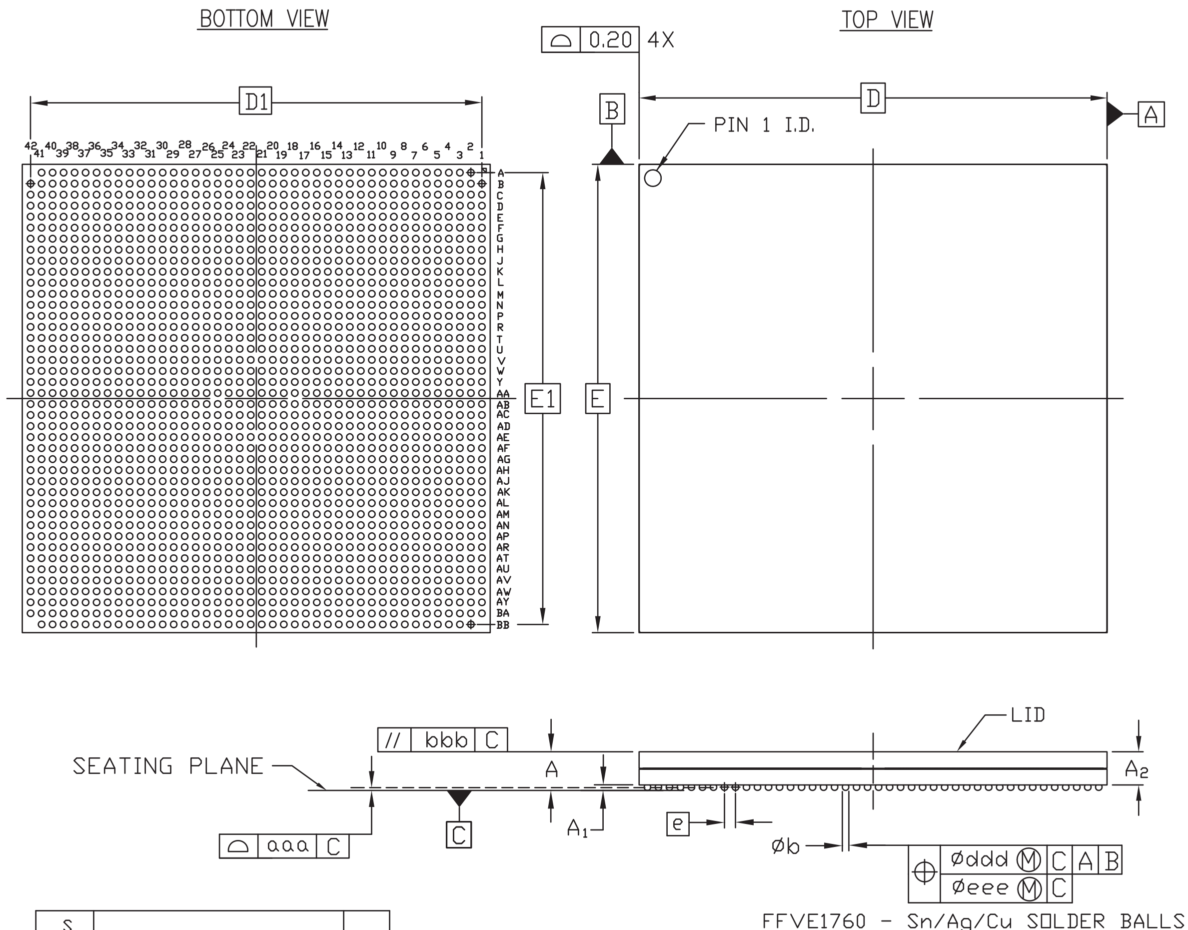
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)

ug575_c4_111_041615

Figure 4-33: **Package Dimensions for FLVB1760 (XCKU085, XCKU115, and XCVU125)**

FFVE1760 Flip-Chip, Fine-Pitch, BGA (XCKU15P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.31	3.51	3.71	
A_1	0.40	0.50	0.60	
A_2	2.81	3.01	3.21	
D/E	42.50 BASIC			
D1/E1	41.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.20	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	42			2

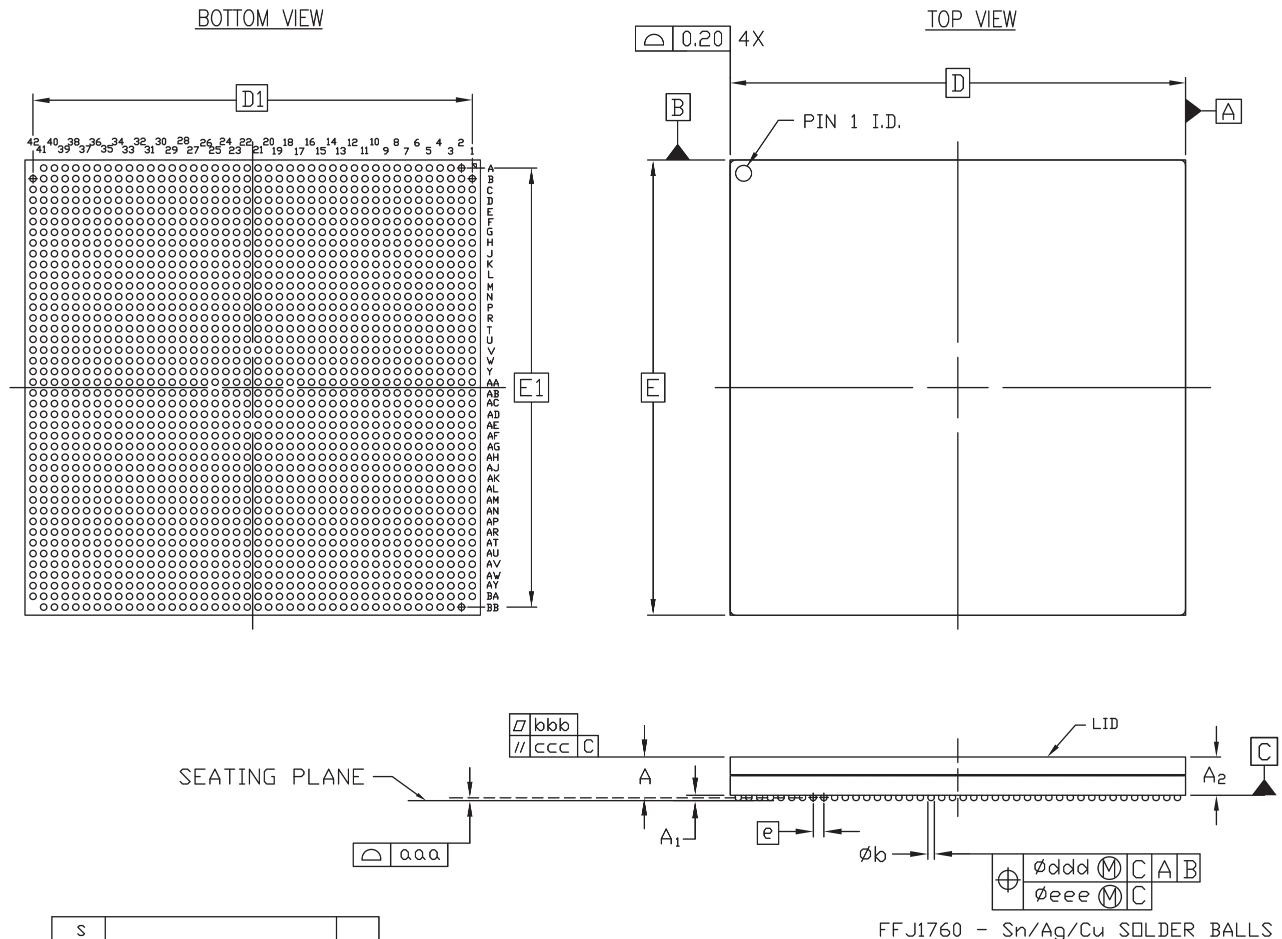
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAV-1 (DEPOPULATED)

ug575_c4_ffve1760_ku15p_042017

Figure 4-34: **Package Dimensions for FFVE1760 (XCKU15P)**

FFVJ1760 Flip-Chip, Fine-Pitch, BGA (XCKU19P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.87	4.07	4.27	
A_1	0.40	0.50	0.60	
A_2	3.37	3.57	3.77	
D/E		42.50 BASIC		
D1/E1		41.00 BASIC		
e		1.00 BASIC		
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.10	
ccc	~	~	0.10	
ddd	~	~	0.25	
eee	~	~	0.10	
M		42		2

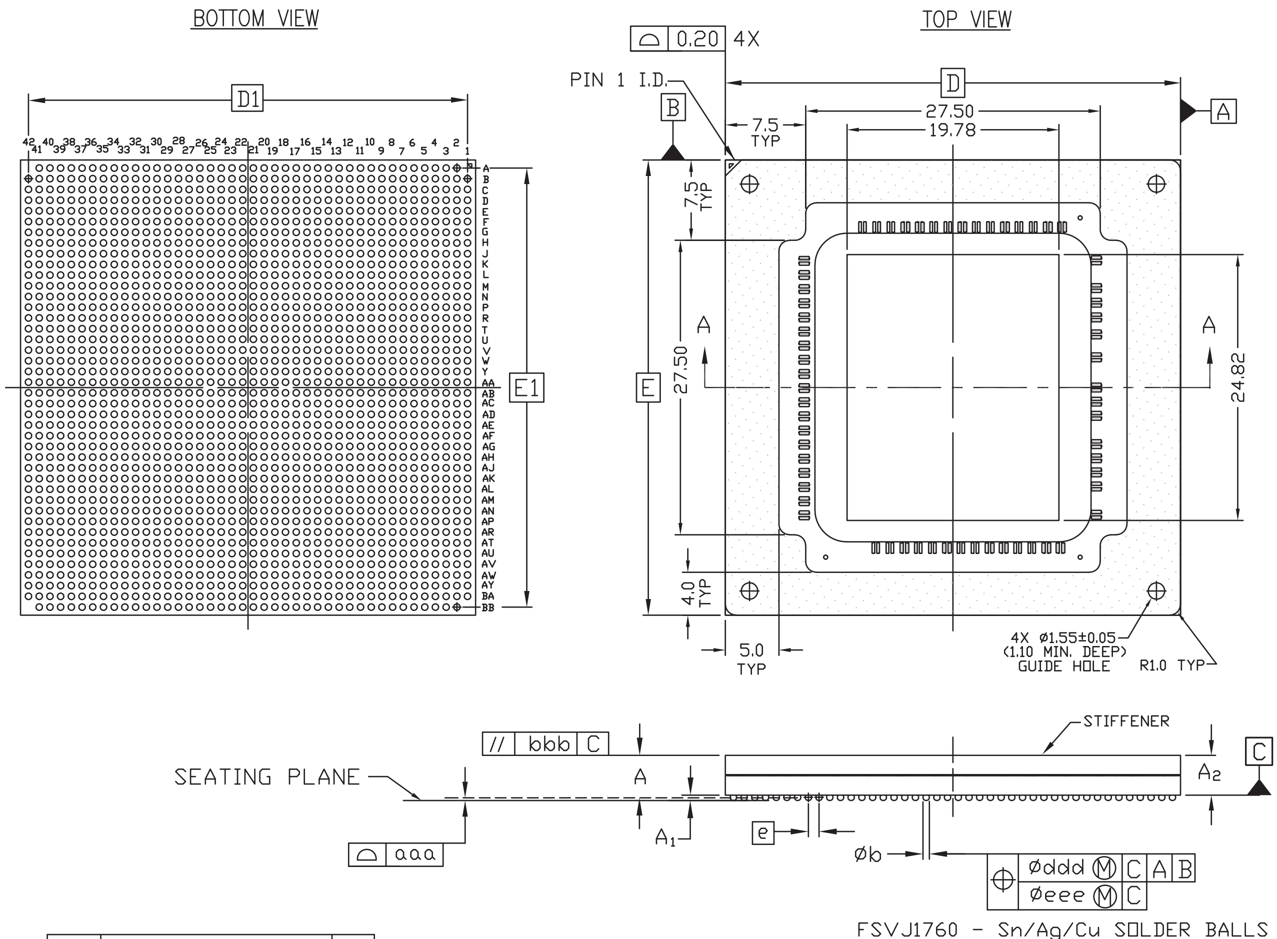
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–318–EF–1764 (DEPOPULATED)

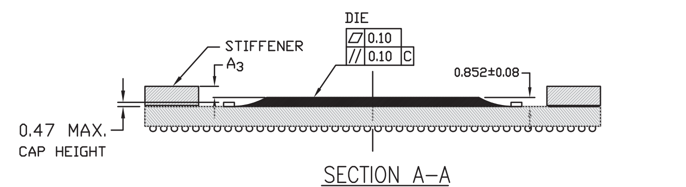
ug575_c4_ffvj1760_083020

Figure 4-35: **Package Dimensions for FFVJ1760 (XCKU19P)**

FSVJ1760 Flip-Chip, Fine-Pitch, BGA (XCVU23P)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.02	4.22	4.42	
A_1	0.40	0.50	0.60	
A_2	3.52	3.72	3.92	
A_3	1.01	1.04	1.07	
D/E	42.50 BASIC			
D_1/E_1	41.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	-	-	0.20	
bbb	-	-	0.35	
ddd	-	-	0.25	
eee	-	-	0.10	
M	42			2



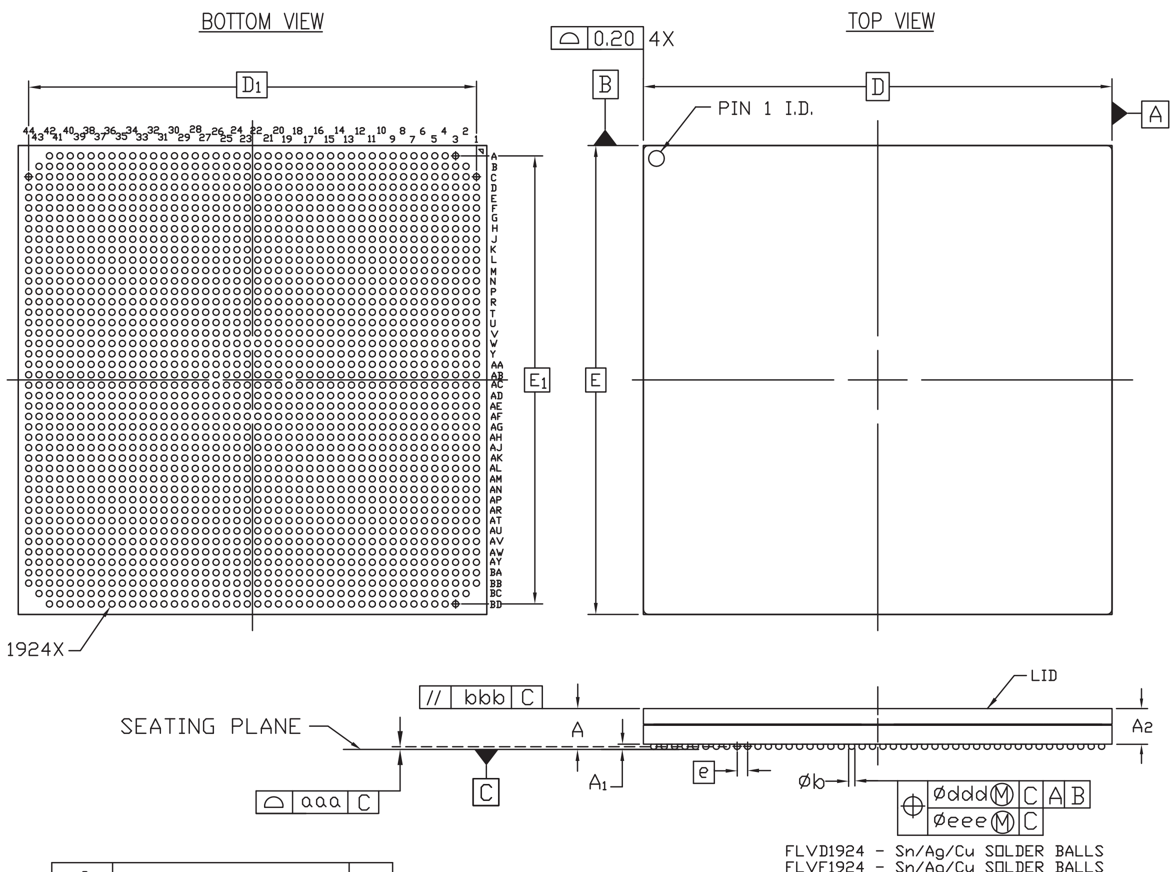
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MO–318 P42.5x42.5–EF–1764 (DEPOPULATED)

ug575_fsvj1760_vu23p_122120

Figure 4-36: **Package Dimensions for FSVJ1760 (XCVU23P)**

FLVD1924 (XCKU115) and FLVF1924 (XCKU085 and XCKU115) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.73	3.93	4.13	
A_1	0.40	0.50	0.60	
A_2	3.23	3.43	3.63	
D/E	45.00 BASIC			
D_1/E_1	43.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	44			2

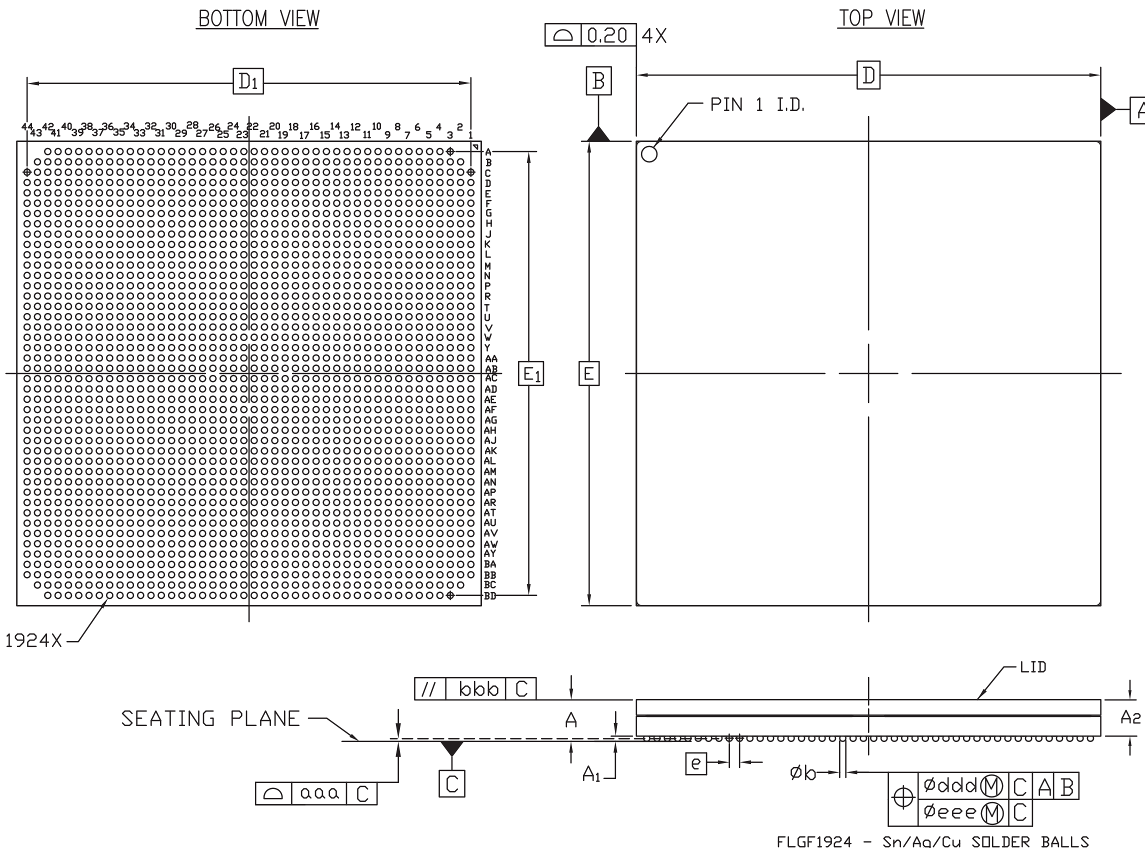
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_10_010715

Figure 4-37: **Package Dimensions for FLVD1924 (XCKU115) and FLVF1924 (XCKU085 and XCKU115)**

FLGF1924 (XCVU11P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.84	4.04	4.24	
A_1	0.40	0.50	0.60	
A_2	3.34	3.54	3.74	
D/E	45.00 BASIC			
D_1/E_1	43.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

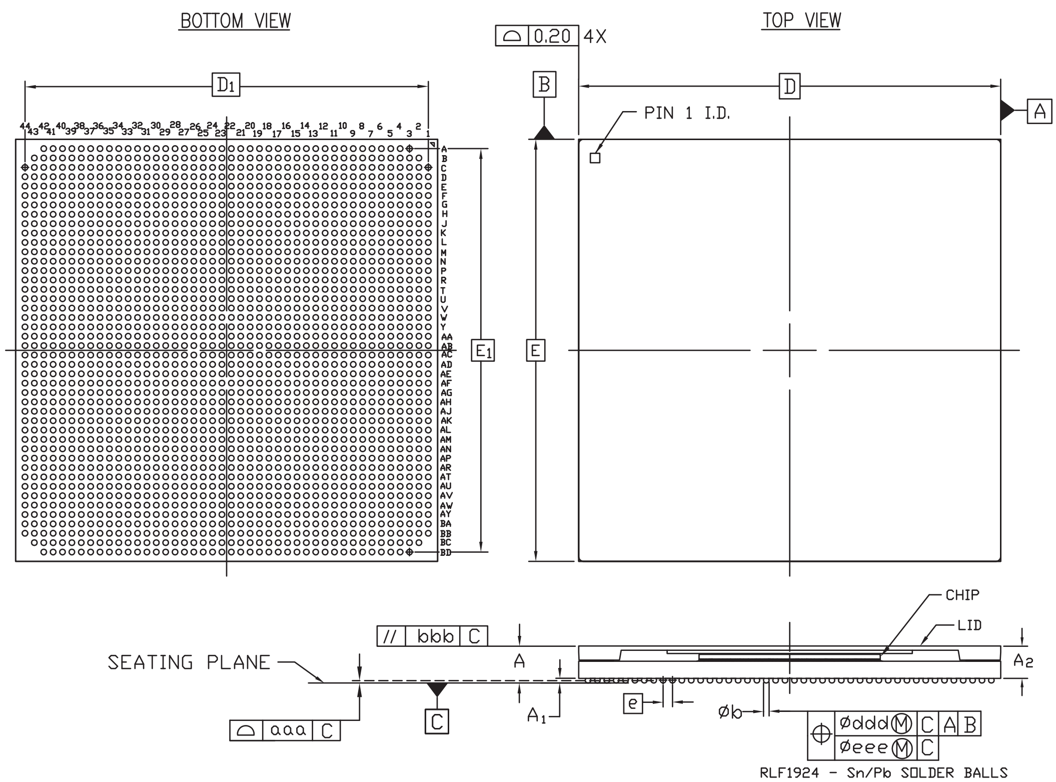
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

ug575_c4_flgf1924_040217

Figure 4-38: **Package Dimensions for FLFG1924 (XCVU11P)**

RLF1924 (XQKU115) Ruggedized Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.75	3.95	4.15	
A_1	0.40	0.50	0.60	
A_2	3.25	3.45	3.65	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	44			2

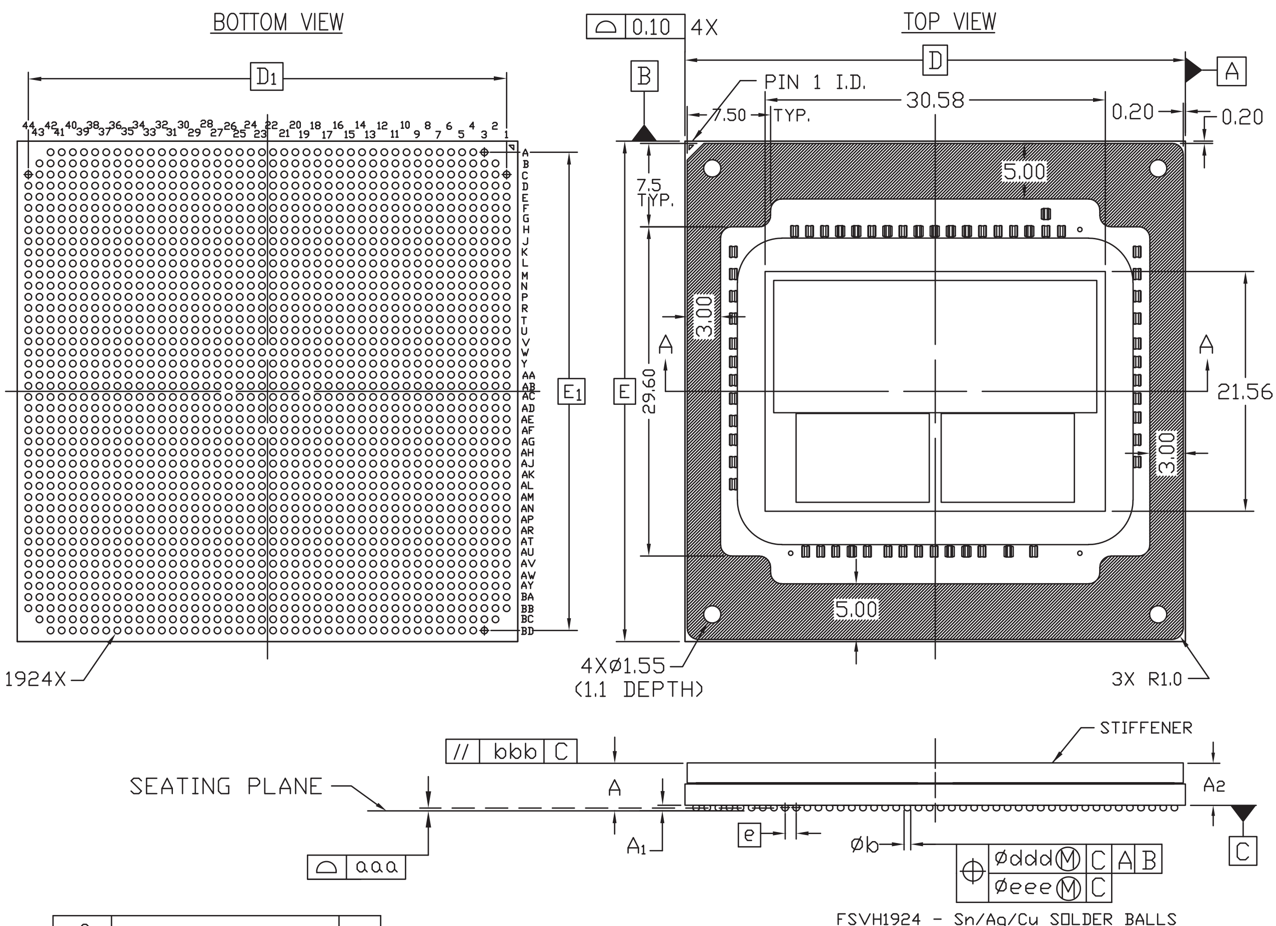
NOTES:

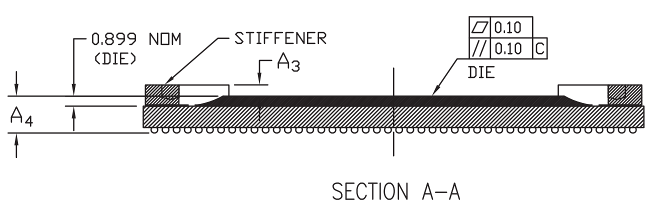
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924
4. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

ug575_c4_r5_032417

Figure 4-39: **Package Dimensions for RLF1924 (XQKU115)**

FSVH1924 (XCVU31P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA





SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.11	4.31	4.51	
A_1	0.40	0.50	0.60	
A_2	3.61	3.81	4.01	
A_3	0.89	0.99	1.09	
A_4	3.22	3.32	3.42	
D/E	45.00 BASIC			
D_1/E_1	43.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	--	--	0.30	
bbb	--	--	0.25	
ddd	--	--	0.25	
eee	--	--	0.10	
M	44			2

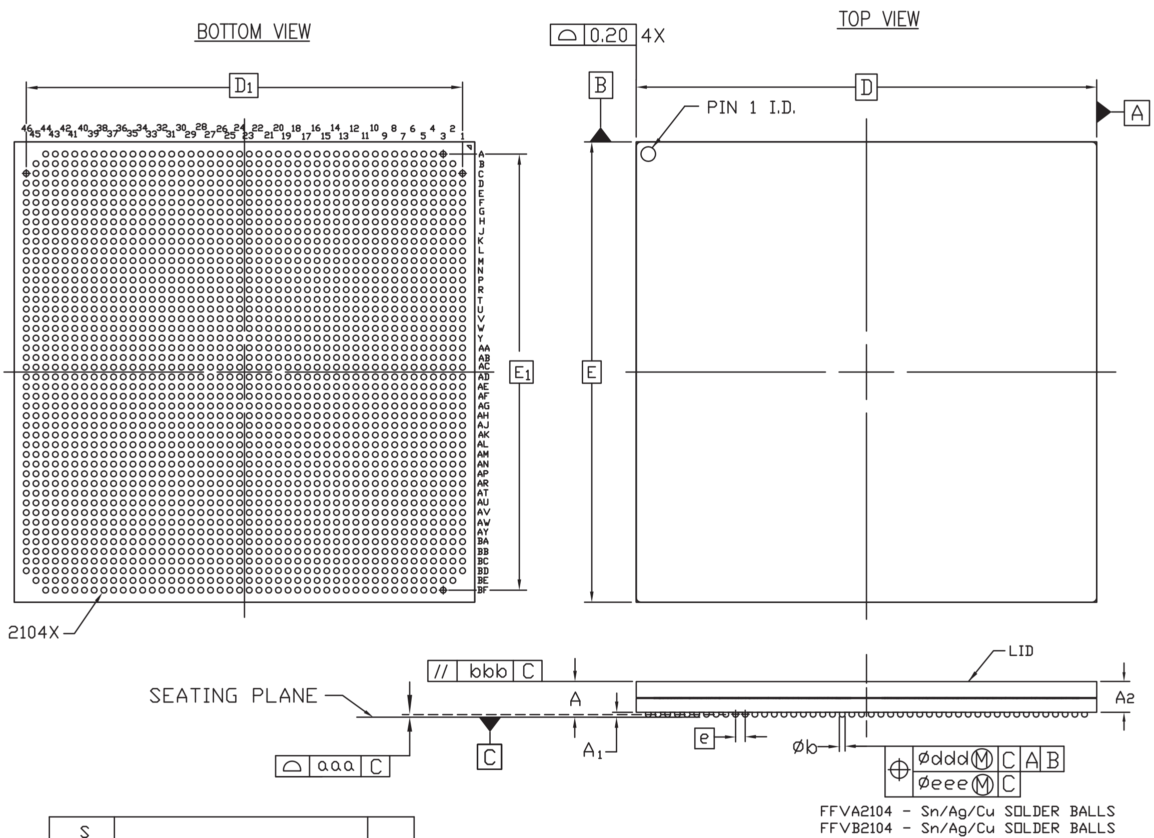
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAW-1 (DEPOPULATED)

ug575_fsvh1924_vu31p_122120

Figure 4-40: **Package Dimensions for FSVH1924 (XCVU31P)**

FFVA2104 (XCVU080 and XCVU095) and FFVB2104 (XCKU095, XCVU080, and XCVU095) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.46	3.66	3.86	
A_1	0.40	0.50	0.60	
A_2	2.96	3.16	3.36	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

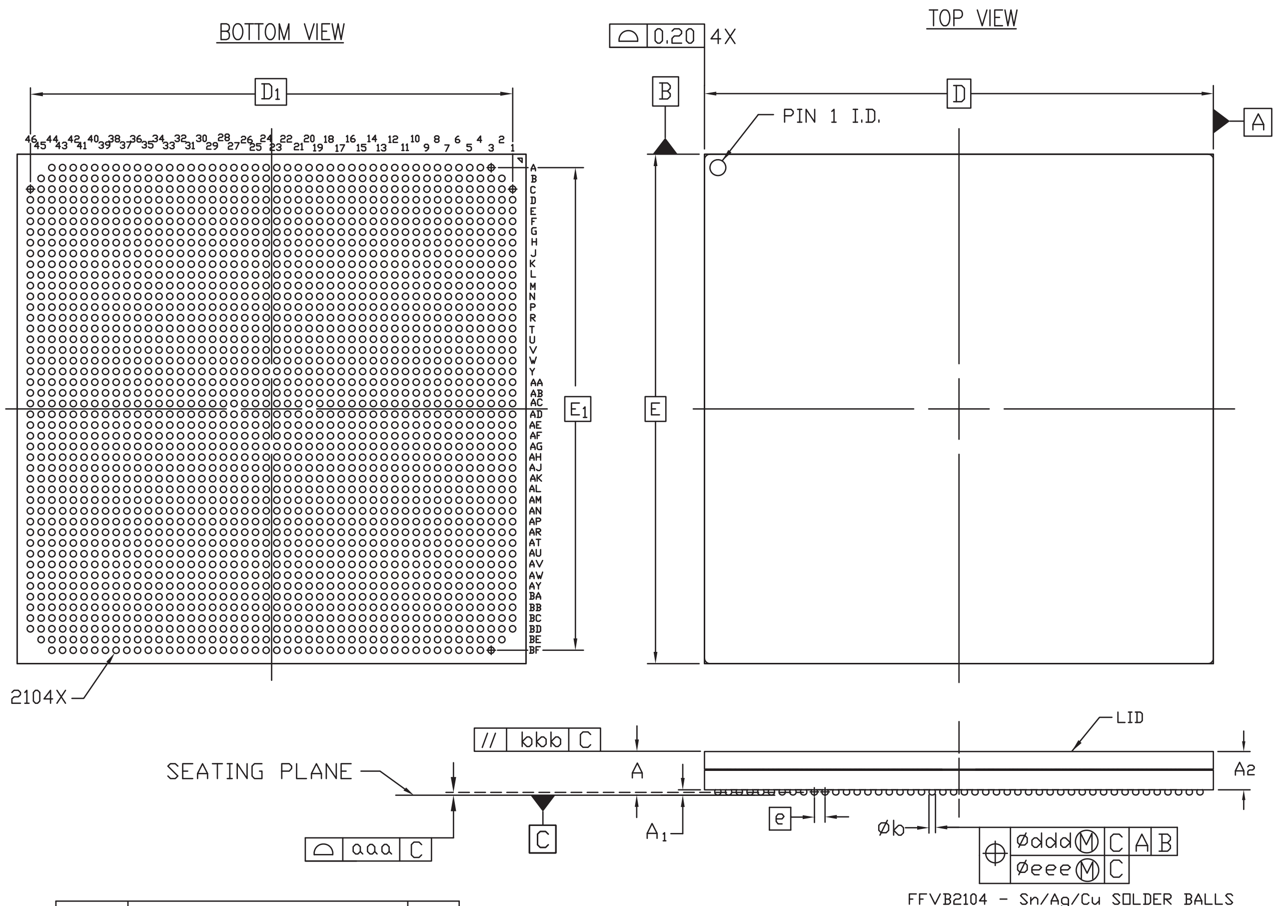
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_11_010715

Figure 4-41: **Package Dimensions for FFVA2104 (XCVU080, and XCVU095) and FFVB2104 (XCKU095, XCVU080, and XCVU095)**

FFVB2104 (XCKU19P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.87	4.07	4.27	
A_1	0.40	0.50	0.60	
A_2	3.37	3.57	3.77	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

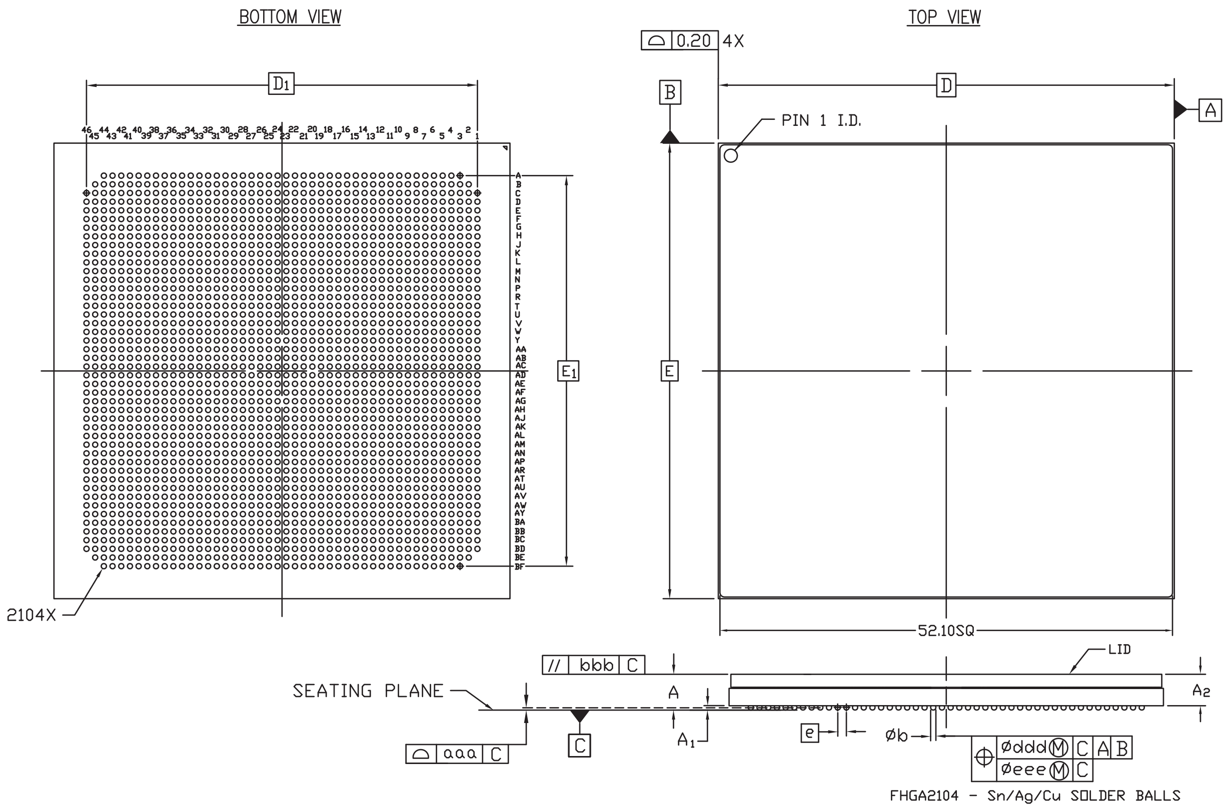
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_ffvb2104_083020

Figure 4-42: **Package Dimensions for FFVB2104 (XCKU19P)**

FHGA2104 (XCVU13P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.84	4.04	4.24	
A_1	0.40	0.50	0.60	
A_2	3.34	3.54	3.74	
D/E	52.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

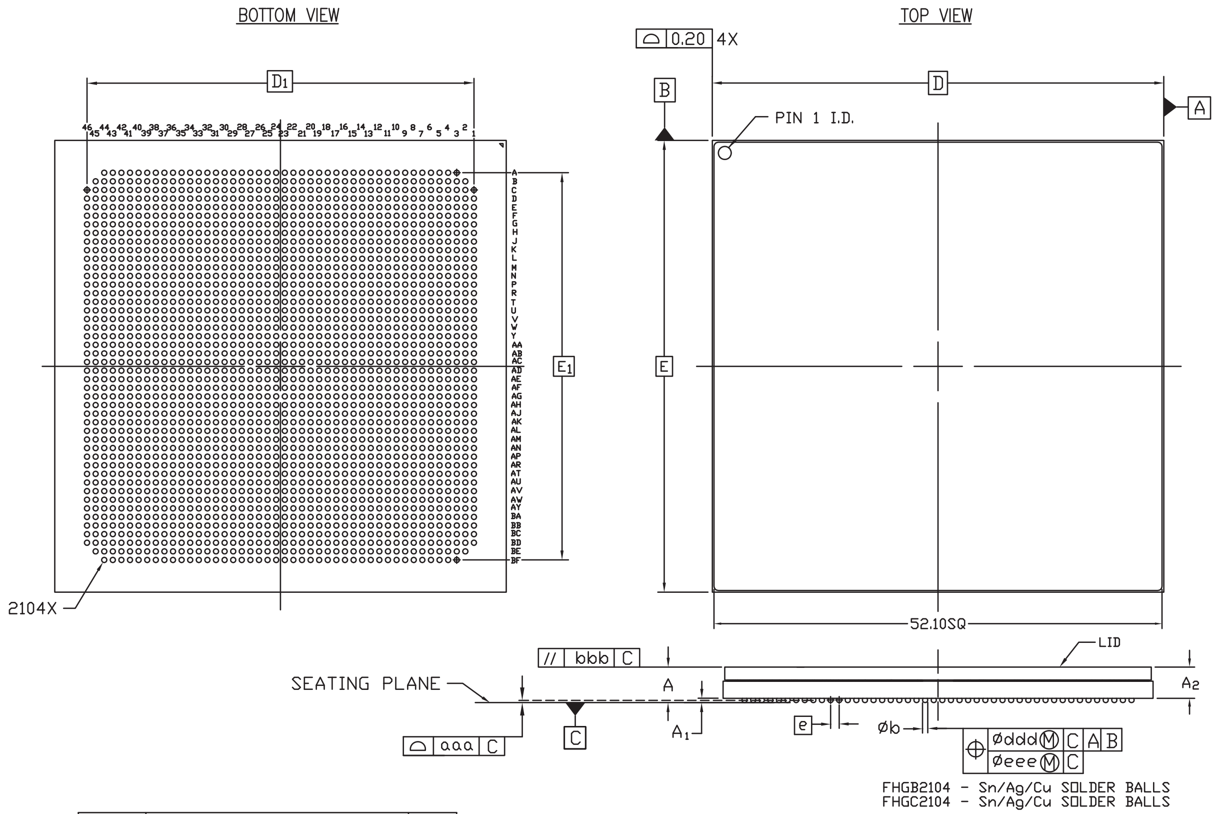
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-ABF-2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_fhga2104_vu13p_041917

Figure 4-43: **Package Dimensions for FHGA2104 (XCVU13P)**

FHGB2104 (XCVU13P) and FHGC2104 (XCVU13P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.92	4.12	4.32	
A1	0.40	0.50	0.60	
A2	3.42	3.62	3.82	
D/E	52.50 BASIC			
D1/E1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

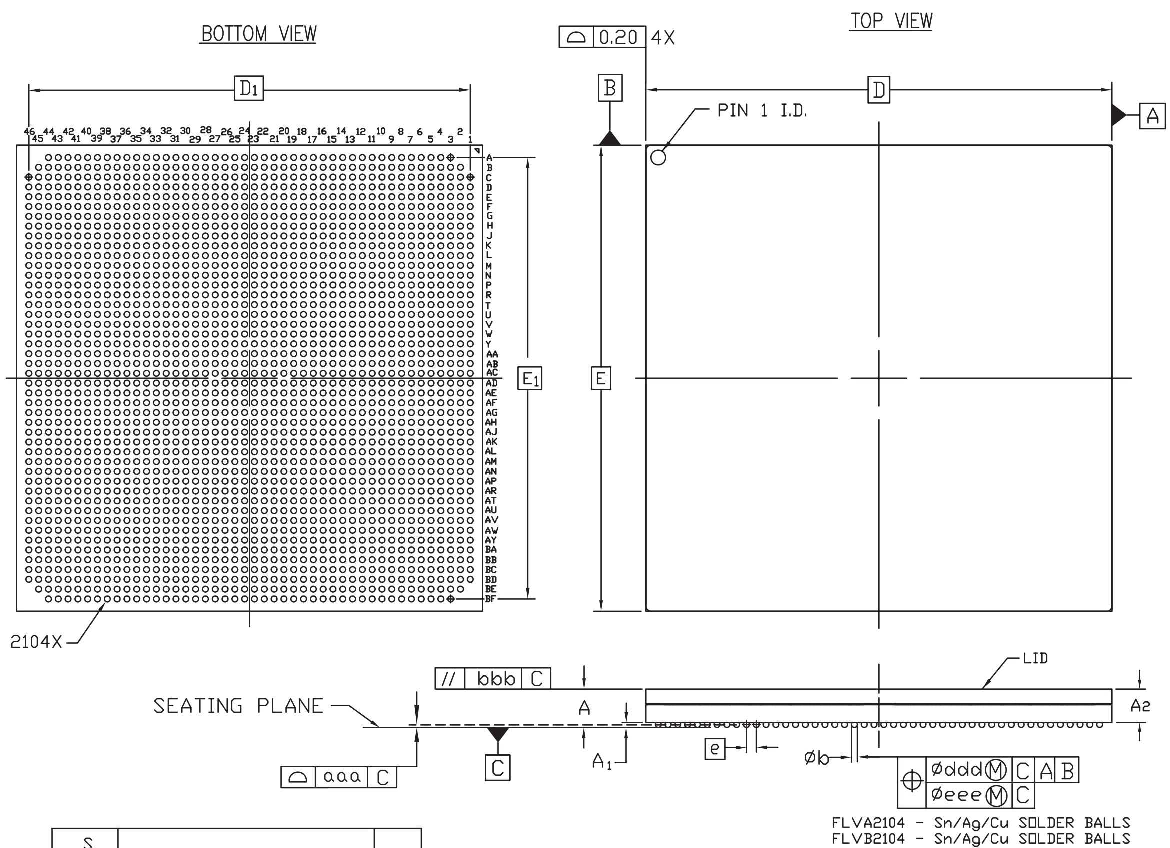
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-ABF-2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_fhgb2104_fhgc2104_vu13p_041917

Figure 4-44: **Package Dimensions for FHGB2104 (XCVU13P) and FHGC2104 (XCVU13P)**

FLVA2104 (XCKU115 and XCVU125) and FLVB2104 (XCKU115 and XCVU125) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	3.71	3.91	4.11	
A1	0.40	0.50	0.60	
A2	3.21	3.41	3.61	
D/E	47.50 BASIC			
D1/E1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

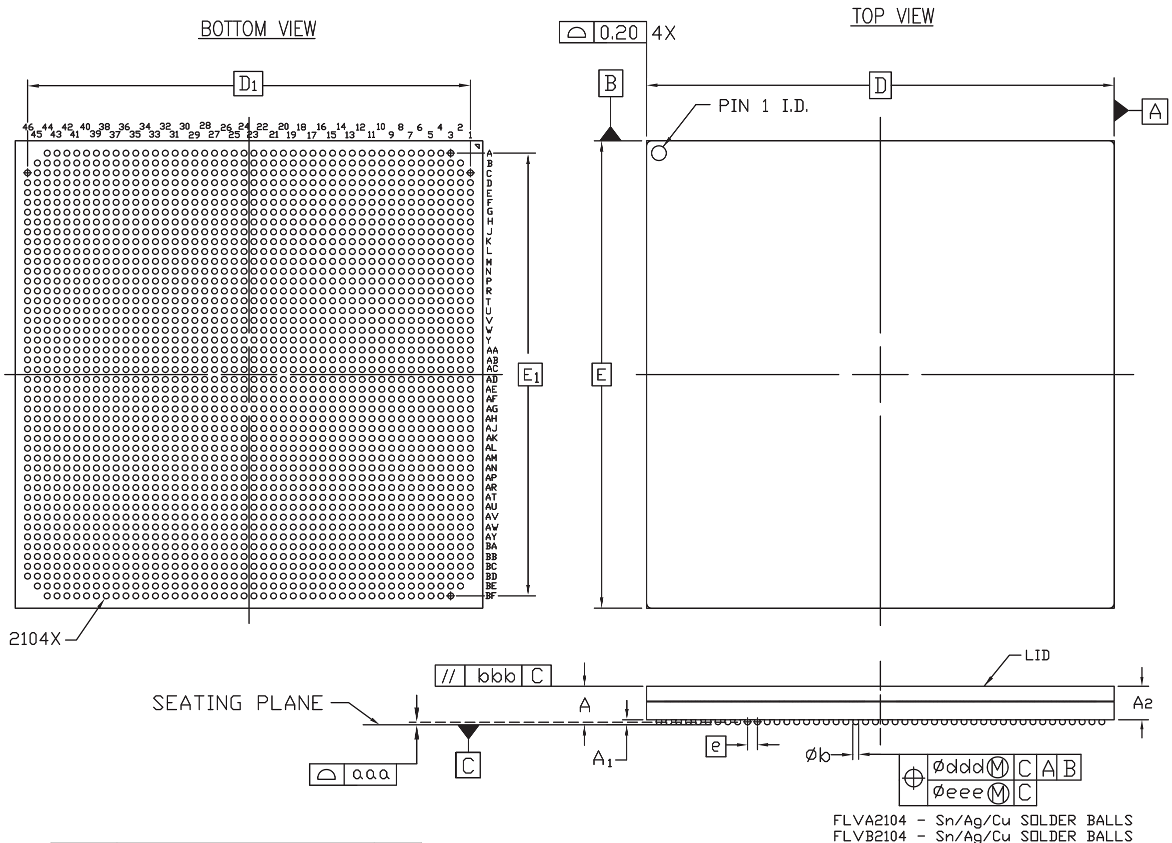
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAY-2 (DEPOPULATED)

ug575_c4_114_041615

Figure 4-45: **Package Dimensions for FLVA2104 (XCKU115 and XCVU125) and FLVB2104 (XCKU115 and XCVU125)**

FLVA2104 (XCVU5P and XCVU7P) and FLVB2104 (XCVU5P and XCVU7P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.71	3.91	4.11	
A_1	0.40	0.50	0.60	
A_2	3.21	3.41	3.61	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

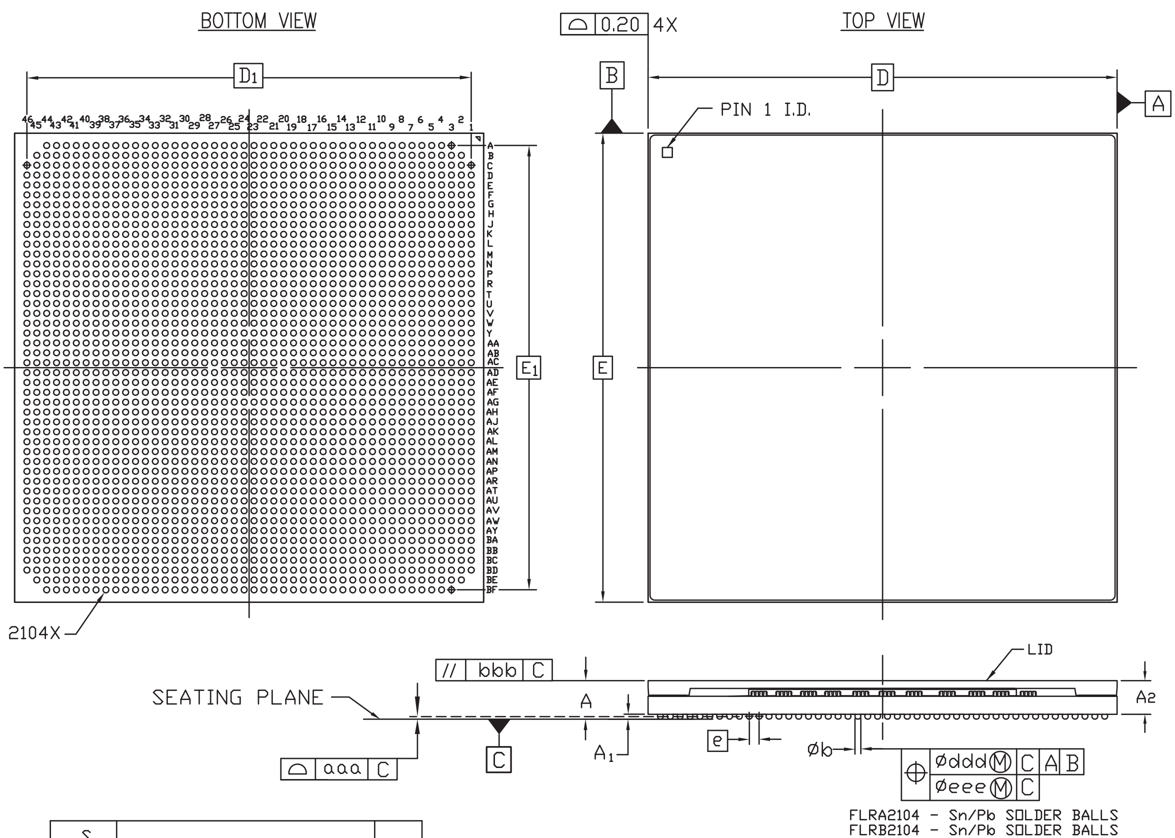
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_flvx_040217

Figure 4-46: **Package Dimensions for FLVA2104 (XCVU5P and XCVU7P) and FLVB2104 (XCVU5P and XCVU7P)**

FLRA2104 (XQVU7P) and FLRB2104 (XQVU7P) Ruggedized Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	3.71	3.91	4.11	
A_1	0.40	0.50	0.60	
A_2	3.21	3.41	3.61	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

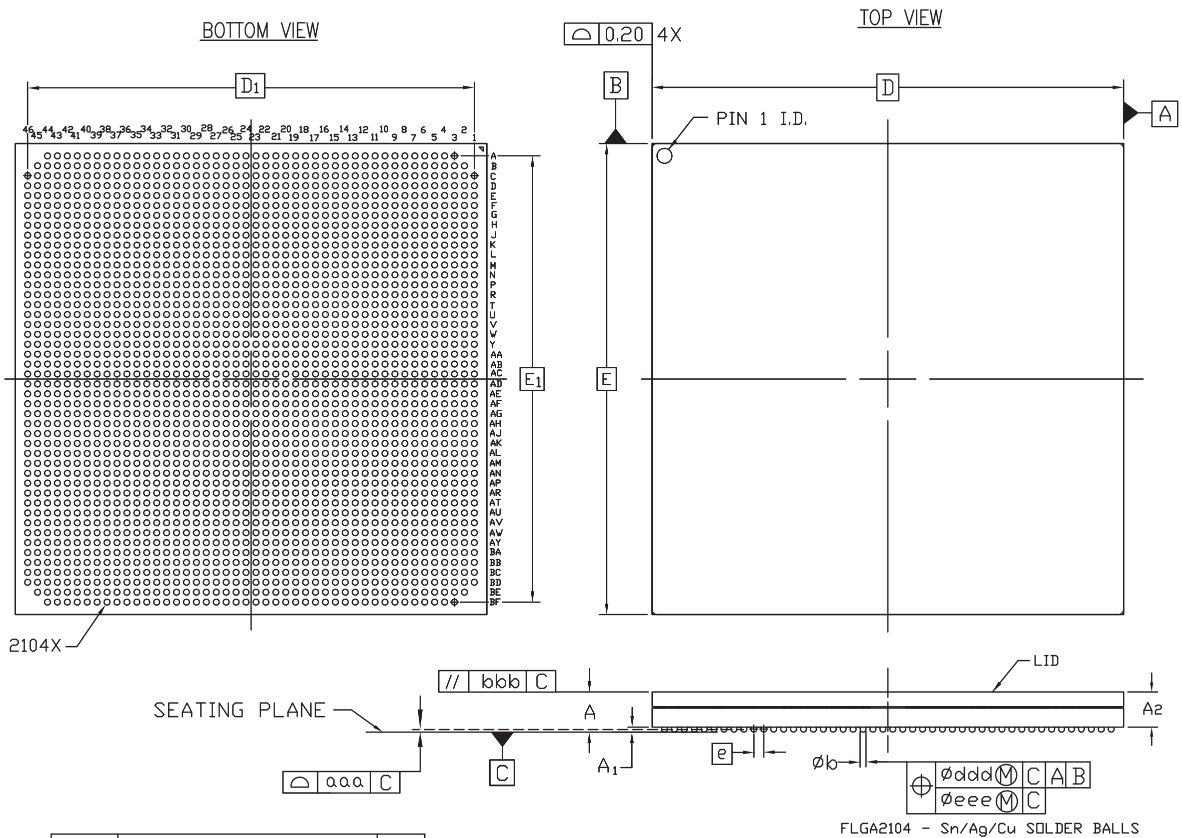
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAY-2 (DEPOPULATED)

ug575_c4_flra2104_flrb2104_010819

Figure 4-47: **Package Dimensions for FLRA2104 (XQVU7P) and FLRB2104 (XQVU7P)**

FLGA2104 (XCVU9P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.84	4.04	4.24	
A_1	0.40	0.50	0.60	
A_2	3.34	3.54	3.74	
D/E	47.50 BASIC			
D1/E1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

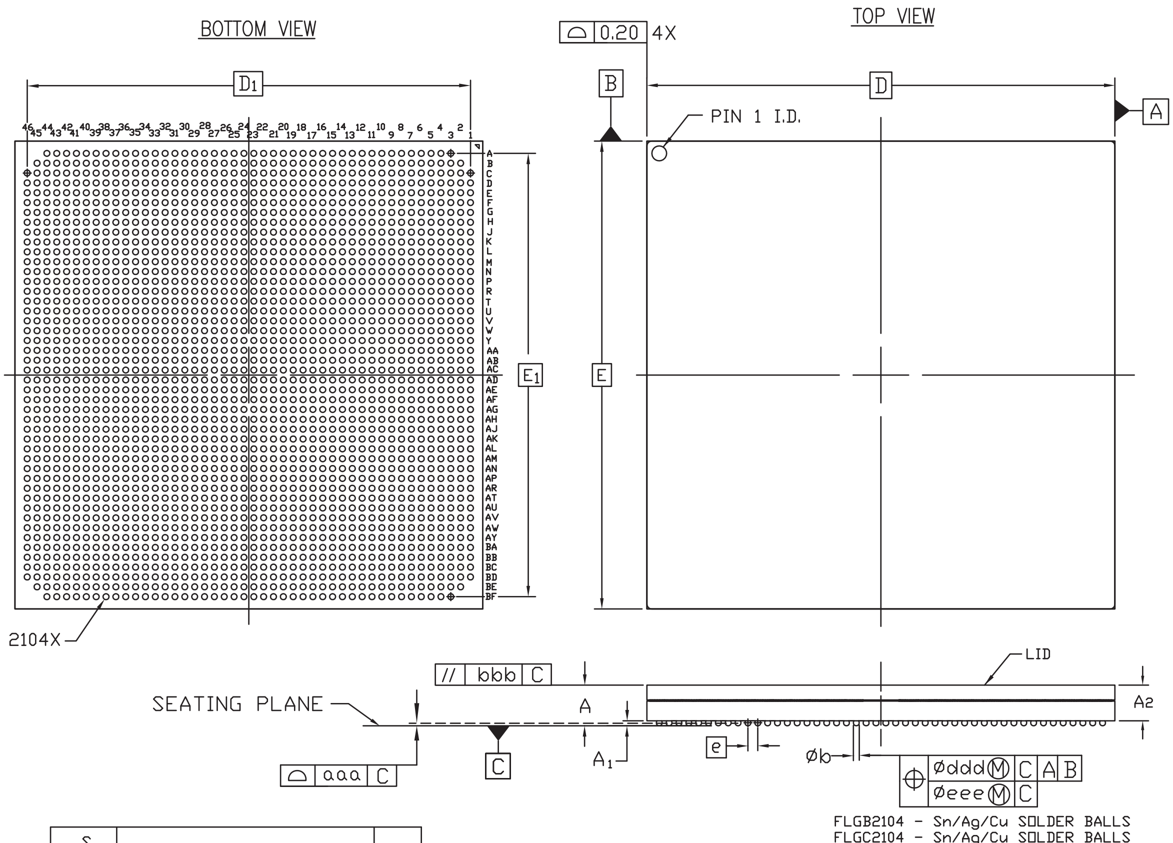
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_flga2104_040217

Figure 4-48: **Package Dimensions for FLGA2104 (XCVU9P)**

FLGB2104 (XCVU160 and XCVU190) and FLGC2104 (XCVU160 and XCVU190) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.92	4.12	4.32	
A_1	0.40	0.50	0.60	
A_2	3.42	3.62	3.82	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

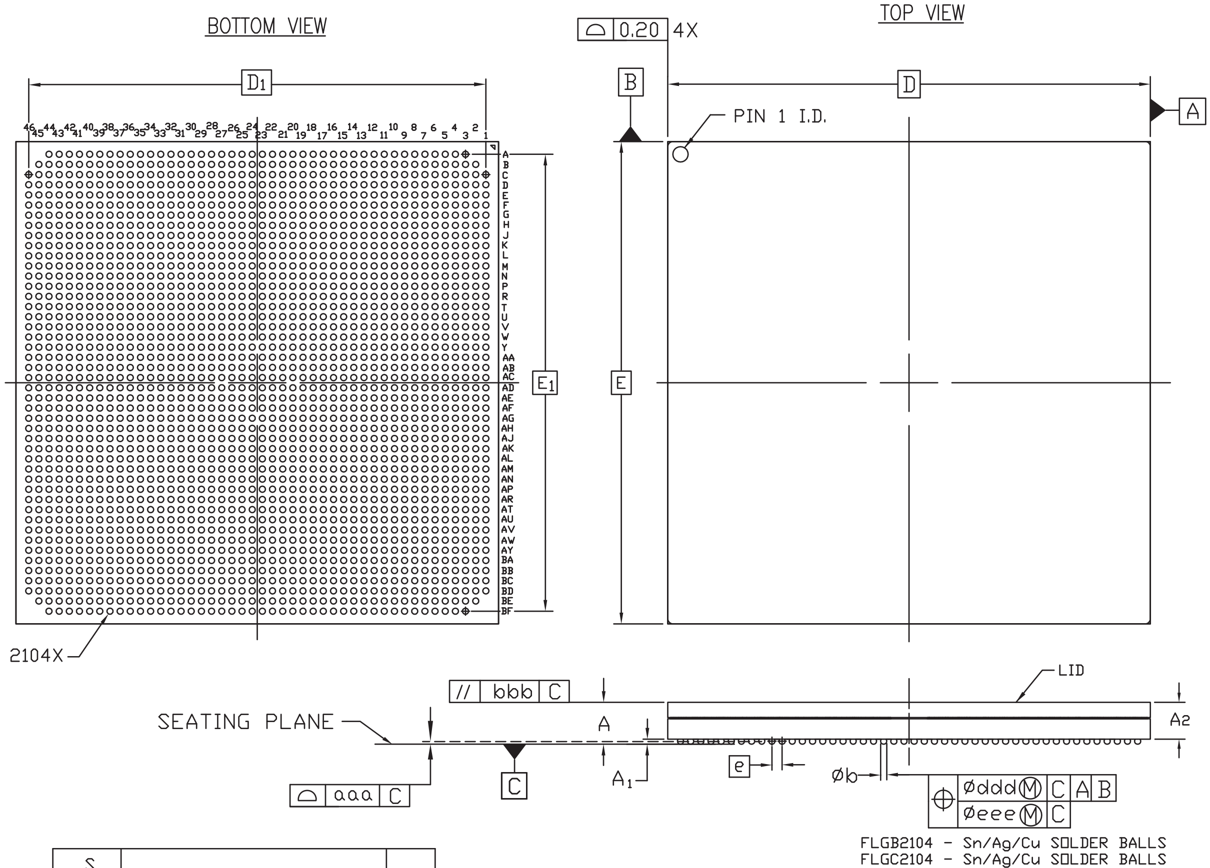
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAY-2 (DEPOPULATED)

ug575_c4_115_120215

Figure 4-49: **Package Dimensions for FLGB2104 (XCVU160 and XCVU190) and FLGC2104 (XCVU160 and XCVU190)**

FLGB2104 (XCVU9P and XCVU11P) and FLGC2104 (XCVU11P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.92	4.12	4.32	
A_1	0.40	0.50	0.60	
A_2	3.42	3.62	3.82	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

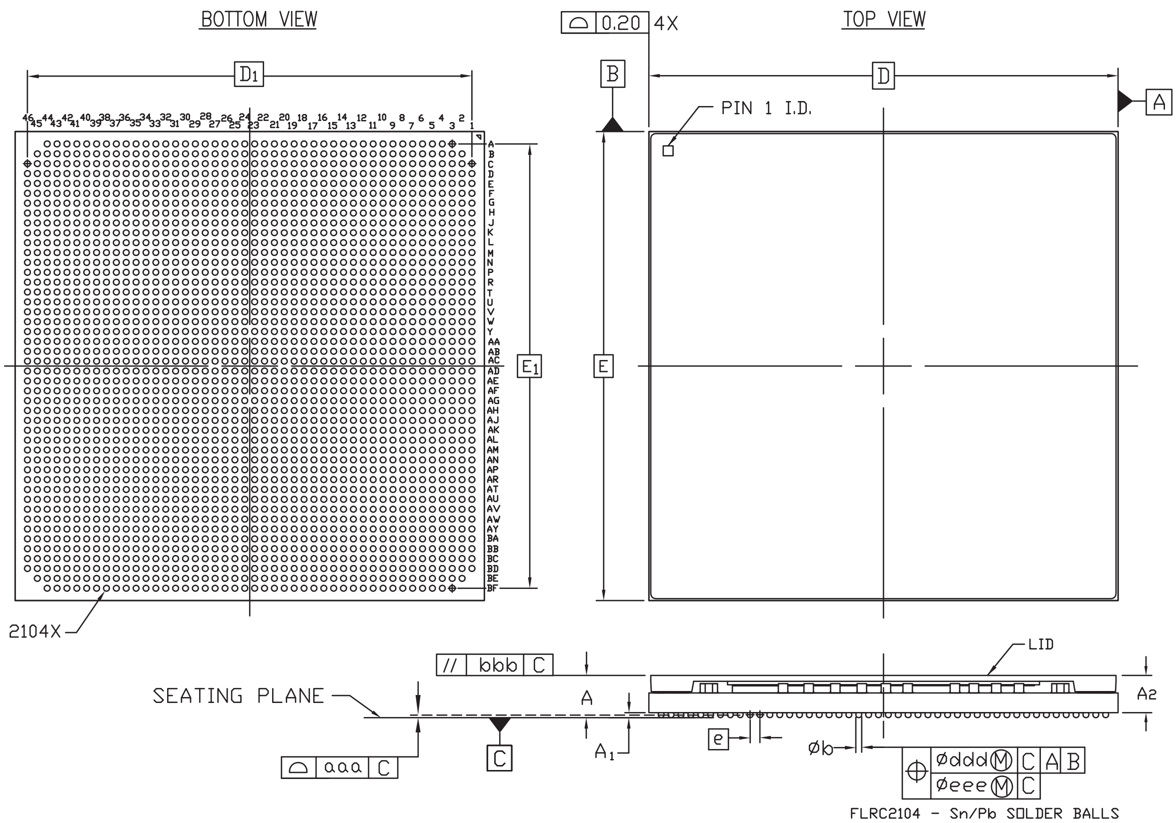
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_flgb_vu9p_vu11p_040417

Figure 4-50: **Package Dimensions for FLGB2104 (XCVU9P and XCVU11P) and FLGC2104 (XCVU11P)**

FLRC2104 (XQVU11P) Ruggedized Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.07	4.27	4.47	
A_1	0.40	0.50	0.60	
A_2	3.57	3.77	3.97	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

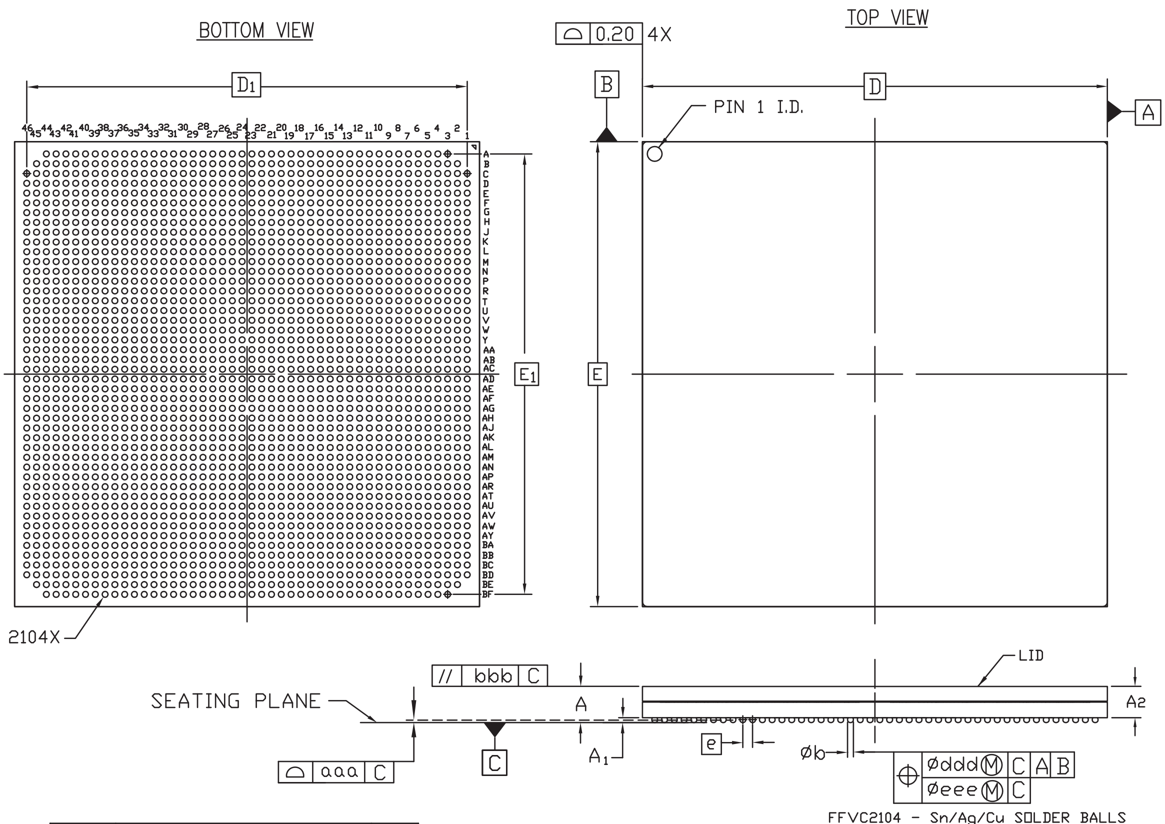
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAY-2 (DEPOPULATED)

ug575_c4_flrc2104_010819

Figure 4-51: **Package Dimensions for FLRC2104 (XQVU11P)**

FFVC2104 (XCVU095) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.64	3.84	4.04	
A_1	0.40	0.50	0.60	
A_2	3.14	3.34	3.54	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.20	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

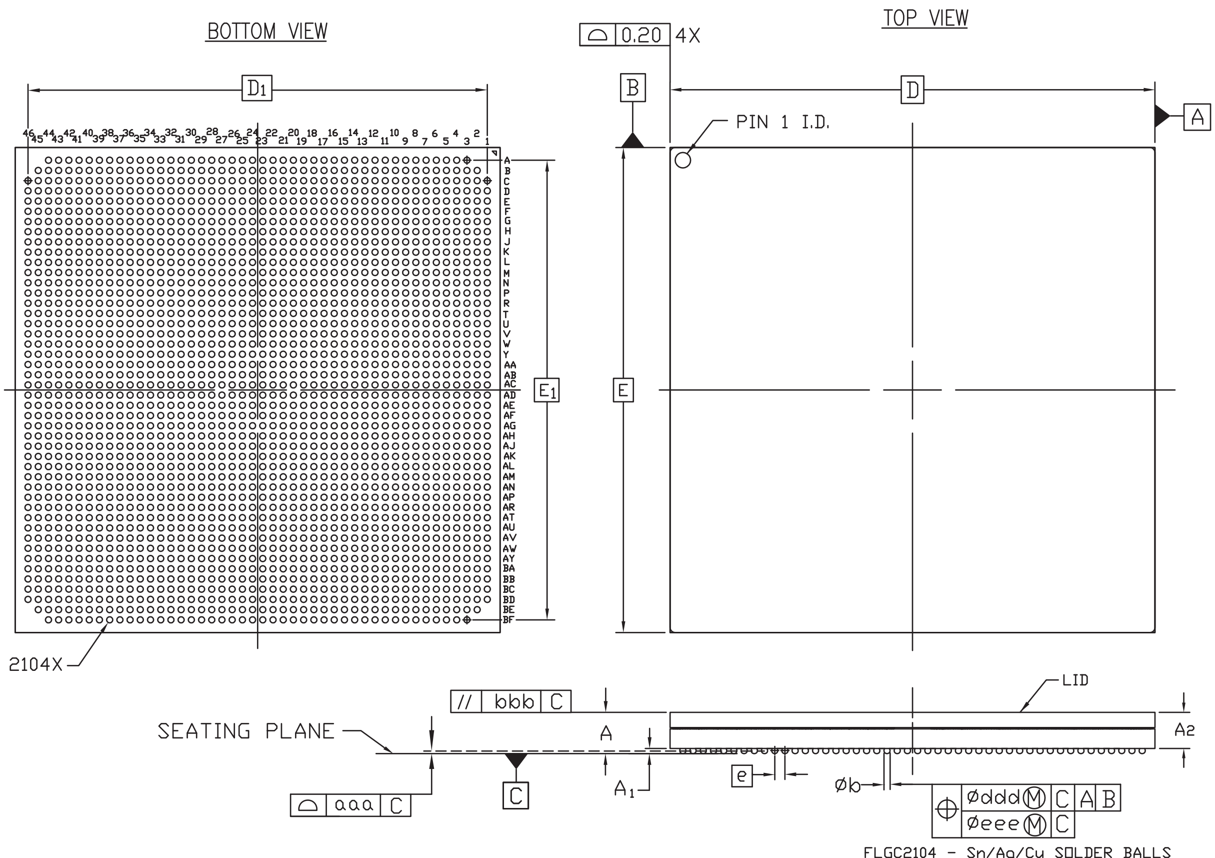
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAY-2 (DEPOPULATED)

ug575_c4_18_041716

Figure 4-52: **Package Dimensions for FFVC2104 (XCVU095)**

FLGC2104 (XCVU9P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.84	4.04	4.24	
A_1	0.40	0.50	0.60	
A_2	3.34	3.54	3.74	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

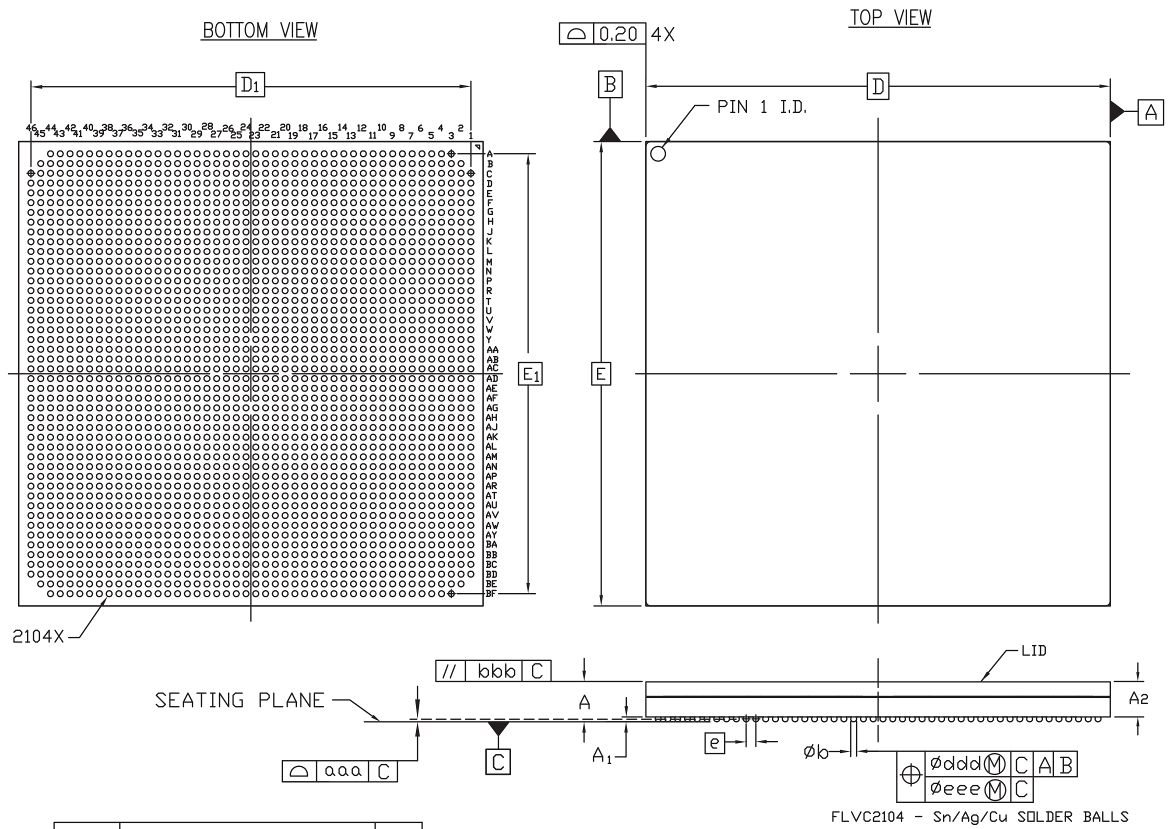
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_flgc_vu9p_040417

Figure 4-53: **Package Dimensions for FLGC2104 (XCVU9P)**

FLVC2104 (XCVU125) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.89	4.09	4.29	
A_1	0.40	0.50	0.60	
A_2	3.39	3.59	3.79	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

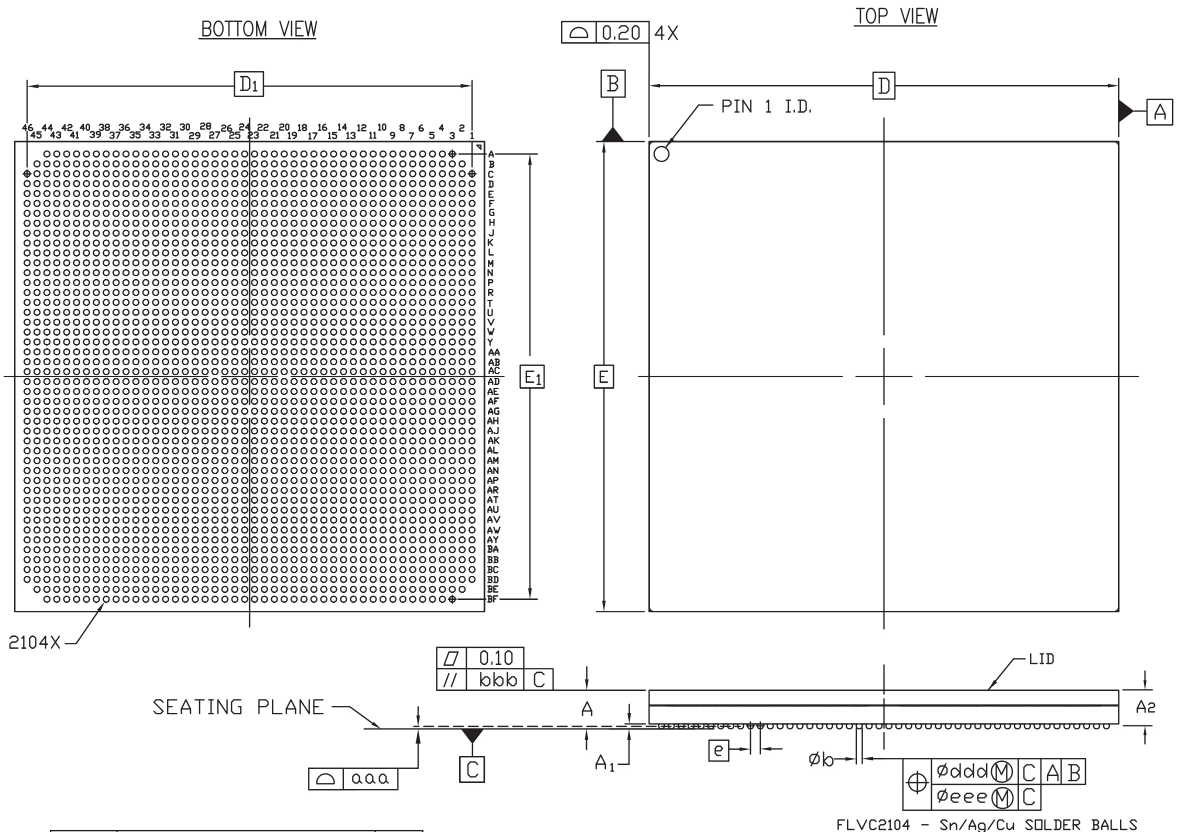
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_117_041615

Figure 4-54: **Package Dimensions for FLVC2104 (XCVU125)**

FLVC2104 (XCVU5P and XCVU7P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.71	3.91	4.11	
A_1	0.40	0.50	0.60	
A_2	3.21	3.41	3.61	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

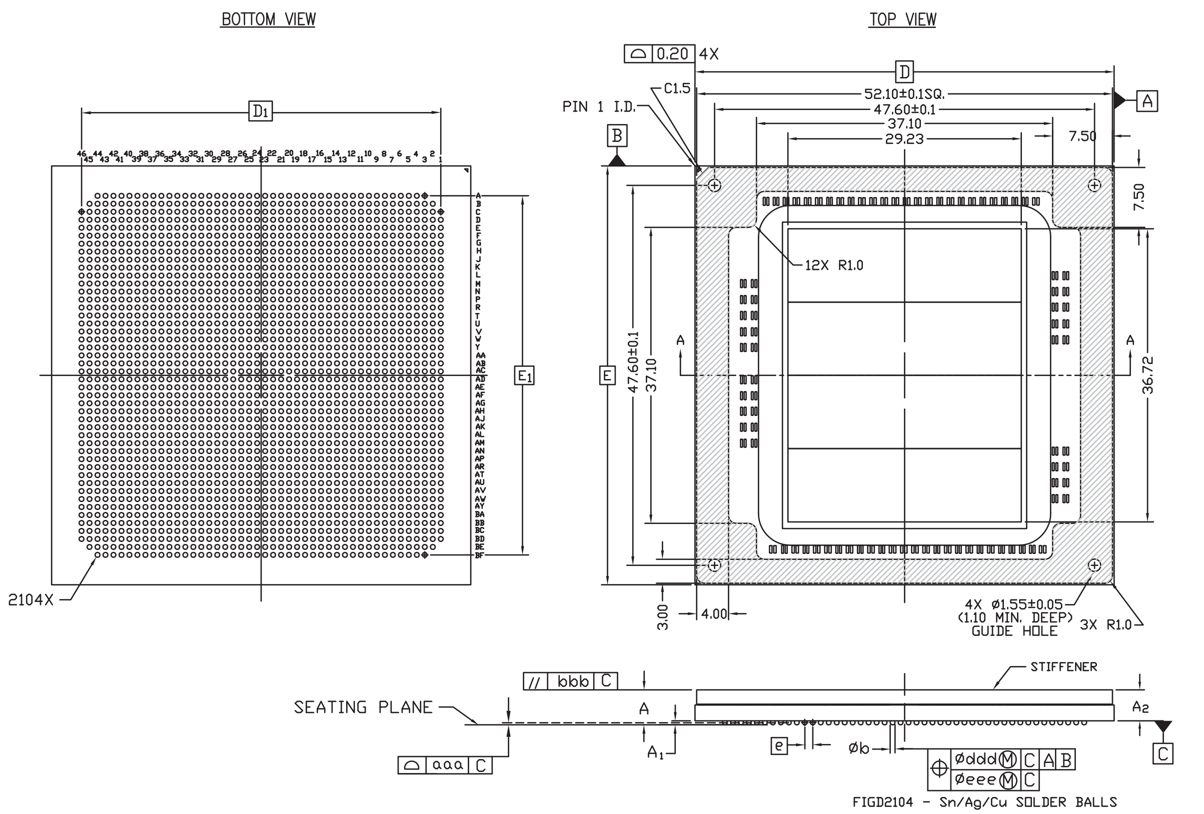
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS−034 AAY−2 (DEPOPULATED)
4. APPLIES TO DEVICE VU7P PACKAGE

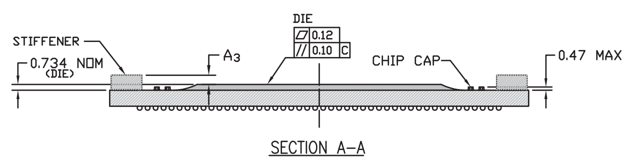
ug575_c4_flvc2104_vu5p_vu7p_041917

Figure 4-55: **Package Dimensions for FLVC2104 (XCVU5P and XCVU7P)**

FIGD2104 (XCVU13P, XCVU27P, and XCVU29P) Flip-Chip, Fine-Pitch, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.19	4.39	4.59	
A1	0.40	0.50	0.60	
A2	3.69	3.89	4.09	
A3	1.06	1.16	1.26	
D/E	52.50 BASIC			
D1/E1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2



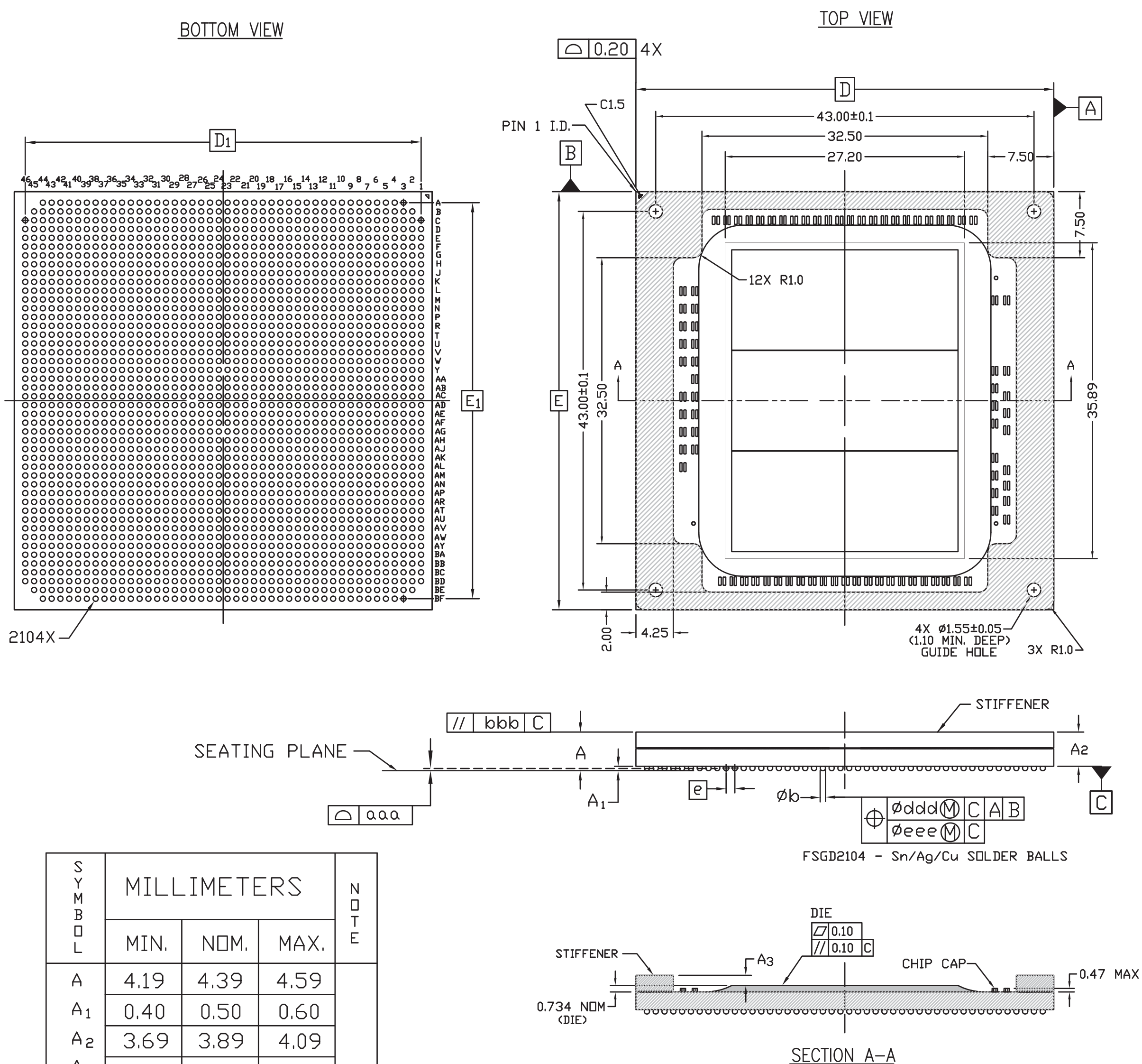
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-ABF-2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_vu13P_figd2104_102517

Figure 4-56: **Package Dimensions for FIGD2104 (XCVU13P, XCVU27P, and XCVU29P)**

FSGD2104 (XCVU9P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA



SYMBOL	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.	NOTE
A	4.19	4.39	4.59	
A_1	0.40	0.50	0.60	
A_2	3.69	3.89	4.09	
A_3	1.06	1.16	1.26	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	46			2

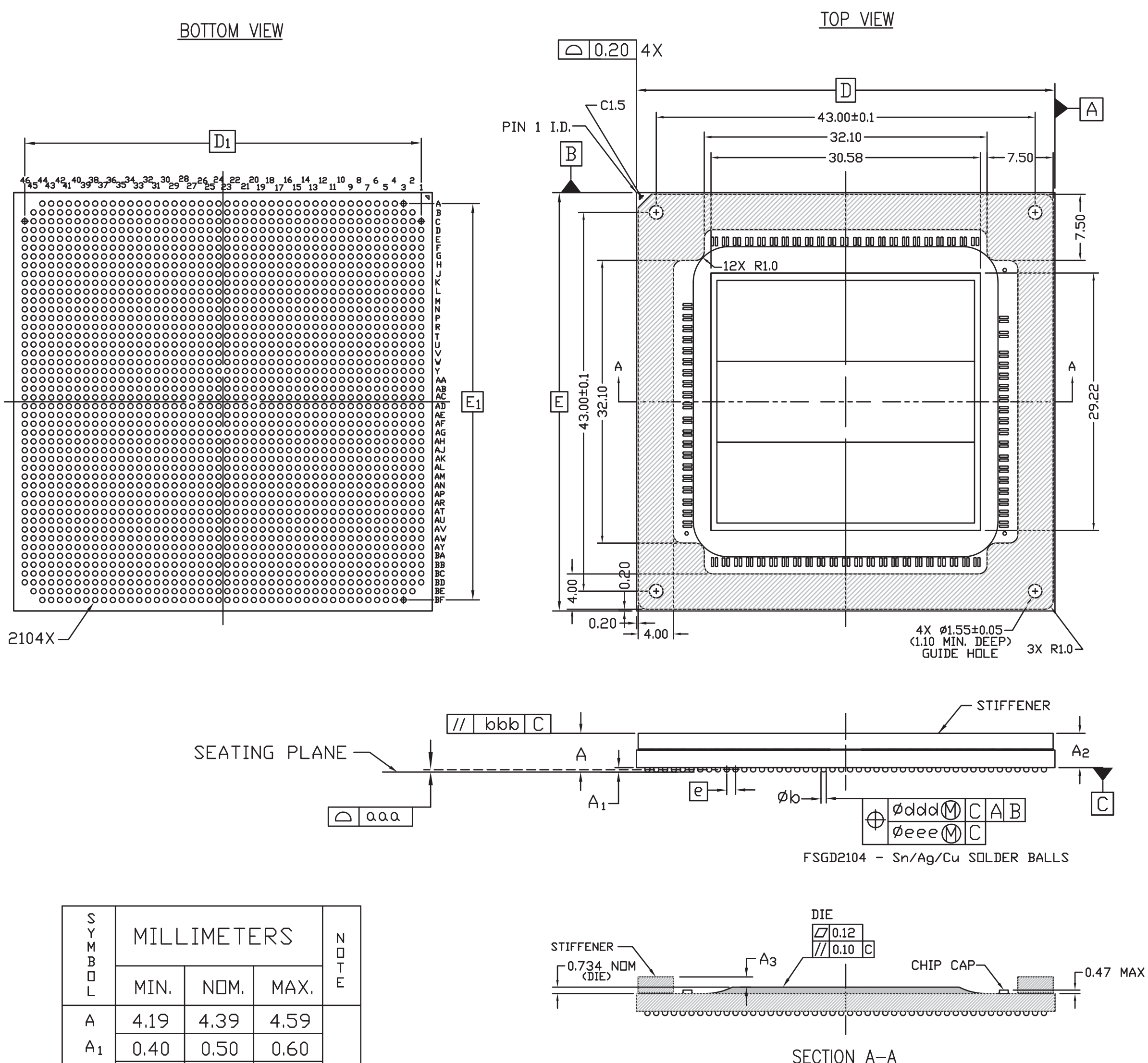
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_vu9P_fsgd2104_100717

Figure 4-57: **Package Dimensions for FSGD2104 (XCVU9P)**

FSGD2104 (XCVU11P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.19	4.39	4.59	
A_1	0.40	0.50	0.60	
A_2	3.69	3.89	4.09	
A_3	1.06	1.16	1.26	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	46			2

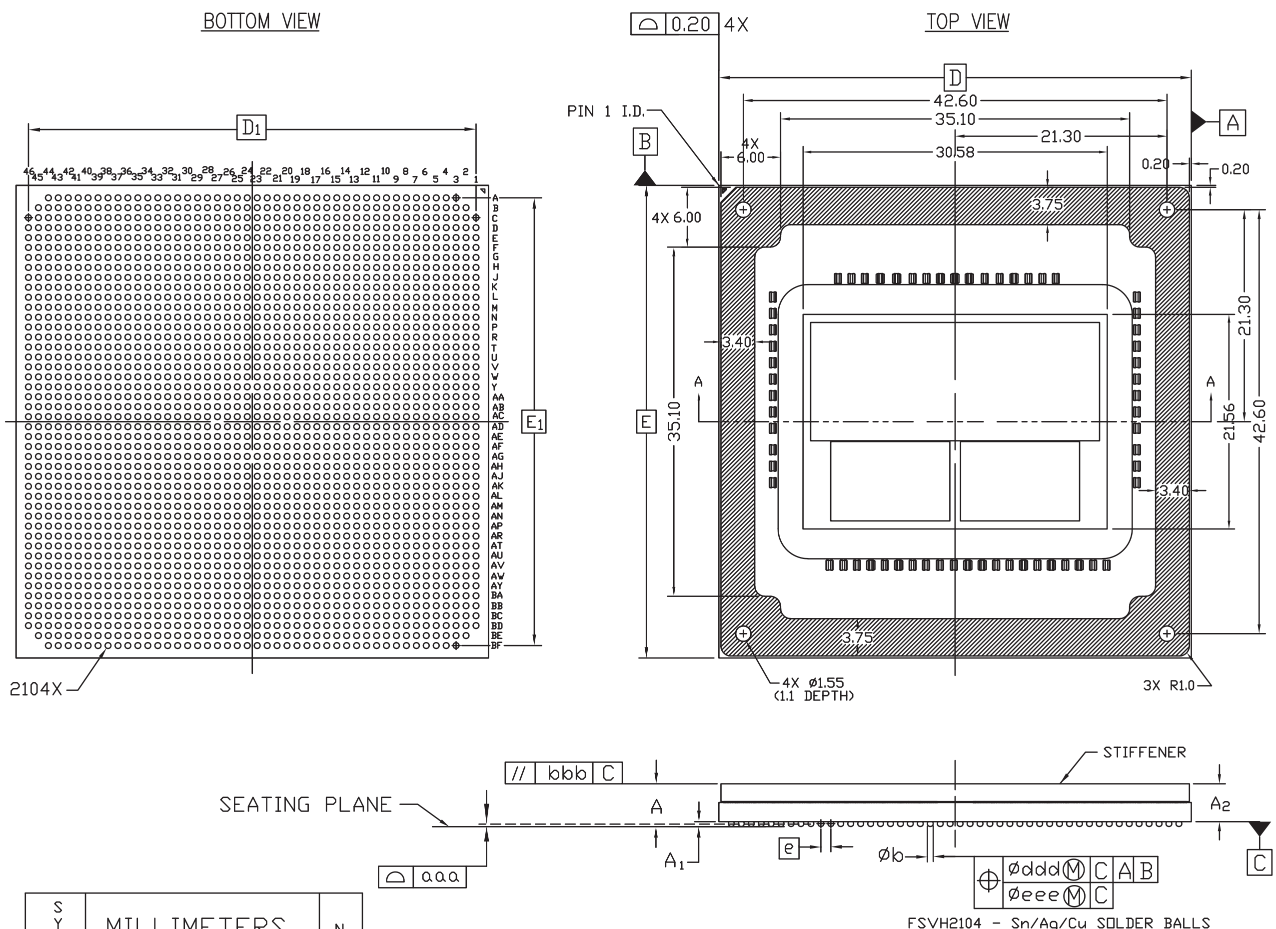
NOTES:

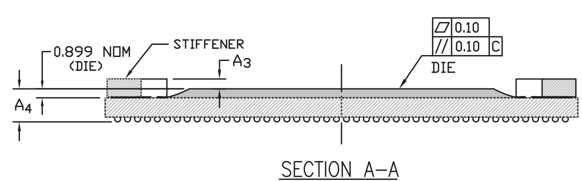
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

ug575_c4_vu11P_fsgd2104_102517

Figure 4-58: **Package Dimensions for FSGD2104 (XCVU11P)**

FSVH2104 (XCVU33P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA





SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.11	4.31	4.51	
A_1	0.40	0.50	0.60	
A_2	3.61	3.81	4.01	
A_3	0.89	0.99	1.09	
A_4	3.22	3.32	3.42	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	46			2

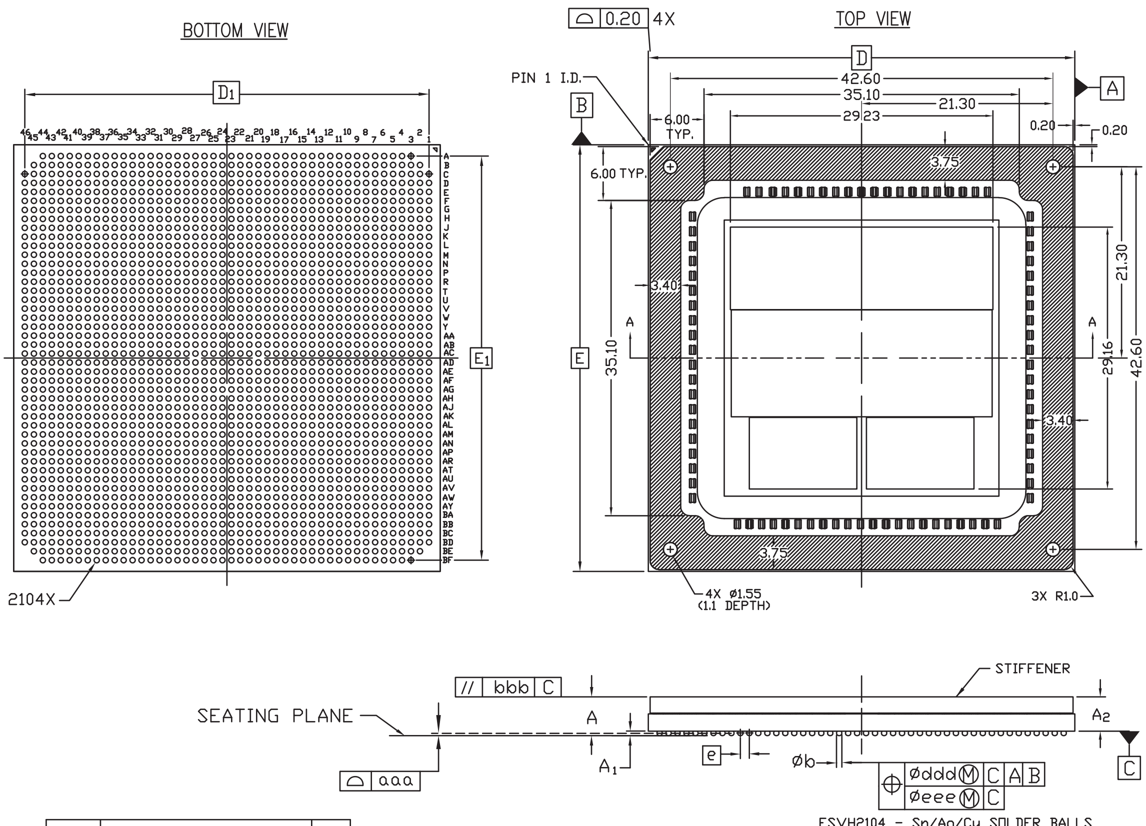
NOTES:

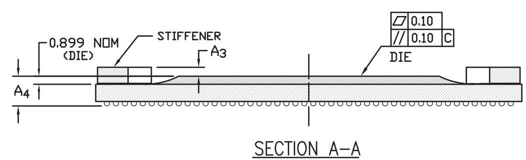
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034 AAY-2 (DEPOPULATED)

ug575_fsvh2104_vu33p_122120

Figure 4-59: **Package Dimensions for FSVH2104 (XCVU33P)**

FSVH2104 (XCVU35P and XCVU45P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA





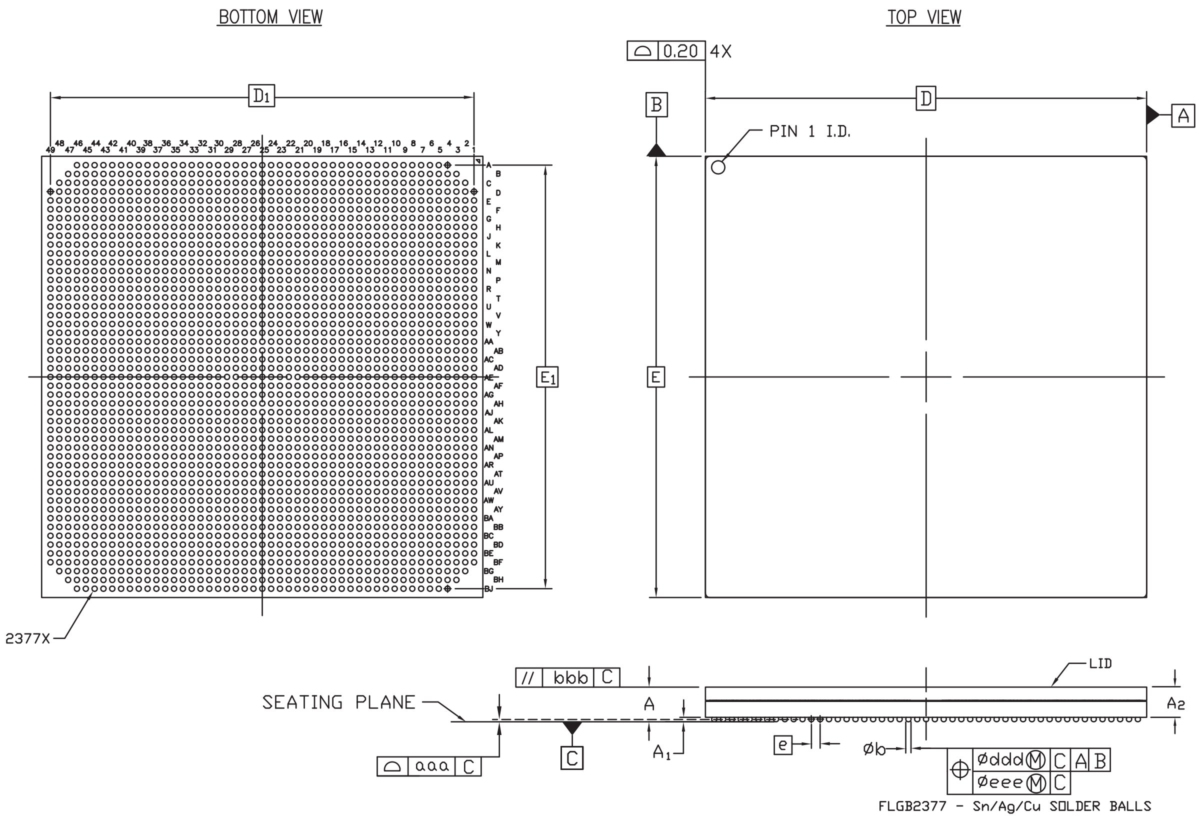
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.11	4.31	4.51	
A_1	0.40	0.50	0.60	
A_2	3.61	3.81	4.01	
A_3	0.89	0.99	1.09	
A_4	3.22	3.32	3.42	
D/E	47.50 BASIC			
D_1/E_1	45.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	46			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034 AAY–2 (DEPOPULATED)

Figure 4-60: **Package Dimensions for FSVH2104 (XCVU35P and XCVU45P)**

FLGB2377 Flip-Chip, Fine-Pitch, BGA (XCVU440)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.73	3.93	4.13	
A_1	0.40	0.50	0.60	
A_2	3.23	3.43	3.63	
D/E	50.00 BASIC			
D_1/E_1	48.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	--	--	0.30	
bbb	--	--	0.25	
ddd	--	--	0.25	
eee	--	--	0.10	
M	49			2

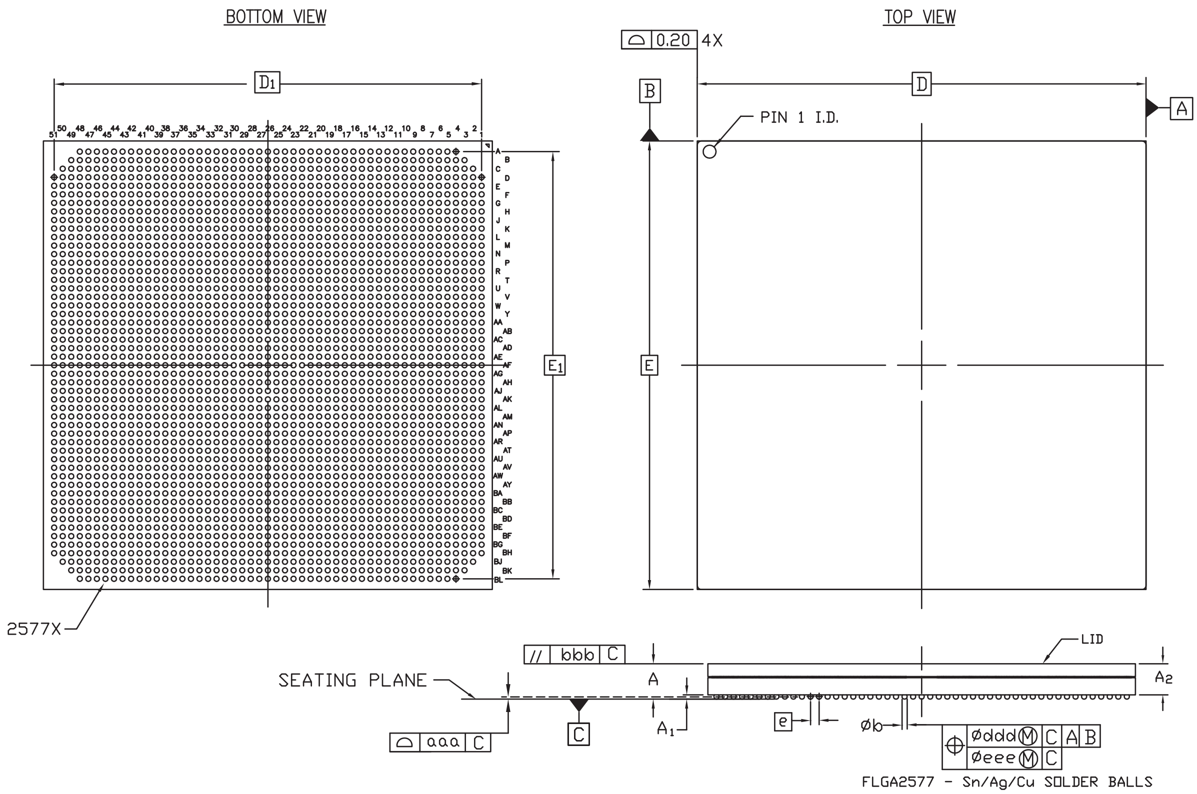
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC REFERENCE MS-034-ABA-1 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_12_100615

Figure 4-61: **Package Dimensions for FLGB2377 (XCVU440)**

FLGA2577 Flip-Chip, Fine-Pitch, BGA (XCVU190)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.91	4.11	4.31	
A_1	0.40	0.50	0.60	
A_2	3.41	3.61	3.81	
D/E	52.50 BASIC			
D_1/E_1	50.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	51			2

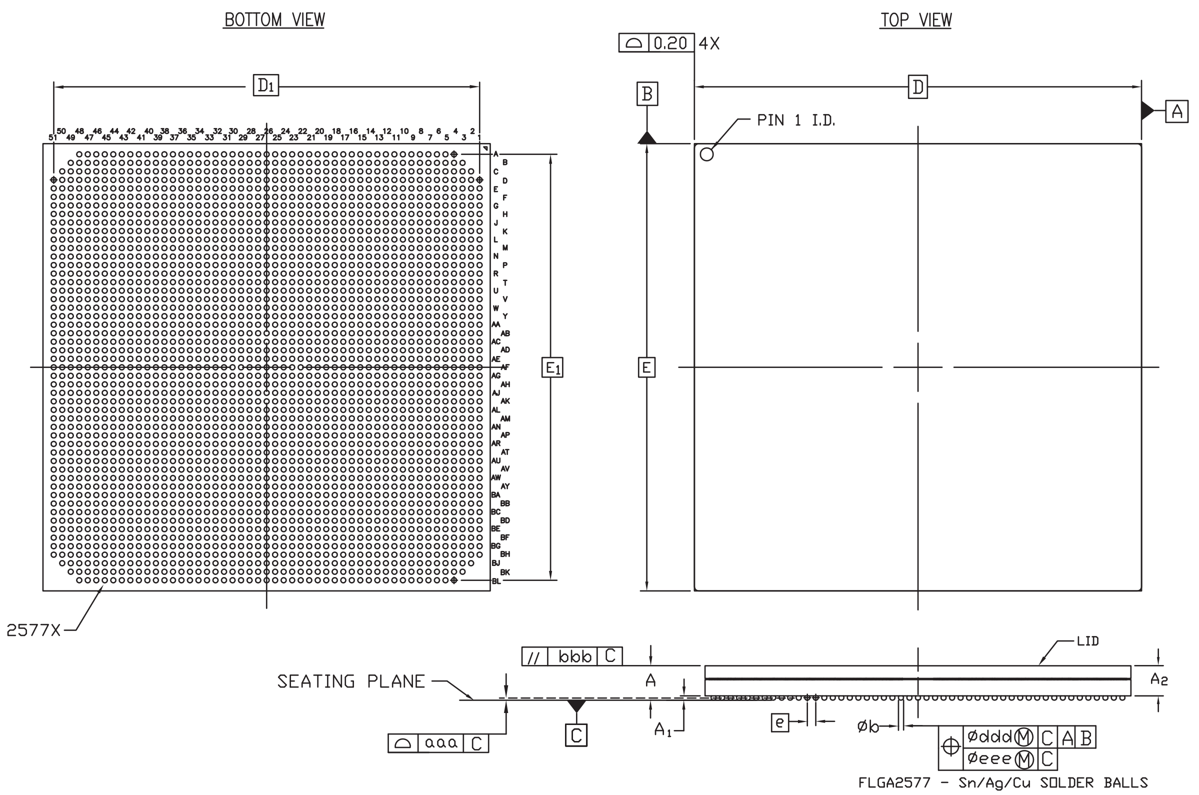
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M−1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS−034−ABF−2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_13_101215

Figure 4-62: **Package Dimensions for FLGA2577 (XCVU190)**

FLGA2577 Flip-Chip, Fine-Pitch, BGA (XCVU9P and XCVU13P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.84	4.04	4.24	
A_1	0.40	0.50	0.60	
A_2	3.34	3.54	3.74	
D/E	52.50 BASIC			
D_1/E_1	50.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	-	-	0.30	
bbb	-	-	0.25	
ddd	-	-	0.25	
eee	-	-	0.10	
M	51			2

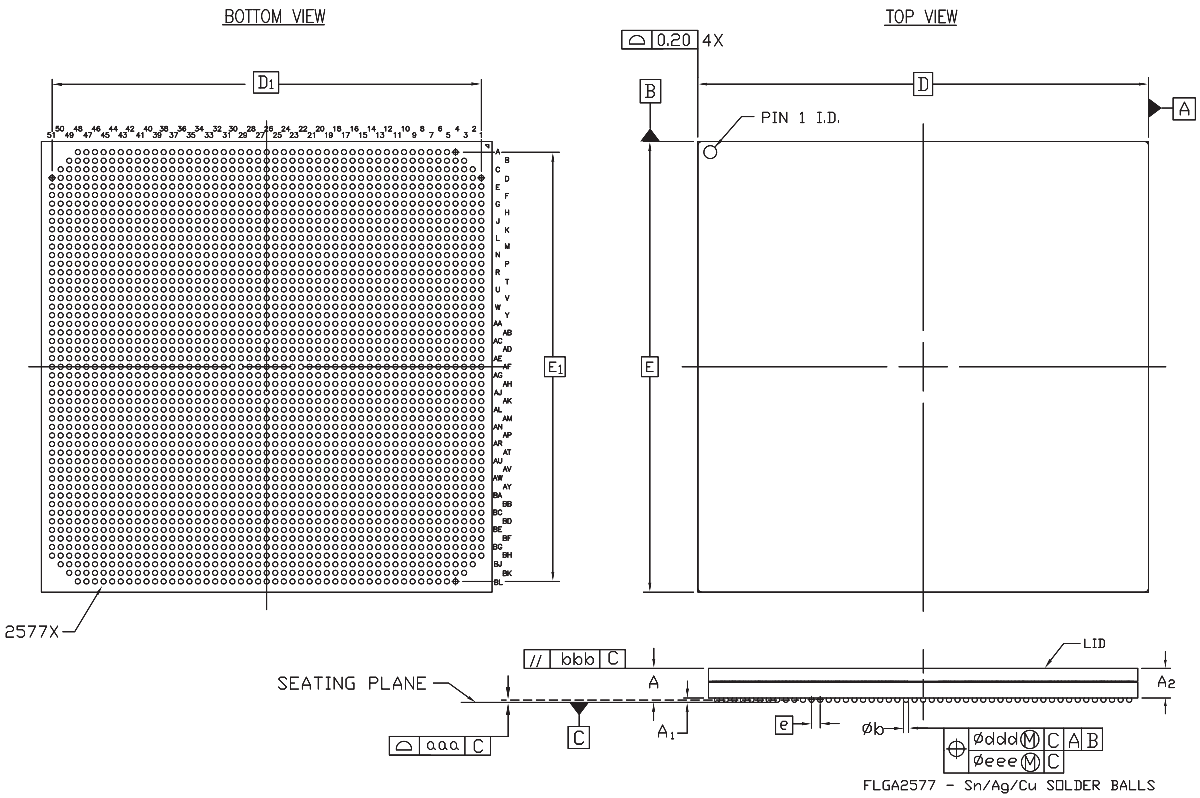
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-ABF-2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"
4. THS PACKAGE APPLIES TO UltraScale+ XCVU9P & XCVU13P DEVICES

ug575_c4_flga2577_040217

Figure 4-63: **Package Dimensions for FLGA2577 (XCVU9P and XCVU13P)**

FLGA2577 Flip-Chip, Fine-Pitch, BGA (XCVU11P)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.74	3.94	4.14	
A_1	0.40	0.50	0.60	
A_2	3.24	3.44	3.64	
D/E	52.50 BASIC			
D_1/E_1	50.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	-	-	0.30	
bbb	-	-	0.25	
ddd	-	-	0.25	
eee	-	-	0.10	
M	51			2

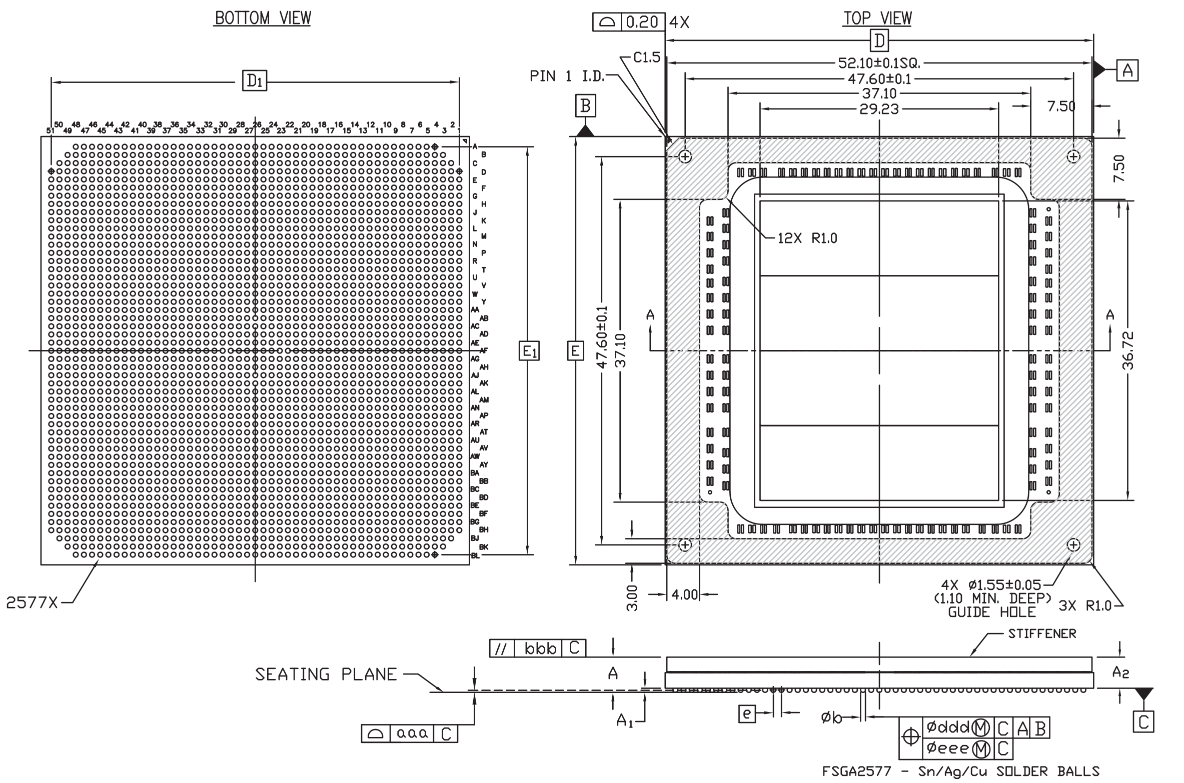
NOTES:

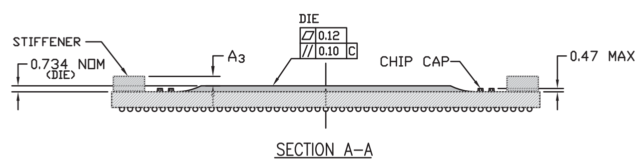
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–ABF–2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_flga2577_vu11p_040217

Figure 4-64: **Package Dimensions for FLGA2577 (XCVU11P)**

FSGA2577 Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA (XCVU13P, XCVU27P, and XCVU29P)





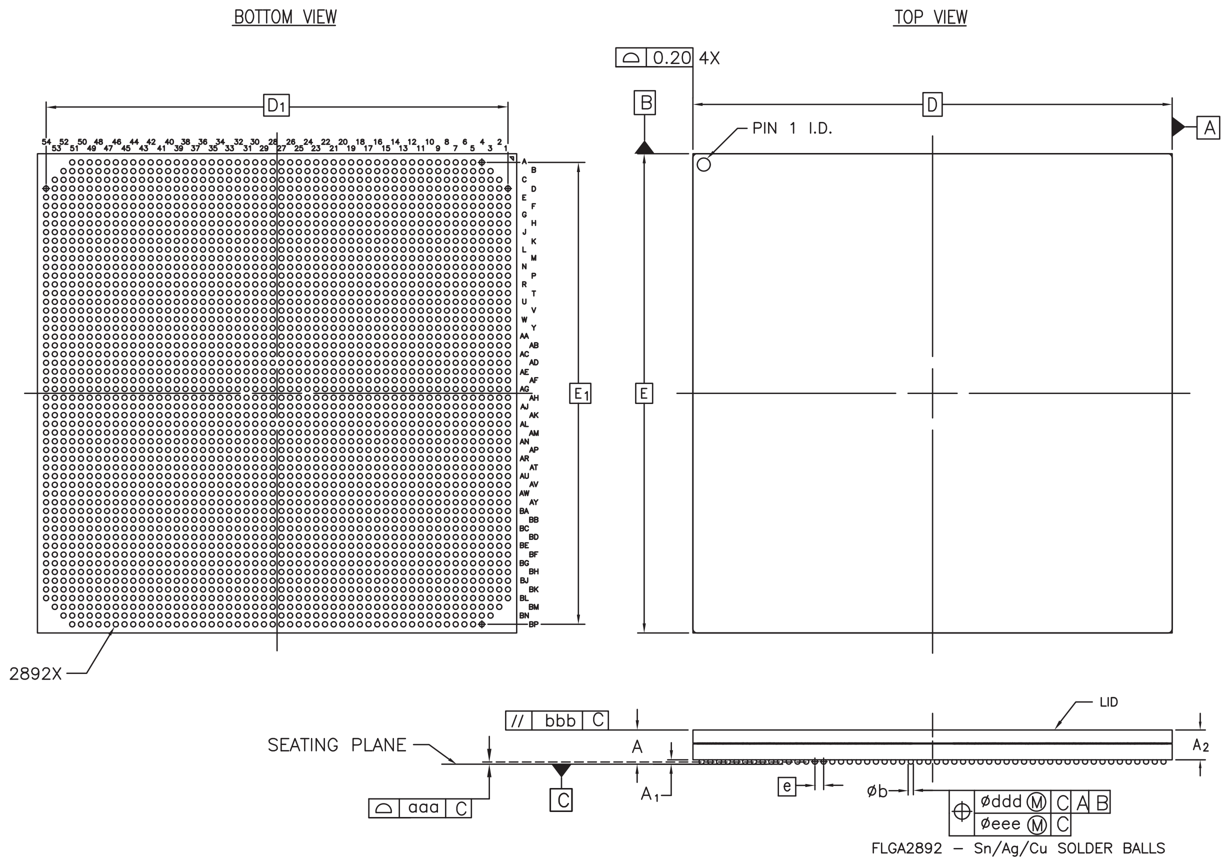
SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.11	4.31	4.51	
A_1	0.40	0.50	0.60	
A_2	3.61	3.81	4.01	
A_3	1.06	1.16	1.26	
D/E	52.50 BASIC			
D1/E1	50.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	-	-	0.30	
bbb	-	-	0.25	
ddd	-	-	0.25	
eee	-	-	0.10	
M	51			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-ABF-2 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

Figure 4-65: **Package Dimensions for FSGA2577 (XCVU13P, XCVU27P, and XCVU29P)**

FLGA2892 Flip-Chip, Fine-Pitch, BGA (XCVU440)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.73	3.93	4.13	
A_1	0.40	0.50	0.60	
A_2	3.23	3.43	3.63	
D/E		55.00 BASIC		
D_1/E_1		53.00 BASIC		
e		1.00 BASIC		
øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M		54		2

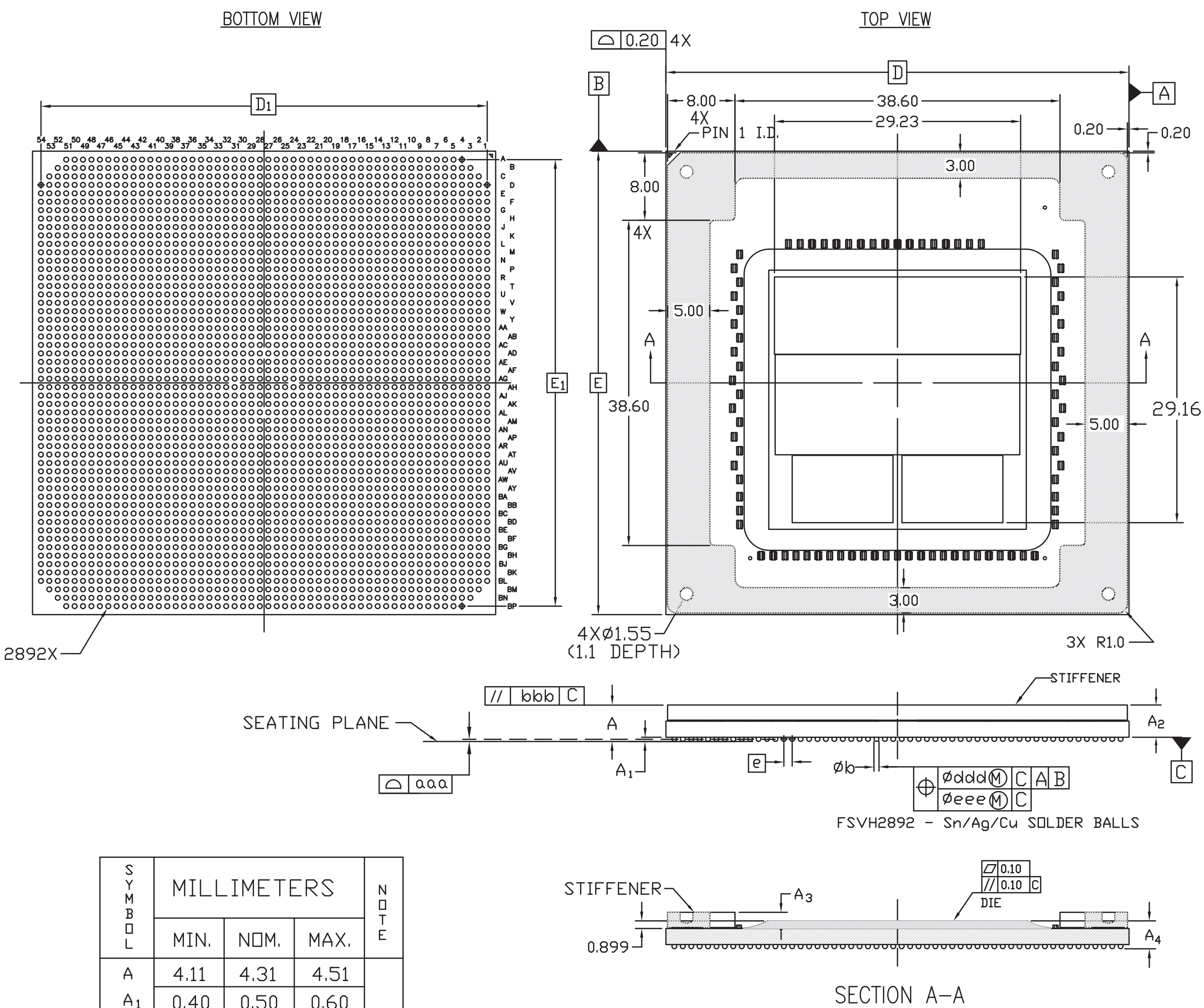
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC MS–034 ABG–1 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_c4_14_100615

Figure 4-66: **Package Dimensions for FLGA2892 (XCVU440)**

FSVH2892 (XCVU35P and XCVU45P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.11	4.31	4.51	
A_1	0.40	0.50	0.60	
A_2	3.61	3.81	4.01	
A_3	0.89	0.99	1.09	
A_4	3.22	3.32	3.42	
D/E	55.00 BASIC			
D_1/E_1	53.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	54			2

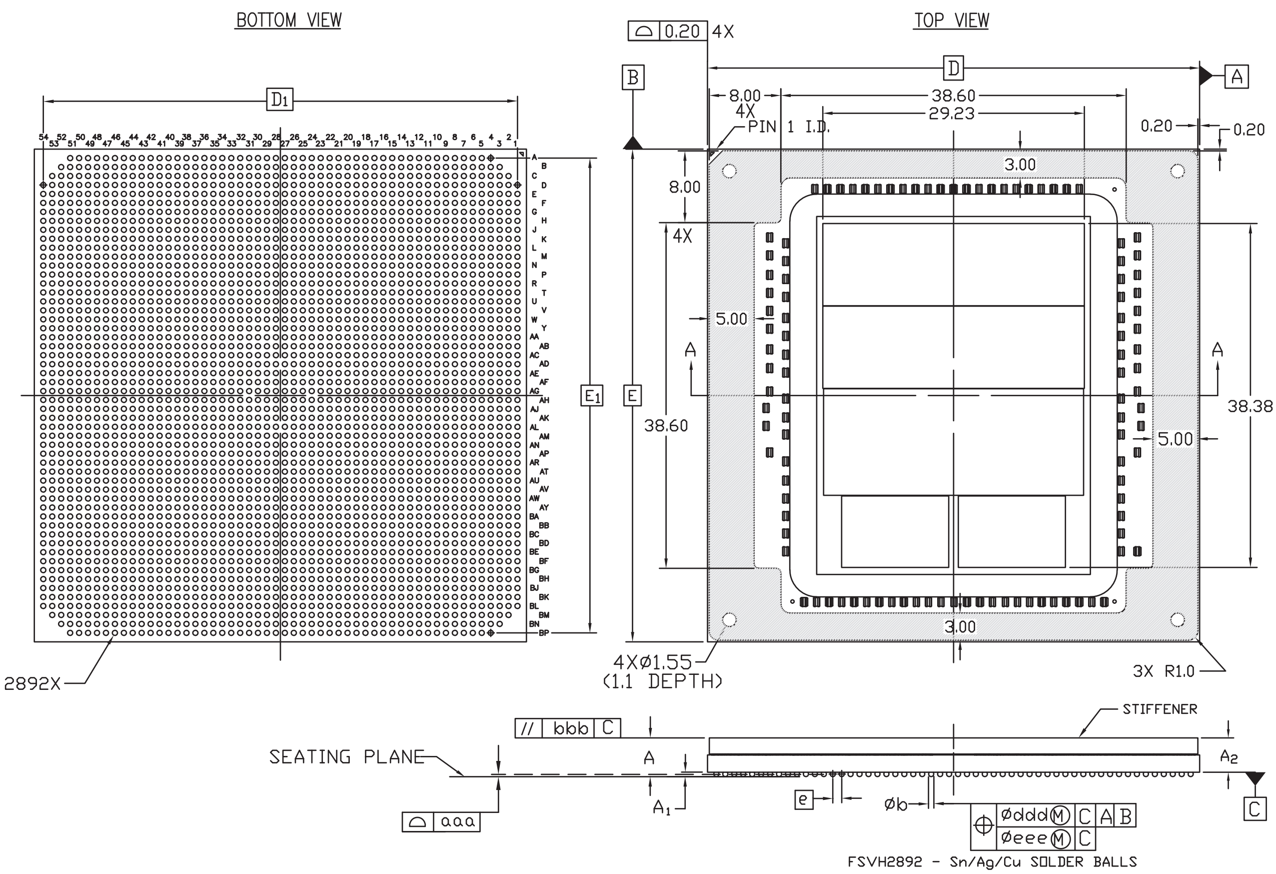
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC MS–034 ABG–1 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

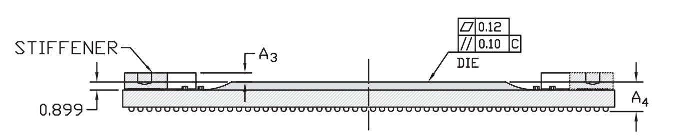
ug575_fsvh2892_vu35p_vu45p_122120

Figure 4-67: **Package Dimensions for FSVH2892 (XCVU35P and XCVU45P)**

FSVH2892 (XCVU37P and XCVU47P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	4.11	4.31	4.51	
A_1	0.40	0.50	0.60	
A_2	3.61	3.81	4.01	
A_3	0.89	0.99	1.09	
A_4	3.22	3.32	3.42	
D/E	55.00 BASIC			
D_1/E_1	53.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa	—	—	0.30	
bbb	—	—	0.25	
ddd	—	—	0.25	
eee	—	—	0.10	
M	54			2



SECTION A–A

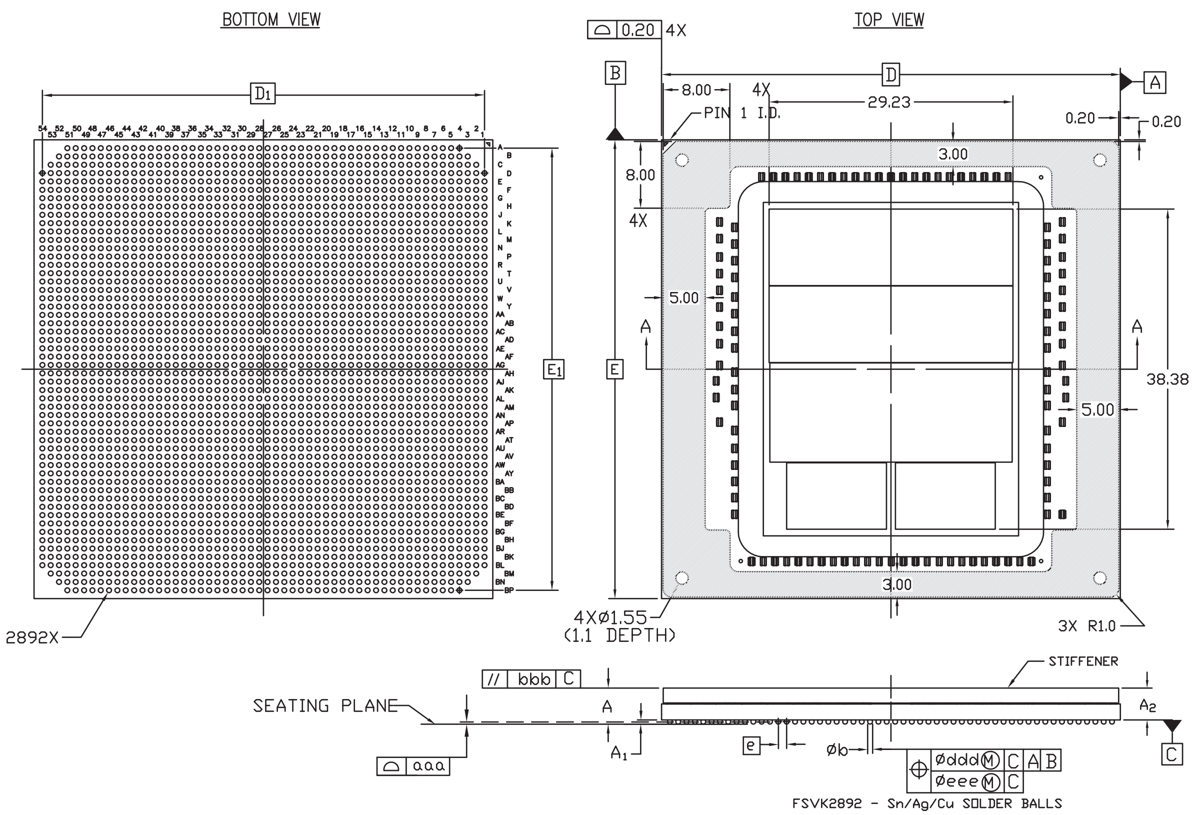
NOTES:

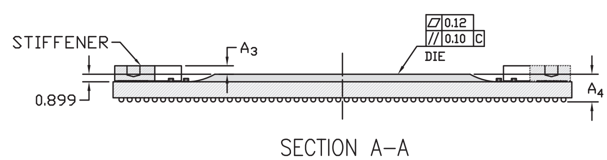
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC MS–034 ABG–1 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

ug575_fsvh2892_vu37p_vu47p_122120

Figure 4-68: **Package Dimensions for FSVH2892 (XCVU37P and XCVU47P)**

FSVK2892 (XCVU57P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA





SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.11	4.31	4.51	
A1	0.40	0.50	0.60	
A2	3.61	3.81	4.01	
A3	0.89	0.99	1.09	
A4	3.22	3.32	3.42	
D/E	55.00 BASIC			
D1/E1	53.00 BASIC			
e	1.00 BASIC			
Øb	0.50	0.60	0.70	
aaa			0.30	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	54			2

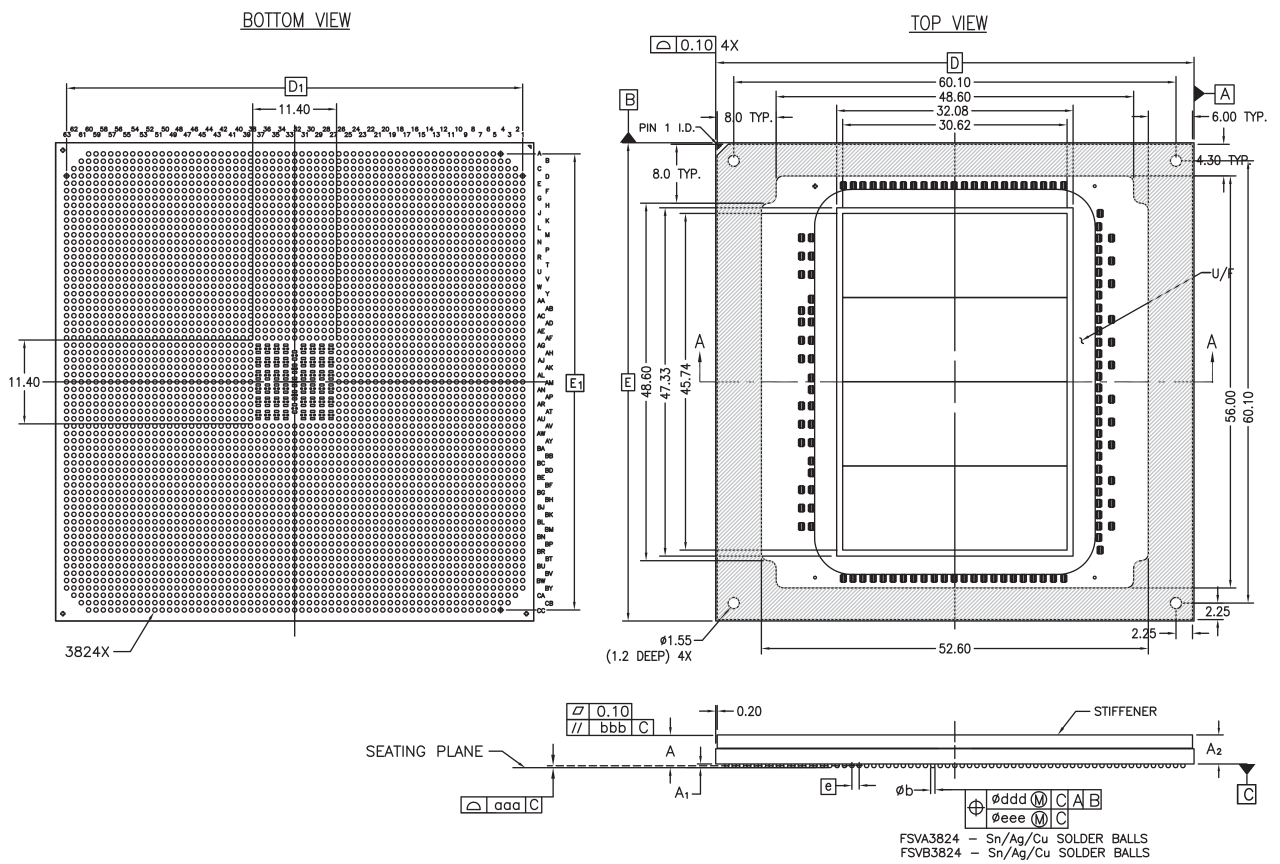
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE
3. CONFORMS TO JEDEC MS-034 ABG-1 (DEPOPULATED) EXCEPT FOR DIMENSION "aaa"

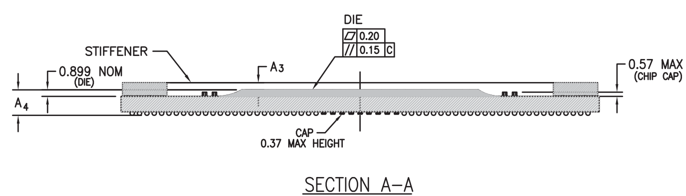
ug575_c4_fsvk2892_083020

Figure 4-69: **Package Dimensions for FSVK2892 (XCVU57P)**

FSVA3824 and FSVB3824 (XCVU19P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	4.24	4.44	4.64	
A_1	0.40	0.50	0.60	
A_2	3.74	3.94	4.14	
A_3	0.86	0.96	1.06	
A_4	3.38	3.48	3.58	
D/E	65.00 BASIC			
D_1/E_1	62.00 BASIC			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.30	
bbb	~	~	0.13	
ddd	~	~	0.25	
eee	~	~	0.10	
M	63			2



NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE

ug575_fsva3824_fsvb3824_vu19p_122120

Figure 4-70: **Package Dimensions for FSVA3824 and FSVB3824 (XCVU19P)**

Package Marking

Introduction

The package top-markings for the AMD UltraScale™ and AMD UltraScale+™ devices are similar to the examples shown in the following figures. Most of these figures show both the old and changed top markings. In addition to the markings explained in Table 5-1, refer to the *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424).

The package top-markings for the AMD Spartan™ UltraScale+, AMD XQ Kintex™ UltraScale+, and AMD XQ Virtex™ UltraScale+ FPGAs are as shown in Figure 5-6. On these devices only the AMD logo and the 2D bar code are marked.

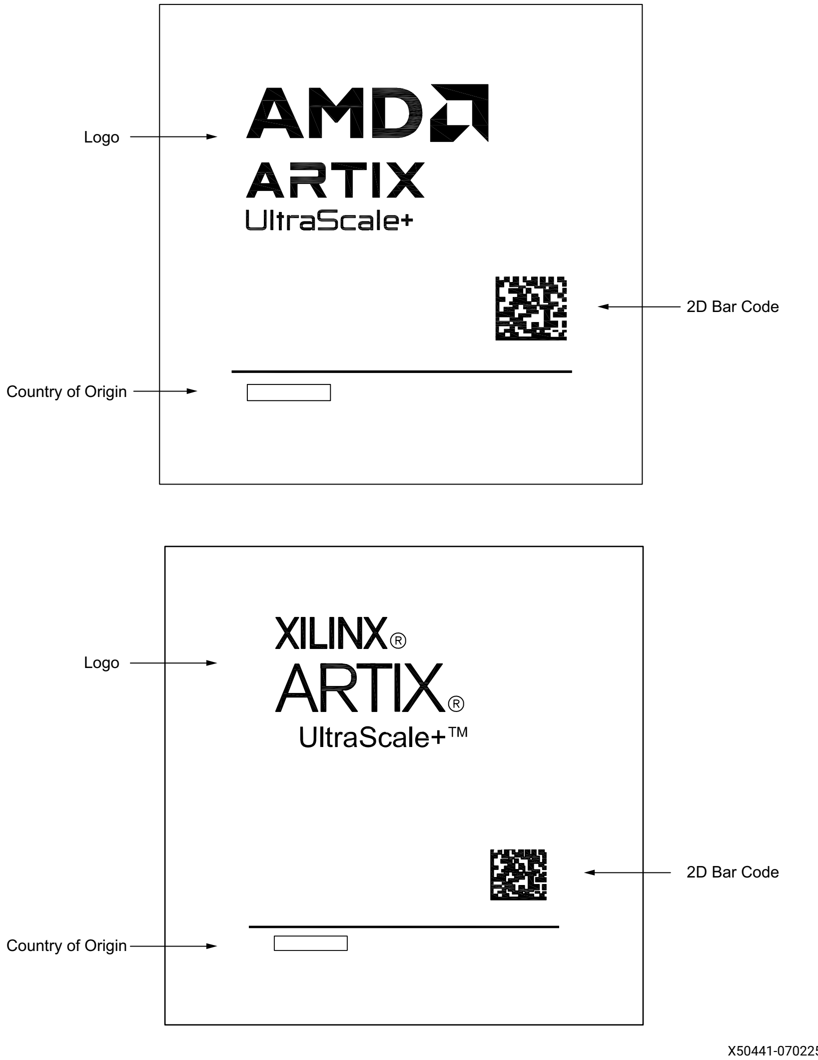


Figure 5-1: **Artix UltraScale+ Device Package Marking**

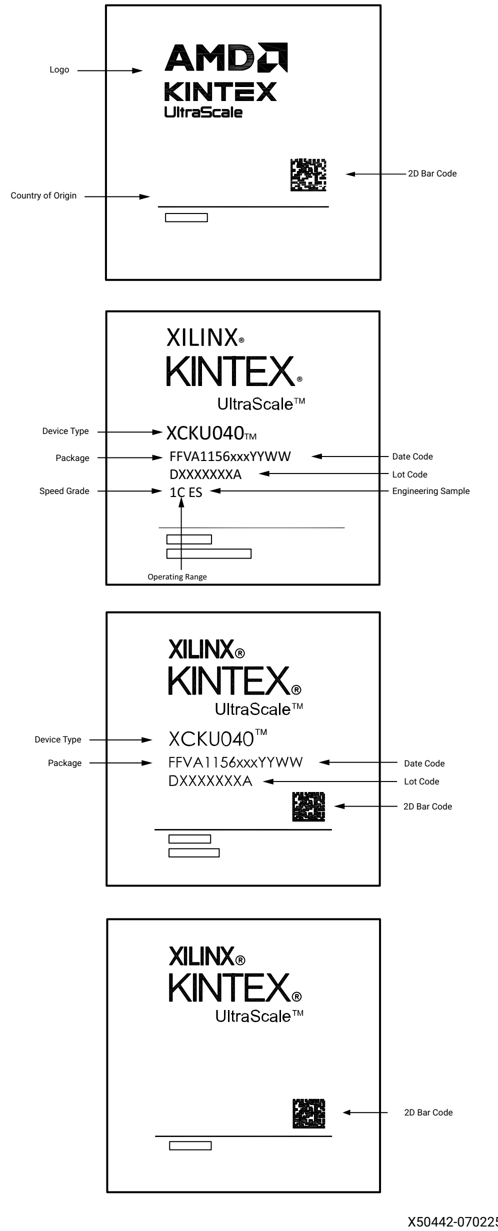


Figure 5-2: **Kintex UltraScale Device Package Marking**

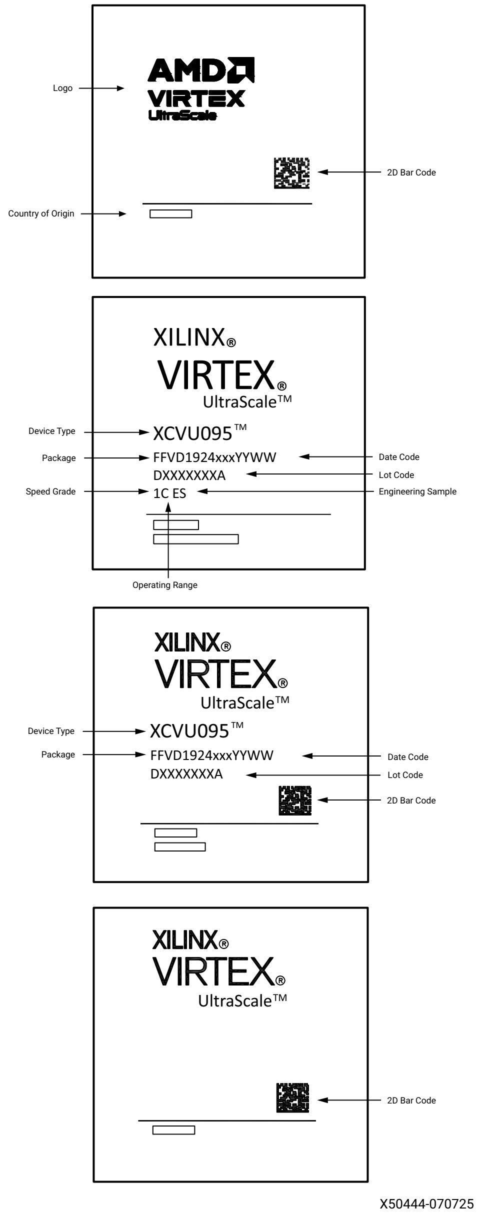


Figure 5-3: **Virtex UltraScale Device Package Marking**

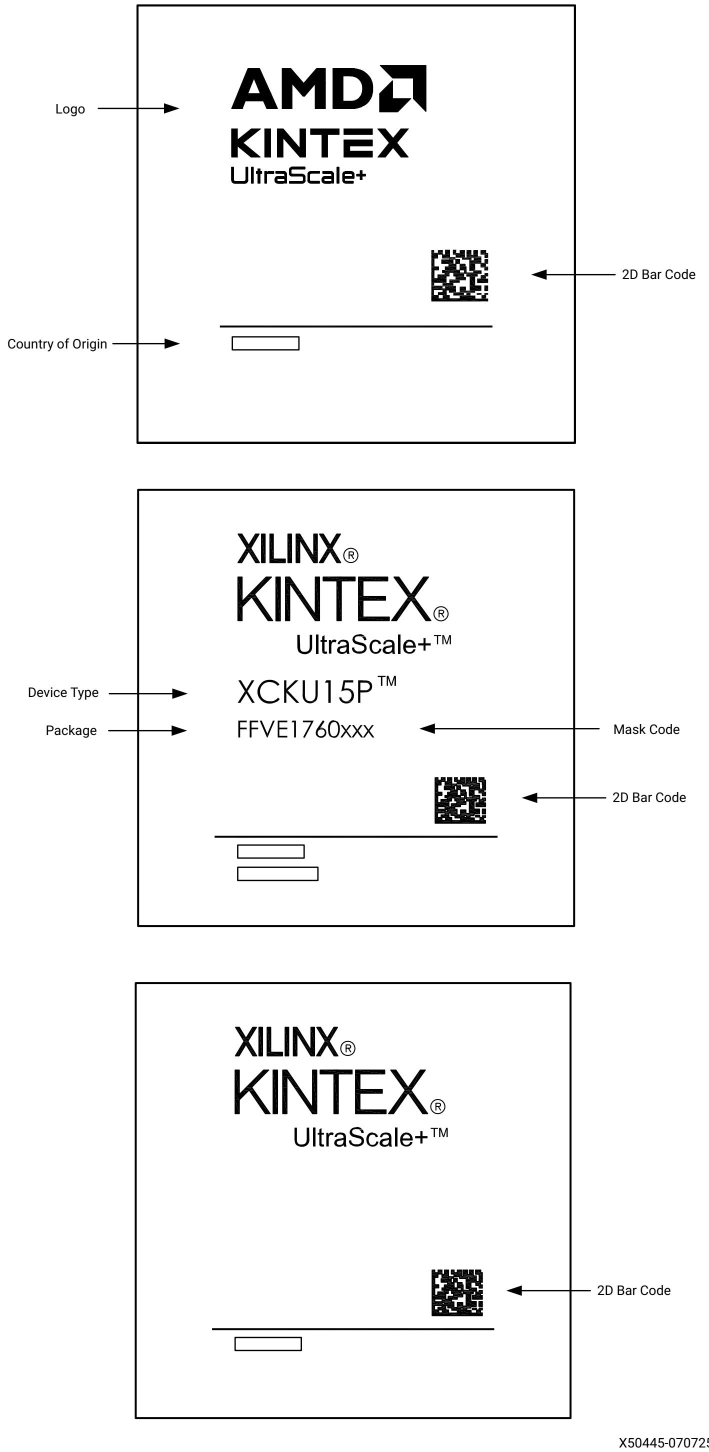


Figure 5-4: **Kintex UltraScale+ Device Package Marking**

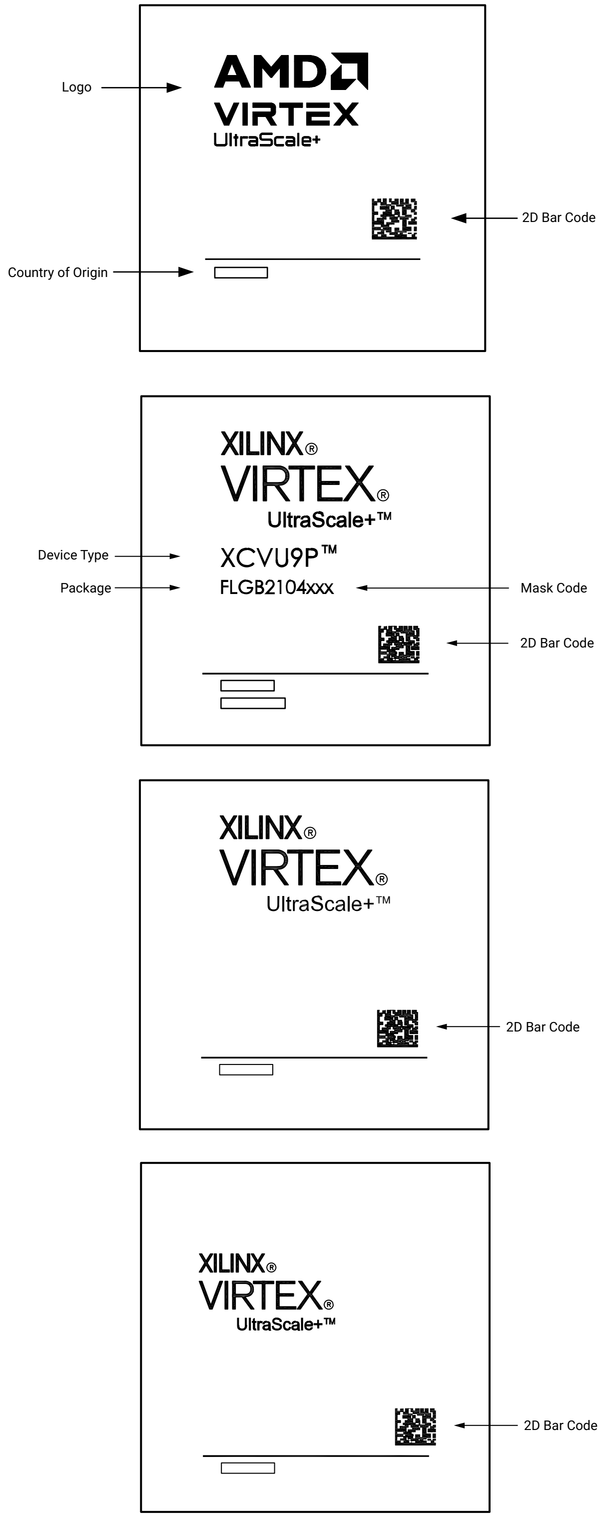


Figure 5-5: **Virtex UltraScale+ Device Package Marking**

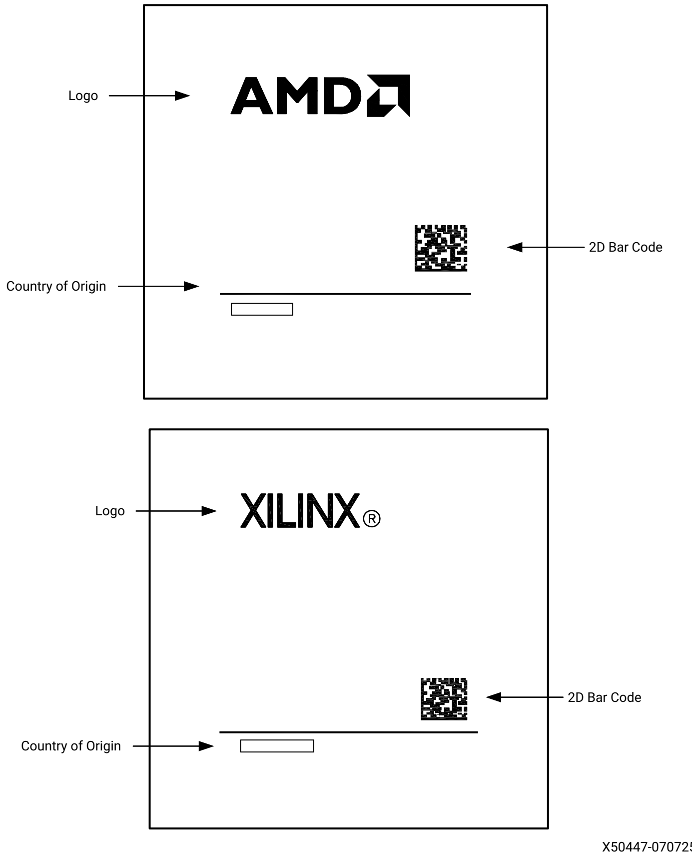


Figure 5-6: **Spartan UltraScale+, XQ Kintex UltraScale+, and XQ Virtex UltraScale+ Device Package Marking**

Table 5-1: **XC Device Marking Definition—Example**

<table>
<tr><th>Item</th><th colspan="2">Definition</th></tr>
<tr><td>Company Logo</td><td colspan="2">Company logo, company name.</td></tr>
<tr><td>Family Brand Logo</td><td colspan="2">Device family name with trademark and trademark-registered status. This line is optional and could appear blank.</td></tr>
<tr><td>1st Line</td><td colspan="2">Device name. This line is not marked on some devices. Refer to the bar code for device information.</td></tr>
<tr><td>2nd Line</td><td colspan="2">This line is not marked on some devices. Refer to the bar code for device information.
• Package code: FF
1st digit: F for flip-chip BGA, S for flip-chip BGA with 0.8 mm ball pitch.
2nd digit: F for lidded, L for lidded SSI, B for bare-die, H for overhang SSI, S for lidless SSI stiffener, and I for overhang lidless SSI stiffener.
• 3rd digit: Pb-free code: V for RoHS 6/6, G for RoHS 6/6 with exemption 15, or for packages with eutectic BGA balls (R or Q).
All commercial (XC) UltraScale Architecture devices have Pb-free RoHS compliant packaging. For more details on AMD Pb-free and RoHS compliant products, see: www.xilinx.com/pbfree.
• 4th digit: This is the pin out (net list) identifier.
• 5th–8th digits: These are the physical pin count identifiers: A1156 and D1924 are shown in the Figure 5-2 and Figure 5-3 example marking drawings. Example: A package code of FFVA1517 and FFVC1517 means they have a different pinout (net list) but the same physical ball count and physical dimensions.
• Three letter circuit design revision, the location code for the wafer fab, and the geometry code (xxx). Designated as the mask code in some figures.
• When marked, the date code: YYWW (two digit year and work week). This code is not marked on some devices. Refer to the bar code for more information.</td></tr>
<tr><td>3rd Line</td><td colspan="2">When marked, this line describes ten alphanumeric characters for assembly location, 7-digit lot number, and step information. The last digit is usually an A or an M if a stepping version does not exist.
This line is not marked on some devices. Refer to the bar code for more information.</td></tr>
<tr><td rowspan="4">4th Line</td><td colspan="2">When marked, this line describes the device speed grade (1) and temperature operating range (C). When not marked on the package, the product is considered to operate at the extended (E) temperature range.
If a bar code is present on the device, the 4th line might be blank or unmarked. In this case, refer to the bar code for speed grade and temperature range information. For more information on the ordering codes, see the UltraScale Architecture and Product Overview (DS890).
Other variations for the 4th line:</td></tr>
<tr><td>L1I</td><td>The L1I indicates a -1LI device. The -1LI speed grade offers reduced maximum power consumption. For more information, see the UltraScale Device Data Sheets.</td></tr>
<tr><td>1C xxxx</td><td>The xxxx indicates a 4-digit SCD device option. An SCD is a special ordering code that is not always marked in the device top mark.</td></tr>
<tr><td>1C ES
2E ES
L1I ES</td><td>The addition of an ES after the operating temperature range code indicates an engineering sample.</td></tr>
<tr><td>Bar Code</td><td colspan="2">A device-specific bar code is marked on each device. Refer to the FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products (XTP424).</td></tr>
</table>

Chapter 6

Packing and Shipping

Introduction

The AMD UltraScale™ and AMD UltraScale+™ devices are packed in trays. Trays are used to pack most of AMD surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are manufactured using anti-static material to provide limited protection against ESD damage and can withstand a bake temperature of 125°C.

Table 6-1: **Standard Device Counts per Tray and Box**

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
FCVA289	260	1300
CMVA361	240	1200
UBVA368	168	840
SBVB484, SBVC484	84	420
CMVA529	152	760
SBVB625	60	300
FBVA676, RBA676	40	200
FFVA676, FFVB676, RRFB676	40	200
SFVA784, SFVB784, SFRB7784	60	300
FBVA900	27	135
FFVD900, FFVE900	27	135
FFVA1156, RFA1156, FFRA1156	24	120
VSVA1365	24	72
FFVA1517, FFVC1517, FFVD1517, FFVE1517, FFRC1517, FFRE1517	21	105
FLVA1517, FLVD1517, RLD1517	21	63
FFVA1760, FFVB1760, FFVE1760, FFVJ1760	12	60
FLVB1760, FSVJ1760	12	36
FLVD1924, FLVF1924, RLF1924	12	36
FLGF1924	12	36

Table 6-1: **Standard Device Counts per Tray and Box *(Cont'd)***

Package	Maximum Number of Devices Per Tray	Maximum Number of Units In One Internal Box
FSVH1924	12	36
FFVA2104, FLVA2104, FLGA2104, FLRA2104 FFVB2104, FLVB2104, FLGB2104, FLRB2104 FFVC2104, FLVC2104, FLGC2104, FLRC2104	12	36
FHGA2104, FHGB2104, FHGC2104 FIGD2104	10	30
FSGD2104	12	36
FSVH2104	12	36
FLGB2377	10	30
FLGA2577	10	30
FSGA2577	10	30
FLGA2892	10	30
FSVH2892, FSVK2892	10	30
FSVA3824, FSVB3824	4	12

IMPORTANT: *All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC, and the third digit in the package name is Q (for example: FFQA1156).*

Chapter 7

Soldering Guidelines

Soldering Guidelines

To implement and control the production of surface-mount assemblies, the dynamics of the Pb-free solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

RECOMMENDED: *AMD recommends that customers qualify their custom PCB assembly processes using package samples.*

The primary phases of the Pb-free reflow process are:

- Melting the particles in the solder paste
- Wetting the surfaces to be joined
- Solidifying the solder into a strong metallurgical bond

The peak reflow temperature of a surface-mount component body should not be more than 250°C maximum (260°C for dry rework only) for Pb-free packages and 220°C for eutectic packages, and is package size dependent. For multiple BGAs in a single board and because of surrounding component differences, AMD recommends checking all BGA sites for varying temperatures.

The infrared reflow (IR) process is strongly dependent on equipment and loading. Components might overheat due to lack of thermal constraints. Unbalanced loading can lead to significant temperature variation on the board. These guidelines are intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

IMPORTANT: *Following the initial placement and reflow process, devices should not be reflowed more than two additional times and should not be removed from the board. Any additional rework beyond that is likely to cause irreparable damage to the device.*

Sn/Pb Reflow Soldering

Figure 7-1 shows typical conditions for solder reflow processing of Sn/Pb soldering using IR/convection. Both IR and convection furnaces are used for BGA assembly. The moisture sensitivity of PSMCs must be verified prior to surface-mount flow.

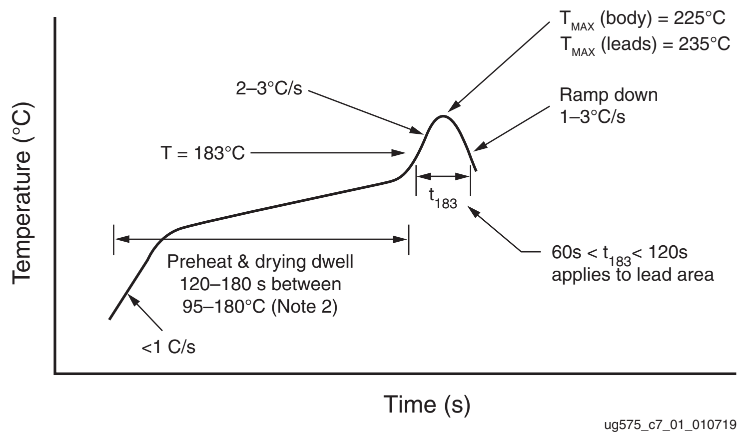


Figure 7-1: **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**

Notes for Figure 7-1:

1. Maximum temperature range = 225°C (body). Minimum temperature range = 205°C (leads/balls).
2. Preheat dwell 95–180°C for 120–180 seconds.
3. IR reflow must be performed on dry packages.

Pb-Free Reflow Soldering

AMD uses SnAgCu solder balls for BGA packages. In addition, suitable package materials are qualified for the higher reflow temperatures (250°C maximum, 260°C for dry rework only) required by Pb-free soldering processes.

AMD does not support soldering SnAgCu BGA packages with SnPb solder paste using a Sn/Pb soldering process. Traditional Sn/Pb soldering processes have a peak reflow temperature of 220°C. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields can be compromised.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board. Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

Table 7-1 and Figure 7-2 provide guidelines for profiling Pb-free solder reflow for package sizes up to 45 mm x 45 mm. Table 7-2 provides guidelines for package sizes greater than 45 mm x 45 mm and up to 55 mm x 55 mm. Table 7-3 provides guidelines for packages sizes greater than 55 mm x 55 mm. In general, a gradual, linear ramp into a spike has been shown by various sources to be the optimal reflow profile for Pb-free solders (Figure 7-2). This profile has been shown to yield better wetting and less thermal shock than conventional ramp-soak-spike profile for the Sn/Pb system. SnAgCu alloy reaches full liquidus temperature at 235°C. When profiling, identify the possible locations of the coldest solder joints and ensure that those solder joints reach a minimum peak temperature of 235°C for at least 10 seconds. Reflowing at high peak temperatures of 260°C and above can damage the heat sensitive components and cause the board to warp. Users should reference the latest IPC/JEDEC J-STD-020 standard for the allowable peak temperature on the component body. The allowable peak temperature on the component body is dependent on the size of the component. Refer to Table 7-4 for peak package reflow body temperature information. In any case, use a reflow profile with the lowest peak temperature possible.

Table 7-1: **Pb-Free Reflow Soldering Guidelines for Package Sizes Up to 45 mm x 45 mm**

Reflow Profile	Convection, IR/Convection
Preheat ramp-up rate 30°–150°C	2°C/s maximum 1°C/s maximum for lidless packages with stiffener ring
Preheat temperature soak time 150°–200°C	60–120 seconds
Temperature maintained above 217°C	60–150 seconds (60–90 seconds typical)
Time within 5°C of actual peak temperature	30 seconds maximum
Peak temperature (lead/ball)	230°C—245°C typical (depends on solder paste, board size, component mixture)
Maximum peak temperature (body)	240°C—250°C, package body size dependent (see the specific data sheet under UltraScale Device Data Sheets)
Ramp-down rate	2°C/s maximum
Time 25°C to peak temperature	3.5 minutes minimum, 5.0 minutes typical, 8 minutes maximum

Table 7-2: **Pb-Free Reflow Soldering Guidelines for Package Sizes Greater than 45 mm x 45 mm and Up to 55 mm x 55 mm**

Reflow Profile	Convection, IR/Convection
Preheat ramp-up rate 30°–150°C	0.5°C/s–1.5°C/s
Preheat temperature soak time 150°–190°C	65–70 seconds
Temperature maintained above 217°C	50–60 seconds
Maximum peak temperature (body)	234°C—238°C (see the specific data sheet under UltraScale Device Data Sheets)
Ramp-down rate 240°–125°C	1°C/s – 2°C/s

Table 7-3: **Pb-Free Reflow Soldering Guidelines for Package Sizes Greater than 55 mm x 55 mm**

Reflow Profile	Convection, IR/Convection
Preheat ramp-up rate 30°–150°C	0.5°C/s–1.5°C/s
Preheat temperature soak time 150°–190°C	76–81 seconds
Temperature maintained above 217°C	77–93 seconds
Maximum peak temperature (body)	231°C—240°C (see the specific data sheet under UltraScale Device Data Sheets)
Ramp-down rate 240°–185°C	0.7°C/s – 0.8°C/s
Ramp-down rate 185°–125°C	1.6°C/s – 1.75°C/s

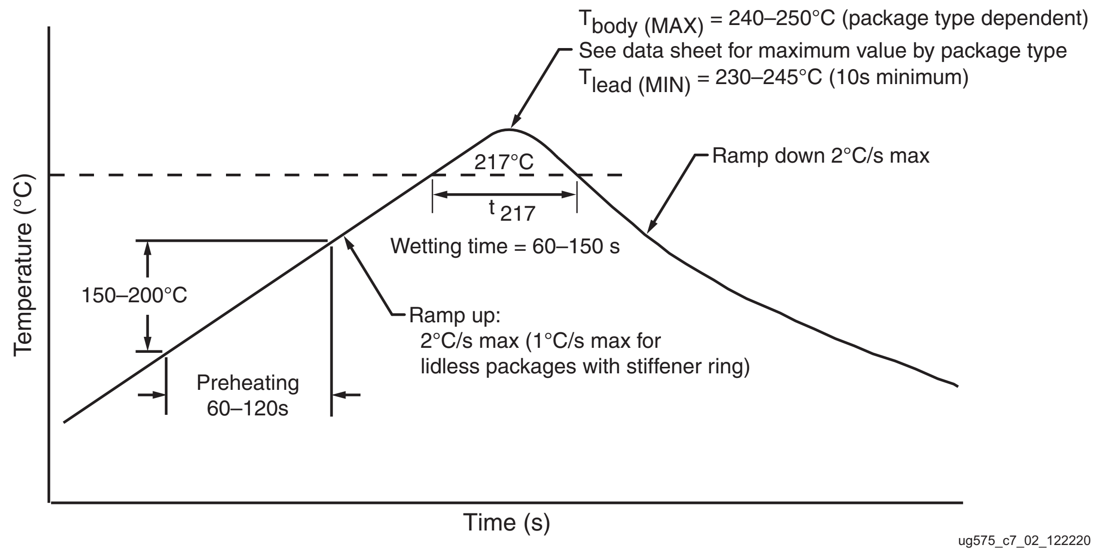


Figure 7-2: **Typical Conditions for Pb-Free Reflow Soldering (Package Sizes up to 45 mm x 45 mm)**

Table 7-4: **Peak Package Reflow Body Temperature for AMD Packages (Based on J-STD-020 Standard)**

Package	Product Category	Peak Package Reflow Body Temperature[1]	JEDEC Moisture Sensitivity Level (MSL)
CMVA361 CMVA529 FBVA676 FFVA676, FFVB676 SBVB484, SBVC484 SBVB625 SFVA784, SFVB784	XC	Mass reflow: 250°C Dry rework: 260°C	4
UBVA368 FBVA900 FFVD900, FFVE900 FFVA1156 FFVA1517, FLVA1517, FFVC1517, FFVD1517, FLVD1517, FFVE1517 FFVA1760, FFVB1760, FLVB1760, FFVE1760, FFVJ1760 FLVD1924, FLVF1924, FLGF1924 FFVA2104, FLVA2104, FLGA2104, FHGA2104 FFVB2104, FLVB2104, FLGB2104, FHGB2104 FFVC2104, FLVC2104, FLGC2104, FHGC2104 FLGB2377 FLGA2577 FLGA2892	All	Mass reflow: 245°C Dry rework: 260°C	4
VSVA1365 FSVJ1760 FSVH1924 FSGD2104, FIGD2104, FSVH2104 FSGA2577 FSVH2892, FSVK2892 FSVA3824, FSVB3824	All	Mass reflow: 240°C Dry rework: 260°C	4

Table 7-4: **Peak Package Reflow Body Temperature for AMD Packages (Based on J-STD-020 Standard)** ***(Cont'd)***

Package	Product Category	Peak Package Reflow Body Temperature[1]	JEDEC Moisture Sensitivity Level (MSL)
RBA676, RFA1156, RLD1517, RLF1924 FFRB676, SFRB784 FFRA1156, FFRC1517, FFRE1517 FLRA2104, FLRB2104, FLRC2104	XQ[2]	Mass reflow: 225°C Dry rework: 235°C	4

Notes:

1. See the specific data sheet under UltraScale Device Data Sheets for the most up-to-date specifications.
2. For devices with the Pb-free signifier in the package name (labeled as Q vs. V) use the temperatures and MSL listed for the XQ product category.

For sophisticated boards with a substantial mix of large and small components, it is critical to minimize the ΔT across the board (<10°C) to minimize board warpage and thus, attain higher assembly yields. Minimizing the ΔT is accomplished by using a slower rate in the warm-up and preheating stages.

It is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cooling down phase. The key is to optimize cooling while maintaining a minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder balls should be maintained at less than 7°C during the critical region of the cooling phase of the reflow process. This critical region is in the part of the cooling phase where the balls are not completely solidified to the board yet, usually between the 200°C–217°C range. To efficiently cool the parts, divide the cooling section into multiple zones, with each zone operating at different temperatures.

The optimal profile must take into account the solder paste/flux used, the size of the board, the density of the components on the board, and the mix between large components and smaller, lighter components. Profiles should be established for all new board designs using thermocouples at multiple locations on the component. In addition, if there is a mixture of devices on the board, then the profile should be checked at various locations on the board, as shown in Figure 7-3 and Figure 7-4 (thermocouple pictures). Ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that might damage the smaller, heat sensitive components.

TOP Profile,
TC 1 : U17 Edge 1
TC 2 : U17 Edge 2
TC 3 : U17 Edge 3
TC 4 : U17 Edge 4
TC 5 : U17 Middle 1
TC 6 : U17 Middle 2
TC 7 : U17 Body
TC 8 : Q25
TC 9 : U25

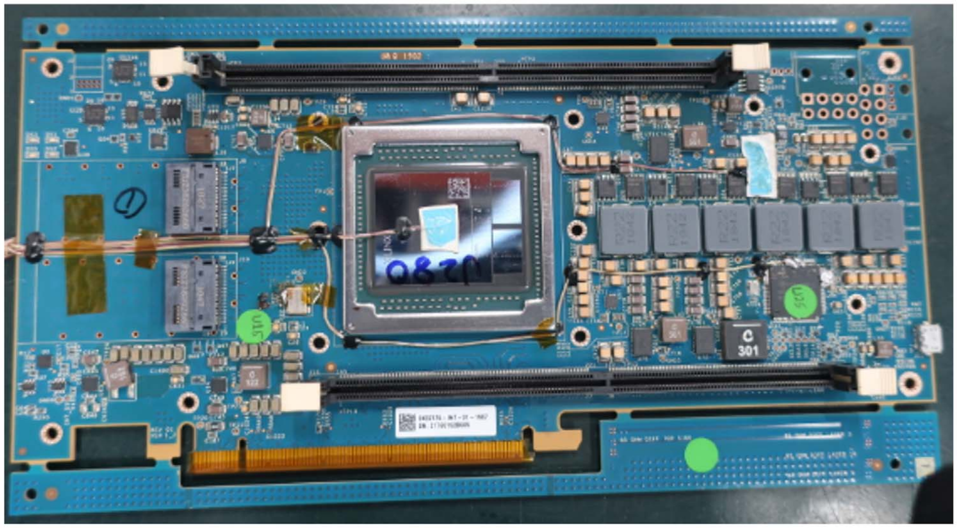


Figure 7-3: **Thermocouple Top**

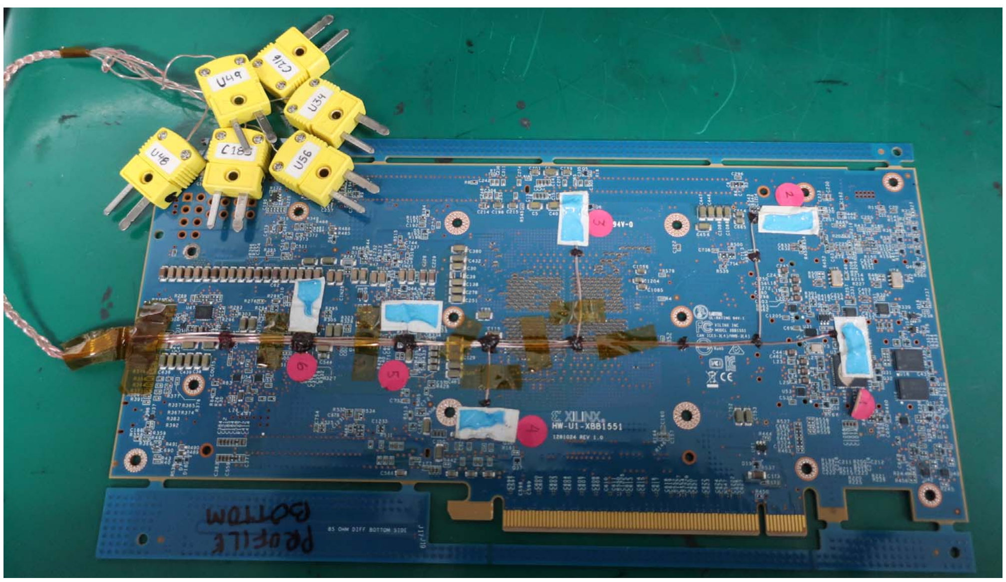


Figure 7-4: **Thermocouple Bottom**

Post Reflow/Cleaning/Washing

Many PCB assembly subcontractors use a no-clean process in which no post-assembly washing is required. Although a no-clean process is recommended, if cleaning is required, AMD recommends a water-soluble paste and a washer using a deionized-water. Baking after the water wash is recommended to prevent fluid accumulation.

Cleaning solutions or solvents are not recommended because some solutions contain chemicals that can compromise the lid adhesive, thermal compound, or components inside the package.

Strain Gauge Measurement

Strain gauge measurements are recommended to be done at each process step that has the potential to cause excessive board flexing leading to solder joint cracking. Assembly processes where strain gauge measurements are recommended include:

- PCB Router (during PCB loading/unloading into fixture and during the routing process)
- PTH solder assembly during top-catch loading/unloading
- Press fit assembly during press base and tooling loading/unloading and during machine pressing process
- DIMM memory (during PCB loading/unloading and during insertion/removal of DIMM)
- Heat-sink assembly process (during PCB loading/unloading and during entire screw assembly process)
- X-ray fixture (during PCBA loading/unloading)

Strain gauge measurements should be in the range of ±500 µstrain. Dye and pry analysis is required to confirm if the measured strain causes solder joint cracking. It is recommended to conduct dye and pry analysis for any strain reading greater than 500 µstrain.

To reduce the affects of strain on a device, edge bonding can be used and is recommended for larger packages. See Edge Bonding and Underfill Guidelines for implementation details.

Solder Paste

Solder paste consists of solder alloy and a flux system. A typical solder paste composition by volume is split between about 50% alloy and 50% flux. The metal load mass (solder alloy powder) is around 90%, with the remaining 10% mass a flux system. The primary purpose of the flux system is to remove the contaminations from the solder joints during the soldering process. The capability of removing contaminations is determined by the activation level of the type of solder paste. The preferred solder paste metal alloy has a lead-free composition (SnAgCu where Ag is 3–4% and Cu is 0.5–1%). A *no-clean* solder paste is preferred to eliminate any risk of improper cleaning that could leave active residue beneath the device and other BTC components. The paste must be suitable for printing the solder stencil aperture dimensions. Type 4 paste is recommended for better paste release performance. When using a solder paste, you must adhere to the handling recommendations of the paste manufacturer.

Component Placement

IMPORTANT: *The following component placement guidelines apply to all package types included in this guide (lidded, lidless, bare-die, etc.).*

AMD device packages must be placed accurately according to their geometry outline. Positioning packages manually via hand mounting is not recommended.

Typical component placement accuracies of ±50 µm can be achieved using standard pick and placement machine equipment with vision system. The PCB and the components are optically checked and measured and the components are placed on the PCB in specific programmed positions based on the PCB CAD information. The pick and placement machine vision system detects the fiducials on the PCB immediately prior to mounting the FPGA. Recognition of the packages is performed by the vision system, to ensure correct centering of the FPGA placement on the PCB pad array.

BGA packages with solder balls can self-align during the reflow process because of the solder high surface tension that enables the pulling and centering of the device, and where a slight offset of the placement is still allowed. For guidance, the maximum tolerable offset of device placement is around 30% of the pad diameter on the PCB for typical non-solder mask defined pads. This means that for device packages the solder ball to PCB pad misalignment must be better than 150 µm to assure a robust mounting process. Generally, this is achievable using a wide range of modern pick and placement systems. The following setup conditions are important for the pick and placement systems:

- The pick and placement nozzle type should be sized to the dimensions of the AMD device. The nozzle needs to firmly hold the device package during the pick and placement stage. The appropriate nozzle type for the device package can be chosen from the manual provided by the pick and placement equipment company.
- The ball recognition capabilities of the placement system should be used and package outline centering should be avoided. This eliminates the solder ball to package edge tolerances of the package. Refer to the specific package outline drawing for details.
- To ensure the proper identification of the device package by the vision system, a suitable lighting system and the correct choice of the features of the measuring method are essential. The most suitable settings can be chosen from the manual provided by the pick and placement equipments company.
- To avoid solder bridging or solder smear, ensure the proper placement force of the device package during placement on the PCB. Excessive placement force can lead to excess solder paste and cause solder bridging. However, a slight placement force can lead to insufficient solder paste contact between the device package solder balls and the solder paste, causing solder defects including open solder joints, badly centered packages, or even head-in-pillow (HIP) defects.

Recommended PCB Design Rules for BGA Packages

BGA Packages

AMD provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure 8-1 and summarized in Table 8-1. PCB pad size is based on the BGA ball size. Typical requirements for the PCB pad size are 80-120% of ball size however, given a large package size and to prevent solder bridging, a pad size closer to 80% of the ball size is recommended. For AMD BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 8-1.

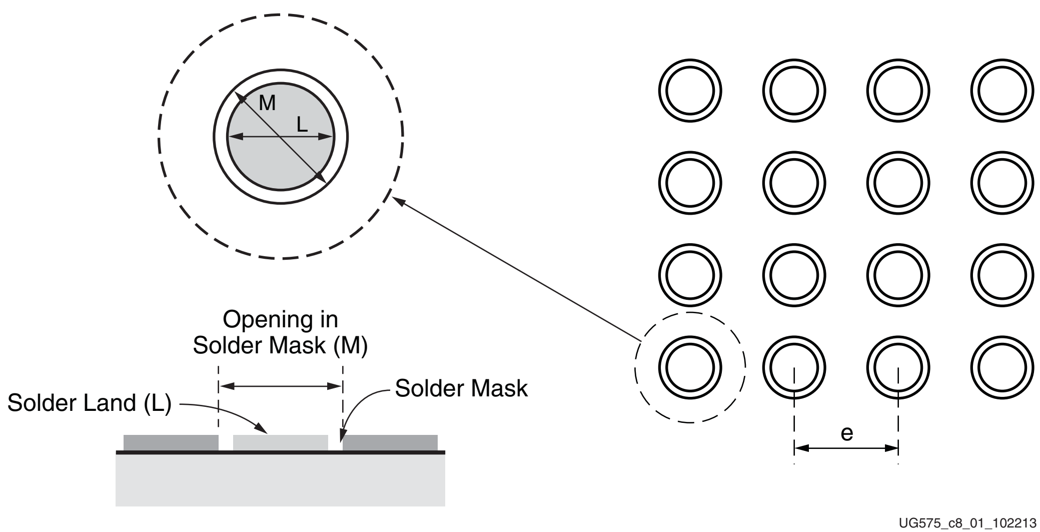


Figure 8-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

An example of an NSMD PCB pad solder joint is shown in Figure 8-2. The space between the NSMD pad and the solder mask, as well as the actual signal trace widths, depends on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

RECOMMENDED: *AMD recommends not mixing PCB pad isolated via-in-pad plated over (VIPPO) and non-VIPPO design styles because they can cause hot tear defects that are related to localized Z-direction thermal expansion coefficient mismatch between VIPPO and non-VIPPO vias. A VIPPO via expands less than a non-VIPPO via.*

RECOMMENDED: *For packages that include land-side capacitors (LSCs), such as the FSVA3824 or FSVB3824, the region underneath the LSCs should be covered by solder mask.*

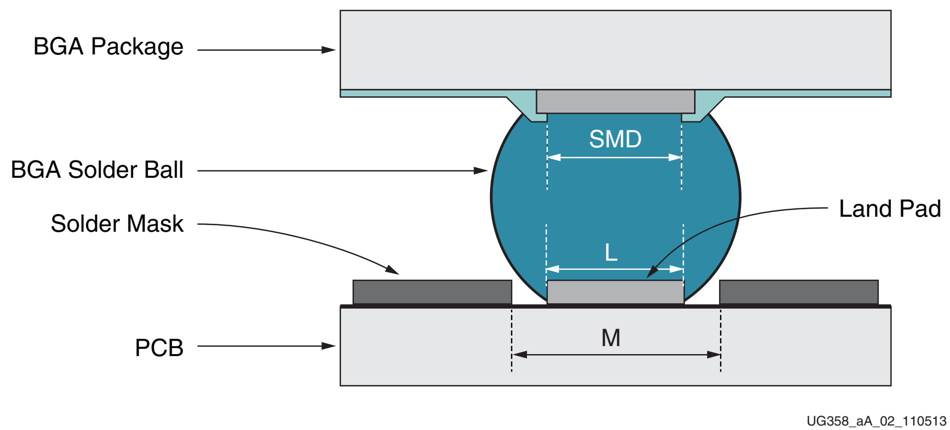


Figure 8-2: **Example of an NSMD PCB Pad Solder Joint**

Table 8-1: **BGA Package Design Rules**

Flip-Chip BGA Packages	1.0 mm Pitch	0.92 mm Pitch	0.8 mm Pitch	0.5 mm Pitch
Design Rule	**Dimensions in mm (mils)**			
Package land pad opening (SMD)	0.53 mm (20.9 mils)	0.53 mm (20.9 mils)	0.40 mm (15.7 mils)	0.28 mm (11.0 mils)
Maximum PCB solder land (L) diameter	0.50 mm (19.7 mils)	0.51 mm (20.0 mils)	0.40 mm (15.7 mils)	0.30 mm (12 mils)
Opening in PCB solder mask (M) diameter	0.65 mm (25.6 mils)	0.61 mm (24.0 mils)	0.50 mm (19.7 mils)	0.41 mm (16 mils)
Solder ball land pitch (e)	1.00 mm (39.4 mils)	0.92 mm (36.2 mils)	0.80 mm (31.5 mils)	0.50 mm (19.7 mils)

Notes:
1. Controlling dimension in mm.

Stencil

Solder paste is applied to PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases, the thickness of a stencil must be matched to the needs of all components on the PCB. Stencil apertures should be a circular shape. To ensure a uniform and high-solder paste transfer to the PCB, laser-cut stencil, made from mostly stainless steel, is typically used. Nickel Blank stencils, referring to stencils where the entire foil is laser-cut from a sheet of pure nickel material, can also be used. However, high-quality nano-coated stencils (laser cut from stainless steel) can perform as well as or better than Nickel Blanks.

Uniform Stencil Aperture Design

- Uniform stencil aperture can be implemented for the package size of up to 60 mm x 60 mm, and/or the package coplanarity of ≤8 mils, and/or the substrate warpage at peak reflow temperature is ≤100 µm or less for 1 mm pitch and 0.92 mm pitch packages. Under these conditions, the uniform stencil aperture opening of 19.7 mils to 20.0 mils round is recommended, matching the PCB pad size and the stencil thickness is 5 mil.
- For InFO packages with 0.5 mm ball pitch, a uniform stencil with squared aperture openings (rounded corners) of 12 mils and pitch of 19.8 mils, as show in Figure 8-3 is recommended. A stencil thickness of 4 mils is also recommended.

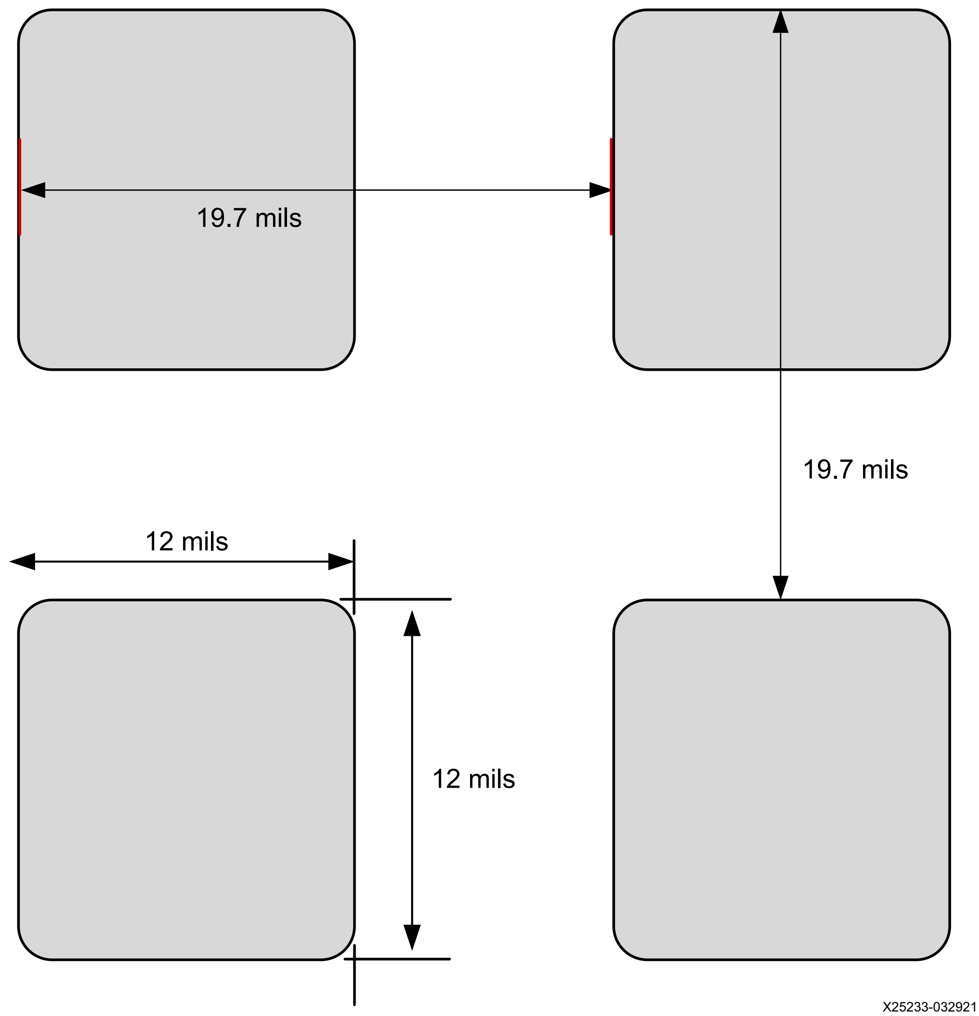


Figure 8-3: **Recommended Stencil Design for InFO Packages**

Non-Uniform (Bull's Eye) Stencil Aperture Design

Another option is to use a non-uniform stencil aperture, where the board land-pad diameter increases from the center of the device outward with a variable stencil opening that depends on the warpage as a function of thermal expansion and mechanical attachment. This can vary depending on the PCB. The bull's eye offers a capture margin, because with an increased opening size with respect to the outer BGA balls, more solder paste is printed.

For 1 mm pitch packages, the non-uniform stencil aperture design can be implemented for a package size up to 77.5 mm x 77.5 mm, and/or the package coplanarity of ≤2 mils, and/or the substrate warpage at peak reflow temperature is ≤25μ. Under these conditions, the nonuniform stencil aperture opening is recommended, and the stencil thickness is 5 mil.

The final stencil design should be based on an evaluation of the board design. Designers should work with their contract manufacturer to optimize the stencil design and assembly process.

Bull's Eye Stencil Recommendation

Another option is to use a *Bull's Eye* stencil aperture, where the board land-pad diameter increases from the center of the device outward, matching the variable aperture diameter of the stencil, at a rate that depends on the warpage as a function of thermal expansion and mechanical attachment. This can vary depending on the PCB. The bull's eye offers a capture margin, because with an increased opening size with respect to the outer BGA balls, more solder paste is printed. A recommended stencil design for the bull's eye design is shown in Figure 8-4. Similar stencil designs are recommended for packages 55 mm x 55 mm and larger with 1 mm ball pitch. The final stencil design should be based on an evaluation of the board design. Designers should work with their CM to optimize the stencil design and assembly process.

RECOMMENDED: *AMD recommends using a 4 mil to 5 mil thick stencil.*

RECOMMENDED: *AMD* recommends using a uniform stencil aperture opening of 19.7 mils to 20 mils round, matching the PCB pad size for packages less than 60 mm x 60 mm with 1.0 mm ball pitch.

RECOMMENDED: *AMD* recommends using a non-uniform (*Bull's Eye*) stencil aperture opening for packages larger than 60 mm x 60 mm and smaller than 77.5 mm x 77.5 mm with 1.0 mm ball pitch, including 2892 and 3824 pin packages.

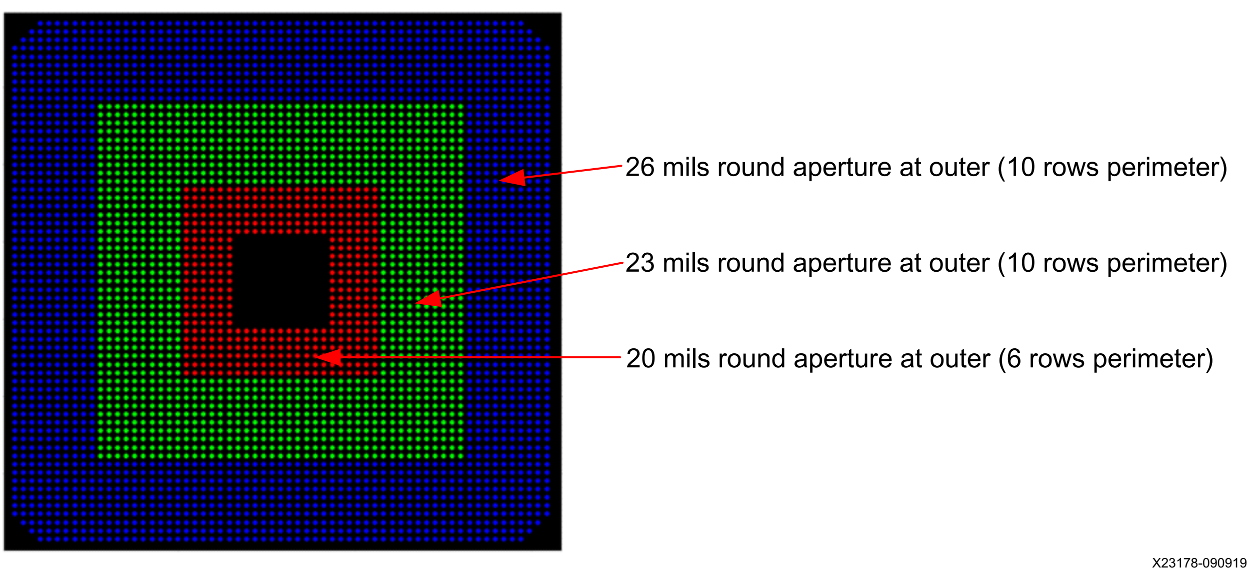


Figure 8-4: **Bull's Eye Stencil Aperture**

Chapter 9

Edge Bonding and Underfill Guidelines

Summary

The edge bonding technique uses high-adhesion adhesives dispensed along the periphery of a component, as shown in Figure 9-1. AMD recommends edge bonding for increased mechanical reliability in cases where the device is exposed to extensive temperature cycling or extreme shock and vibration, such as space, defense, and telecommunications applications. Designers are expected to evaluate the need for edge bonding based on the requirements of the specific application implementation.

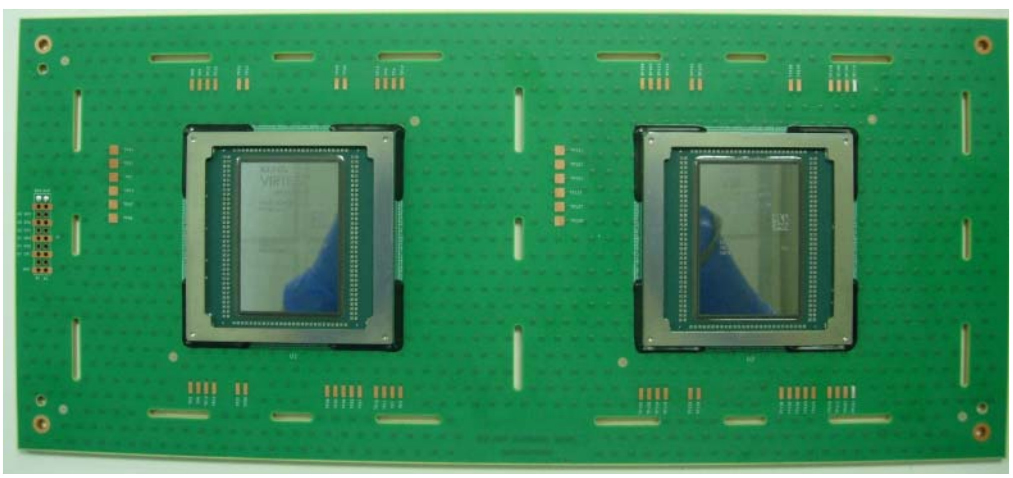


Figure 9-1: **Edge Bonded BGA Packages**

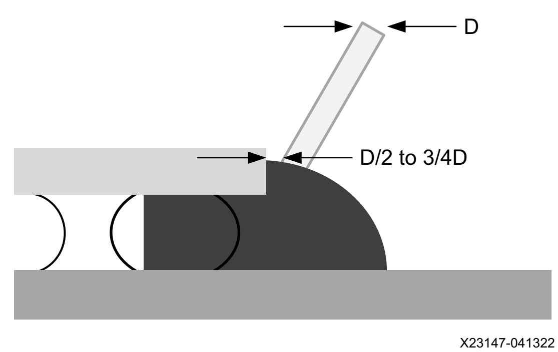
Edge Bonding Implementation

Edge bonding is the dispensing of an epoxy material around the periphery of the package after board mount. The following guidelines are based on evaluation using the Zymet UA-2605-B edge-bonding material. This technique allows for component rework and improves the robustness of the mounted component by controlling the expansion and warpage of the board during normal operating conditions

IMPORTANT: *Following the initial placement and reflow process, devices should not be reflowed more than two additional times and should not be removed from the board. Any additional rework beyond that is likely to cause irreparable damage to the device.*

To place the adhesive while using an in-line soldering robot, AMD recommends the parameters shown in Table 9-1.

Table 9-1: **Process Parameters for Edge Bonding**

Process Parameter	Range Specification
Needle size	25—15, where needle diameter (D) is 20 gauge (0.91 mm) typical for standard packages
Needle height	Above the device edge midpoint, or 0 to 1.5 mm below the device top surface (1.0 mm typical)
Needle edge spacing	Half to three quarters of the needle outer diameter (D) Typical: Half of needle diameter (D/2) or approximately 1.0 mm 
Dispense needle speed	0.1 to 200 mm/second (6 mm/sec typical)
Valve pressure	10 to 60 psi (14.5 psi typical)

The adhesive is dispensed along the perimeter of the assembled component at a width of 2.5 mm to 3 mm and a height of 50% to 90% the substrate height, leaving a small section at the center of each edge unbonded, as illustrated in Figure 9-3. This is to ensure that there is an outlet for any expansion of the air during processing. AMD recommends centering the opening on each side with a width of 25–30% the length of the package substrate. The exact locations and size of the openings can be varied depending on the design and rework.

To ensure proper mechanical bonding between the package and PCB, the edge bonding feature must penetrate the edge bonding material under the package substrate by 1.8 mm. This requirement is necessary for packages with coplanarity ≤200 µm, and BGA pitch of 1 mm or 0.92 mm, to pass physical qualification tests such as thermal cycle, power cycle, and shock and vibration requirements. It is necessary for special applications such as telecom, industrial, and data center applications.

IMPORTANT: *Some package devices have an overhang substrate that can result in the first row of the BGA not being covered by edge-bonding material. In other scenarios, the first BGA row could cover up to 90% of the BGA. See the following scenarios.*

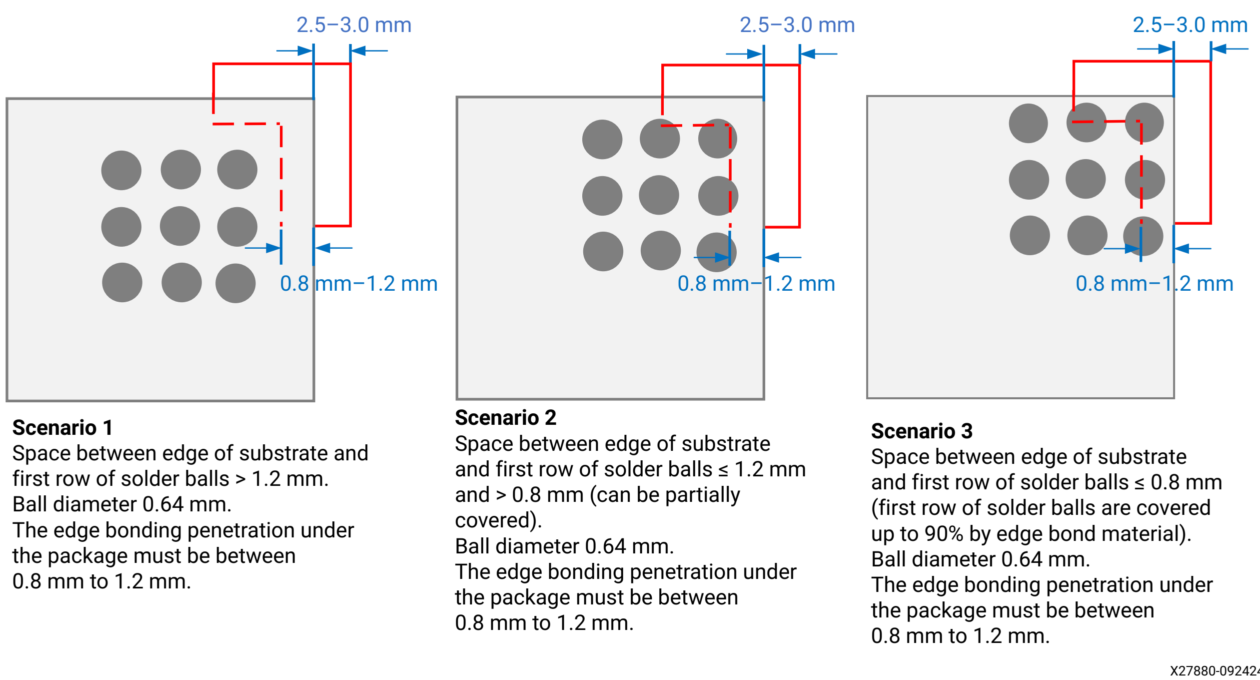


Figure 9-2: **Edge Bonding Scenarios**

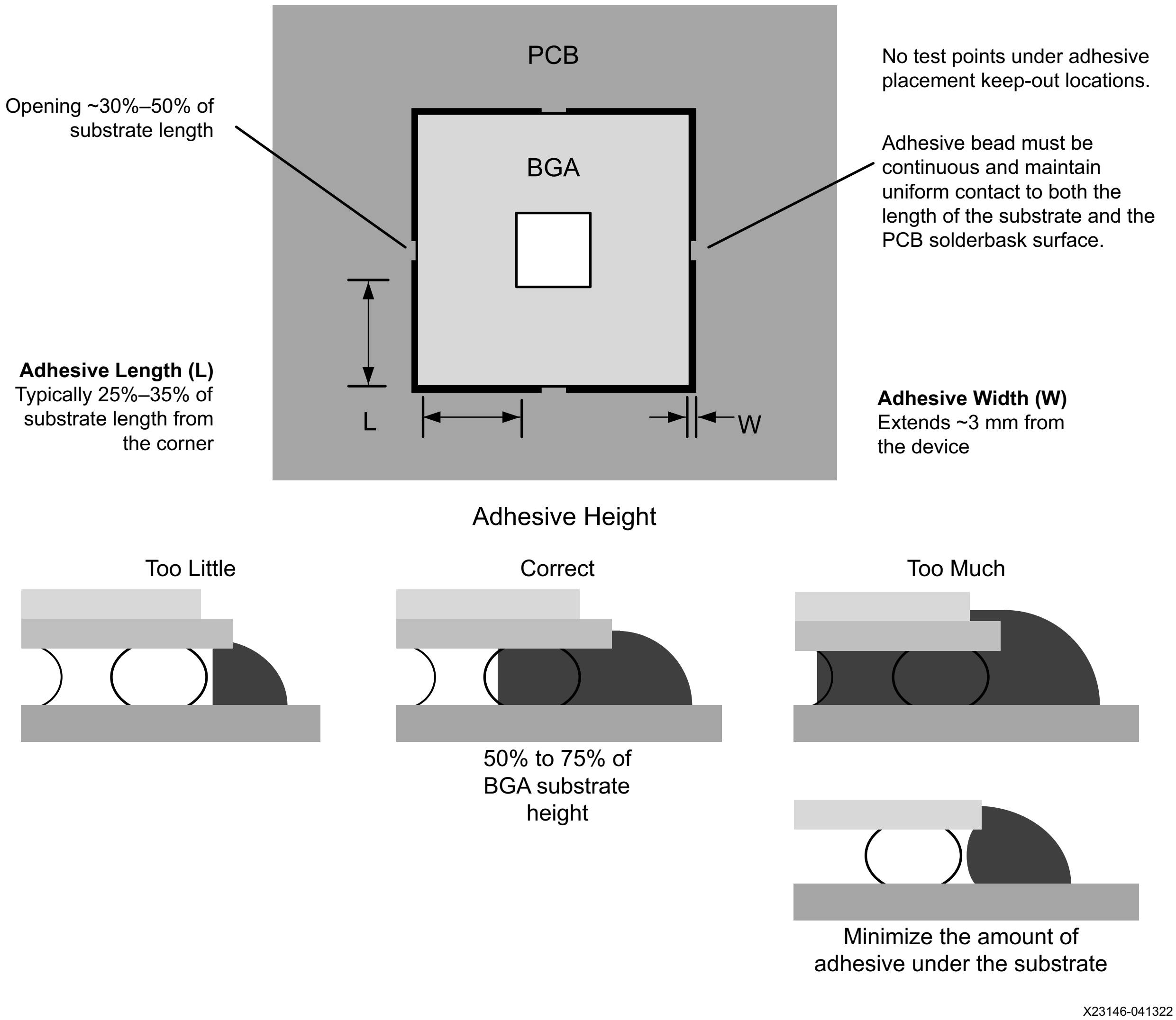


Figure 9-3: **Edge Bonding Adhesive Placement Parameters**

RECOMMENDED: *Curing condition of the Zymet UA-2605-B edge-bonding material is 140°C for 5 minutes.*

Component Clearance Surrounding Edge Bond

An adjacent component clearance surrounding the AMD device is necessary to have the 30° to 45° angle required by the for the edge bond dispenser to dispense the edge bond adhesive material. The surrounding component height and distance from the device is validated based on each unique product design layout.

Edge Bond Removal

Edge bond material can be removed by heating to 170–180°C, and scraping using a stiff probe made of stable organic material such as a non-resinous wood or Teflon. Use a hot air blower on the edge bond area and slowly remove the edge bond adhesive from side to side. Do not use force to remove the edge bond adhesive. Excess adhesive on the PCB can be removed using a chisel-tip soldering iron, with sufficient precautions to limit damage to the PCB surface.

Underfill Guidelines

To meet the mechanical reliability standards for most applications, high-adhesion underfill between the package and the PCB is required for all InFO packages (e.g., UBVA530). This allows for improved robustness of the mounted component by controlling the expansion and warpage of the package and board during normal operating conditions. The following sections detail the recommended implementation of underfill on a pre-mounted InFO package.

Underfill Implementation

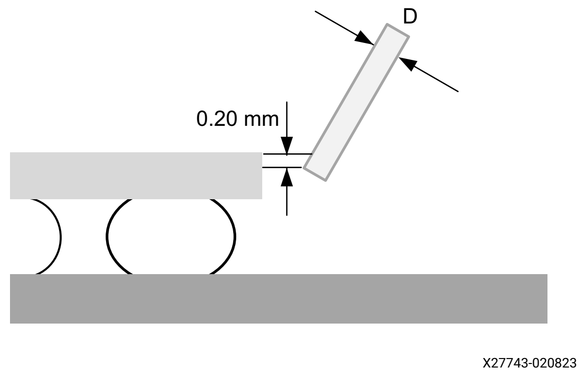
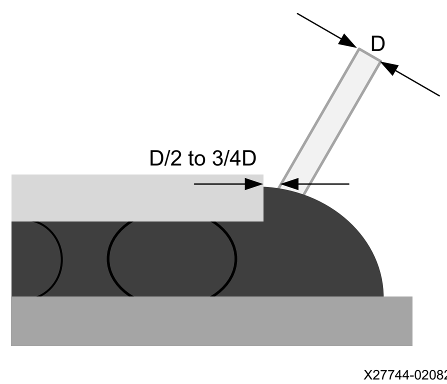
The recommended underfill process comprises of dispensing an epoxy material along one side of the package after board mount and allowing flow by way of capillary action through the BGA field. Based on the evaluation, the recommended dispensing pattern and process are detailed in the following tables.

Note: Underfill recommendations are based on evaluation with AMD devices using LOCTITE® ECCOBOND UF 3812 epoxy underfill.

Table 9-2: **Underfill Pattern**

Dispensing Pattern	Multiple-Pass Variable Length
Dispensing length	75% & 100% of package body length
Dispensing speed	15 mm/sec
Number of passes	4
Pass number and dispense length	Pass 1 & 2: 75% of package body length Pass 3 & 4: 100% of package body length
Interval between each pass	Between pass 1 & 2: 4 seconds Between Pass 2 & 3: 6 seconds Between Pass 3 & 4: 9 seconds

Table 9-3: **Underfill Process Parameters**

Process Parameter	Range Specification
Needle size	Range: 25—20 gauge Recommended: 23 gauge. Needle diameter (D) is 0.64mm
Needle height	Range: Above the device edge midpoint, or 0 to 0.2 mm below the device top surface Recommended: 0.2 mm from the top surface of the device 
Needle edge spacing	Range: Half to three quarters of the needle outer diameter (D) Recommendation: D/2, half of the needle diameter, approximately 0.32 mm 
Dispense needle speed	Range: 0.1 to 200 mm/sec Recommendation: 15 mm/sec
Valve pressure	Range: 10 to 60 psi Recommendation: 14.5 psi

The following image is an example of underfill adhesive placement on a typical InFO package.

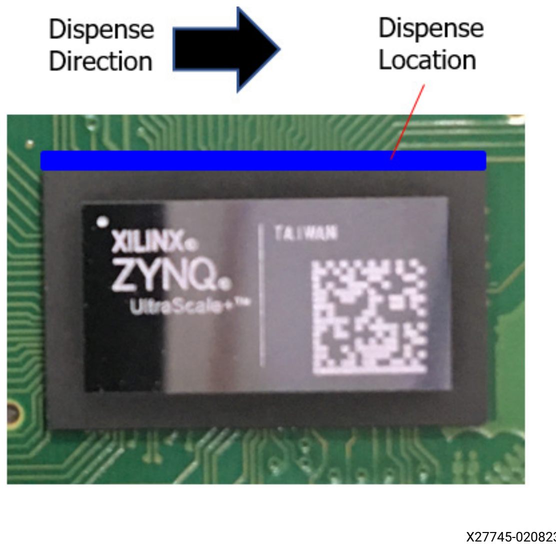


Figure 9-4: **Underfill Dispensing Location**

RECOMMENDED: *Curing time and temperature varies by the type of underfill used. Based on evaluation, oven curing temperature setting conditions are typically 155°C for 12 minutes. In this case, the temperature profile for the underfill material should be 150°C for 7 minutes.*

Underfill Keep-out Requirements

To ensure that underfill bleed-out does not impact surrounding components, the keep-out requirements shown in the following table must be considered.

Table 9-4: **Underfill Keep-out Requirements**

Keep-Out Between Components	Minimum Spacing (mm)
Underfilled BGA to underfilled BGA	5.0
Underfilled BGA to non-underfilled BGA	2.5
Underfilled BGA to passive components	2.5

Underfill Rework

The following steps detail the underfill rework process based on evaluation on a typical InFO package. This process is only possible with re-workable epoxy underfill and varies depending on the underfill type and manufacturer.

Required Instrumentation:

- Equipment: SRT machine, SRT nozzle, and pallet
- Materials: Tacky flux
- Hand tools: Tweezers, steel probe with round pointed tip, solder wick, and cotton swab

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Figure 9-5: **Underfill Rework Tools**

Step 1: Pre-bake

Boards are required to bake at least 4 hours at 125°C to avoid any moisture induced failure during the rework process.

Step 2: SRT Machine Program Creation

An SRT machine is highly recommended for the underfill rework process. An SRT machine allows you to control temperature and time at multiple stages. The underfill rework program for an SRT machine needs to be created with three stages, shown in the following table. The bottom heater temperature should be set at 150°C for all stages to allow efficient ramp time, control board warping, and minimize unnecessary heating of neighboring components.

Table 9-5: **Underfill Rework SRT Machine Program**

Stage	Nozzle Temperature	Time (seconds)	Description
Stage 1	200°C	100	Pre-heating and underfill fillet removal engulfing the component
Stage 2	220°C to 230°C	100	Component Removal
Stage 3	200°C to 225°C	150	Rework site cleaning—scrape underfill residue

Step 3: Machine and Board Setup

a. Select and load the program. Measure the thermal profile prior to underfill rework to validate the program is within specifications.

b. Use the pallet to clamp and secure the board position on the SRT machine. Sufficient support is needed to prevent the board from flexing or warping during rework.

c. Assemble the nozzle to the SRT machine top heater. Use a nozzle that is slightly larger (+1mm) than the component on all sides. This is to allow even heat and air flow to the component and to control excess heat exposure to nearby components. Thermal shielding can also be applied to nearby component to minimize excess heat.

d. To begin the pre-heating process, lower the SRT nozzle to the top of the rework surface (2 mm to 3 mm above), as shown in the following figure.

Figure 9-6: **SRT Nozzle Lowered 2 mm to 3 mm from Component Top Surface**

Step 4 (Stage 1): Pre-Heating

During pre-heating, allow the component to reach 200°C. Use non-abrasive tools (a wooden probe) to scrape off the underfill fillet around the component. If using a steel probe with a round pointed tip, ensure that the tip is directed away from the component side wall to prevent any damage to the solder mask.

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Figure 9-7: **Removing Underfill Using Steel Probe**

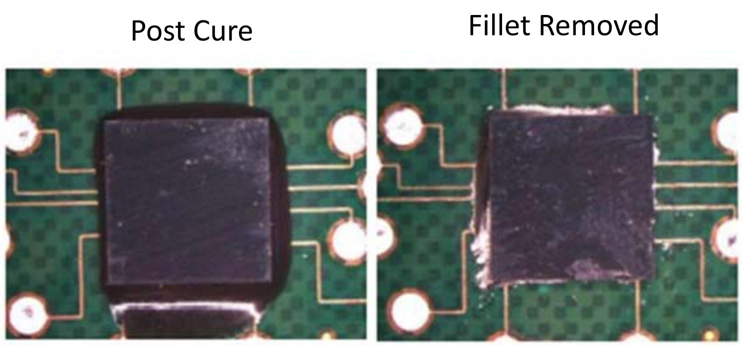

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Figure 9-8: **Removing the Underfill Fillet (Before and After)**

Step 5 (Stage 2): Component Removal

After underfill fillet removal is complete, ramp up the temperature above 220°C prior to component removal. Considering that the solder paste (SAC305) melting point is from 217°C to 220°C, ensure the rework component achieves an even temperature of 220°C or above to avoid potential defects such as pad lifting.

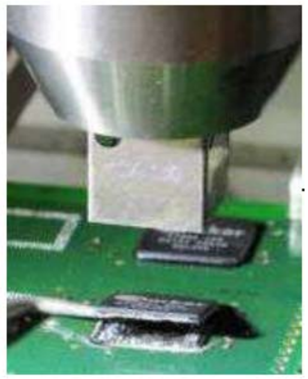

Figure 9-9: **Component Removal**

Step 6 (Stage 3): Rework Site Cleaning

The final stage is rework site cleaning. After component removal, use a non-abrasive tool (wooden probe) to scrape off the underfill residue. Use a flux saturated cotton swab to pick up and clean the remaining underfill residue.

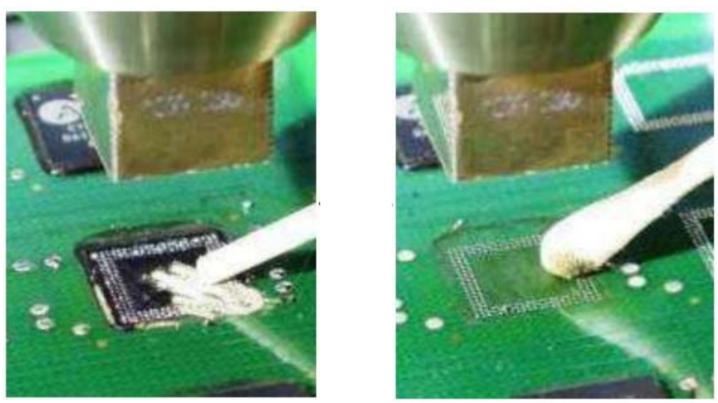

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Figure 9-10: **Scrape Away Underfill Residue and Clean with a Flux Saturated Cotton Swab**

IMPORTANT: *Following the initial placement and reflow process, devices should not be reflowed more than two additional times and should not be removed from the board. Any additional rework beyond that is likely to cause irreparable damage to the device.*

Conformal Coating

AMD does not have information regarding the reliability of flip-chip BGA packages on a board after exposure to any specific conformal coating process. Therefore, any process using conformal coating should be qualified for the specific use case to cover the materials and process steps.

Ruggedized XQ packages are designed to support conformal coating, with vented lids that ensure proper cleaning can occur after the etching process and prior to conformal coating.

RECOMMENDED: *When a conformal coating is required, Parylene-based material should be used to avoid potential risk of weakening the lid or stiffener ring adhesive used in AMD packages.*

Chapter 10

Thermal Specifications

Introduction

AMD UltraScale™ and AMD UltraScale+™ devices are offered exclusively in thermally efficient flip-chip BGA packages. These flip-chip packages range in pin-count from the smaller 9 x 9 mm FCVA289 to the 65 x 65 mm FSVA3824. This suite of packages is used to address the various power requirements of the UltraScale and UltraScale+ devices. UltraScale devices are implemented in the 20 nm process technology. UltraScale+ devices are implemented in the 16 nm process technology.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application is not known to the component supplier. Therefore, it remains a challenge for AMD to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, AMD offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. UltraScale and UltraScale+ devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, AMD devices do not come with preset thermal solutions. Your design operating conditions dictate the appropriate solution.

Thermal Resistance Data

Table 10-1 shows the thermal resistance data for UltraScale and UltraScale+ devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

IMPORTANT: *The data in Table 10-1 is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14. This data is not to be used in place of thermal simulation. Instead, refer to the thermal models provided for each device.*

TIP: *The thermal data query for all available devices by package is available on the AMD website:* www.xilinx.com/cgi-bin/thermal/thermal.pl.

IMPORTANT: *All non-InFO packages are available with eutectic BGA balls. To order these packages, the device type starts with an XQ vs. XC, and the third digit in the package name is Q (for example: FFQA1156). Refer to the XC version of these packages for their thermal resistance data and thermal models.*

Table 10-1: **Thermal Resistance Data**

Package	Package Body Size	Devices	θ_{JB} (°C/W)[2]	θ_{JC} (°C/W)[2]	θ_{JA} (°C/W)[2]	$\theta_{JA\text{-}Effective}$ (°C/W)[1][2]		
						@250 LFM	@500 LFM	@750 LFM
Kintex UltraScale Devices								
FBVA676	27 x 27	XCKU035	2.4	0.03	11.7	7.9	6.6	6.2
		XCKU040	2.4	0.03	11.7	7.9	6.6	6.2
RBA676	27 x 27	XQKU040	3.2	0.26	12.4	8.3	6.9	6.5
SFVA784	23 x 23	XCKU035	2.0	0.21	13.1	9.4	7.9	7.3
		XCKU040	2.0	0.21	13.1	9.4	7.9	7.3
FBVA900	31 x 31	XCKU035	2.5	0.03	10.5	6.8	5.7	5.3
		XCKU040	2.5	0.03	10.5	6.8	5.7	5.3
FFVA1156	35 x 35	XCKU025	2.5	0.21	9.5	5.9	5.0	4.6
		XCKU035	2.5	0.21	9.5	5.9	5.0	4.6
		XCKU040	2.5	0.21	9.5	5.9	5.0	4.6
		XCKU060	1.9	0.15	8.9	5.7	4.7	4.5
		XCKU095	1.7	0.10	8.8	5.6	4.7	4.4
RFA1156	35 x 35	XQKU040	3.0	0.26	9.9	6.1	5.1	4.8
		XQKU060	2.6	0.18	9.6	6.0	5.0	4.7
		XQKU095	2.3	0.12	9.3	5.9	4.9	4.6
FFVA1517	40 x 40	XCKU060	1.9	0.15	7.9	4.8	4.1	3.8
FLVA1517	40 x 40	XCKU085	1.7	0.10	7.8	4.8	4.0	3.8
		XCKU115	1.7	0.10	7.8	4.8	4.0	3.8
FFVC1517	40 x 40	XCKU095	1.7	0.10	7.8	4.8	4.0	3.8
FLVD1517	40 x 40	XCKU115	1.7	0.10	7.8	4.8	4.0	3.8
RLD1517	40 x 40	XQKU115	2.1	0.10	7.4	4.3	3.6	3.9
FFVB1760	42.5 x 42.5	XCKU095	1.7	0.10	7.4	4.5	3.7	3.5
FLVB1760	42.5 x 42.5	XCKU085	1.7	0.10	7.4	4.4	3.7	3.5
		XCKU115	1.7	0.10	7.4	4.4	3.7	3.5
FLVD1924	45 x 45	XCKU115	1.7	0.10	7.0	4.2	3.5	3.3

Table 10-1: **Thermal Resistance Data *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)[2]	θ_{JC} (°C/W)[2]	θ_{JA} (°C/W)[2]	$\theta_{JA\text{-}Effective}$ (°C/W)[1][2]		
						@250 LFM	@500 LFM	@750 LFM
FLVF1924	45 x 45	XCKU085	1.7	0.10	7.0	4.2	3.5	3.3
		XCKU115	1.7	0.10	7.0	4.2	3.5	3.3
RLF1924	45 x 45	XQKU115	2.1	0.10	7.4	4.3	3.6	3.4
FLVA2104	47.5 x 47.5	XCKU115	1.7	0.10	6.7	3.9	3.3	3.1
FFVB2104	47.5 x 47.5	XCKU095	1.7	0.10	6.7	3.9	3.3	3.1
FLVB2104	47.5 x 47.5	XCKU115	1.7	0.10	6.7	3.9	3.3	3.1
Virtex UltraScale Devices								
FFVC1517	40 x 40	XCVU065	1.7	0.18	7.8	4.8	4.0	3.8
		XCVU080	1.7	0.10	7.8	4.8	4.0	3.8
		XCVU095	1.7	0.10	7.8	4.8	4.0	3.8
FFVD1517	40 x 40	XCVU080	1.7	0.10	7.8	4.8	4.0	3.8
		XCVU095	1.7	0.10	7.8	4.8	4.0	3.8
FLVD1517	40 x 40	XCVU125	1.6	0.09	7.7	4.7	4.0	3.7
FFVB1760	42.5 x 42.5	XCVU080	1.7	0.10	7.4	4.5	3.7	3.5
		XCVU095	1.7	0.10	7.4	4.5	3.7	3.5
FLVB1760	42.5 x 42.5	XCVU125	1.7	0.09	7.4	4.4	3.7	3.5
FFVA2104	47.5 x 47.5	XCVU080	1.7	0.10	6.7	3.9	3.3	3.1
		XCVU095	1.7	0.10	6.7	3.9	3.3	3.1
FLVA2104	47.5 x 47.5	XCVU125	1.8	0.09	6.8	3.9	3.3	3.1
FFVB2104	47.5 x 47.5	XCVU080	1.7	0.10	6.7	3.9	3.3	3.1
		XCVU095	1.7	0.10	6.7	3.9	3.3	3.1
FLVB2104	47.5 x 47.5	XCVU125	1.8	0.09	6.8	3.9	3.3	3.1
FLGB2104	47.5 x 47.5	XCVU160	1.5	0.06	6.5	3.8	3.2	3.0
		XCVU190	1.5	0.06	6.5	3.8	3.2	3.0
FFVC2104	47.5 x 47.5	XCVU095	1.7	0.10	6.7	3.9	3.3	3.1
FLVC2104	47.5 x 47.5	XCVU125	1.8	0.09	6.8	3.9	3.3	3.1
FLGC2104	47.5 x 47.5	XCVU160	1.5	0.06	6.5	3.8	3.2	3.0
		XCVU190	1.5	0.06	6.5	3.8	3.2	3.0
FLGB2377	50 x 50	XCVU440	1.4	0.05	6.2	3.6	3.0	2.8
FLGA2577	52.5 x 52.5	XCVU190	1.4	0.06	5.9	3.4	2.8	2.7
FLGA2892	55 x 55	XCVU440	1.5	0.04	5.7	3.2	2.7	2.5

Table 10-1: **Thermal Resistance Data *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)(2)	θ_{JC} (°C/W)(2)	θ_{JA} (°C/W)(2)	$\theta_{JA\text{-Effective}}$ (°C/W)(1)(2)		
						@250 LFM	@500 LFM	@750 LFM
Artix UltraScale+ Devices								
FCVA289	9 x 9	XCAU7P	3.02	0.05	32.2	30.6	25.9	23.00
		XAAU7P	3.02	0.05	32.2	30.6	25.9	23.00
UBVA368	11.5 x 9.5	XCAU10P	2.28	0.03	22.4	19.7	16.5	15.0
		XCAU15P	2.28	0.03	22.4	19.7	16.5	15.0
SBVB484	19 x 19	XCAU10P	2.46	0.06	14.9	11.5	9.6	8.9
		XAAU10P	2.46	0.06	14.9	11.5	9.6	8.9
		XCAU15P	2.46	0.06	14.9	11.5	9.6	8.9
		XAAU15P	2.46	0.06	14.9	11.5	9.6	8.9
SBVC484	19 x 19	XCAU7P	2.46	0.06	14.9	11.5	9.6	8.9
		XAAU7P	2.46	0.06	14.9	11.5	9.6	8.9
FFVB676	27 x 27	XCAU10P	2.07	0.25	10.2	7.1	6.0	5.6
		XAAU10P	2.07	0.25	10.2	7.1	6.0	5.6
		XCAU15P	2.07	0.25	10.2	7.1	6.0	5.6
		XAAU15P	2.07	0.25	10.2	7.1	6.0	5.6
		XCAU20P	2.07	0.25	10.2	7.1	6.0	5.6
		XCAU25P	2.07	0.25	10.2	7.1	6.0	5.6
SFVB784	23 x 23	XCAU20P	2.06	0.25	11.9	8.7	7.3	6.9
		XCAU25P	2.06	0.25	11.9	8.7	7.3	6.9
Kintex UltraScale+ Devices								
FFVA676	27 x 27	XCKU3P	2.07	0.25	10.2	7.1	6.0	5.6
		XCKU5P	2.07	0.25	10.2	7.1	6.0	5.6
FFVB676	27 x 27	XCKU3P	2.07	0.25	10.2	7.1	6.0	5.6
		XCKU5P	2.07	0.25	10.2	7.1	6.0	5.6
FFRB676	27 x 27	XQKU5P	2.26	0.27	10.4	7.3	6.1	5.7
SFVB784	23 x 23	XCKU3P	2.06	0.25	11.9	8.7	7.3	6.9
		XCKU5P	2.06	0.25	11.9	8.7	7.3	6.9
SFRB784	23 x 23	XQKU5P	2.06	0.25	11.9	8.7	7.3	6.9
FFVD900	31 x 31	XCKU3P	2.22	0.26	9.0	6.1	5.1	4.8
		XCKU5P	2.22	0.26	9.0	6.1	5.1	4.8
		XCKU11P	1.83	0.14	8.7	5.9	4.9	4.6
FFVE900	31 x 31	XCKU9P	2.33	0.25	9.2	6.1	5.1	4.9
		XCKU13P	2.25	0.18	9.1	6.1	5.1	4.8

Table 10-1: **Thermal Resistance Data *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)[2]	θ_{JC} (°C/W)[2]	θ_{JA} (°C/W)[2]	$\theta_{JA\text{-Effective}}$ (°C/W)[1][2]		
						@250 LFM	@500 LFM	@750 LFM
FFVA1156	35 x 35	XCKU11P	1.97	0.14	7.8	5.1	4.2	4.0
		XCKU15P	1.69	0.10	7.6	5.0	4.1	3.9
FFRA1156	35 x 35	XQKU15P	1.92	0.11	7.7	5.1	4.2	4.0
FFVE1517	40 x 40	XCKU11P	1.96	0.14	6.8	4.3	3.6	3.4
		XCKU15P	1.76	0.10	6.6	4.2	3.5	3.4
FFRE1517	40 x 40	XQKU15P	1.90	0.11	6.8	4.3	3.5	3.4
FFVA1760	42.5 x 42.5	XCKU15P	1.77	0.10	6.3	3.9	3.2	3.1
FFVE1760	42.5 x 42.5	XCKU15P	1.77	0.10	6.3	3.9	3.2	3.1
FFVJ1760	42.5 x 42.5	XCKU19P	1.81	0.09	6.3	3.9	3.3	3.1
FFVB2104	47.5 x 47.5	XCKU19P	1.85	0.09	5.7	3.4	2.8	2.7
Spartan UltraScale+ Devices								
CMVA361	9 x 9	XCSU10P	3.24	0.09	29.7	27.1	22.9	20.5
		XCSU25P	3.24	0.09	29.7	27.1	22.9	20.5
		XCSU35P	3.24	0.09	29.7	27.1	22.9	20.5
CMVA529	11 x 11	XCSU10P	3.13	0.09	24.8	21.4	18.1	16.4
		XCSU25P	3.13	0.09	24.8	21.4	18.1	16.4
		XCSU35P	3.13	0.09	24.8	21.4	18.1	16.4
SBVB625	21 x 21	XCSU10P	3.82	0.09	17.2	11.9	10.0	9.2
		XCSU25P	3.82	0.09	17.2	11.9	10.0	9.2
		XCSU35P	3.82	0.09	17.2	11.9	10.0	9.2
Virtex UltraScale+ Devices								
VSVA1365	35 x 35	XCVU23P	2.33	0.01	8.2	5.3	4.4	4.2
FFVC1517	40 x 40	XCVU3P	1.82	0.14	6.7	4.2	3.5	3.4
FFRC1517	40 x 40	XQVU3P	1.95	0.14	6.8	4.3	3.6	3.4
FSVJ1760	42.5 x 42.5	XCVU23P	2.33	0.09	6.8	4.2	3.5	3.3
FLGF1924	45 x 45	XCVU11P	1.48	0.07	5.7	3.5	2.9	2.8
FSVH1924	45 x 45	XCVU31P	2.10	0.04	6.2	3.8	3.1	3.0
FLVA2104	47.5 x 47.5	XCVU5P	1.69	0.09	5.5	3.3	2.8	2.7
		XCVU7P	1.69	0.09	5.5	3.3	2.8	2.7
FLRA2104	47.5 x 47.5	XQVU7P	1.69	0.09	5.5	3.3	2.8	2.7

Table 10-1: **Thermal Resistance Data *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)[2]	θ_{JC} (°C/W)[2]	θ_{JA} (°C/W)[2]	$\theta_{JA\text{-}Effective}$ (°C/W)[1][2]		
						@250 LFM	@500 LFM	@750 LFM
FLGA2104	47.5 x 47.5	XCVU9P	1.45	0.06	5.4	3.3	2.7	2.6
FHGA2104	52.5 x 52.5	XCVU13P	1.45	0.05	5.4	3.3	2.7	2.6
FLVB2104	47.5 x 47.5	XCVU5P	1.69	0.09	5.5	3.3	2.8	2.7
		XCVU7P	1.69	0.09	5.5	3.3	2.8	2.7
FLRB2104	47.5 x 47.5	XQVU7P	1.69	0.09	5.5	3.3	2.8	2.7
FLGB2104	47.5 x 47.5	XCVU9P	1.45	0.06	5.4	3.3	2.7	2.6
		XCVU11P	1.53	0.07	5.5	3.3	2.7	2.6
FHGB2104	52.5 x 52.5	XCVU13P	1.45	0.05	5.4	3.3	2.7	2.6
FLVC2104	47.5 x 47.5	XCVU5P	1.69	0.09	5.5	3.3	2.8	2.7
		XCVU7P	1.69	0.09	5.5	3.3	2.8	2.7
FLGC2104	47.5 x 47.5	XCVU9P	1.45	0.06	5.4	3.3	2.7	2.6
		XCVU11P	1.53	0.07	5.5	3.3	2.7	2.6
FLRC2104	47.5 x 47.5	XQVU11P	1.53	0.07	5.5	3.3	2.7	2.6
FHGC2104	52.5 x 52.5	XCVU13P	1.45	0.05	5.4	3.3	2.7	2.6
FIGD2104	52.5 x 52.5	XCVU13P	1.54	0.01	7.6	4.4	3.6	3.3
		XCVU27P	1.54	0.01	7.6	4.4	3.6	3.3
		XCVU29P	1.54	0.01	7.6	4.4	3.6	3.3
FSGD2104	47.5 x 47.5	XCVU9P	1.66	0.01	7.8	4.8	3.9	3.5
		XCVU11P	1.63	0.01	7.9	4.9	4.0	3.7
FSVH2104	47.5 x 47.5	XCVU33P	2.10	0.03	5.9	3.5	2.9	2.8
		XCVU35P	1.78	0.02	5.6	3.4	2.8	2.7
		XCVU45P	1.78	0.02	5.6	3.4	2.8	2.7
FLGA2577	52.5 x 52.5	XCVU9P	1.61	0.06	5.0	2.9	2.4	2.3
		XCVU11P	1.70	0.07	5.0	2.9	2.5	2.4
		XCVU13P	1.63	0.05	5.0	2.9	2.4	2.4
FSGA2577	52.5 x 52.5	XCVU13P	1.61	0.01	7.6	4.4	3.6	3.3
FSGA2577	52.5 x 52.5	XCVU27P	1.61	0.01	7.6	4.4	3.6	3.3
		XCVU29P	1.61	0.01	7.6	4.4	3.6	3.3
FSVH2892	55 x 55	XCVU35P	1.91	0.02	4.9	2.9	2.4	2.3
		XCVU37P	1.72	0.01	4.8	2.8	2.2	2.2
		XCVU45P	1.91	0.02	4.9	2.9	2.4	2.3
		XCVU47P	1.72	0.01	4.8	2.8	2.2	2.2
FSVK2892	55 x 55	XCVU57P	1.72	0.01	4.8	2.8	2.2	2.2
FSVA3824	65 x 65	XCVU19P	1.58	0.002	4.0	2.2	1.83	1.78

Table 10-1: **Thermal Resistance Data *(Cont'd)***

Package	Package Body Size	Devices	θ_{JB} (°C/W)[2]	θ_{JC} (°C/W)[2]	θ_{JA} (°C/W)[2]	$\theta_{JA\text{-}Effective}$ (°C/W)[1][2]		
						@250 LFM	@500 LFM	@750 LFM
FSVB3824	65 x 65	XCVU19P	1.58	0.002	4.0	2.2	1.83	1.78

Notes:

1. All $\theta_{JA\text{-}Effective}$ values assume no heat sink and include thermal dissipation through a standard JEDEC four-layer board. The power estimation tools (Vivado Power Analysis and Power Estimator), which require detailed board dimensions and layer counts, are useful for deriving more precise $\theta_{JA\text{-}Effective}$ values. This data is not to be used in place of thermal simulation. Instead, refer to the thermal models provided for each device.
2. This data is for device/package comparison purposes only. Attempts to recreate this data are only valid using the transient 2-phase measurement techniques outlined in JESD51-14.

Support for Thermal Models

Table 10-1 provides the traditional thermal resistance data for UltraScale and UltraScale+ devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect your actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required.

Though AMD continues to support these figure of merit data, for UltraScale and UltraScale+ devices, boundary conditions independent thermal resistor network (Delphi) models are offered for all UltraScale and UltraScale+ devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 10-1.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi models are available for download on the AMD website (under the Device Model tab).

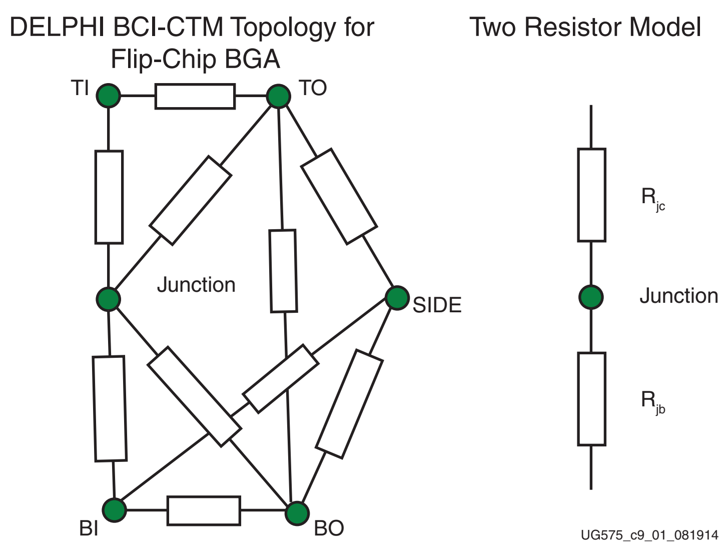

Figure 10-1: **Thermal Model Topologies**

RECOMMENDED: *AMD recommends use of the Delphi thermal model during thermal modeling of a package. The Delphi thermal model includes consideration of the thermal interface material parameters and the manufacture variation on the thermal solution. Examples of manufacture variations include the tolerance in airflow from a fan, the tolerance on performance of the heat pipe and vapor chamber, and the manufacture variation of the attachment of fins to the heat-sink base and the flatness of the surface.*

Thermal Management Strategy

Introduction

As described in this section, AMD relies on a multi-pronged approach to consuming less power and dissipating heat for systems using AMD UltraScale™ and AMD UltraScale+™ devices.

Flip-Chip Packages

UltraScale and UltraScale+ devices are offered in flip-chip BGA packages, which present a low thermal path. With the exception of the bare-die packages, the flip-chip BGA packages incorporate a heat spreader with an additional thermal interface material (TIM), as shown in Figure 11-1.

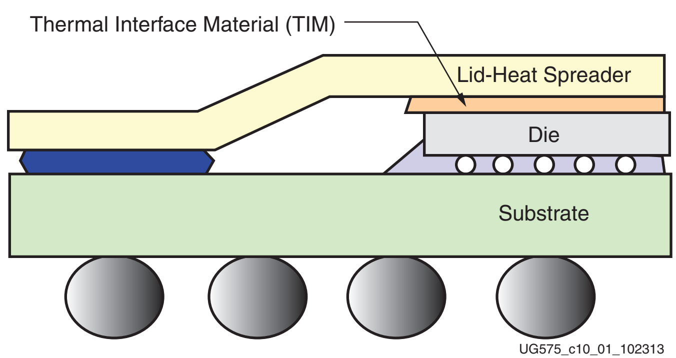

Figure 11-1: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process deliver low thermal resistance to the heat spreader.

A parallel effort to ensure optimized package electrical return paths produces the added benefit of enhanced power and ground plane arrangement in the packages. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity.

System Level Heat Sink Solutions

To complete a comprehensive thermal management strategy, an overall thermal budget that includes custom or OEM heat-sink solutions depends on the physical and mechanical constraints of the system. A heat-sink solution, managed by the system-level designer, should be tailored to the design and specific system constraints. This includes understanding the inherent device capabilities for delivering heat to the surface.

By considering the system's physical, mechanical, and environmental constraints, the overall thermal budget is maintained and does not exceed the device’s maximum operating temperature. The heat sink is an integral part of the thermal management solution to maintain a safe operating temperature. As a result, the system-level designer must be aware of the following:

- For lidless packages, the nominal stiffener height can be different from the height of the die. Therefore, the heat sink must have an island to contact the die.
- Especially for lidless packages, AMD advises against direct use of the θ_{JC} parameters (see Table 10-1) to determine the thermal performance of the device in your application. The calculation of these parameters are done in accordance with the JEDEC standard JESD51 where system parameters differ greatly from most applications. Instead, run thermal simulations of the system in worst-case environmental conditions using Delphi thermal models, which more accurately represent the device thermal performance under all boundary conditions.
- Consider the mechanical specifications of the package as well as the selection of the thermal interface between the die and the thermal management solution to ensure the lowest thermal contact resistance.
- The total thermal contact of the thermal interface material is determined based on parameters from the thermal interface supplier’s data sheet.
- See the applied pressure recommendation on page 541. Lower pressure runs the risk of poor thermal contact and higher pressure runs the risk of damaging the device; therefore, strict control of pressure is required.
- Consider all uncertainties in thermal modeling, including manufacturing variations from the thermal solutions (for example, fan airflow tolerance, heat pipe or vapor chamber performance tolerance, variation of the attachment of fins to heat sink base, and surface flatness).

Thermal Interface Material

When installing heat sinks for UltraScale or UltraScale+ devices, a suitable thermal interface material must be used. This thermal material significantly aids the transfer of heat from the component to the heat sink.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGA and lidded flip-chip BGAs are different. AMD recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

Thermal interface material is needed because even the largest heat sink and fan cannot effectively cool an UltraScale or UltraScale+ device unless there is good physical contact between the base of the heat sink and the top of the UltraScale or UltraScale+ device. The surfaces of both the heat sink and the UltraScale or UltraScale+ device silicon are not absolutely smooth. This surface roughness is observed when examined at a microscopic level. Because surface roughness reduces the effective contact area, attaching a heat sink without a thermal interface material is not sufficient due to inadequate surface contact.

A thermal interface material such as phase-change material, thermal grease, or thermal pads fills these gaps and allows effective transference of heat between the UltraScale or UltraScale+ device die and the heat sink.

The selection of the thermal interface material between the package and the thermal management solution is critical to ensure the lowest thermal contact resistance. Therefore, the following parameters must be considered.

1. The flatness of the lid and the flatness of the contact surface of the thermal solution.
2. The applied pressure of the thermal solution on the package, which must be within the allowable maximum pressure that can be applied on the package.
3. The total thermal contact of the thermal interface material. This value is determined based on the parameters in step 1 and step 2, which are published in the data sheet of the thermal interface supplier.

Types of TIM

There are many type of TIM available for sale. The most commonly used thermal interface materials are listed.

- Thermal grease
- Thermal pads
- Phase-change material
- Thermal paste
- Thermal adhesives
- Thermal tape

Guidelines for Thermal Interface Materials

Five factors affect the choice, use, and performance of the interface material used between the processor and the heat sink:

- Thermal Conductivity of the Material
- Electrical Conductivity of the Material
- Spreading Characteristics of the Material
- Long-Term Stability and Reliability of the Material
- Ease of Application
- Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Thermal Conductivity of the Material

Thermal conductivity is the quantified ability of any material to transfer heat. The thermal conductivity of the interface material has a significant impact on its thermal performance. The higher the thermal conductivity, the more efficient the material is at transferring heat. Materials that have a lower thermal conductivity are less efficient at transferring heat, causing a higher temperature differential to exist across the interface. To overcome this less efficient heat transfer, a better cooling solution (typically, a more costly solution) must be used to achieve the desired heat dissipation.

Electrical Conductivity of the Material

Some metal-based TIM compounds are electrically conductive. Ceramic-based compounds are typically not electrically conductive. Manufacturers produce metal-based compounds with low-electrical conductivity, but some of these materials are not completely electrically inert. Metal-based thermal compounds are not hazardous to an UltraScale or UltraScale+ device die itself, but other elements on an UltraScale or UltraScale+ device or the motherboard can be at risk if they become contaminated by the compound. For this reason, AMD does not recommend the use of electrically conductive thermal interface material.

Spreading Characteristics of the Material

The spreading characteristics of the thermal interface material determines its ability, under the pressure of the mounted heat sink, to spread and fill in or eliminate the air gaps between the UltraScale or UltraScale+ device and the heat sink. Because air is a very poor thermal conductor, the more completely the interface material fills the gaps, the greater the heat transference.

Long-Term Stability and Reliability of the Material

The long-term stability and reliability of the thermal interface material is described as the ability to provide a sufficient thermal conductance even after an extended time or extensive. Low-quality compounds can harden or leak out over time (the pump-out effect), leading to overheating or premature failure of the UltraScale or UltraScale+ device. High-quality compounds provide a stable and reliable thermal interface material throughout the lifetime of the device. Thermal greases with higher viscosities are typically more resistant to pump out effects on bare-die devices.

Ease of Application

A spreadable thermal grease requires the surface mount supplier to carefully use the appropriate amount of material. Too much or too little material can cause problems. The thermal pad is a fixed size and is therefore easier to apply in a consistent manner.

Applied Pressure from Heat Sink to the Package via Thermal Interface Materials

Measure applied pressure using a calibrated pressure sensor on multiple locations between the device and the heat sink assembly as shown in Figure 11-2.

Figure 11-2: **Pressure Sensor**

IMPORTANT: *The following table shows the required applied pressure on the thermal interface material (TIM) between the package and the heat sink. Thermocouples should not be present between the package and the heat sink, as their presence will degrade the thermal contact and result in incorrect thermal measurements. The best practice is to select the appropriate pressure for the optimum thermal contact performance between the package and the thermal system solution, and the mechanical integrity of the package (with the thermal solution to pass all mechanical stress and vibration qualification tests).*

Table 11-1: **Required Applied Pressure by Package Type**

Package Type	Supported Pressure Range (PSI)
0.8 mm, 0.92 mm, and 1.0 mm pitch	20 to 50 PSI
0.5 mm InFO and chip scale packages (for example: UBVA530 or CMVA529)	3 to 20 PSI

TIP: *These recommendations and specifications are the same for both lidded and lidless devices.*

RECOMMENDED: *AMD recommends using dynamic mounting around the four corners of the device package. On the PCB, use a bracket clip as part of the heat sink attachment to provide mechanical package support. See Figure 11-3.*

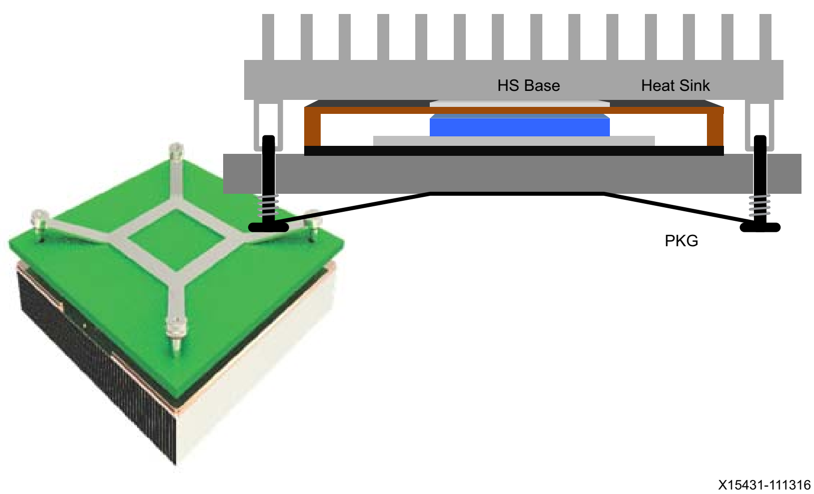

Figure 11-3: **Dynamic Mounting and Bracket Clips on Heat Sink Attachment**

Heat Sink Removal

When removing or reworking heat sinks, the phase-change material residue must be removed from the surface of the die. Laird Technologies, Inc. provides the following guidance for complete removal of the phase-change material from the component.

Instructions for Removal of Phase-change Material

1. Separate the Components
2. Scrape Away Thick Residue
3. Clean Remaining Residue with Solvent
4. Working with Laird Material

Separate the Components

At room temperature, if possible, use a back and forth twisting motion to break the bond between the phase-change thermal interface material and mated components (i.e., heat sink and FPGA). See Figure 11-4.

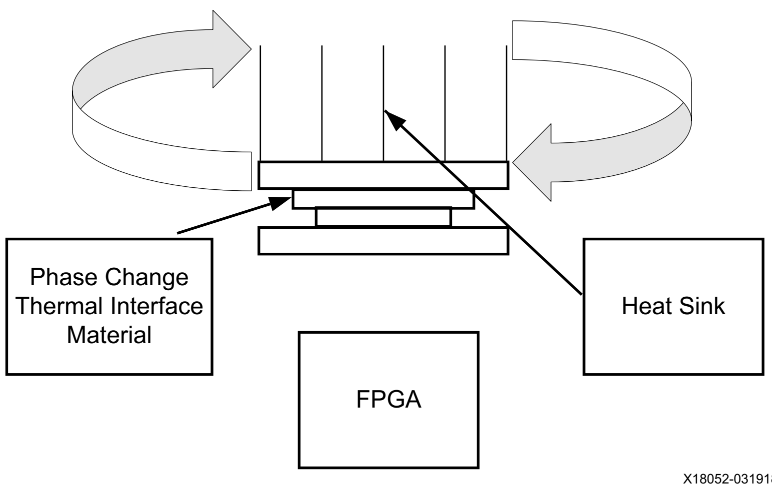

Figure 11-4: **Breaking the Bond between Thermal Interface Material and Mated Components**

For smaller components (typically 15 mm x 15 mm or less), the bond usually breaks free easily at room temperature. For larger components, in situations where minimal movement is available, or if using fragile components, heat the component (preferred) or heat sink to about 40°C–60°C before removal.

The guideline is 40°C–60°C, however, you might find that for your application, heating to 35°C is adequate. You might prefer to heat to 70°C which makes the phase-change thermal interface material very soft and the components can be easily separated.

Scrape Away Thick Residue

For a faster clean-up once components are separated, scrape away any large residual material amounts with a plastic spatula or a wooden tongue depressor. A clean dry rag can be used to wipe away excess material.

Clean Remaining Residue with Solvent

Using a clean cloth/wipe, wet it with your choice of solvent (see the following list) and wipe away any remaining residue.

- Toluene (easiest)
- Acetone (very good)
- Isoparaffinic hydrocarbon: Isopar, Soltrol (trade names) (very good)
- Isopropyl alcohol (OK)

Working with Laird Material

Safe handling, disposal, and first-aid measures for working with phase-change material are included in the Laird Technologies material safety data sheet (MSDS). Read the MSDS before using or handling. See the Laird Technologies, Inc. website, www.lairdtech.com.

Measurement Debug

When performing in-system thermal testing, to ensure accurate data and not incur damage to the device, do not place a thermocouple in between the device and the heat sink. On the extreme side, it might cause additional mechanical and/or thermal stress to the device, leading to damage. Even if damage does not occur, it often leads to a thicker and or uneven thermal interface material thickness, leading to a thermal performance difference from a system without a thermocouple. To obtain the device temperature, use the System Monitor as a non-invasive means to get accurate device measurements while debugging the system.

Chapter 12

Heat Sink Guidelines for Bare-die Flip-Chip Packages

Heat Sink Attachments for Bare-die FB Packages

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

Silicon and Decoupling Capacitors Height Consideration

When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered (Figure 12-1). This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors.

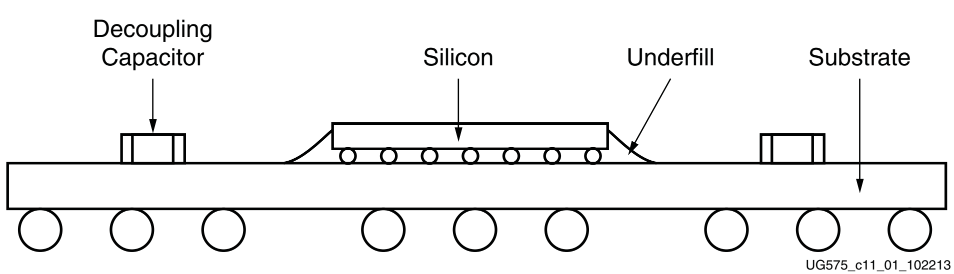

Figure 12-1: **Cross Section of Bare-die Flip-chip BGA**

Types of Heat Sink Attachments

There are six main methods for heat sink attachment. Table 12-1 lists their advantages and disadvantages.

- Thermal tape
- Thermally conductive adhesive or glue
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs

Table 12-1: **Heat Sink Attachment Methods**

Attachment Method	Advantages	Disadvantages
Thermal tape	• Generally easy to attach and is inexpensive. • Lowest cost approach for aluminum heat sink attachment. • No additional space required on the PCB.	• The surfaces of the heat sink and the chip must be very clean to allow the tape to bond correctly. • Because of the small contact area, the tape might not provide sufficient bond strength. • Tape is a moderate to low thermal conductor that could affect the thermal performance.
Thermally conductive adhesive or glue	• Outstanding mechanical adhesion. • Fairly inexpensive, costs a little more than tape. • No additional space required on the PCB.	• Adhesive application process is challenging and it is difficult to control the amount of adhesive to use. • Difficult to rework. • Because of the small contact area, the adhesive might not provide sufficient bond strength.
Wire form Z-clips	• It provides a strong and secure mechanical attachment. In environments that require shock and vibration testing, this type of strong mechanical attachment is necessary. • Easy to apply and remove. Does not cause the semiconductors to be destroyed (epoxy and occasionally tape can destroy the device). • It applies a preload onto the thermal interface material (TIM). Pre-loads actually improve thermal performance.	• Requires additional space on the PCB for anchor locations.

Table 12-1: **Heat Sink Attachment Methods *(Cont'd)***

Attachment Method	Advantages	Disadvantages
Plastic clip-ons	• Suitable for designs where space on the PCB is limited. • Easy to rework by allowing heat sinks to be easily removed and reapplied without damaging the PCB board. • Can provide a strong enough mechanical attachment to pass shock and vibration test.	• Needs a keep out area around the silicon devices to use the clip. • Caution is required when installing or removing clip-ons because localized stress can damage the solder balls or chip substrate.
Threaded stand-offs (PEMs) and compression springs	• Provides stable attachments to heat source and transfers load to the PCB, backing plate, or chassis. • Suitable for high mass heat sinks. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Holes are required in the PCB taking valuable space that can be used for trace lines. • Tends to be expensive, especially since holes need to be drilled or predrilled onto the PCB board to use stand-offs.
Push-pins and compression springs	• Provides a stable attachment to a heat source and transfers load to the PCB. • Allows for tight control over mounting force and load placed on chip and solder balls.	• Requires additional space on the PCB for push-pin locations.

Heat Sink Attachment

Component Pick-up Tool Consideration

For pick-and-place machines to place bare-die flip-chip BGAs onto PCBs, AMD recommends using soft tips or suction cups for the nozzles. This prevents chipping, scratching, or even cracking of the bare die (Figure 12-2).

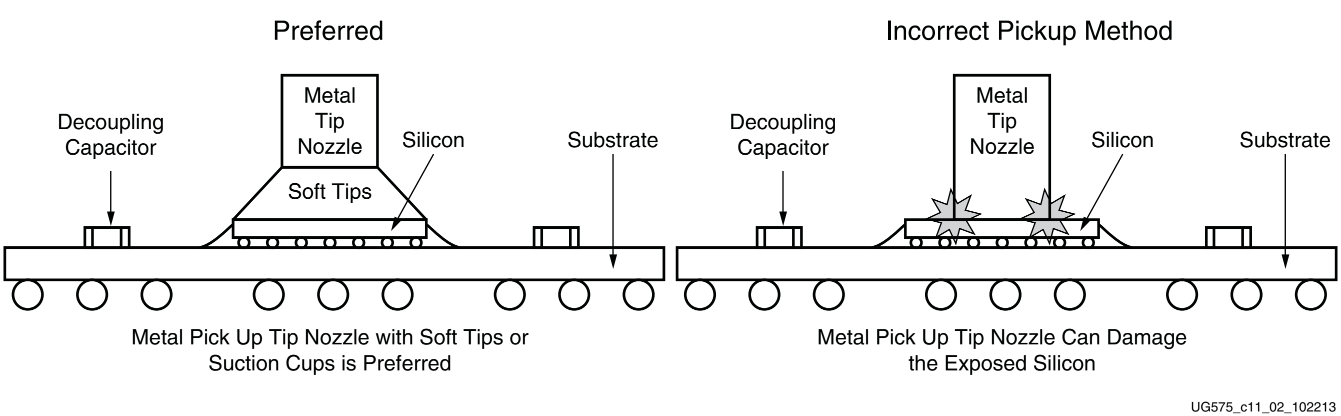

Figure 12-2: **Recommended Method For Using Pick-up Tools**

Heat Sink Attachment Process Considerations

After the component is placed onto the PCBs, when attaching a heat sink to the bare-die package, the factors in Table 12-2 must be carefully considered (see Figure 12-3).

Table 12-2: **Heat Sink Attachment Considerations**

Consideration(s)	Effect(s)	Recommendation(s)
In heat sink attach process, what factors can cause damage to the exposed die and passive capacitors?	• Uneven heat sink placement • Uneven TIM thickness • Uneven force applied when placing heat sink placement	• Even heat sink placement • Even TIM thickness • Even force applied when placing heat sink placement
Does the heat sink tilt or tip the post attachment?	Uneven heat sink placement will damage the silicon and can cause field failures.	• Careful handling not to contact the heat sink with the post attachment. • Use a fixture to hold the heat sink in place with post attachment until it is glued to the silicon.

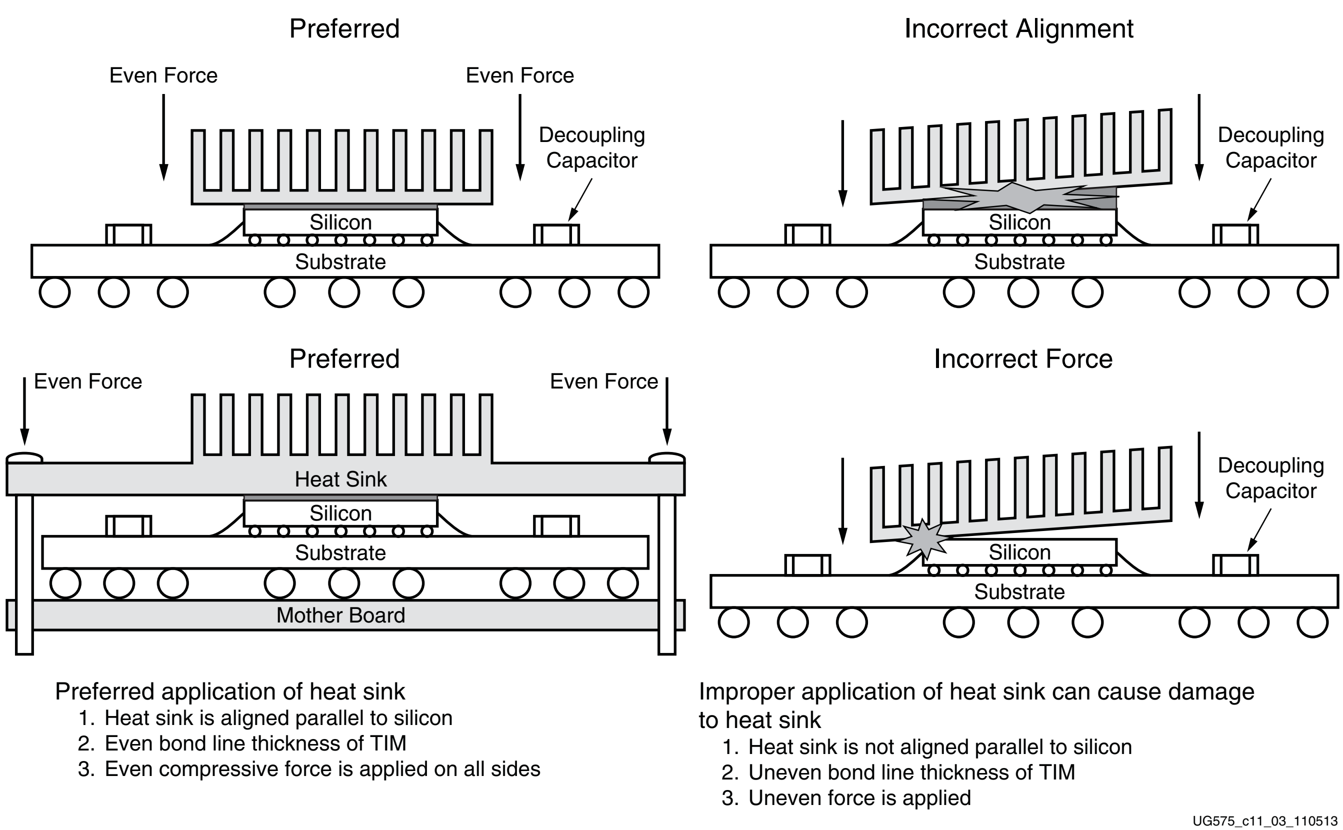

Figure 12-3: **Recommended Application of Heat Sink**

Standard Heat Sink Attach Process with Thermal Conductive Adhesive

Prior to attaching the heat sink, the UltraScale or UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermoset material (electrically non-conductive) is applied over the backside surface of silicon in a pattern using automated dispensing equipment. Automated dispensers are often used to provide a stable process speed at a relatively low cost. The optimum dispensing pattern needs to be determined by the SMT supplier.

   Note: Minimal volume coverage of the backside of the silicon can result in non-optimum heat transfer.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the adhesive spreads to cover the backside silicon. A force transducer is normally used to measure and limit the placement force.
4. The epoxy is cured with heat at a defined time.

   Note: The epoxy curing temperature and time is based on manufacturer's specifications.

Standard Heat Sink Attach Process with Thermal Adhesive Tape

Prior to attaching the heat sink, the UltraScale or UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.
2. Thermal adhesive tape cut to the size of the heat sink is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.
3. The heat sink is placed on the backside of the silicon with a pick and place machine. A uniform pressure is applied over the heat sink to the backside of the silicon. As the heat sink is placed, the thermal adhesive tape is glued to the backside of the silicon. A force transducer is normally used to measure and limit the placement force.
4. A uniform and constant pressure is applied uniformly over the heat sink and held for a defined time.

   Note: The thermal adhesive tape hold time is based on manufacturer's specifications.

Push-Pin and Shoulder Screw Heat Sink Attachment Process with Phase Change Material (PCM) Application

Prior to attaching the heat sink, the UltraScale or UltraScale+ device needs be surface mounted on the motherboard.

1. Place the motherboard into a jig or a fixture to hold the motherboard steady to prevent any movement during the heat sink attachment process.

   Note: The jig or fixture needs to account for the push pin depth of the heat sink.

2. PCM tape, cut to the size of the heat sink, is applied on the underside of the heat sink at a modest angle with the use of a squeegee rubber roller. Apply pressure to help reduce the possibility of air entrapment under the tape during application.

3. Using the push-pin tool, heat sinks are applied over the packages ensuring a pin locking action with the PCB holes. The compression load from springs applies the appropriate mounting pressure required for proper thermal interface material performance.

   Note: Heat sinks must not tilt during installation. This process cannot be automated due to the mechanical locking action which requires manual handling. The PCB drill hole tolerances need to be close enough to eliminate any issues concerning the heat sink attachment.

Chapter 13

Mechanical and Thermal Design Guidelines for Lidless Flip-chip Packages

Introduction

This chapter discusses the challenges of thermal management including reducing device thermal resistance and optimal power dissipation without an increase in junction temperature. The lidless UltraScale+ FPGA packages target the largest devices while allowing for cooler operation temperatures (up to 10°C) with the same power dissipation.

Precise mechanical design and component thermal management is vital for device and system performance. This document presents the unique thermal and mechanical design requirements for lidless devices.

Lidless Flip-Chip Packages

The AMD flip-chip BGA packages exhibit a low-resistance thermal path that adequately cools devices. These packages incorporate a heat spreader lid with additional thermal interface material (Figure 13-1).

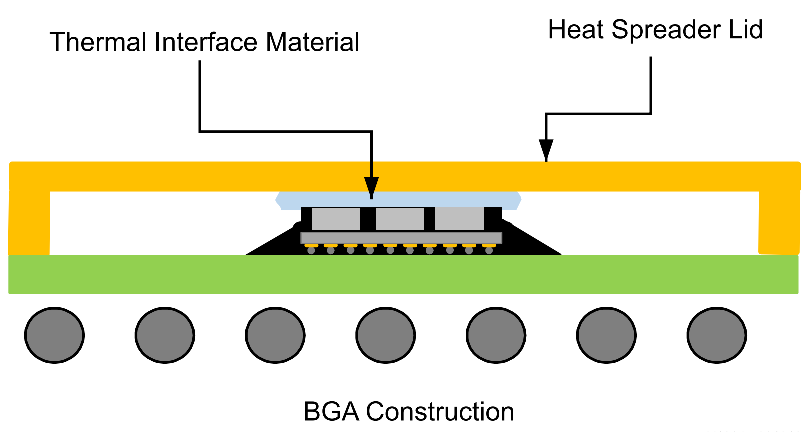

Figure 13-1: **Flip-Chip BGA Construction with Heat Spreader and Thermal Interface Material**

Materials with high thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. A parallel effort to ensure optimized package electrical return paths produces an enhanced power and ground plane arrangement in the package. A boost in copper density on the planes improves the overall thermal conductivity through the laminate. The extra density and distribution via fields in the package also increases the vertical thermal conductivity.

The lidless packages (Figure 13-2) offer the same package substrate design with electrical and board thermal conductivity similar to the flip-chip BGA packages. However, removing the lid (heat spreader) and the thermal interface material allows for direct contact between the external heat sink and the die. This further reduces the thermal resistance and exhibits improved thermal behaviors. The use of custom passive or active heat-sink designs is facilitated by incorporating two-phase (heat pipe, vapor chamber, or even liquid) cooling methods directly adjacent to the source of the dissipated heat on the die, which allows for a more efficient means of removing the heat from the device. Consequently, the device can operate at higher ambient temperatures while in area-constrained surroundings resulting in operational power advantages.

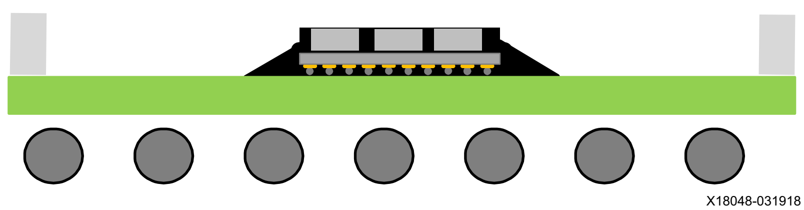

Figure 13-2: **Lidless Flip-Chip BGA Construction**

A unique feature of lidless packages is the addition of a stiffener ring around the periphery of the package substrate, providing additional package rigidity and helping to improve the overall package coplanarity (flatness). It also serves as a guide for the heat sink solution applied to the device. For examples, see Figure 4-56, Figure 4-57, and Figure 4-58.

In the lidless packages, capacitors can be placed in the area surrounding the die. Contact with electrically conductive materials must be avoided because the die-side capacitors, which are only slightly shorter than the die height, could be electrically conductive. Any thermal and mechanical solution higher than the die must not interfere with the package stiffener. Therefore, the thermal solution must have an island, see System Level Heat Sink Solutions in Chapter 11.

For further guidelines on mechanical and thermal designs of lidless packages, refer to *Mechanical and Thermal Design Guidelines for Lidless Flip-Chip Packages Application Note* (XAPP1301).

Appendix A

Additional Resources and Legal Notices

Finding Additional Documentation

Technical Information Portal

The AMD Technical Information Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Technical Information Portal, go to https://docs.amd.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help > Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools > DocNav**.
- At the Linux command prompt, enter `docnav`.

Note: For more information on DocNav, refer to the Documentation Navigator User Guide (UG968).

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the Design Hubs web page.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

1. *UltraScale Architecture and Product Overview* (DS890)
2. *XQ UltraScale Architecture Data Sheet Overview* (DS895)
3. UltraScale Device Data Sheets
    - *Spartan UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics* (DS930)
    - *Kintex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS892)
    - *Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics* (DS893)
    - *Artix UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS931)
    - *Kintex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS922)
    - *Virtex UltraScale+ FPGAs Data Sheet: DC and AC Switching Characteristics* (DS923)
    - *Radiation Tolerant Kintex UltraScale XQRKU060 FPGA Data Sheet* (DS882)
4. *Zynq UltraScale+ MPSoC Packaging and Pinouts User Guide* (UG1075)
5. *UltraScale Architecture SelectIO Resources User Guide* (UG571)
6. *UltraScale Architecture Clocking Resources User Guide* (UG572)
7. *UltraScale Architecture Configuration User Guide* (UG570)
8. *UltraScale Architecture GTH Transceivers User Guide* (UG576)
9. *UltraScale Architecture GTY Transceivers User Guide* (UG578)
10. *UltraScale Architecture System Monitor User Guide* (UG580)
11. *UltraScale Architecture PCB and Pin Planning User Guide* (UG583)
12. *Spartan UltraScale+ FPGAs Configuration User Guide* (UG860)
13. *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424)
14. *UltraScale Architecture FPGAs Memory IP Product Guide* (PG150)
15. *UltraScale Devices Gen3 Integrated Block for PCI Express Product Guide* (PG156)
16. *UltraScale+ Devices Integrated Block for PCI Express Product Guide* (PG213)
17. *Integrated Interlaken 150G Product Guide* (PG169)
18. *UltraScale Devices Integrated Block for 100G Ethernet Product Guide* (PG165)
19. *UltraScale+ Devices Integrated 100G Ethernet Subsystem Product Guide* (PG203)
20. *Mechanical and Thermal Design Guidelines for Lidless Flip-Chip Packages Application Note* (XAPP1301)

21. MDDS files: Click on this link to find the UltraScale and UltraScale+ FPGA Packaging Specifications. In step 2 select the product category: FPGAs and 3D ICs. In step 3, select the product type. In step 4, click on the package specifications selection to find the available MDDS files.
22. The following websites contain additional information on heat management and contact information.
    - Wakefield: www.wakefield-vette.com
    - Aavid: www.aavid.com
    - Advanced Thermal Solutions: www.qats.com
    - Radian Thermal Products: www.radianheatsinks.com
    - Thermo Cool: www.thermocoolcorp.com
    - CTS: www.ctscorp.com
23. Refer to the following websites for interface material sources:
    - Henkel: www.henkel.com
    - Bergquist Company: www.bergquistcompany.com
    - AOS Thermal Compound: www.aosco.com
    - Chomerics: www.chomerics.com
    - Kester: www.kester.com
24. Refer to the following websites for CFD tools AMD supports with thermal models.
    - Mentor Flotherm: www.mentor.com/products/mechanical/flotherm/flotherm/
    - ANSYS Icepak: www.ansys.com
25. Refer to the thermal device models.
26. The following papers are referenced for more information on thermal modelling.
    - Lemczyk, T.F., Mack, B., Culham, J.R. and Yovanovich, M.M., 1992, “Printed Circuit Board Trace Thermal Analysis and Effective Conductivity”, ASME J. Electronic Packaging, Vol. 114, pp. 413 - 419.50.
    - Refai-Ahmed, G. and Karimanal, K., 2003, “Validation of Compact Conduction Models of BGA Under Realistic Boundary,” J. of Components and Packaging Technology, Vol. 26, No. 3, pp. 610-615.
    - Sansoucy, E, Refai-Ahmed, G., and Karimanal, K., 2002, “Thermal Characterization of TBGA Package for an integration in Board Level Analysis,” Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego., USA.
    - Karimanal,K and Refai-Ahmed, G., and., 2002, “Validation of Compact Conduction Models of BGA Under Realistic Boundary Conditions,” Eighth Intersociety on Thermal Conference Phenomena in Electronic Systems, San Diego, USA.

- Karminal, K. and Refai-Ahmed, G., 2001, "Compact conduction Model (CCM) of Microelectronic Packages- A BGA Validation Study," APACK Conference on Advance in Packaging, Singapore.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
7/31/2025	1.21	Added XCSU10P, XCSU25P, and XCSU35P devices and the CMVA361, CMVA529, and SBVB625 packages throughout the guide.
		In Chapter 3, added Table 3-6 and the images presented in this table.
		In Chapter 4, added Figure 4-2, Figure 4-6, Figure 4-7, and updated the ZD/ZE values in Figure 4-3.
		In Chapter 5, updated all the device families to include the AMD top mark.
10/04/2024	1.20	Added the XCAU7P and XAAU7P in the FCVA289 package throughout the guide.
		Added notes to VCCAUX_IO pins for XQ devices to Figure 3-103, Figure 3-105, Figure 3-117, and Figure 3-121.
		Fixed Zd/Ze dimensions in Figure 4-3.
		Updated the 0.5 mm pitch values in Table 8-1 for the maximum PCB solder land (L) diameter and opening in PCB solder mask (M) diameter design rules.
		Updated Underfill Guidelines in Chapter 9.
		Updated notes for Applied Pressure from Heat Sink to the Package via Thermal Interface Materials.
5/10/2023	1.19	Added the XCAU7P and XAAU7P in the SBVC484 package throughout the guide.
		Added the XAAU10P and XAAU15P devices in SBVB484 and FFVB676 packages.
		Changed the HP total user I/O and differential I/O for the XCKU095-FFVB1760, XCKU115-FFVB1760, XCKU115-FLVB2104 in Table 1-5.
		Updated Uniform Stencil Aperture Design and added the Non-Uniform (Bull's Eye) Stencil Aperture Design section.
		Updated the Edge Bonding Implementation section and added the Underfill Guidelines section.

Date	Version	Revision
4/22/2022	1.18	Added the following Artix UltraScale+ FPGA specifications throughout the guide: • XCAU10P in the UBVA368, SBVB484, and FFVB676 packages • XCAU15P in the UBVA368, SBVB484, and FFVB676 packages Updated the type of pin for the User I/O Pins. Updated XCKU19P-FFVB2104 I/O mapping in Table 1-8 and Figure 1-107. Updated the package status in Table 2-1, Table 3-3, Table 3-4, Table 3-5, and Table 4-1. Updated Package Dimensions for FSVH2104 (XCVU35P and XCVU45P). Updated for clarity Package Dimensions for FSVH2104 (XCVU35P and XCVU45P) in Chapter 4. Added an Important note on page 444 about BGA balls replaced by capacitors (LSC). Moved the Conformal Coating section to Chapter 9, Edge Bonding and Underfill Guidelines. Updated the Process Parameters for Edge Bonding table and the Edge Bonding Adhesive Placement Parameters figure to include InFO package values. Updated the recommended curing conditions on page 519.
9/01/2021	1.17	Revised the design of the XCAU20P Bank Diagrams in Figure 1-76, Figure 1-77, and Figure 1-78. Also updated Table 1-8 with revised banks. Updated Table 3-5 to add the FFVB676 (XCAU20P) section.
8/05/2021	1.16	Added the following Artix UltraScale+ FPGA specifications throughout the guide: • XCAU20P in the SFVB784 and FFVB676 packages • XCAU25P in the SFVB784 and SFVB784 packages Added note below Figure 1-140: XCVU23P Banks in VSVA1365 Package, page 175. Corrected a pin error in Figure 3-193 and Figure 3-195. Added a Tip on the MDDS file information to the Mechanical Drawings Summary.
1/21/2020	1.15	Added the following specifications throughout the guide: • XCVU23P in the VSVA1365 and FSVJ1760 packages • XCKU19P in FFVJ1760 and FFVB2104 packages • XCVU57P in the FSVK2892 package Chapter 4: Added Table 4-2 and updated the following mechanical drawings: • FSVH1924 (XCVU31P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA • FSVH2104 (XCVU33P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA • FSVH2104 (XCVU35P and XCVU45P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA • FSVH2892 (XCVU35P and XCVU45P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA • FSVH2892 (XCVU37P and XCVU47P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA • FSVA3824 and FSVB3824 (XCVU19P) Flip-Chip, Fine-Pitch, Lidless with Stiffener Ring, BGA Chapter 7: Removed the *Typical Conditions for IR Reflow Soldering of Ceramic Column Grid Array Packages* section, including Figure 7-2, because the *Radiation Tolerant Kintex UltraScale XQRKU060 FPGA Data Sheet* (DS882) has this content. Chapter 8: Updated the Stencil section. Chapter 10: Updated the *Important* note in the Thermal Resistance Data section.

Date	Version	Revision
3/18/2020	1.14	Updated Table 2-1, Table 3-4, and Table 4-1 XCVU19P (FSVA3824 and FSVB3824 packages) to production. Chapter 5: Updated definitions in Table 5-1 for when the bar code contains the mark information. Updated Figure 5-2, Figure 5-3, Figure 5-4, and Figure 5-5 with the updated mark images. Chapter 7: Added the *Typical Conditions for IR Reflow Soldering of Ceramic Column Grid Array Packages* section. Updated the Pb-Free Reflow Soldering section including adding Table 7-2 and Table 7-3, changes to Table 7-4 (mass reflow), heating rate recommendations, and other discussions including adding photos of thermocouples. Updated the Conformal Coating recommendation. Added a Strain Gauge Measurement section, moved and updated the Solder Paste section, and added the Component Placement section. Chapter 8: Updated the BGA Packages section, added the Stencil section, and moved the Solder Paste section. Chapter 9: Added the Component Clearance Surrounding Edge Bond section and updated the Edge Bond Removal section. Chapter 11: Updated the Applied Pressure from Heat Sink to the Package via Thermal Interface Materials section.
9/27/2019	1.13	Added XCVU19P (FSVA3824 and FSVB3824 packages). Added the XCVU45P (FSVH2104 and FSVH2892) and XCVU47P (FSVH2892) devices/package combinations to appropriate tables and chapters. Chapter 1: Added Table 1-9: I/O Bank Migration for VU19P devices: HP I/O Banks are Unshaded and HD I/O Banks are in Dark Gray. Updated Figure 1-134 GTY Quad power supply designations on the right side. Chapter 3: Updated Figure 3-181, Figure 3-182, Figure 3-183, and Figure 3-184. Chapter 7: Revised the maximum peak temperature range from 240°C–250°C to 245°C–250°C. Chapter 8: Updated discussions, added the Bull's Eye Stencil Recommendation section with Figure 8-4 and the Solder Paste section. Chapter 9: Added chapter.

Date	Version	Revision
3/20/2019	1.12	Chapter 1: Added an Important note about XQ devices with eutectic BGA balls on page 12. Added the XQKU5P (FFRB676, SFRB784), XQKU15P (FFRA1156, FFRE1517), XQVU3P (FFRC1517), XQVU7P (FLRA2104, FLRB2104), and XQVU11P (FLRC2104) device/package combinations to Table 1-1, Table 1-2, Table 1-5, Table 1-7, Table 1-8, Table 1-10, Table 1-10, and the appropriate figures in the Device Diagrams section. In Table 1-6, corrected D[*04 to 31]* configuration data pins label and added note to VCCAUX_IO. Revised the XCVU31P Bank Diagrams, XCVU33P Bank Diagrams, XCVU35P and XCVU45P Bank Diagrams, XCVU37P and XCVU47P Bank Diagrams and to show the correct PCIE4 and PCIE4C banks.Added the XCVU27P (FIGD2104, FSGA2577) and XCVU29P (FIGD2104, FSGA2577) devices. This includes adding Table 1-3 and updates to Table 1-1, Table 1-5, Table 1-6, Table 1-7, Table 1-8, Table 1-10, and the appropriate figures in the Device Diagrams section. Updated the XCVU27P Bank Diagrams. Chapter 2: Added an Important note about XQ devices with eutectic BGA balls on page 200. In Table 2-1, added the XCVU27P (FIGD2104, FSGA2577) and XCVU29P (FIGD2104, FSGA2577) devices and the XQKU5P (FFRB676, SFRB784), XQKU15P (FFRA1156, FFRE1517), XQVU3P (FFRC1517), XQVU7P (FLRA2104, FLRB2104), and XQVU11P (FLRC2104) device/package combinations. Chapter 3: Added an Important note about XQ devices with eutectic BGA balls on page 205. In Table 3-3, added the XQKU5P (FFRB676, SFRB784), XQKU15P (FFRA1156, FFRE1517) device/package combinations. In Table 3-4, added the XCVU27P (FIGD2104, FSGA2577), XCVU29P (FIGD2104, FSGA2577), XQVU3P (FFRC1517), XQVU7P (FLRA2104, FLRB2104), and XQVU11P (FLRC2104) device/package combinations. Chapter 4: Added to the Summary information on XQ devices with eutectic BGA balls and updated Table 4-1 with the packages specific to the XQ versions. In Table 4-1, added the mechanical drawings for the XQKU5P (FFRB676, SFRB784), XQKU15P (FFRA1156, FFRE1517), XQVU3P (FFRC1517), XQVU7P (FLRA2104, FLRB2104), and XQVU11P (FLRC2104), and updated the FIGD2104 and FSGA2577 drawings to add the XCVU27P and XCVU29P. Chapter 5: Added Figure 5-6 and updated Table 5-1. Chapter 6: Updated Table 6-1 with the FSGA2577 package and the XQ packages (FFRB676, SFRB784, FFRA1156, FFRC1517, FFRE1517, FLRA2104, FLRB2104, FLRC2104). Added an Important note about XQ devices with eutectic BGA balls on page 499. Chapter 7: Updated the Sn/Pb reflow soldering guidelines including changes to Figure 7-2. Added the FSGA2577 package and the XQ packages (FFRB676, SFRB784, FFRA1156, FFRC1517, FFRE1517, FLRA2104, FLRB2104, FLRC2104) to Table 7-4 and added Note 2. Updated the Conformal Coating section. Chapter 10: Added an Important note about XQ devices with eutectic BGA balls on page 530. Updated Table 10-1 with new data. Although the same information was already in Note 2 at the end of Table 10-1, it is repeated in an additional Important note on page 529. Added an Important note about XQ devices with eutectic BGA balls on page 530. In Table 10-1, revised FFVE900 values, added the XCVU27P (FIGD2104, FSGA2577), XCVU29P (FIGD2104, FSGA2577), XQKU5P (FFRB676, SFRB784), XQKU15P (FFRA1156, FFRE1517), XQVU3P (FFRC1517), XQVU7P (FLRA2104, FLRB2104), and XQVU11P (FLRC2104) device/package data. Also added data to the XCVU31P, XCVU33P, XCVU35P, and XCVU37P devices. Chapter 11: Updated applied pressure range in Recommended note on page 541 to 20–50 psi.

Date	Version	Revision
8/23/2018	1.11	Chapter 1: In Table 1-6, updated the GC or HDGC direction to Input/Output. In Table 1-10, updated the XCVU160-FLGB2104 map to change the 233 quad location and added the 233 and 133 quads to XCVU160-FLGC2104 map. Chapter 2: In Table 2-1, updated the XCVU31P-FSVH1924, XCVU33P/XCVU35P-FSVH2104, XCVU13P-FSGA2577, and XCVU35P/XCVU37P-FSVH2892 to production and revised the links. Chapter 3: In Table 3-4, updated the XCVU31P-FSVH1924, XCVU33P/XCVU35P-FSVH2104, XCVU13P-FSGA2577, and XCVU35P/XCVU37P-FSVH2892 to production. Chapter 4: In Table 4-1, updated the mechanical drawing status for XCVU31P-FSVH1924, XCVU33P/XCVU35P-FSVH2104, XCVU13P-FSGA2577, and XCVU35P/XCVU37P-FSVH2892 to production. Chapter 10: In Table 10-1, added the XCVU31P-FSVH1924, XCVU33P/XCVU35P-FSVH2104, XCVU13P-FSGA2577, and XCVU35P/XCVU37P-FSVH2892 devices.
4/09/2018	1.10	Chapter 1: Updated the Bank Locations of Dedicated and Multi-Function Pins section. Added the XCVU13P-FSGA2577 device/package combination and the XCVU31P, XCVU33P, XCVU35P, and XCVU37P devices. This includes updates to Table 1-1, Table 1-2, Table 1-5, Table 1-6, Table 1-7, Table 1-8, and Table 1-10. Added Figure 1-148, Figure 1-149, Figure 1-150, Figure 1-151, Figure 1-152, Figure 1-153, Figure 1-154, Figure 1-155, and Figure 1-156. Chapter 2: Added the XCVU13P-FSGA2577 device/package combination and the XCVU31P, XCVU33P, XCVU35P, and XCVU37P devices to Table 2-1. Chapter 3: Added the XCVU13P-FSGA2577 device/package combination and the XCVU31P, XCVU33P, XCVU35P, and XCVU37P devices to Table 3-4. Chapter 4: Added the XCVU13P-FSGA2577 device/package combination and the XCVU31P, XCVU33P, XCVU35P, and XCVU37P devices to Table 4-1. Chapter 6: Added the FSVH1924, FSVH2104, FSGA2577, and FSVH2892 packages to Table 6-1. Chapter 7: Added the FSVH1924, FSVH2104, FSGA2577, and FSVH2892 packages to Table 7-4. Chapter 10: Added the XCVU13P-FSGA2577 device/package combination and the XCVU31P, XCVU33P, XCVU35P, and XCVU37P devices to Table 10-1. Chapter 13: Added a link to *Mechanical and Thermal Design Guidelines for Lidless Flip-Chip Packages Application Note (XAPP1301)*.
12/15/2017	1.9	Chapter 2, Package Files: Updated links and package designations in Table 2-1. Chapter 3, Device Diagrams: Updated package designations in Table 3-3 and Table 3-4. Added Figure 3-109, Figure 3-110, Figure 3-163, and Figure 3-164. Chapter 4, Mechanical Drawings: Updated package designations in Table 4-1. Added Figure 4-56. Updated Figure 4-57 (the dimensions inside the Top View changed). Added Figure 4-58. Chapter 10, Thermal Specifications: Added Note 2 to Table 10-1. Chapter 11, Thermal Management Strategy updated the System Level Heat Sink Solutions and Heat Sink Removal sections. Added the Measurement Debug section. Chapter 13, Mechanical and Thermal Design Guidelines for Lidless Flip-chip Packages was added to user guide.

Date	Version	Revision
8/25/2017	1.8	Chapter 1, Packaging Overview: In Table 1-5, corrected (increased) the available HP I/O pin counts for the XCKU095-FFVB2104. In Table 1-6, revised the VCCINT_IO description. In Table 1-8, updated the XCKU5P-FFVB676 mapping and added the XCKU095-FFVC1517. Added at Tip on page 61. Updated bank designations in Figure 1-8, Figure 1-13, Figure 1-15, Figure 1-28, Figure 1-32, Figure 1-35, all XCVU080 Bank Diagrams, XCVU095 Bank Diagrams, Figure 1-52, XCKU9P Bank Diagrams, Figure 1-96, XCKU13P Bank Diagrams, and XCKU15P and XQKU15P Bank Diagrams. Chapter 2, Package Files: Updated links and package designations in Table 2-1. Chapter 3, Device Diagrams: Updated package designations in Table 3-3 and Table 3-4. Added Figure 3-115 and Figure 3-116. Updated Figure 3-119 and Figure 3-120. Added Figure 3-143, Figure 3-144, Figure 3-157, Figure 3-158, Figure 3-165, and Figure 3-166. Chapter 4, Mechanical Drawings: Updated package designations in Table 4-1. Chapter 5, Package Marking: Updated the Top Marks for Figure 5-2 and Figure 5-3 to show the date code and lot number on the bar code version. Added package types to Table 5-1. Chapter 6, Packing and Shipping: Added package types to Table 6-1. Chapter 7, Soldering Guidelines: Added guidelines for lidless packages with stiffener ring and updated Table 7-1. Revised the Mass Reflow from 250°C to 245°C on a number of package types in Table 7-4. Revised Figure 7-2 with new guidelines. Chapter 10, Thermal Specifications: Added package types to Table 10-1. Added Documentation Navigator in Appendix A.
4/27/2017	1.7.1	Replaced the FFVE1760 (XCKU15P) figures in Chapter 3, Device Diagrams.
4/26/2017	1.7	Added the XQKU040, XQKU060, XQKU095, and XQKU115 devices where applicable. Added the RBA676, RFA1156, RLD1517, and RLF1924 packages where applicable. Chapter 1, Packaging Overview: Updated Note 5 in Table 1-6. Revised Table 1-7, Table 1-8, and Table 1-10. Added notes and recommendations to the SYSMON, Configuration, PCIe, Interlaken, and 100GE Integrated Blocks section. Revised many of the Device Diagrams. Chapter 2, Package Files: Updated the links. Added and updated package files for Virtex UltraScale+ and Kintex UltraScale+ FPGAs. Chapter 3, Device Diagrams: Added and updated diagrams for Virtex UltraScale+ and Kintex UltraScale+ FPGAs. Chapter 4, Mechanical Drawings: Added and replaced many of the mechanical drawings for the Virtex UltraScale+ and Kintex UltraScale+ devices. Chapter 5, Package Marking: Updated the Virtex UltraScale and Kintex UltraScale device top-mark diagrams to include the bar code top-mark diagrams. Added the Virtex UltraScale+ and Kintex UltraScale+ device top-mark diagrams. Chapter 7, Soldering Guidelines: Added the Sn/Pb Reflow Soldering section. Updated the Conformal Coating recommendation.

Date	Version	Revision
4/25/2016	1.6	Added Kintex UltraScale+ and Virtex UltraScale+ FPGAs. Chapter 1, Packaging Overview: Revised GC or HDGC description and added RSVDGND to Table 1-6. Revised the Die Level Bank Numbering Overview section including adding and replacing figures and removing tables. Chapter 2, Package Files: Updated the links. Chapter 3, Device Diagrams: Corrected Figure 3-7 and Figure 3-8. Chapter 4, Mechanical Drawings: Updated top-lid flat-surface dimension from 31.05 sq. max. to 29.70sq. max. in Figure 4-19 (FFVA1156). Updated the top-lid flat-surface dimension from 29.10 max. to 29.70 sq. max. in Figure 4-20 (FFVA1156) and Figure 4-21 (FFVA1156). Added top-lid flat-surface dimension 33.10 in Figure 4-26 (FFVA1517). Update dimension A nominal from 3.61 to 3.51 in Figure 4-32 (FFVB1760). Updated Figure 4-49 (FLGB2104) to add a missing decimal point. Updated Figure 4-52 (FFVC2104) with the correct package dimensions. Chapter 7, Soldering Guidelines: Updated the device list in Table 7-4. Chapter 11, Thermal Management Strategy: Added a new recommendation and Figure 11-3.
10/19/2015	1.5	Added the XCKU025 and the XCKU095 in the FFVA1156 package. In Chapter 1, Packaging Overview, updated SFVA784 package in Table 1-8, Table 1-9 and Table 1-10. Updated the FLVB1760 rows in Table 1-10.Added an important note in Footprint Compatibility between Packages. Replaced Figure 1-13. In Chapter 3, Device Diagrams, replaced the SFVA784 drawings in Figure 3-3 and Figure 3-4 with updated pinouts. Updated Figure 3-43 and Figure 3-44. In Chapter 4, Mechanical Drawings, updated Figure 4-13 (SFVA784) and Figure 4-20 (FFVA1156), and corrected the heading for Figure 4-49 to include FLGB2104 and FLGC2104. Replaced Figure 4-49, Figure 4-61, Figure 4-62, and Figure 4-66. In Chapter 8, Recommended PCB Design Rules for BGA Packages, updated Table 8-1. In Chapter 10, Thermal Specifications, added thermal resistance data to Table 10-1. Substantial edits to the Introduction, Thermal Resistance Data, and Support for Thermal Models sections. Added a new recommendation on page 536. In Chapter 11, Thermal Management Strategy, removed *Design and Silicon* section, updated the Flip-Chip Packages and System Level Heat Sink Solutions sections, removed the *Thermal Management Options* section, added more information to Types of TIM, removed the *Comparing the Types of Interface Materials* section, added the Applied Pressure from Heat Sink to the Package via Thermal Interface Materials section, and removed the *Package Pressure Handling Capacity* section. In Chapter 12, Heat Sink Guidelines for Bare-die Flip-Chip Packages, removed the *Package Loading Specifications* section.
5/13/2015	1.4	Added the XCKU035 and XCKU040 devices in the SFVA784 package throughout this guide. Added XCKU085 and XCKU095 updates throughout including Table 1-8, Table 1-10, and Table 3-1. In Chapter 1, Packaging Overview, in Table 1-6 changed D01_DIN_0, D02_0, and D03_0 to bidirectional. Updated Figure 1-9 to Figure 1-14 with new GTH Quad placements. In Chapter 4, Mechanical Drawings, updated Table 4-1 and the specific mechanical drawings of the SFVA784, FBVA900, FLVA1517, FLVD1517, FLVB1760, FLVA2104, FLVB2104, FLGB2104, FFVC2104, FLVC2104, and FLGC2104.

Date	Version	Revision
3/23/2015	1.3	Updated the Differences from Previous Generations section. In Table 1-6, updated VCCINT and VCCAUX descriptions and the Multi-gigabit Serial Transceiver Pins (GTHE3 and GTYE3) section. Updated the Die Level Bank Numbering Overview section including adding the SYSMON, Configuration, PCIe, Interlaken, and 100GE Integrated Blocks section. Replaced Figure 1-4 through Figure 1-62 and updated information in Table 1-9 through Table 1-21. Removed the XCKU075 and XCKU100 throughout. Added the XCKU085 and XCKU095 where data is available. In Chapter 2, Package Files, updated the links to the ASCII files. In Chapter 3, Device Diagrams, updated Figure 3-13, Figure 3-14 and added numerous new figures. In Chapter 4, Mechanical Drawings, removed the FBVA900 mechanical drawings and updated Figure 4-29. In Chapter 5, Package Marking, added to the 2nd line description in Table 5-1. Revised Table 10-1.
1/12/2015	1.2	Revised the device/package combinations per the update to the *UltraScale Architecture and Product Overview* (DS890) [Ref 1]. This revision was throughout the guide in every table with package listings, Package Files, Device Diagrams, and Mechanical Drawings. Updated Table 1-16, Table 1-17, and replaced Table 1-18, Table 1-19, and Table 1-20. Updated descriptions in Table 5-1. Updated descriptions in Table 7-4. Revised and added to Table 10-1. Added references to Appendix A.

Date	Version	Revision
9/04/2014	1.1	Added a discussion on ULA materials on page 11. In Differences from Previous Generations, updated the differential clock pin pairs and the VREF pin discussion. Added the Virtex UltraScale FPGA packages to Table 1-1. Also added the Virtex UltraScale devices to Table 1-2, Table 1-5, and Table 1-7. Updated PERSTN[*0 to 1*], DOUT_CSO_B, FWE_FCS2_B, RS[*0 to 1*], RDWR_FCS_B_0, D00_MOSI_0, D01_DIN_0, and VREF_[bank number] descriptions. Updated Multi-gigabit Serial Transceiver Pins (GTHE3 and GTYE3) pin names. Added Table 1-8 and Table 1-10. Revised the T[*0 to 3*][*U or L*] and N[*0 to 12*] descriptions in the User I/O Pins section of Table 1-6: Pin Definitions. Updated the figures and added tables to the Die Level Bank Numbering Overview section. Changed the TXT and CSV files associated with Table 2-1. Also updated Table 2-1 with additional device/packages and links. In Chapter 3, Device Diagrams, replaced or added figures. Added Figure 4-8 through Figure 4-4. Replaced Figure 4-19 and Figure 4-20. Added Figure 4-26 through Figure 4-13. Added the Virtex UltraScale device package marking template to Chapter 5. Clarified the maximum reflow soldering guidelines on page 500 and updated Table 7-4: Peak Package Reflow Body Temperature(1). Replaced Figure 7-2. Removed the *Sn/Pb Reflow Soldering* section from Chapter 7, Soldering Guidelines. Added Post Reflow/Cleaning/Washing and Conformal Coating sections. Updated *Thermal Management Options* and Figure 10-2. Added Heat Sink Removal and *Package Pressure Handling Capacity* to Chapter 11. Updated the links to references [Ref 22], [Ref 23], and [Ref 24] in Appendix A. Added further references.
12/10/2013	1.0	Initial AMD release.

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