# RTL8326

# 24-PORT 10/100M + 2-PORT 10/100/1000M ETHERNET SWITCH CONTROLLER WITH EMBEDDED MEMORY

## DATASHEET

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## USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 1.8 | 2003/05/15 | First external release. |
| 1.9 | 2003/08/08 | Add AC/DC characteristics and mechanical information. |
| 2.0 | 2003/9/17 | Add thermal data |
| 2.1 | 2003/11/27 | Add digital timing characteristics diagram |

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# 1. General Description

The RTL8326 is a layer-2 switch controller that integrates 2.5Mbits of high-speed SSRAM, an 8K-entry MAC address lookup table, 24 Ethernet/Fast Ethernet MACs, two Gigabit Ethernet MACs, and a switch engine into one chip.

The Remote Management Tool (RMT) software package is bundled with the RTL8326. The RMT is a Windows-based tool developed to enhance the functionality of Realtek's dumb layer 2 switches via software. The RMT gives network administrators the ability to remotely configure and monitor dumb layer 2 switches as though they were intelligent switches. With QoS, Trunking, VLAN, bandwidth control, remote control, and an 0.18µm process, the RTL8326 is a cost effective switch controller for a 24+2G dumb or smart switch application.

Port trunking is supported on all ports to increase bandwidth. Load balancing and fault tolerance provide top performance and reliability. The RTL8326 provides 2-level priority queues for multimedia or real-time network applications. The CoS (Class of Service) can be port-based, IEEE 802.1p tag-based, and/or TCP/IP header TOS/DS field based. The RTL8326 supports up to 32 VLAN groups that may be configured as port-based VLANs and/or IEEE 802.1Q tagged VLANs. ARP broadcast and Leaky VLAN are also supported.

The RTL8326 features a built-in PCS (Physical Coding Sublayer) to support a SERDES (serializer/deserializer) transceiver for Gigabit fiber applications. For diagnostics/analysis, RX byte count, RX packet count, TX byte count, TX packet count, CRC error packet count, collision packet count, drop packet count, and drop byte counters are included. The RTL8326 supports TX and RX bandwidth control on each port. 128Kbps, 256Kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, and 8Mbps may be selected in each direction.

A loop-detection function is provided to notify if a network loop exists, either via a visual LED, or via a register flag for smart applications. LED displays for broadcast storm, trunking status, flow control, and traffic utilization are also provided.

Maximum packet length can be up to 1552 bytes. A filtering function of the 802.1D specified reserved group MAC addresses according to pin strapping upon reset or register setting is supported for flexible proprietary applications.

The RTL8326 supports IEEE 802.3x full duplex flow control and back pressure half duplex flow control. Full duplex flow control can be disabled manually or automatically to ensure QoS control or bandwidth control works correctly. Broadcast storm filtering prevents network crashes caused by abnormal broadcast activity.

As well as supporting 802.3u auto-negotiation, the RTL8326 supports PHY Read/Write registers to access PHY registers through an MDC/MDIO interface. This expands system configuration options. In-band management of the functions provided by the RTL8326 may be implemented using a simple 8051 microprocessor, or via the RTL8326's RRCP® protocol based Remote Management Tool (RMT).

The RTL8326 is designed with a link-list buffer management architecture and provides 8.8Gbps of bandwidth to achieve wire-speed performance. It also has an intelligent switching engine to prevent Head-of-Line blocking. Only a single 25MHz crystal is required for clock generation.

# 2. Features

- 24 10/100Mbps + 2 10/100/1000Mbps port layer-2 Ethernet switch controller with embedded lookup table and packet buffer
- Supports SMII on 10/100Mbps ports
- Supports MII, GMII, or TBI on Giga-ports
  - ◆ Complies with 802.3z and 802.3ab
  - ◆ Half/full duplex for MII
  - ◆ Full duplex for GMII/TBI
  - ◆ Built-in PCS for SERDES transceiver
- Built-in 8K entry MAC address lookup table plus 64-entry CAM to eliminate hash collision problems
- Built-in 2.5Mbit SSRAM packet buffer
- Non-blocking wire-speed forwarding and filtering (8.8Gbps throughput)
- Store and forward architecture and head-of-line blocking prevention
- All ports support Speed, Duplex, and 802.3x flow-control ability auto-negotiation
- Supports broadcast storm filtering control
- Supports 802.3x full duplex flow control and back pressure half duplex flow control
- Supports Trunking function with load balancing and fault tolerance for 10/100M ports and Gigabit ports
- Supports up to 32 VLAN groups for port-based VLAN and 802.1Q tag VLAN
- Supports Leaky VLAN
- Two priority queues for three types of Class of Service (CoS)
  - ◆ Port- based 802.1p priority tag
  - ◆ TCP/IP header's TOS/DS classifier
- Weighted round robin queue scheduling
- Priority tag insert and remove function
- Supports ASIC based IGMP snooping function
- Supports pin strapping, EEPROM, or serial CPU configuration interface
- Supports PHY register read/write access
- Supports Realtek Remote Control Protocol (RRCP®) for in-band configuration and management
- Supports SMII/GMII interface I/O delay control
- Supports simple MIB counters
- TX/RX packet/byte, CRC error, and collision counter for diagnostics/statistics
- Supports per-port bandwidth control
- Supports loop detection and indication function
- Provides serial LED and parallel LED interface for port properties and diagnostic display
- Needs only one low cost 25MHz crystal or OSC input
- 0.18µm, 208-pin PQFP, 3.3V single power, 5V I/O tolerance

# 3. Block Diagram

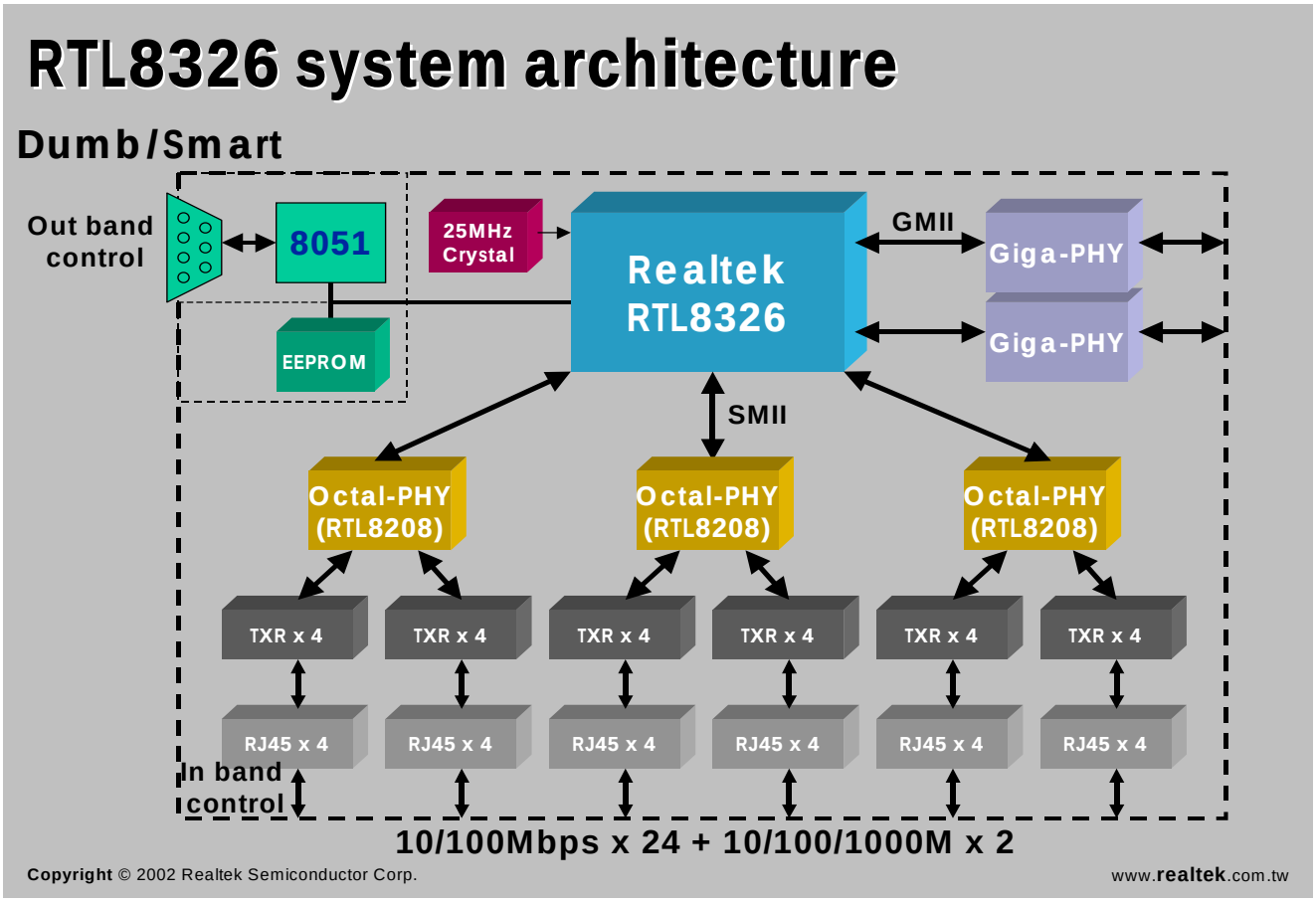



**Figure 1. Block Diagram**

# 4. Functional Block Diagram

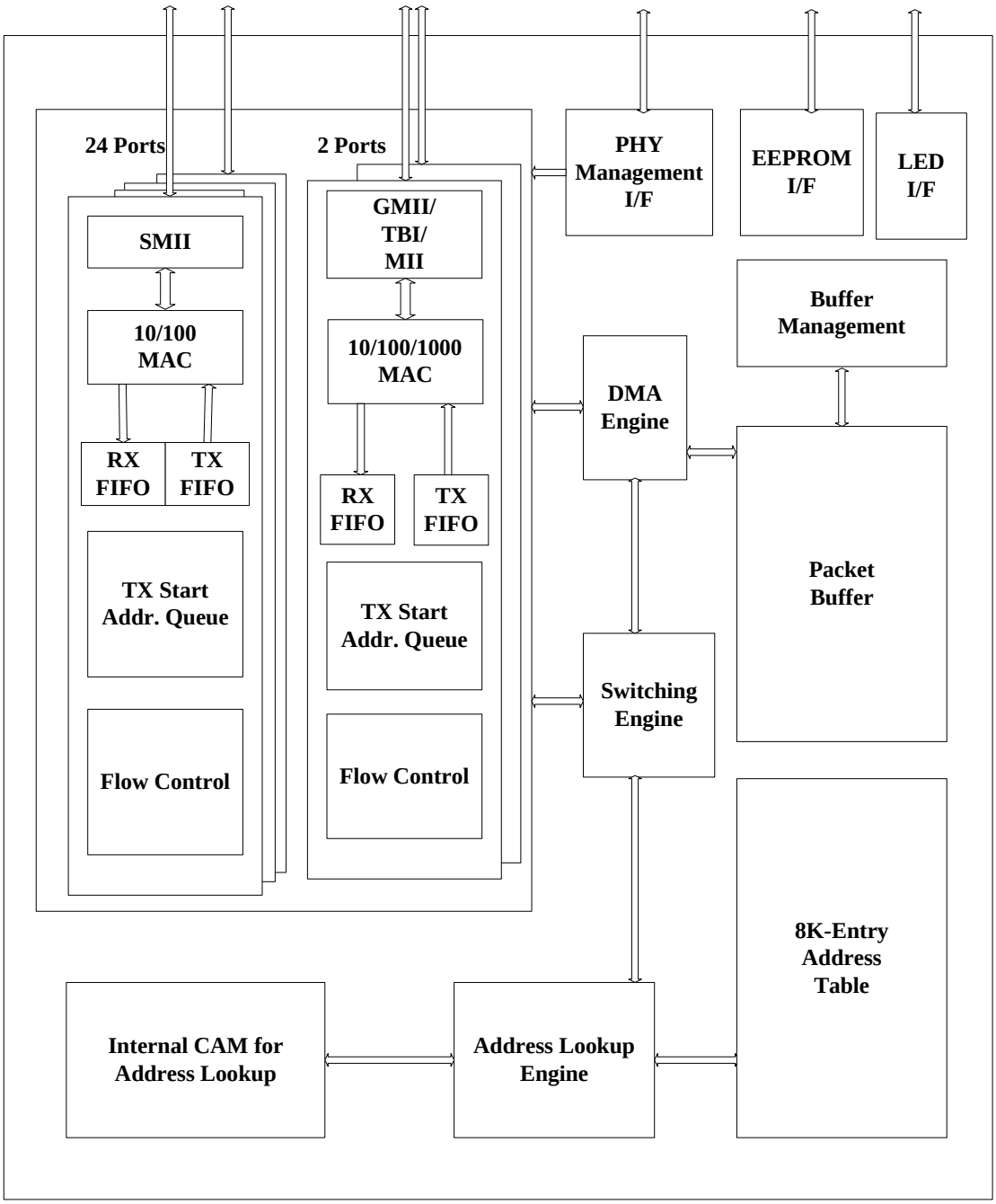



**Figure 2. Functional Block Diagram**

# 5. Pin Assignments

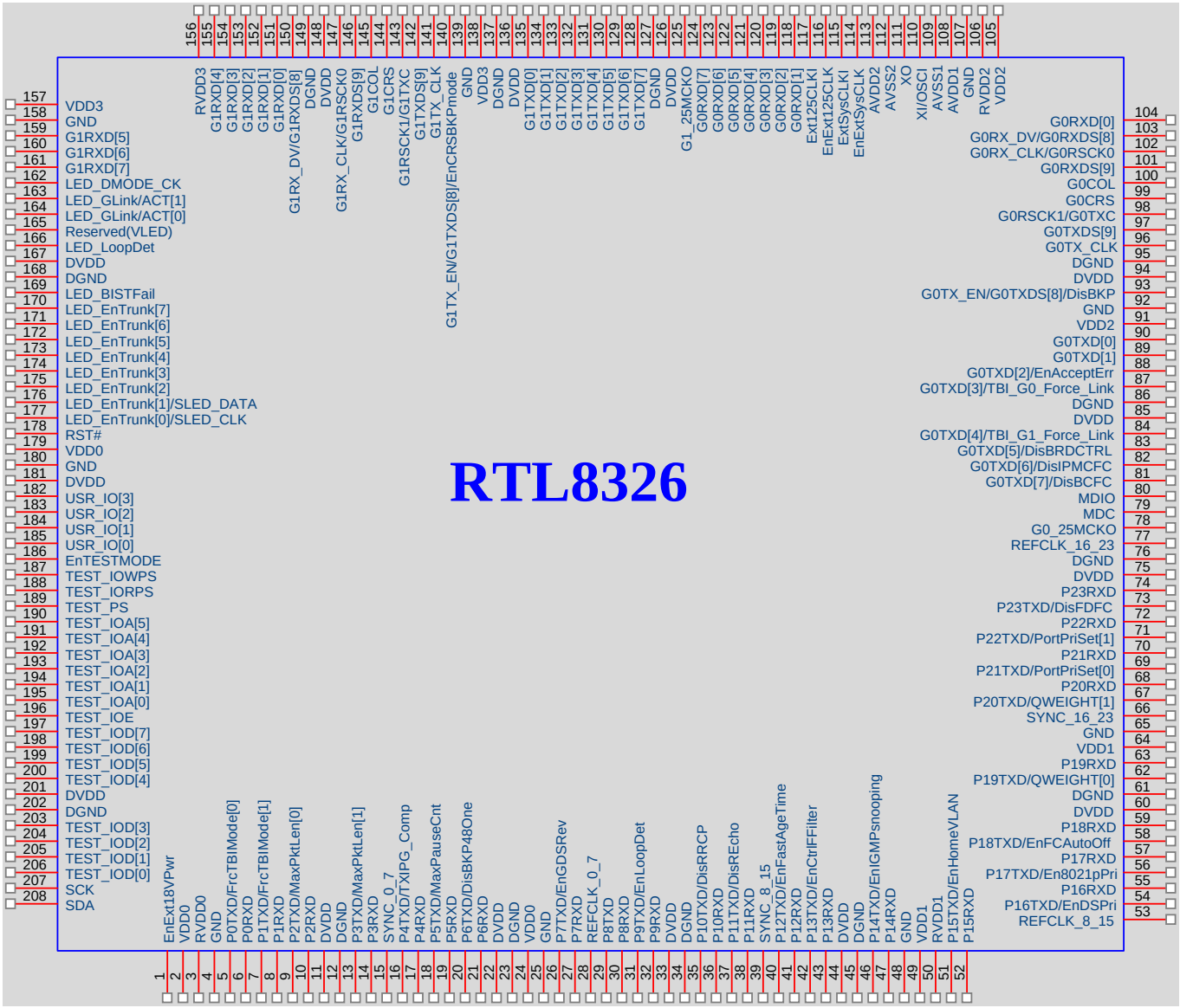



**Figure 3. Pin Assignments**

# 5.1. Pin Assignment Table (208-Pin PQFP)

Type codes used: P = Power; G = Ground, I = Input, O = Output.

**Table 1. Pin Assignments (1 ~ 104)**

| Pin # | Signal Name | Type | Pin # | Signal Name | Type |
|---|---|---|---|---|---|
| 1 | EnExt18VPwr | I | 53 | REFCLK_8_15 | O |
| 2 | VDD0 | P | 54 | P16TXD/(EnDSPri) | O |
| 3 | RVDD0 | P | 55 | P16RXD | I |
| 4 | GND | G | 56 | P17TXD/(En8021pPri) | O |
| 5 | P0TXD/(FrcTBIMode[0]) | O | 57 | P17RXD | I |
| 6 | P0RXD | I | 58 | P18TXD/(EnFCAutoOff) | O |
| 7 | P1TXD/(FrcTBIMode[1]) | O | 59 | P18RXD | I |
| 8 | P1RXD | I | 60 | DVDD | P |
| 9 | P2TXD/(MaxPktLen[0]) | O | 61 | DGND | G |
| 10 | P2RXD | I | 62 | P19TXD/(QWEIGHT[0]) | O |
| 11 | DVDD | P | 63 | P19RXD | I |
| 12 | DGND | G | 64 | VDD1 | P |
| 13 | P3TXD/( MaxPktLen[1]) | O | 65 | GND | G |
| 14 | P3RXD | I | 66 | SYNC_16_23 | O |
| 15 | SYNC_0_7 | O | 67 | P20TXD/(QWEIGHT[1]) | O |
| 16 | P4TXD/(TXIPG_Comp) | O | 68 | P20RXD | I |
| 17 | P4RXD | I | 69 | P21TXD/(PortPriSet[0]) | O |
| 18 | P5TXD/(MaxPauseCnt) | O | 70 | P21RXD | I |
| 19 | P5RXD | I | 71 | P22TXD/(PortPriSet[1]) | O |
| 20 | P6TXD/(DisBKP48One) | O | 72 | P22RXD | I |
| 21 | P6RXD | I | 73 | P23TXD/(DisFDFC) | O |
| 22 | DVDD | P | 74 | P23RXD | I |
| 23 | DGND | G | 75 | DVDD | P |
| 24 | VDD0 | P | 76 | DGND | G |
| 25 | GND | G | 77 | REFCLK_16_23 | O |
| 26 | P7TXD/(EnGDSRev) | O | 78 | G0_25MCKO | O |
| 27 | P7RXD | I | 79 | MDC | O |
| 28 | REFCLK_0_7 | O | 80 | MDIO | IO |
| 29 | P8TXD | O | 81 | G0TXD[7]/(DisBCFC) | O |
| 30 | P8RXD | I | 82 | G0TXD[6]/(DisIPMCFC) | O |
| 31 | P9TXD/(EnLoopDet) | O | 83 | G0TXD[5]/(DisBRDCTRL) | O |
| 32 | P9RXD | I | 84 | G0TXD[4]/(TBI_G1_Force_Link) | O |
| 33 | DVDD | P | 85 | DVDD | P |
| 34 | DGND | G | 86 | DGND | G |
| 35 | P10TXD/(DisRRCP) | O | 87 | G0TXD[3]/(TBI_G0_Force_Link) | O |
| 36 | P10RXD | I | 88 | G0TXD[2]/(EnAcceptErr) | O |
| 37 | P11TXD/(DisREcho) | O | 89 | G0TXD[1]/(DisTXCRCGen) | O |
| 38 | P11RXD | I | 90 | G0TXD[0]/(EnSpdBkOff) | O |
| 39 | SYNC_8_15 | O | 91 | VDD2 | P |
| 40 | P12TXD/(EnFastAgeTime) | O | 92 | GND | G |
| 41 | P12RXD | I | 93 | G0TX_EN/G0TXDS[8] /(DisBKP) | O |
| 42 | P13TXD/(EnCtrlFFilter) | O | 94 | DVDD | P |
| 43 | P13RXD | I | 95 | DGND | G |
| 44 | DVDD | P | 96 | G0TX_CLK | O |
| 45 | DGND | G | 97 | G0TXDS[9]/(EnSPDUP) | O |
| 46 | P14TXD/(EnIGMPsnooping) | O | 98 | G0RSCK1/G0TXC | I |
| 47 | P14RXD | I | 99 | G0CRS | I |
| 48 | GND | G | 100 | G0COL | I |
| 49 | VDD1 | P | 101 | G0RXDS[9] | I |
| 50 | RVDD1 | P | 102 | G0RX_CLK/G0RSCK0 | I |
| 51 | P15TXD/(EnHomeVLAN) | O | 103 | G0RX_DV/G0RXDS[8] | I |
| 52 | P15RXD | I | 104 | G0RXD[0] | I |

**Table 2. Pin Assignments (105 ~208)**

| Pin # | Signal Name | Type | Pin # | Signal Name | Type |
|---|---|---|---|---|---|
| 105 | VDD2 | P | 157 | VDD3 | P |
| 106 | RVDD2 | P | 158 | GND | G |
| 107 | GND | G | 159 | G1RXD[5] | I |
| 108 | AVDD1 | P | 160 | G1RXD[6] | I |
| 109 | AVSS1 | P | 161 | G1RXD[7] | I |
| 110 | XI/OSCI | I | 162 | LED_DMODE_CK | O |
| 111 | XO | O | 163 | LED_GLink/ACT[1] | O |
| 112 | AVSS2 | P | 164 | LED_GLink/ACT[0] | O |
| 113 | AVDD2 | P | 165 | Reserved (VLED) | O |
| 114 | EnExtSysCLK | I | 166 | LED_LoopDet | O |
| 115 | ExtSysCLKI | I | 167 | DVDD | P |
| 116 | EnExt125CLK | I | 168 | DGND | G |
| 117 | Ext125CLKI | I | 169 | LED_BISTFail | O |
| 118 | G0RXD[1] | I | 170 | LED_EnTrunk[7] | O |
| 119 | G0RXD[2] | I | 171 | LED_EnTrunk[6] | O |
| 120 | G0RXD[3] | I | 172 | LED_EnTrunk[5] | O |
| 121 | G0RXD[4] | I | 173 | LED_EnTrunk[4] | O |
| 122 | G0RXD[5] | I | 174 | LED_EnTrunk[3] | O |
| 123 | G0RXD[6] | I | 175 | LED_EnTrunk[2] | O |
| 124 | G0RXD[7] | I | 176 | LED_EnTrunk[1]/SLED_DATA | O |
| 125 | G1_25MCKO | O | 177 | LED_EnTrunk[0]/ SLED_CLK | O |
| 126 | DVDD | P | 178 | RST# | I |
| 127 | DGND | G | 179 | VDD0 | P |
| 128 | G1TXD[7] | O | 180 | GND | G |
| 129 | G1TXD[6] | O | 181 | DVDD | P |
| 130 | G1TXD[5] | O | 182 | USR_IO[3] | I |
| 131 | G1TXD[4] | O | 183 | USR_IO[2] | I |
| 132 | G1TXD[3] | O | 184 | USR_IO[1] | I |
| 133 | G1TXD[2] | O | 185 | USR_IO[0] | I |
| 134 | G1TXD[1] | O | 186 | EnTESTMODE | I |
| 135 | G1TXD[0] | O | 187 | TEST_IOWPS | IO |
| 136 | DVDD | P | 188 | TEST_IORPS | IO |
| 137 | DGND | G | 189 | TEST_PS | IO |
| 138 | VDD3 | P | 190 | TEST_IOA[5] | IO |
| 139 | GND | G | 191 | TEST_IOA[4] | IO |
| 140 | G1TX_EN/G1TXDS[8]/(EnCRSBKPmode) | O | 192 | TEST_IOA[3] | IO |
| 141 | G1TX_CLK | O | 193 | TEST_IOA[2] | IO |
| 142 | G1TXDS[9] | O | 194 | TEST_IOA[1] | IO |
| 143 | G1RSCK1/G1TXC | I | 195 | TEST_IOA[0] | IO |
| 144 | G1CRS | I | 196 | TEST_IOE | IO |
| 145 | G1COL | I | 197 | TEST_IOD[7] | IO |
| 146 | G1RXDS[9] | I | 198 | TEST_IOD[6] | IO |
| 147 | G1RX_CLK/G1RSCK0 | I | 199 | TEST_IOD[5] | IO |
| 148 | DVDD | P | 200 | TEST_IOD[4] | IO |
| 149 | DGND | G | 201 | DVDD | P |
| 150 | G1RX_DV/G1RXDS[8] | I | 202 | DGND | G |
| 151 | G1RXD[0] | I | 203 | TEST_IOD[3] | IO |
| 152 | G1RXD[1] | I | 204 | TEST_IOD[2] | IO |
| 153 | G1RXD[2] | I | 205 | TEST_IOD[1] | IO |
| 154 | G1RXD[3] | I | 206 | TEST_IOD[0] | IO |
| 155 | G1RXD[4] | I | 207 | SCK | IO |
| 156 | RVDD3 | P | 208 | SDA | IO |

# 6. Pin Descriptions

Type codes used: P = Power; G = Ground, I = Input, O = Output, Pu = Internal pull up (75K ohm), Pd = Internal pull down (75K ohm).

## 6.1. SMII Interface (Port #0 ~ Port #23)

**Table 3. SMII Interface (Port #0 ~ Port #23)**

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| P0TXD | O | 5 | SMII Transmit Data Output: |
| P1TXD | | 7 | SMII transmit data is formed in 10-bit serial words. Each word contains one |
| P2TXD | | 9 | data byte (two nibbles of 4B coded data) and two |
| P3TXD | | 13 | status bits. |
| P4TXD | | 16 | The SMII operates at 125MHz using a global reference clock |
| P5TXD | | 18 | (REFCLK) and frame synchronization signal (SYNC). |
| P6TXD | | 20 | |
| P7TXD | | 26 | SMII transmit data is input on these pins, where: |
| P8TXD | | 29 | Ports 0~7 transmit data is sent synchronously to SYNC_0_7 |
| P9TXD | | 31 | and REFCLK_0_7. |
| P10TXD | | 35 | Ports 8~15 transmit data is sent synchronously to SYNC_8_15 |
| P11TXD | | 37 | and REFCLK_8_15. |
| P12TXD | | 40 | Ports 16~23 transmit data is sent synchronously to SYNC_16_23 and |
| P13TXD | | 42 | REFCLK_16_23. |
| P14TXD | | 46 | |
| P15TXD | | 51 | |
| P16TXD | | 54 | |
| P17TXD | | 56 | |
| P18TXD | | 58 | |
| P19TXD | | 62 | |
| P20TXD | | 67 | |
| P21TXD | | 69 | |
| P22TXD | | 71 | |
| P23TXD | | 73 | |

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| P0RXD<br>P1RXD<br>P2RXD<br>P3RXD<br>P4RXD<br>P5RXD<br>P6RXD<br>P7RXD<br>P8RXD<br>P9RXD<br>P10RXD<br>P11RXD<br>P12RXD<br>P13RXD<br>P14RXD<br>P15RXD<br>P16RXD<br>P17RXD<br>P18RXD<br>P19RXD<br>P20RXD<br>P21RXD<br>P22RXD<br>P23RXD | I | 6<br>8<br>10<br>14<br>17<br>19<br>21<br>27<br>30<br>32<br>36<br>38<br>41<br>43<br>47<br>52<br>55<br>57<br>59<br>63<br>68<br>70<br>72<br>74 | SMII Receive Data Input:<br>SMII receive data is input on these pins. Where ports 0~7 receive data is received synchronously to SYNC_0_7 and REFCLK_0_7.<br>Ports 8~15 receive data is received synchronously to SYNC_8_15 and REFCLK_8_15.<br>Ports 16~23 receive data is received synchronously to SYNC_16_23 and REFCLK_16_23. |
| SYNC_0_7<br>SYNC_8_15<br>SYNC_16_23 | O | 15<br>39<br>66 | SMII Synchronization Output.<br>SMII transmit/receive data 10-bit word frame synchronization.<br>Where:<br>SYNC_0_7 synchronizes data for ports 0~7.<br>SYNC_8_15 synchronizes data for ports 8~15.<br>SYNC_16_23 synchronizes data for ports 16~23. |
| REFCLK_0_7<br>REFCLK_8_15<br>REFCLK_16_23 | O | 28<br>53<br>77 | SMII Reference Clock Output.<br>The SMII reference clock output is a 125MHz +- 50ppm clock used to synchronize the SMII data.<br>Ports 0~7 data is sent or received synchronously to SYNC_0_3.<br>Ports 8~15 data is sent or received synchronously to SYNC_8_15.<br>Ports 16~23 data is sent or received synchronously to SYNC_16_23. |

# 6.2. TBI/GMII/MII Interface (Port #G0 ~ Port #G1)

**Table 4. TBI/GMII/MII Interface (Port #G0 ~ Port #G1)**

| Symbol | Mode | Type | Pin No. | Description |
|---|---|---|---|---|
| G0TX_CLK | TBI | O | 96 | Gigabit port Transmit Clock Output (TBI mode).<br>125Mhz transmit 8B/10B encoded code-group clock. |
| G0TX_CLK | GMII | | | Transmit Clock Output (GMII mode).<br>125MHz transmit clock used for G0_TXD synchronization. |
| Not Used | MII | | | |

| Symbol | Mode | Type | Pin No. | Description |
|---|---|---|---|---|
| G0TXDS[3:0] | TBI | O | 87<br>88<br>89<br>90 | Transmit Data Output (TBI mode).<br>Transmits 8B/10B code group data synchronously to the rising edge of G0_TXCLK. |
| G0TXD[3:0] | GMII | | | Transmit Data Output (GMII mode).<br>Transmits data synchronously to the rising edge of G0_TXCLK. |
| G0TD[3:0] | MII | | | Transmit Data Output (MII mode).<br>Transmits data synchronously to the rising edge of G0_TXC. |
| G0TXDS[7:4] | TBI | O | 81<br>82<br>83<br>84 | Transmit Data Output (TBI mode).<br>Transmits 8B/10B code group data synchronously to the rising edge of G0_TXCLK. |
| G0TXD[7:4] | GMII | | | Transmit Data Output (GMII mode).<br>Transmits data synchronously to the rising edge of G0_TXCLK. |
| Not Used | MII | | | |
| G0TXDS[8] | TBI | O | 93 | Transmit Data Output, bit[8] (TBI mode).<br>Transmits 8B/10B code group data synchronously to the rising edge of G0_TXCLK. |
| G0TX_EN | GMII | | | Transmit Enable Output (GMII mode).<br>Transmit enable which is sent synchronously to the rising edge of G0_TXCLK. |
| G0TX_EN | MII | | | Transmit Enable Output (MII mode).<br>Transmit enable which is sent synchronously to the rising edge of G0_TXC. |
| G0TXDS[9] | TBI | O | 97 | Transmit Data Output, bit[9] (TBI mode).<br>Transmits 8B/10B code group data synchronously to the rising edge of G0_TXCLK. |
| Not Used<br>Not Used | GMII<br>MII | | | Keep logic low level (GMII, MII) |
| G0RSCK0 | TBI | I | 102 | Receive Clock 0 Input (TBI mode).<br>62.5MHz receive clock. Used to latch odd numbered code-group data G0_TXDS in the received PHY bit stream. |
| G0RX_CLK | GMII | | | Receive Clock Input (GMII modes).<br>125Mhz receive clock. Used to synchronize received G0_TXD data. |
| G0RXC | MII | | | Receive Clock Input (MII modes).<br>2.5/25 MHz (10Mbps/100Mbps) receive clock. Used to synchronize received G0_RXD data. |
| G0RSCK1 | TBI | I | 98 | Receive Clock 1 Input (TBI mode).<br>62.5MHz receive clock. Used to latch even numbered code-group data in the received PHY bit stream. |
| Leave Unconnected | GMII | | | |
| G0TXC | MII | | | Transmit Clock Input (MII modes).<br>2.5/25 MHz (10Mbps/100Mbps) receive clock. The transmit data is sent synchronously on the rising edge of G0_TXC. |

| Symbol | Mode | Type | Pin No. | Description |
|---|---|---|---|---|
| G0RXDS[3:0] | TBI | I | 120<br>119<br>118<br>104 | Receive Data Input (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G0_RXCLK. |
| G0RXD[3:0] | GMII | | | Receive Data Input (GMII mode).<br>Receive data that is received synchronously at the rising edge of G0_RXCLK. |
| G0RXD[3:0] | MII | | | Receive Data Input (MII mode).<br>Receive data that is received synchronously at the rising edge of G0_RXC. |
| G0RXDS[7:4] | TBI | I | 124<br>123<br>122<br>121 | Receive Data Input (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G0_RXCLK. |
| G0RXD[7:4] | GMII | | | Receive Data Input (GMII mode).<br>Receive data that is received synchronously at the rising edge of G0_RXCLK. |
| Not Used | MII | | | |
| G0RXDS[8] | TBI | I | 103 | Receive Data Input (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G0_RXCLK. |
| G0RX_DV | GMII | | | Receive Data Valid Input (GMII mode).<br>Receive data valid that is received synchronously at the rising edge of G0_RXCLK. |
| G0RX_DV | MII | | | Receive Data Valid Input (MII mode).<br>Receive data valid that is received synchronously at the rising edge of G0_RXC. |
| G0RXDS[9]<br>Not Used<br>Not Used | TBI<br>GMII<br>MII | I | 101 | Receive Data Input bit[9] (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G0_RXCLK. |
| Not Used<br>Not Used<br>G0CRS | TBI<br>GMII<br>MII | I | 99 | Carrier Sense Input (MII mode).<br>G0CRS is only valid in MII half duplex mode. It is asserted high when a valid carrier is detected on the media. |
| Not Used<br>Not Used<br>G0COL | TBI<br>GMII<br>MII | I | 100 | Collision Detect Input (MII).<br>G0COL is only valid in MII half duplex mode. It is asserted high when a collision is detected on the media. |
| G1TX_CLK | TBI | O | 141 | Gigabit port Transmit Clock Output (TBI mode).<br>125Mhz transmit 8B/10B encoded code-group clock. |
| G1TX_CLK | GMII | | | Transmit Clock Output (GMII mode).<br>125MHz transmit clock used for G1_TXD synchronization. |
| Not Used | MII | | | |

| Symbol | Mode | Type | Pin No. | Description |
|---|---|---|---|---|
| G1TXDS[3:0] | TBI | O | 132<br>133<br>134<br>135 | Transmit Data Output (TBI mode).<br>Transmits 8B/10B code group data synchronously at the rising edge of G1_TXCLK. |
| G1TXD[3:0] | GMII | | | Transmit Data Output (GMII mode).<br>Transmit data that is sent synchronously at the rising edge of G1_TXCLK. |
| G1TD[3:0] | MII | | | Transmit Data Output (MII mode).<br>Transmit data that is sent synchronously at the rising edge of G1_TXC. |
| G1TXDS[7:4] | TBI | O | 128<br>129<br>130<br>131 | Transmit Data Output (TBI mode).<br>Transmits 8B/10B code group data synchronously at the rising edge of G1_TXCLK. |
| G1TXD[7:4] | GMII | | | Transmit Data Output (GMII mode).<br>Transmit data that is sent synchronously at the rising edge of G1_TXCLK. |
| Not Used | MII | | | |
| G1TXDS[8] | TBI | O | 140 | Transmit Data Output, bit[8] (TBI mode).<br>Transmits 8B/10B code group data synchronously at the rising edge of G1_TXCLK. |
| G1TX_EN | GMII | | | Transmit Enable Output (GMII mode).<br>Transmit enable that is sent synchronously at the rising edge of G1_TXCLK. |
| G1TX_EN | MII | | | Transmit Enable Output (MII mode).<br>Transmit enable that is sent synchronously at the rising edge of G1_TXC. |
| G1TXDS[9] | TBI | O | 142 | Transmit Data Output, bit[9] (TBI mode).<br>Transmits 8B/10B code group data synchronously at the rising edge of G1_TXCLK. |
| Not Used<br>Not Used | GMII<br>MII | | | Keep logic low level (GMII, MII) |
| G1RSCK0 | TBI | I | 147 | Receive Clock 0 Input (TBI mode).<br>62.5MHz receive clock. Used to latch odd numbered code-group data G1_TXDS in the received PHY bit stream. |
| G1RX_CLK | GMII | | | Receive Clock Input (GMII modes).<br>125Mhz receive clock. Used to synchronize G1_TXD received data. |
| G1RXC | MII | | | Receive Clock Input (MII modes).<br>2.5/25 MHz (10Mbps/100Mbps) receive clock. Used to synchronize G1_RXD received data. |
| G1RSCK1 | TBI | I | 143 | Receive Clock 1 Input (TBI mode).<br>62.5MHz receive clock. Used to latch even numbered code-group data in the received PHY bit stream. |
| Leave Unconnected | GMII | | | |
| G1TXC | MII | | | Transmit Clock Input (MII modes).<br>2.5/25 MHz (10Mbps/100Mbps) receive clock. The transmit data is sent synchronously at the rising edge of G1_TXC. |

| Symbol | Mode | Type | Pin No. | Description |
|---|---|---|---|---|
| G1RXDS[3:0] | TBI | I | 154<br>153<br>152<br>151 | Receive Data Input (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G1_RXCLK. |
| G1RXD[3:0] | GMII | | | Receive Data Input (GMII mode).<br>Receive data that is received synchronously at the rising edge of G1_RXCLK. |
| G1RXD[3:0] | MII | | | Receive Data Input (MII mode).<br>Receive data that is received synchronously at the rising edge of G1_RXC. |
| G1RXDS[7:4] | TBI | I | 161<br>160<br>159<br>155 | Receive Data Input (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G1_RXCLK. |
| G1RXD[7:4] | GMII | | | Receive Data Input (GMII mode).<br>Receive data that is received synchronously at the rising edge of G1_RXCLK. |
| Not Used | MII | | | |
| G1RXDS[8] | TBI | I | 150 | Receive Data Input (TBI mode).<br>Receives 8B/10B code group data synchronously at the rising edge of G1_RXCLK. |
| G1RX_DV | GMII | | | Receive Data Valid Input (GMII mode).<br>Receive data valid that is received synchronously at the rising edge of G1_RXCLK. |
| G1RX_DV | MII | | | Receive Data Valid Input (MII mode).<br>Receive data valid that is received synchronously at the rising edge of G1_RXC. |
| G1RXDS[9]<br>Not Used<br>Not Used | TBI<br>GMII<br>MII | I | 146 | Receive Data Input bit[9] (TBI mode).<br>Receive 8B/10B code group data that is received synchronously at the rising edge of G1_RXCLK. |
| Not Used<br>Not Used<br>G1CRS | TBI<br>GMII<br>MII | I | 144 | Carrier Sense Input (MII mode).<br>G1CRS is only valid in MII half duplex mode. It is asserted high when a valid carrier is detected on the media. |
| Not Used<br>Not Used<br>G1COL | TBI<br>GMII<br>MII | I | 145 | Collision Detect Input (MII).<br>G1COL is only valid in MII half duplex mode. It is asserted high when a collision is detected on the media. |

# 6.3. Serial Management Interface (SMI)

**Table 5. Serial Management Interface (SMI)**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| MDC | O<br>(Pu) | 79 | Serial Management Data Clock (MDC).<br>MDC operates at 1MHz.<br>MDC is in tri-state when RST# is active low. |
| MDIO | IO<br>(Pu) | 80 | Serial Management Data Input/Output.<br>MDIO is in tri-state when RST# is active low. |

## 6.4. Serial EEPROM Interface

**Table 6. Serial EEPROM Interface**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| SCK | IO<br>(Pu) | 207 | Serial EEPROM interface Clock Output/ Serial CPU Access Clock Input.<br>SCLK acts as an output pin after hardware reset for EEPROM read access. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then the SCLK will act as an input pin driven by an external CPU to access the RTL8326 internal registers.<br>SCLK Frequency:<br>Output: Operates at 100KHz<br>Input: Max limit: 10MHz |
| SDA | IO<br>(Pu) | 208 | Serial EEPROM Data Input/Output/Serial CPU Access Data Input/Output.<br>After power on, this pin is EEPROM serial data IO. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then this pin acts as a serial CPU data IO.<br>See 7.28 Serial CPU Interface, page 48 for detailed data access format and timing information. |

## 6.5. System Pins

**Table 7. System Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| RST# | I<br>(Pu) | 178 | System Reset.<br>Active low to reset the system to a known state. After power-on reset (low to high), the configuration modes from Mode Control Pins (page 26) are strapped and determined. |
| XI/OSCI | I | 110 | Crystal Input/Oscillator Input.<br>This is a 25Mhz +-50 ppm crystal input or oscillator input.<br>When crystal is used, a capacitor connected from this pin to ground is recommended. |
| XO | O | 111 | Crystal Output.<br>When crystal is used, a capacitor connected from this pin to ground is recommended. When an oscillator is used, keep this pin floating. |
| G0_25MCKO<br>G1_25MCKO | O | 78<br>125 | 25MHz Clock Output.<br>These pins provide general purpose 25MHz clock outputs that are free running after power is stable, and are low jitter (50 ppm), with a 45 ~ 65% duty cycle.<br>This 25Mhz clock could be used for Gigabit 1000Base-TX PHY reference clock input. |
| USR_IO[3:0] | I<br>(Pd) | 182<br>183<br>184<br>185 | User Defined Data IO.<br>Used to define a level of detected input signal for system fault event management. The defined level is written to the internal registers.<br>These pin are internally pulled-low.<br>These pins may be used for external trigger signal input, for example, FAN fault, Thermal Fault, Factory Reset, or any other sensor detection. |

# 6.6. Mode Control Pins

*Note: The Mode Control pin values are strapped on power on reset. The strapped values may be updated via EEPROM configuration if it exists. They can also be modified by internal register access from the CPU interface.*

**Table 8. Mode Control Pins**

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| MaxPktLen[1:0]/ [P3TXD, P2TXD] | I (Pd, Pd) | 13, 9 | Max. Valid Packet Length Control.<br>00: 1536 bytes (Default)<br>01: 1552 bytes<br>1x: Reserved |
| TXIPG_Comp/ P4TXD | I (Pd) | 16 | Transmit IPG (Inter-Packet Gap) Compensation.<br>Used to compensate the oscillator frequency or incoming packet IPG tolerance.<br>0: +65 ppm TXIPG compensation (Default)<br>1: +90 ppm TXIPG compensation |
| MaxPauseCnt/ P5TXD | I (Pd) | 18 | Max Pause frame Count for Congestion Control.<br>0: 128 (Default)<br>1: Continuous |
| EnCRSBKPmode/ G1TX_EN | I (Pu) | 140 | Enable Carrier-Based Back Pressure Mode.<br>Half duplex back pressure flow control algorithm selection.<br>0: Collision-based back pressure mode<br>1: Carrier-based back pressure mode (Default) |
| FrcTBIMode[1:0]/ [P1TXD, P0TXD] | I (Pd) | 7, 5 | Force Enable Gigabit port at TBI Mode Interface of Port G0 or G1.<br>FrcTBImode[0], for Gigabit port 0<br>FrcTBImode[1], for Gigabit port 1<br>0: Enable GMII/MII Mode Interface (Default)<br>1: Enable TBI Mode Interface.<br><br>*Note: After the Gigabit Port Interface Mode is selected, the port will be auto disabled whenever the interface receive clock is idle for a defined timeout period.* |
| DisRRCP/ P10TXD | I (Pd) | 35 | Disable Realtek Remote Control Protocol Function.<br>0: Enable RRCP (Default)<br>1: Disable RRCP |
| DisREcho/ P11TXD | I (Pd) | 37 | Disable Realtek Echo Function.<br>0: Enable REcho (Default)<br>1: Disable REcho |
| EnCtrlFFilter/ P13TXD | I (Pu) | 42 | Enable 802.1D Specified Reserved Control Frame Filtering.<br>When network control frames are received with the destination MAC address as the group MAC address: (01-80-C2-00-00-03 ~ 01-80-C2-00-00-0F), the switch will drop the frames if the EnCtrlFilter=1. If EnCtrlFilter=0 the frames will be flooded.<br>0: Disable Filtering<br>1: Enable Filtering (Default) |
| EnIGMPsnooping/ P14TXD | I (Pd) | 46 | Enable IGMP Snooping.<br>0: Disable (Default)<br>1: Enable |

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| EnHomeVLAN/<br>P15TXD | I<br>(Pd) | 51 | Enable Home-VLAN Configuration.<br>When enabled, the switch will be configured in 24VLAN mode, "Home-VLAN topology". That is, ports 0~23 are all individual VLANs shared with two port members, Gigabit ports 0 & 1.<br>0: Disable (Default)<br>1: Enable |
| PortPriSet[1:0]/<br>[P22TXD,<br>P21TXD] | I<br>(Pd, Pd) | 71, 69 | High Priority Port Setting of Port-based QoS Function.<br>00: No high priority port (Default)<br>01: Set port 0 as high priority ports<br>10: Set ports 0, 1 as high priority ports<br>11: Set ports 0, 1, 2, 3 as high priority ports |
| En8021pPri/<br>P17TXD | I<br>(Pd) | 56 | Enable 802.1p VLAN Tag-based Priority QoS Function.<br>0: Disable (Default)<br>1: Enable |
| EnDSPri/<br>P16TXD | I<br>(Pd) | 54 | Enable TCP/IP TOS/DS (DiffServ) based Priority QoS Function.<br>0: Disable (Default)<br>1: Enable<br>High Priority: If TOS/DS[0:5]:<br>(EF) '101110';<br>(AF) '001010', '010010',<br>'011010', '100010';<br>(Network Control) '11x000';<br>Low Priority: If TOS/DS: Other then Codepoint values are applied. |
| QWEIGHT[1:0]/<br>[P20TXD,<br>P19TXD] | I<br>(Pu,Pd ) | 67, 62 | Weighted Round Robin Ratio Setting of Priority Queue.<br>The frame service rate of High-pri queue: Low-pri queue is.<br>00: 4:1<br>01: 8:1<br>10: 16:1 (Default)<br>11: 1:0 (always high priority queue first) |
| EnFCAutoOff/<br>P18TXD | I<br>(Pd) | 58 | Enable Flow Control Ability Auto Turn Off for QoS Enabled.<br>Enable auto turn-off of a port's queue flow control ability for 1~2 seconds whenever the port receives a high priority frame. The flow control ability of the port will be re-enabled when no high priority frames are received at this port during a 1~2 second period.<br>When EnFCAutoOff is disabled, the flow control ability of this port for any packet will be enabled as set.<br>0: Disabled (Default)<br>1: Enabled |
| DisFDFC/<br>P23TXD | I<br>(Pd) | 73 | Global Disable Full Duplex 802.3x Pause Flow Control Ability.<br>Globally disables the 802.3x Pause ability flow control of all ports.<br>0: Enable 802.3x Pause flow control ability (Default)<br>1: Disable 802.3x Pause flow control ability |
| DisBKP/<br>G0TX_EN | I<br>(Pd) | 93 | Global Disable Half Duplex Back Pressure Flow Control Ability.<br>Globally disables the back pressure flow control ability of all ports.<br>0: Enable back pressure flow control ability (Default)<br>1: Disable back pressure flow control ability |
| DisBKP48One/<br>P6TXD | I<br>(Pd) | 20 | Disable Back Pressure 48 Pass One Algorithm.<br>When the 48 Pass One algorithm is enabled, the switch will pass one incoming packet for every 48 collisions.<br>0: Enable 48 Pass One algorithm (Default)<br>1: Disable 48 Pass One algorithm |

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| DisBCSFC/<br>G0TXDS7 | I<br>(Pd) | 81 | Disable Broadcast Packet Strict Flood Control.<br>Set to disable broadcast packet (DA: 'FF-FF-FF-FF-FF-FF') strict flood mode and configure to loose flood mode.<br>Strict flood mode will drop all broadcast packets if any one destination port is congested.<br>Loose flood mode allows broadcast packets to be flooded to all non-congested ports.<br>0: Enable Broadcast Packet Strict Flood (Strict flood mode) (default)<br>1: Disable Broadcast Packet Strict Flood (Loose flood mode) |
| DisIPMCSFC/<br>G0TXDS6 | I<br>(Pd) | 82 | Disable IP Multicast Packet Strict Flood Control.<br>Set to disable IP Multicast packet (DA: '01-00-5E-XX-XX-XX') strict flood mode and configure to loose flood mode.<br>Strict flood mode will drop all IP Multicast packets if any one destination port is congested.<br>Loose flood mode allows IP Multicast packets to be flooded to all non-congested ports.<br>0: Enable IP Multicast Packet Strict Flood (Strict flood mode) (default)<br>1: Disable IP Multicast Packet Strict Flood (Loose flood mode) |
| DisBRDCTRL/<br>G0TXDS5 | I<br>(Pu) | 83 | Broadcast Storm Filtering Control.<br>Disables broadcast storm filtering control.<br>0: Enable Broadcast storm filtering control<br>1: Disable Broadcast storm filtering control (Default) |
| EnLoopDet/<br>P9TXD | I<br>(Pd) | 31 | Enable Loop Detect function.<br>0: Disable (Default)<br>1: Enable |
| EnGDSRev/<br>P7TXD | I<br>(Pd) | 26 | Enable Gigabit Port Data Sequence Reverse.<br>When set, reverses the sequence of TXD '[7:0]' to '[0:7]'.<br>RXD[7:0] maintains the original sequence.<br>0: Disable (Default)<br>1: Enable |
| OCT2_RXD_<br>Delay_2ns/<br>G1TXDS2 | I<br>(Pd) | 133 | To delay 2ns on OCT_PHY_2 RXD<br>0: Delay 0 ns (Default)<br>1: Delay 2 ns (Recommended)<br>If EEPROM exists, the EEPROM configuration will override the delay configuration set here. |
| OCT1_RXD_<br>Delay_2ns/<br>G1TXDS1 | I<br>(Pd) | 134 | To delay 2ns on OCT_PHY_1 RXD<br>0: Delay 0 ns (Default)<br>1: Delay 2 ns (Recommended)<br>If EEPROM exists, the EEPROM configuration will override the delay configuration set here. |
| OCT0_RXD_<br>Delay_2ns/<br>G1TXDS0 | I<br>(Pd) | 135 | To delay 2ns on OCT_PHY_0 RXD.<br>0: Delay 0 ns (Default)<br>1: Delay 2 ns (Recommend)<br>If EEPROM exists, the EEPROM configuration will override the delay configuration set here. |
| TBI_G0_Force_<br>Link/<br>G0TXDS3 | I<br>(Pd) | 87 | Force TBI G0 Link Up.<br>0: Normal (Default)<br>1: Force Link Up |
| TBI_G1_Force_<br>Link/<br>G0TXDS4 | I<br>(Pd) | 84 | Force TBI G1 Link Up.<br>0: Normal (Default)<br>1: Force Link Up |

| Symbol | Type | Pin No. | Description |
|---|---|---|---|
| EnFastAgeTime/<br>P12TXD | I<br>(Pd) | 40 | Enable Fast Aging Time.<br>0: 300 sec Aging Time (Default)<br>1: 12 sec Aging Time (Fast Aging Time) |
| EnAcceptErr/<br>G0TXDS2 | I<br>(Pd) | 88 | Enable Accept CRC Error packet.<br>Set to enable acceptance of a CRC error packet with valid packet length (64 byte ~ max packet length).<br>0: Disable accept CRC error packet (Default)<br>1: Enable accept CRC error packet |

# 6.7. LED Pins

**Table 9. LED Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| SLED_DMODE_CK | I | 162 | Serial LED Diagnostic Mode Item Select Control Pulse Input.<br>This is an external signal pulse input signal for diagnostic item selection. The diagnostic LED display item will change whenever there is a signal pulse clock input on this pin.<br>The diagnostic items list and its display sequence is as follows:<br>(1) DisablePort/RxError (active low)<br>On: Port disabled<br>Blinking: Error Packet Received (includes dropped packets)<br>(2) FlowControl/FCActive (active low)<br>On: Flow control ability enabled<br>Blinking: Congestion flow control active<br>(3) TrunkPort/TKFault (active low)<br>On: Trunk Port<br>Blinking: Trunk link fault port<br>(4) HighPriorityPort (active low)<br>On: High priority port<br>(5) LoopDetectPort (active low)<br>On: Loop event detected.<br>(6) BroadcastStormAlarmPort (active low)<br>On: Broadcast Storm detected<br>(7) TX Utilization: TX port bandwidth utilization (active low)<br>(8) RX Utilization: RX port bandwidth utilization (active low) |
| SLED_CLK/<br>LED_EnTrunk[0] | O | 177 | Serial LED Shift Clock/Trunk Port 0 Enabled LED output.<br>In Parallel LED mode, acts as Trunk 0 Enable LED.<br>In Serial LED mode, when Serial LED mode is enabled, periodically active to enable SLED_DATA shift into external shift register. |
| SLED_DATA/<br>LED_EnTrunk[1] | O | 176 | Serial LED Data Output/Trunk Port 1 Enabled LED output.<br>In Serial LED mode, when Serial LED mode is enabled, serial LED data is shifted out when SLED_CLK is active.<br>See 7.31 LED Interfaces, page 51 for detailed information. |

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| LED_EnTrunk[7:2] | O | 170<br>171<br>172<br>173<br>174<br>175 | Trunk Port Enabled LED output.<br>0 (On): Trunk Enabled<br>1 (Off): Trunk Disabled.<br>The LED blinks to indicate that there is a trunk member port link down.<br>LED_EnTrunk0: (port 0, 1)<br>LED_EnTrunk1: (port 2, 3)<br>LED_EnTrunk2: (port 4, 5, 6, 7)<br>LED_EnTrunk3: (port 8, 9, 10, 11)<br>LED_EnTrunk4: (port 12, 13, 14, 15)<br>LED_EnTrunk5: (port 16, 17, 18, 19)<br>LED_EnTrunk6: (port 20, 21, 22, 23)<br>LED_EnTrunk7: (port G0, G1) |
| Reserved | O | 165 | Reserved for testing (VLED). |
| LED_LoopDet | O | 166 | Loop Detect LED output.<br>0: Loop detected<br>1: Loop not detected |
| LED_BISTFail | O | 169 | Built-In Self Test (BIST) LED output.<br>0: BIST FAIL<br>1: BIST PASS |
| LED_GLink/ACT[1:0] | O | 163<br>164 | Gigabit Ports 1000Mbps Speed Link/Active LED output.<br>This LED show the state information of the Gigabit Port when it is linked at 1000Mbps.<br>The definition of this LED is different in serial mode and parallel mode:<br>In Serial Mode it is 1000M speed<br>In Parallel Mode it is 1000M Link/ Activity<br>0: Link Up<br>1: Link Down<br>Blinking: TX/RX Activity<br>(Blinking is 40 ms ON then 40 ms OFF) |

# 6.8. Power/Ground Pins

**Table 10. Power/Ground Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| AVDD | P | 108<br>113 | 3.3V for Phase-Locked Loop (PLL) Power. |
| AVSS | G | 109<br>112 | GND for Phase-Locked Loop (PLL). |
| DVDD | P | 11, 22, 33, 44, 60, 75, 85, 94, 126, 136, 148, 167, 181, 201 | 3.3V for IO digital power. |
| DGND | G | 12, 23, 34, 45, 61, 76, 86, 95, 127, 137, 149, 168, 202 | GND for IO. |
| RVDD | P | 3, 50, 106, 156 | 3.3V for internal 3.3V to 1.8V regulator power input.<br>*Note: Pins 3, 50, 106, 156) map to RVDD0, RVDD1, RVDD2, RVDD3.* |
| *VDD0* | P | 2, 24,179 | 1.8V for Core power. Generated by internal regulator.<br>Only an external 10uF CAP and bypass CAP are required.<br>*Note: DO NOT supply 1.8V power to these pins.* |
| *VDD1* | P | 49, 64 | 1.8V for Core power. Generated by internal regulator.<br>Only an external 10uF CAP and bypass CAP are required.<br>*Note: DO NOT supply 1.8V power to these pins.* |
| *VDD2* | P | 91, 105 | 1.8V for Core power. Generated by internal regulator.<br>Only an external 10uF CAP and by pass CAP are required.<br>*Note: DO NOT supply 1.8V power to these pins.* |
| *VDD3* | P | 138, 157 | 1.8V for Core power. Generated by internal regulator.<br>Only an external 10uF CAP and by pass CAP are required.<br>*Note: DO NOT supply 1.8V power to these pins.* |
| GND | G | 4, 25, 48, 65, 92, 107, 139, 158, 180, | GND for Core power. |

## 6.9. Test Pins

**Table 11. Test Pins**

| Symbol | Type | Pin No | Description |
|---|---|---|---|
| ExtSysCLKI | I | 115 | Test pin.<br>Normally kept floating. |
| EnExtSysCLK | I<br>(Pd) | 114 | Test pin.<br>Normally kept floating. |
| Ext125CLKI | I | 117 | Test pin.<br>Normally kept floating. |
| EnExt125CLK | I<br>(Pd) | 116 | Test pin.<br>Normally kept floating. |
| EnExt18VPwr | I<br>(Pd) | 1 | Test pin.<br>Normally kept floating. |
| EnTESTMODE | I<br>(Pd) | 186 | Test pin.<br>Normally kept floating. |
| TEST_PIN [17:0] | IO | 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 203, 204, 205, 206 | Test Pins.<br>Normally kept floating. |

# 7. Functional Description

## 7.1. Reset

### 7.1.1. Hardware Reset

In a power-on reset, an internal power on reset pulse (44ms) will be generated and the RTL8326 will start the reset initialization procedures. These are:

1. Determine various default settings via the hardware strap pins at the end of the RST# signal
2. Auto load the configuration from EEPROM if EEPROM is detected (approx. 10ms)
3. Complete the embedded SSRAM BIST process (approx. 24 ms)
4. Initialize the packet buffer descriptor allocation
5. Initialize the internal registers and prepare them to be accessed by the serial CPU interface
6. Start MDC/MDIO configuration and polling

*Note 1: To guarantee register access is valid and correct, the RTL8326 registers should not be accessed before the reset initialization process is finished.*

*Note 2: The connected PHY should have completed the reset process before the RTL8326 starts the MDC/MDIO configuration and polling process.*

### 7.1.2. Software Reset

The software reset command resets the system control circuit and restarts auto-negotiation. It keeps the user configured settings. Hardware pin strapping, EEPROM auto load, and SSRAM BIST are NOT done when using the software reset command.

## 7.2. MAC to PHY Interface

The MAC to PHY interface supports SMII for 10/100M ports, and GMII/MII/TBI for Gigabit ports. Two 25Mhz clock outputs for external Gigabit PHY save BOM costs.

## 7.3. Fast Ethernet Port (SMII Interface)

Ports 0~23 are 10/100M Fast Ethernet ports supporting a Serial Media Independent Interface (SMII). The RTL8326 provides three SMII synchronous 125Mhz clock outputs for three octal PHYs. The SMII RXD IO delay control and Reference clock delay control are supported by configuring register 0x0002~ 0x0003. This function allows SMII timing fine-tuning for different PCB layout traces. The default values are optimized for SMII interface timing.

## 7.4. Gigabit Ethernet Ports (GMII/TBI/MII)

The Gigabit Ethernet ports may be configured as GMII (Gigabit Media Independent Interface), TBI (Ten-Bit Interface), or MII (Media Independent Interface) mode to support 1000Base-T, 1000Base-X, and

10Base-T/100Base-TX modes. These interface modes are enabled by hardware configuration pins FrcTBIMode[1:0]:

GMII TXD/RXD IO delay control is also supported on register 0x0002~0x0003.

When configured as a GMII or TBI interface, only full-duplex operation is supported. When configured as an MII interface, both full and half-duplex operations are supported.

## 7.5. GMII/MII/TBI Signal Mapping

GMII/MII/TBI support is implemented via the same hardware pins. The signal mapping is shown in the following table:

**Table 12. GMII/MII/TBI Signal Mapping**

| GMII | MII | TBI | IO |
|---|---|---|---|
| GTX_CLK(125Mhz) | - | G_TXCLK(125Mhz) | O |
| GTXD0 | GTXD0 | GTXDS0 | O |
| GTXD1 | GTXD1 | GTXDS1 | O |
| GTXD2 | GTXD2 | GTXDS2 | O |
| GTXD3 | GTXD3 | GTXDS3 | O |
| GTXD4 | - | GTXDS4 | O |
| GTXD5 | - | GTXDS5 | O |
| GTXD6 | - | GTXDS6 | O |
| GTXD7 | - | GTXDS7 | O |
| GTX_EN | GTX_EN | GTXDS8 | O |
| - | - | GTXDS9 | O |
| GRX_CLK(125Mhz) | GRXC(2.5/25Mhz) | GRSCK0(62.5Mhz) | I |
| - | GTXC(2.5/25Mhz) | GRSCK1(62.5Mhz) | I |
| GRXD0 | GRXD0 | GRXDS0 | I |
| GRXD1 | GRXD1 | GRXDS1 | I |
| GRXD2 | GRXD2 | GRXDS2 | I |
| GRXD3 | GRXD3 | GRXDS3 | I |
| GRXD4 | - | GRXDS4 | I |
| GRXD5 | - | GRXDS5 | I |
| GRXD6 | - | GRXDS6 | I |
| GRXD7 | - | GRXDS7 | I |
| GRX_DV | GRX_DV | GRXDS8 | I |
| - | - | GRXDS9 | I |
| - | GCRS | - | I |
| - | GCOL | - | I |

In TBI interface mode, the RTL8326 implements a built-in PCS (Physical Coding Sublayer) for SERDES transceiver applications. The PCS function implemented by the RTL8326 comprises:

- PCS Transmit process
- PCS Receive process
- 8-bit to 10-bit Encoding and 10-bit to 8-bit Decoding
- Synchronization process
- Auto-negotiation process for 1000BASE-X.

*Note: Half-duplex is not supported by the RTL8326's Gigabit PCS).*

## 7.6. MAC Address Table Search and Learning

The RTL8326 MAC address lookup table consists of an 8K-entry hash table and 64-entry CAM. The RTL8326 uses the last 13 bits of the MAC address to index the 8K-entry lookup table for address searching and learning. If the mapped location in the 8K entries is occupied, then the RTL8326 will compare the destination MAC address with the contents of the CAM for address searching and store the source MAC address to the CAM for address learning. The 128-entry CAM helps avoid address hash collisions and improves switch performance.

## 7.7. MAC Table Aging Function

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if it is not updated by the address learning process within a set aging time period. The default aging timer of the MAC address lookup table is between 200 ~ 300 seconds.

## 7.8. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded. The max. packet length may be 1536 or 1552 bytes and is controlled by register 0x0001.

## 7.9. 802.1D Reserved Group Addresses Filtering Control

The RTL8326 supports the ability to drop 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-03 to 01-80-C2-00-00-0F. The RTL8326 default setting enables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered.

## 7.10. Backoff Algorithm

The RTL8326 implements the truncated exponential backoff algorithm compliant with the IEEE 802.3 standard. The collision counter is restarted after 16 consecutive collisions.

## 7.11. Inter-Packet Gap

The Inter-Packet Gap is 9.6μs for 10Mbps Ethernet, 960ns for 100Mbps fast Ethernet, and 96ns for Gigabit Ethernet.

The RTL8326 supports Transmit Inter-Packet Gap compensation for the frequency shift tolerance of the on-board oscillator, which is controlled by register 0x0001.

## 7.12. Buffer Management

An embedded 2.5Mbit SSRAM is built-in as a packet storage buffer. To efficiently utilize the packet buffer, the RTL8326 divides the SSRAM into 2.5k 128-byte page-based buffers that are linked by a descriptor link list. For an Ethernet packet, a minimum of one, and maximum of 12 pages can be used. The system supports 24 10/100M ports plus 2 Gigabit ports non-blocking wire speed switching.

# 7.13. Flow Control

The RTL8326 supports IEEE 802.3x full-duplex flow control, and half-duplex back pressure congestion control.

## 7.13.1. 802.3x Pause Flow Control

IEEE 802.3x flow control is auto-negotiated between the remote device and the RTL8326 by writing the flow control ability, via MDIO, to an external connected PHY.

If a good PAUSE frame is received from any PAUSE flow control enabled port with DA=0180C2000001, the corresponding port of the RTL8326 will stop its packet transmission until a PAUSE timer timeout or another PAUSE frame with zero PAUSE time is received.

The maximum transmitted Pause frame count during a congestion event is controllable. (1) limited to a 128 count (2) unlimited count. The limited count is used to avoid unexpectedly long pause time locks for some network topology traffic. This is controlled by register 0x0001.

## 7.13.2. Half Duplex Back Pressure Flow Control

The RTL8326 supports two back pressure flow control schemes to force incoming packet backoff when the switch destination port is congested. The back pressure mode is controlled by 'EnCRSBKPMode' at register 0x0001. A hardware control pin is supported.

**Collision-based back pressure:** Uses a 4-byte jam pattern to force collisions with each incoming packet to force the link partner to back off transmissions according to CSMA/CD until the destination port congestion event is cleared. The RTL8326 uses a special half-duplex back pressure design; after 48 forced collisions it unconditionally receives and forwards one packet successfully. This prevents the connected repeater from being partitioned due to excessive collisions.

**Carrier sense-based back pressure:** When a congested event is asserted, the RTL8326 continuously sends 4k jam packets with a minimum Inter-Packet Gap to prevent the link partner from transmitting more packets.

# 7.14. Broadcast Storm Filtering Control

The RTL8326 supports broadcast storm filtering control via hardware pin 'DisBRDCTRL' or register 0x0607.

This function enables each port to drop broadcast packets (Destination MAC ID is 'ff ff ff ff ff ff') after a ***continuous received broadcast packets counter*** count of 64. The counter is reset to 0 every 800ms or when receiving non-broadcast packets (Destination MAC ID is not 'ff ff ff ff ff ff').

# 7.15. Head-Of-Line Blocking Prevention

The RTL8326 incorporates a simple mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8326 first checks the destination address of an incoming packet. If the destination port is congested, then the RTL8316 discards this packet to avoid blocking following packets destined for a non-congested port.

# 7.16. Port Trunking and Fault Recovery Support

Port Trunking is the ability to aggregate several 10/100Mbps ports or several gigabit ports into a single logical link. There are 8 trunk groups supported by the RTL8326. They are identified as:

Trunk 0: (Port 0, 1)

Trunk 1: (Port 2, 3)

Trunk 2: (Port 4, 5, 6, 7)

Trunk 3: (Port 8, 9, 10, 11)

Trunk 4: (Port 12, 13, 14, 15)

Trunk 5: (Port 16, 17, 18, 19)

Trunk 6: (Port 20, 21, 22, 23)

Trunk 7: (Port G0, G1)

They are individually enabled by Register 0x0307 EnTrunk[7:0] during hardware reset. Each trunk supports a trunking port status LED. The LED will be active low when the trunking function is enabled.

The RTL8326 trunking port always sends packets over the same link path in the trunk with a given source and destination MAC address to prevent frames from getting out of order, but the reverse path may follow a different link.

## 7.16.1. Load Balancing

The load balancing scheme between links in a trunk group is determined by an Index[2:0] value that is calculated by a DA and SA hash algorithm.

Mapping algorithm. Given a number between 8 values of Index[2:0],

If link up port is 4. Index value {(7, 6), (5, 4), (3, 2), (1, 0)} maps to LinkUpPort[3:0]

If link up port is 3. Index value {(7, 6, 5), (4, 3, 2), (1, 0)} maps to LinkUpPort[2:0]

If link up port is 2. Index value {(7, 6, 5, 4), (3, 2, 1, 0)} maps to LinkUpPort[1:0]

If link up port is 1. Index value {(7, 6, 5, 4, 3, 2, 1, 0)} maps to LinkUpPort[0]

## 7.16.2. Trunk Fault Auto Recovery

If a physical port of a trunk group is link down, then the TrunkLED will blink to warn of a link-down fault event. The Fault flag will be reported on register 0x0102 (System Fault Indication Register).

The RTL8326 will auto-start the Auto Fault Recovery scheme to distribute the trunk load to the remaining link up ports.

## 7.17. IGMP Snooping Support

The RTL8326 supports ASIC-based IGMP (Internet Group Management Protocol) snooping. This can be enabled via register 0x0308 and no other external CPU handling is required. It supports the ability to parse the IGMP control protocol packets and IP multicast data packets and learn the multicast router port and group address member ports into the multicast address table.

The RTL8326 differentiates between IGMP control protocol packets according to the message type:

- Router protocol packets (IGMP query packets and multicast routing protocol packets) are broadcast to all ports.
- Group member protocol packets (IGMP v1, v2 Report and Leave packets) are sent directly to multicast router ports.

IP multicast data packets involve multicast group table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to all member ports and router ports. If the multicast address is not stored in the address table (i.e. lookup miss), the packet is broadcast to all ports of the broadcast domain.

The multicast table is combined with a L2 MAC table with a maximum of 8k entries. For a given multicast entry, the valid port member bit will auto age out after about 5 min if the port does not receive a corresponding group address IGMP report packet.

## 7.18. VLAN Function

The RTL8326 supports a VLAN function to segregate the switch into 32 VLANs. Each VLAN is a broadcast domain and each VLAN may be flexibly configured from 0 to 26 port members. Both port-based and tag-based VLAN functions are supported. The PVID, Tagging Control, and Ingress/Egress rules are manually configured on the VLAN Table at registers 0x030B~0x037C. The VLAN table format is shown as follows:

**Table 13. VLAN Table Format**

| VLAN Entry Index | VID (12-Bit) | Port Member Set (26-bit Bitmap) |
|---|---|---|
| 0 | | |
| 1 | | |
| 2 | | |
| : | | |
| 31 | | |

'VID' defines the 802.1Q VLAN ID. The value of 'VID' may NOT be '0x000' or '0xfff'. 'Port Member Set' defines the VLAN group members via a 26-bit bitmap.

**Table 14. Port VLAN ID (PVID) Assignment Table**

| Port No. | "PVID Index for 802.1Q VLAN" or "VLAN Index for Port-based VLAN" *(5-bit addressing to 32 VLAN entries)* |
|---|---|
| 0 | |
| 1 | |
| 2 | |
| : | |
| 25 | |

The per-port default Port VLAN Identifier (PVID) is defined at PVID register (0x030C~0x0318) which is a VLAN table entry index mapped to a 12-bit VID. Each port should be assigned a unique PVID. The VID of each VLAN Table entry should be different. Overlapping port groups are allowed. This feature makes it easy to allow a server port to be shared between different VLAN groups without routing through an external router device.

A VLAN is used to divide the broadcast domain to cut broadcast scope. The VLAN Frame Forwarding Rules are defined as follows:

- A received broadcast/multicast frame will be flood forwarded to VLAN member ports only ('Port Member Set' in the VLAN table) of the VLAN except the source port.
- A received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded unless Leaky VLAN control is enabled.
- All VLAN groups share the same layer-2 learned MAC address table (Shared Learning).

## 7.18.1. Port-based VLAN

By setting the 0x030B register to disable the En8021Qaware control bit, port-based VLAN is enabled and 802.1Q VLAN tagging is ignored. All other VLAN table configurations are the same as tag-based VLAN functions. The VLAN classification of an incoming packet on a port-based VLAN is defined by the port PVID. The RTL8326 uses the Port VLAN Identifier (PVID) to search the VLAN table for the VLAN member.

## 7.18.2. 802.1Q Tag-based VLAN

By setting the 0x030B register to enable the En8021Qaware control bit, 802.1Q tag-based VLAN is enabled.

VLAN classification is the first step before VLAN table lookup. The method of assigning a unique VID value to a received packet is as follows:

1. For a VLAN-tagged packet.

   If the tagged 12-bit VID != 0, then the tagged VID value is used.

   If the tagged VID = 0 (Null VID, priority tag), then the port's PVID value is used.

2. For a non-VLAN-tagged packet.

   The port's 12-bit PVID value is used.

After the unique 12-bit VID is assigned, the RTL8326 checks the VLAN table ingress/egress rule, and then forwards the packet to valid destination ports.

## 7.18.3. Ingress/Egress Filtering Control Parameters

Two VLAN filtering rule control parameters are provided on register 0x030B:

- Acceptable frame type control: Admits all frames or admits only VLAN-tagged frames.
- Ingress filtering control: Enables filtering of frames received from a port that is not in this port's VLAN group.

### 7.18.4. Leaky VLAN

The Leaky VLAN feature enables specific frames to be forwarded between different VLANs.

For example, if the VLAN table entry is:

VLAN 1: Port members = { Port 1, 2, 3 }

VLAN 2: Port members = { Port 4, 5, 6}

Normally, broadcast/multicast, and unicast packets not allowed to be switched between these two VLANs. Port 1 broadcast packets will only flood to Port 2 and 3. A Port 1 unicast packet is not allowed to be forwarded to a member of VLAN 2.

If the Leaky VLAN function is enabled, three types of packets may be forwarded to destination ports outside the current VLAN.

1. **Unicast Packet:** May be forwarded to a destination port (L2 table lookup hit) on a different VLAN.
2. **ARP Broadcast Packet:** May be broadcast to all ports on a switch.
3. **IP Multicast Packet:** May be flooded to all the multicast address group member set, ignoring the VLAN member set domain limitation.

These types of leaky control are used when:

- a switch is divided into multiple VLANs and host to host communication is required between the different VLANs without using a router.
- you want to improve router performance.

### 7.18.5. Insert/Remove VLAN Priority Tag

The RTL8326 supports Output Priority tagging control via register set 0x0319~0x031C. There are four types of VLAN tagging:

1. Remove the VLAN tag from all tagged packets.
2. Insert a priority tag into untagged high-priority packets (Set priority field: 7, VID field: 0 for high priority packet).
3. Insert a priority tag into all untagged packets.
   (Set priority field: 7, VID field: 0 for high priority packet; Set priority field: 0, VID field: 0 for low priority packet.)
4. Don’t touch (No modification made to the packet).

*Note: This function may be enabled whether the VLAN function is enabled or not.*

## 7.19. QoS Function

The RTL8326 can recognize QoS priority information in an incoming packet and send the packet to different priority queues for different service priority. The RTL8326 identifies the packet’s priority based on three types of QoS priority information:

1. Port-based priority
2. 802.1p/Q VLAN tag
3. TCP/IP TOS/DiffServ (DS) priority field

These three types of QoS can be configured via hardware pins, EEPROM, or Registers 0x0400 and 0x0401.

The RTL8326 supports two priority level queues. The queue service rate is based on the Weighted Round Robin algorithm. The packet-based service weight ratio of high-priority and low-priority queuing can be set as 4:1, 8:1, 16:1 or 'Always high priority first'.

## 7.19.1. Port-Based Priority

When port-based priority is applied, any packet received from a high priority port will be treated as a high priority packet.

## 7.19.2. 802.1p/Q Based Priority

When 802.1p tag priority is applied, the RTL8326 recognizes 802.1Q VLAN tagged packets and extracts the 3-bit User Priority information from the VLAN tag. The RTL8326 sets the User Priority threshold to 3. VLAN tagged packets with User Priority values 4~7 are treated as high priority packets, and other User Priority values (0~3) as low priority packets (follows the IEEE 802.1p standard).

## 7.19.3. Differentiated Service Based Priority

When TCP/IP's TOS/DiffServ (DS) based priority is applied, the RTL8326 recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for IPv4 is the Type-of-Service (TOS) octet, and for IPv6, it is the Traffic-Class octet. Recommended DiffServ Codepoints are defined in RFC2597 for classifying traffic into different service classes. The RTL8326 extracts the codepoint value of the DS field from IPv4 and IPv6 packets and identifies the priority of the incoming IP packet following the definitions listed below:

High Priority. DS-field = 101110 (EF, Expected Forwarding)

001010; 010010; 011010; 100010 (AF, Assured Forwarding)

11x000 (Network Control)

Low Priority. DS-field = Other values

VLAN tagged packet formats are shown below:

| 6 bytes | 6 bytes | 2 bytes | 3 bits | 5 bits | | 4 bytes |
|---|---|---|---|---|---|---|
| DA | SA | 81-00 | User Priority<br>(0~3: Low-pri; 4~7: High-pri) | ---- | Data | CRC |

**Figure 4. 802.1Q VLAN Tag Frame Format**

| 6 bytes | 6 bytes | 4 bytes | 2 bytes | 4 bits | 4 bits | 6 bits | 2 bits | | 4 bytes |
|---|---|---|---|---|---|---|---|---|---|
| DA | SA | 802.1Q Tag<br>(Optional) | 08-00 | Version<br>IPv4: 0100 | IHL | TOS[0:5]: DS-field | ---- | Data | CRC |

**Figure 5. IPv4 Frame Format**

| 6 bytes | 6 bytes | 4 bytes | 2 bytes | 4 bits | 6 bits | 2bits | | 4 bytes |
|---|---|---|---|---|---|---|---|---|
| DA | SA | 802.1Q Tag<br>(Optional) | 08-00 | Version<br>IPv6: 0110 | Traffic Class [0:5]<br>=DS-field | ---- | Data | CRC |

**Figure 6. IPv6 Frame Format**

### 7.19.4. Flow Control Auto Turn Off

The RTL8326 can automatically turn off 802.3x flow control and back pressure flow control for 1~2 seconds whenever the port receives a high priority packet. Flow control is re-enabled when no priority packet are received for 1~2 seconds. This auto-turn off function is enabled via hardware pin EnFCAutoOff or Register 0x0400.

## 7.20. Ingress and Egress Bandwidth Control

The RTL8326 supports bandwidth control on all ports. Each port's bandwidth is configurable on both ingress and egress traffic independently. Port bandwidth may be configured as: 128kbps, 256kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, or 8Mbps.

When the ingress or egress traffic bandwidth exceeds the configured threshold, flow control is triggered to limit the throughput. The control description is shown in register 0x020A ~0x0216, page 73.

## 7.21. Simple MIB Counter Support

Three 32-bit MIB counters (Counter 1, Counter 2, and Counter 3) are implemented on each port for basic traffic management and diagnostic purposes.

The MIB object of each counter is configurable. The MIB object selection on each counter is shown in Table 15. A detailed description is given in 9.8 MIB Counter Registers, page 12.

**Table 15. MIB Object Selection**

| MIB Object | Counter 1 | Counter 2 | Counter 3 |
|---|---|---|---|
| RX Packet Count | V | - | - |
| RX Byte Count | V | - | - |
| TX Packet Count | - | V | - |
| TX Byte Count | - | V | - |
| Drop Packet Count | - | - | V |
| Drop Byte Count | - | - | V |
| CRC Error Packet Count | V | V | V |
| Collision Count | V | V | V |

## 7.22. RRCP® Realtek Remote Control Protocol

The RRCP is a Realtek proprietary simple and easy device management program that is implemented for **in-band remote control** purposes.

The protocol is hardware ASIC based and does not require an external CPU. It allows the system administrator to get/set the switch configuration, to read the statistic counters, and to find RRCP aware devices.

The Remote Management Tool (RMT) software package is bundled with the RTL8326. The RMT is a Windows-based tool developed to enhance the functionality of Realtek's dumb layer 2 switches via software. The RMT gives network administrators the ability to remotely configure and monitor dumb layer 2 switches as though they were intelligent switches.

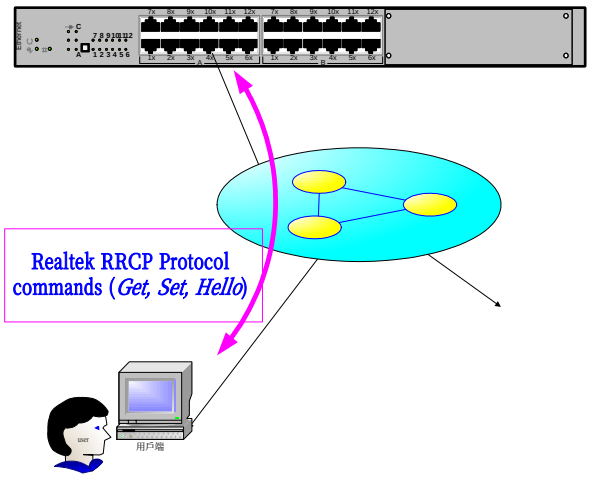



**Figure 7. Realtek Remote Control Protocol**

## 7.22.1. RRCP Capabilities

The RRCP is limited to the same network domain.

The RRCP supports the following:

1. Network Topology Discovery
2. Get/Set Configuration value of Register
3. Security Management by an Authentication Key and management port setting

Operation commands are:

Management Operation (1) register Get
(2) register Set
(3) Hello

Switch Operation (1) register Get Reply
(2) Hello Reply

The Hello Reply packet reports the switch's link vector information back to the manager (Downlink MAC, Downlink Port), (Uplink MAC, Uplink Port). The link vector information enables discovery of the network topology.

## 7.22.2. Management Security Scheme

Two RRCP security schemes are implemented:

**RRCP Management Authorized Port Control**

An authorized port can be configured via registers 0x0201~0x0202. Only RRCP packets originating from an authorized port will be processed and responded to. Other RRCP with DA=switch's MAC address will be dropped.

**Protocol Authentication Key control**

Each RRCP packet must contain the Authentication Key defined in the register 0x0209. After powering on, the Authentication Key is reset to the default value (0x2379). It can be updated through a valid RRCP Set command or through a Serial CPU interface.

## 7.22.3. RRCP® Protocol Packet Format

**Hello/Get/Set/Get_Reply Packet Format**

<table>
<tr><th>0</th><th>8</th><th>16</th><th>24</th><th>32</th></tr>
<tr><td colspan="5">DA (6)</td></tr>
<tr><td colspan="2">DA</td><td colspan="3">SA (6)</td></tr>
<tr><td colspan="5">SA</td></tr>
<tr><td colspan="2">RealtekEtherType (2)</td><td>Protocol (1)</td><td>r</td><td>OP Code (7bit)</td></tr>
<tr><td colspan="2">Authentication Key (2)</td><td colspan="3">Register Address (2)</td></tr>
<tr><td colspan="5">Register Data (4)</td></tr>
<tr><td colspan="5">Reserved (4)</td></tr>
<tr><td colspan="5">Reserved (4)</td></tr>
<tr><td colspan="5">Pad 00<br>:<br>:</td></tr>
<tr><td colspan="5">CRC (4)</td></tr>
</table>

**Figure 8. Hello/Get/Set/Get_Reply Packet Format**

**Table 16. Hello/Get/Set/Get_Reply Packet Format Description**

| Field | Length | Description | Value |
|---|---|---|---|
| DA | 6B | Destination MAC Address.<br>-For a Get, Set Packet, this is the unicast address of a switch.<br>-For a Get_Reply Packet, this is the unicast address of the management station.<br>-For a Hello Packet, this can be the unicast address of a switch or a broadcast address to all RRCP aware switches.<br>*Note: If the Authentication Key register has been updated after power on, the switch will only respond to a unicast Hello Packet.* | -- |
| SA | 6B | Source MAC address. | -- |
| RealtekEtherType | 2B | Identifies the packet as a Realtek Remote Control packet. The EtherType value=0x8899. | 0x8899 |
| Protocol | 1B | Realtek Proprietary protocol type definition.<br>01: Realtek Remote Control Protocol<br>Others: Reserved | 01h |
| OP Code | 7bit | Operation Code (7bit).<br>Code definition.<br>00: Hello packet<br>01: Get configuration<br>02: Set configuration | -- |
| r | 1 bit | Reply flag.<br>On receiving a control packet reply from the switch to the management station, this flag will be set to 1. Otherwise, this bit should be 0. | Station to switch: 0<br>Switch to station: 1 |

| Field | Length | Description | Value |
|---|---|---|---|
| Authentication Key | 2B | Authentication Key.<br>Used for security of the management operation.<br>The default Authentication key value is 0x2379.<br>The Key value can be modified by the administrator via a remote control packet.<br>A received control packet with a valid Destination MAC address but with an unmatched authentication key will be dropped with no reply.<br>If the DA is a broadcast address or is the address of another switch, it still will be relayed. | Default: 0x2379 |
| Register Address | 2B | Register address of the configuration. | -- |
| Register Data | 2B | Register data of the configuration. | -- |

## Hello_Reply Packet Format

| 0 | 8 | 16 | 24 | 32 |
|---|---|---|---|---|
| DA (6) | | | | |
| DA | | SA (6) | | |
| SA (=Downlink MAC) | | | | |
| RealtekEtherType (2) | | Protocol (1) | r | OP Code (7bit) |
| Authentication Key (2) | | Downlink Port (1) | | Uplink Port (1) |
| Uplink MAC (6) | | | | |
| Uplink MAC | | Chip ID (2) | | |
| Vender ID (4) | | | | |
| Pad 00<br>:<br>: | | | | |
| CRC (4) | | | | |

**Figure 9. Hello_Reply Packet Format**

**Table 17. Hello_Reply Packet Format Description**

| Field | Length | Description | Value |
|---|---|---|---|
| Downlink Port | 1B | Downlink Port number of the link vector.<br>Indicates the port number on the Hello Reply switch that is connected to the Uplink switch.<br>This is set by the Hello reply switch. | -- |
| Uplink Port | 1B | Uplink Port number of the link vector.<br>Indicates the port number of the Uplink switch that is connected to the Hello reply switch.<br>This is set by the Uplink switch. | Default=00h<br>Updated by the Uplink_MAC switch |
| Uplink MAC | 6B | The MAC address of the Uplink switch.<br>The default value is 000000000000h and is updated by the Uplink switch.<br>When a switch receives a Hello_Reply frame with zero UplinkMAC, then it will enter the SA MAC address here. | Default: 0 |
| Chip ID | 2B | Realtek Chip ID.<br>This is set by the Hello_Reply switch.<br>Each Realtek switch controller that is aware of the RRCP has a unique Chip ID (see 10.4.7 0x0206H: Chip Model ID, page 72). | EEPROM |

| Field | Length | Description | Value |
|---|---|---|---|
| Vender ID | 4B | Vender ID.<br>This is set by the Hello_Reply switch.<br>The 4-byte vender ID is reserved for the system vender to configure its company name or the device model ID. | EEPROM |

# 7.23. Network Loop Connection Fault Detection

The RTL8326 periodically transmits a Realtek-EtherType (=0x8899) protocol frame to detect network loop faults.

- Normal transmission time interval is five minutes
- If a port detects a loop, the loop event flag will be set (register 0x0101) and the transmission time interval will change to one second to speed up the new topology change detection.
- The loop event flag will be cleared and the transmission time interval will return to five minutes if the port does not receive a self-loop detect packet for 3 seconds.

**Loop Detect Packet Format**

The Loop Detect Packet Format is shown below:

| 0 | 8 | 16 | 24 | 32 |
|---|---|---|---|---|
| DA (6) [=0xffffffffffff] | | | | |
| DA | | SA (6)[=Switch MAC] | | |
| SA | | | | |
| RealtekEtherType (2) [=0x8899] | | Protocol (1) [=03] | Pad 0000 | |
| Pad 00000000<br>:<br>: | | | | |
| CRC (4) | | | | |

**Figure 10. Loop Detect Packet Format**

# 7.24. Realtek Echo Protocol

The Realtek Echo Protocol (REP) supports the Layer 2 Echo test. It is easy for a host to do network connection diagnostics through a simple test packet, with or without other hosts on the network. No IP assignment is required.

When the RTL8326 receives a REP packet, it replies by sending the original REP frame to the source MAC address with the DA and SA exchanged.

**Realtek Echo Protocol Frame**

The REP frame format is shown below:

<table>
<tr><th>0</th><th>8</th><th>16</th><th>24</th><th>32</th></tr>
<tr><td colspan="5">DA (6) [=0xffffffffffff]</td></tr>
<tr><td colspan="3">DA</td><td colspan="2">SA (6)[=Switch MAC]</td></tr>
<tr><td colspan="5">SA</td></tr>
<tr><td colspan="2">RealtekEtherType (2) [=0x8899]</td><td>Protocol (1) [=02]</td><td colspan="2">Pad 0000</td></tr>
<tr><td colspan="5">Pad 00000000<br>:<br>:</td></tr>
<tr><td colspan="5">CRC (4)</td></tr>
</table>

**Figure 11. Realtek Echo Protocol Frame**

# 7.25. Port Security Control

The RTL8326 supports a scheme for port security control by per-port disabling of MAC address auto-learning (register 0x0301~0x0302) and enabling of dropping packets with an unknown destination MAC address (register 0x0300). This feature requires that the MAC table aging process is disabled (to keep the known MAC address table static). If port security control is enabled, all incoming packets with unknown destination MAC addresses will be dropped. A detected unknown source MAC address will be captured on register 0x0303~0x0306.

The RTL8326 also supports a fast aging time setting (12 seconds) to quickly refresh the MAC address table (register 0x0300). A detailed description is given in Table 56, page 75, register 0x0300 ~ 0x0306.

# 7.26. Disable Port

A port can be disabled via the Port Disable Control Register (register 0x0608~0x0609). When a port is disabled, the port will cease all packet transmission and reception except for Realtek Remote Control Protocol (RRCP) packets. The physical link status is not changed.

# 7.27. Port Properties Configuration

The RTL8326 supports a flexible method to configure port properties via the PHY MII registers. Configurable properties include Media Speed (10M/100M/1000M), Duplex Mode, and 802.3x PAUSE flow control. The properties of each can be configured by auto-negotiation or force mode (disable auto negotiation).

The port link state will be reported in the port Link Status registers. The configuration description is shown in registers 0x060A ~ 0x0625.

Gigabit Port Pause Ability configuration is as follows:

**Table 18. Gigabit Port Pause**

| Local Device Setup (DUT) | | Link Partner Setup (Testing Device) | | Target Resolution | |
|---|---|---|---|---|---|
| PAUSE (1000Base-X: Reg4.7) or (1000Base-T: Reg4.10) | ASM_DIR (1000Base-X: Reg4.8) or (1000Base-T: Reg4.11) | PAUSE (1000Base-X: Reg5.7) or (1000Base-T: Reg5.10) | ASM_DIR (1000Base-X: Reg5.8) or (1000Base-T: Reg5.11) | **Local Resolution (DUT)** | **Link Partner Resolution (Testing Device)** |
| 1 ◄——► | - | 1 | - | Enable PAUSE TX/RX | Enable PAUSE TX/RX |
| 1 | 1 | 0 | 1 | Enable PAUSE RX ◄—— | Enable PAUSE TX |
| 0 | 1 | 1 | 1 | Enable PAUSE TX ——► | Enable PAUSE RX |
| Others | | Others | | Disable PAUSE | Disable PAUSE |

The following shows how to configure the Pause and Asymmetric Pause ability on port property registers (0x060A~0x0616) to get an expected negotiation result.

**Table 19. Configuring Pause and Asymmetric Pause**

| PAUSE | Asymmetric PAUSE | Expected PAUSE Result |
|---|---|---|
| 0 | 0 | Disable |
| 0 | 1 | Asymmetric to Link Partner |
| 1 | 0 | Symmetric |
| 1 | 1 | Asymmetric to Link Local or Symmetric |

# 7.28. Serial CPU Interface

The RTL8326 supports a serial CPU interface (Slave mode) that shares the same hardware pin (SCK, SDA) as the EEPROM interface (Master mode). The EEPROM and Serial interface can coexist by assigning a different device ID. Define EEPROM device ID=1010-000, RTL8326 device ID=1010-100. The interface is compatible with EEPROM 24LC024.

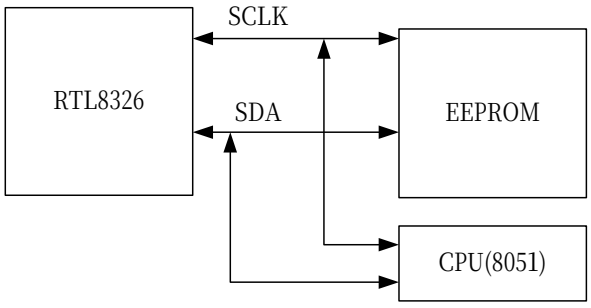



**Figure 12. Serial CPU Interface**

The serial CPU interface is enabled after the EEPROM download has finished. When operating in serial CPU mode the SCK is an input pin. The SDA is an IO pin with internal pull high.

## 7.28.1. Serial-CPU Access Format

In Serial CPU mode, 16-bit and 32-bit data access are both supported by the RTL8326. The Serial Read Write access format is as follows.

- 16-bit Address (MSB first)
- 16/32-bit data Burst Read (Low byte (Byte0) first; MSB first)
- 16/32-bit data Burst Write (Low byte (Byte0) first; MSB first)

*Note: Each burst is one byte.*

**Start and Stop Definition (START; STOP)**

A high-to-low transition of SDA with SCLK high is a START condition and it must precede any other command.

A LOW to HIGH transition of the SDA line while the clock (SCLK) is HIGH determines a STOP condition. All operations must end with a STOP.

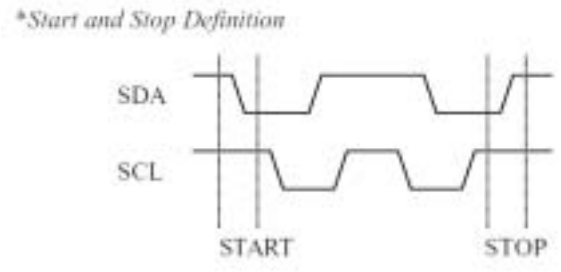



**Figure 13. Start and Stop Definition**

**Output Acknowledge (ACK)**

When addressed, each receiving device is obliged to generate an acknowledgment after reception of each byte.

The master device must generate an extra clock pulse that is associated with this acknowledgement bit.

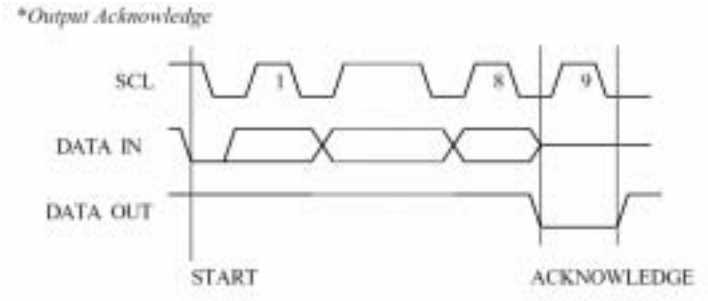



**Figure 14. Output Acknowledge (ACK)**

**Data Valid**

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

**Serial CPU 16-Bit Read/Write Format**

| Bit Width | 1 | 4 | 3 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Operation | Start Bit | Control code | Chip Select | R/~W | Ack | Reg. Addr. [7:0] (MSB first) | Ack | Reg. Addr. [15:8] (MSB first) | Ack | Reg. Data. [7:0] (MSB first) | Ack | Reg. Data [15:8] (MSB first) | Ack | Stop Bit |
| 16-bit Read | Start | 1010 | 100 | 1 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Read Data | 0 (*B) | Read Data | 1 (*B) | Stop |
| 16-bit Write | Start | 1010 | 100 | 0 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 1 (*A) | Stop |

**Figure 15. Serial CPU 16-Bit Read/Write Format**

*Note: *A = ACK by RTL8326. *B = ACK by CPU*

**Serial CPU 32-Bit Read/Write Format**

| Bit Width | 1 | 4 | 3 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Operation | Start Bit | Control code | Chip Select | R/ ~W | Ack | Reg. Addr. [7:0] (MSB first) | Ack | Reg. Addr. [15:8] (MSB first) | Ack | Reg. Data. [7:0] (MSB first) | Ack | Reg. Data. [7:0] (MSB first) | Ack | Reg. Data. [7:0] (MSB first) | Ack | Reg. Data [15:8] (MSB first) | Ack | Stop Bit |
| 32-bit Read | Start | 1010 | 100 | 1 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Read Data | 0 (*B) | Read Data | 0 (*B) | Read Data | 0 (*B) | Read Data | 1 (*B) | Stop |
| 32-bit Write | Start | 1010 | 100 | 0 | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 0 (*A) | Write Data | 1 (*A) | Stop |

**Figure 16. Serial CPU 32-Bit Read/Write Format**

*Note: *A = ACK by RTL8326. *B = ACK by CPU*

# 7.29. PHY Serial Management Interface

The RTL8326 supports PHY management through the serial MDIO and MDC signal (SMI) to start the auto-negotiation process. After a power-on reset, the RTL8326 writes its abilities to the advertisement registers 0, 4, and 9 of the connected PHY and commands the PHY to restart the auto negotiation process. The PHY device address setting is defined as:

Address 2, 3 for port G0, G1

Address 8~31 for Fast Ethernet ports 0~23

After restarting auto-negotiation, the RTL8326 will continuously read the link status and abilities of local and link partners to determine the link state.

Port properties (speed, duplex, 802.3x flow control) can be configured via auto-negotiation or force mode. The configuration is described in register 0x060A ~ 0x0616. The final link status is reported in register 0x0619~0x0625.

## 7.29.1. SMI (MDC, MDIO) Interface

**SMI (MDC, MDIO) Management Packet Format**

**Table 20. SMI (MDC, MDIO) Management Packet Format**

| | Management Frame Fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **PRE** | **ST** | **OP** | **PHYAD** | **REGAD** | **TA** | **DATA** | **IDLE** |
| **Read** | 1…1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| **Write** | 1…1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

## 7.29.2. PHY Register Indirect Access

The RTL8326 supports the ability to randomly access PHY registers through a set of control registers at 0x0500~0x0502. Users need to define the PHY address ID, PHY Register ID, Data content of the write command, and operating command type (Read or Write) on the above registers. Then the RTL8326 will auto process the PHY Read/Write access through the MDC/MDIO interface.

**Read PHY Register Procedure**

Configure PHY Access Control Register (0x0500)

Read the result on PHY Access Read Data Register (0x0502)

**Write PHY Register Procedure**

Write the PHY Access Write Data Register (0x0501)

Configure the PHY Access Control Register (0x0500)

**PHY Address ID Definition**

The PHY address ID corresponds to the port location. The PHY address ID of Ports 0~23 are 0x08, 0x09, 0x0A, …., 0x1F. The PHY ID of ports 24 & 25 (Gigabit ports G0, G1) are 0x02, 0x03.

# 7.30. General Purpose I/O Interface

A 4-bit user defined I/O interface pin is supported on PIN USR_IO[3:0] and register 0x0004 (General Purpose User Defined I/O Data Register). This is an input interface. Users can connect it to any real-time level-trigger signal output circuit for control or diagnostic purposes. For example, it can be used to detect the fan, temperature sensor, or other fault detect circuit.

# 7.31. LED Interfaces

The RTL8326 provides a flexible per-port LED display to show the per-port link status and diagnostic information. Both a parallel and serial interface are provided to drive the LEDs.

During power on reset, the parallel LED signals are driven low and the serial interface shifts to a low value for about two seconds to turn on all the LEDs for testing purposes.

# 7.32. Parallel LED Interface

The parallel interface only provides a Gigabit port status LED and system status LED.

LED signals include: LED_Glink#/ACT[1:0], LED_loopDet#, LED_BISTFail#, LED_EnTrunk[7:0]#.

# 7.33. Serial LED Interface

The serial interface, SLED_CLK, and SLED_DATA provide clock and data to enable the external shift registers 74164 to capture the per-port link status and diagnostic information.

Another pin, SLED_DMODE_CK, provides the diagnostic items selection control. Each pulse signal input from this pin changes the diagnostic item to be displayed on the diagnostic LED.

Each port provides three port state LEDs (StateLED) and one diagnostic LED (DiagLED). The LED display type can be flexibly configured and can be enabled or disabled to achieve the optimal BOM cost.

The LED display configuration is controlled by register 0x0005h 'LED Display Configuration Register', and can also be configured via EEPROM.

The StateLED display is defined by StatLED_mode[2:0] on register 0x0005. The available display types are shown in the following table.

**Table 21. Serial LED Interface**

| **StatLEDn_mode[2:0]** | **000** | **001** | **010** | **011** | **100** | **101** | **110** | **111** |
|---|---|---|---|---|---|---|---|---|
| **StateLEDn Display Type** | Link /Act | 100Spd | Duplex /Col | Link/Act /100Spd | Duplex | Act | Link | Col |

The display items of the diagnostic LED (DiagLED) are internally defined and are as follows:

| | |
|---|---|
| (DiagItem_0) DisablePort/RxError | ON: Disabled port. Blinking: RX CRC error |
| (DiagItem_1) FlowControl/FCActive | ON: Flow control enabled. Blinking: Flow control active |
| (DiagItem_2) TrunkPort/TKFault | ON: Trunking enabled port. Blinking: Trunk fault warning |
| (DiagItem_3) HighPriorityPort | ON: High priority port |
| (DiagItem_4) LoopDetectPort | ON: Network loop connection fault detect |
| (DiagItem_5) BroadcastStormAlarmPort | ON: Broadcast Storm Alarm port |
| (DiagItem_6) NULL | Reserved for TX Utilization testing mode |
| (DiagItem_7) NULL | Reserved for RX Utilization testing mode |

The DiagLED display item is changed by a trigger signal input from hardware pin 'SLED_DMODE_CK'. The change sequence order of the DiagLED is:

DiagItem_0 → DiagItem_1→ DiagItem_2→ ……. → DiagItem_7→ Loop to DiagItem_0

## 7.33.1. Serial LED Display Panel Example (4 LEDs, Register 0x0005)

Enable serial LED display mode:

➔ set EnSerialMode: 1

Define the per-port 4 LED display mode:

➔ Configuration. set EnLED[3:0]: 1111

Define the statLED display type as: StatLED0=Link/Act, StatLED1=10/100M, StatLED2=Duplex/Collision:

➔ Configuration. set StatLED0_mode[2:0]=000, StatLED1_mode[2:0]=001, StatLED2_mode[2:0]=010

Follow the same method to configure the per-port 1 LED, per-port 2 LED, and per-port 3 LED display mode, with or without enabling the diagnostic LED.

The LED panel is shown in Figure 17.

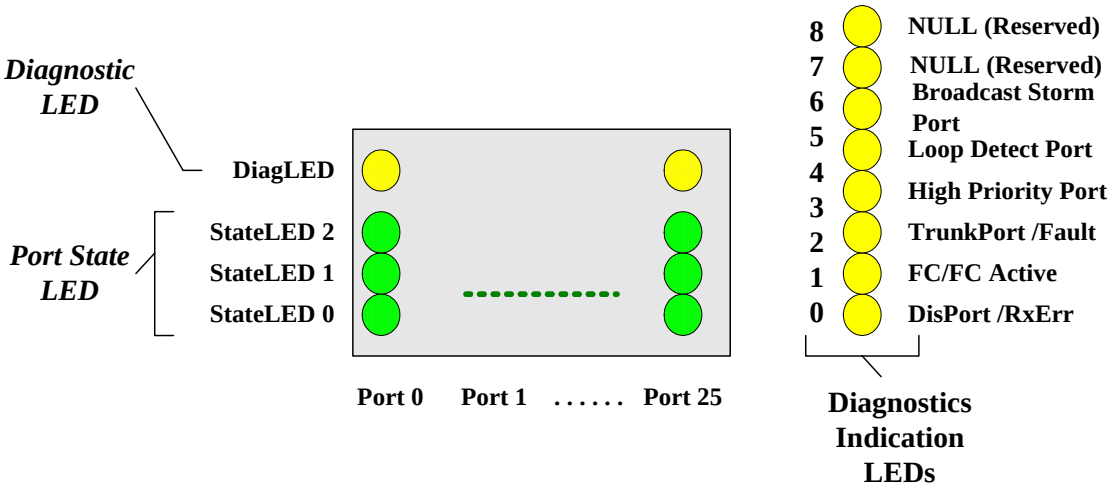



**Figure 17. Serial LED Display**

## 7.33.2. Serial LED Shift Out Sequence Order

The Serial LED output sequence is defined as follows: (first bit →….→ last bit).

Each port has four LEDs. There are eight diagnostic LEDs:

→ [P0 StateLED0] → [P0 StateLED1] → [P0 StateLED2] → [P0 DiagLED0]
→ [P1 StateLED0] → [P1 StateLED1] → [P1 StateLED2] → [P1 DiagLED0]
→- - - - - - - - - - - - →- - - - - - - - - - - - →- - - - - - - - - - - - →- - - - - - - - - - - -
→ [P25 StateLED0] → [P25 StateLED1] → [P25 StateLED2] → [P25 DiagLED0]
→ [Reserved_(DiagS0)] → [Reserved_(DiagS1)] → [Reserved_(DiagS2)] → [Reserved_(DiagS3)]
→ [Reserved_(DiagS4)] → [Reserved_(DiagS5)] → [Reserved_(DiagS6)] → [Reserved_(DiagS7)]

# 8. Serial EEPROM Configuration (24LC024)

The EEPROM Configuration bits are directly mapped to some of the internal registers. For example, EEPROM addresses 0x00h and 0x01h directly map to internal register 0x0002 ‘RX IO PAD Delay Configuration’.

The mapping rule is: EEPROM 0x00h: REG. 0x0002[7:0], EEPROM 0x01h: REG. 0x0002[15:8]

## 8.1. EEPROM Configuration vs. Internal Register Mapping Table

**Table 22. EEPROM Configuration vs. Internal Register Mapping Table**

| EEPROM Physical Address (8-Bit Data Entry) (24LC02) | Description | Corresponding Internal Register Address Mapping | Internal Default Value |
|---|---|---|---|
| 0x 01~00 | RX IO PAD Delay Configuration<br>Bit[5:0] value MUST be 000000<br>(Bit 5 is used for BIST enable/disable of Control Point (CP) test) | 0x0002 | 0A80 |
| 0x 03~02 | TX IO PAD Delay Configuration | 0x0003 | 0140 |
| 0x 05~04 | LED Display Configuration | 0x0005 | 1E88 |
| 0x 07~06 | Reserved | x | -- |
| 0x 09~08 | Reserved | x | -- |
| 0x 0B~0A | Reserved | x | -- |
| 0x 0D~0C | Realtek Protocol Control | 0x0200 | 0000 |
| 0x 0F~0E | RRCP security Mask Configuration 0 | 0x0201 | 0000 |
| 0x 11~10 | RRCP security Mask Configuration 1 | 0x0202 | 0000 |
| 0x 13~12 | Switch MAC ID 0 | 0x0203 | 0000 |
| 0x 15~14 | Switch MAC ID 1 | 0x0204 | 0000 |
| 0x 17~16 | Switch MAC ID 2 | 0x0205 | 0000 |
| 0x 19~18 | Chip Model ID | 0x0206 | 0000 |
| 0x 1B~1A | Vender ID 0 | 0x0207 | 0000 |
| 0x 1D~1C | Vender ID 1 | 0x0208 | 0000 |
| 0x 1F~1E | Reserved | x | -- |
| 0x 21~20 | Reserved | x | -- |
| 0x 23~22 | ALT Configuration | 0x0300 | 0004 |
| 0x 25~24 | Port Trunking Configuration | 0x0307 | 0000 |
| 0x 27~26 | IGMP Snooping Control | 0x0308 | 0000 |
| 0x 29~28 | VLAN Control | 0x030B | 0000 |
| 0x 2B~2A | Reserved | x | -- |
| 0x 2D~2C | Reserved | x | -- |
| 0x 2F~2E | QoS Control | 0x0400 | 0010 |
| 0x 31~30 | Port Priority Configuration 0 | 0x0401 | 0000 |
| 0x 33~32 | Port Priority Configuration 1 | 0x0402 | 0000 |
| 0x 35~34 | Reserved | x | -- |
| 0x 37~36 | Reserved | x | -- |
| 0x 39~38 | Global Port Control Register | 0x0607 | 0010 |
| 0x 3B~3A | Port Property Configuration 0 | 0x060A | AFAF |
| 0x 3D~3C | Port Property Configuration 1 | 0x060B | AFAF |
| 0x 3F~3E | Port Property Configuration 2 | 0x060C | AFAF |
| 0x 41~40 | Port Property Configuration 3 | 0x060D | AFAF |

| EEPROM Physical Address (8-Bit Data Entry) (24LC02) | Description | Corresponding Internal Register Address Mapping | Internal Default Value |
|---|---|---|---|
| 0x 43~42 | Port Property Configuration 4 | 0x060E | AFAF |
| 0x 45~44 | Port Property Configuration 5 | 0x060F | AFAF |
| 0x 47~46 | Port Property Configuration 6 | 0x0610 | AFAF |
| 0x 49~48 | Port Property Configuration 7 | 0x0611 | AFAF |
| 0x 4B~4A | Port Property Configuration 8 | 0x0612 | AFAF |
| 0x 4D~4C | Port Property Configuration 9 | 0x0613 | AFAF |
| 0x 4F~4E | Port Property Configuration 10 | 0x0614 | AFAF |
| 0x 51~50 | Port Property Configuration 11 | 0x0615 | AFAF |
| 0x 53~52 | Port Property Configuration 12 | 0x0616 | BFBF |
| 0x 55~54 | Reserved | x | -- |
| 0x 57~56 | Reserved | x | -- |
| 0x 58 ------- 0x 5f | Reserved | x | -- |
| 0x 61~60 | Diagnostic Configuration purposes (must be configured as 0000) | 0xFFFF | 0000 |

# 9. Internal Register Descriptions

Register Symbols:

R: Read

W: Write

RW: Read/Write

*Note: Pin = Supports hardware pin strapping.*

*EE = Supports EEPROM configuration.*

## 9.1. System Configuration Registers

**Table 23. System Configuration Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0000 | 0 | System Reset Control Register. | W | 0 | | |
| | 1 | Switch Parameter Register. | RW | 0480 | V | |
| | 2 | RX I/O PAD Delay Configuration. | R | 0A80 | | V |
| | 3 | TX I/O PAD Delay Configuration. | R | 0140 | | V |
| | 4 | General Purpose User Define I/O Data Register. | R | 0 | V | |
| | 5 | LED Display Configuration. | RW | 1E88 | | V |

## 9.2. System Status Registers

**Table 24. System Status Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0100 | 0 | Board Trapping Status Register. | RW | 0 | V | |
| | 1 | Loop Detect Status Register (32-bit). | R | 0 | | |
| | 2 | System Fault Indication Register. | R | 0 | | |

## 9.3. Management Configuration Registers

**Table 25. Management Configuration Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0200 | 0 | Realtek Protocol Control Register. | RW | 0 | V | V |
| | 1 | RRCP Security Mask Configuration 0. | RW | 0 | | V |
| | 2 | RRCP Security Mask Configuration 1. | RW | 0 | | V |
| | 3 | Switch MAC ID Register 0. | R | 0 | | V |
| | 4 | Switch MAC ID Register 1. | R | 0 | | V |
| | 5 | Switch MAC ID Register 2. | R | 0 | | V |
| | 6 | Chip Mode ID. | R | 0 | | V |
| | 7 | System Vender ID Register 0. | R | 0 | | V |
| | 8 | System Vender ID Register 1. | R | 0 | | V |
| | 9 | RRCP Authentication Key Configuration Register. | R | 2379 | | |
| | A | Port 0, 1 Bandwidth Control Register. | RW | 0 | | |
| | B | Port 2, 3 Bandwidth Control Register. | RW | 0 | | |
| | C | Port 4, 5 Bandwidth Control Register. | RW | 0 | | |
| | D | Port 6, 7 Bandwidth Control Register. | RW | 0 | | |
| | E | Port 8, 9 Bandwidth Control Register. | RW | 0 | | |
| | F | Port 10, 11 Bandwidth Control Register. | RW | 0 | | |
| | 10 | Port 12, 13 Bandwidth Control Register. | RW | 0 | | |
| | 11 | Port 14, 15 Bandwidth Control Register. | RW | 0 | | |
| | 12 | Port 16, 17 Bandwidth Control Register. | RW | 0 | | |
| | 13 | Port 18, 19 Bandwidth Control Register. | RW | 0 | | |
| | 14 | Port 20, 21 Bandwidth Control Register. | RW | 0 | | |
| | 15 | Port 22, 23 Bandwidth Control Register. | RW | 0 | | |
| | 16 | Port 24, 25 Bandwidth Control Register. | RW | 0 | | |

## 9.4. Address Lookup Table (ALT) Control Register

**Table 26. Address Lookup Table (ALT) Control Register**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0300 | 0 | ALT Configuration Register. | RW | 0004 | V | V |
| | 1 | Address Learning Control Register 0. | RW | 0 | | |
| | 2 | Address Learning Control Register 1. | RW | 0 | | |
| | 3 | Unknown SA Capture Register 0. | R | 0 | | |
| | 4 | Unknown SA Capture Register 1. | R | 0 | | |
| | 5 | Unknown SA Capture Register 2. | R | 0 | | |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 6 | Unknown SA Status Register. | R | 0 | | |
| | 7 | Port Trunking Configuration Register. | RW | 0 | | V |
| | 8 | IGMP Snooping Control Register. | RW | 0 | V | V |
| | 9 | IP Multicast Router Port Discovery Register (32-bit). | R | 0 | | |
| | A | Reserved. | -- | -- | | |
| | B | VLAN Control Register. | RW | 0 | V | V |
| | C | Port VLAN ID Assignment Index Register 0 (Port 0, 1). | RW | 0100 | | |
| | D | Port VLAN ID Assignment Index Register 1 (Port 2, 3). | RW | 0302 | | |
| | E | Port VLAN ID Assignment Index Register 2 (Port 4, 5). | RW | 0504 | | |
| | F | Port VLAN ID Assignment Index Register 3 (Port 6, 7). | RW | 0706 | | |
| | 10 | Port VLAN ID Assignment Index Register 4 (Port 8, 9). | RW | 0908 | | |
| | 11 | Port VLAN ID Assignment Index Register 5 (Port 10, 11). | RW | 0B0A | | |
| | 12 | Port VLAN ID Assignment Index Register 6 (Port 12, 13). | RW | 0D0C | | |
| | 13 | Port VLAN ID Assignment Index Register 7 (Port 14, 15). | RW | 0F0E | | |
| | 14 | Port VLAN ID Assignment Index Register 8 (Port 16, 17). | RW | 1110 | | |
| | 15 | Port VLAN ID Assignment Index Register 9 (Port 18, 19). | RW | 1312 | | |
| | 16 | Port VLAN ID Assignment Index Register 10 (Port 20, 21). | RW | 1514 | | |
| | 17 | Port VLAN ID Assignment Index Register 11 (Port 22, 23). | RW | 1716 | | |
| | 18 | Port VLAN ID Assignment Index Register 12 (Port 24, 25). | RW | 1918 | | |
| | 19 | VLAN Output Port Priority-tagging Control Register 0 (P#0~7). | RW | FFFF | | |
| | 1A | VLAN Output Port Priority-tagging Control Register 1 (P#8~15). | RW | FFFF | | |
| | 1B | VLAN Output Port Priority-tagging Control Register 2 (P#16~23). | RW | FFFF | | |
| | 1C | VLAN Output Port Priority-tagging Control Register 3 (P#24~25). | RW | FFFF | | |
| | | VLAN Table Configuration Registers. | | | | |
| | 1D | VLAN_0_Entry_Configuration_0 (member[15:0]). | RW | 0001 | | |
| | 1E | VLAN_0_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 1F | VLAN_0_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 20 | VLAN_1_Entry_Configuration_0 (member[15:0]). | RW | 0002 | | |
| | 21 | VLAN_1_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 22 | VLAN_1_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 23 | VLAN_2_Entry_Configuration_0 (member[15:0]). | RW | 0004 | | |
| | 24 | VLAN_2_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 25 | VLAN_2_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 26 | VLAN_3_Entry_Configuration_0 (member[15:0]). | RW | 0008 | | |
| | 27 | VLAN_3_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 28 | VLAN_3_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 29 | VLAN_4_Entry_Configuration_0 (member[15:0]). | RW | 0010 | | |
| | 2A | VLAN_4_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 2B | VLAN_4_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 2C | VLAN_5_Entry_Configuration_0 (member[15:0]). | RW | 0020 | | |
| | 2D | VLAN_5_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 2E | VLAN_5_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 2F | VLAN_6_Entry_Configuration_0 (member[15:0]). | RW | 0040 | | |
| | 30 | VLAN_6_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 31 | VLAN_6_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 32 | VLAN_7_Entry_Configuration_0 (member[15:0]). | RW | 0080 | | |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 33 | VLAN_7_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 34 | VLAN_7_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 35 | VLAN_8_Entry_Configuration_0 (member[15:0]). | RW | 0100 | | |
| | 36 | VLAN_8_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 37 | VLAN_8_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 38 | VLAN_9_Entry_Configuration_0 (member[15:0]). | RW | 0200 | | |
| | 39 | VLAN_9_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 3A | VLAN_9_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 3B | VLAN_10_Entry_Configuration_0 (member[15:0]). | RW | 0400 | | |
| | 3C | VLAN_10_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 3D | VLAN_10_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 3E | VLAN_11_Entry_Configuration_0 (member[15:0]). | RW | 0800 | | |
| | 3F | VLAN_11_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 40 | VLAN_11_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 41 | VLAN_12_Entry_Configuration_0 (member[15:0]). | RW | 1000 | | |
| | 42 | VLAN_12_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 43 | VLAN_12_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 44 | VLAN_13_Entry_Configuration_0 (member[15:0]). | RW | 2000 | | |
| | 45 | VLAN_13_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 46 | VLAN_13_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 47 | VLAN_14_Entry_Configuration_0 (member[15:0]). | RW | 4000 | | |
| | 48 | VLAN_14_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 49 | VLAN_14_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 4A | VLAN_15_Entry_Configuration_0 (member[15:0]). | RW | 8000 | | |
| | 4B | VLAN_15_Entry_Configuration_1 (member[25:16]). | RW | 0300 | | |
| | 4C | VLAN_15_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 4D | VLAN_16_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 4E | VLAN_16_Entry_Configuration_1 (member[25:16]). | RW | 0301 | | |
| | 4F | VLAN_16_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 50 | VLAN_17_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 51 | VLAN_17_Entry_Configuration_1 (member[25:16]). | RW | 0302 | | |
| | 52 | VLAN_17_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 53 | VLAN_18_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 54 | VLAN_18_Entry_Configuration_1 (member[25:16]). | RW | 0304 | | |
| | 55 | VLAN_18_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 56 | VLAN_19_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 57 | VLAN_19_Entry_Configuration_1 (member[25:16]). | RW | 0308 | | |
| | 58 | VLAN_19_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 59 | VLAN_20_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 5A | VLAN_20_Entry_Configuration_1 (member[25:16]). | RW | 0310 | | |
| | 5B | VLAN_20_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 5C | VLAN_21_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 5D | VLAN_21_Entry_Configuration_1 (member[25:16]). | RW | 0320 | | |
| | 5E | VLAN_21_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 5F | VLAN_22_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 60 | VLAN_22_Entry_Configuration_1 (member[25:16]). | RW | 0340 | | |
| | 61 | VLAN_22_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 62 | VLAN_23_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 63 | VLAN_23_Entry_Configuration_1 (member[25:16]). | RW | 0380 | | |
| | 64 | VLAN_23_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 65 | VLAN_24_Entry_Configuration_0 (member[15:0]). | RW | FFFF | | |
| | 66 | VLAN_24_Entry_Configuration_1 (member[25:16]). | RW | 03FF | | |
| | 67 | VLAN_24_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 68 | VLAN_25_Entry_Configuration_0 (member[15:0]). | RW | FFFF | | |
| | 69 | VLAN_25_Entry_Configuration_1 (member[25:16]). | RW | 03FF | | |
| | 6A | VLAN_25_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 6B | VLAN_26_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 6C | VLAN_26_Entry_Configuration_1 (member[25:16]). | RW | 0000 | | |
| | 6D | VLAN_26_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 6E | VLAN_27_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 6F | VLAN_27_Entry_Configuration_1 (member[25:16]). | RW | 0000 | | |
| | 70 | VLAN_27_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 71 | VLAN_28_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 72 | VLAN_28_Entry_Configuration_1 (member[25:16]). | RW | 0000 | | |
| | 73 | VLAN_28_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 74 | VLAN_29_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 75 | VLAN_29_Entry_Configuration_1 (member[25:16]). | RW | 0000 | | |
| | 76 | VLAN_29_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 77 | VLAN_30_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 78 | VLAN_30_Entry_Configuration_1 (member[25:16]). | RW | 0000 | | |
| | 79 | VLAN_30_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |
| | 7A | VLAN_31_Entry_Configuration_0 (member[15:0]). | RW | 0000 | | |
| | 7B | VLAN_31_Entry_Configuration_1 (member[25:16]). | RW | 0000 | | |
| | 7C | VLAN_31_Entry_Configuration_2 (VID[11:0]). | RW | 0000 | | |

# 9.5. Queue Control Registers

**Table 27. Queue Control Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0400 | 0 | QoS Control Register. | RW | 0010 | V | V |
| | 1 | Port Priority Configuration Register 0. | RW | 0 | V | V |
| | 2 | Port Priority Configuration Register 1. | RW | 0 | | V |

# 9.6. PHY Access Control Register

**Table 28. PHY Access Control Register**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0500 | 0 | PHY Access Control Register. | RW | 0 | | |
| | 1 | PHY Access Write Data Register. | RW | 0 | | |
| | 2 | PHY Access Read Data Register. | R | 0 | | |

# 9.7. Port Control Registers

**Table 29. Port Control Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0600 | 0~6 | Reserved. | -- | -- | | |
| | 7 | Global Port Control Register. | RW | 0010 | V | V |
| | 8 | Port Disable Control Register 0. | RW | 0 | | |
| | 9 | Port Disable Control Register 1. | RW | 0 | | |
| | A | Port Property Configuration Register 0 (Port 0, 1). | RW | AFAF | | V |
| | B | Port Property Configuration Register 1 (Port 2, 3). | RW | AFAF | | V |
| | C | Port Property Configuration Register 2 (Port 4, 5). | RW | AFAF | | V |
| | D | Port Property Configuration Register 3 (Port 6, 7). | RW | AFAF | | V |
| | E | Port Property Configuration Register 4 (Port 8, 9). | RW | AFAF | | V |
| | F | Port Property Configuration Register 5 (Port 10, 11). | RW | AFAF | | V |
| | 10 | Port Property Configuration Register 6 (Port 12, 13). | RW | AFAF | | V |
| | 11 | Port Property Configuration Register 7 (Port 14, 15). | RW | AFAF | | V |
| | 12 | Port Property Configuration Register 8 (Port 16, 17). | RW | AFAF | | V |
| | 13 | Port Property Configuration Register 9 (Port 18, 19). | RW | AFAF | | V |
| | 14 | Port Property Configuration Register 10 (Port 20, 21). | RW | AFAF | | V |
| | 15 | Port Property Configuration Register 11 (Port 22, 23). | RW | AFAF | | V |
| | 16 | Port Property Configuration Register 12 (Port 24, 25). | RW | BFBF | | V |
| | 17~18 | Reserved. | -- | -- | | |
| | 19 | Port Link Status Register 0 (Port 0, 1). | R | 0 | | |
| | 1A | Port Link Status Register 1 (Port 2, 3). | R | 0 | | |
| | 1B | Port Link Status Register 2 (Port 4, 5). | R | 0 | | |
| | 1C | Port Link Status Register 3 (Port 6, 7). | R | 0 | | |
| | 1D | Port Link Status Register 4 (Port 8, 9). | R | 0 | | |
| | 1E | Port Link Status Register 5 (Port 10, 11). | R | 0 | | |
| | 1F | Port Link Status Register 6 (Port 12, 13). | R | 0 | | |
| | 20 | Port Link Status Register 7 (Port 14, 15). | R | 0 | | |
| | 21 | Port Link Status Register 8 (Port 16, 17). | R | 0 | | |
| | 22 | Port Link Status Register 9 (Port 18, 19). | R | 0 | | |
| | 23 | Port Link Status Register 10 (Port 20, 21). | R | 0 | | |
| | 24 | Port Link Status Register 11 (Port 22, 23). | R | 0 | | |
| | 25 | Port Link Status Register 12 (Port 24, 25). | R | 0 | | |

# 9.8. MIB Counter Registers

**Table 30. MIB Counter Registers**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | 0 | Port MIB Counter Object Selection Register 0 (Port 0, 1). | RW | 0555 | | |
| | 1 | Port MIB Counter Object Selection Register 1 (Port 2, 3). | RW | 0555 | | |
| | 2 | Port MIB Counter Object Selection Register 2 (Port 4, 5). | RW | 0555 | | |
| | 3 | Port MIB Counter Object Selection Register 3 (Port 6, 7). | RW | 0555 | | |
| | 4 | Port MIB Counter Object Selection Register 4 (Port 8, 9). | RW | 0555 | | |
| | 5 | Port MIB Counter Object Selection Register 5 (Port 10, 11). | RW | 0555 | | |
| | 6 | Port MIB Counter Object Selection Register 6 (Port 12, 13). | RW | 0555 | | |
| | 7 | Port MIB Counter Object Selection Register 7 (Port 14, 15). | RW | 0555 | | |

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| | 8 | Port MIB Counter Object Selection Register 8 (Port 16, 17). | RW | 0555 | | |
| | 9 | Port MIB Counter Object Selection Register 9 (Port 18, 19). | RW | 0555 | | |
| | A | Port MIB Counter Object Selection Register 10 (Port 20, 21). | RW | 0555 | | |
| | B | Port MIB Counter Object Selection Register 11 (Port 22, 23). | RW | 0555 | | |
| | C | Port MIB Counter Object Selection Register 12 (Port 24, 25). | RW | 0555 | | |

## 9.8.1. Port MIB Counter 1 Register (RX Counter) (32-bits)

**Table 31. Port MIB Counter 1 Register (RX Counter) (32-bits)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | D | Port 0 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | E | Port 1 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | F | Port 2 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 10 | Port 3 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 11 | Port 4 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 12 | Port 5 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 13 | Port 6 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 14 | Port 7 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 15 | Port 8 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 16 | Port 9 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 17 | Port 10 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 18 | Port 11 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 19 | Port 12 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 1A | Port 13 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 1B | Port 14 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 1C | Port 15 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 1D | Port 16 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 1E | Port 17 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 1F | Port 18 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 20 | Port 19 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 21 | Port 20 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 22 | Port 21 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 23 | Port 22 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 24 | Port 23 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 25 | Port 24 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |
| | 26 | Port 25 MIB Counter 1 Register (RX Counter) (32-bits). | R | 0 | | |

## 9.8.2. Port MIB Counter 2 Register (TX Counter) (32-bits)

**Table 32. Port MIB Counter 2 Register (TX Counter) (32-bits)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | 27 | Port 0 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 28 | Port 1 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 29 | Port 2 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 2A | Port 3 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 2B | Port 4 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 2C | Port 5 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 2D | Port 6 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 2E | Port 7 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 2F | Port 8 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 30 | Port 9 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 31 | Port 10 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 32 | Port 11 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 33 | Port 12 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 34 | Port 13 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 35 | Port 14 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 36 | Port 15 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 37 | Port 16 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 38 | Port 17 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 39 | Port 18 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 3A | Port 19 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 3B | Port 20 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 3C | Port 21 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 3D | Port 22 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 3E | Port 23 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 3F | Port 24 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |
| | 40 | Port 25 MIB Counter 2 Register (TX Counter) (32-bits). | R | 0 | | |

### 9.8.3. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

**Table 33. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0x0700 | 41 | Port 0 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 42 | Port 1 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 43 | Port 2 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 44 | Port 3 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 45 | Port 4 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 46 | Port 5 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 47 | Port 6 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 48 | Port 7 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 49 | Port 8 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 4A | Port 9 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 4B | Port 10 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 4C | Port 11 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 4D | Port 12 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 4E | Port 13 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 4F | Port 14 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 50 | Port 15 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 51 | Port 16 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 52 | Port 17 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 53 | Port 18 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 54 | Port 19 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 55 | Port 20 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 56 | Port 21 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 57 | Port 22 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 58 | Port 23 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 59 | Port 24 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |
| | 5A | Port 25 MIB Counter 3 Register (Diagnostic Counter) (32-bits). | R | 0 | | |

## 9.9. System Parameter Register (Reserved)

**Table 34. System Parameter Register (Reserved)**

| Register Base Address | Offset | Description | RW | Default | Pin | EE |
|---|---|---|---|---|---|---|
| 0xFFFF | -- | System Parameter Register (Reserved). | RW | 0 | V | V |

# 10. Internal Register Settings

Register Symbols:

| | | | |
|---|---|---|---|
| R: | Read | LL: | Latch Low until cleared |
| W: | Write | LH: | Latch High until cleared |
| RW: | Read/Write | SC: | Self Clearing |
| | | RC: | Read to Clear |

## 10.1. System Configuration Register

### 10.1.1. 0x0000H: System Reset Control Register

**Table 35. 0x0000H: System Reset Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | SRST | Soft Reset.<br>A soft reset will reset the system similar to a power on reset except that the user configuration will not be cleared:<br>1. The MAC table and VLAN table data will be kept.<br>2. All current user configured internal register values will be kept.<br>3. The EEPROM download will not be done again.<br>4. The system will restart the auto-negotiation process.<br>0: Normal<br>1: Soft reset | W/SC | 0 |
| 1 | HRST | Hardware Reset.<br>Resets the system to the power on initial state:<br>1. Downloads configuration from strap pin and EEPROM.<br>2. Starts internal Memory self test.<br>3. Clears all the MAC, VLAN tables.<br>4. Resets all registers to default values.<br>5. Restarts auto-negotiation.<br>0: Normal<br>1: Hardware reset | W/SC | 0 |
| 15:2 | Reserved | | | |

## 10.1.2. 0x0001H: Switch Parameter Register

*Note: The Write operation is reserved for IC testing mode. Do NOT write this register.*

**Table 36. 0x0001H: Switch Parameter Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 1:0 | MaxPktLen[1:0] | System Valid Max Packet Length.<br>The minimum packet length is 64 bytes. The maximum packet length is controlled by MaxPktLen[1:0]:<br>00: 1536 bytes (Default)<br>01: 1552 byte<br>1x: Reserved. | RW | HW pin MaxPktLen[1:0] |
| 2 | TXIPG_Comp | Transmit IPG Compensation.<br>Used to compensate the oscillator frequency or incoming packet Inter-Packet Gap (IPG) tolerance.<br>0: Give +65 ppm TXIPG compensation (Default)<br>1: Give +90 ppm TXIPG compensation | RW | HW pin TXIPG_Comp |
| 3 | MaxPauseCnt | Max Pause Count for Congestion Control.<br>0: Supports a maximum of 128 Pause frames during congestion control (Default)<br>1: Continue Pause mode. Do not limit the Pause frame count during congestion control. | RW | HW pin MaxPauseCnt |
| 4 | DisBKP48One | Disable Back pressure 48 Pass One Algorithm.<br>When the 48One algorithm is enabled, the switch will pass one incoming packet after every 48 collisions.<br>0: Enable 48 Pass One algorithm (Default)<br>1: Disable 48 Pass One algorithm | RW | HW pin DisBKP48One |
| 5 | SWTest | This is a system test bit. | RW | 0 |
| 6 | En24Drop | Enable congested Packet Drop after over per-port flow control threshold 24 buffer page.<br>When disabled, it allows reception of incoming packets until the output queue is full.<br>0: Disable (Default)<br>1: Enable | RW | HW pin En24Drop |
| 7 | EnCRSBKPMode | Enable Carrier Based Back Pressure Mode.<br>Half duplex back pressure algorithm selection.<br>0: Select Collision based back pressure mode<br>1: Select Carrier based back pressure mode (Default) | RW | HW pin EnCRSBKPmode |
| 8 | DisBkOffBIST | Disable Back Off Timer BIST.<br>0: Enable Back Off Timer BIST (Built-In Self Test)<br>1: Disable Back Off Timer BIST | RW | 0 |
| 9 | SpdBkOff | Speed Up Back Off Timer<br>0: Normal timer (Default)<br>1: Speed up timer | RW | HW pin EnSpdBkOff |
| 10 | EnBKPBkOff3 | Enable Advanced Back Pressure Back Off scheme.<br>0: Normal mode<br>1: Advanced mode; k: min (n, 3) | RW | 1 |
| 12:11 | PortDscThr[1:0] | Reserved for Port Descriptor Threshold Tuning Control Testing.<br>Keep the value at 00. | RW | 00 |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 14:13 | GlobalDscThr[1:0] | Reserved for Global Descriptor Threshold Tuning Control Testing purposes only.<br>Keep the value at 00. | RW | 00 |
| 15 | SpeedUp | Reserved for Speed Up Internal BIST Clock for Control Point (CP) Testing.<br>Keep the value at 0. | RW | HW pin EnSPDUP |

## 10.1.3. 0x0002H: RX I/O PAD Delay Configuration

**Table 37. 0x0002H: RX I/O PAD Delay Configuration**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 4:0 | Reserved (EEPROM check) | Reserved bits.<br>Used for EEPROM existence checking.<br>Keep the value at 000000. | R | 0 |
| 5 | DisBIST | Reserved for engineering test mode.<br>0: Enable BIST<br>1: Disable BIST<br>Keep the value at 0. | R<br>(W: EEPROM) | 0 |
| 7:6 | RxDelayF0_Cfg[1:0] | Fast Ethernet Port 0~7 SMII RX I/O PAD input delay Configuration.<br>00: Delay 0 ns (Default)<br>01: Delay 1 ns<br>10: Delay 2 ns (Recommend)<br>11: Delay 3 ns | R<br>(W: EEPROM) | HW pin. OCT0_RXD_Delay_2ns |
| 9:8 | RxDelayF1_Cfg[1:0] | Fast Ethernet Port 8~15 SMII RX I/O PAD input delay Configuration.<br>00: Delay 0 ns (Default)<br>01: Delay 1 ns<br>10: Delay 2 ns (Recommend)<br>11: Delay 3 ns | R<br>(W: EEPROM) | HW pin. OCT1_RXD_Delay_2ns |
| 11:10 | RxDelayF2_Cfg[1:0] | Fast Ethernet Port 16~23 SMII RX I/O PAD input delay Configuration.<br>00: Delay 0 ns (Default)<br>01: Delay 1 ns<br>10: Delay 2 ns (Recommend)<br>11: Delay 3 ns | R<br>(W: EEPROM) | HW pin. OCT2_RXD_Delay_2ns |
| 13:12 | RxDelayG0_Cfg[1:0] | Gigabit Port G0 GMII RX I/O PAD input delay Configuration.<br>00: Delay 0 ns (Default)<br>01: Delay 1 ns<br>10: Delay 2 ns<br>11: Delay 3 ns | R<br>(W: EEPROM) | 00 |
| 15:14 | RxDelayG1_Cfg[1:0] | Gigabit Port G1 GMII RX I/O PAD input delay Configuration.<br>00: Delay 0 ns (Default)<br>01: Delay 1 ns<br>10: Delay 2 ns<br>11: Delay 3 ns | R<br>(W: EEPROM) | 00 |

## 10.1.4. 0x0003H: TX I/O PAD Delay Configuration

**Table 38. 0x0003H: TX I/O PAD Delay Configuration**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 5:0 | Reserved | | | |
| 7:6 | TxDealyG0_Cfg[1:0] | Gigabit Port G0 GMII TX I/O PAD output delay Configuration.<br>00: Delay 0 ns<br>01: Delay 1 ns (Default)<br>10: Delay 2 ns<br>11: Delay 3 ns | R<br>(W: EEPROM) | 01 |
| 9:8 | TxDealyG1_Cfg[1:0] | Gigabit Port G1 GMII TX I/O PAD output delay Configuration.<br>00: Delay 0 ns<br>01: Delay 1 ns (Default)<br>10: Delay 2 ns<br>11: Delay 3 ns | R<br>(W: EEPROM) | 01 |
| 10 | TxDelayRefClk0 | Fast Ethernet Port 0~7 SMII REFCLK I/O PAD output delay Configuration.<br>0: Delay 0 ns (Default)<br>1: Delay 2 ns | R<br>(W: EEPROM) | 0 |
| 11 | TxDelayRefClk1 | Fast Ethernet Port 8~15 SMII REFCLK I/O PAD output delay Configuration.<br>0: Delay 0 ns (Default)<br>1: Delay 2 ns | R<br>(W: EEPROM) | 0 |
| 12 | TxDelayRefClk2 | Fast Ethernet Port 16~23 SMII REFCLK I/O PAD output delay Configuration.<br>00: Delay 0 ns (Default)<br>01: Delay 1 ns | R<br>(W: EEPROM) | 0 |
| 15:13 | Reserved | | | |

## 10.1.5. 0x0004H: General Purpose User Defined I/O Data Register

**Table 39. 0x0004H: General Purpose User Defined I/O Data Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 3:0 | USR_IOD[3:0] | User Defined I/O Data.<br>These bits reflect the real time value of the hardware pin USR_IO[3:0]. | R | HW pin:<br>USR_IOD[3:0] |
| 15:4 | Reserved | | | |

# 10.2. 0x0005H: LED Display Configuration

**Table 40. 0x0005H: LED Display Configuration**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 2:0 | StatLED0_mode[2:0] | Mode Selection for State LED0.<br>This state LED mode selection register controls the status type of the State LED0. The Status type is defined as follows:<br>000: Link/Act (Default)<br>001: 100Spd<br>010: Duplex/Col<br>011: Link/Act/100Spd<br>100: Duplex<br>101: Act<br>110: Link<br>111: Col | RW | 000 |
| 5:3 | StatLED1_mode[2:0] | Mode Selection for State LED1.<br>000: Link/Act (Default)<br>001: 100Spd<br>010: Duplex/Col<br>011: Link/Act/100Spd<br>100: Duplex<br>101: Act<br>110: Link<br>111: Col | RW | 001 |
| 8:6 | StatLED2_mode[2:0] | Mode Selection for State LED2.<br>000: Link/Act (Default)<br>001: 100Spd<br>010: Duplex/Col<br>011: Link/Act/100Spd<br>100: Duplex<br>101: Act<br>110: Link<br>111: Col | RW | 010 |
| 12:9 | EnLED[3:0] | State LED 0,1,2 and Diagnostic LED Enable/Disable Control.<br>EnLED[3:0] controls enabling/disabling of DiagLED, StatLED2, StatLED1, StatLED0.<br>0: Disable<br>1: Enable<br>If an LED is disabled, the corresponding serial clock will be masked. | RW | 1111 |
| 14:13 | Reserved | | | |
| 15 | EnSerialMode | Serial/Parallel LED Display Mode Configuration.<br>Two LED output display modes are supported; parallel mode and serial mode.<br>0: Parallel LED mode<br>1: Serial LED mode | RW | 0 |

# 10.3. System Status Register

## 10.3.1. 0x0100H: Board Trapping Status Register

**Table 41. 0x0100H: Board Trapping Status Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | EEPROM_detect_ status | EEPROM Existence Status.<br>0: Exists<br>1: Does not Exist | R | - |
| 1 | EnGDSRev | Enable Gigabit Port GMII/TBI TXD[7:0] Sequence Reverse. When set, reverses the sequence of GMII/TBI TXD '[7:0]' to '[0:7]'.<br>*Note: RXD[7:0] keeps the original sequence.*<br>0: Disable (Default)<br>1: Enable (Reverses the sequence) | RW | HW pin. EnGDSRev |
| 3:2 | FrcTBIMode[1:0] | Force Enable Gigabit port at TBI Mode Interface of Port G0 or G1.<br>Bit FrcTBImode[0], control Gigabit port 0<br>Bit FrcTBImode[1], control Gigabit port 1<br>0: Force enable GMII/MII Mode Interface (Default)<br>1: Force enable TBI Mode Interface | RW | HW pin. FrcTBIMode [1:0] |
| 15:4 | Reserved | | | |

## 10.3.2. 0x0101H: Loop Detect Status Register (32-Bit Register)

**Table 42. 0x0101H: Loop Detect Status Register (32-Bit Register)**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 25:0 | LoopDetPort[25:0] | Network Loop event Detect Port Status.<br>If the loop detect function is enabled, the corresponding bit of LoopDetPort[25:0] will be set whenever a loop event is detected on the corresponding switch port. The set bit is cleared only when the loop event has disappeared on that port.<br><br>When the loop detect function is enabled, the switch will periodically transmit one loop detect diagnostic frame. The normal interval time is approx. five minutes. When a loop event is detected the interval time will be changed to fast mode. In fast mode the interval time is about 1 second in order to accelerate detection and diagnostic. The loop event will be reported in this Loop Detect Status Register.<br>0: No Loop detected on this port<br>1: Loop detected on this port | R | 0 |
| 31:26 | Reserved | | | |

## 10.3.3. 0x0102H: System Fault Indication Register

**Table 43. 0x0102H: System Fault Indication Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | BTest | A system test bit. | R | 000 |
| 1 | TrunkFault | Trunk Fault event flag.<br>The flag indicates that there is a trunk port member link down. The trunk will still continue to operate due to the trunk auto fault recovery algorithm.<br>0: No trunk fault detected<br>1: Trunk fault detected | R | 0 |
| 2 | LoopFault | Network Loop Fault Indication.<br>When the Loop Fault indication is set, a loop detected port will be reported on the Loop Detect Port Register.<br>0: Network Loop not detected<br>1: Network Loop detected | R | 0 |
| 4:3 | GigaPHY_ NotExist[1:0] | Gigabit PHY existence report for Gigabit Port G1, G0.<br>0: Exists<br>1: Does not exist | R | 0 |
| 12:5 | FaultTkGroup[7:0] | The Fault Trunk Group Indication.<br>Indicates a Link Fault in the trunk group.<br>A physical link failure of an enabled trunk group will cause the corresponding bit to be set in the FaultTkGroup[7:0]. This is a real time fault status report.<br>Even though the Trunk Group's fault occurred and the fault bit is set, the corresponding trunk can still work properly as fault recovery will be auto applied.<br><br>FaultTkGroup[0] indicator for Trunk 0: (port 0, 1)<br>FaultTkGroup[1] indicator for Trunk 1: (port 2, 3)<br>FaultTkGroup[2] indicator for Trunk 2: (port 4, 5, 6, 7)<br>FaultTkGroup[3] indicator for Trunk 3: (port 8, 9, 10, 11)<br>FaultTkGroup[4] indicator for Trunk 4: (port 12, 13, 14, 15)<br>FaultTkGroup[5] indicator for Trunk 5: (port 16, 17, 18, 19)<br>FaultTkGroup[6] indicator for Trunk 6: (port 20, 21, 22, 23)<br>FaultTkGroup[7] indicator for Trunk 7: (port G0, G1)<br>0: Trunk OK<br>1: Trunk Fault detected | R | 00000000 |
| 15:10 | Reserved | | | |

# 10.4. Management Configuration Register

## 10.4.1. 0x0200H: Realtek Protocol Control Register

**Table 44. 0x0200H: Realtek Protocol Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | DisRRCP | Disable Realtek Remote Control Protocol (RRCP).<br>0: Enable RRCP (Default)<br>1: Disable RRCP | RW | HW pin: DisRRCP |
| 1 | DisREcho | Disable Realtek Remote Echo Protocol.<br>0: Enable REcho protocol (Default)<br>1: Disable REcho protocol | RW | HW pin. DisREcho |
| 2 | EnLoopDet | Enable Loop Detect Function.<br>When enabled, the loop detect status will be reported in register 0x0101 (Loop Detect Status Register).<br>0: Disable<br>1: Enable | RW | HW pin. EnLoopDet |
| 15:3 | Reserved | | | |

## 10.4.2. 0x0201H: RRCP Security Mask Configuration Register 0

**Table 45. 0x0201H: RRCP Security Mask Configuration Register 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | RRCP_SMask[15:0] | RRCP Management Security Mask Configuration.<br>Configuration for ports 0 to 15.<br>Specifies which port's incoming RRCP access commands will be responded to.<br>0: RRCP Access enabled port<br>1: RRCP Access disabled port<br>*Note: Ports 0~23 RRCP security mask will be set if the hardware strap pin EnHomeVlan is pulled high during power on reset. This can be over written by EEPROM or registers access.* | RW | 0 |

## 10.4.3. 0x0202H: RRCP Security Mask Configuration Register 1

**Table 46. 0x0202H: RRCP Security Mask Configuration Register 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 9:0 | RRCP_SMask[25:16] | RRCP Management Security Mask Configuration.<br>Configuration for ports 16 to 25.0.<br>Specifies which port's incoming RRCP access commands will be responded to.<br>0: RRCP Access enabled port<br>1: RRCP Access disabled port<br>*Note: Ports 0~23 RRCP security mask will be set if the hardware strap pin EnHomeVlan is pulled high during power on reset. This can be over written by EEPROM or register access.* | RW | 0 |

### 10.4.4. 0x0203H: Switch MAC ID Register 0

**Table 47. 0x0203H: Switch MAC ID Register 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | MACID[15:0] | Switch Physical MAC Address bit[15:0].<br>Bitmap example. For a given 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52. | R<br>(W: EEPROM) | 0 |

### 10.4.5. 0x0204H: Switch MAC ID Register 1

**Table 48. 0x0204H: Switch MAC ID Register 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | MACID[31:16] | Switch Physical MAC Address bit[31:16]<br>Bitmap example. For a given 48-bit MAC address '52-54-4C-01-02-03', then MACID[31:16]=01-4C. | R<br>(W: EEPROM) | 0 |

### 10.4.6. 0x0205H: Switch MAC ID Register 2

**Table 49. 0x0205H: Switch MAC ID Register 2**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | MACID[47:32] | Switch Physical MAC Address bit[47:32].<br>Bitmap example. For a given 48-bit MAC address '52-54-4C-01-02-03', then MACID[47:32]=03-02. | R<br>(W: EEPROM) | 0 |

### 10.4.7. 0x0206H: Chip Model ID

**Table 50. 0x0206H: Chip Model ID**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:0 | ChipID[7:0] | Chip ID.<br>Identifies the chip version for programmer version control. | R<br>(W: EEPROM) | 0 |
| 15:8 | Reserved | | | |

## 10.5. 0x0207H: System Vender ID Register 0

**Table 51. 0x0207H: System Vender ID Register 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | VenderID[15:0] | System Vender Identity Stream [15:0].<br>Used for the system vender to fill a code or name stream for switch device model number or vender name identification. | R<br>(W: EEPROM) | 0 |

## 10.6. 0x0208H: System Vender ID Register 1

**Table 52. 0x0208H: System Vender ID Register 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | VenderID[31:16] | System Vender Identity Stream [31:16].<br>Used for system vender to fill a code or name stream for switch device model number or vender name identification. | R<br>(W: EEPROM) | 0 |

## 10.7. 0x0209H: RRCP Authentication Key Configuration Register

**Table 53. 0x0209H: RRCP Authentication Key Configuration Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | RRCP_KEY[15:0] | RRCP Access Authentication Key Configuration.<br>After power on reset, the RRCP Authentication Key is set to the default value '0x2379'. It can be updated via the CPU interface or by an RRCP control frame with a correct current authentication key value in the frame.<br><br>The Authentication Key checking rule for RRCP frames is defined as follows:<br>1. For the Hello command frame:<br>-- Broadcast Hello frame: Do not check Auth. Key.<br>-- Unicast Hello frame: Auth. Key = RRCP_KEY[15:0]<br>*Note: When the RRCP_KEY[15:0] is updated by the user, only unicast Hello frames are valid.*<br>2. For a Get/Set command frame:<br>Always uses the current key value defined by RRCP_KEY[15:0] | RW | 0x2379 |

## 10.8. 0x020AH: Port 0, 1 Bandwidth Control Register

**Table 54. 0x020AH: Port 0, 1 Bandwidth Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 3:0 | P0RXRate[3:0] | Port 0 RX Bandwidth Control.<br>Configures the maximum output bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum RX rate of the port.<br>000: Disables rate control<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:4 | P0TXRate[3:0] | Port 0 TX Bandwidth Control.<br>Configures the maximum input bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum TX rate of the port.<br>000: Disables rate control<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |
| 11:8 | P1RXRate[3:0] | Port 1 RX Bandwidth Control<br>Configures the maximum output bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum RX rate of the port.<br>000: Disables rate control<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |
| 15:12 | P1TXRate[3:0] | Port 1 TX Bandwidth Control<br>Configures the maximum input bandwidth of the port.<br>Bit 3 is a reserved bit.<br>Bit[2:0] controls the maximum TX rate of the port.<br>000: Disables rate control<br>001: 128Kbps<br>010: 256Kbps<br>011: 512Kbps<br>100: 1Mbps<br>101: 2Mbps<br>110: 4Mbps<br>111: 8Mbps | RW | 0000 |

## 10.8.1. 0x020BH ~ 0x0216H: Port 2 ~ 25 Bandwidth Control Register

Refer to Table 54, page 73, for Configuration description of n: 1 ~ 12.

**Table 55. 0x020BH ~ 0x0216H: Port 2 ~ 25 Bandwidth Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 3:0 | P2nRXRate[3:0] | Port 2n RX Bandwidth Control. | RW | 0000 |
| 7:4 | P2nTXRate[3:0] | Port 2n TX Bandwidth Control. | RW | 0000 |
| 11:8 | P2n+1RXRate[3:0] | Port 2n+1 RX Bandwidth Control. | RW | 0000 |
| 15:12 | P2n+1TXRate[3:0] | Port 2n+1 TX Bandwidth Control. | RW | 0000 |

# 10.9. Address Lookup Table (ALT) Control Register

## 10.9.1. 0x0300H: ALT Configuration Register

**Table 56. 0x0300H: ALT Configuration Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | DisMacAging | Global Disable Mac Table Aging Function.<br>0: Enable Aging function (Default)<br>1: Disable Aging function | RW | 0 |
| 1 | EnFastAgeTime | Enable Fast Aging Time Mode.<br>0: Disable Fast Aging time; 300 seconds (Default)<br>1: Enable Fast Aging time; 12 seconds | RW | HW pin. EnFastAge |
| 2 | EnCtrlFFilter | Global Enable 802.1D Specified Reserved Control Frame Filtering.<br>When network control packets are received with a destination MAC address as the group MAC address: (01-80-C2-00-00-03 ~ 01-80-C2-00-00-0F), the switch will drop the packets if the bit EnCtrlFilter=1. Otherwise (EnCtrlFilter=0) they will be flooded.<br>1: Enable Filtering (Default)<br>0: Disable Filtering | RW | HW pin. EnCtrlFFilter |
| 3 | EnDropUknDA | Global Enable Drop Unknown Destination MAC address (DA) packet.<br>If drop unknown DA is disabled, packets with an unknown DA will be flooded.<br>If drop unknown DA is enabled, packets with an unknown DA will be dropped.<br>0: Disable Drop Unknown DA<br>1: Enable Drop Unknown DA | RW | 0 |
| 15:4 | Reserved | | | |

## 10.9.2. 0x0301H: Address Learning Control Register 0

**Table 57. 0x0301H: Address Learning Control Register 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | DisMacLearn[15:0] | Per-Port Disable Mac Address Learning Function (Ports 0~15). DisMacLearn[15:0] control port[15:0].<br>The Layer 2 MAC address learning function can be per-port disabled for security management purposes.<br>Generally this register is used with the ALT Configuration Register (0x0300) bits 'DisMacAging' & 'EnDropUknDA'.<br>0: Enable learning (Default)<br>1: Disable learning | RW | 0 |

## 10.9.3. 0x0302H: Address Learning Control Register 1

**Table 58. 0x0302H: Address Learning Control Register 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 9:0 | DisMacLearn[25:16] | Per-Port Disable Mac Address Learning Function (port 16~25).<br>DisMacLearn[25:16] control port[25:16].<br>The Layer 2 MAC address learning function can be per-port disabled for security management purposes.<br>Generally this register is used with the ALT Configuration Register (0x0300H) bits 'DisMacAging' & 'EnDropUknDA'.<br>0: Enable learning (Default)<br>1: Disable learning | RW | 0 |
| 15:10 | Reserved | | | |

## 10.9.4. 0x0303H: Unknown SA Capture Register 0

**Table 59. 0x0303H: Unknown SA Capture Register 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | UnknownSA[15:0] | Unknown Source MAC Address Capture (Byte 0, 1).<br>Registers 0, 1, and 2 are used to capture unknown Source MAC addresses for MAC table address security management.<br>When a port's MAC address learning function is disabled (locked), then any incoming Source MAC address from this port that has not been learned on the MAC table will be captured into the Unknown SA Management Register 0, 1, 2. Only the first detected unknown SA can be captured until the unknownSAPID register has been read.<br>The unknown Source MAC address will be captured into Register addresses 0x0303 ~ 0x0305. The incoming port ID of the unknown Source MAC address and valid bit is reported in register address 0x0306. | R | 0 |

## 10.9.5. 0x0304H: Unknown SA Capture Register 1

**Table 60. 0x0304H: Unknown SA Capture Register 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | UnknownSA[31:16] | Unknown Source MAC Address Capture (Byte 2, 3). | R | 0 |

## 10.9.6. 0x0305H: Unknown SA Capture Register 2

**Table 61. 0x0305H: Unknown SA Capture Register 2**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | UnknownSA[47:32] | Unknown Source MAC Address Capture (Byte 4, 5) | R | 0 |

## 10.9.7. 0x0306H: Unknown SA Status Register

**Table 62. 0x0306H: Unknown SA Status Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 4:0 | UnknownSAPID[4:0] | Unknown Source MAC Address Incoming Port ID.<br>When an unknown SA is detected, UnknownSAPID[4:0] reports the Port ID incoming port. | R | 0000 |
| 5 | UnknownSAstatus | Unknown SA Capture Status.<br>When an unknown SA is detected and captured, this bit will be set to '1'.<br>The read sequence is Reg 0x0305 → Reg 0x0304 → Reg 0x0303.<br><br>0: Idle (previous old status)<br>1: New unknown SA was detected and captured in Unknown SA Management Registers. This bit will be auto cleared after being read. | RC | 0 |
| 15:6 | Reserved | | | |

## 10.9.8. 0x0307H: Port Trunking Configuration Register

**Table 63. 0x0307H: Port Trunking Configuration Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:0 | EnTrunk[7:0] | Trunk Group Enable/Disable Control<br>Enables trunk groups.<br>EnTrunk[0] control for Trunk 0: (port 0, 1).<br>EnTrunk[1] control for Trunk 1: (port 2, 3).<br>EnTrunk[2] control for Trunk 2: (port 4, 5, 6, 7).<br>EnTrunk[3] control for Trunk 3: (port 8, 9, 10, 11).<br>EnTrunk[4] control for Trunk 4: (port 12, 13, 14, 15).<br>EnTrunk[5] control for Trunk 5: (port 16, 17, 18, 19).<br>EnTrunk[6] control for Trunk 6: (port 20, 21, 22, 23).<br>EnTrunk[7] control for Trunk 7: (port G0, G1).<br>0: Disable Trunking<br>1: Enable Trunking | RW | 0x00 |
| 8 | PNTest | Test bit.<br>Keep as 0.<br>The bit value of EEPROM should be set to 0. | RW | 0 |
| 15:8 | Reserved | | | |

## 10.9.9. 0x0308H: IGMP Snooping Control Register

**Table 64. 0x0308H: IGMP Snooping Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | EnIGMPsnooping | Enable IGMP Snooping.<br>The switch controller features an ASIC-based auto IGMP v1 & v2 snooping function. No software support is required. When enabled, the switch can automatically snoop IGMP packets and build up an IP multicast address table.<br>The discovered IP multicast Router port will be indicated in the 'IP Multicast Router Port Discovery Register'.<br>0: Disable IGMP snooping<br>1: Enable IGMP snooping | RW | HW pin. EnIGMP snooping |
| 15:1 | Reserved | | | |

## 10.9.10. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)

**Table 65. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 25:0 | IPMRouterDISC[25:0] | IP Multicast Router Ports Discovery Result.<br>This is a bit map that indicates which port is an IP Multicast Router port. IPMRouterDISC[25:0] maps to port 25 ~ 0<br>0: Normal port<br>1: IP multicast Router port | R | 0 |
| 31:26 | Reserved | | | |

## 10.9.11. 0x030BH: VLAN Control Register

**Table 66. 0x030BH: VLAN Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | EnVlan | Enable VLAN Function.<br>When the VLAN function is enabled, the power on default VLAN topology is 24 Home VLAN for non-EEPROM environments. The VLAN topology can be configured by Port VLAN Configuration Registers.<br>0: Disable VLAN<br>1: Enable VLAN | RW | HW pin. EnHomeVLAN |
| 1 | EnUCleaky | Unicast Packet Inter-VLAN Leaky Control<br>Enables inter-VLAN communication for unicast forwarding packets.<br>Normally, inter-VLAN packet switching is not valid. The RTL8326 supports a control bit to enable inter-VLAN communication in the switch without an external router.<br>0: Disable<br>1: Enable | RW | 0 |
| 2 | EnARPleaky | ARP broadcast Packet Inter-VLAN Leaky Control.<br>Enables inter-VLAN communication for ARP broadcast packet forwarding.<br>0: Disable<br>1: Enable | RW | 0 |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 3 | EnIPMleaky | IP Multicast Packet Inter-VLAN Leaky Control.<br>Enables inter-VLAN communication for ARP broadcast packet forwarding.<br>0: Disable<br>1: Enable | RW | 0 |
| 4 | En8021Qaware | Enable 802.1Q VLAN tag aware.<br>If 802.1Q VLAN aware, the switch supports the ability to identify the VLAN ID from the VLAN tag. Reset to force the switch to ignore the VLAN tag header and classify the VLAN only by the PVID.<br>0: Disable 802.1Q VLAN aware (Default)<br>1: Enable 802.1Q VLAN aware | RW | 0 |
| 5 | EnIR_TagAdmit | Ingress Rule for Acceptable frame types control.<br>If this parameter is set to 'Admit only VLAN-Tagged Frames', any frames received on that port that carry no VID (i.e., Untagged Frames or Priority-Tagged Frames) are discarded. If this parameter is set to 'Admit all Frames', all incoming Priority-Tagged and Untagged Frames are associated with a VLAN by the ingress rule on the receiving port.<br>0: Admit all Frames (Default)<br>1: Admit only VLAN-Tagged Frames | RW | 0 |
| 6 | EnIR_MembSet | Ingress Rule for Ingress Filtering control.<br>If the Enable Ingress Filtering parameter 'EnIR_MembSet' is set, then all frames received on a port whose VLAN classification does not include that port in its member set shall be discarded.<br>0: Disable ingress member set Filtering (Default)<br>1: Enable ingress member set filtering | RW | 0 |
| 15:7 | Reserved | | | |

## 10.9.12. 0x030C~0x0318H: Port VLAN ID Assignment Index Register 0~12

For Port(2n), and Port(2n+1) the register is defined as follows: where n=0, 1, 2, … 11, 12 (Addr: 0x030CH + n).

**Table 67. 0x030C~0x0318H: Port VLAN ID Assignment Index Register 0~12**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:0 | P(2n)_VIDIndex[7:0] | Port(2n) VID assignment Index.<br>Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID<br>Bit[7:5]: Reserved, currently not used | RW | n |
| 15:8 | P(2n+1)_VIDIndex[7:0] | Port(2n+1) VID assignment Index.<br>Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID<br>Bit[7:5]: Reserved, current not used | RW | 2n+1 |

### 10.9.13. 0x0319~0x031CH: VLAN Output Port Priority-Tagging Control Register 0, 1, 2, 3

For Port(8n), Port(8n+1), …. ~ Port(8n+7) the register is defined as follows: n=port0~port25.

**Table 68. 0x0319~0x031CH: VLAN Output Port Priority-Tagging Control Register 0, 1, 2, 3**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 1:0 | P(8n)_PriTagCtl[1:0] | Port(8n) VLAN Output priority Tag/Untag Control.<br>00: Remove the VLAN tag from a tagged frame<br>01: Insert priority tag into an untagged high-priority frame. (set priority field: 7, VID field: 0 for high priority frame)<br>10: Insert priority tag into all untagged frames.<br>(set priority field: 7, VID field: 0 for high priority frame; set priority field: 0, VID field: 0 for low priority frame)<br>11: Don't touch (Don't modify the packet) (Default) | RW | 11 |
| 3:2 | P(8n+1)_PriTagCtl[1:0] | Port(8n+1) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 5:4 | P(8n+2)_PriTagCtl[1:0] | Port(8n+2) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 7:6 | P(8n+3)_PriTagCtl[1:0] | Port(8n+3) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 9:8 | P(8n+4)_PriTagCtl[1:0] | Port(8n+4) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 11:10 | P(8n+5)_PriTagCtl[1:0] | Port(8n+5) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 13:12 | P(8n+6)_PriTagCtl[1:0] | Port(8n+6) VLAN Output priority Tag/Untag Control. | RW | 11 |
| 15:14 | P(8n+7)_PriTagCtl[1:0] | Port(8n+7) VLAN Output priority Tag/Untag Control. | RW | 11 |

## 10.10. 0x031D~0x037CH: VLAN Table Configuration Registers

Each VLAN configuration entry requires three 16-bit registers. There are 32 VLAN configuration entries in the VLAN table. The VLAN configuration entry is combined with three registers: VLAN_Entry_Configuration_0, 1, 2. For VLAN m, its format is defined as follows: m=0, 1, 2, …. 31.

### 10.10.1. Register VLAN(m)_Entry_Configuration_0 (Addr: (0x031DH+3m))

**Table 69. Register VLAN(m)_Entry_Configuration_0 (Addr: (0x031DH+3m))**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | VLAN(m)_PM[15:0] | VLAN (entry m) Port Member, 26-bit map (bit 0~15).<br>Bit value 0: Port is not a member of the VLAN<br>Bit value 1: Port is a member of the VLAN | RW | Default set to 24+2 Home VLAN topology |

### 10.10.2. Register VLAN(m)_Entry_Configuration_1 (Addr: (0x031DH+3m+1))

**Table 70. Register VLAN(m)_Entry_Configuration_1 (Addr: (0x031DH+3m+1))**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 9:0 | VLAN(m)_PM[25:16] | VLAN(m) Port Member 26-bit map (bit 16~25).<br>Bit value 0: Port is not a member of the VLAN<br>Bit value 1: Port is a member of the VLAN | RW | Default set as 24+2 Home VLAN topology |
| 15:10 | Reserved | | | |

### 10.10.3. Register VLAN(m)_Entry_Configuration_2 (Addr: (0x031DH+3m+2))

**Table 71. Register VLAN(m)_Entry_Configuration_2 (Addr: (0x031DH+3m+2))**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 11:0 | VLAN(m)_VID[11:0] | VLAN(m) VID[11:0] bit 11~0.<br>Each VLAN must be assigned a 12-bit VID. | RW | 0 |
| 15:12 | Reserved | | | |

## 10.11. QoS Configuration Register

### 10.11.1. 0x0400H: QoS Control Register

**Table 72. 0x0400H: QoS Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | EnDSPri | Enable TCP/IP TOS/DS (DiffServ) based Priority QoS.<br>0: Disabled (Default)<br>1: Enabled<br>When enabled, the priority definition is defined as follows:<br>High Priority: If TOS/DS[0:5]:<br>(EF) '101110';<br>(AF) '001010', '010010',<br>'011010', '100010';<br>(Network Control) "11x000'<br>Low Priority: TOS/DS = Other codepoint values<br>*Note 1: The DS[0:5] bit location is equal to the mapping of TOS[0:5] ={precedence[2:0], Delay, Throughput, Reliability}.*<br>*Note 2: DS=Differentiated Services, EF= Expected Forwarding, AF= Assured Forwarding.* | RW | HW pin.<br>EnDSPri |
| 1 | En8021pPri | Enable 802.1p VLAN Tag Based Priority QoS Function.<br>0: Disable (Default)<br>1: Enable | RW | HW pin.<br>En8021pPri |
| 2 | EnFCAutoOff | Enable Flow Control Ability Auto Turn Off for QoS.<br>Enabled: Enables auto turn off of a port's queue flow control ability for 1~2 seconds whenever the port receives a high priority frame. The flow control ability of this port is re-enabled when no high priority frames are received at this port during a 1~2 second period.<br>When EnFCAutoOff is disabled, the flow control ability of this port for any packet will be enabled as it was set.<br>0: Disabled (Default)<br>1: Enabled | RW | HW pin.<br>EnFCAutoOff |
| 4:3 | QWeight[1:0] | Weighted round robin ratio setting of priority queue.<br>The frame service rate of High-pri queue: Low-pri queue is.<br>00: 4:1<br>01: 8:1<br>10: 16:1 (Default)<br>11: High priority queue first always | RW | HW pin.<br>QWeight[1:0] |
| 15:5 | Reserved | | | |

### 10.11.2. 0x0401: Port Priority Configuration Registers 0

**Table 73. 0x0401: Port Priority Configuration Registers 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | PortPriCfg[15:0] | Port based Priority setting (Port0 ~ Port15).<br>Sets the priority QoS based on the physical port.<br>If a port is set as a high priority port, all packets received from that port will be treated as high priority packets.<br>Bit value 1: Sets that port as a high priority port<br>Bit value 0: Sets that port as a low priority port<br>*Note: Ports 0~15 map to bits 0~ 15.* | RW | Bit[15:4]=0;<br>Bit[3:0].depend on HW pin. PortPriSet[1:0] |

### 10.11.3. 0x0402: Port Priority Configuration Registers 1

**Table 74. 0x0402: Port Priority Configuration Registers 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 9:0 | PortPriCfg[25:16] | Port based Priority setting (Port16 ~ Port25).<br>Sets the priority QoS based on the physical port.<br>If a port is set as a high priority port, all packets received from that port will be treated as high priority packets.<br>Bit value 1: Sets that port as a high priority port<br>Bit value 0: Sets that port as a low priority port<br>*Note: Ports 16~25 map to bits 0~ 9.* | RW | 0 |
| 15:10 | Reserved | | | |

## 10.12. PHY Access Control Register

### 10.12.1. 0x0500H: PHY Access Control Register

**Table 75. 0x0500H: PHY Access Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 4:0 | REG_addr | PHY Register address setting for the PHY Access command. | RW | 0 |
| 9:5 | PHY_ID[4:0] | PHY ID (PHY address) setting for the PHY Access command.<br>RTL8326 connected PHY ID is fixed as:<br>Fast Ethernet Port0 ~ 23. PHY ID: 8, 9, …, 30, 31.<br>Gigabit Port G1 and G2. PHY ID: 2 and 3. | RW | 0 |
| 13:10 | Reserved | | | 0 |
| 14 | PHY_RW | PHY Access Command.<br>0: PHY Access Read command<br>1: PHY Access Write command | RW | 0 |
| 15 | PHYCmdExeSta | PHY Access Command Execution Status.<br>0: Idle<br>1: Busy | R | 0 |

### 10.12.2. 0x0501H: PHY Access Write Data Register

**Table 76. 0x0501H: PHY Access Write Data Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | PHY_WD[15:0] | PHY Access Write Out Data (16 bits). | RW | 0 |

### 10.12.3. 0x0502H: PHY Access Read Data Register

**Table 77. 0x0502H: PHY Access Read Data Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | PHY_RD[15:0] | PHY Access Read In Data (16 bits). | R | 0 |

## 10.13. Port Control Register

### 10.13.1. 0x0607H: Global Port Control Register

**Table 78. 0x0607H: Global Port Control Register**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 0 | DisFDFC | Disable Full Duplex Flow Control (802.3x PAUSE ability). This control bit will be applied to the switch only when a software reset is sent to the switch.<br>This function can also be directly controlled by PHY register access through the PHY Access Control Register<br>0: Enable 802.3x Pause ability<br>1: Disable 802.3x Pause ability | RW | HW pin: DisFDFC |
| 1 | DisBKP | Globally Disable Half Duplex Back Pressure Flow Control Ability.<br>Set to globally disable the back pressure flow control ability of all ports.<br>0: Enable back pressure flow control ability<br>1: Disable back pressure flow control ability | RW | HW pin. DisBKP |
| 2 | DisBCSFC | Disable Broadcast Packet Strict Flood Control.<br>Set to disable broadcast packet (DA: 'FFFFFFFFFFFF') strict flood mode and configure to loose flood mode. The control function is used under 802.3x flow control mode.<br>Strict flood mode will drop broadcast packets if any one destination port member is congested. Loose flood mode allows broadcast packets to be flooded to all non-congested ports.<br>0: Disable Broadcast Packet Strict Flood (Loose flood mode)<br>1: Enable Broadcast Packet Strict Flood (Strict flood mode) | RW | HW pin. DisBCFC |
| 3 | DisIPMSFC | Disable IP Multicast Packet Strict Flood Control.<br>Set to disable IP Multicast packet (DA: '01-00-5E-XX-XX-XX') strict flood mode and configure to loose flood mode. The control function is used under 802.3x flow control mode.<br>Strict flood mode will drop IP Multicast packets if any one destination port member is congested. Loose flood mode allows IP multicast packets to be flooded to all non-congested ports.<br>0: Disable IP Multicast Packet Strict Flood (Loose flood mode)<br>1: Enable IP Multicast Packet Strict Flood (Strict flood mode) | RW | HW pin. DisIPMFC |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 4 | DisBRDCTRL | Disable Broadcast Storm Filtering Control.<br>Set to disable the broadcast storm filtering control function.<br>1: Disable Broadcast storm filtering control (Default)<br>0: Enable Broadcast storm filtering control | RW | HW pin: DisBRDCTRL |
| 15:5 | Reserved | | | |

## 10.13.2. 0x0608H: Port Disable Control Register 0

**Table 79. 0x0608H: Port Disable Control Register 0**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:0 | PortDisable[15:0] | Port Enable/Disable Control for port 0 ~ 15.<br>Bit value 0: Port enable<br>Bit value 1: Port disable<br>When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets.<br>*Note: Ports 0~15 map to bits 0~ 15.* | RW | 0 |

## 10.13.3. 0x0609H: Port Disable Control Register 1

**Table 80. 0x0609H: Port Disable Control Register 1**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 9:0 | PortDisable[25:16] | Port Enable/Disable Control for port 16 ~ 25.<br>Bit value 0: Port enable<br>Bit value 1: Port disable<br>When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets.<br>*Note: Ports 16~25 map to bits 0~ 9.* | RW | 0 |
| 15:10 | Reserved | | | |

## 10.13.4. 0x060AH~0x0616. Port Property Configuration Register 0 ~ 12

For Port(2n) and Port(2n+1) the Port Property is defined as follows: n = 0, 1, 2,. …, 12 (Addr: 0x060AH +n); where n=0~11 for Fast Ethernet ports, n=12 for Gigabit ports).

**Table 81. 0x060AH~0x0616. Port Property Configuration Register 0 ~ 12**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:0 | P(2n)_Property[7:0] | Port(2n) Port Property configuration.<br>Bit [4:0]: Media Capability[4:0]= (1000F, 100F, 100H, 10F, 10H).<br>Bit [5]: Pause ability (1: Enable).<br>Bit [6]: AsyPause ability (Asynchronous Pause) (1. enable)<br>Bit [7]: Enable Auto Negotiation (1: Enable).<br>*Note: A software reset is required to complete the port properties update.* | RW | 100M. 0xAF<br>1000M: 0xBF |
| 15:8 | P(2n+1)_Property[7:0] | Port(2n+1) Port property configuration.<br>Bit [4:0]: Media Capability[4:0]= {1000F, 100F, 100H, 10F, 10H}.<br>Bit [5]: Pause ability (1: Enable).<br>Bit [6]: AsyPause ability ( Asynchronous Pause) (1: Enable).<br>Bit [7]: Enable Auto Negotiation (1: Enable).<br>*Note: A software reset is required to complete the port properties update.* | RW | 100M. 0xAF<br>1000M: 0xBF |

*Note: A configuration update of these registers requires a software reset (via write Reg. 0x0000 bit 0 =1) to force the configuration to be written to the PHY register and restart the auto-negotiation process.*

## 10.13.5. 0x0619H~0x0625. Port Link Status Register 0 ~ 12

For Port(2n) and Port(2n+1) the Port Properties are defined as follows: (n: 0,1,2,. …, 12) (Addr: 0x060AH +n).

**Table 82. 0x0619H~0x0625. Port Link Status Register 0 ~ 12**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 7:0 | P(2n)_LinkStatus[7:0] | Port (2n) Port Link Status.<br><br>Bit [1:0]: Link speed[1:0]:<br>00: 10Mbps<br>01: 100Mbps<br>10: 1000Mbps<br>11: NA.<br><br>Bit [2]: Full duplex:<br>0: Half duplex<br>1: Full duplex<br>Bit[3]: Reserved.<br><br>Bit [4]: Link up:<br>0: Link down<br>1: Link up<br><br>Bit [5]: Flow control (back pressure or 802.3x):<br>For ports 0~23 (Fast Ethernet ports). Defined as Pause ability.<br>For ports 24~25 (Gigabit ports). Defined as TX Pause ability.<br>In half duplex mode. Defined as back pressure ability.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [6]: AsyPause ability (Asymmetric Pause):<br>For ports 0~23 (Fast Ethernet ports) Don’t Care.<br>For ports 24~25 (Gigabit ports). Defined as RX Pause ability.<br>In half duplex mode. Don’t Care.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [7]: Enable Auto Negotiation (AN):<br>0: Disable AN<br>1: Enable AN | R | 0 |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 15:8 | P(2n+1)_LinkStatus[7:0] | Port(2n+1) Port Link Status.<br><br>Bit [1:0]: Link speed[1:0]:<br>00: 10Mbps<br>01: 100Mbps<br>10: 1000Mbps<br>11: NA.<br><br>Bit [2]: Full duplex:<br>0: Half duplex<br>1: Full duplex<br><br>Bit[3]: Reserved.<br><br>Bit [4]: Link up:<br>0: Link down<br>1: Link up<br><br>Bit [5]: Flow Control (back pressure or 802.3x):<br>For ports 0~23 (Fast Ethernet ports). Defined as Pause ability.<br>For ports 24~25 (Gigabit ports). Defined as TX Pause ability.<br>In half duplex mode. Defined as back pressure ability.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [6]: AsyPause ability (Asymmetric Pause):<br>For ports 0~23 (Fast Ethernet ports) Don't Care.<br>For ports 24~25 (Gigabit ports). Defined as RX Pause ability.<br>In half duplex mode. Don't Care.<br>0: Flow control disabled<br>1: Flow control enabled<br><br>Bit [7]: Enable Auto Negotiation (AN):<br>0: Disable AN<br>1: Enable AN | R | 0 |

# 11. MIB Counter Register

## 11.1. 0x0700H ~ 0x070CH: Port MIB Counter Object Selection Register 0 ~ 12

For Port(2n), Port(2n+1), the Port MIB Counter Object Selection Register is defined as follows: n = 0, 1, 2, …, 12) (Addr=0x0700H +n)

**Table 83. 0x0700H ~ 0x070CH: Port MIB Counter Object Selection Register 0 ~ 12**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 1:0 | P(2n)CNT1_MIBS [1:0] | Port(2n) Counter_1 MIB Object Selection<br>P(2n)CNT_1_MIBS [1:0]<br>00: MIB object: RX byte count<br>01: MIB object: RX packet count (Default)<br>10: MIB object: CRC error packet count<br>11: MIB object: Collision packet count<br><br>RX byte count. This counter is incremented once for every data byte of a received and forwarded packet (includes both good and bad packets).<br>RX packet count. This counter is incremented once for every received and forwarded packet (includes both good and bad packets). | RW | 01 |
| 3:2 | P(2n)CNT2_MIBS [1:0] | Port(2n) Counter_2 MIB Object Selection<br>P(2n)CNT_2_MIBS [1:0]<br>00: MIB object: TX byte count<br>01: MIB object: TX packet count (Default)<br>10: MIB object: CRC error packet count<br>11: MIB object: Collision packet count<br><br>TX byte count. This counter is incremented once for every data byte of a transmitted packet (includes both good and bad packets).<br>TX packet count. This counter is incremented once for every transmitted packet (includes both good and bad packets). | RW | 01 |

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 5:4 | P(2n)CNT3_MIBS [1:0] | Port(2n) Counter_3 MIB Object Selection<br>P(2n)CNT_3_MIBS [1:0]<br>00: MIB object: Drop byte count<br>01: MIB object: Drop packet count (Default)<br>10: MIB object: CRC error packet count<br>11: MIB object: Collision packet count<br><br>Drop packet count. This counter is incremented once for every drop of a received packet. Packet drop events could be due to undersize, oversize, CRC error, lack of resources, local packet, point-to-point control packet (ex. Pause packet, LACP packet, including RRCP® packets).<br>CRC error packet count. This counter is incremented once for every received packet with a valid length but with a CRC error.<br>Collision packet counter. This counter is incremented once for every collision event detected. | RW | 01 |
| 7:6 | P(2n+1)CNT1_MIBS [1:0] | Port(2n+1) Counter_1 MIB Object Selection. | RW | 01 |
| 9:8 | P(2n+1)CNT2_MIBS [1:0] | Port(2n+1) Counter_2 MIB Object Selection. | RW | 01 |
| 11:10 | P(2n+1)CNT3_MIBS [1:0] | Port(2n+1) Counter_3 MIB Object Selection. | RW | 01 |

## 11.2. 0x070DH ~0726H: Port MIB Counter 1 Register (RX Counter) (32 bits)

The MIB counters are 32-bit counters. After power on reset, the counters are all reset to 0. A read access of the MIB counter will NOT reset the counter to 0. When a MIB counter MIB object is changed, then the counter will be reset to 0 and the count will restart.

The time before the next read of the same counter should not be longer than the counter's timeout. The timeout of the 32-bit MIB counter depends on the object type and the port speed, and is calculated as follows:

Packet counter timeout is calculated based on 64-byte packets and byte counter timeout is calculated based on 1518 byte packets).

**Table 84. MIB Counter Timeout**

| Port Speed | MIB Object Type | MIB Counter Timeout (Sec.) |
|---|---|---|
| **1000Mbps** | Packet count | 2886 |
| | Byte count | 34 |
| **100Mbps** | Packet count | 28862 |
| | Byte count | 348 |
| **10Mbps** | Packet count | 288621 |
| | Byte count | 3481 |

### 11.2.1. For Port(n) MIB Counter 1 Register (32-bit). n=0, 1, 2, … 25 (Addr: 0x070DH+n)

**Table 85. 0x070DH ~0726H: Port MIB Counter 1 Register (RX Counter) (32 bits)**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 31:0 | Port(n)_MIB_CNT_1[31:0] | Port(n) MIB Counter_1[31:0] | R | 0 |

### 11.2.2. 0x0727~0740H: Port MIB Counter 2 Register (TX Counter) (32-bits)

For Port(n) MIB Counter 2 Register (32-bit): n = 0, 1, 2, … 25 (Addr: 0x0727H+n).

**Table 86. 0x0727~0740H: Port MIB Counter 2 Register (TX Counter) (32 bits)**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 31:0 | Port(n)_MIB_CNT_2[31:0] | Port(n) MIB Counter_2[31:0] | R | 0 |

### 11.2.3. 0x0741~075AH: Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

For Port(n) MIB Counter 3 Register (32-bit): n = 0, 1, 2, … 25 (Addr: 0x0741H+n).

**Table 87. 0x0741~075AH: Port MIB Counter 3 Register (Diagnostic Counter) (32 bits)**

| Bits | Name | Description | RW | Default |
|---|---|---|---|---|
| 31:0 | Port(n)_MIB_CNT_3[31:0] | Port(n) MIB Counter_3[31:0] | R | 0 |

# 12. Characteristics

## 12.1. Absolute Maximum Ratings

**WARNING:** Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 88. Electrical Characteristics/Ratings**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Storage Temperature | -55 | +150 | °C |
| Vcc Supply Referenced to GND | -0.5 | +5.0 | V |
| Digital Input Voltage | -0.5 | VDD | V |
| DC Output Voltage | -0.5 | VDD | V |

## 12.2. Operating Range

| Parameter | Min | Max | Units |
|---|---|---|---|
| Ambient Operating Temperature (Ta) | 0 | +70 | °C |
| 3.3V VDD Supply Voltage Range | 3 | 3.6 | V |

## 12.3. DC Characteristics

Supply Voltage VDD: 3.3V ± 5%.

**Table 89. DC Characteristics**

| Parameter | Symbol | Conditions | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| Power Supply Current | Icc | 24FE+2G, wire-speed traffic load<br>24FE, wire-speed traffic load<br>16FE+2G, wire-speed traffic load<br>2G, wire-speed traffic load<br>24FE+2G all idle | | | 480<br>340<br>430<br>330<br>190 | mA |
| Total Power Consumption | PS | 24FE+2G, wire-speed traffic load<br>24FE, wire-speed traffic load<br>16FE+2G, wire-speed traffic load<br>2G, wire-speed traffic load<br>24FE+2G all idle | | | 1584<br>1122<br>1419<br>1089<br>627 | mW |
| TTL Input High Voltage | $V_{ih}$ | | 2.0 | | | V |
| TTL Input Low Voltage | $V_{il}$ | | | | 0.8 | V |
| TTL Input Current | $I_{in}$ | | -10 | | 10 | uA |
| TTL Input Capacitance | $C_{in}$ | | | 2.9 | | pF |
| Output High Voltage | $V_{oh}$ | | 2.6 | | 3.6 | V |
| Output Low voltage | $V_{ol}$ | | 0 | | 0.4 | V |

# 12.4. Digital Timing Characteristics

## 12.4.1. PHY Management (SMI) Timing

**Table 90. PHY Management (SMI) Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| t1 | MDC clock period | - | 1360 | - | ns |
| t2 | MDC high level width | - | 680 | - | ns |
| t3 | MDC low level width | - | 680 | - | ns |
| t4 | MDIO to MDC rising setup time (Write Bits) | | 680 | - | ns |
| t5 | MDIO to MDC rising hold time (Write Bits) | | 680 | - | ns |
| t6 | MDC to MDIO delay (Read Bits) | - | - | 20 | ns |
| t7 | MDC/MDIO actives from RST# deasserted | - | 45 | - | ms |

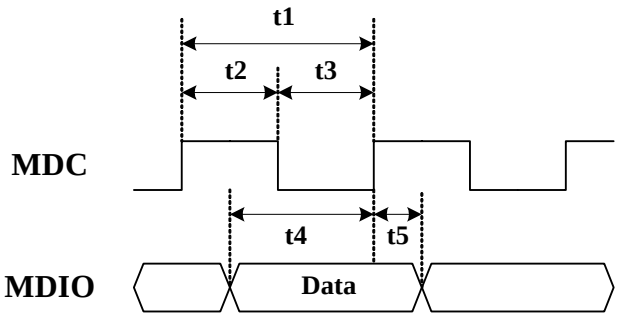



**Figure 18. MDC/MDIO Write Timing**

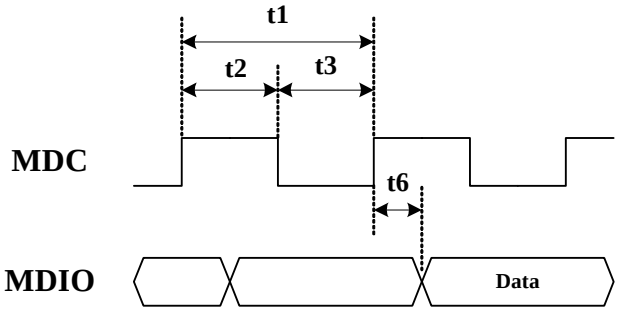



**Figure 19. MDC/MDIO Read Timing**

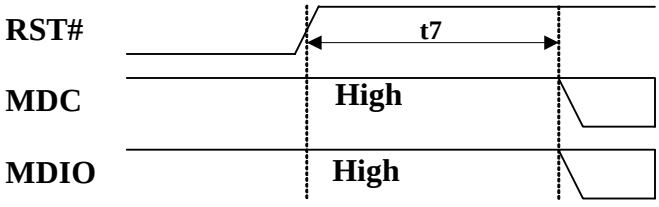



**Figure 20. MDC/MDIO Reset Timing**

## 12.4.2. SMII Transmit Timing

**Table 91. PHY Management (SMI) Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_opd_txd_smii | REFCLK rising edge to TXD (SYNC) delay. | 2 | 4 | 5 | ns |

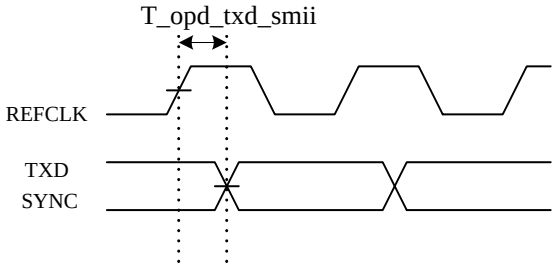



**Figure 21. SMII Transmit Timing**

## 12.4.3. SMII Receive Timing

**Table 92. SMII Receive Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_ipsu_rxd_smii[a] | RXD setup time to REFCLK. | 2 | | | ns |
| T_iphd_rxd_smii[a] | RXD hold time from REFCLK. | 1.5 | | | ns |

a. When SMII RXD delay option set to 2ns (refer to 10.1.3 0x0002H: RX I/O PAD Delay Configuration, page 66).

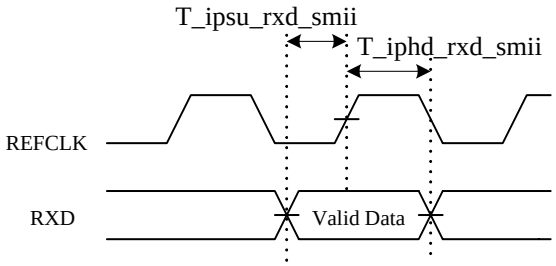



**Figure 22. SMII Receive Timing**

## 12.4.4. GMII Transmit Timing

**Table 93. GMII Transmit Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_opd_txd_gmii | GxTX_CLK rising edge to TXD delay. | 1.2 | 2.5 | 4 | ns |

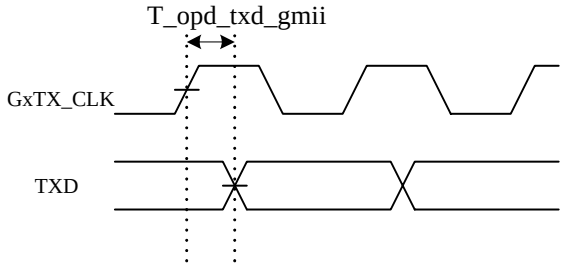



Figure 23. GMII Transmit Timing

## 12.4.5. GMII Receive Timing

**Table 94. GMII Receive Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_su_rxd_gmii | RXD(RX_DV) setup time to GxRX_CLK. | 2.5 | | | ns |
| T_hd_rxd_gmii | RXD(RX_DV) hold time from GxRX_CLK. | 0.5 | | | ns |

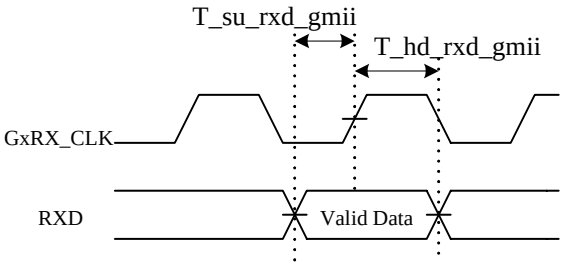



Figure 24. GMII Receive Timing

## 12.4.6. MII Transmit Timing

**Table 95. MII Transmit Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_opd_txd_mii | GxTXC rising edge to TXD delay. | 4 | 7.4 | 10 | ns |

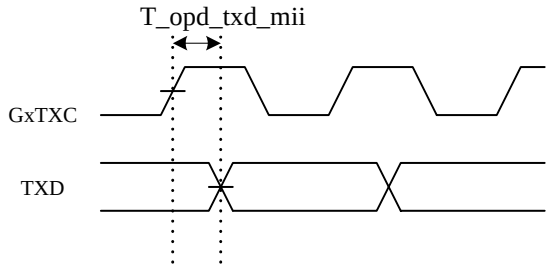



Figure 25. MII Transmit Timing

## 12.4.7. MII Receive Timing

**Table 96. MII Receive Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_su_rxd_mii | RXD(RX_DV) setup time to GxRXC. | 2 | | | ns |
| T_hd_rxd_mii | RXD(RX_DV) hold time from GxRXC. | 1 | | | ns |

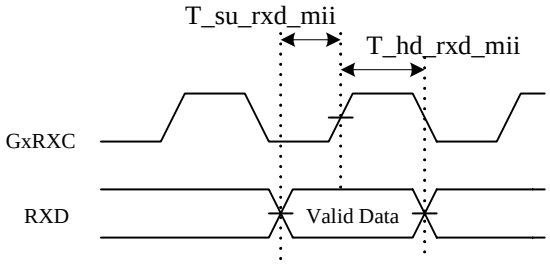



Figure 26. MII Receive Timing

## 12.4.8. TBI Transmit Timing

**Table 97. TBI Transmit Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_opd_txd_TBI | GxTX_CLK rising edge to TXD delay. | 1.5 | 2.5 | 4 | ns |

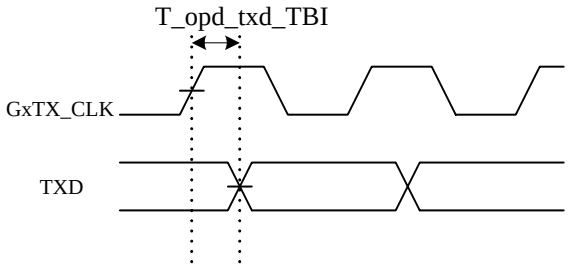



Figure 27. TBI Transmit Timing

## 12.4.9. TBI Receive Timing

**Table 98. TBI Receive Timing**

| Symbol | Description | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| T_su_rxd_TBI | RXD setup time to GxRSCK0/1. | 3 | | | ns |
| T_hd_rxd_TBI | RXD hold time from GxRSCK0/1. | 0.5 | | | ns |

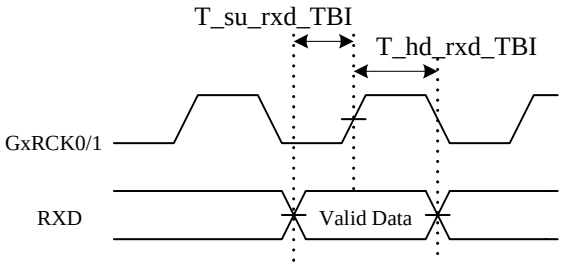



Figure 28. TBI Receive Timing

## 12.5. Thermal Data

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined as below according to JEDEC standard JESD 51-2, 51-6:

1. θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

   θja = (Tj - Ta) / Ph

   Where Tj is the junction temperature
   Ta is the ambient temperature
   Ph is the power dissipation
2. θjc (Thermal resistance from junction to case), represents resistance to heat flow from the chip to the package top case. θjc is important when an external heat sink is attached on the package top.

   θjc = (Tj - Tc) / Ph, where Tj is the junction temperature and Tc is the case temperature.

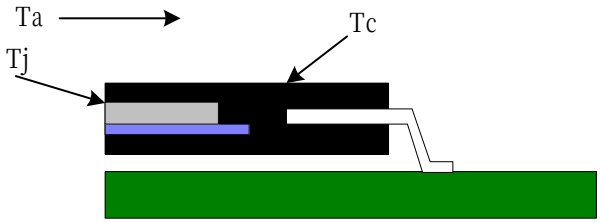



**Figure 29. Cross-section of 208 PQFP**

**Table 99. Thermal Operating Range**

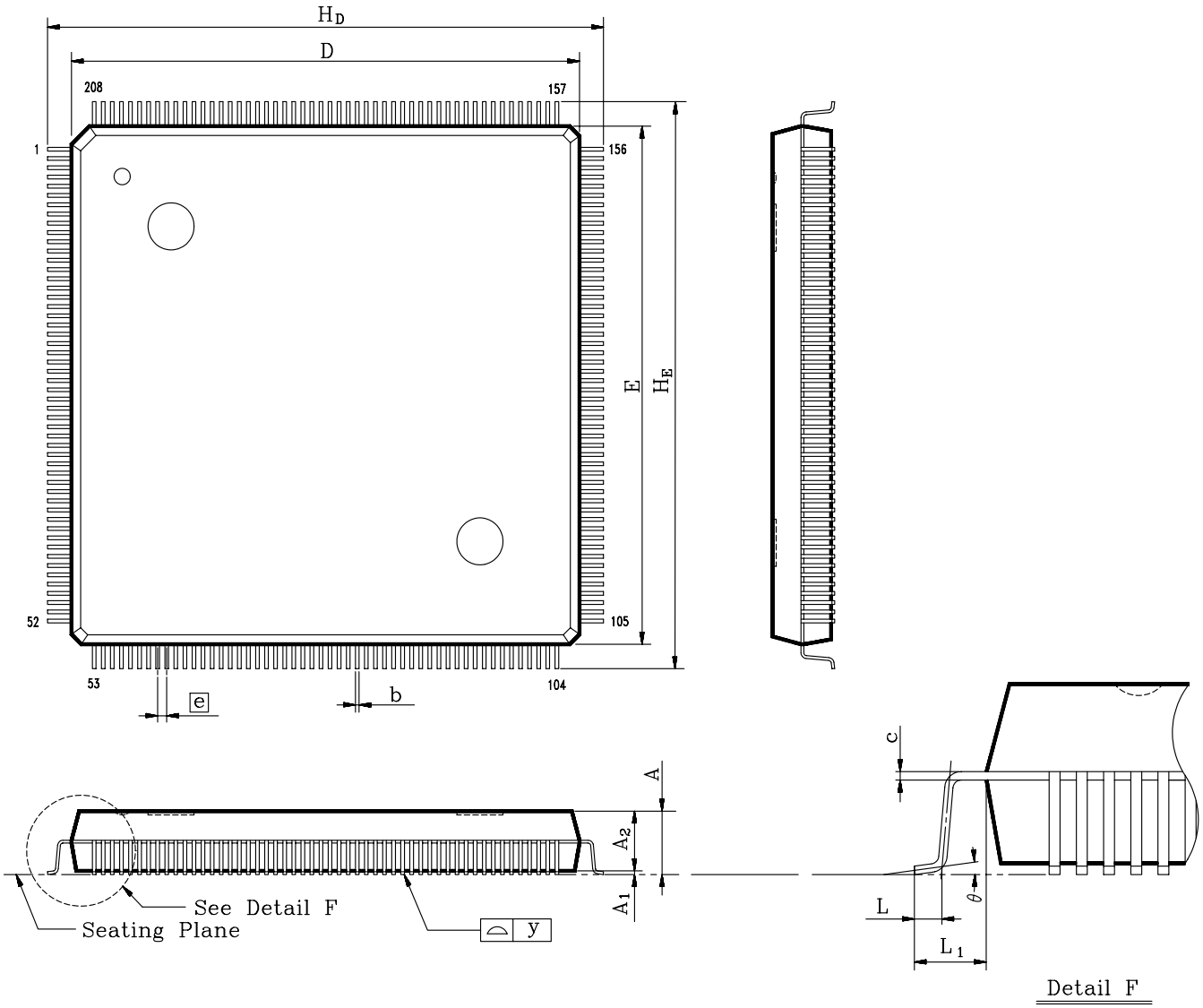
| Parameter | SYM | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| Junction operating temperature | Tj | | 0 | 25 | 125 | °C |
| Ambient operating temperature | Ta | | 0 | 25 | 70 | °C |

**Table 100. Thermal Resistance**

| Parameter | SYM | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| Thermal resistance: junction to ambient | θja | 2 layer PCB, 0 ft/s airflow. | | 33.7 | | °C/W |
| Thermal resistance: junction to case | θjc | 2 layer PCB, 0 ft/s airflow. | | 1.4 | | °C/W |

** PCB conditions (JEDEC JESD51-7). Dimensions: 300 x 140 mm. Thickness: 1.6mm*

# 13. Mechanical Information




See the Mechanical Dimensions notes on the next page.

# 13.1. Mechanical Dimensions Notes

| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.136 | 0.144 | 0.152 | 3.45 | 3.65 | 3.85 |
| $A_1$ | 0.004 | 0.010 | 0.036 | 0.10 | 0.25 | 0.91 |
| $A_2$ | 0.119 | 0.128 | 0.136 | 3.02 | 3.24 | 3.46 |
| b | 0.004 | 0.008 | 0.012 | 0.10 | 0.20 | 0.30 |
| c | 0.002 | 0.006 | 0.010 | 0.04 | 0.15 | 0.26 |
| D | 1.093 | 1.102 | 1.112 | 27.75 | 28.00 | 28.25 |
| E | 1.093 | 1.102 | 1.112 | 27.75 | 28.00 | 28.25 |
| e | 0.012 | 0.020 | 0.031 | 0.30 | 0.50 | 0.80 |
| $H_D$ | 1.169 | 1.205 | 1.240 | 29.70 | 30.60 | 31.50 |
| $H_E$ | 1.169 | 1.205 | 1.240 | 29.70 | 30.60 | 31.50 |
| L | 0.010 | 0.020 | 0.030 | 0.25 | 0.50 | 0.75 |
| $L_1$ | 0.041 | 0.051 | 0.061 | 1.05 | 1.30 | 1.55 |
| y | - | - | 0.004 | - | - | 0.10 |
| $\theta$ | 0° | - | 12° | 0° | - | 12° |

Notes:

1.Dimensions D & E do not include interlead flash.

2.Dimension b does not include dambar protrusion/intrusion.

3.Controlling dimension: Millimeter

4.General appearance spec. should be based on final visual inspection spec.

| TITLE. 208 PQFP ( 28x28 mm) FOOTPRINT 2.6mm PACKAGE OUTLINE DRAWING | | | |
|---|---|---|---|
| LEADFRAME MATERIAL: | | | |
| APPROVE | | DOC. NO. | 530-ASS-P004 |
| | | VERSION | 1 |
| | | PAGE | |
| CHECK | | DWG NO. | Q208 - 1 |
| | | DATE | |
| REALTEK SEMICONDUCTOR CORP. | | | |

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