JEDEC STANDARD

Compute Express Link (CXL™) Memory Module Reference Base Standard

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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COMPUTE EXPRESS LINK (CXL™) MEMORY MODULE REFERENCE BASE STANDARD

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COMPUTE EXPRESS LINK (CXL™) MEMORY MODULE REFERENCE BASE STANDARD

(From JEDEC Board ballot JCB-23-09A formulated under the cognizance of the JC-45 Committee for DRAM Modules, item 2286.99).

1 Scope

This standard defines the specifications of interface parameters, signaling protocols, environmental requirements, packaging, and other features as reference for specific target implementations of CXL™-attached memory modules.

The purpose is to provide certain reference base targets for CXL™-attached memory modules to enable system design simplification, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Further module design detail may be later found in annexes that comply with this base specification and as associated with the specific base reference modules defined herein.

Unless otherwise noted in the document, device operation is not guaranteed.

JEDEC's CXL™ Memory Module (CMM) Reference Standard leverages and references specific external and JEDEC internal standards:

- PCI Express® (PCIe) Base Specification (https://www.pcisig.com)
- PCI Express® (PCIe) Card Electromechanical Specification (https://www.pcisig.com)
- Compute Express Link Consortium: CXL™ Specification (https://www.computeexpresslink.org/)
- SNIA SFF-TA-1002, Card Edge multilane protocol agnostic connector specification (https://www.snia.org/sff/specifications)
- SNIA SFF-TA-1006 Enterprise and Datacenter 1U Short Device Form Factor available (https://www.snia.org/sff/specifications)
- SNIA SFF-TA-1008 Enterprise and Datacenter Form Factor (https://www.snia.org/sff/specifications)
- SNIA SFF-TA-1009 Enterprise and Datacenter Standard Pin and Signal Specification (https://www.snia.org/sff/specifications)
- SNIA SFF-TA-1023 Thermal Characterization Specification for EDSFF Devices (https://www.snia.org/sff/specifications)
- JESD405-1 CXL™ Module Label Standard

1.1 Module Reference Standard

This standard encompasses a variety of requirements, many of which exist in the industry independently. In most cases, these external specifications are referenced directly without modification. In other cases, this standard provides specific implementations or restrictions on these standards for the intended application.

1.1 Module Reference Standard (cont'd)

Title	Clause	Description
Mechanical	Chapter 2	This clause describes the mechanical dimensions for the CMM Base Reference target form factors.
Pinout and Electrical	Chapter 3	This clause defines the module pin signal definitions, pin assignments, and electrical interface.
Protocol	Chapter 4	This clause defines and further describes the CMM protocol interface.
Power and Thermal	Chapter 5	This clause defines module power and thermal support and other related characteristics.
Environmental	Chapter 6	This clause defines the environmental characteristics including temperature, humidity, shock, and vibration.

Table 1 — JEDEC CMM Attributes - Quick Reference

Base Module Details	Value	CMM Reference Chapter
Enclosure Dimensions	118.75 mm x 34 mm x 15 mm	Chapter 2 (E1.S 15mm – Ref A)
	112.75 mm x 76 mm x 16.8 mm	Chapter 2 (E3.S 2T – Ref B)
	112.75 mm x 76 mm x 7.5 mm	Chapter 2 (E3.S 1T – Ref C)
Pin count	56, 84	Chapter 2 for connector and Chapter 3 for pinout
CXL™ link width	x4, x8	
CXL™ link speed	32 GT/s (PCIe Gen 5.0)	Chapter 3.2

1.2 CMM Basic Block Architecture

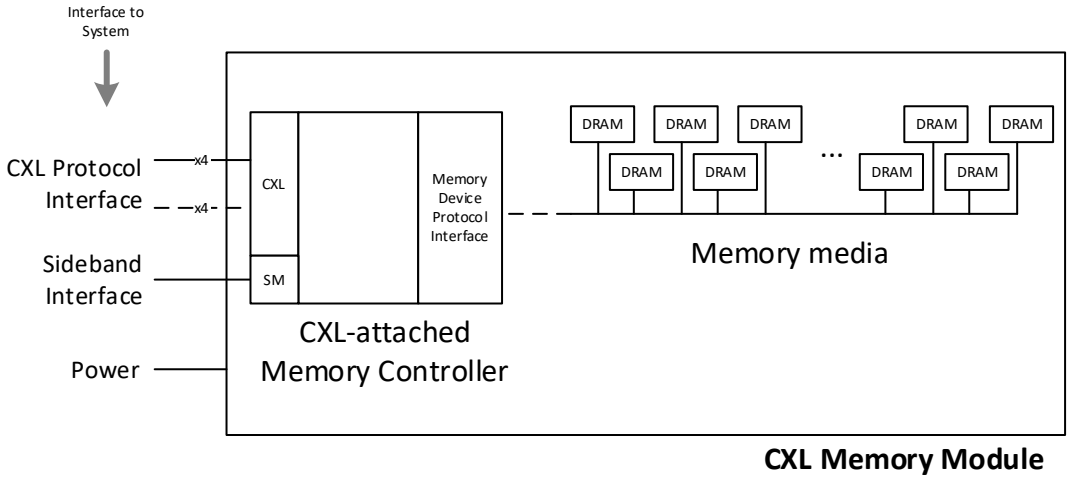

Figure 1 — CMM Basic Block Architecture

2 Mechanical Specifications

2.1 CMM Base Reference A: EDSFF E1.S

The module outer dimensions of this target reference module are 118.75 mm x 33.75 mm x 15 mm.

CMM “Reference A” interfaces according to the SFF-TA-1002 EDSFF connector specification Rev. 1.3, with 2C (x8) width configuration.

CMM “Reference A” adheres to the SFF-TA-1006 EDSFF E1.S form factor specification Rev. 1.5 and as defined for the 15mm variant in section 5.5.

CMM “Reference A” aligns with the SFF-TA-1009 specification for a x8 width (2C) CXL™ interface as described in Chapter 3.

External, reference only:

Figure 2 — Example E1.S Form Factor

2.2 CMM Base Reference B: EDSFF E3.S 2T

The module outer dimensions of this target reference module are 112.75 mm x 76 mm x 16.8 mm.

CMM “Reference B” interfaces according to the SFF-TA-1002 EDSFF connector specification Rev. 1.3, with 2C (x8) width configuration.

CMM “Reference B” adheres to the SFF-TA-1008 EDSFF E3 form factor specification Rev. 2.0 and as defined for the 2T (16.8 mm) variant in section 5.3.

CMM “Reference B” aligns with the SFF-TA-1009 specification for a x8 width (2C) CXL™ interface as described in Chapter 3.

2.3 CMM Base Reference C: EDSFF E3.S 1T

The module outer dimensions of this target reference module are 112.75 mm x 76 mm x 7.5 mm.

CMM “Reference C” interfaces according to the SFF-TA-1002 EDSFF connector specification Rev. 1.3, with 1C (x4) width configuration.

CMM “Reference C” adheres to the SFF-TA-1008 EDSFF E3 form factor specification Rev. 2.0 and as defined for the 1T (7.5 mm) variant in clause 5.2.

2.3 CMM Base Reference C: EDSFF E3.S 1T (cont'd)

CMM "Reference C" aligns with the SFF-TA-1009 specification for a x4 width (1C) CXL™ interface as described in Chapter 3.

External, reference only:

Figure 3 — Example E3.S Form Factor

3 Pinout and Electrical Specification

3.1 Pin Description and Assignment

CMM Base References A and B adhere to the x8 (2C) signal description and pin assignment as described in SNIA SFF-TA-1009 Enterprise and Datacenter Standard Pin and Signal Specification, Revision 3.0a.

Signal and pinout in Tables 2 and 3 are provided as reference only.

Table 2 — CMM Signal Description: Ref A and B

Interface	Signal Name	Host I/O	Function	Voltage
Power and Grounds	12 V	O	+12 V power	12V
	3.3 Vaux	O	+3.3 V power	3.3V
	GND	O	Return current path	0V
PCIe	PETp0, PETn0	O	PCIe TX Differential signals defined by the PCI Express Card Electromechanical Specification. PETp/n[0..3] are supported in the x4, x8, and x16 connectors. PETp/n[4..7] are supported with the x8 and x16 connectors. PETp/n[8..15] are supported only with the x16 connector.	
	PETp1, PETn1			
	PETp2, PETn2			
	PETp3, PETn3			
	PETp4, PETn4			
	PETp5, PETn5			
	PETp6, PETn6			
	PETp7, PETn7			
	PETp8, PETn8			
	PETp9, PETn9			
	PETp10, PETn10			
	PETp11, PETn11			
	PETp12, PETn12			
	PETp13, PETn13			
	PETp14, PETn14			
	PETp15, PETn15			
	PERp0, PERn0	I	PCIe RX Differential signals defined by the PCI Express Card Electromechanical Specification. PERp/n[0..3] are supported in the x4, x8, and x16 connectors. PERp/n[4..7] are supported with the x8 and x16 connectors. PERp/n[8..15] are supported only with the x16 connector.	
	PERp1, PERn1			
	PERp2, PERn2			
	PERp3, PERn3			
	PERp4, PERn4			
	PERp5, PERn5			
	PERp6, PERn6			
	PERp7, PERn7			
	PERp8, PERn8			
	PERp9, PERn9			
	PERp10, PERn10			
	PERp11, PERn11			
	PERp12, PERn12			
	PERp13, PERn13			
	PERp14, PERn14			
	PERp15, PERn15			

Table 2 — CMM Signal Description: Ref A and B (cont'd)

Interface	Signal Name	Host I/O	Function	Voltage
PCIe	REFCLKp0, REFCLKn0	O	PCIe Reference Clock signals defined by the *PCI Express Base Specification*.	
	PERST0#	O	PE-Reset is a fundamental reset to the device defined as PERST# by the *PCI Express Base Specification*.	3.3V
	REFCLKp1, REFCLKn1	O	PCIe Reference Clock signals defined by the *PCI Express Base Specification*. This clock is for dual port mode only and is only used if DUALPORTEN# is low.	
	PERST1#/CLKREQ#	I/O	PERST1#: PE-Reset is a fundamental reset to the device defined as PERST# by the *PCI Express Base Specification*. If dual port mode is supported by the device, PERST1# is only used when DUALPORTEN# is low. CLKREQ#: Clock Request is a reference clock request signal defined by the *PCI Express Base Specification.* It may be supported by a device in single port mode only. If CLKREQ# is supported by the host and the device, then the signal is Open Drain with a pull up on host.	3.3V
Sideband Signals	PRSNT0#	I	Active low signal. This signal indicates to the host that the device is electrically attached.	3.3V
	PRSNT1#	I	Active low signal. This signal is available in the x8 and x16 versions of the connector as a 2nd presence signal to indicate to the host that the device is electrically attached. This signal is not available in the x4 version of the connector.	3.3V
	PRSNT2#[1]	I	Active low signal. This signal is available in the x16 connector as a 3rd presence signal to indicate to the host that the device is electrically attached. This signal is not available in the x4 and x8 versions of the connector.	3.3V
	SMBCLK	O	SMBCLK: Open Drain with pull-up on host. SMBus Clock.	3.3V
	SMBDATA	I/O	SMBDATA: Open Drain with pull-up on host. SMBus Data.	3.3V
	SMBRST#	O	Active low signal. SMBRST# is a reset for the management interface.	3.3V
	DUALPORTEN#	O	Open drain. Pull-up on device. This signal indicates if dual port mode is supported by the host.	3.3V
	LED	O	Active high signal. This signal is used to drive the amber or amber/blue LED state from the host to the device.	3.3V
	PWRDIS	O	Active high signal. Power Disable notifies the device to turn off all systems connected to 12 V power.	3.3V
	MFG	N/A	Manufacturing mode, signal used only for the manufacturing of the device.	N/A
	RFU	N/A	Reserved for Future Use	N/A

NOTE 1 PRSNT2# is not used in the 2C connector.

3.1 Pin Description and Assignment (cont'd)

Table 3 — CMM Pinout: Ref A and B

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B1	2nd mate	12 V	GND	1st mate	A1
B2	2nd mate	12 V	GND	1st mate	A2
B3	2nd mate	12 V	GND	1st mate	A3
B4	2nd mate	12 V	GND	1st mate	A4
B5	2nd mate	12 V	GND	1st mate	A5
B6	2nd mate	12 V	GND	1st mate	A6
B7	2nd mate	MFG	SMBCLK	2nd mate	A7
B8	2nd mate	RFU	SMBDATA	2nd mate	A8
B9	2nd mate	DUALPORTEN#	SMBRST#	2nd mate	A9
B10	2nd mate	PERST0#	LED	2nd mate	A10
B11	2nd mate	3.3 Vaux	PERST1#/CLKREQ#	2nd mate	A11
B12	2nd mate	PWRDIS	PRSNT0#	2nd mate	A12
B13	1st mate	GND	GND	1st mate	A13
B14	2nd mate	REFCLKn0	REFCLKn1	2nd mate	A14
B15	2nd mate	REFCLKp0	REFCLKp1	2nd mate	A15
B16	1st mate	GND	GND	1st mate	A16
B17	2nd mate	PETn0	PERn0	2nd mate	A17
B18	2nd mate	PETp0	PERp0	2nd mate	A18
B19	1st mate	GND	GND	1st mate	A19
B20	2nd mate	PETn1	PERn1	2nd mate	A20
B21	2nd mate	PETp1	PERp1	2nd mate	A21
B22	1st mate	GND	GND	1st mate	A22
B23	2nd mate	PETn2	PERn2	2nd mate	A23
B24	2nd mate	PETp2	PERp2	2nd mate	A24
B25	1st mate	GND	GND	1st mate	A25
B26	2nd mate	PETn3	PERn3	2nd mate	A26
B27	2nd mate	PETp3	PERp3	2nd mate	A27

Table 3 — CMM Pinout: Ref A and B (cont'd)

Pin	Contact Sequence	Signal	Signal	Contact Sequence	Pin
B28	1st mate	GND	GND	1st mate	A28
		Key	Key		
B29	1st mate	GND	GND	1st mate	A29
B30	2nd mate	PETn4	PERn4	2nd mate	A30
B31	2nd mate	PETp4	PERp4	2nd mate	A31
B32	1st mate	GND	GND	1st mate	A32
B33	2nd mate	PETn5	PERn5	2nd mate	A33
B34	2nd mate	PETp5	PERp5	2nd mate	A34
B35	1st mate	GND	GND	1st mate	A35
B36	2nd mate	PETn6	PERn6	2nd mate	A36
B37	2nd mate	PETp6	PERp6	2nd mate	A37
B38	1st mate	GND	GND	1st mate	A38
B39	2nd mate	PETn7	PERn7	2nd mate	A39
B40	2nd mate	PETp7	PERp7	2nd mate	A40
B41	1st mate	GND	GND	1st mate	A41
B42	2nd mate	PRSNT1#	RFU	2nd mate	A42

3.2 Electrical Specifications

CMMs support PCI Express® (PCIe) Base Specification, Revision 5.0, Version 1.0

CMMs support a peak transfer rate of 32 Gb/s on each lane of PCIe.

CMMs support SFF-TA-1002 Signal Integrity Requirements per Section 5 of the specification

CMMs support SFF-TA-1009 Signal Integrity Requirements per Section 8 of the specification

4 Protocol Requirements

4.1 Protocol Requirements

CMMs are compatible with the Compute Express Link™ Specification 2.0

CMMs support at minimum CXL.io and CXL.mem protocols

5 Power and Thermal Requirements

5.1 Power Classes

CMM Power Classes define the maximum sustained power that is thermally relevant to the device (change in power resulting to measurable temperature change by 0.1 ºC or more)

Table 4 — Power Classes

Power Class Reference	Value	Notes
Class 1A	6 W	
Class 1B	12 W	
Class 2A	25 W	Common target for EDSFF modules
Class 3A	30 W	
Class 4A	40 W	
Class 5A	75 W	
Class 6A	150 W	

5.2 Thermal Guidelines

CMMs follow the SNIA SFF-TA-1023 Thermal Characterization Specification for EDSFF Devices, Revision 1.0a for characterization of module thermal performance.

6 Environmental Requirements

6.1 Module Environmental Requirements

Table 5 — Environmental Requirement Parameters

Symbol	Parameter	Rating		Units	Acronym	Notes
		Min	Max			
TOPR	Operating Temperature	0	+95	°C	XT	1
TSTG	Storage Temperature	-55	+100	°C	Tstg_extended1b	2

NOTE 1 Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs is at the minimum and maximum values. See JESD402-1 for details.

NOTE 2 Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability

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