JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163A

(Revision of JEP163 dated September 2015)

DECEMBER 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2022
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Contact JEDEC

This page intentionally left blank

SELECTION OF BURN-IN/LIFE TEST CONDITIONS AND CRITICAL PARAMETERS FOR QML MICROCIRCUITS

Contents

Foreword

This publication was developed as a guideline to assist manufacturers of integrated circuits (microcircuits) in defining the conditions for burn-in and life test of their products to meet the quality and reliability performance requirements of MIL-PRF-38535 and the applicable Standard Military Drawing. Documentation of the manufacturer's technical rationale in accordance with this guideline will also facilitate customer understanding and acceptance of the manufacturer's Quality Management (QM) plan.

Introduction

MIL-PRF-38535, in conjunction with MIL-STD-883, defines the basic screening requirements for compliant microcircuits. MIL-STD-883 Test Method 5004 specifies two independent burn-in conditions for Class Level S devices. A dynamic burn-in is performed for 240 hours at 125°C. A static or reverse bias burn-in is performed for 72 hours at 150°C. Per Test Method 5004 the reverse bias burn-in is a requirement only when specified in the applicable device specification (i.e. Standard Military Drawing) and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern.

These requirements have been part of the military standards for decades and originated at a time when design rules and wafer fabrication processes were much less advanced than current state-of-the art technologies. With the advent of improved wafer fabrication processes, Statistical Process Controls (SPC), Wafer Level Reliability (WLR), Circuit Design Tools, Design-For-Test (DFT) techniques, and modern simulation and characterization techniques, the presence of certain failure modes have been reduced and/or eliminated for certain wafer fabrication processes. However, deep submicron and System On A Chip wafer fabrication processes have potentially greater transistor to transistor process variations; hence, they may have a greater need for burn-in and life test to evaluate and screen infant life mortality. Due to the current variation in geometry sizes and different levels of technology maturity and circuit designs, the establishment of the appropriate burn-in/life test stress and test conditions must be evaluated in relation to each product's wafer fabrication process and circuit design techniques. The stress conditions must demonstrate adequate Early Failure detection and Intrinsic Failure Rate (IFR) performance that meets customer failure rate requirements. For example, a typical space application has a goal of 10 to 15 years operating life.

SELECTION OF BURN-IN/LIFE TEST CONDITIONS AND CRITICAL PARAMETERS FOR QML MICROCIRCUITS

(From JEDEC Board Ballot JCB-22-50, formulated under the cognizance of JC-13 Committee: Government Liaison.)

1 Scope

This publication is intended as a guideline to develop and establish conditions for burn-in and life test of MIL-PRF-38535 QML integrated circuits. These guidelines are intended to provide manufacturers with a consistent means of defining burn-in and life test stress and electrical test requirements acceptable to user organizations and for the development of Standard Military Drawings.

The guidelines cover the entire design, wafer fabrication and manufacturing flows, including design and process awareness. Without design awareness (critical circuit blocks/functionality, etc.), burn-in/life test of an integrated circuit might be compromised, or it might dramatically shorten the device's life prior to system use.

2 References

EEE-INST-002, *Instructions for EEE Parts Selection, Screening, Qualification, and Derating (NASA Goddard Space Flight Center)*

JEP122, *Failure Mechanisms and Models for Semiconductor Devices*

JESD85, *Methods for Calculating Failure Rates in Units of FITs*

MIL-HDBK-1331, *Handbook for Parameters to be Controlled for the Specification of Microcircuits (DLA Land and Maritime)*

MIL-PRF-38535, *General Specification for Integrated Circuits (Microcircuits) Manufacturing (DLA Land and Maritime)*

MIL-STD-883, *Test Method Standard Microcircuits (DLA Land and Maritime)*

3 Terms and Definitions

For the purposes of this publication, the terms and definitions given in the above references and the following apply:

absolute maximum rated junction temperature: The maximum junction temperature of an operating device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

NOTE Manufacturers may also specify maximum case temperatures for specific packages.

3 Terms and Definitions (cont'd)

absolute maximum rated voltage: The maximum voltage that may be applied to a device, as listed in its data sheet and beyond which damage (latent or otherwise) may occur; it is frequently specified by device manufacturers for a specific device and/or technology.

acceleration factor (A, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of 1/kT, the reciprocal of the product of Boltzmann's constant in electron-volts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electron-volts.

NOTE 4 The abbreviation AF is often used in place of the symbol A.

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature.

NOTE 1 This is the acceleration factor most often referenced. The Arrhenius equation for reliability is commonly used to calculate the acceleration factor that applies to the acceleration of time-to-failure distributions for microcircuits and other semiconductor devices:

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp[(-E_{aa}/k)(1/T_1 - 1/T_2)]$$

Where:

E_{aa} is the apparent activation energy (eV);

k is Boltzmann's constant (8.62×10^{-5} eV/K);

T_1 is the absolute temperature of test 1 (K);

T_2 is the absolute temperature of test 2 (K);

λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});

λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1}).

NOTE 2 The best-fit linear slope of a plot of the natural log of the time-to-failure as a function of 1/kT, the reciprocal of the product of Boltzmann's constant in electron-volts per kelvin and the absolute temperature in kelvins, is equal to the apparent activation energy in electron-volts.

NOTE 3 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s.

3 Terms and Definitions (cont'd)

activation energy (E_a): The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur.

NOTE The activation energy is used in the Arrhenius equation for the thermal acceleration of physical reactions. The term "activation energy" is not applicable when describing thermal acceleration of time-to-failure distributions, e.g., in the Arrhenius equation for reliability; hence the need for the term "apparent activation energy."

apparent activation energy (E_{aa}): An energy value, analogous to activation energy, that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions.

NOTE 1 An apparent activation energy should be associated with a specific failure mechanism and an observed time-to-failure distribution to calculate the acceleration factor for converting the observed failure rate to the quoted failure rate at a different temperature.

NOTE 2 An activation energy is a measure of the heat energy needed to establish the rate of reaction for a specific failure mechanism. The reaction rate and other contributing factors, e.g., radiation, voltage, humidity, magnetic fields, determine the unique time-to-failure distribution for the modeled failure mechanism.

NOTE 3 The apparent activation energy is empirically determined from the change in an observed time- to-failure distribution with temperature.

failures in time (FITs): The number of failures per 10^9 device hours.

high-temperature forward-bias (HTFB) test: A static test configured to forward-bias at least a majority of the solid-state junctions of the devices operating at, or near, absolute maximum rated junction temperature and voltages.

high-temperature reverse-bias (HTRB) test: A static test configured to reverse-bias at least a majority of the solid-state junctions of the devices operating at, or near, absolute maximum rated junction temperature and voltages.

NOTE For some CMOS circuits, any static state will reverse-bias approximately half the junctions (others are zero-biased).

recommended operating conditions: The operating conditions, such as supply voltage and junction temperature, at which a device is specified to operate in compliance with the applicable device specification or data sheet.

NOTE 1 Maximum and minimum values are applicable; these adjectives refer to the magnitudes.

NOTE 2 The maximum recommended operating supply voltage is not the absolute maximum rated voltage, i.e., the voltage beyond which, damage is likely.

toggle coverage: The percentage of signals in a device that are toggled (transitioned Low to High and from High to Low) during one complete cycle (an entire sequence of applied signals).

4 Wafer Fabrication and Design Considerations

The goal of burn-in is to screen early life defects. These defects are normally due to variation or anomalies within the wafer fabrication process or circuit design. The burn-in stress needs to be negligible with regard to life time wearout mechanisms.

Wafer fabrication defect density variation, ionic contamination sources, process variability, parametric performance variability, and other potential process features contribute to early life failures. The use of Statistical Process Controls (SPC) helps ensure the consistency of the wafer fabrication process.

An FMEA (Failure Mode Effects Analysis) assessment in regards to design, transistor layout and interconnect technology in concert with the wafer fabrication process and the processes' capabilities and limitations is needed to help identify potential early life failure modes and wearout mechanisms.

The FMEA provides identification of those process/design features that need to be evaluated using wafer level reliability (WLR) assessments. This reliability assessment is needed to accelerate life time wearout mechanisms that cannot be determined without extensive long term stress testing.

The device design shall then be reviewed in regards to Design for Test / Design for Burn-in for the controllability/observability of the mechanisms to be observed in order to develop the appropriate burn-in and life test conditions.

There are many stresses that accelerate various failure mechanisms in silicon. Such stresses include temperature, voltage, frequency and current density. Acceleration factors for typical individual failure mechanisms are found in JEP122. The performance of accelerated reliability assessments of the given technology can provide a more accurate determination of the wafer process failure mechanism acceleration factors.

5 Burn-In Stress and Electrical Test Conditions Development

5.1 Considerations for Burn-In Stress Conditions

The basic burn-in test conditions are defined in MIL-STD-883, Test Method 1015. The key to determine the appropriate burn-in condition is the integrated circuit design, its use of transistors, and interconnect layouts within a wafer fabrication process.

Burn-in configurations may be bias stress (static or pulsed) and/or operating stress (dynamic). Depending upon the biasing configuration, input voltages may be grounded or raised to a maximum potential chosen to ensure a stressing temperature not higher than the maximum-rated junction temperature. Device outputs may be unloaded or loaded, to achieve the specified output voltage level. If a device has a thermal shutdown feature it shall not be biased in a manner that could cause the device to go into thermal shutdown. Logic being observed with burn-in monitor pin needs to be determined and properly set. Device enable pins must be properly set to ensure maximum stressing and operation of the functional circuits.

5.1 Considerations for Burn-In Stress Conditions (cont'd)

Static Burn-in:

Static burn-in is typically considered more effective than dynamic burn-in for defects resulting from intermetallic formation or contamination (e.g., surface issues). Using well-controlled wafer fabrication processes in conjunction with a well-designed wafer level reliability program, contamination defects have been greatly diminished. There are still a number of older technology components being produced using less that state-of-the-art facilities; therefore, static burn-in may still be necessary in some instances to safeguard against failure mechanisms such as mobile ion contamination.

The part is powered on and held in a static configuration for the duration of stress. In reverse bias, the goal is to hold each junction in a single state. This is effective to activate ionic contaminants by creating a consistent electric field. Static condition can be achieved by configuring the part in a repeatable low power (I_{DDQ}) state. The bias voltage should be set to create the highest possible voltage field condition.

The selection among the following static burn-in approaches is dependent upon the circuit design for creation of a static bias across all transistors. A single static burn-in is sufficient for some technologies such as digital CMOS in which all of the transistors are biased in reverse or zero bias field. Otherwise, two static burn-in circuits may be needed in order to properly stress the active circuit areas.

i) Single circuit used with half of the inputs biased low and the other half biased high.

- Post static burn-in electrical.

ii) Two circuits used.

- All inputs low (Static I)
- All inputs high (Static II)
- Post static burn-in electrical performed after completion of both (Static I and Static II) burn-ins.

iii) Two circuits used.

- All inputs low (Static I)
- All inputs high (Static II)
- Post static burn electrical performed after completion of each static burn-in (This approach may be needed if the potential failure mode recovers after removal of bias and is not observable after the 2nd static burn-in. This is the default condition unless proven otherwise.)

Dynamic Burn-in:

Dynamic burn-in is intended to simulate the operation of the device in an application. Dynamic burn-in is typically more effective applying stresses within internal circuitry at a higher degree than static burn-in. The goal of dynamic burn-in is to place a maximum field across as many internal circuits as possible, resulting in maximum defect screening. The temperature, dynamic current and output states of the device under test should be monitored during burn-in.

5.1 Considerations for Burn-In Stress Conditions (cont'd)

The selection of static and/or dynamic burn-in is based on the susceptibility of the product to the failure mechanisms in Table 1.

Table 1 — Burn-In Mechanisms

Failure Mechanism	Acceleration Factors	Failure Mode/Location	Type/Stress Mode
Mobile Ions/Surface Charging	Voltage, Temperature	Well - Well Leakage	Contamination/Static
Gate Oxide Integrity	Voltage, Temperature	Gate Oxide leakage	Defect/Dynamic
Back End of Line (BEOL) Defects	Voltage, Temperature	Metal, Interlevel Dielectrics	Defect/Dynamic

- The ambient burn-in test temperature should be 125°C minimum. Since case and junction temperature will, under normal circumstances, be significantly higher than ambient temperature, the circuit employed should be so structured that maximum rated junction temperature for test or operation shall not exceed 200°C for class level B or 175°C for class level S.
- For devices whose maximum operating temperature is stated in terms of case temperature T_C or junction temperature T_J, and whose operation cannot exceed the maximum allowable junction temperature, the ambient life test operating temperature may be reduced. The ambient temperature may be reduced from +125°C T_A or T_C, provided T_J is maintained within 10% of its maximum specified value. The burn-in duration shall be adjusted to ensure the equivalent stress remains the same under these modified conditions.
- Some products may have restricted temperature ranges due to the materials properties limitation and/or have high power consumption. Exceeding the maximum allowable temperature could accelerate the degradation of the product and may render it un-reliable. The reliability can be compromised by exposing the devices to excessive burn-in temperature. The reliability can also be compromised if the devices see subsequent excessive temperatures such as during column attach or during circuit board installation.
- Some elements of a microcircuit product such as solder attach of chip capacitors may also limit the allowable burn-in stress temperature.
- The processing of solder finish products through burn-in is also not recommended due to the potential of scraping or deforming the solder finish. A secondary solder finish application may be necessary post burn-in.
- Voltage stress per pinned out product supplies and for internal regulators will determine the number of voltage supplies required for burn-in.
- The value of each supply should be evaluated to set the requirement of supply domain level shifters and the voltage and temperature conditions for reliability validation.

5.1 Considerations for Burn-In Stress Conditions (cont'd)

- Complex digital logic should be exercised by patterns that address predominant failure mechanisms with a minimum toggle coverage of 70%. These patterns need to be simulated and verified operational on an ATE at the same junction temperature as they would run in the Burn-in chamber.
- For system on a chip, analog logic should be exercised by test description logic (TDL) driven analog system patterns or tested through built-in self-test (BIST) circuitry. The toggle coverage goal should be 70% or higher if possible. The analog BIST function should reflect worst case customer "system" operation of analog circuitry.
- BIST patterns should be used to stress the memories.
- Note that burn-in pattern toggle coverage and pattern coverage should not to be confused with electrical test fault coverage as specified in MIL-PRF-38535 and MIL-STD-883.
- For high-speed digital circuits, consideration must be made to maximize the burn-in oven frequency to ensure that the device is adequately stressed to screen the failure mechanisms intended. The typical burn-in chamber timing generator is capable of <10 MHz although some specialized systems are capable of much higher frequencies.
- For complex processors, system on a chip, and memory circuits, gate oxide is best stressed using supply voltages above normal recommended operating conditions. This over-voltage must be evaluated in conjunction with burn-in time and temperature to avoid overstress of the component. It must be determined whether the product will functionally run at the accelerated stress voltage conditions. Caution must be exercised to assure maximum operating conditions are not exceeded unless data is provided.
- The appropriate stressing of EEPROMs is addressed within JESD22-A117, Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test.

5.2 Electrical Test and Data Analysis for Burn-In

The electrical test analysis begins with the determination of the key test parameters to be measured. Annex B provides a guideline for the key parameters for various technologies. The test program development needs to ensure key parameters have adequate tester resolution to identify outlier measurements. The tester variation, independent of the product, needs to be understood in order to quantify whether the source of variation in measurement is due to the test setup vs. the product.

Consideration must also be given to the sensitivity of the product in relation to test temperature variation in assuring a consistent measurement environment from pre-to-post burn-in electrical test measurements. The pre-to-post delta-shift measurements are restricted to room temperature to provide a more accurate means of comparison. Most products have a higher variability of readings at hot and/or cold temperatures due to the temperature effects in socket contact and higher sensitivity to small changes in temperature. The test limits for the delta parameters should be split into room temp and over temp limits (reference Table I of the DLA Standard Microcircuit Drawing). It is important to ensure that subsequent testing is performed with proper range scaling to prevent measurement error.

5.2 Electrical Test and Data Analysis for Burn-In (cont'd)

Device variability, wafer to wafer and within a wafer, has been observed to increase with smaller geometry technologies. It is more important than ever to understand the impact of burn-in on device performance and variability. To assess variations that are present, the following evaluation is suggested:

- Use a sample from three separate wafer lots or utilize a single split-lot where wafers are run at low, nominal, and upper limits of the distribution for critical in-process parameters. With small volume application specific products there may be just one wafer lot to perform the analysis.
- Collect data on critical device parameters pre and post burn-in electrical test.
- Evaluate the measurement data and determine if the distribution is normal before calculating a C_{PK} capability distribution. This includes an analysis of pre and post burn-in room electrical test drift for the selected parameters. It is recommended that a C_{PK} of 1.33 or better be the target for critical parameters. The C_{PK} may be dependent on the "competitiveness/risk-to-produce" trade-off as these are nominally conflicting goals. The analysis should determine the normal variability of the product and be able to distinguish outlier readings. This analysis should result in the determination of the acceptable absolute limits and pre and post drift limits. This will serve as the basis for the limits to be set in the SMD. Once this evaluation is complete and appropriate limits are set, the controls must be implemented to ensure acceptable product.
- Tight parametric limits (guard bands) may be set on critical parameters at wafer level or packaged product electrical test to remove marginal devices from the lot distribution.
- Outlier yield limits should be considered at each electrical test point in addition to normal burn-in PDA. For example, a low yield at first electrical test, or +125°C / -55°C, may indicate an outlier lot. These "maverick" lots should be carefully evaluated by test engineering and quality assurance prior to allowing continuation of processing.
- Yield fall-out may not be a reliability or a process problem; transistor models and circuit designers often push the limits. For a small manufacturing lot/design a "low yield" may be acceptable because limits were pushed.

6 Life Test Stress and Electrical Test Conditions Development

6.1 Considerations for Life Test Stress Conditions

The basic life test conditions are defined in MIL-STD-883, Test Method 1005. Life test is intended to evaluate the effects of wearout over the life of the product. The life test demonstration is an interim life test due to the obvious impracticality of performing a life test for 10 to 15 years. The interim life test results are statistically analyzed to provide a mathematical estimate of the product life. Life test is typically run for 1000 hours at 125ºC with alternate temperatures and durations based on acceleration factors and activation energy detailed in Test Method 1005.

There are many stresses that accelerate various failure mechanisms in silicon. Such stresses include temperature, voltage, frequency and current density.

6.1 Considerations for Life Test Stress Conditions (cont'd)

The dynamic mode should be considered for life test, if the normal wearout mechanisms need active currents to be activated. Some of the wearout mechanisms are not current activated (i.e. TDDB, NVM endurance/retention). It needs to be decided if life test is to be done as the part will be operated or if the purpose of life test is to verify intrinsic reliability limitations.

If the purpose is to verify intrinsic reliability limitations, then it is not as important to stress every circuit component on a part with all bias combinations. It is more important to stress representatives of each type of component within a design at a single optimal stress condition for maximum duration.

For example, with a complementary CMOS circuit design, about half the transistors would be forward biased, and half reverse biased for each external bias condition. For TDDB, using a static bias condition will stress roughly half of the transistor oxides for the full 1000 hour duration. Whereas, if you use a dynamic approach and take each transistor through both logic low and high states, then the total stress for any oxide would be roughly 500 hours. The static 1000 hour stress would be a better indicator of intrinsic reliability even though not every transistor would see equal stress.

The differences between digital and analog circuits also need to be considered, since dynamic stress may be needed to affect negative bias temperature instability (NBTI) mechanisms, positive bias temperature instability (PBTI) mechanisms, or channel hot carrier (CHC) mechanisms for a digital circuit, but could potentially be stressed with a static condition on an analog part.

The typical wearout mechanisms are listed in Table 2.

Table 2 — Life Test Wearout Mechanisms

Failure Mechanism	Acceleration Factors	Failure Mode/Location	Type
Electromigration	Voltage, Temperature, Current, Frequency	Metallization	Wearout
Time Dependent Dielectric Breakdown	Electric Field	Gate Oxide	Wearout
Intermetallic Growth	Temperature	Bi-metallic Wire Bonds	Wearout
Bias Temperature Instability	Temperature, Voltage	MOSFET Degradation	Wearout
Contact Resistance	Temperature	Metallization, Vias	Wearout
Aluminum-Silicon Diffusion	Temperature	Metallization Over Silicon	Wearout
Non-Volatile Memory Retention/Endurance	Temperature, voltage	Memory cell	Wearout
Channel Hot Carrier	Voltage, Frequency, Temperature	MOSFET Degradation	Wearout

6.1 Considerations for Life Test Stress Conditions (cont'd)

The performance of life testing may need to be conducted using more than one circuit design. The device circuitry needed to demonstrate maximum frequency performance for a new technology may not be compatible for the frequencies needed to properly exercise a product in assessing other potential wearout conditions.

- For high-speed digital circuits, consideration must be given for the maximum life test frequency to ensure that the device is adequately stressed to detect the failure mechanisms intended. For example, gate oxide stresses in the memory and core versus electromigration in the inputs and outputs.

The considerations of dynamic life test patterns are similar to those earlier described for burn-in stress. They need to comprehend the targeted/required life test frequency, toggle coverage, junction temperature monitoring, etc., to control proper life test of a device.

- When performing high-frequency life test stressing, consideration must be given to ensure the maximum allowable junction temperature is not exceeded. This will require a means to determine the junction temperature. This may be accomplished with a temperature sensor on the die or some other means to determine or calculate junction temperature. This may result in reducing the oven temperature but at the same time ensure the worst case ambient use conditions are represented by the life test stress.
- Complex digital logic should be exercised by patterns that address predominant failure mechanisms with a minimum toggle coverage of 70%. These patterns need to be simulated and verified operational on an ATE at the same junction temperature as they would run in the life test chamber.
- The appropriate life test stressing of EEPROMs is addressed within JESD22-A117, Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test.

6.2 Electrical Test and Data Analysis for Life Test

Just like burn-in, the electrical test analysis begins the determination of the key test parameters to be measured. Annex B provides a guideline for the key parameters for various technologies.

The test program development needs to ensure key parameters have adequate tester resolution to identify outlier measurements. The tester variation, independent of the product, needs to be understood in order to quantify whether the source of variation in measurement is due to the test setup vs. the product.

Consideration must also be given to the sensitivity of the product in relation to test temperature variation in assuring a consistent measurement environment from pre-to-post burn-in electrical test measurements. The pre-to-post delta-shift measurements are restricted to room temperature to provide a more accurate means of comparison. Most products have a higher variability of readings at hot and/or cold temperatures due to the temperature effects in socket contact and higher sensitivity to small changes in temperature.

- Use a sample from three separate wafer lots or utilize a single split-lot where wafers are run at low, nominal, and upper limits of the distribution for critical in-process parameters. With small volume application specific products there may be just one wafer lot to perform the analysis.

6.2 Electrical Test and Data Analysis for Life Test (cont'd)

- Collect data on critical device parameters pre and post life electrical test.
- Evaluate the measurement data and determine if the distribution is normal before calculating a C_{PK} capability distribution. This includes an analysis of pre and post burn-in room electrical test drift for the selected parameters. It is recommended that a C_{PK} of 1.33 or better be the target for critical parameters. The C_{PK} may be dependent on the "competitiveness/risk-to-produce" trade-off as these are nominally conflicting goals. The analysis should determine the normal variability of the product and be able to distinguish outlier readings. This analysis should result in the determination of the acceptable absolute limits and pre and post drift limits. This will serve as the basis for the limits to be set in the SMD.
- Due to the wide variations in activation energies that comprise the semiconductor failure mechanisms during life tests, the results are used to calculate a failure rate per JESD85 using an activation energy representing the dominant failure mechanism which has typically been 0.7 eV for integrated circuits. For historical technology nodes with gate oxide thicknesses >4nm, the thermal activation energy of 0.7 eV may be used. For newer, more complex and smaller technology nodes, characterization of the technology should evaluate potential failure mechanisms and mitigation strategies, calculations of activation energies and acceleration factors for the failure modes identified, and establishment of long term reliability failure rates, based on the manufacturer's technology characterization-specific data

Annex A (Informative) Example Burn-In Condition Evaluations

Without FMEA, the designer, reliability engineer, burn-in engineer, and test engineer do not know what the "best" burn-in condition may be. Each circuit is unique in its implementation. An outline for a "methodology" to determine the best burn-in / life test analysis is needed. The following examples represent different approaches for burn-in/life test biasing and stimulus for various circuit functions and wafer fabrication technologies.

Case 1 - Analog to Digital Converter

- Bipolar analog core operates from a 5-V supply, while the output uses a 3.3-V supply to provide LVDS compatible outputs.
- The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages with the outputs combined in a digital correction logic block.
- Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in data latency of four clock cycles, after which the output data is available as a 13-bit parallel word, coded in offset binary format.
- The analog input consists of an analog differential buffer followed by a bipolar track-and- hold. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500 Ω resistor connected from.
- 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.
- Power Supply: 5.0 V – AV_{DD}, 3.3 V DV_{DD}, 4.0 V – Oscillator supply.
- Differential Input levels: $A_{IN}+$ = 2.9 V (applied), $A_{IN}-$ = 2.4 V (input common mode is set internally).
- Clocking scheme: An on-board oscillator chip is installed which provides a 3.0 V p-p, 170 MHz single-ended clocking scheme.
- Device Outputs: Outputs D0 through D11 differential pair and OVR, DRY pair are open. The MSB output differential pair D12 is used for monitoring.
- Power consumption/Supply current: 1.9 W, 330 mA AV_{DD}, 70 mA DV_{DD}, 6 mA Oscillator.

Dynamic life test is the right scheme to use for this device type. Clocking keeps the functional blocks of the device operating in the nominal range. The bulk of the supply current is consumed by bipolar analog/digital circuitry. Bipolar ECL (Emitter-Coupled Logic) scheme is used in the digital portion of the circuitry which includes clock, digital error correction and digital output circuitry. MOS circuitry is used almost in entirety as global bias circuit for bipolar analog and digital block's transistor base input current. MOS is also used in the fuse trim circuitry.

Annex A (Informative) Example Burn-In Condition Evaluations (cont'd)

Case 2 - Wideband, Fully Differential Amplifiers

- In choosing bias conditions for burn-in, target applications for these devices must be considered. However, since these are analog devices, there are an infinite number of potential bias levels that could be applied within the recommended operating conditions. It is this uncertainty of signal characteristics that makes static burn-in at nominal bias conditions equally valid to any arbitrary dynamic condition. Therefore, the bias conditions were selected based on nominal input and output conditions targeted for each device type. The output will be driven high or low depending on whether the respective V_{IO} of each device is positive or negative. This essentially gives a random sample of bias conditions across the population of devices.
- Static burn-in is therefore optimal for this device. V_S+ = 5V, V_S- = GND, Power Dissipation 200 mW

Case 3 – Amplifiers

- The device is a dual, single-supply, 10-MHz-bandwidth amplifier featuring rail-to-rail inputs and outputs. The device is manufactured on a mature bipolar wafer fabrication process. It operates from 3 V to 30 V (or ± 1.5 V to ± 15 V).
- The manufacturer selected forward-bias static burn-in condition (MI-STD-883, TM1015 condition B) for this device. +/-V_S are set to +/-15 V. In this burn-in circuit, the op amp is connected in a voltage follower configuration with a 10 kΩ load, 1 kΩ in the feedback loop, and 10 kΩ on the positive input. A positive DC voltage is applied to amplifier A and a negative DC voltage is applied to amplifier B.

In this circuit, all device components are operational which include the input, gain and output stages. This condition exercises all circuitry at DC and represents the worst case operating condition for the op amp.

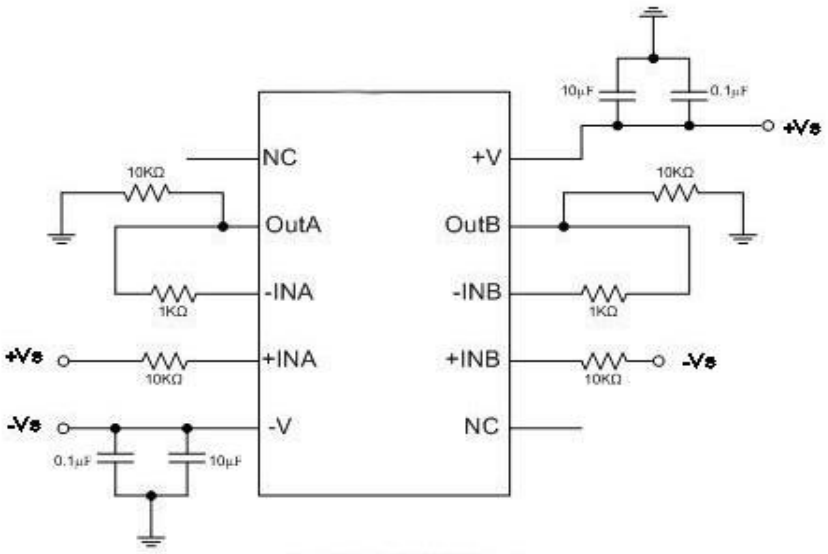

Figure 1 — Burn-In Schematic

Annex A (Informative) Example Burn-In Condition Evaluations (cont'd)

Case 4 – 4Mb SRAM Memory Microcircuit

- There are two methods of burn-in defined. For "Static" burn-in, all possible addresses are written with High data for half of the burn-in duration, and Low data for the remaining half. For "Dynamic" burn-in, all possible addresses are written with alternating High and Low data.
- All I/O pins specified in the burn-in pin lists are driven through individual series resistors. The burn-in voltages are defined as follows:

  VDD = maximum operating VDD [for a 3.3 V +/- 10% power supply, use VDD = 3.63 V; if dual power supplies, then for example 1.5 V +/- 5% (core) and 3.3 V +/- 10% (I/O), use V_1 = 1.575 V and V_2 = 3.63 V]

  V_{IL+}= 0.00 V to +0.40 V = LOW level for all programmed signals V_{IH} = +3.30 V to +3.63 V = HIGH level for all programmed signals

NOTE All device GND pins are to be tied to ground or 0 V.

Table 3 shows the dynamic burn-in pin listing. F = square wave, 100 kHz to 1.0 MHz

Table 3 — Dynamic Burn-In Pin Listing

Input	Signal	Input	Signal	Input	Signal	Input	Signal
A0	F/2	A6	F/128	A12	F/8192	A18	F/524288
A1	F/4	A7	F/256	A13	F/16384	$\overline{W}$	F/1048576
A2	F/8	A8	F/512	A14	F/32768	DQ0...7	F/2097152
A3	F/16	A9	F/1024	A15	F/65536	$\overline{S}$	F
A4	F/32	A10	F/2048	A16	F/131072	$\overline{G}$	V_{IL} or GND
A5	F/64	A11	F/4096	A17	F/262144	E	V_{IH}

Table 4 shows the static burn-in pin listing. F = square wave, 100 kHz to 1.0 MHz

Table 4 — Static Burn-In Pin Listing

Input	Signal	Input	Signal	Input	Signal	Input	Signal
A0	F/2	A6	F/128	A12	F/8192	A18	F/524288
A1	F/4	A7	F/256	A13	F/16384	$\overline{W}$	F/1048576
A2	F/8	A8	F/512	A14	F/32768	DQ0...7	V_{IL} 1st half V_{IH} 2nd half
A3	F/16	A9	F/1024	A15	F/65536	$\overline{S}$	F
A4	F/32	A10	F/2048	A16	F/131072	$\overline{G}$	V_{IL} or GND
A5	F/64	A11	F/4096	A17	F/262144	E	V_{IH}

Annex A (Informative) Example Burn-In Condition Evaluations (cont'd)

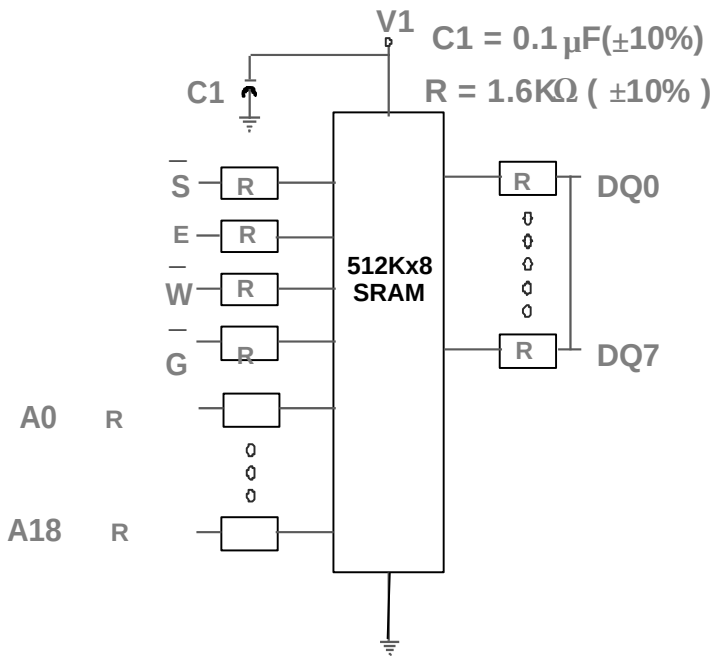

Figure 2 — SRAM Burn-In Example

Case 5 – Logic Circuit (Digital ASIC)

Product

- 0.25μm digital CMOS ASIC with ≈ 1,000,000 equivalent scan-enabled gates, using 3.3±0.3 V I/O and 2.5±0.25 V core. Die size is ≈ 11 mm per side, and draws ≈ 0.05 (μW/gate)/MHz) at maximum core voltage and 125°C case temperature.
- Part contains internal PLL for clock synchronization and 1 MB on chip SRAM for data buffering. PLL output accessible through test modes, with SRAM testable by Memory Built-In Self-Test (BIST).
- Part has 350 I/O pads (including CMOS and LVDS) and 100 power/ground pads.
- Package is 472-pin LGA with junction to case thermal resistance of 5°C/W.
- Technology has absolute maximum rated junction temperature defined to be 150°C.

Targeted Defects

- The primary targeted defects, for this process, are defects in the gate oxide.

Conditions

- Dynamic life test is the right scheme to use for this device type.

Annex A (Informative) Example Burn-In Condition Evaluations (cont'd)

- A high toggle coverage pattern would include scan for core and I/O logic followed by memory BIST, followed by an output toggling functional pattern run at >1 Mhz.
- PLL should be set to "free-run" mode and operated continually through burn-in.
- V_{DDcore} and V_{DDIO} should be set at maximum operating voltage.
- It is recommended that LVDS transmit and receive pins be tied in loopback through a 100 Ω resistor, and CMOS outputs be alternately tied to V_{DDIO} through a >1 kΩ resistor.
- Non-digital logic inputs should be driven alternately High and Low at a 2-MHz rate.
- It is recommended that inputs used in the pattern be driven to values ≈ 100 mV below V_{DDIO} and 100mV above V_{SS} to prevent current flow through ESD protection.
- Based on the values above, at a standard burn-in oven supplied frequency of 2 MHz, the part will draw ≈ 0.1 W, meaning that the junction temperature increase in burn-in is negligible, and there is no risk of exceeding the technology maximum junction temperature limit.
- In this case, it is acceptable to perform burn-in at 125°C oven temperature.

Annex B (Informative) Burn-In and Electrical Measurement Requirements

Table 5 — Burn-In and Electrical Measurement Requirements

IC Type	Required Burn-In 1/		Delta	Electrical Measurements 2/, 3/, 4/
	Static (Condition C)	**Dynamic (Condition D)**		
Digital Bipolar & Digital MOS/ BiCMOS: LOGIC (Gates, Buffers, Flip-Flops, Multiplexers, Registers and Counters, etc.) RAMs, FIFOs, Microprocessors/ DSPs Interface Peripherals FPGAs, PROMs, PLD/PLA **5/**	Not required for Digital Bipolar Technology. Required for Digital MOS Technology. T_A = 125°C Vin = VDD across one-half input pins and VSS across the remaining inputs. Vout = 0.5 VDD through RL	Required for both technologies. T_A = 125°C Vin = Square wave, 50% Duty Cycle to input pins and control pins. Frequency = 100 Hz to 1 Mhz. Vout = VCC/2 or VDD/2 through RL	ΔICC or ΔIDD	**DC:** VIC, VOH, VOL, ICC(IEE), IIL, IIH, IDD, IOZL, IOZH, IOS, QIDD **AC:** TPLH, TPHL, TTLH, TTHL, TPZH, TPHZ, TPLZ, TPZL, TA, TS, TH **Functional Tests:** a) For simple logic devices, verify truth table. b) For complex logic devices such as microprocessors, FPGAs, etc., functional testing includes fault coverage calculations required per MIL-STD-883, Method 5012. c) For PROMs, check fuse map; for RAMs, perform pattern sensitive tests such as March, Galpat, etc.
Linear MOS, Bipolar, and Bi-FET: Op-Amp, Instrument Amplifiers, S/H, and Comparator	T_A = 125°C Vout = Terminated to ground through RL	T_A = 125°C Vin= Square wave or sine wave F = 10Hz to 100 KHz, 50% duty cycle Vout = Terminated to ground through RL	ΔIIB ΔIIO ΔVIO	**DC:** ICC, IEE, IIO, VIO, VOPP, AV, CMRR, PSRR, VOS, IB, IOS **AC:** Slew rate
Linear MOS, Bipolar and JFET: Line Drivers and Receivers	T_A = 125°C Vin= VDD max across one-half input pins and VSS across the remaining inputs.	T_A = 125°C Vin = Square wave at a specified frequency and duty cycle Vout = VCC through RL	ΔICC ΔIIH	**DC:** VOH, VOL, ICC, IIL, IIH, IOS, IOFF, IOZ, IDDSB, IIN, IINH, IINL **AC:** TPLH, TPHL, TTLH, TTHL **Functional Test:** Verify truth table.
Linear MOS, Bi-FET, and Bipolar: Analog Switches and Multiplexers	T_A = 125°C Vin = VDD max across one-half of inputs and VSS across the other remaining inputs. Vout = ± VCC through RL	T_A = 125°C Vin = Square wave F = 100 KHz and 50% duty cycle Vout = ± VCC through RL	ΔICC ΔID(OFF) ΔIS(OFF) ΔR(ON)	**DC:** ICC, ID(ON), R(ON), ID(OFF), IS(ON), IS(OFF), RDSON, I+, I- **AC:** T(ON), T(OFF) break-before-make-time
Linear Bipolar: Voltage Regulators	T_A =125°C Vout = Terminated to ground through RL	Not required.	ΔISCD ΔVOUT	**DC:** ICC, VOUT, IOS, line/load regulation, AUX OUT, INPUT LEAKAGE, OUTPUT NOISE

Table 5 — Burn-In and Electrical Measurement Requirements (cont'd)

IC Type	Required Burn-In 1/		Delta	Electrical Measurements 2/, 3/, 4/
	Static (Condition C)	**Dynamic (Condition D)**		
Linear Bipolar: Pulse-width-modulator	Not required.	T_A = 125°C Vout= Terminated to ground through RL Rext, Cext connected if applicable.	ΔIIO ΔVREF	**DC:** VREF, IIB, IIO, IOS, VIO, VOL, VOH, AV, CMRR, PSRR,ICC **AC:** TR , TF, fOSC
Darlington Transistor Array	T_A = 125°C Vout = Supply through RL	Not required.	ΔICEX ΔhFE	**DC:** V CE(SAT) , VF, ICEX, IF **AC:** hFE, tPHL, tPLH
Linear CMOS: Timers	T_A = 125°C Vout = VCC through RL	Not required.	ΔICEX ΔVOH ΔVOL	**DC:** VTRIG, VTH, VR, VOL, VOH, VSAT, ICC, ITRIG, ITH, IR, ICEX **AC:** TTLH,
Linear MOS and Bipolar: Active Filters	Not required	T_A = 125°C Vin = Sine wave at frequency < fO V = Terminated to ground through R	ΔICC ΔVOS	**DC:** ICC, ISS, VOS **AC:** fO, Q, input frequency range.
Mixed Signal MOS, Bi-CMOS and Bipolar: Analog to Digital (A/D)	T_A = 125°C Vin = Max analog DC input Vout = VCC/2 through RL	T_A = 125°C Vin = Analog input to generate maximum digital codes. Vout = VCC/2 through RL	ΔICC ΔIEE ΔVIO	**DC:** VREF, VOH, VOL, VIO, ICC, IEE, IIL, IIH, IOZL, IOZH, IOS, zero error, gain error, linearity error.
Mixed Signal MOS, Bi-CMOS and Bipolar: Digital to Analog (D/A) Converters	T_A = 125°C Vin = VDD on one-half data inputs and VSS on remaining inputs. Vout = Terminated to ground through RL	T_A = 125°C Vin = Apply appropriate digital codes for all inputs and for control signals. Vout = Terminated to ground through RL.	ΔICC ΔIEE	**DC:** ICC, IEE, IIL, IIH, IOZL, IOZH, IOS, IDDQ, zero error, gain error, linearity error, PSRR **AC:** TC, TS, TH
Voltage Reference	T_A = 125°C Vout = Terminated to ground through RL	Not Required	ΔVOUT ΔICC	**DC:** VOUT, ICC

Table 5 — Burn-In and Electrical Measurement Requirements (cont'd)

NOTE 1 Static and dynamic burn-in shall be performed at maximum recommended operating supply voltage at T_A = 125°C. Biasing conditions including the value of RL shall be selected to assure that the junction temperature shall not exceed Tjmax specified for the device type. T_A = 125ºC minimum

NOTE 2 See MIL-HDBK-1331: Parameters to be controlled for the Specification of Microcircuits, for symbol definitions.

NOTE 3 These are typically recommended electrical parameters based on MIL specifications and SMDs. Since electrical parameters are device dependent, refer to detail specifications or manufacturing data sheets for actual DC and AC parametric test conditions and limits.

NOTE 4 For digital devices, all DC parameters, functional tests, and switching tests shall be tested at 25°C, at minimum operating temperature and at maximum operating temperature. For linear devices, all DC parameters shall be tested at 25°C, at minimum operating temperature and at maximum operating temperature. All AC and switching tests shall be performed at 25°C at minimum operating temperature and at maximum operating temperature. The burn- in patterns need to be verified as working over the burn-in temperature range.

NOTE 5 For one-time programmable devices (e.g., PROMs, PLDs/PLAs). It may be necessary to subject to dynamic burn-in with user application specific burn-in circuit. The post burn-in should include DC, AC, and functional tests for user's program verification.

Annex C (Informative) Burn-In Alternatives

This Annex lists several publications that present methodologies for alternatives to standard burn-in. Although there are advantages to using these enhanced techniques, it is important to have detailed knowledge of the component in order to fully implement these strategies. When using alternative conditions as defined in MIL-STD-883, TM 1005, the manufacturer is expected to provide justification to the Qualifying Activity. When methods are used to shorten or eliminate traditional burn-in, it is suggested that for space level devices that wafer lots still be subjected to Life Test to validate the effectiveness of alternate screens used in lieu of burn-in.

Sagar Suresh Sabade, *Integrated Circuit Outlier Identification by Multiple Parameter Correlation*, Date May 2004.

R. Kawahara, O. Nakayama and T. Kurasawa, *The Effectiveness of IDDQ and High Voltage Stress for Burn-in Elimination (CMOS production)*, Date Added to IEEE *Xplore*: 06 August 2002.

T. Barrette, V. Vhide, K. De, M. Stover and E. Sugasawara, *Evaluation of early failure screening methods [ASICs]*, Date Added to IEEE *Xplore*: 06 August 2002

Nik Sumikawa, Li-C. Wang and Magdy S. Abadir *An Experiment of Burn-In Time Reduction Based On Parametric Test Analysis*, Date Added to IEEE *Xplore*: 2012

Rabindra Roy, Kaushik Royt, and Abhijit Chatterje *Stress Testing: A Low Cost Alternative for Burn-in* , 1997.

M. Ooi, M.F. Zakaria, Z. Abu Kassim, S.N. Demidenko *Reducing Burn-in Time Through High-Voltage Stress Test and Weibull Statistical Analysis*, April 2006.

M. Quach , Tuan Pham ; T. Figal ; B. Kopitzke ; P. O'Neill, *Wafer-level defect-based testing using enhanced voltage stress and statistical test data evaluation*, Date Added to IEEE *Xplore*: 10 December 2002.

P. Maxwell , P. O'Neill ; R. Aitken ; R. Dudley ; N. Jaarsma ; M. Quach ; D. Wiseman, *Current ratios: a self-scaling technique for production I/sub-DDQ testing*, Date of Conference**:** 30-30 Sept. 1999.

R. Madge, M. Rehani, K. Cota ,W.R. Daasch, *Statistical post-processing at wafer sort-an alternative to burn-in and a manufacturable solution to test limit setting for sub-micron technologies*, Date Added to IEEE *Xplore***:** 07 August 2002.

Standard Improvement Form JEDEC JEP163A

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street, Suite 240 S
Arlington, VA 22201

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC