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Guidelines for Measuring the Threshold Voltage (V_T) of SiC MOSFETs

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GUIDELINES FOR MEASURING THE THRESHOLD VOLTAGE (V_T) OF SIC MOSFETS

Contents

Foreword

This document was drafted by JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use in the SiC power semiconductor and related power electronic industries, and provides guidelines for measuring the threshold voltage (V_T) of SiC power devices.

Introduction

Threshold voltage (V_T) is a key parameter in the evaluation of changes in the characteristics of physical stimulus such as voltage and/or temperature stress. Without accurately measuring threshold voltage, it is not possible to monitor how device characteristics are changed by the stress applied to a device. SiC/SiO_2 interface of Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is more complex than the Si/SiO_2 interface, which requires careful handling of traps in the device with regard to the change monitoring of characteristics.

The test methods provided in this document can be used as a guideline for measuring threshold voltage of SiC power device, focused on N-channel vertical structure MOSFET technologies. These three test methods may be applied for datasheet, process control, technology development, final tests and other usage.

GUIDELINES FOR MEASURING THE THRESHOLD VOLTAGE (V_T) OF SIC MOSFETS

(From JEDEC Board Ballot JCB-22-48, formulated under the cognizance of JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee.)

1 Scope

SiC MOSFETs have threshold voltage hysteresis, which must be carefully considered when evaluating the VT shift caused by stress tests such as bias-temperature instabilities (BTI) [1]. This publication describes the guidelines for VT measurement methods and conditioning prior to VT testing in SiC power MOSFETs to reduce or eliminate the effect of the aforementioned hysteresis.

The test methods can be applied to the following:

- N-channel SiC MOSFET (vertical structure)
- Wafer and package levels

2 Symbols and Definitions

The symbols and terms below apply to this measurement method:

SYMBOL	DEFINITION
DUT	**DEVICE UNDER TEST**
V_{DD}	**SUPPLY VOLTAGE**
V_{DS}	**DRAIN TO SOURCE VOLTAGE**
V_{GS}	**GATE TO SOURCE VOLTAGE**
VT	**THRESHOLD VOLTAGE OF DUT**
VT^{UP}	**THRESHOLD VOLTAGE OF DUT TAKEN BY UPWARD SWEEP**
VT^{DOWN}	**THRESHOLD VOLTAGE OF DUT TAKEN BY DOWNWARD SWEEP**
$VT_{(GDS)}$	**THRESHOLD VOLTAGE OF DUT MEASURED BY TEST CIRCUIT WHERE GATE AND DRAIN ARE SHORTED**
I_{DS}	**DRAIN-SOURCE CURRENT IN ON-STATE**
Ith	**THRESHOLD CURRENT**
t_con	**CONDITIONING TIME**
t_ VT	**VT MEASUREMENT TIME**
t_float	**TIME AFTER CONDITIONING BEFORE MAKING VT MEASUREMENT**

Note In JESD 77-B, the symbol for the threshold voltage for enhancement FET is defined as VGS(th). In this document, VT is used as a symbol instead of VGS(th).

3 Requirements

When performing threshold voltage (VT) measurement by “sweeping” the gate voltage with an upward staircase sweep followed by a downward staircase sweep, a shift of the transfer curve with hysteresis-type characteristics can be observed, as shown in Figure 1.

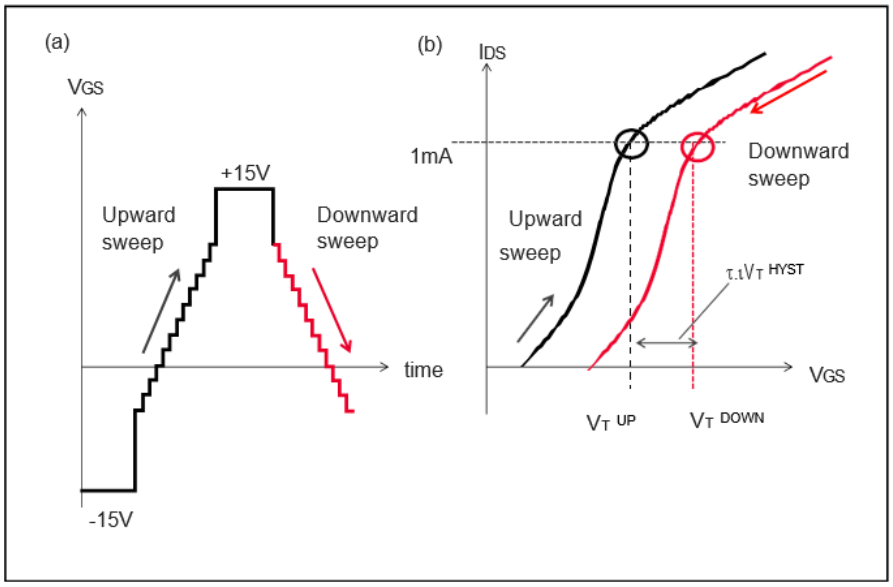

Figure 1 — V_T Hysteresis Observed by Upward and Downward Sweep Measurement

This phenomenon is caused by traps in the SiC MOSFET.

It is known that with a positive gate pulse smaller than or equal to VGS_MAX, the VT will virtually become flat over time, as shown in Figure 2. [1]

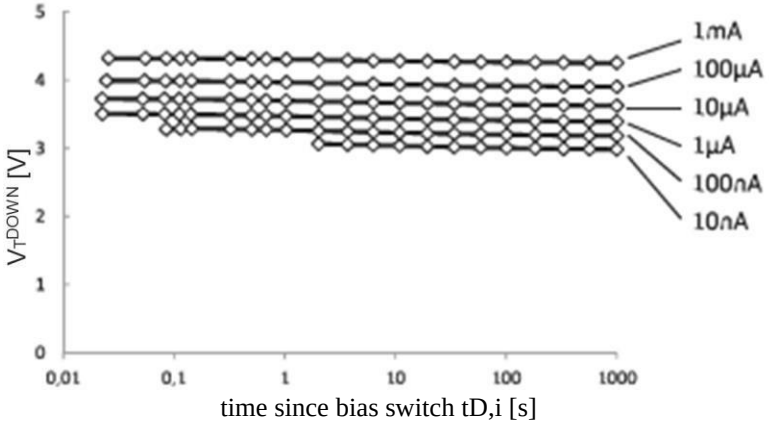

Figure 2 — V_T ^{DOWN} Extracted from a SiC MOSFET Device at Different Current Levels After Biasing the Device in Deep Inversion for 100 ms

3 Requirements (cont'd)

Using this mechanism, the conditioning of V_T can be performed by simply applying a positive gate pulse (i.e. a conditioning pulse) prior to measuring the V_T, as shown in Figure 3. This should also be done before the output characteristic is recorded or R_{ON} is measured

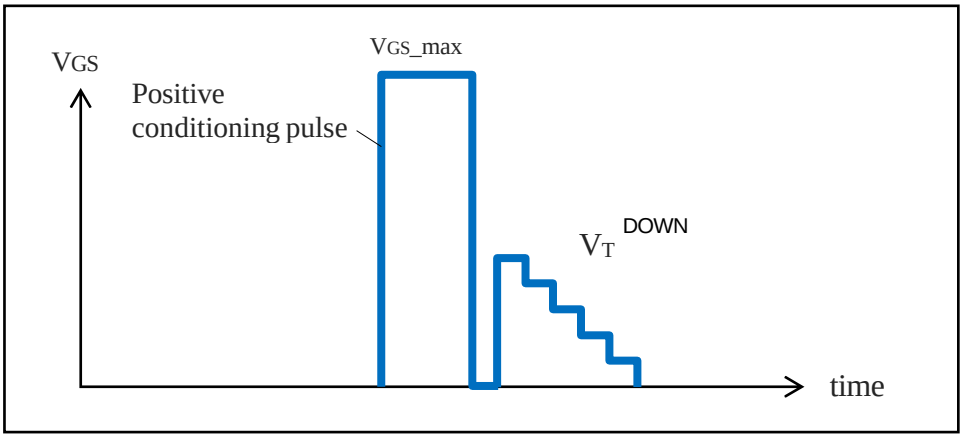

Figure 3 — Conditioning Before Threshold Voltage Measurement

4 Test Circuits

V_T is measured using a conventional test circuit with source measure unit (SMU) as shown in Figure 4.

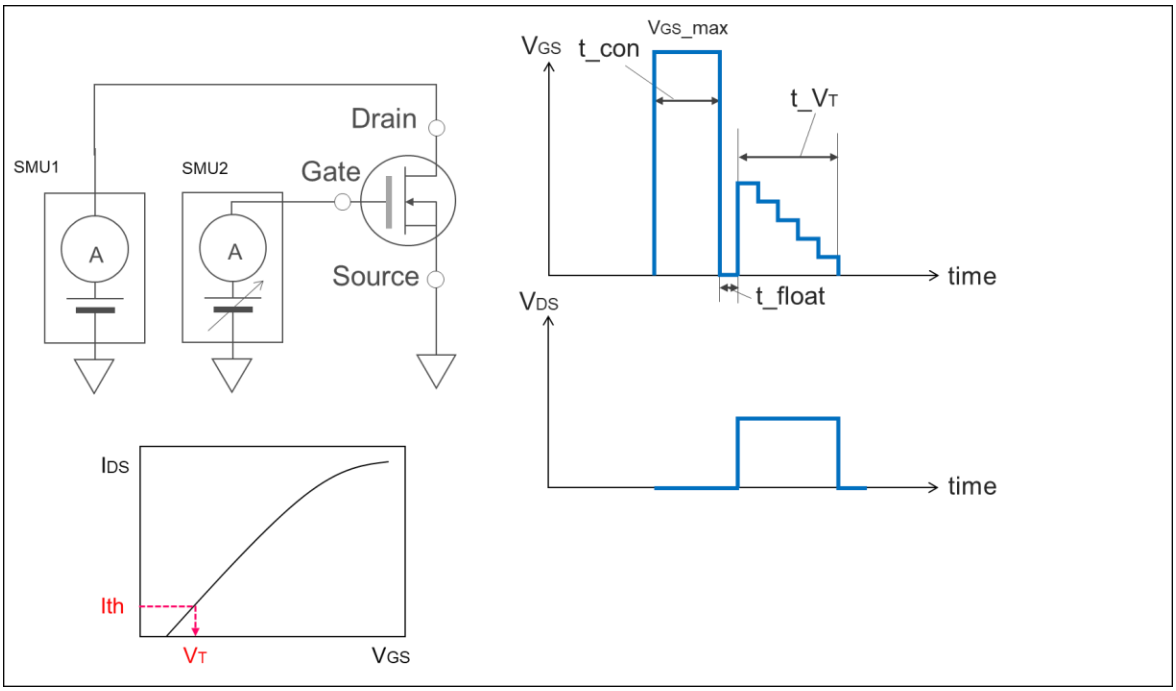

Figure 4 — V_T Test Circuit and Timing Diagram

4 Test Circuits (cont'd)

Drain-to-source current (I_{DS}) is measured while sweeping gate-to-source voltage (V_{GS}). The drain-to-source voltage (V_{DS}) is kept constant when measuring I_{DS}. A threshold current needs to be defined to measure VT. VT is the V_{GS} when the I_{DS} crosses the threshold current (Ith) during the V_{GS} sweep operation. It is important to define the time intervals for conditioning and V_T measurement.

Recommended time intervals are provided as follows:

- t_con: 1 to 100 ms
- t_float: < 10 ms
- t_ VT: < 10 ms x number of steps

It is important to have consistent time intervals across different measurements. t_float should be kept as short as possible to avoid unnecessary relaxation.

The optimal conditioning time for a given pulse amplitude can be evaluated by varying pulse width prior to V_T evaluation. It can be longer than 100ms, in particular, if conditioning voltages lower than max ratings are used.

The V_{GS} step voltage should be small (e.g. 0.1V) to make accurate VT extraction.

An alternative VT test circuit configuration is shown in Figure 5. The VT is the X-intercept of the interpolated line of the square root of I_{DS}. The square root of I_{DS} is proportional to V_{GS} as long as the DUT is measured in the saturation region (V_{GD} < VT). This circuit configuration is effective, since the DUT always stays in the saturation region when VT is positive.

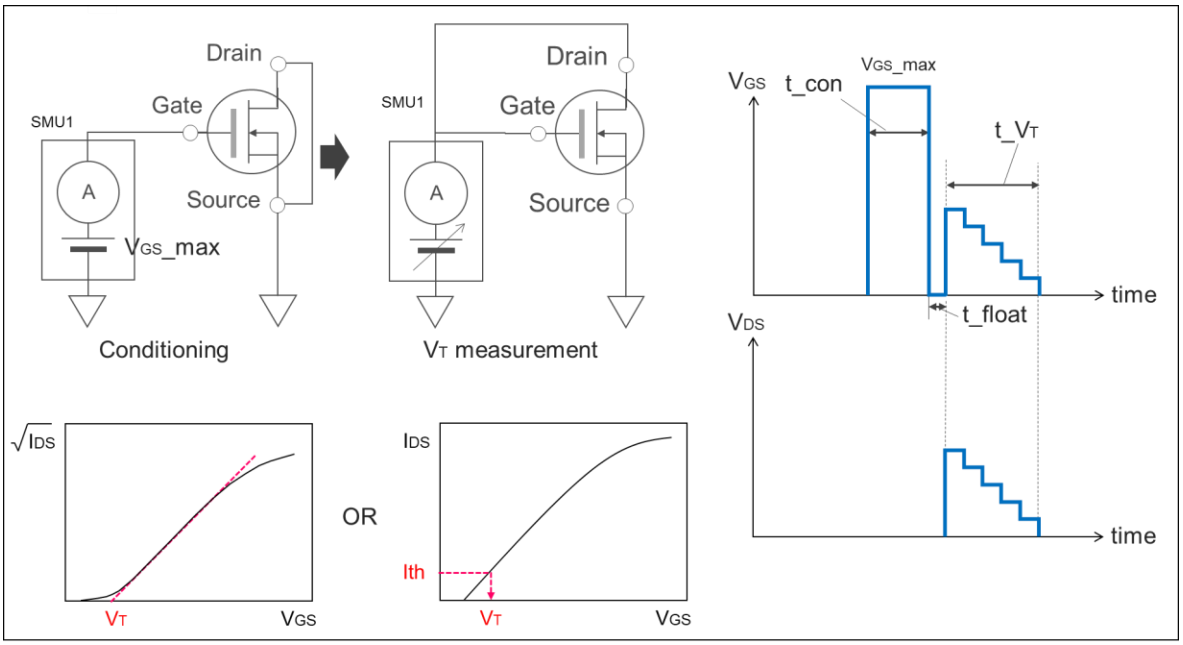

Figure 5 — Alternative VT Test Circuit and Timing Diagram

4 Test Circuits (cont'd)

The other V_T extraction method using the test circuit in Figure 5 is to simply take the V_{GS} value when the I_{DS} crosses the threshold current (Ith).

The alternative test method shown in Figure 6 is slightly different from Figure 5. It forces the target threshold current to the DUT where gate and drain are connected together. It allows one to determine the threshold voltage with a spot measurement.

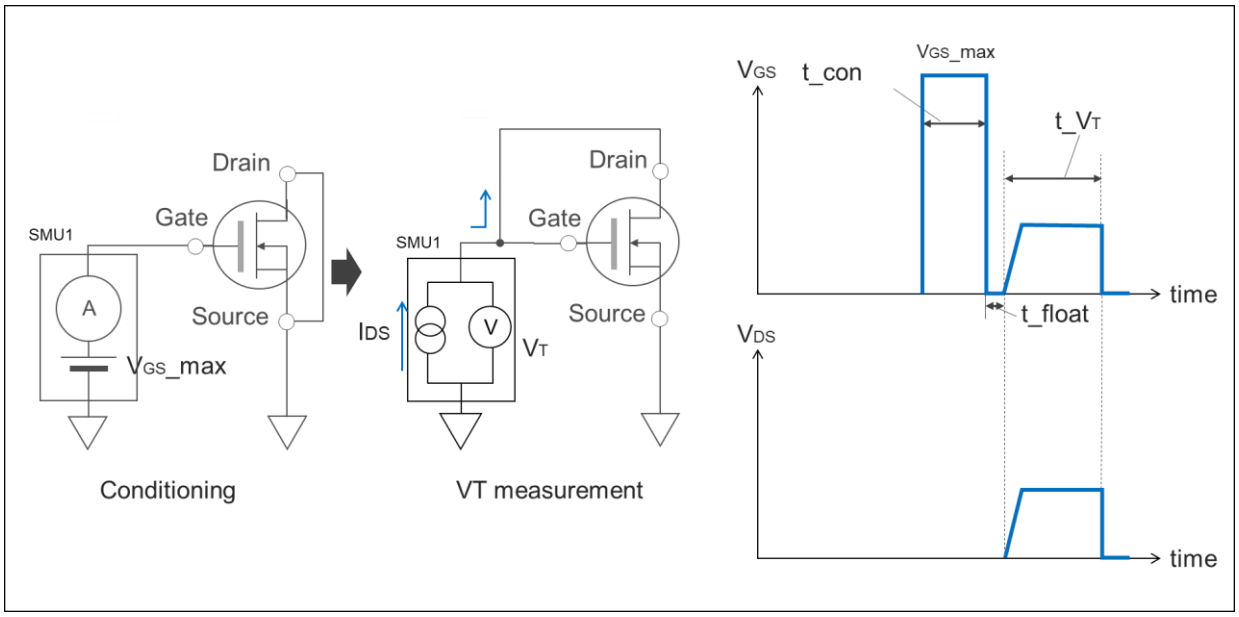

Figure 6 — Alternative Test Method

Recommended time intervals are provided as follows:

- t_con: 1 to 100 ms
- t_float: < 50 ms
- t_ VT: < 100 ms. Actual time dependent on the time needed for stabilization of the forced current.

It is important to have consistent time intervals across different measurements. t_float should be kept as short as possible to avoid unnecessary relaxation.

The optimal conditioning time for a given pulse amplitude can be evaluated by varying pulse width prior to V_T evaluation. It can be longer than 100ms, in particular, if conditioning voltages lower than max ratings are used.

The latter two VT measurement methods use a different test circuit from the first method. In other words, drain and gate are shorted for the latter two, while the first one has separated drain and gate. In order to distinguish the test circuit differences, the symbol for threshold voltage for the latter two has the subscript (GDS) as shown in Chapter 6. GDS stands for Gate Drain Shorted.

4.1 How to Define Conditioning

A common practice to determine a V_{GS} value for conditioning is simply to use the maximum rating of V_{GS} for 100ms. The maximum allowable gate voltage is a good value to ensure conditioning, but the pulse width should also be checked to determine whether it is effective enough for conditioning in order to prevent the hysteresis effect.

It is advisable to check the pulse width that provides a consistent V_T value by varying the V_{GS} pulse width prior to any reliability, on-resistance transition or other evaluation.

The pulse width should be consistent across the evaluation. It should be noted that the pulse width required to ensure conditioning will vary with device temperatures. For consistent V_T values, device temperature should not change significantly across the evaluation.

5 References

[1] T.Aichinger, Gerald Rescher, Gregor Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs, "Microelectronics Reliability 80 (2018) 68-78

Annex A (Informative) Differences Between Revisions

This annex briefly outlines the changes appearing in this publication, JEP183A, compared to its predecessor JEP183.

Clause	Description of Change
4	Updates to recommended time interval descriptions associated with the conventional test circuit and the alternative test circuit.

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☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

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