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Guidelines for Gate Charge (Q_G) Test Method for SiC MOSFET

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GUIDELINES FOR GATE CHARGE (Q_G) TEST METHOD FOR SIC MOSFET

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Foreword

This method describes how to measure and extract the gate charge of silicon-carbide insulated-gate-controlled power devices, such as silicon-carbide MOSFETs. The text focuses on enhancement-mode field effect transistors.

The gate charge Q_G is a key parameter when evaluating the device characteristics. Especially for switching and driver loss estimation, it is necessary to generate confident values of the total gate charge $Q_{G,TOT}$, gate-drain charge Q_{GD} and gate-source charge needed to reach the threshold voltage $Q_{GS,TH}$.

The purpose of this document is to make gate-charge measurement and extraction of defined portions of gate charge trustable by taking the specialties of silicon-carbide MOSFETs into account.

GUIDELINES FOR GATE CHARGE (Q_G) TEST METHOD FOR SIC MOSFET

(From JEDEC Board Ballot JCB-22-58, formulated under the cognizance of JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee.)

1 Scope

For SiC MOSFET, the gate-charge characteristic behaves different to conventional silicon power MOSFETs. The most distinct point is the absence of a real Miller plateau. Due to short n-channels, which are typically used in SiC MOSFETs, practically a Miller "ramp" is measured. The standard Q_G extraction methods [1] cannot be easily applied. Furthermore, the presence of a $V_{GS,TH}$ hysteresis [2] makes it necessary to define clearly the starting gate voltage for Q_G measurement and extraction. The following document defines a $Q_{GS,TOT}$, Q_{GD} and $Q_{GS,TH}$ which can be extracted from a measured Q_G waveform.

The test and extraction method can be applied to the following:

- N-Channel SiC MOSFET (vertical structure)
- Wafer and package levels

2 Introduction and Description

Figure 1 is an idealization of a recorded turn-on gate-charge waveform at a SiC MOSFET. As can be seen, a strong pronounced Miller-ramp phase is observed. The main reason is the before-mentioned short-channel effect [3] of SiC MOSFETs which lead to a change of the threshold voltage $V_{GS,TH}$ during the change of the drain-source voltage. For a reduction of the drain-source voltage, e.g., during turn-on, $V_{GS,TH}$ is effectively rising. For an increase of the drain-source voltage, e.g. during turn-off, $V_{GS,TH}$ is effectively reduced. Therefore, the gate voltage changes in the moment of drain-source voltage change and describes a "ramp" behavior, see Miller-ramp phase in Figure 1.

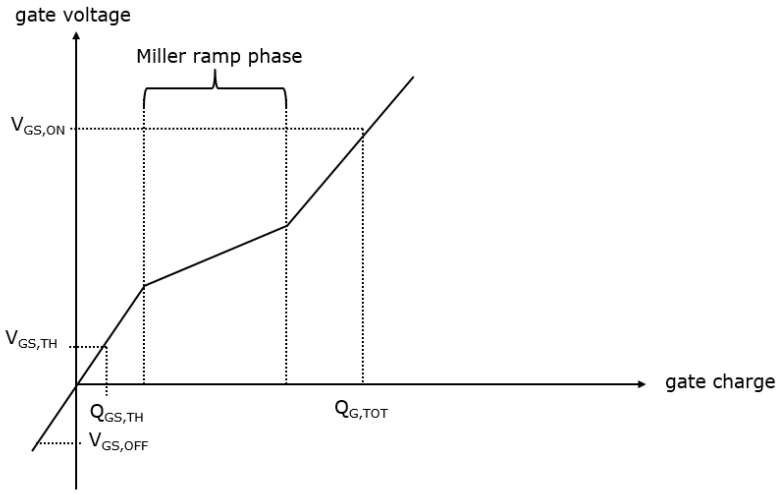


Figure 1 — Idealized Gate-Charge Waveform Measured at Turn-on of a SiC MOSFET

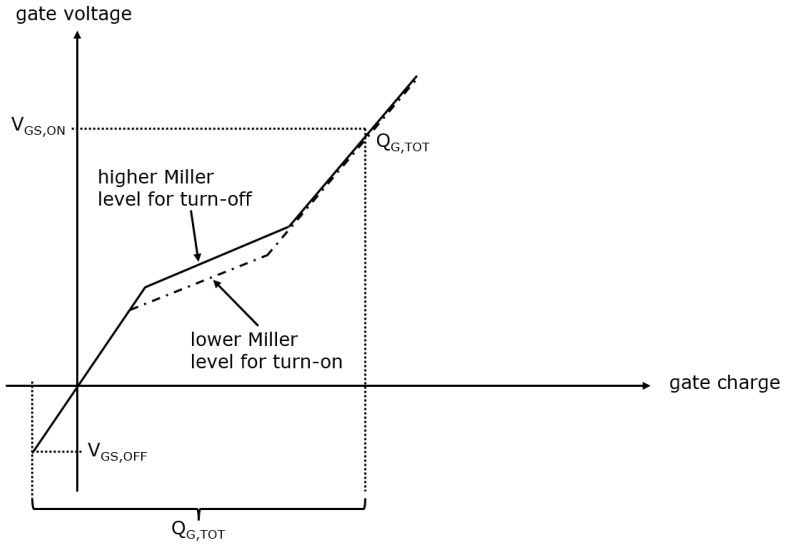


Figure 2 — Difference in Turn-on and Turn-off Q_G Measurement Due to $V_{GS,TH}$ Hysteresis [2]

2 Introduction and Description (cont'd)

Due to $V_{GS,TH}$ hysteresis of SiC MOSFETs [2] it is also necessary to define a starting voltage of Q_G measurement, e.g. the $V_{GS,OFF}$ level (recommended off gate voltage in the datasheet) or the decision, if the turn-on or turn-off event is used for extraction. The $V_{GS,TH}$ hysteresis will change the level of the Miller ramp and the value of $Q_{GS,TH}$., as shown in Figure 2. It is also recommended to define the Q_G measurement conditions afterwards very clearly in the datasheet with respect to temperature and switching conditions (drain current, drain voltage). As test current, the nominal current $I_{D,NOM}$ should be used. At the end, for measurement it is important, between which limits $Q_{G,TOT}$ is extracted. E.g., if it is between the recommended $V_{GS,OFF}$ and $V_{GS,ON}$ level, the test pulse should also start at $V_{GS,OFF}$, as shown in Figure 3.

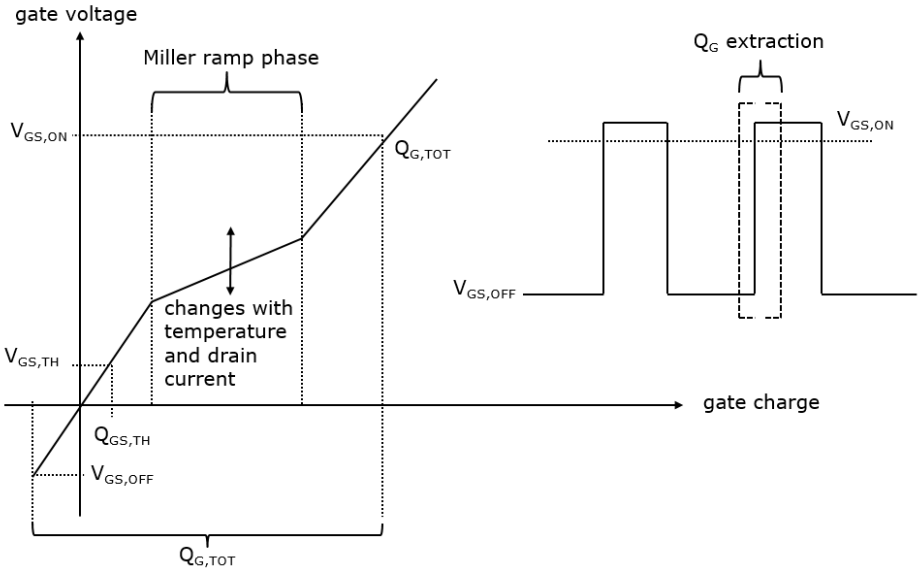


Figure 3 — Total Gate Charge Should be Extracted Between $V_{GS,OFF}$ and $V_{GS,ON}$. Gate Signal Should Start at $V_{GS,OFF}$.

Specific Q_G points in the gate voltage vs. gate charge plot are:

- $Q_{GS,TH}$: Charge needed, until $V_{GS,TH}$ is reached
- $Q_{G,TOT}$: Total gate charge between a specific interval, e.g. -5V (=$V_{GS,OFF}$) → 15V (=$V_{GS,ON}$)
- Q_{GD}: Charge which is cumulated during the drain-source voltage change; this charge defines the possible switching speed with respect to *dv/dt* and helps also to describe the parasitic turn-on effect

2 Introduction and Description (cont'd)

In the Q_{GD} period, V_{GS} is not allowed to rise (or change). Therefore, the Miller "ramp" is graphically transposed to a plateau, as shown in Figure 4. The third straight line (c) of the Q_G measurement is extended to lower values. Then, the kinking point between straight line (a) and (b) is horizontally connected to the extended line (c). The length of the auxiliary line (d) between the crossing points is reflected to the x-axis and Q_{GD} can be extracted. Starting with Q_{GD} from the kink between (a) and (b) takes most of the DIBL (short-channel effect [3]) into account which is especially present at high drain-source voltages at turn-on, see V_{DS} curve and output characteristic in Figure 4, right side. For lower drain-source voltage, the bended output characteristic is mostly described by the JFET effect of the shielding p-regions. The extracted value is also close to the mathematical expression of Q_{GD}, as shown in Equation 1.

$$Q_{\mathrm{GD}} = \int_{V_{\mathrm{DS,on}}}^{V_{\mathrm{DC}}} C_{GD}\,\mathrm{d}V \tag{1}$$

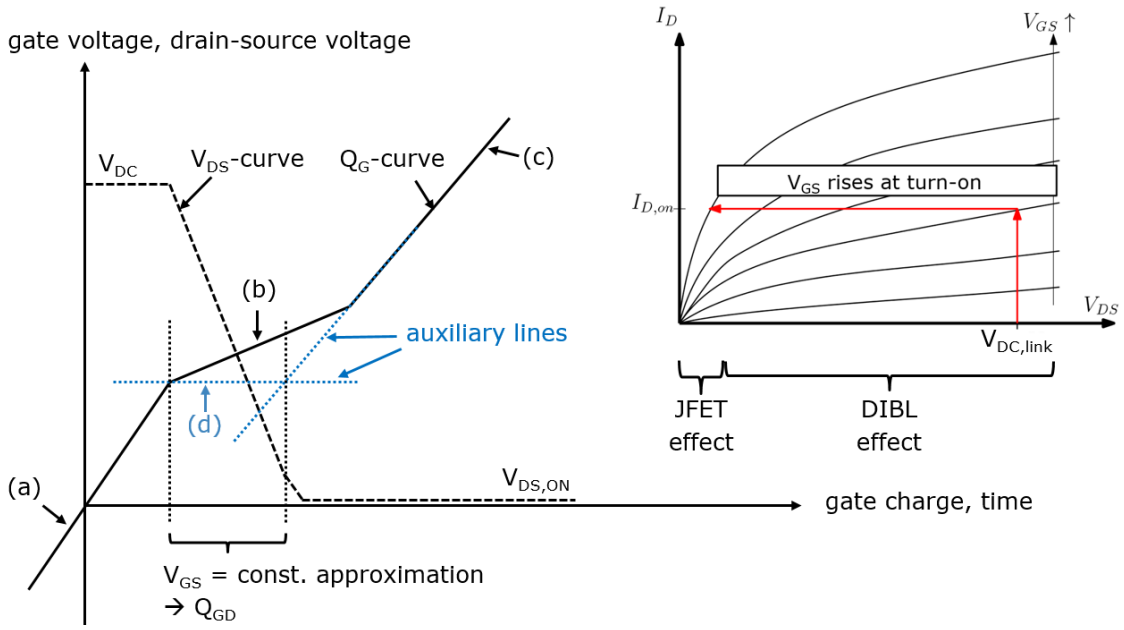
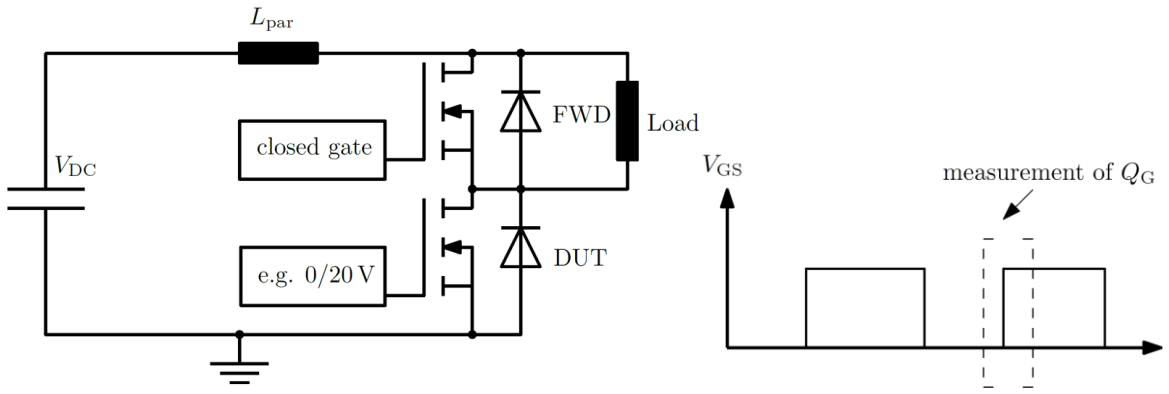


Figure 4 — Proposed Q_{GD} Extraction Method; with the Help of Auxiliary Lines a Constant V_{GS} Phase is Graphically Constructed and Thus Q_{GD} can be Extracted.

3 Test Circuit

Different methods can be used to measure the gate-charge curve. However, it is recommended to use the standard double-pulse measurement, which is also used for dynamic characterization of devices. This gives the most realistic behavior of the gate-charge characteristic. The gate charge may be measured during turn-on or during turn-off event. Typically, it is measured during the second turn-on event, as shown in Figure 5, right side. It has to be considered to place a free-wheeling diode (FWD) in parallel to the load. The signals of V_{DS}, I_{DS}, V_{GS} and I_G should be measured, with $Q_G = I_G \cdot t$. The free-wheeling diode should not have a too big stored charge Q_{RR} to not influence the gate-charge measurement too much. E.g., a SiC Schottky diode may be used, or for practical reasons the body diode of the respective SiC MOSFET that is characterized, as shown in schematic in Figure 5.

As discussed above, important parameters must be clearly defined ($V_{GS,OFF}$, $V_{GS,ON}$, $I_{D,NOM}$, temperature, typical DC-link voltage (V_{DC}) - for the used device voltage class, e.g. 800 V for 1200 V device class).



NOTE Typical Q_G is recorded during turn-on of the second pulse

Figure 5 — Double-Pulse Test Circuit and Test Sequence.

An alternative method is to use a curve tracer by performing two measurements, one with the target high drain voltage (V_{DC}) with low drain current and the other with the target high drain current with low drain voltage, as shown in Figure 6. Unlike the double pulse test, this method applies a single pulse to the DUT. The gate charge curve is measured during the turn-on event for each test. The complete gate-charge curve is made by combining two gate charge curves measured under the conditions.

3 Test Circuit (cont'd)

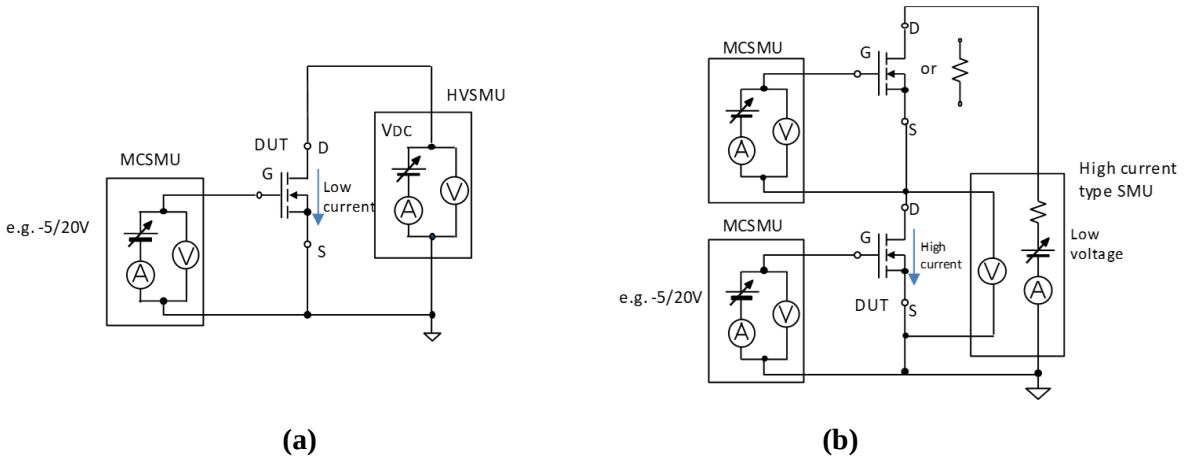


Figure 6 — Alternative Measurement Method for (a) High Voltage Part, (b) High Current Part

The following graph in Figure 7 shows an example of the combined gate charge curve. Curve (a) and curve (b) relate back to the test circuits in Figure 6. The yellow curve is the combined gate charge curve.

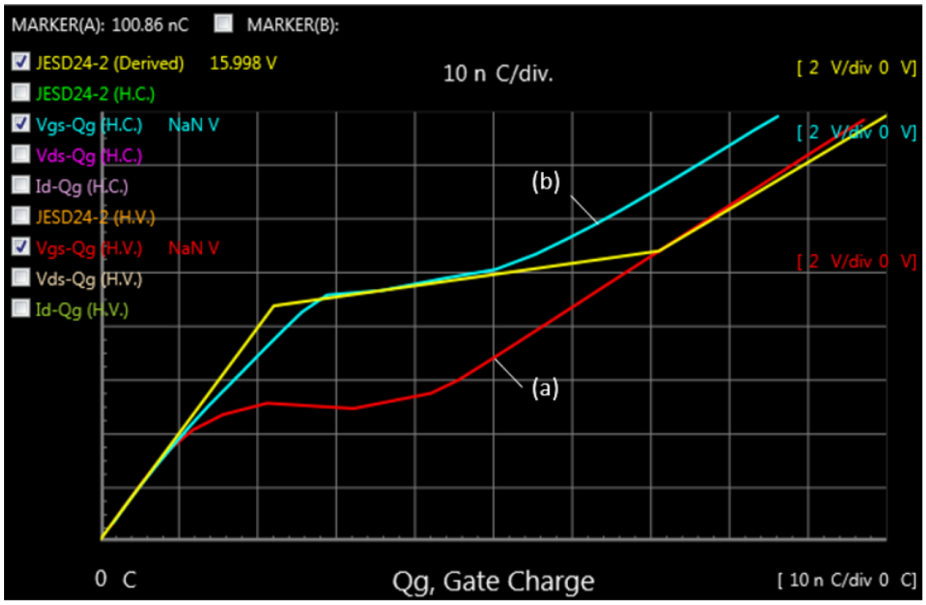


Figure 7 — Gate Charge Curve Measured by this Method

The first segment is drawn by taking the slope of curve (a) because the high voltage makes the input capacitance C_{iss} small when the DUT is off and the V_{DS} is high. The voltage level at the second segment (ramped plateau) is drawn by taking the curve (b) because the current determines this Miller voltage level. The onset of last segment is the cross point of extended ramped plateau and curve (a). The slope in this segment is the slope of curve (b) because the C_{ISS} is increased due to the drop of V_{DS} in this segment.

4 Symbols and Definitions

The symbols and terms below apply to this test method:

SYMBOL	DEFINITION
DUT	**DEVICE UNDER TEST**
V_{DD}, V_{DC}	**SUPPLY VOLTAGE**
V_{DS}	**DRAIN TO SOURCE VOLTAGE**
I_{DS}	**DRAIN CURRENT IN ON-STATE**
V_{GS}	**GATE TO SOURCE VOLTAGE**
I_G	**GATE CURRENT**
$V_{GS,TH}$	**THRESHOLD VOLTAGE**
Q_G	**GATE CHARGE**
$Q_{G,TOT}$	**TOTAL GATE CHARGE BETWEEN CERTAIN LIMITS**
Q_{GD}	**GATE CHARGE CUMULATED DURING MILLER PHASE**
$Q_{GS,TH}$	**GATE CHARGE NEEDED TO CHARGE V_{GS} ABOVE V_{TH}**
C_{ISS}	**INPUT CAPACITANCE**
$I_{D,NOM}$	**NOMINAL CURRENT**
$V_{GS,OFF}$	**NOMINAL OFF-GATE VOLTAGE**
$V_{GS,ON}$	**NOMINAL ON-GATE VOLTAGE**
FWD	**FREE-WHEELING DIODE**

5 References

[1] JEDEC: Gate Charge Test Method JESD24-2, October 2002

[2] T. Aichinger, Gerald Rescher, Gregor Pobegen, “Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs”, Microelectronics Reliability 80 (2018) 68-78

[3] T. Basler, D. Heer, D. Peters, T. Aichinger and R. Schoerner, "Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET," PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2018, pp. 1-7.

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