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Survey On Latch-Up Testing Practices and Recommendations for Improvements

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SURVEY ON LATCH-UP TESTING PRACTICES AND RECOMMENDATIONS FOR IMPROVEMENTS

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Introduction

This white paper reports on a survey that has been conducted to better understand how the latch-up standard JESD78 revision E (JESD78E) is interpreted and was used in the industry. It also lays a path for potential adaptations needed to accommodate its use in future technologies and applications. This executive summary provides a high-level overview of the key findings of the survey analysis and recommendations for future JESD78 improvements. It serves explicitly as an invitation to read further clauses of this report and analysis details.

NOTE At the time of the survey the standard JESD78E was in effect. After the close of the survey JESD78F was released. JESD78F is a largely rewritten version of JESD78E but the basic testing strategy of the test method is unchanged. While a few issues involved in this survey were addressed in JESD78F there is no reason to believe that the results of this survey would be substantially different if JESD78F were in force at the time of the survey. In this white paper, references to the "current", "present", or "existing" JEDEC standard are referring to JESD78E unless otherwise specified.

The survey was set-up to answer high level questions such as:

- How is the test standard interpreted and executed across the industry?
- Which real-life events does JESD78 intend to simulate? Do these occur in present day applications?
- The prescribed voltage compliance limits prevent any significant current injection for low voltage pins. Is that intended and/or desired?
- Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
- What changes should be made to the standard to better suit the reality of present day and future technologies and products?

The survey was divided into nine clauses, each addressing sub-topics like the ones listed above. More details on the structure of the survey are provided in Clause 4 of this report.

Clause 5 describes the analysis of the responses. An effort was made to address topics in the same sequence as the questions appeared in the survey. The analysis is meant to strictly report and summarize the information provided by the respondents and to find potential correlations between different topics. However, whenever the analysis team felt it was appropriate to offer a "possible interpretation", it was clearly indicated using a special box format with the disclaimer that other interpretations would be possible. The full survey and an overview of all responses are provided in Annex B and Annex C, respectively.

The conclusions and recommendations are provided in Clause 6. Some of the key results are summarized below. For a full understanding of the survey results, it is recommended to read the full report.

One of the most relevant questions is if JESD78 latch-up testing ensures robustness of products in the field. Related key findings are:

- JESD78 is considered useful and should not be removed.
- It is evident that passing JESD78 testing is insufficient to guarantee latch-up robustness in the field, as shown in Figure 1, and seems to be more related to the type of stress rather than the levels.
- Respondents see value in JESD78 testing for modeling real world stress events beyond the specified test conditions.

Introduction (cont'd)

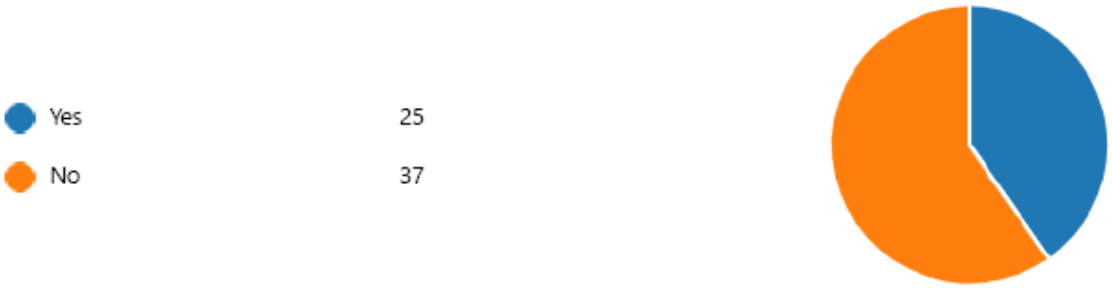

Figure 1 — Pie Chart of [Q41]

[Q41] "Does passing JESD78 testing guarantee latch-up robustness in the field?"

Another major topic is the assessment how large the latch-up problem is in practice. The figures below show at what step latch-up was detected (Figure 2), what the root causes were (Figure 3) and how often such cases lead to re-spins (Figure 4).

Examples of key findings related to this are:

- Figure 2 shows the majority of latch-up fails are reported during the JESD78 qualification test and many of these fails result in a re-spin, but this accounts for a very small fraction of the total number of re-spins as shown in Figure 4.
- More than 50% of all latch-up failures (field + JESD78 testing) do not require a re-spin, but the failure drives alternative mitigations such as board modifications or software changes

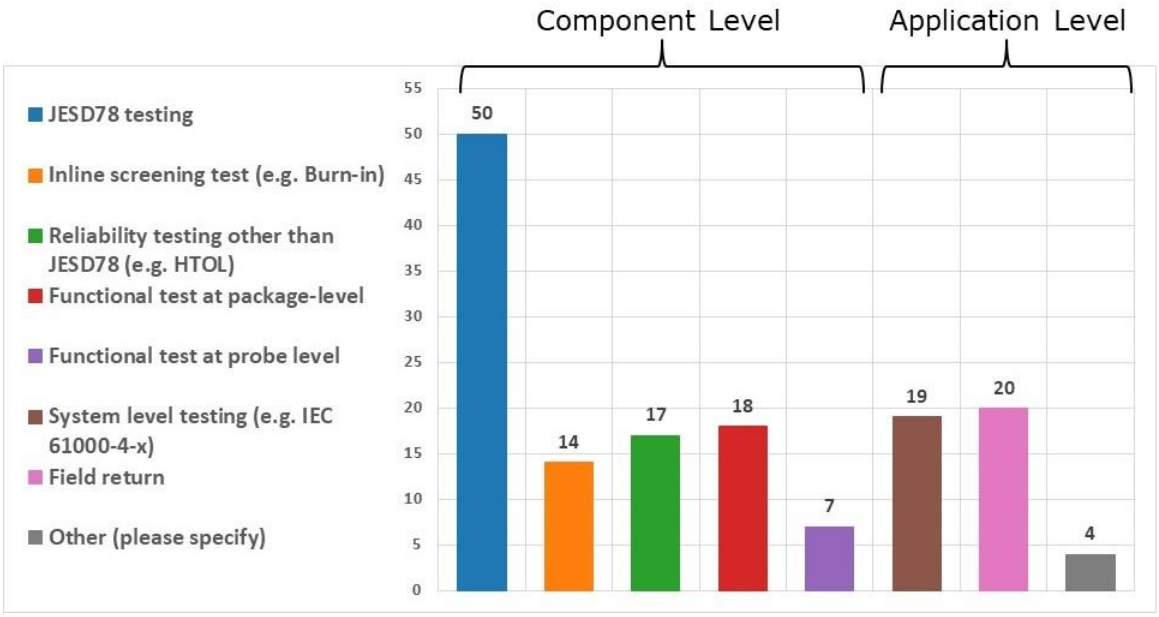

Figure 2 — Feedback to [Q12], in the Case Where [Q11], Was Answered "Yes"

[Q12] "Where have you experienced latch-up failures?"

[Q11] "Have you experienced latch-up failures?"

Introduction (cont'd)

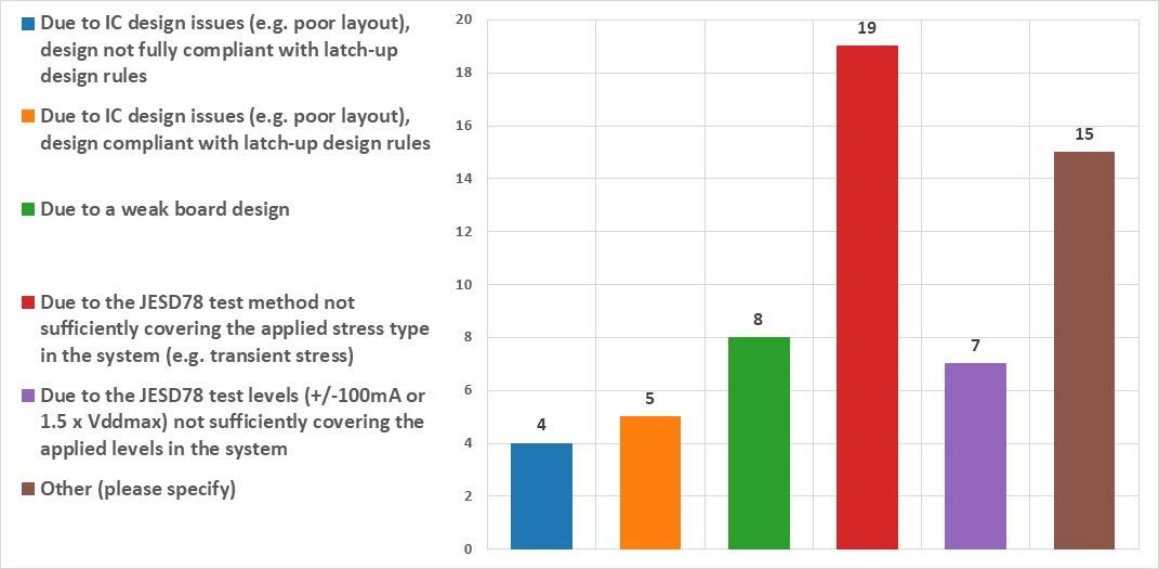

Figure 3 — Pareto of [Q20]

[Q20] "For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?"

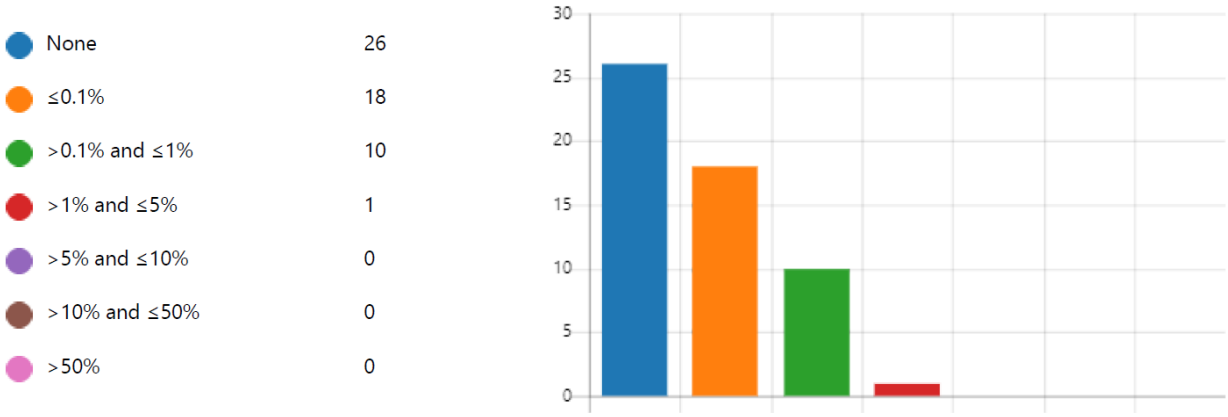

Figure 4 — Pareto of [Q21]

[Q21] "What percentage of your company's product re-spins were due to latch-up failures in a system application?"

The last highlighted topic is the question if the standard is sufficiently clear. It appears that some concepts in the standard are not interpreted in the same way by all users and sometimes are even used incorrectly. The most important examples are:

- The concept of the "Maximum Stress Voltage" is commonly used in the industry but very often misinterpreted or incorrectly applied to JESD78 testing.
- Many respondents believe that the pin stress voltage should not exceed the product AMR, see Figure 5.

Introduction (cont'd)

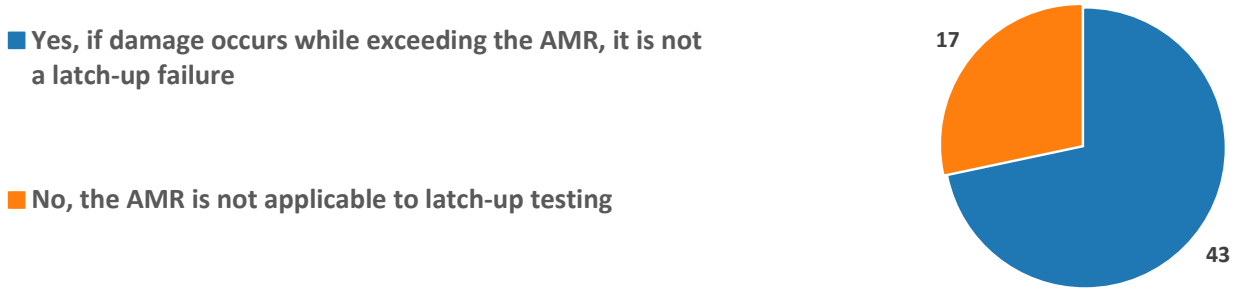

Figure 5 — Pie Chart of [Q90]

[Q90] "Do you set the pin stress voltage limits so that they do not exceed the product AMR?"

Key recommendations for possible improvements and extensions of JESD78E are listed below. Some of them may reach beyond the JESD78 specification – they may appeal to other industry bodies, symposia, trainers, vendors, etc. A more comprehensive list of recommendations is given in Clause 6.3.

- Create a JESD78 user guide with practical explanations, hints, and examples.
- Provide seminars and workshops aligned with the latest JESD78 revision F release, discussing the major changes from JESD78 revision E and implications to LU testing.
- Consider ways to standardize LU testing at the application level (System Level ESD, Transient LU).

Clause 6.4 concludes the white paper with a summary of the major differences between JESD78 revision E and JESD78 revision F.

SURVEY ON LATCH-UP TESTING PRACTICES AND RECOMMENDATIONS FOR IMPROVEMENTS

(From JEDEC Board Ballot JCB-22-57, formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This white paper presents the results of a latch-up survey on JEDEC JESD78E conducted by the Industry Council on ESD Target Levels. Results of the survey are presented with interpretation of the results along with recommendations for future revisions of JEDEC JESD78. In this white paper, references to the "current", "present", or "existing" JEDEC standard are referring to JESD78E unless otherwise specified.

2 References

[1] https://www.esdindustrycouncil.org/ic/en/documents

[2] B. L. Gregory and B. D. Shafer, "Latch-Up in CMOS Integrated Circuits", IEEE Transactions on Nuclear Science, Volume: 20, Issue: 6, pp 293-299, 1973

[3] R. R. Troutman, "Latch-up in CMOS Technology", Springer-Verlag, 1986 (2nd edition in 2012)

[4] https://www.jedec.org/document_search?search_api_views_fulltext=jesd78

[5] J. Salcedo-Suner et al., 'A new I/O signal latch-up phenomenon in voltage tolerant ESD protection circuits', Proceedings of the International Reliability Physics Symposium Proceedings, 2003, pp. and Jorge Salcedo-Suner et al., "Latch-up in voltage tolerant circuits: a new phenomenon", Microelectronics Reliability, vol. 44, pp. 549, 2004

[6] https://www.surveymonkey.com/

3 Terms and Definitions

AEC	Automotive Electronics Council
ATE	automated test equipment
CDE	cable discharge event
CDM	charged device model
CMOS	complementary metal-oxide semiconductor
C_{FOM}	correlation figure of merit
DPI	direct pin injection
DUT	device under test
EDA	electronic design automation
EIPD	electrically induced physical damage
EIAJ	Electronic Industries Association of Japan
EFT	electrical fast transient
EOS	electrical overstress
ESD	electrostatic discharge
ESDA	Electrostatic Discharge Association; ESD Association; EOS/ESD Association, Inc.
GND	negative voltage supply in digital logic, neutral voltage supply in analog logic
GPIO	general purpose I/O
HBM	human body model
HDMI	high-definition multimedia interface
HTOL	high temperature operating life
IC	integrated circuit
I_{DD}	positive supply current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
I/O	input/output
IP	intellectual property
ISO	International Organization for Standards
JEDEC	JEDEC Solid State Technology Association
JEITA	Japan Electronics and Information Technology Industries Association
LDO	low-dropout
LU	latch-up
LV	low voltage
NPN	negative-positive-negative (transistor)
OEM	original equipment manufacturer
PCB	printed circuit board
PNP	positive-negative-positive (transistor)
PNPN	positive-negative-positive-negative (thyristor)
QBS	qualification by similarity
RF	radio frequency
SoC	system on a chip
SEL	single event latch-up
TLP	transmission line pulse
TLU	transient latch-up
USB	universal serial bus
V_{CC}, V_{EE}	voltage applied to the collector and emitter, respectively (bipolar BJT)
V_{DD}, V_{SS}	positive voltage supply and negative (or GND) voltage supply, respectively (MOSFET)

3 Terms and Definitions (cont'd)

absolute maximum rating (AMR): The maximum limit for either the voltage across, the current through, or the power dissipated in a device which causes immediate damage or malfunction, or latent damage resulting in an unpredictable reduction of its lifetime.

maximum operating voltage (MOV): The maximum voltage allowed during normal operation of the device which still meets all data sheet specifications, typically including the DC/AC tolerance of the power supply.

maximum stress voltage (MSV): The maximum voltage (duration dependent) allowed to be placed on a given pin *during latch-up immunity testing* without causing irreversible damage to the device from a permanent physical breakdown of the silicon device or circuit not related to latch-up.

NOTE 1 A positive MSV is higher than the maximum operating voltage and a negative MSV is lower than the minimum operating voltage.

NOTE 2 MSV is NOT the same as the absolute maximum voltage rating (AMR) from the device datasheet. MSV applies to latch-up testing only, protecting the DUT from physical damage from stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in non-latch-up induced catastrophic breakdown of the silicon device/circuit.

NOTE 3 MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. In many medium and high voltage designs, MSV is very rarely the same value as AMR.

NOTE 4 The MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should consider the pulse width as well as process technology and circuit topology.

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4 Latch-Up Characterization

4.1 Short Introduction to Latch-Up and Standards Timeline

After publishing white papers [1] on target levels for human body model (HBM), charged device model (CDM), system level electrostatic discharge (ESD), and the elimination of MM testing, the Industry Council on ESD Target Levels recognized the effectiveness of this organization for addressing fundamental reliability issues facing the electronics industry. This led to the publication of a white paper on Electrical Overstress (EOS) which has brought increased clarity to the understanding of EOS and the need for cooperation between suppliers and users of integrated circuits for understanding the causes and solutions to EOS issues. In light of these successes, the Council has addressed the issue of latch-up and latch-up testing by performing a survey of industry experience with latch-up and latch-up testing. This white paper is a report on the finding of that survey.

Latch-up, which is the triggering of a parasitic low-ohmic path between power supply rails that can either damage the integrated circuit (IC) or make the IC inoperable, has been described since the late 1960s [2]. Latch-up became a reliability concern in the mid-80s [3], leading to the first standard document JESD17. The first practical industry IC latch-up testing method with injection current requirement, JESD78, was published in the mid-90s by JEDEC and has been revised five times by the JESD78 Working Group (see Figure 6) [4]. Subsequent revisions brought improvements, clarifications, and different trigger conditions, as illustrated in Figure 6.

At the time this survey was conducted, latch-up standard JESD78E was in effect and used for most latch-up testing. However, JESD78F was in the ballot process at that time. JESD78F was approved and issued in early 2022. JESD78F is a substantial rewrite of JESD78E intended to make the standard easier to understand and deal with the challenges of applying latch-up testing to a wide variety of integrated circuits functioning over a wide range of voltages. It is important to understand however that the basic latch-up testing requirements in JESD78F are fundamentally the same as in JESD78E. In this white paper, references to the “current”, “present”, or “existing” JEDEC standard are referring to JESD78E unless otherwise specified.

4.1 Short Introduction to Latch-Up and Standards Timeline (cont'd)

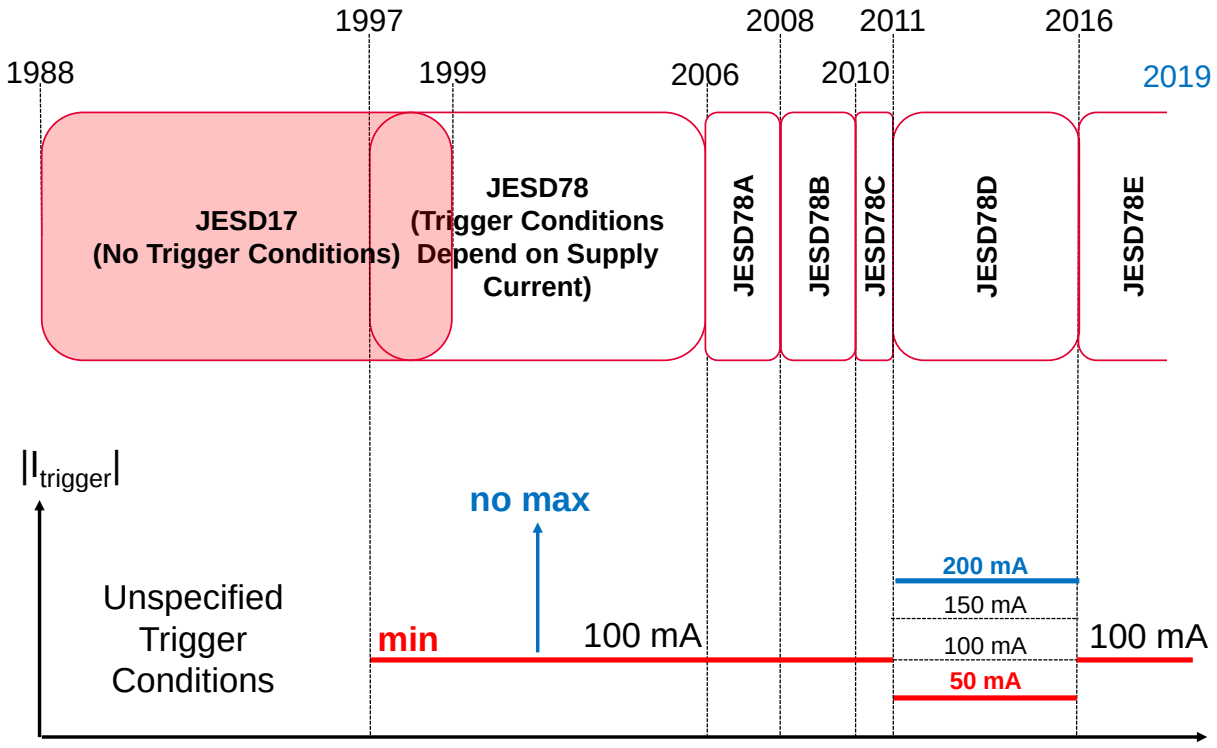


Figure 6 — Latch-up Testing Method Revisions and Associated Current Injection Requirements

The I/O test method essentially tests latch-up robustness by trying to inject a ±100 mA current with a clamping voltage applied to the pin. This will lead to substrate currents that may, for example, trigger a parasitic thyristor in an I/O or an internal buffer, as illustrated in Figure 7.

For various reasons, including technology scaling, increasing amounts of integration, and the complexity and variety of semiconductor components, the standard has faced challenges addressing the needs of the increasingly diverse semiconductor product space. Some of those challenges include:

- It is unclear how this test method correlates to real threats.
- Lack of data to show that the same standard applies under all applications.
- Challenge of testing a wide range of integrated circuit working voltages.
  - In many low-voltage I/O cases, the current injected in the I/O is very limited.
  - Avoiding overstress for high voltage devices.
- Many technicalities can disqualify a result. Examples are the active state of the device under test (DUT), the definition of special pins and power supply instability.
- There is confusion about the method and its results. Examples are the required temperature setting, the definition of low-dropout (LDO) pins, and the use of the maximum stress voltage (MSV).

4.1 Short Introduction to Latch-Up and Standards Timeline (cont'd)

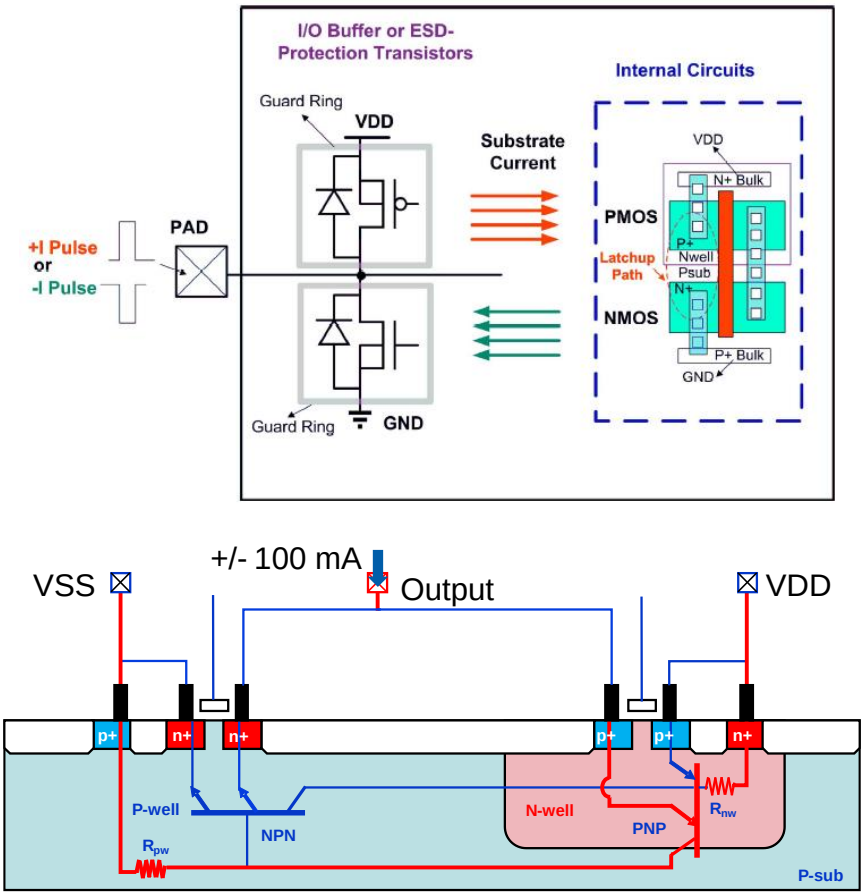


Figure 7 — Example of I/O Test with Cross-Section of Parasitic Thyristor in CMOS Buffer

4.2 Survey Report Organization

These challenges have prompted the industry Council on ESD Target Levels to re-evaluate the existing latch-up standard, JESD78E, in today's context. Throughout this document definitions of terms like e.g., injection current and MSV, are used as described in JESD78E. To understand more on how the industry is dealing with the topic and to get more information on how the industry uses latch-up testing results and to understand what industry expects from latch-up testing, the Industry Council on ESD Targets has set up a concise, yet detailed survey. A full version of the survey is available in Annex B.

4.2 Survey Report Organization (cont'd)

Some of the major questions that this survey is trying to answer include:

- How is the test standard interpreted and executed across the industry?
- Which real-life events does JESD78 intend to simulate? Do these occur in present-day applications?
- Why does the test specify ±100 mA for I/O assessments? Are the recommended qualification levels appropriate? Does a uniform specification make sense?
- The prescribed voltage compliance limits prevent any significant current injection for low voltage pins. Is that intended and/or desired?
- The formal latch-up definition describes parasitic thyristors. Should latch-up testing only be concerned about that? What about latch-up of other structures under the same conditions?
- Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
- What changes should be made to the standard to better suit the reality of present day and future technologies and products?

The survey was created by a sub-team of the Industry Council on ESD Targets and made available online for anonymous responses. The survey was announced via publicity channels of the Industry Council on ESD Targets, ESDA, JEDEC, JEITA, and an article in In Compliance Magazine.

The goal of this survey is to provide clarification on the test execution and use of the testing results and to derive recommendations, based on the data collected from a wide audience, for future directions of the JESD78 standard and potentially other standards. The data analysis and the recommendations are presented in this report. The response summary is available in Annex C.

For better readability, Clause 5 ("Detailed Analysis of the Survey") is split into different parts. We do this by following the same order of individual clauses as used in the survey, which is:

1. Affiliation and Background
2. Case Studies and Field Returns
3. Goal and Testing Strategy
4. Next Steps of Latch-up Testing
5. Reporting and Design Rules
6. Test Execution Details
7. Maximum Stress Voltage
8. Failure Criteria
9. Conclusion

In some cases, the feedback and result of a question are given descriptively ("high-level"). But in some other cases, we bring the analysis one level further as one important aspect of this survey analysis was finding meaningful correlations between answers to certain questions. This approach is described in detail in Annex A Clause A.2 and is used throughout this document. The method provides the possibility to make statements like:

- Respondents who answered "<answer text x>" to [Qxx] were more likely to answer "<answer text y>" to [Qyy] (<Nx> % versus <Ny> % baseline).
- Respondents who answered "<answer text x>" to [Qxx] were more likely to agree/disagree with the following statement, "<statement derived from [Qyy]>" (<Nx> % versus <Ny> % baseline).

4.2 Survey Report Organization (cont'd)

Through such correlations, it is possible to check the data for consistency, but also work out information that is not obvious at first glance and identify relevant coherences and implications. This helps enormously to better understand how users interpret, apply, and use JESD78 testing.

NOTE Whenever we refer to a specific question in this document, we use the term [Q?]. Here, "?" represents the number of the question according to its listing in the survey (e.g.: [Q11] relates to question "11" in the survey, which is "Have you experienced latch-up failures?")

Clause 6 then summarizes the findings and provides recommendations for future work.

5 Detailed Analysis of the Survey

5.1 Affiliation and Background

This part of the analysis deals with the responses to [Q01] through [Q08] of the survey, which are:

- [Q01] Which company do you represent?
- [Q02] In which country are you working?
- [Q03] Which market segments does your company serve?
- [Q04] What type of business is your company?
- [Q05] Which IC product types do you support?
- [Q06] How many latch-up related customer complaints does your company receive per year (approximate number)?
- [Q07] Are you filling out the survey for the whole company or just a part of it?
- [Q08] Which aspects of the JESD78 test standard are you familiar with?

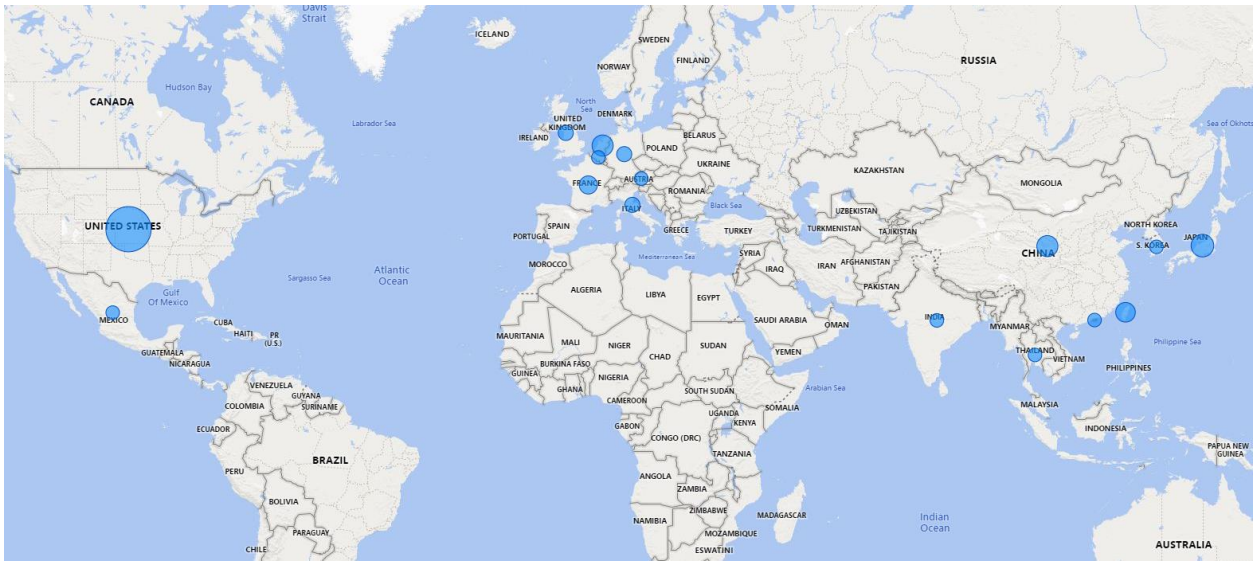
5.1.1 Demographics and Response Numbers

This clause describes important aspects of the responses to the survey, such as the number of responses, the distribution over different fields of the industry, the geographical distribution, etc. This serves to get an impression of how well the responders represent the industry.

The Industry Council on ESD Targets received 70 individual responses, from at least 35 companies from more than 16 countries. As we explain in detail in Annex A Clause A.1 (Statistical Meaning), the number of 70 responses let us claim the data of the survey has statistical relevance and is meaningful to derive conclusions and recommendations for the future of latch-up testing in the industry.

The distribution around the globe and different regions is illustrated by Figure8 and Figure 9. Multiple responses per company were encouraged because of the wide diversity of products, customers, and requirements. This makes it likely that even within one company, different approaches to latch-up testing may be used. Figure 10 shows that most responses received are representing relatively large groups or whole companies, while about 20% of the responses are on an individual basis.

5.1.1 Demographics and Response Numbers (cont'd)



NOTE The size of the balls is an indication of the number of responses from a country.

Figure 8 — Global Distribution of Responses

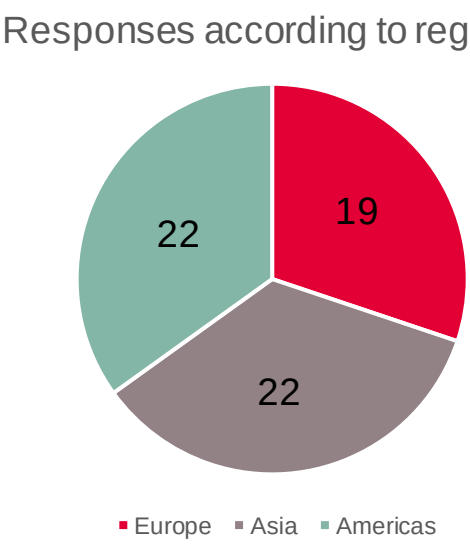


Figure 9 — Pie Chart of Responses Assigned to Different Regions

5.1.1 Demographics and Response Numbers (cont'd)

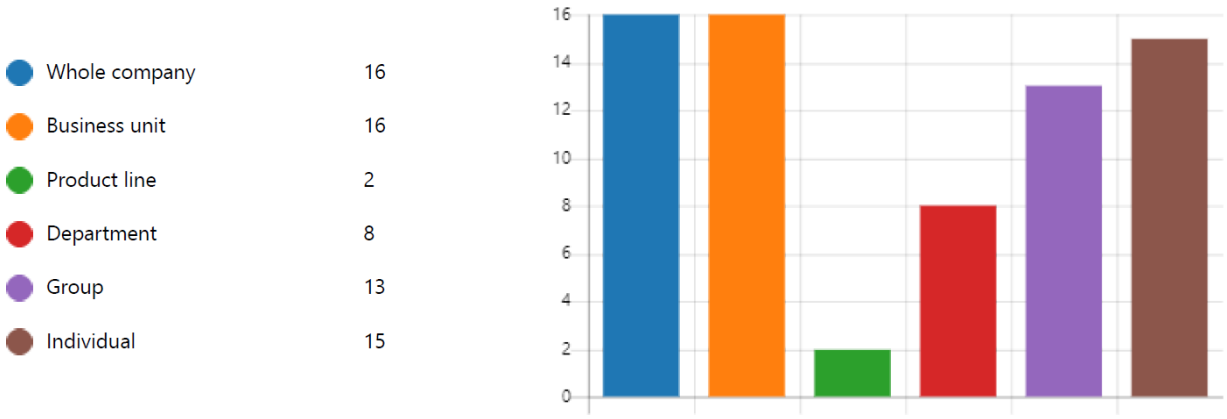


Figure 10 — Pareto of Group Representation per Response Received [Q07]

[Q07] "Are you filling out the survey for the whole company or just a part of it?"

5.1.2 Distribution Over Type of Market Space/Business/Application

Figure 11 and Figure 12 show the distribution of the responses over the type of business and type of IC respectively. The highest number of responses are from the category "IC Supplier with Fab". Although the responses were obviously not evenly distributed, Figure 13 illustrates that the overall industry is well covered. The exceptions are OEMs using analog and respondents from the "Tier/subsystem" category using very low voltage ICs.

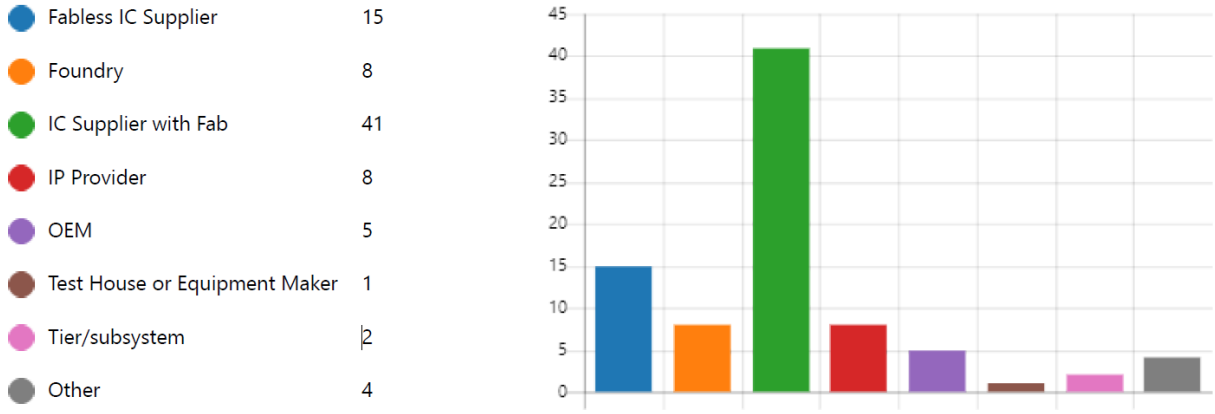


Figure 11 — Pareto of Responses Across Business Type [Q04]

[Q04] "What type of business is your company?"

5.1.2 Distribution Over Type of Market Space/Business/Application (cont'd)

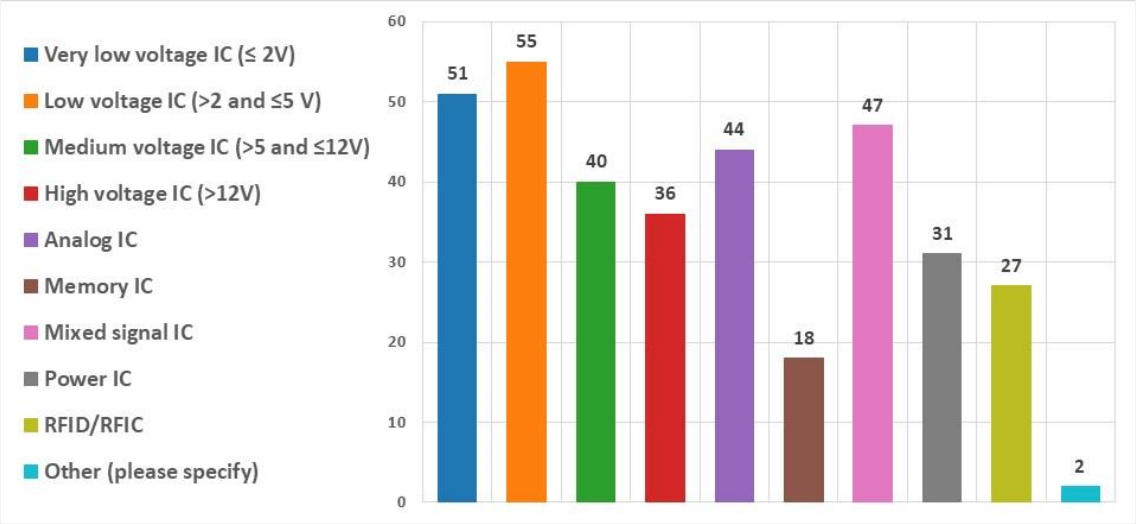


Figure 12 — Pareto of Responses Across Product Type [Q05]

[Q05] "Which IC product types do you support?"

	Very low voltage IC (≤ 2V)	Low voltage IC (>2 and ≤5 V)	Medium voltage IC (>5 and ≤12V)	High voltage IC (>12V)	Analog IC	Memory IC	Mixed signal IC	Power IC	RFID/RFIC	Other (please specify)
Fabless IC Supplier										
Foundry										
IC Supplier with Fab										
IP Provider										
OEM										
Test House or Equipment Maker										
Tier/Subsystem										

NOTE A green filled cell indicates that this combination of the type of business and IC product type is covered by at least one response in the survey.

Figure 13 — Combination of Responses from [Q04] and [Q05].

5.1.2 Distribution Over Type of Market Space/Business/Application (cont'd)

Finally, Figure 14 shows that the respondents are primarily active in the Automotive, Consumer, and Industrial market segments. The other market segments combined make a comparable contribution to the responses. In Clause 5.2, selected questions will be analyzed for possible correlations with business type or market segments.

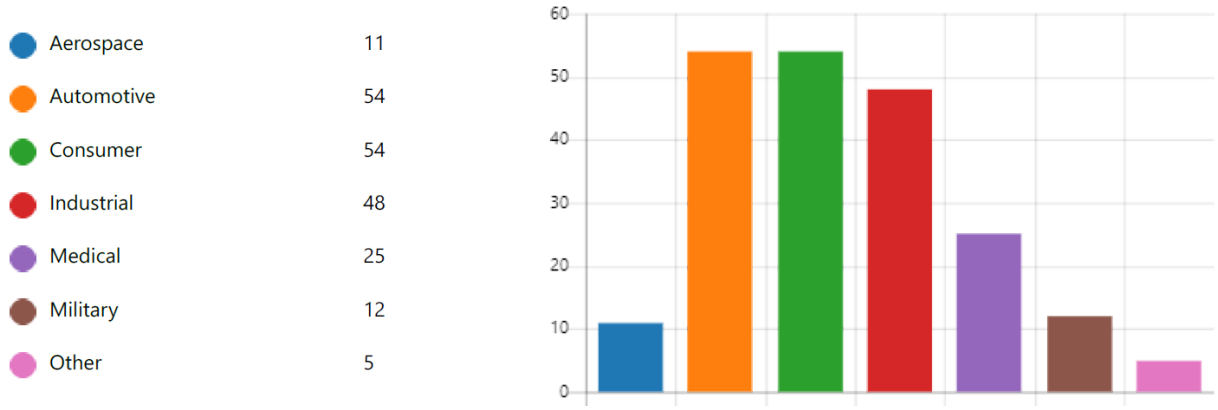


Figure 14 — Pareto of Responses Across Market Segments [Q03]

[Q03] "Which market segments does your company serve?"

5.1.3 Familiarity of the Industry Community Concerning the Different Aspects of Latch-Up Testing According to JESD78

To assess the significance of responses, it is relevant to have a general impression of how familiar the respondents are with the different aspects of latch-up testing. In general, the JEDEC JESD78 standard can be divided into different clauses, starting with "Immunity levels classification", "Detailed test procedure", and "Pass / Fail criteria" up to the more specific clauses like "Special Pins", "Maximum Stress voltage" and "Reporting Requirements".

[Q08] was designed to gauge the familiarity of the survey participants with the different aspects of latch-up testing. To do this [Q08] simply asked if the survey participants were familiar with the following aspects of latch-up testing:

- Pass/Fail criteria
- Immunity levels classification
- Detailed test procedure
- Special pins
- Reporting requirements
- Maximum stress voltage (MSV)

The general familiarity of the industry community with latch-up testing could then be gauged by the percentage of participants that agreed they were familiar with each of the aspects of latch-up testing listed above. The results are shown in Figure 15, first considering all 70 responses by the community.

5.1.3 Familiarity of the Industry Community (cont'd)

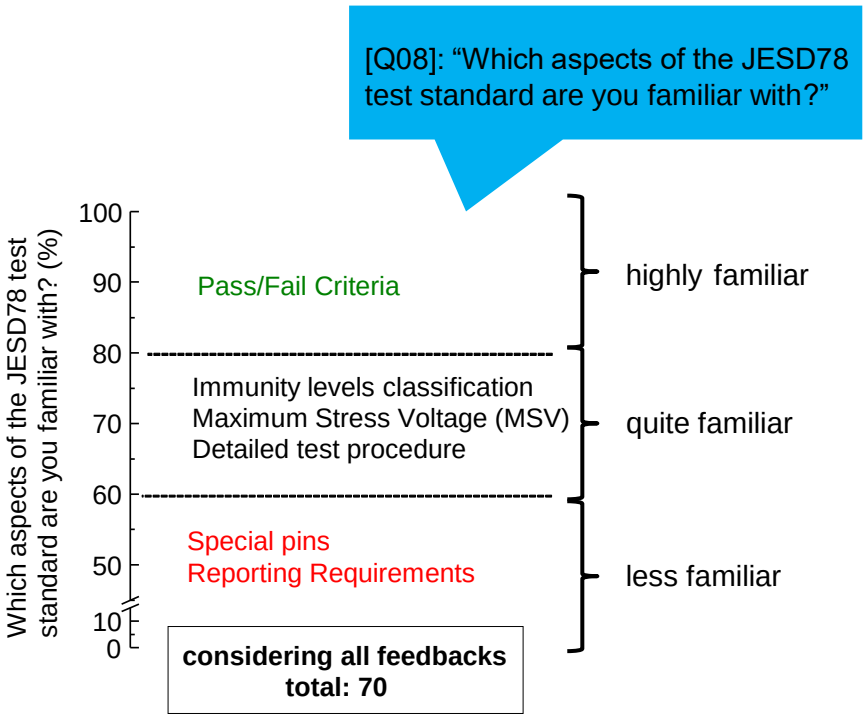


Figure 15 — Responses Regarding the Familiarity of Different Clauses of the Latch-up Standard [Q08], Considering all Feedback.

[Q08] "Which aspects of the JESD78 test standard are you familiar with?"

To better classify the data, three categories were created, and correspondingly sensible levels were introduced, which then map to the degree of familiarity with individual clauses: from "highly familiar" (agreement of 100% - 80% of all participants in the survey) to "quite familiar" (80% - 60%) down to "less familiar" (< 60%). Accordingly, almost 90% of all participants (and thus practically everyone) were familiar with handling the "Pass / Fail Criteria", the highest value reported here. In the areas of "Immunity levels classification", "Detailed test procedure" and "Maximum stress voltage (MSV)", familiarity has decreased with 70% agreement in the middle ("quite familiar"). In the areas of "Special Pins" and "Reporting Requirements", the level continues to slide, so that only every second participant states that they are very familiar with the requirements of the corresponding clause in the standard.

Knowing the complexity and scope of the latch-up standard, this question was re-evaluated, but now only for those respondents who have given feedback for a company as a whole. It is undisputed that the topic of latch-up is multifaceted, starting with topics relating to the derivation of protective measures against latch-up within the scope of product design, the implementation, and organization of latch-up tests, through to the subject of field relevance and field returns. In this context, field returns refer to returned goods following production release at the corresponding level of integration. We have assumed that respondents who overlook the entire process and cycle are much more familiar with the individual clauses of the latch-up standard.

5.1.3 Familiarity of the Industry Community (cont'd)

We now demonstrate the change of the previous results (Figure 16), but now focusing only on feedback given by survey participants responding for a company as a whole.

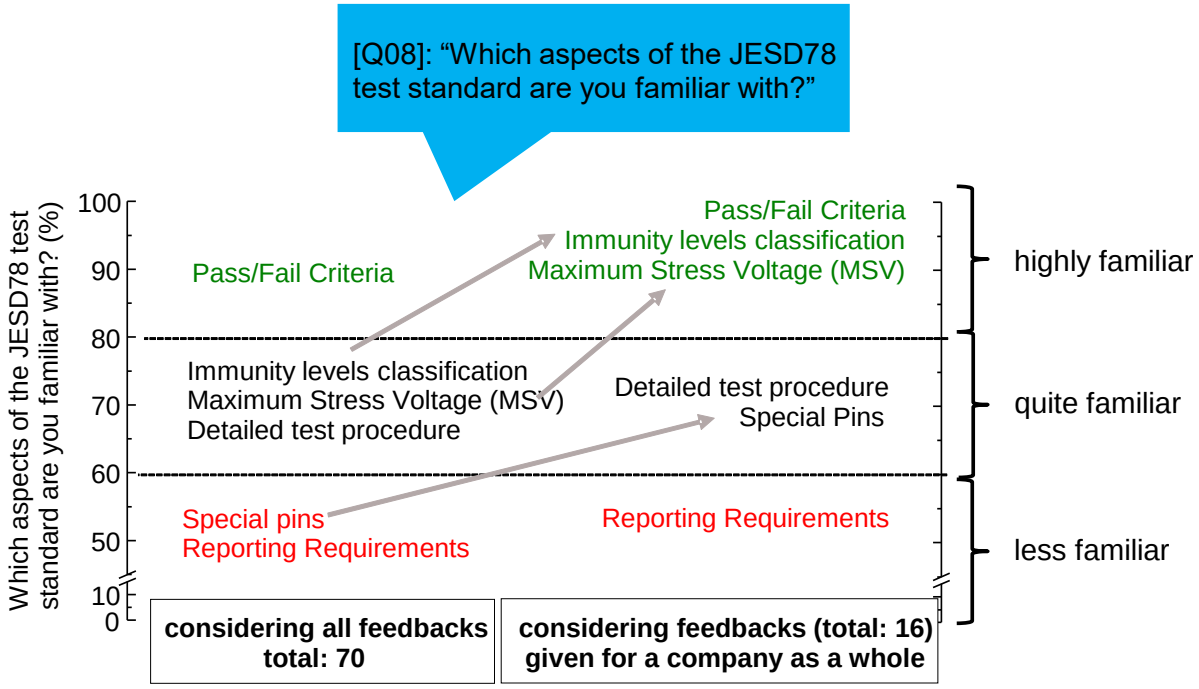


Figure 16 — Change in the Distribution of Responses Regarding the Familiarity if Restricted to Respondents Giving Feedback for a Company as a Whole.

A clear trend can be perceived and confirms the hypothesis made above. For this group of respondents, confidence in the knowledge of the relevant clauses of the standard is higher in all areas. In return, however, this means that colleagues who only have an overview of part of the latch-up value chain, have a greater need for training or clarification.

Finally, taking any of the different aspects ("Pass/Fail Criteria", "Immunity levels", "MSV", "Detailed test procedure", "Special Pins", "Reporting Requirements"), it becomes apparent that it is more or less always the same group consisting of Tier, OEM and "Other" that respond to be less familiar with each particular topic (see Figure 17). In contrast, the IC Supplier and Test House groups seem to have a good understanding. They deal with these issues "naturally" more often than other comparison groups and are trained accordingly. It is relevant to note that this trend is unique regardless of which of the potential answers to the base [Q08] "Which aspects of the JESD78 test standard are you familiar with?" is considered for correlating the data.

5.1.3 Familiarity of the Industry Community (cont'd)

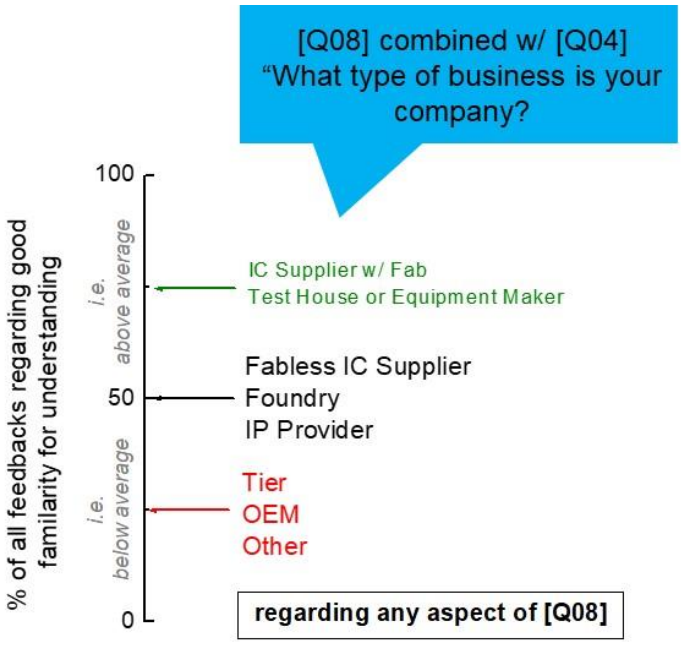


Figure 17 — Taking Any Aspect of the JESD78 Standard Like "Pass/Fail criteria" or "Reporting Requirements" and Correlating to the Type of Business [Q04]

5.2 Case Studies and Field Returns

This clause is dedicated to the survey responses on JESD78 latch-up test implementation, failures, and root causes. Particular topics that will be discussed include questions on return rates, expected field issues prevented by meeting JESD78 requirements, coverage of real-life threats, etc. This part of the analysis deals with the responses to [Q09] through [Q22] of the survey, which are:

- [Q09] Do you think that the JESD78 standard is useful to prevent system failure caused by overcurrent or overvoltage in real world scenarios?
  - [Q10] Please provide examples of the above reply
- [Q11] Have you experienced latch-up failures?
  - [Q12] If yes, where have you experienced latch-up failures?
- [Q13] Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?
  - [Q14] If yes, were the actual stress levels reported to the customer?
  - [Q15] If yes, did that part have any latch-up related field returns?
  - [Q16] If yes, please specify approximate return rate
  - [Q17] If yes, were there any measures taken at the board/system level to mitigate the latch-up risk (e.g., add board-resistor, etc.)?
  - [Q18] If yes, please describe the measures taken
- [Q19] For products that have had latch-up failures in the system, what were the conditions needed to replicate the failure?

5.2 Case Studies and Field Returns (cont'd)

- [Q20] For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?
- [Q21] What percentage of your company's product re-spins were due to latch-up failures in a system application? (Discussed in Clause 5.3.1)
- [Q22] Has your company experienced EIPD (electrical induced physical damage) related to latch-up with parts that passed JESD78 testing at the semiconductor supplier? (Discussed in Clause 5.4.3)

5.2.1 Failure Rates

To get an impression of the occurrence rates of problems at the end-customer side, several questions were included in the survey. As a first high-level question, the number of latch-up related customer complaints (returns) was requested. 58 respondents provided an answer, the results of which are shown in Figure 18. The overwhelming majority receive very few customer complaints per year.

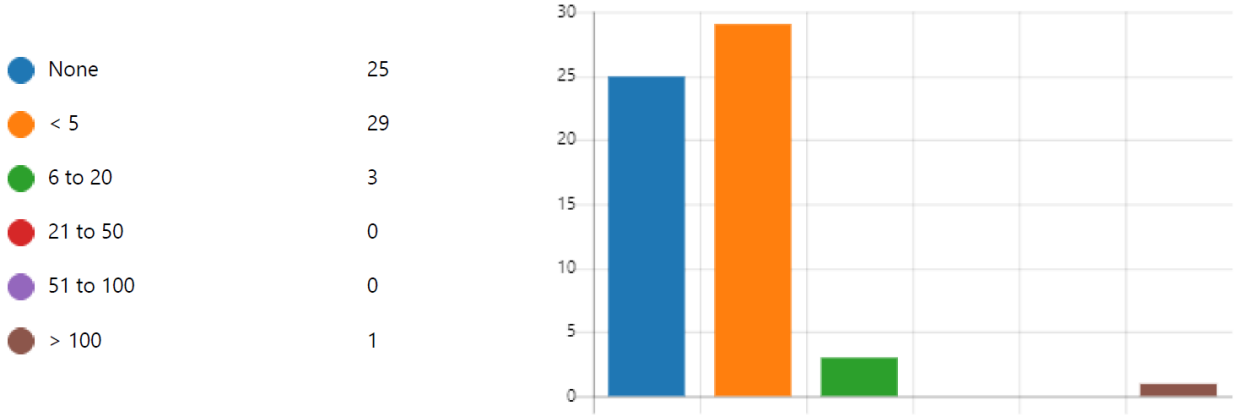


Figure 18 — Pareto of [Q06]

[Q06] "How many latch-up related customer complaints does your company receive per year (approximate number)?"

To better understand what the contribution of JESD78 testing is in preventing customer complaints, a series of questions dives deeper into the testing results.

[Q11] through [Q17] investigate different ways to look at failure rates. From the response on [Q11] "Have you experienced latch-up failures?" we learn that the vast majority (59 out of 69 respondents, 85%) of the respondents have experienced latch-up failures. When asked where failures were observed, 85% of the respondents include JESD78 testing, but 60% include a situation that can (only) occur in the final application and/or at the location of the customer. Looking at it another way, 25% exclusively list JESD78 testing, whereas only single responses exclusively list situations that can be done by the customer. This is discussed in more detail in Clause 5.2.3. From [Q13] "Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?" we learn that immunity level B qualification is used by about 50% of the respondents, see Figure 19, and most of them use it for both voltage and current. In most of these cases, the actual stress levels are shared with the customer. Follow-up questions did not lead to a conclusion on increased failure rates: 1 out of 24 had field returns, but without any measure taken to mitigate it. 17 out of 24 did not get any field returns, while for 6 it was too early to tell.

5.2.1 Failure Rates (cont'd)

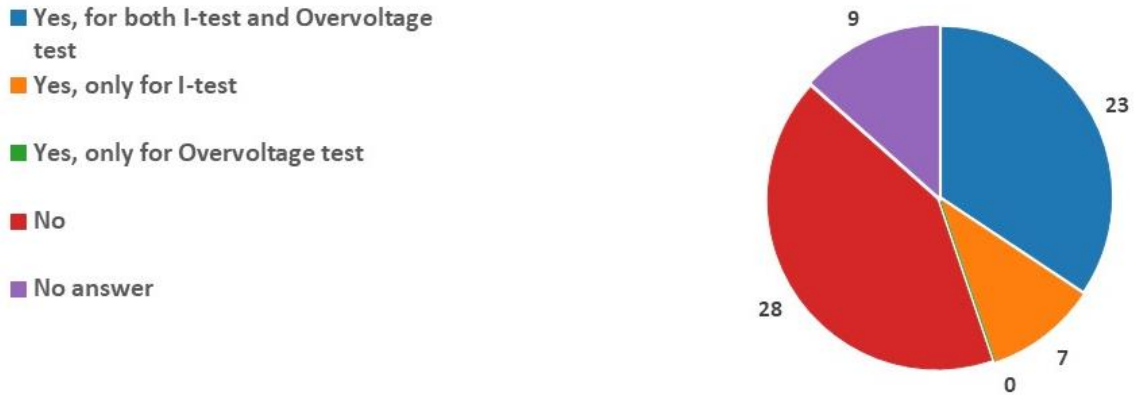
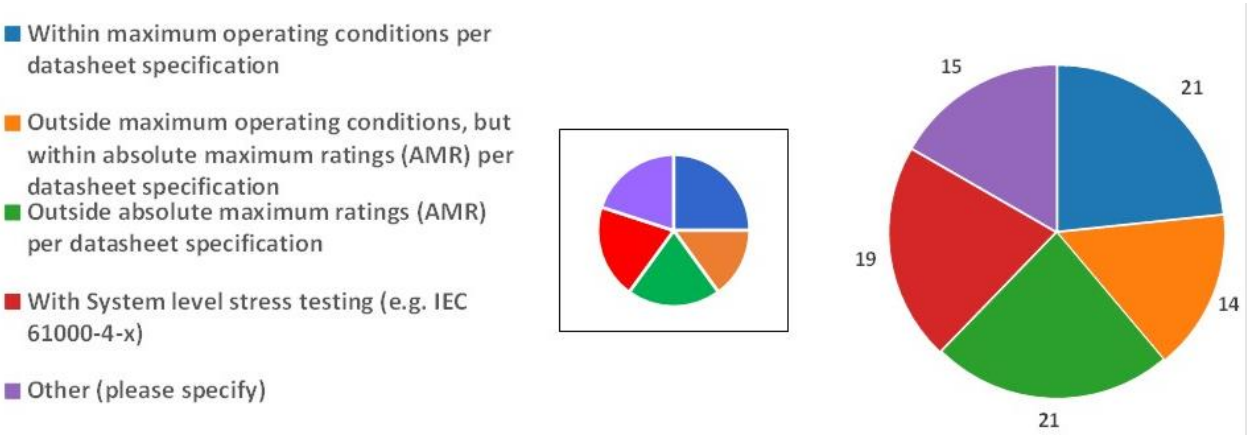


Figure 19 — Pie Chart of [Q13]

[Q13] "Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?"

Next, the survey addresses in [Q19] how the failure could be replicated. The five main categories are surprisingly evenly distributed in the answers of 59 respondents, as shown in Figure 20. Forty out of those responding provided a single answer and this distribution is shown in the small inset. The distribution is very compatible with the overall distribution. The "Other" category showed very diverse answers, however about 1/3 of those entries were related to the stress pulse. Respondents used non-default pulses to trigger the latch-up event: longer or shorter pulses, special system-level pulses, or ESD pulses. All other answers were combinations of the pre-defined answers, but each of these combinations occurred only once or twice. The combination that occurred most was "Within maximum operating conditions per datasheet specification" combined with "With System level stress testing (e.g., IEC 61000-4-x)".



NOTE Inset Shows the Distribution of Responses with Single Responses.

Figure 20 — Pie Chart of the Distribution of the Replication Methods [Q19]

[Q19] "For products that have had latch-up failures in the system, what were the operating conditions needed to replicate the failure?"

5.2.1 Failure Rates (cont'd)

[Q20] asked about failure root causes for products that had passed JESD78 testing. The raw distribution is provided in Figure 21. After analyzing the "Other" category it can be concluded that the main root causes of failures while passing JESD78 are:

1. Issues with standard not addressing the phenomenon (54%)
2. Issues with board design (19%)
3. Issues with IC design (16%)

This indicates that the most common problem is that JESD78 does not address a significant category of real-life stresses that can bring an application into latch-up attributed to fast events, like system level ESD stress and fast power-up situations for example. As indicated by the purple bar in Figure 21 it is generally not a matter of the levels being too low. A minority of IC design-related latch-up problems are not caught by the current way of JESD78 testing. Board issues cannot be expected to be caught by an IC level test.

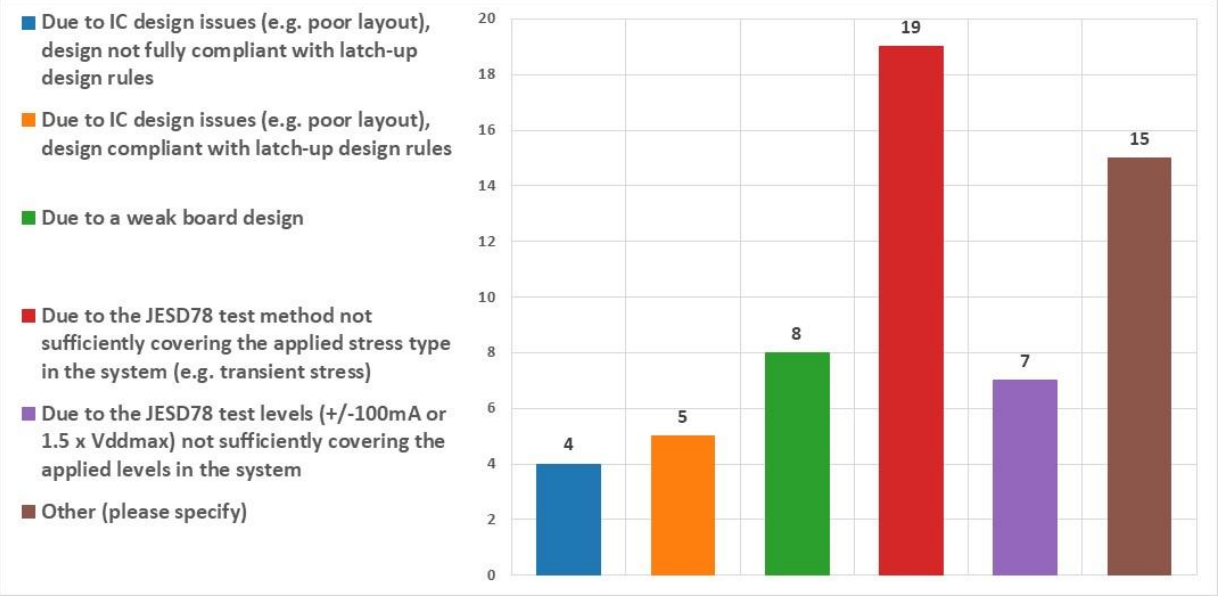


Figure 21 — Distribution of Responses for [Q20]

[Q20] "For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?"

5.2.2 Latch-up Testing vs. Real-World Latch-up Failure Scenarios

It is evident that the main motivation for performing a latch-up qualification on semiconductor products is to check the conformity of the individual IC pins regarding the occurrence of latch-up-related damage in specific overcurrent or overvoltage situations. At this stage, we simply refer to the term "failure caused by latch-up" as the triggering of a low-impedance internal path between supply and ground in the IC.

5.2.2 Latch-up Testing vs. Real-World Latch-up Failure Scenarios (cont'd)

JESD78 describes a method for performing latch-up testing, including the specification of corresponding target values. The question now is to what extent this method and the requirements for overcurrent and overvoltage described therein are sufficient and complete. Complete in the sense that all situations that occur in reality, i.e., in the field, regarding overvoltage and overcurrent are covered. Ideally, applying the JESD78 standard within the scope of a latch-up product qualification could then prove that the IC reacts robustly in its environment at any time and in any situation and does not suffer any damage with regard to latch-up-like phenomena.

As a first step, [Q12] is worked out to confirm that such "real" latch-up-like damage and situations do indeed exist (see Figure 22).

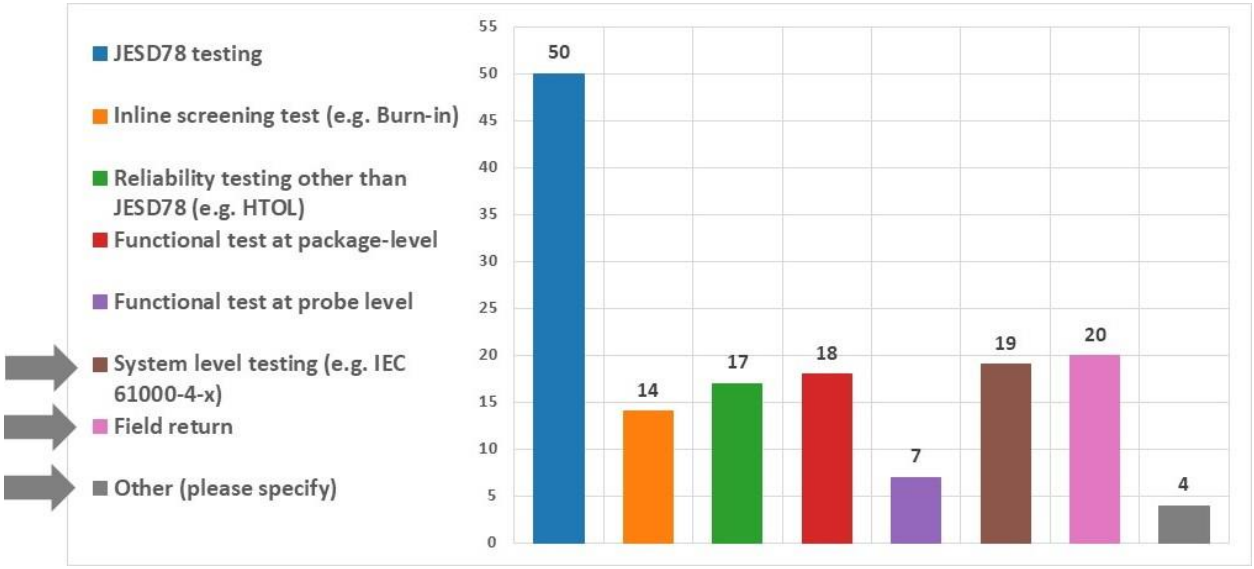


Figure 22 — Pareto of [Q12], in the Case Where [Q11] Was Answered "Yes"

[Q12] "Where have you experienced latch-up failures?"

[Q11] "Have you experienced latch-up failures?"

The term "real-world scenarios" is used here to summarize the areas "System Level Testing", "Field Returns" and "Others". According to the evaluation, for each category, there is definitely corresponding feedback on occurrences available.

To what extent the JESD78 standard has been useful to prevent system failure caused by overcurrent or overvoltage in real-world scenarios is addressed in [Q09] and the results are shown in Figure 23.

5.2.2 Latch-up Testing vs. Real-World Latch-up Failure Scenarios (cont'd)

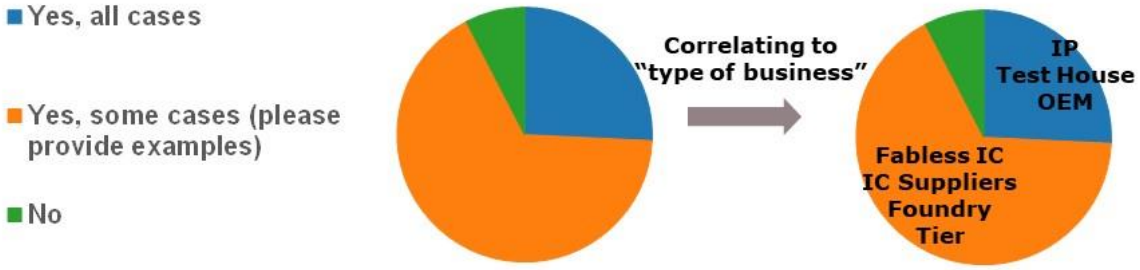


Figure 23 — Pie Chart to Visualize Opinion About [Q09] (Step 1) and Then Correlating Feedback to [Q04] (Step 2)

[Q09] "Do you think that the JESD78 standard is useful to prevent system failure caused by overcurrent or overvoltage in real-world scenarios?"

[Q04] "What type of business is your company?"

Almost 3 out of 4 of all respondents, and thus the vast majority of the participants in the survey, believe that the application of the JESD78 standard was not helpful in identifying all, but only some of the latch-up-type damage observed in the field. In reality, there exists many more latch-up-like failure scenarios that are not addressed by the JESD78 standard. Which specific scenarios that could be (for example transient-related latch-up stress or ESD system-level-related stress) will be dealt with in detail in a later part of the survey. Only about 1 out of 4 participants expressed that through testing according to JESD78, latch-up-like events in the field can be principally avoided.

With the help of the feedback to [Q04], and as shown in Figure 23 it is possible to find out who responded predominantly optimistically and who responded more pessimistically. For example, more than 65% of all respondents from Fabless IC companies, IC suppliers, Foundries, and Tier found that JESD78 would only catch some cases of latch-up susceptibility. In contrast, 75% of respondents from IP Suppliers, Test Houses, and OEMs had faith that JESD78 would find all latch-up susceptibility.

5.2.3 Experience of the Semiconductor Industry Concerning the Amount and Frequency of Latch-up Failures and their Root Cause

The question about the frequency of failures due to latch-up was asked twice. First with the background of how many times *per year* every single participant of this survey *currently* must deal with such an error pattern. This was addressed in [Q06] and the results are shown in Figure 24.

5.2.3 Experience of the Semiconductor Industry (cont'd)

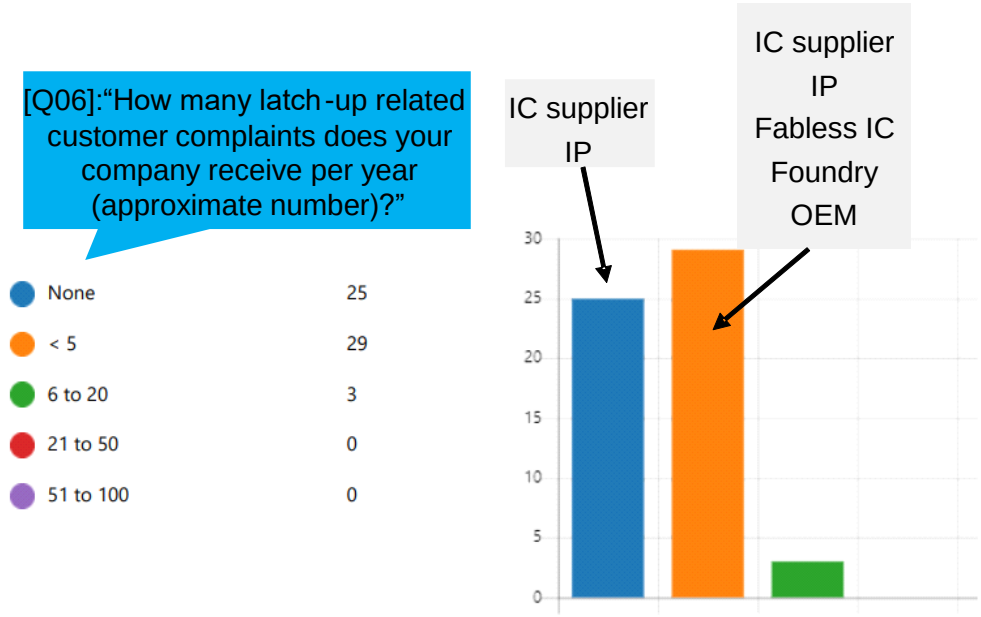


Figure 24 — Pie Chart of [Q06], and Correlating Feedback to [Q04]

[Q06] "How many latch-up related customer complaints does your company receive per year (approximate number)?"

[Q04] "What type of business is your company?"

The vast majority of the answers given are limited to the two options "no complaints" or "number of complaints < 5". The occurrence of higher failure rates is rarely reported. With the help of the answers to [Q04] "What type of business is your company?", it can be determined that it is fifty-fifty of the participants of the group "IC suppliers" and "IP providers" that report they either have no complaint or complaint rates below 5. On the other hand, more or less all participants from the areas of fabless IC, foundry, and OEM must deal with some small number of failures each year.

If one does not look at the current day-to-day business but asks whether there have been latch-up failures *in the past in general* ([Q11]), the following picture emerges in Figure 25.

Figure 25 — Pie Chart of [Q11],

[Q11] "Have you experienced latch-up failures?"

5.2.3 Experience of the Semiconductor Industry (cont'd)

Accordingly, almost 85% of all participants of the survey had to deal with latch-up failures in the course of their work. The subject of latch-up failure is therefore present in all branches of the semiconductor industry.

Continuing by asking in which situations a latch-up failure occurred [Q12], the results are shown in Figure 26.

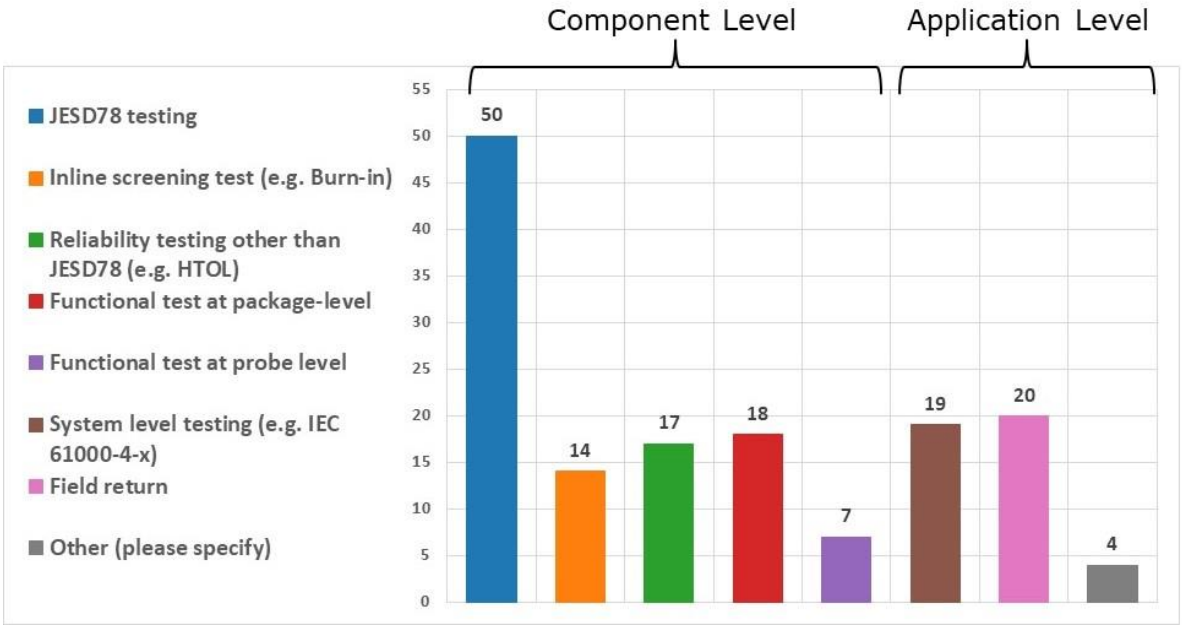


Figure 26 — Feedback to [Q12], in the Case Where [Q11] Was Answered "Yes"

[Q12] "Where have you experienced latch-up failures?"

[Q11] "Have you experienced latch-up failures?"

First of all, it is important to note that there was the possibility of submitting multiple answers to this question. For better orientation, it is marked additionally, whether the underlying failure situation appeared in a situation when the component was "isolated" or used in a system or application.

In this presentation and overview, the category "JESD78 testing" clearly dominates. About two-thirds of all participants have reported at least one latch-up-like failure during a latch-up qualification over the years. However, there are definitely further situations at the level of a single component or its use in the application (for example due to the use of additional test procedures such as screening or system level stress) that have led to a latch-up-like failure.

If one evaluates the data further, the dominance that it is precisely the class of JESD78 testing that rules the number of latch-up failures is lost! To do this, we take the number of responses that stated that they had ever had to deal with latch-up failures (59 in [Q11]) and divided them into these 3 categories, as shown in Figure 27.

- Exclusively fails from JESD78 testing ⇨ 13
- Fails from JESD78 testing and at least one other event ⇨ 38
- Latch-up failures but not caused by JESD78 testing ⇨ 8

5.2.3 Experience of the Semiconductor Industry (cont'd)

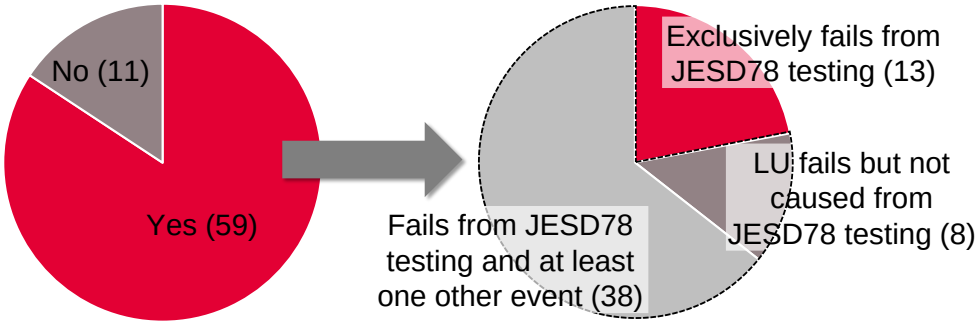


Figure 27 — Evaluation of [Q11], and in the Case of "Yes", Identifying How Many Responses Saw Any Further Event Besides JESD78 Testing Mentioned.

[Q11] "Have you experienced latch-up failures?"

Only in 13 cases (22%), and thus for a smaller part of the participants, latch-up failures in the past were solely due to JESD78 testing. On the other hand, 8 + 38 = 46 (78%) of the responses indicated that events other than JESD78 testing were also possible to explain latch-up damage in the past.

From this evaluation, one could conclude that it was indeed very likely that latch-up-like damage was not generated by JESD78 testing alone but popped up in a variety of other ways.

Finally, Figure 28 illustrates which business areas reported situations that led to a latch-up-like behavior. The participants from the "Fabless IC", "Foundry", and "IC Supplier" areas showed latch-up-like failures in all the areas listed. In the "IP Supplier" domain, the failures are limited to "Testing according to JESD78" and for OEMs to "System Level Testing" or "Field failure".

5.2.3 Experience of the Semiconductor Industry (cont'd)

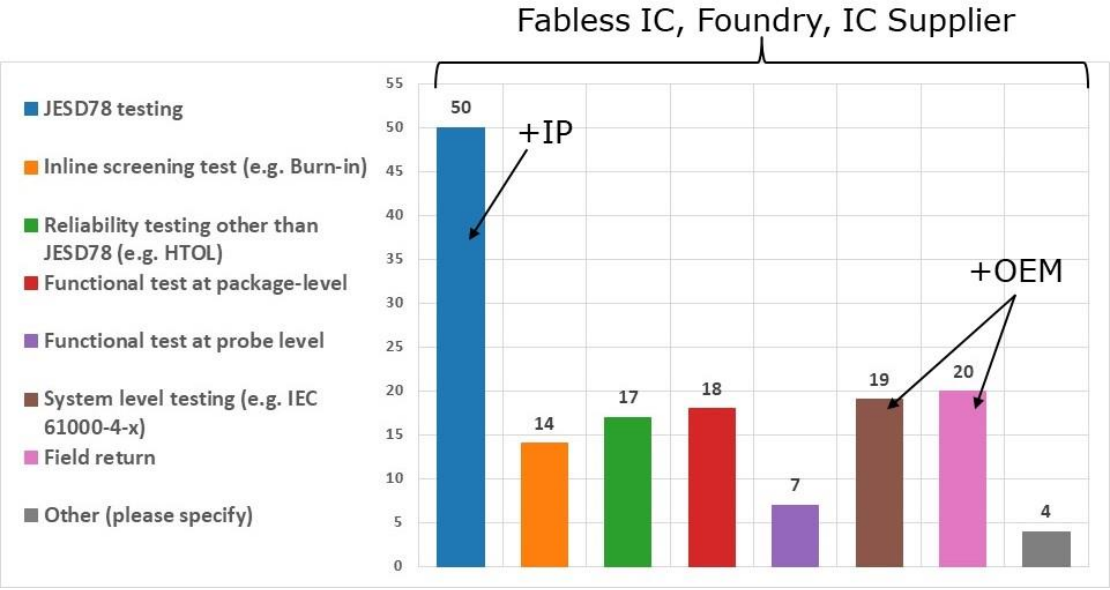


Figure 28 — Correlating [Q12], in the Case Where [Q11] Was Answered "Yes", With [Q04],

[Q12] "Where have you experienced latch-up failures?"

[Q11] "Have you experienced latch-up failures?"

[Q04] "What type of business is your company?"

5.2.3.1 Further Observations and Implications for the Case Where Participants in the Questionnaire Indicated That They Have Had or Had Not to Deal with Latch-Up Faults at All.

From the deeper correlation analysis, interesting clues emerge as to how participants …

- who have not previously had to deal with latch-up failures on their products, or
- who were facing latch-up issues during "System level testing (e.g., IEC 61000-4-x)" or "Inline screening test (e.g., Burn-in)"…

think about whether the JESD78 standard is sufficient to prevent latch-up failures in the field. First, the relevant data for the group of respondents having no latch-up problem in its overview is shown in Figure 29, Figure 30, and Figure 31.

5.2.3.1 Further Observations and Implications (cont'd)

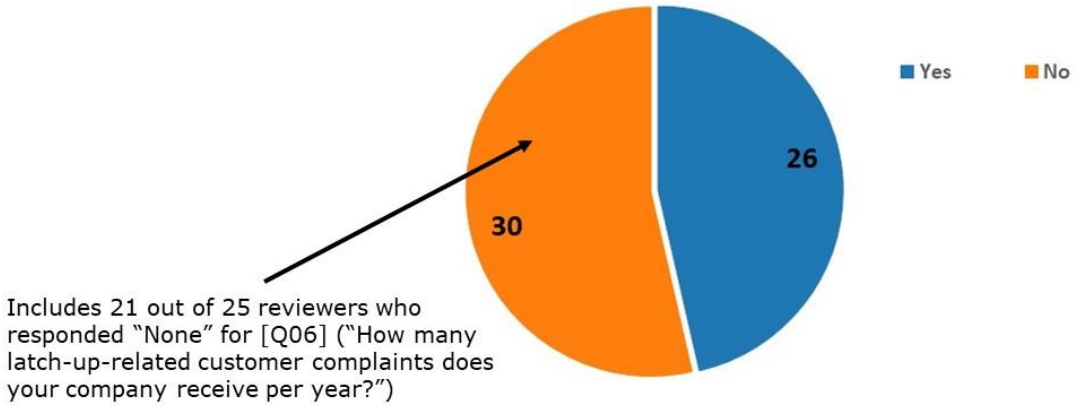


Figure 29 — Correlating Those Who Answered "No" for [Q49] With Those Choosing "None" as Feedback for [Q06]

[Q49] "Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?"

[Q06] "How many latch-up related customer complaints does your company receive per year (approximate number)?"

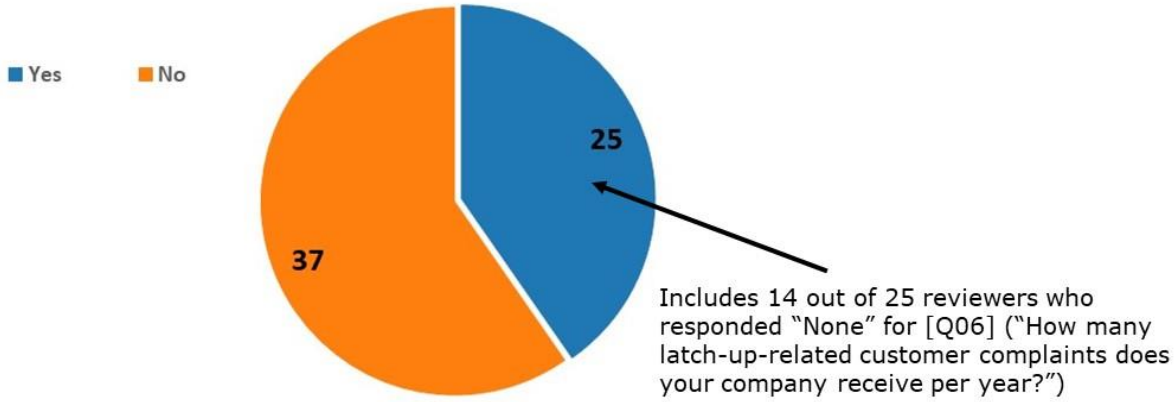


Figure 30 — Correlating Those Who Answered "Yes" for [Q41] With Those Choosing "None" as Feedback for [Q06]

[Q41] "Does passing JESD78 testing guarantee latch-up robustness in the field?"

[Q06] "How many latch-up related customer complaints does your company receive per year (approximate number)?"

5.2.3.1 Further Observations and Implications (cont'd)

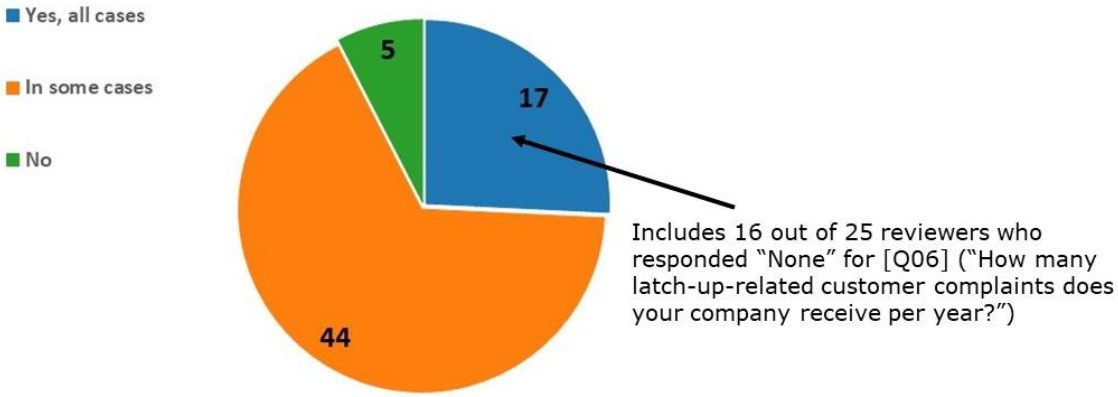


Figure 31 — Correlating Those Who Answered "Yes, All Cases" for [Q09], With Those Choosing "None" as Feedback for [Q06]

[Q09] "Do you think that the JESD78 standard is useful to prevent system failure caused by overcurrent or overvoltage in real world scenarios?"

[Q06] "How many latch-up related customer complaints does your company receive per year (approximate number)?"

From the standards point of view, it is good to learn that the group of respondents who have not previously been affected by any latch-up damage in the context of JESD78 testing or field returns are also convinced that the application of the JESD78 standard in effect when the survey was performed is perfectly sufficient to detect and avoid latch-up situations.

What is the mindset of respondents that had to deal with latch-up issues in the past caught during either "System level testing" or "Inline Screening test"? The results are shown in Figure 32.

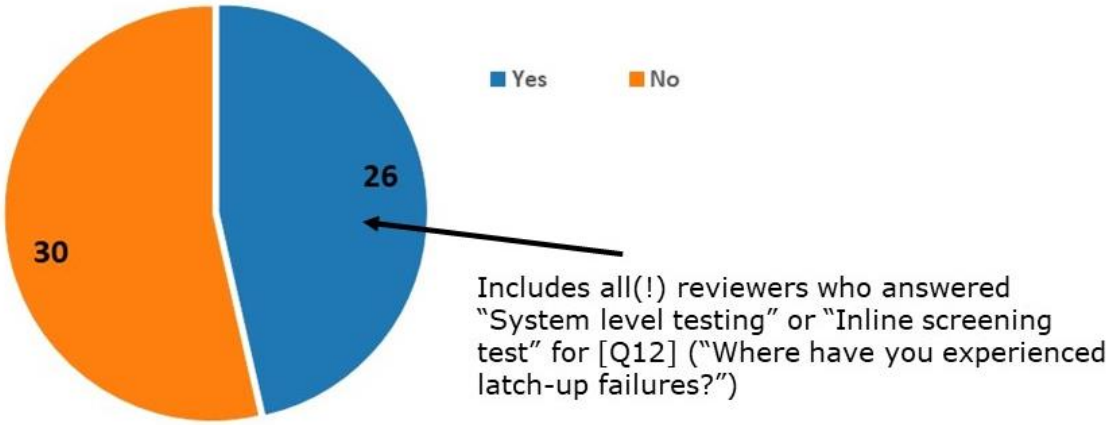


Figure 32 — Correlating [Q49] With Those Choosing "System Level Testing" and "Inline Screening Test" for [Q12]

[Q49] "Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?"

[Q12] "Where have you experienced latch-up failures?"

5.2.3.1 Further Observations and Implications (cont'd)

All(!) affected respondents choosing either "System level testing" or "Inline Screening test" suggested a need for a new test method that specifies generic current injection and voltage testing.

5.2.4 Qualification vs. Real Life

About half of the respondents (30) affirm that their companies are selling immunity level B components (either for current injection or overvoltage) according to [Q13]. However, 25 of them didn't get any latch-up related field return and just 1 declared to have failures without giving any rate. The remaining cannot report any data since the qualification is recent.

For products that have had latch-up failures in the system ([Q19]), conditions to replicate the failure can be grouped as "within AMR limits", and "outside of AMR limits". This grouping suggests that a number of latch-up failures lie within the testing range of JESD78 since the voltage limits specified by the standard and MSV values frequently exceed AMR values (see Figure 33).

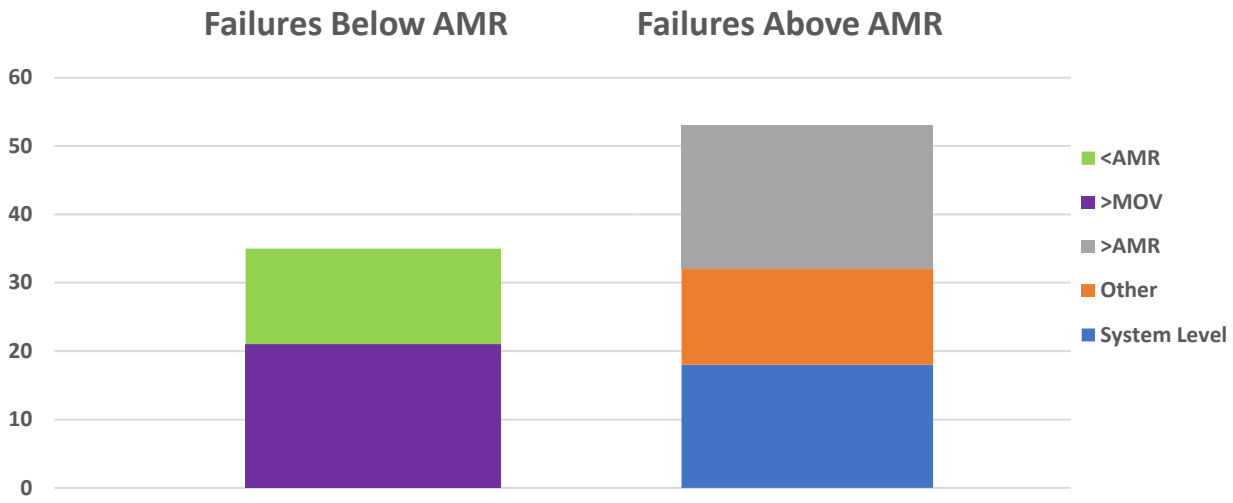


Figure 33 — Conditions to Replicate Failures in the System

For products that have had latch-up failures in the system, but had passed JESD78 testing ([Q20]), we can perform the same analysis grouping that results in:

- JESD78 not covering the applied stress (26)
- IC design issues (8)
- Board or Other issues (23)

Two main detractors are lack of JESD78 coverage and Board or Other causes.

This result is almost market, technology, and type of business independent, although all IC issues are related to companies that are dealing with Mixed Signal (8/8) and that are in Automotive (7/8) and Industrial (6/8) markets.

5.2.4 Qualification vs. Real Life (cont'd)

Latch-up is a mandatory qualification test ([Q23]) but for products that are offered in multiple packages that use the same die ([Q25]) half of the companies perform trials on all packages while half qualify their ICs by similarity regardless of market. Looking to company business, Fabless IC suppliers seem to prefer testing all packages (9/12) while IC Suppliers with Fab prefer qualification by similarity (20/31).

Possible Interpretation
This is not surprising because Fabless IC suppliers have less control on technology and maybe less products to compare having lower confidence level. Companies selling multichip products generally qualify them using the same strategy used for single die ICs.

In the same way, it is possible to roughly distinguish product types in two macro categories: technologies based on standard I/O cells (low or very low voltage, memories and radio frequency (RF)) or based on custom I/O cells (medium or high voltage, Analog, Mixed signal, and Power ICs); given this definition testing all packages is the preferred methodology for custom I/O designers while for the others both strategies are equally used ([Q25]).

Qualification strategies do not have any impact on either the latch-up experience ([Q11]) nor on where the latch-up has been detected ([Q12]).

5.3 Goal and Testing Strategy

This part of the survey addresses issues like "Reflecting latch-up Test Goals", "latch-up test coverage vs. real world", and "supplier latch-up reporting". In particular, it is the response to [Q23] through [Q42] of the survey, which are:

Latch-up test goals:

- [Q23] Is JESD78 testing a product qualification requirement in your company?
  - [Q24] If only for certain product types, please specify
- [Q25] What is the JESD78 test requirement in your company for products that are offered in multiple packages that use the same die? (Discussed in Clause 5.2.4)
- [Q26] What is the JESD78 test requirement in your company for Multi-Chip Products?

Occurrence rate of latch-up failures and consequences:

- [Q27] What percentage of your company's products has experienced latch-up failures (either in JESD78 qualification testing or in the field)?
- [Q28] What percentage of your company's product re-spins were due to failures during JESD78 qualification test?
- [Q29] What percentage of your company's product re-spins were due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?

Latch-up test coverage vs. real world:

- [Q30] What is the goal of the supply overvoltage test and I/O (signal pin) injection test in the present JESD78 standard?

5.3 Goal and Testing Strategy (cont'd)

- [Q31] Does the JESD78 testing address real world stress events like HBM and CDM do?
  - [Q32] If JESD78 testing were removed as a qualification requirement for the industry, what would happen?
  - [Q33] Please specify why

Latch-up reporting

- [Q34] Do you require detailed JESD78 information from an IC supplier?
- [Q35] Do you scrutinize the JESD78 information provided by an IC Supplier?
- [Q36] How are JESD78 test results provided in an IC Supplier datasheet or qualification report used for system design?

Modes and Test-Parameters considered for latch-up testing:

- [Q37] Would increasing the overvoltage or injection current levels of JESD78 decrease the latch-up failures in the field?
- [Q38] Is the operational state of an IC used during JESD78 testing (i.e., low power mode, stable current) representative of real-world applications?
  - [Q39] If not, please specify why not
- [Q40] If a product has multiple modes of operation, how does your company test for JESD78 latch-up?
- [Q41] Does passing JESD78 testing guarantee latch-up robustness in the field?
  - [Q42] If no, what other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?

5.3.1 Customer Complaints

In the next questions, we try to assess the magnitude of the latch-up problem in practical situations. Figure 34 shows the Pareto of the percentage of products that experienced latch-up failures, in qualification testing or the field.

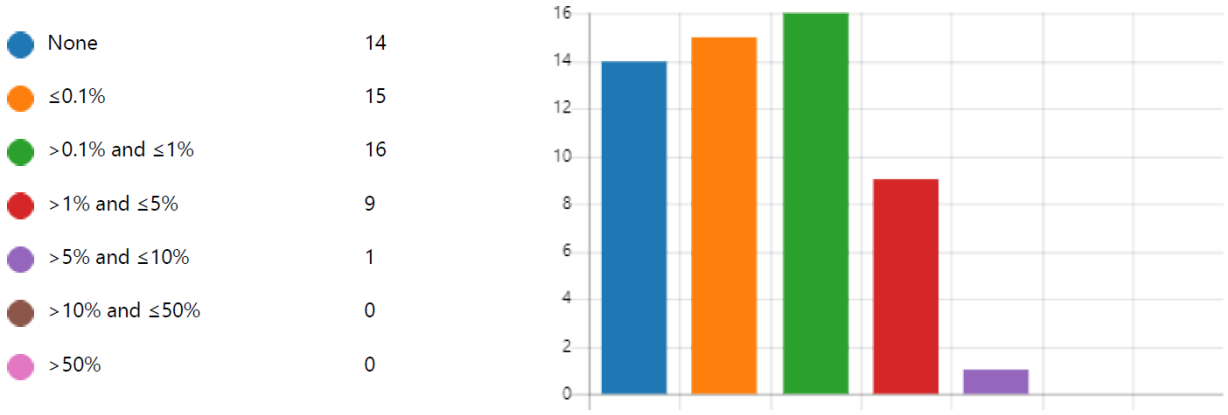


Figure 34 — Pareto of [Q27]

[Q27] "What percentage of your company's product has experienced latch-up failures (either in JESD78 qualification testing or in the field)?"

5.3.1 Customer Complaints (cont'd)

Next, it is time to look at re-spins resulting from latch-up related problems. Figure 35 shows a Pareto of the re-spin rates provided by the respondents. Roughly, 50% of the respondents do not have re-spins due to latch-up related problems. This can indicate that the problems can be solved in other ways, are not severe enough, or are not even reported.

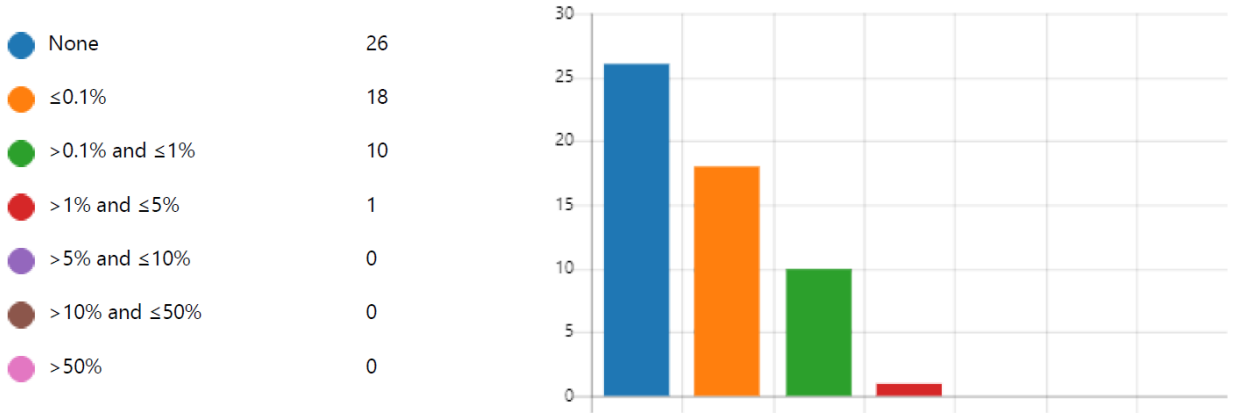


Figure 35 — Pareto of [Q21]

[Q21] "What percentage of your company's product re-spins were due to latch-up failures in a system application?"

Possible Interpretation
It is likely that for 50% of the LU related problems, options exist to solve the issue without an IC re-spin, for example, by software modifications or by changes on the application board.

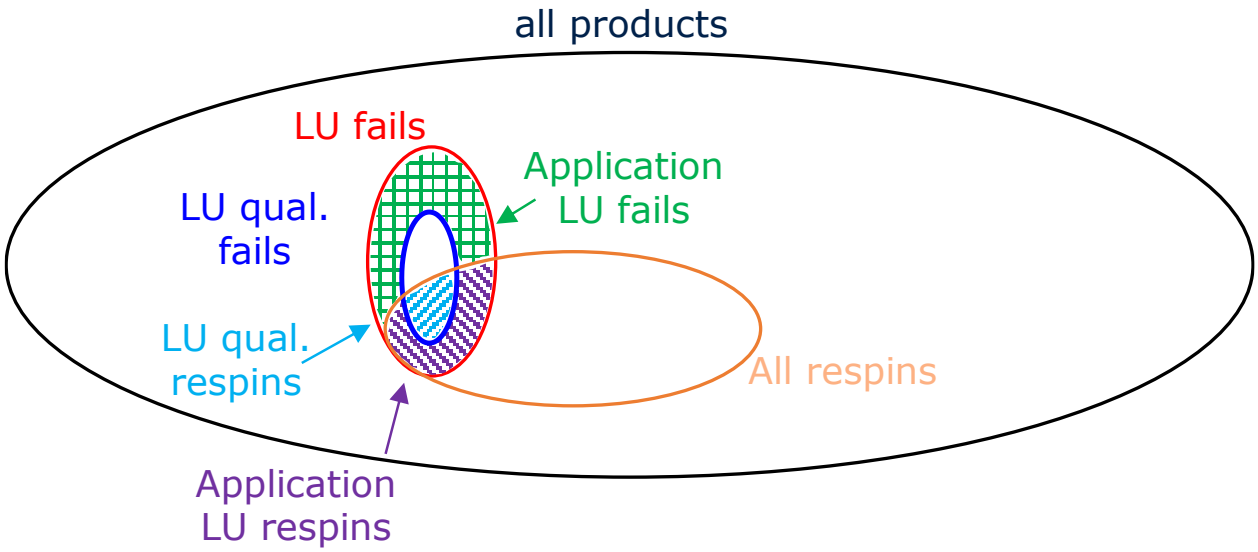
To get a numerical impression of the relationship between the questions related to returns and re-spins the following estimate may be useful. For each question, the sum of the upper limit of each interval times the number of responses for that limit is calculated and the result is divided by the total number of responses. This way a "weighted average" of the percentages serves as an estimate. The results are provided in Table 1. Based on these numbers the average system application latch-up re-spin rate is smaller than 0.3%. Similarly, a rough upper bound estimate for the average percentage of problematic products is 1.3%.

Table 1 — Calculated Estimates of Occurrence

Question	Weighted Average
[Q21] – **re-spins** after latch-up failures in system application	0.3%
[Q27] – **latch-up failures** in JESD78 & field	1.3%
[Q28] – **re-spins** after failure in latch-up qualification	0.6%
[Q29] – **re-spins** after latch-up failure not caught by JESD78	0.5%

5.3.1 Customer Complaints (cont'd)

From [Q28] and [Q29] we find that the distributions of latch-up related re-spins from qualification testing and application-related failure are almost identical. Figure 36 provides a graphical illustration of how the responses relate to each other.



NOTE All latch-up failures [Q27] comprise latch-up qualification failures and re-spins [Q28] and application testing latch-up re-spins [Q29] and failures [Q21] within the groups of all re-spins and products.

Figure 36 — Illustration of how the Responses to [Q28] and [Q29] Relate to Each Other

[Q28] "What percentage of your company's product re-spins were due to failures during JESD78 qualification test?"

[Q29] "What percentage of your company's product re-spins were due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?"

5.3.1 Customer Complaints (cont'd)

Figure 37 gives an example of how the occurrence of latch-up failures relates to re-spins resulting from qualification fails.

Figure 37 — Relationship Between [Q27] and [Q28] in Absolute Numbers (Top Graph) and Relative to the Number of Replies per Answer to [Q27] (Bottom Graph)

[Q27] "What percentage of your company's product has experienced latch-up failures (either in JESD78 qualification testing or in the field)?"

[Q28] "What percentage of your company's product re-spins were due to failures during JESD78 qualification test?"

5.3.1 Customer Complaints (cont'd)

Figure 37 shows some things that are unexpected (and may say something about accuracy). For example, the first column is about responders indicating "NO failures". Yet at least one respondent is stating they did re-spins for latch-up. Therefore, further analysis was done.

Another way of looking at this data is the following. [Q27] asked for the percentage of products that had experienced latch-up failures (either in JESD78 qualification testing or in the field). Fourteen out of 55 respondents replied 'None'. For consistency, it was verified that these respondents also replied 'None' to [Q21], [Q28], and [Q29]. For the respondents that replied with a percentage to [Q27], the responses to these questions are categorized in Table 2.

Table 2 — Categorization of Responses to Questions Related to Re-Spins

Base: [Q27] & replied with > 0%		
	# Of Responders Reporting Redesigns	**# Of Responders Reporting No-Redesigns**
[Q21] re-spins due to latch-up failures in a system application?	27	11
[Q28] re-spins due to failures during the JESD78 qualification test?	36	5
[Q29] re-spins due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?	22	17

This leads to the following observations:

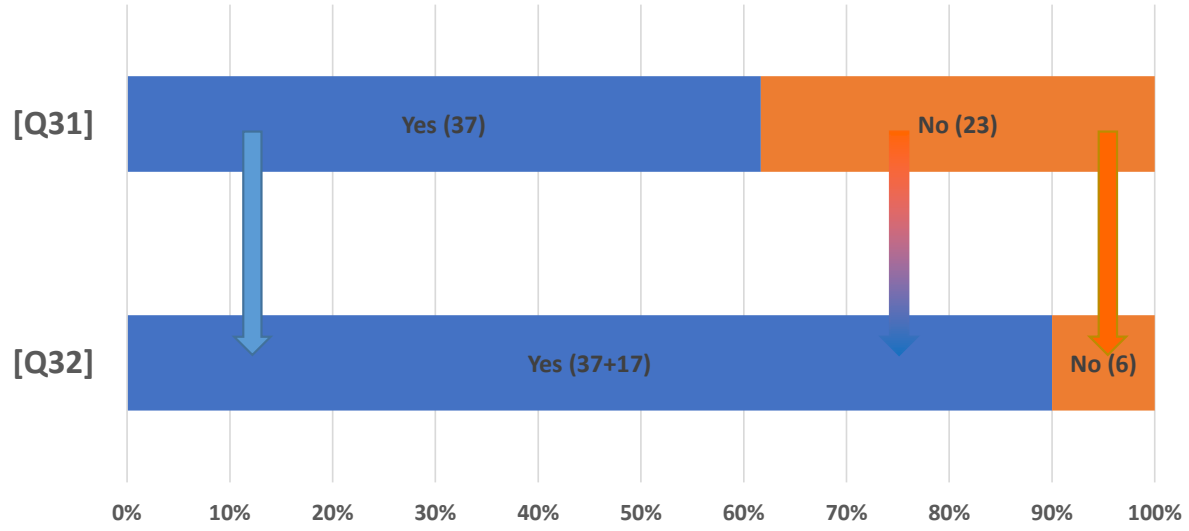
- 2/3 of all participants reported having latch-up failures.
- In the case of latch-up failures detected during JESD78 testing, a significant majority of the products received a re-design.
- In the case of latch-up failures detected during reliability testing or system testing, only half of the situations were contained by re-designs.

The interpretation of the data is as follows: Generally, the number of re-spins is smaller than the number of failures (consistency check). But e.g., in the column "failures between 1% and 5%" there is only a small number of respondents saying that the percentage of re-spins is between 1% and 5%. This is an indication that latch-up failures do not automatically lead to re-spins and that re-spins (which are very costly for the suppliers) are under-represented.

This supports the claim that there are more ways to solve latch-up problems.

5.3.2 Expectations and Usefulness

[Q31] through [Q33] are asking for expectations of users of the JESD78 method and results are shown in Figure 38.



NOTE [Q32] = Yes → Components would be less reliable in the field. [Q32] = No → It would have no effect.

Figure 38 — Distribution of Responses to [Q31] and [Q32]

[Q31] "Does the JESD78 testing address real world stress events like HBM and CDM do?"

[Q32] "If JESD78 testing were removed as a qualification requirement for the industry, what would happen?"

A 90% majority (54 out of 60 total) of the respondents to both questions answered YES at [Q32], thinking components would be less reliable in the field, 100% of them answering YES at [Q31], thinking that JESD78 addresses real-world scenarios. Asked for a reason ([Q33] Please specify why), responders who answered positively to both questions (62%) confirmed with different flavor that JESD78 ensures some level of robustness against system disturbances.

The 17 respondents (28%) that answered differently to [Q31] and [Q32] would like to keep JESD78 mainly because it is still useful in some situations as a rough check.

On the other hand, the remaining 10% who answered NO on [Q32] also answered NO on [Q31], believing that JESD78 does not address real world scenarios nor has an impact on reliability in the field. Looking for their reasons, we find:

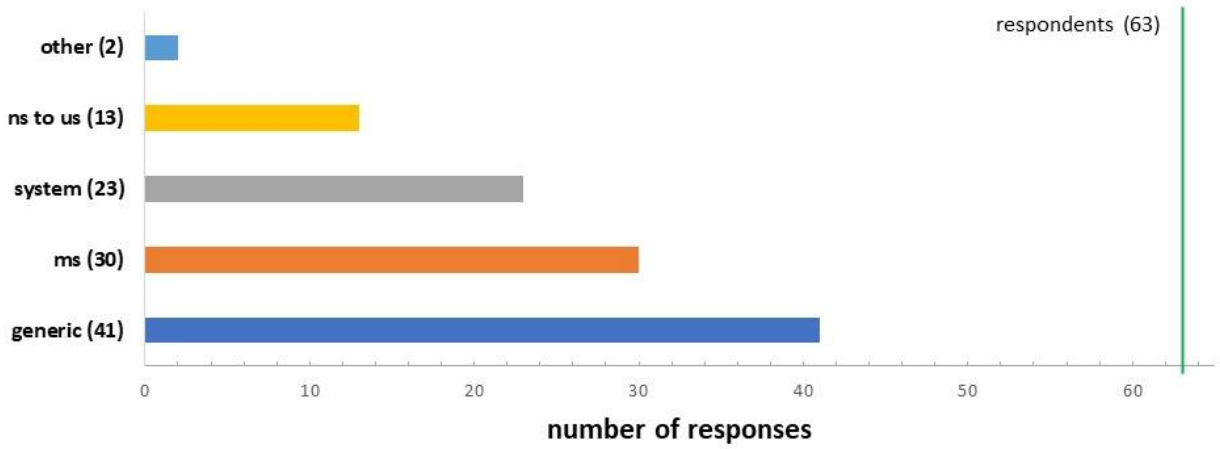
- Low number of latch-up occurrences
- Wrong interpretation of AMR
- Common "non-belief" in the effectiveness of the test method

5.3.2 Expectations and Usefulness (cont'd)

Looking deeper into [Q33] ("Specify why" related to [Q32] "If JESD78 testing were removed as a qualification requirement for the industry, what would happen?"), explanations are given as to why removing JESD78 can lead to reliability reduction in the field can be classified as follow:

- 55% state that JESD78 at least covers part of the threat
- 13% state the standard drives robust design
- 13% say it provides a minimum robustness level
- Some claim it is used as a benchmark or EOS test
- Respondents that say 'nothing would happen' point out that the failure/return rates are very low

When asked about the goal of the overvoltage and current injection test ([Q30] "What is the goal of the supply overvoltage test and I/O (signal pin) injection test in the present JESD78 standard?") respondents were able to choose more than one answer. About half (30) of the responders (63 in total) expect robustness against disturbances in the millisecond time range, but only 6 of them selected only this answer. A total of 79 responses (= 41 + 23 + 13 + 2) expect robustness against pulses in the nanosecond to microsecond range, system level pulses, or other pulse shapes far beyond JESD78. Typical JESD78 settings apply pulses with millisecond duration to the DUT.



NOTE Since multiple answers were allowed, the Total Sum is > 100%

Figure 39 — Distribution of Responses to [Q30]

Possible Interpretation
The applied conditions during JESD78 stress are far more limited than given credit for. It is questionable that passing JESD78 would address the same failure mechanisms during stress events with other pulse shapes and/or shorter or longer pulse widths. Survey participants believe that the relatively long pulses used during JESD78 testing can be effective in detecting latch-up events by a wide variety of pulse shapes, intensities, and durations.

5.3.2 Expectations and Usefulness (cont'd)

Figure 40 shows that 86% (59 out of 69) believe that after removal of JESD78 testing, components would be less reliable in the field. However, a majority of 54% (32 out of 59) does not believe that a further increase of stress levels would decrease the number of latch-up failures in the field.

		[Q37] Would increasing the overvoltage or injection current levels of JESD78 decrease the latch-up failures in the field?			
	Total #	**Yes**	**No**	**No answer**	
[Q32] If JESD78 testing were removed as a qualification requirement for the industry, what would happen?	**Components would be less reliable in the field**	17	32	10	**59**
	No Effect	0	5	1	**6**
	No answer	0	0	4	**4**
		17	**37**	**15**	**69**

Figure 40 — Correlation of [Q32] With [Q37]

Therefore, it seems that over several decades the 100-mA threshold was established and accepted as a general level for sufficient robustness against a variety of electrical stress pulses in the field.

5.3.2 Expectations and Usefulness (cont'd)

Looking for the relationship between [Q31] and [Q41], Figure 41 shows that respondents either thinking JESD78 can mimic real world or not do not fully trust that passing JESD78 is enough to guarantee latch-up robustness in the field.

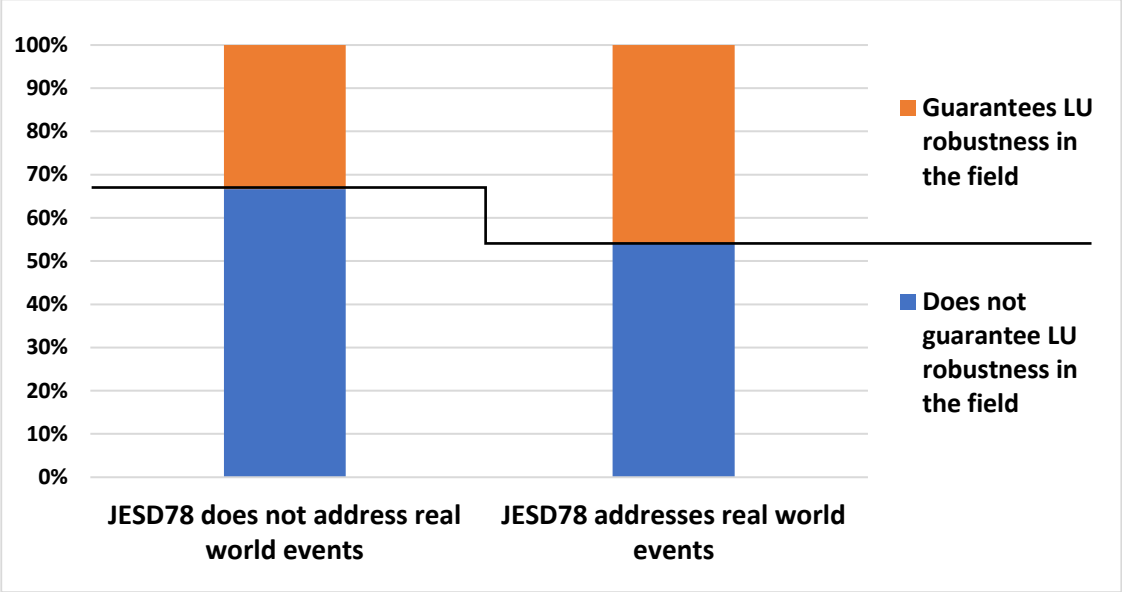


Figure 41 — Comparison of [Q31] and [Q41],

[Q31] "Does JESD78 address real-world events?"

[Q41] "Does passing JESD78 testing guarantee latch-up robustness in the field?"

5.3.2 Expectations and Usefulness (cont'd)

As shown in Figure 42, among respondents thinking JESD78 addresses a real-world scenario ([Q31] → Yes — 37 respondents), the majority of those expecting JESD78 can guarantee latch-up robustness in the field (product safe) claim that operational state should be improved in order to better mimic a real application scenario (orange bar of right graph). In the same way, also for respondents thinking JESD78 does not address real world scenario, as shown in Figure 43, ([Q31] → No – 23 respondents) who answers [Q37] and [Q38], the operational state is required to be adjusted to be closer to the real state.

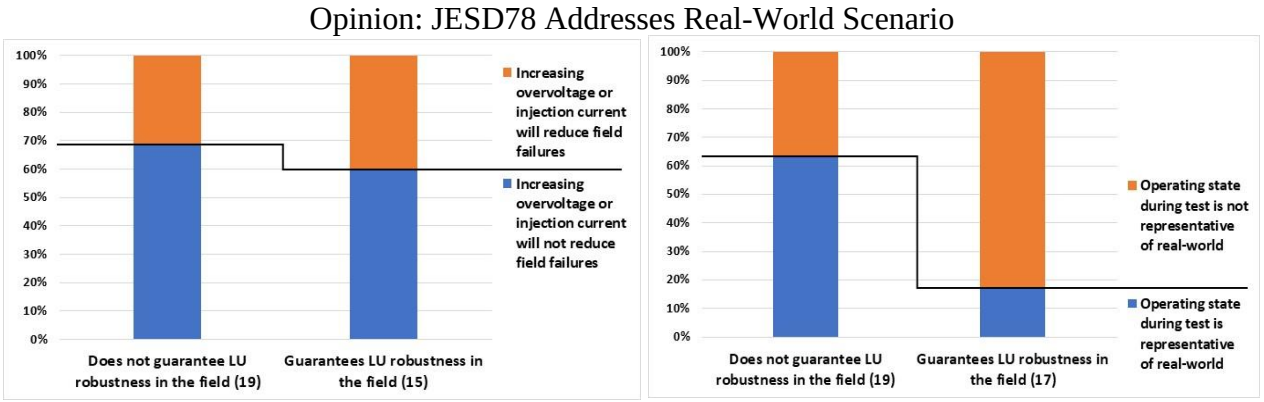


Figure 42 — Comparison of [Q41] With [Q37] and [Q38] for Respondents Thinking JESD78 Addresses Real-World Scenario

[Q41] "Does passing JESD78 testing guarantee latch-up robustness in the field?"

[Q37] "Would increasing test levels reduce latch-up field failures?"

[Q38] "Is the operational state of an IC used during JESD78 testing representative of real-world applications?"

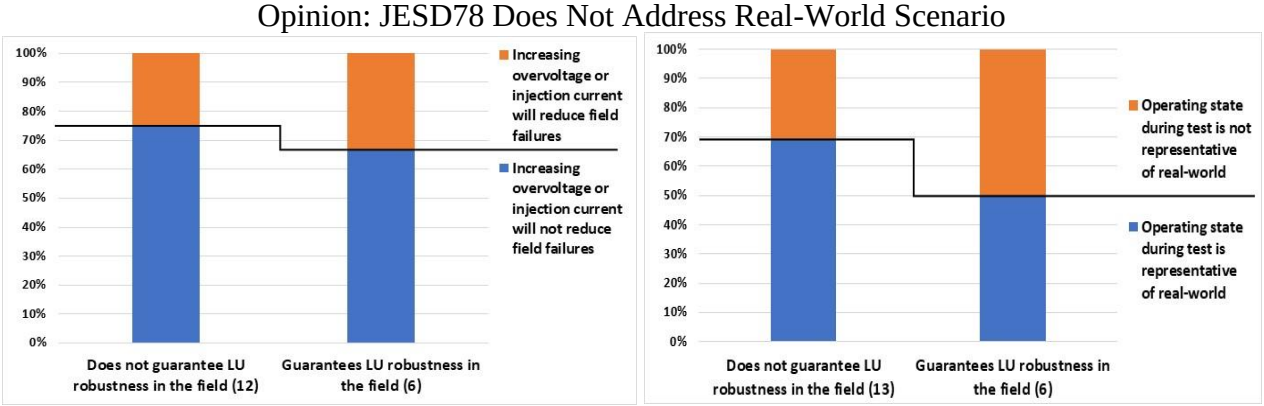


Figure 43 — Comparison of [Q41] with [Q37] and [Q38] for Respondent Thinking JESD78 Does Not Address Real-World Scenario

5.3.2 Expectations and Usefulness (cont'd)

Overall response ratio to [Q38] ("Is the operational state of an IC used during JESD78 testing (i.e., low power mode, stable current) representative of real-world applications?") is depicted in Figure 44. The situation amongst responders thinking JESD78 is a mimic of the real world is almost the same.

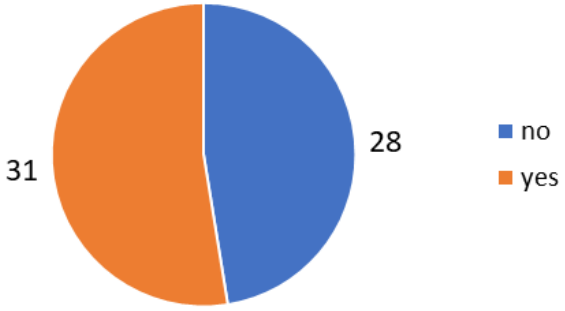


Figure 44 — Pareto of [Q38]

[Q38] "Is the operational state of an IC used during JESD78 testing (i.e., low power mode, stable current) representative of real-world applications?"

Looking to [Q38], almost half of the respondents pointed out that the operational state required by JESD78 is not representative for real world mainly because:

- Low power condition is not representative of a main operational state during the whole lifetime.
- Difficulties exist to replicate real-world operating conditions in a latch-up test scenario (clock, high frequency, decoupling passives, etc.).

Only a minority (8 out of 57), mainly from Automotive, claims to test according to the full IC operational mode. Consumer and Commodity products mainly stick to the minimum requirements of JESD78.

Possible Interpretation
Despite JESD78 being considered to mimic real-world scenarios by most of the respondents, the operational state during testing ("supply current must be stable enough and low enough to reliably detect the supply current increase if latch-up occurs") looks to be far from a real application. However, due to the practical difficulties in replicating operating conditions, only a few companies are and will be able to really explore all possible real-world situations.

5.3.3 Robustness in the Field

As already stated in the basic analysis more than half of the respondent state that JESD78 is not enough to guarantee robustness in the field ([Q41]). This is shown in Figure 45.

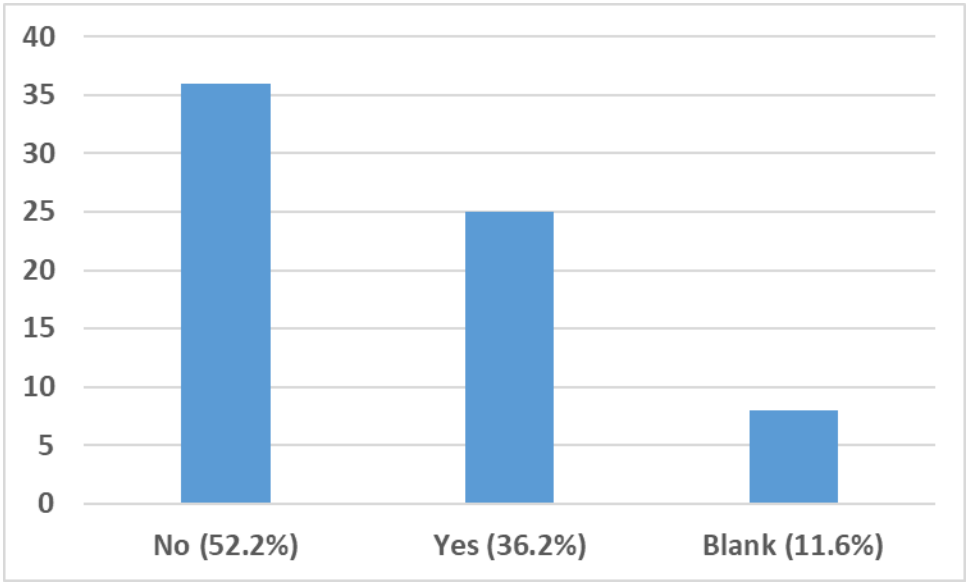


Figure 45 — Pareto of [Q41]

[Q41] "Does passing JESD78 testing guarantee latch-up robustness in the field?"

Except for Military (11 respondent), all other industry domains (Aerospace, Automotive, Consumer, Industrial, & Medical) had a higher percentage of "no" responses than "yes" responses indicating they are, in general, less confident that JESD78 is enough to guarantee robustness in the field as shown in Figure 46.

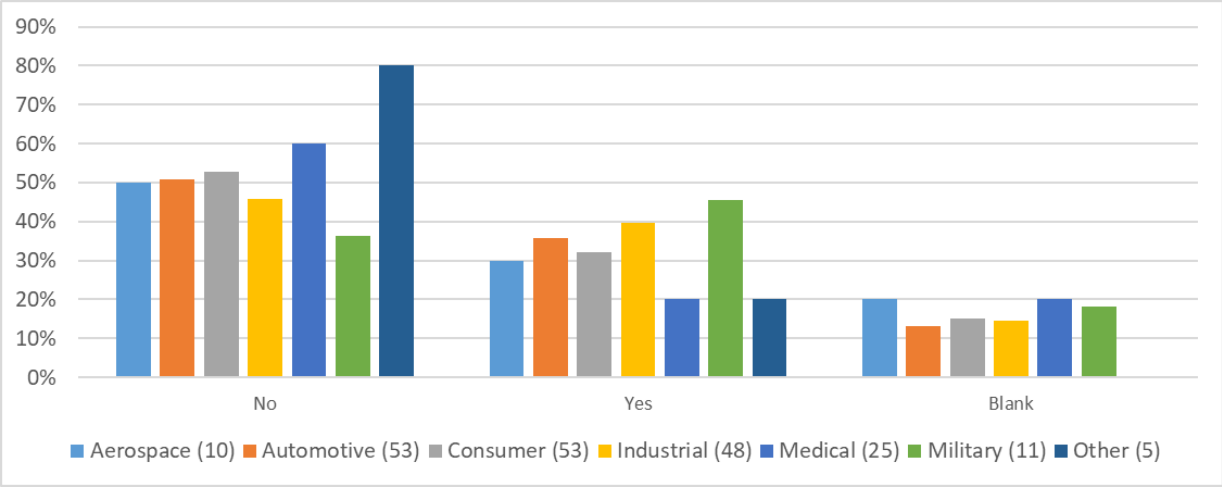


Figure 46 — Pareto of [Q41] by Industry Domain [Q03]

5.3.3 Robustness in the Field (cont'd)

[Q42] and [Q43] deal with tests needed and tests that are already done by a company to complement JESD78 in order to feel confident of latch-up robustness in the field. The results of those responses are shown in Figure 47.

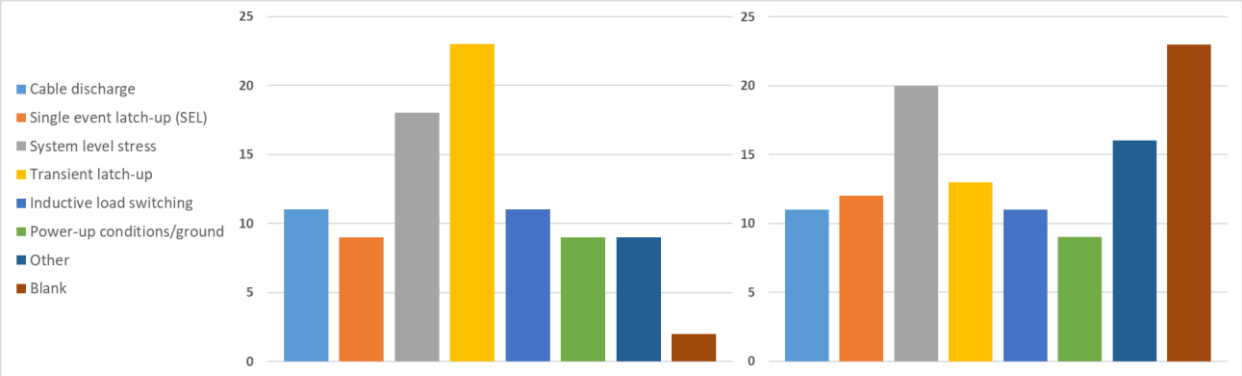


Figure 47 — Pareto of [Q42] (Left) and to [Q43] (Right) if the Answer to [Q41] is No

[Q42] "What other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?"

[Q43] "What other types of latch-up tests does your company perform to qualify a product?"

Both are multiple choice questions and the respondents for [Q42] are only those who think JESD78 is not enough to guarantee latch-up robustness in the field (36) while for [Q43] all respondents were asked to answer it (69).

The majority of [Q42] respondents (left graph of Figure 47) think transient latch-up is the most suitable device level test to complement JESD78, though it is probably the least represented waveform in the exiting JESD78 specification which is primarily a static latch-up test. A possible explanation is that this methodology covers different pulse time length and rise time. Next most popular option is system level stress; this can be explained because most of the respondent are already using this methodology.

Possible Interpretation
JESD78 does not cover pulses with very short rise times that are real world threats. To cover this gap, respondents suggest using TLU and system level stress.

Based on the right graph of Figure 47, 1/3 of the total respondents do not perform any other test to look for latch-up (looking at "Blank" – 23 over 69) and amongst those performing additional tests the most common tests are "System level stress" and those categorized as "Other". A possible reason to have many custom tests is that since there is not any defined standard except for system level stress, respondents would not like to assign a well-defined category; obviously it also counts all customer-specific tests.

5.3.3 Robustness in the Field (cont'd)

Making the split by industry, as shown in Figure 48, it looks as though all industries are aligned in the percentages requesting a different stress except for military, aerospace and other, but the confidence for them is quite low because of the number of respondents. On the other hand, the split by product type sold shows a good alignment as shown in Figure 49.

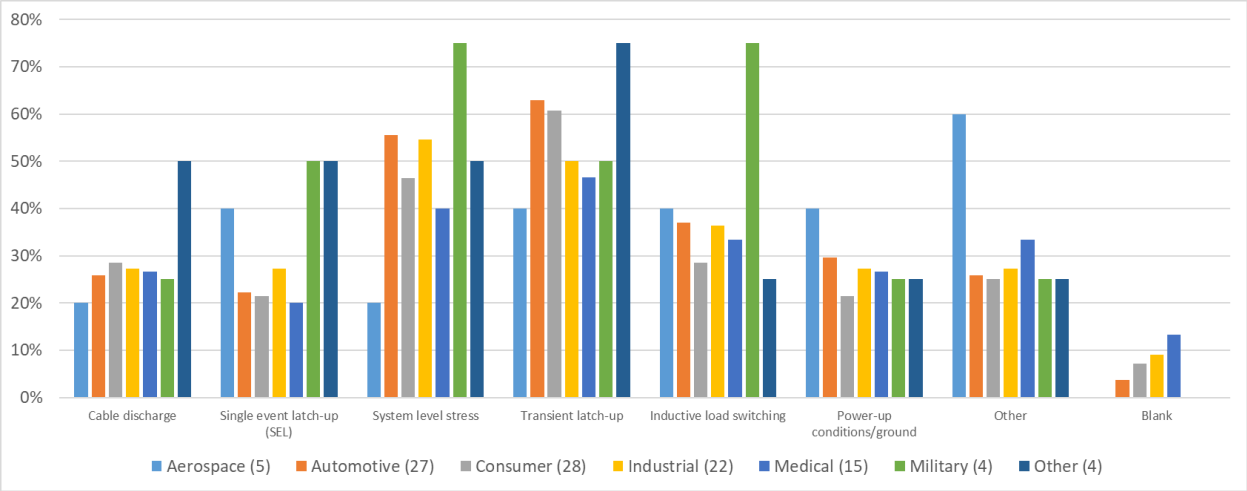


Figure 48 — Pareto of [Q42], if Answer to [Q41] is No, by Industry Domain [Q03]

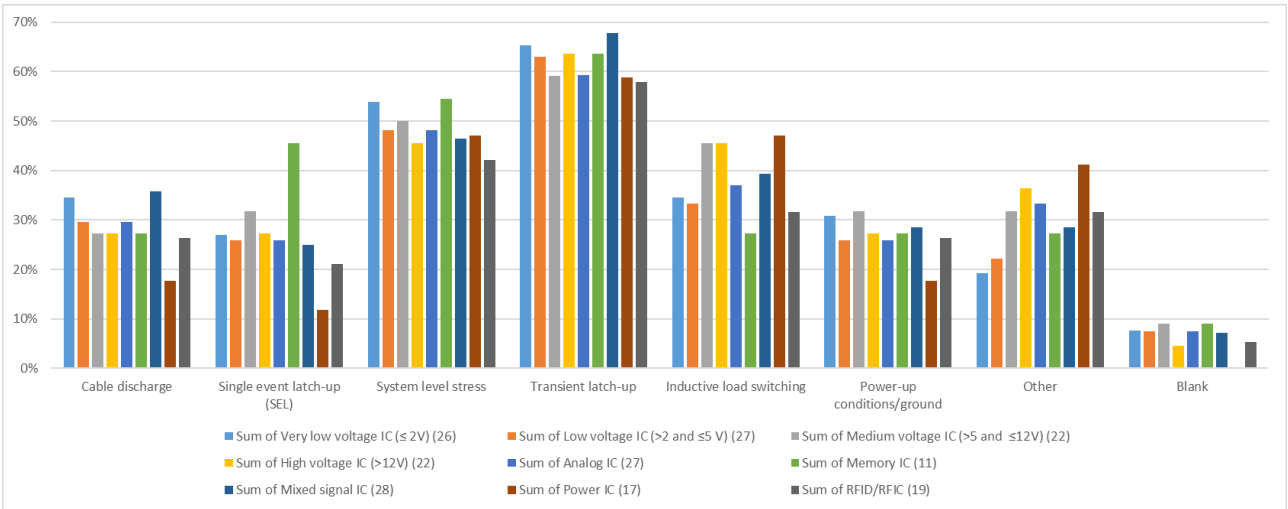


Figure 49 — Pareto of [Q42], if Answer to [Q41] is No, by Product Type [Q05]

Possible Interpretation
Despite all doubts that JESD78 guarantees robustness in the field, specific latch-up tests like transient LU and system level tests are only done by a minority of respondents in qualification.

5.3.4 Discussion

Since 78% (54 out of 69) answered [Q23] ("Is JESD78 testing a product qualification requirement in your company?) with "YES", we can assume that together with HBM and CDM, the JESD78 latch-up test is widely used as a standard test in product qualification. However, the JESD78 standard does not cover the whole range of possible events which can result in a latch-up condition.

Missing issues are:

- Latch-up which occurs in functional modes outside of the state required in JESD78 latch-up testing
- TLU at pins exposed to fast transient signals
- System level events at pins connected to the outside world

However, the survey reveals that even with incomplete coverage, the actual state of the JESD78 test is perceived to deliver a certain basic level of robustness to detect design weaknesses sensitive to unintended voltage/current spikes. While the JESD78 stress may not look like a real-world event:

- It can be used as benchmark.
- It can highlight some marginal designs not covered by EDA tools.
- It is currently the only recognized test to find latch-up susceptibility to current and voltages outside of normal operating conditions.

With the 100-mA threshold for the I-Test in discussion, a majority of respondents do not wish to increase the stress levels and regard 100 mA as sufficient. On the other hand, skipping the JESD78 test is believed to cause poorer reliability in the field. The 100-mA threshold seems to be a commonly accepted compromise between safety and effort!

JESD78 is therefore a good base for latch-up testing but wishes for additional test features like special functional modes, transient latch-up characterization at pins exposed to fast transient signals and system level stress at pins connected to the outside world were expressed. JESD78 seems to have a high level of acceptance – since it is the best right now.

Possible Interpretation
The actual stress conditions (100 mA injection, 1.5 x V_{DDmax} at supply stress) seem to be the "Golden Compromise" between reliability and effort.

5.3.5 Future

The majority of the respondents consider the method relevant, even with significance beyond the boundaries of the applied waveforms. Nevertheless, significant reservations to the usefulness are listed ([Q09]), and roughly, 50% of the responses indicate that JESD78 alone is insufficient ([Q49], [Q50]). See Figure 50 for a distribution of suggestions.

- About half say JESD78 is not sufficient
- Many answering "Yes" at [Q49] suggest that transient latch-up (TLU) and system level stress are needed in addition
- Majority indicates that the current JESD78 levels are suitable as minimum requirements

5.3.5 Future (cont'd)

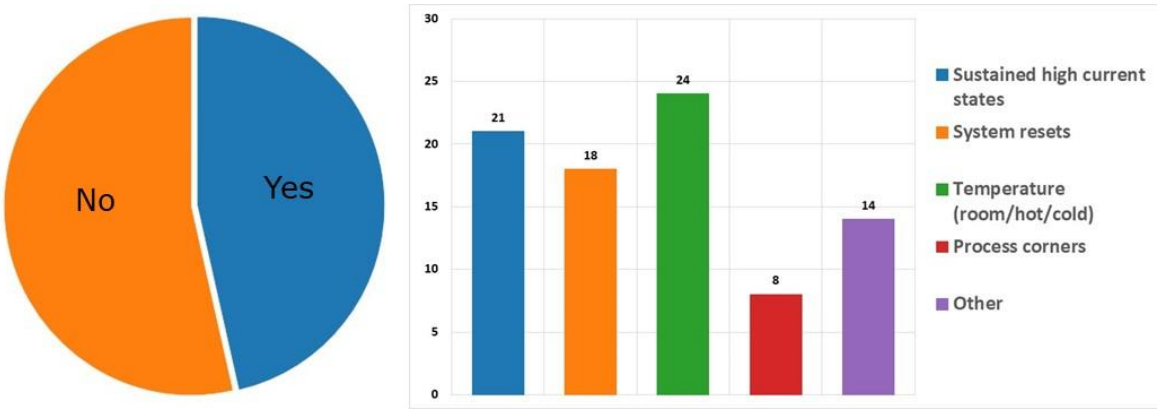


Figure 50 — Responses to [Q49] (Pie Chart) and [Q50] (Pareto)

[Q49] "Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?"

[Q50] "Which conditions should be included in this new test method(s)?"

Opinions differ upon the question if new latch-up testing methods should be developed in the future [Q44], see Figure 51:

- A majority of 75% want to keep the JESD78 test, but only 13% want to avoid adding any new adjustments.
- A significant number of respondents, 61%, want to stay with JESD78, but wish to modify the test settings or add new standards.
- Only 11% want to replace JESD78 by a new test method.

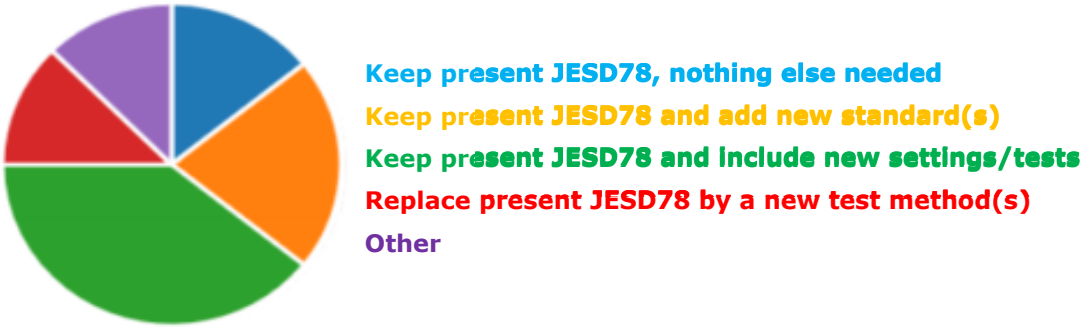


Figure 51 — Pie Chart of [Q44]

[Q44] "If new latch-up testing methods were to be developed in the future what would be your preference?"

Possible Interpretation
JESD78 is a good base for future tests, but respondents wish for modifications in the test method and settings.

5.4 Next Steps of Latch-up Testing

This clause discusses responses to questions that are related to the execution of JESD78 testing in a broad sense. Topics that will be discussed include questions on test settings, verification of test programs, and the identification of needs for latch-up test improvements. In particular, this part of the analysis deals with the responses to [Q43] through [Q56] of the survey, which are:

- [Q43] What other types of latch-up tests does your company perform to qualify a product? (Also discussed in Clause 5.3.3)
- [Q44] If new latch-up testing methods were to be developed in the future what would be your preference? (Also discussed in Clause 5.3.5)
- [Q45] Often, power supplies in applications are not capable of sinking current and can only source current. Such supplies would limit positive injection current into the I/O pin in the application. Should the standard take into account the ability of a supply to sink current when defining current injection level for qualification?
- [Q46] If a JESD78 stress condition results in a sustained decreased current, should it be considered as a JESD78 failure reason?
- [Q47] Which of the following circuit elements, if turning on and causing the sustained increased current, should be considered JESD78 failure reasons?
  - [Q48] If you selected 'Other latching circuitry', please give examples of latching circuits that should be considered a failure in the above situation.
- [Q49] Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause? (Discussed in Clause 5.2.3 and Clause 5.3.5)
- [Q50] Which conditions should be included in this new test method(s)? (Discussed in Clause 5.3.5)
- [Q51] As the supply voltage of ICs keeps shrinking, below about 2 V the 100-mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Does this lead to latch-up risks in the application?
  - [Q52] If yes, please specify why
- [Q53] At what minimum JESD78 current injection level are your company's products safe for final application?
  - [Q54] Please specify the above answer
- [Q55] At what minimum JESD78 overvoltage level are your company's products safe for final application?
  - [Q56] Please specify the above answer

5.4.1 Types of Latch-Up Tests Performed by the Industry

It is possible to split up the tests already performed by industry [Q43], grouping it by test (Figure 52) or by industry (Figure 53); both will give the same result, but these two points of view can help to have the data more easily readable. From the first Pareto it looks clear that high reliability industries (Aerospace, Military and Medical) are doing more stresses than the others with the only exception of single event latch-up (SEL) and power up test. It is also easy to understand that in these industries there are very specific trials not covered by any standard that may depend on customer request or that are dedicated to specific applications. Comparing the ratio of tests done using the second Pareto it looks that for all Industries system level and custom (other) stress are dominant except Aerospace and Military Industries where transient and inductive load switching are at the same level than the other top two.

5.4.1 Types of Latch-Up Tests Performed by the Industry (cont'd)

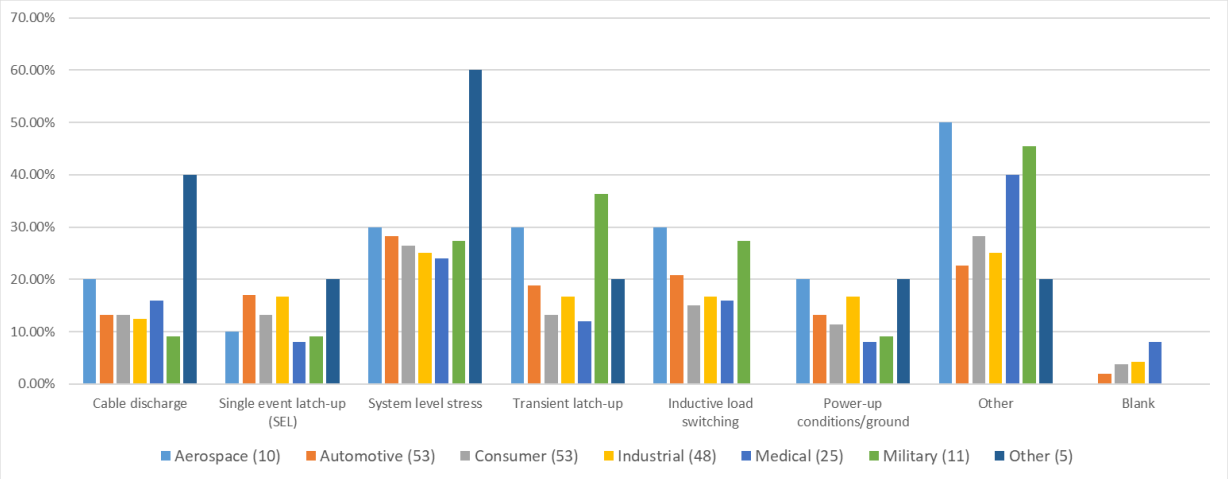


Figure 52 — Pareto of [Q43] by Industry Domain [Q03] Grouped by Test

[Q43] "What other types of latch-up tests does your company perform to qualify a product?"

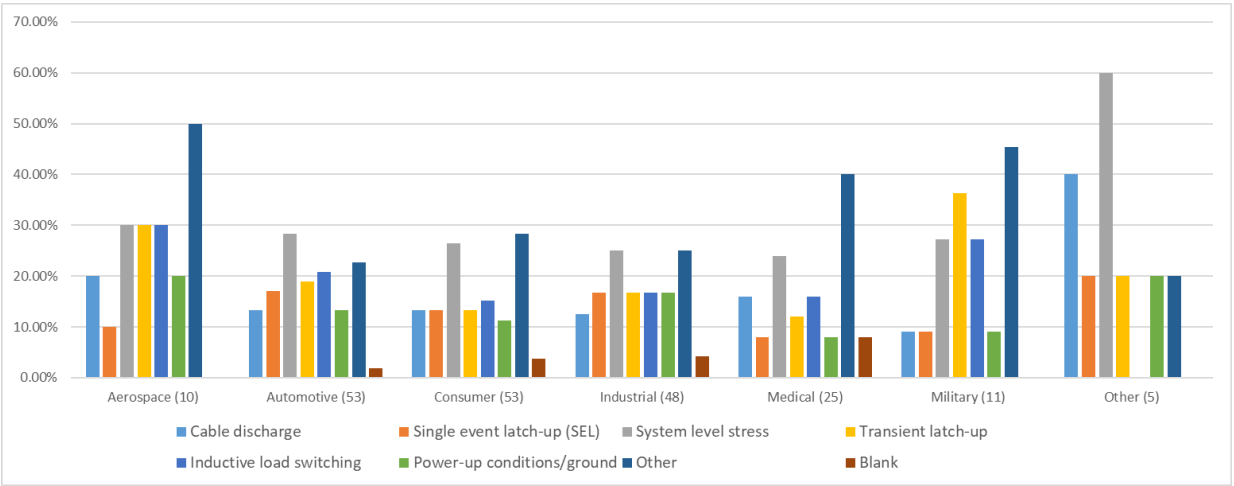


Figure 53 — Pareto of [Q43] by Industry Domain [Q03] Grouped by Industry

As shown in Figure 54, applying the split by product type, it appears clear that almost 45% of companies selling Memory ICs (8 of 19) do not perform any other stress than JESD78 (Blank) for latch-up robustness in the field although 11 of them stated that JESD78 is not enough to guarantee robustness in the field. On the other hand, almost all others (9 of 11) are doing system level stress as a required test for their product.

System level is the most common test for all (perhaps because there are already IEC and ISO standards that are mandatory for system qualification). After system level the second place depends on application. Low, very low voltage and RF applications look to be more attracted by SEL and Other. Medium, high voltage and power IC applications require passing tests related to inductive switching and transient. For mixed signal and analog, all stresses are equally performed. This can be due to both market and application specific requirements.

5.4.1 Types of Latch-Up Tests Performed by the Industry (cont'd)

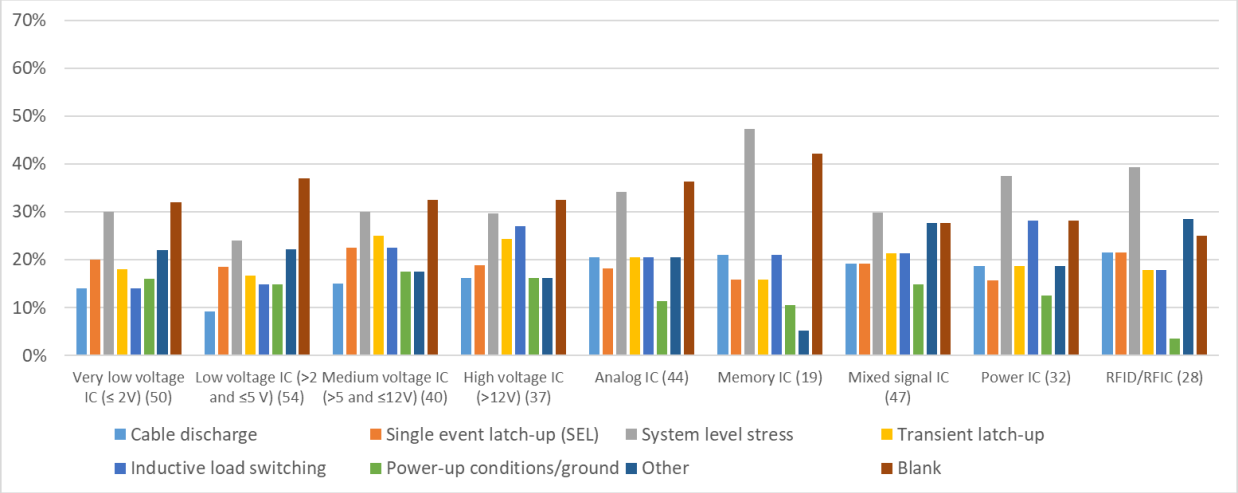


Figure 54 — Pareto of [Q43] by Product Type [Q05]

It is possible to show two additional correlations between [Q42] and [Q43]. How many respondents applying a certain stress think it is useful to prevent latch-up in the field (see Figure 55) and how many respondents suggesting for a test are using it for qualification (see Figure 56).

Surprisingly, the vast majority of the respondents do not suggest the stress that they are applying is a good candidate for complementing JESD78. This can be explained in some way because either some stresses are very specific to certain applications or because respondents think the test is valuable, but not related to latch-up in application.

In the same way the result of respondents suggesting a methodology and using it for qualification are somehow lower than expected, this result can be explained in a very simple way - since there is not any defined standard at the device level (the vast majority of respondents are from IC supplier) for testing an IC against latch-up, except for JESD78, the industry simply does not apply them except for customer specific requests that can fall in a certain category.

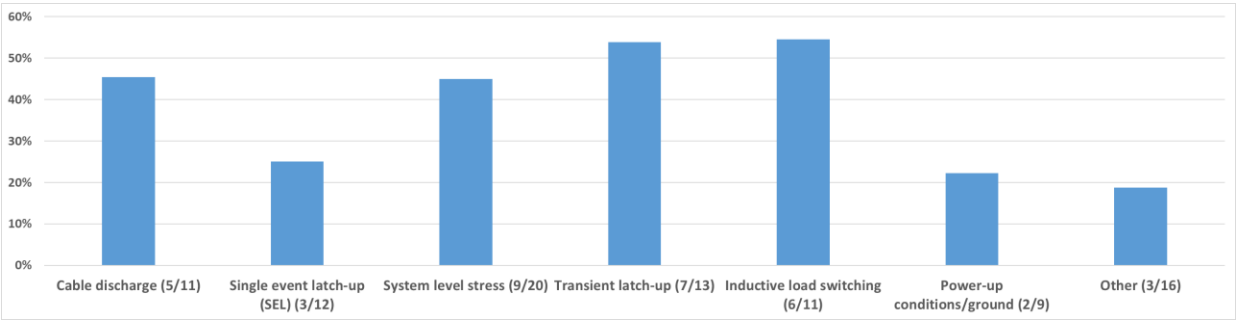


Figure 55 — Percentage of Respondent Already Applying a Certain Stress [Q43], Thinking it is Useful to Complement JESD78 [Q42]

5.4.1 Types of Latch-Up Tests Performed by the Industry (cont'd)

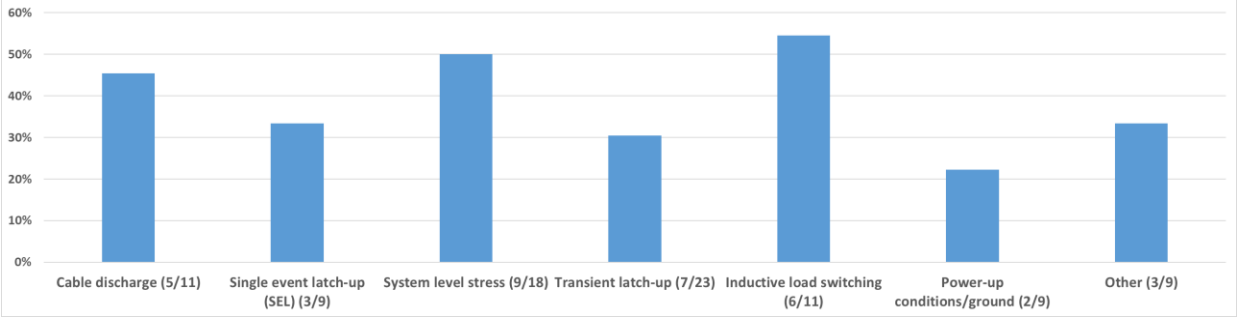


Figure 56 — Percentage of Respondent Suggesting for a Stress [Q42] and Already Applying it for Qualification [Q43]

5.4.2 Failure Criteria and Maximum Stress Voltage ("MSV")

A topic of debate in the latch-up community is the definition of latch-up. Historically, latch-up is associated with the presence of a parasitic thyristor. [Q47] asked for circuit elements that should be considered as valid sources for the latch-up phenomenon. From the responses, it can be seen that:

- There is an overwhelming consensus that failure criteria should change.
- There is a significant disagreement on what should/should not be a 'failure'.

This is illustrated in Figure 57, where it can be concluded that the majority considers that the definition should be much wider. A significant group of respondents agrees with the generic definition 'anything that causes increased supply current'.

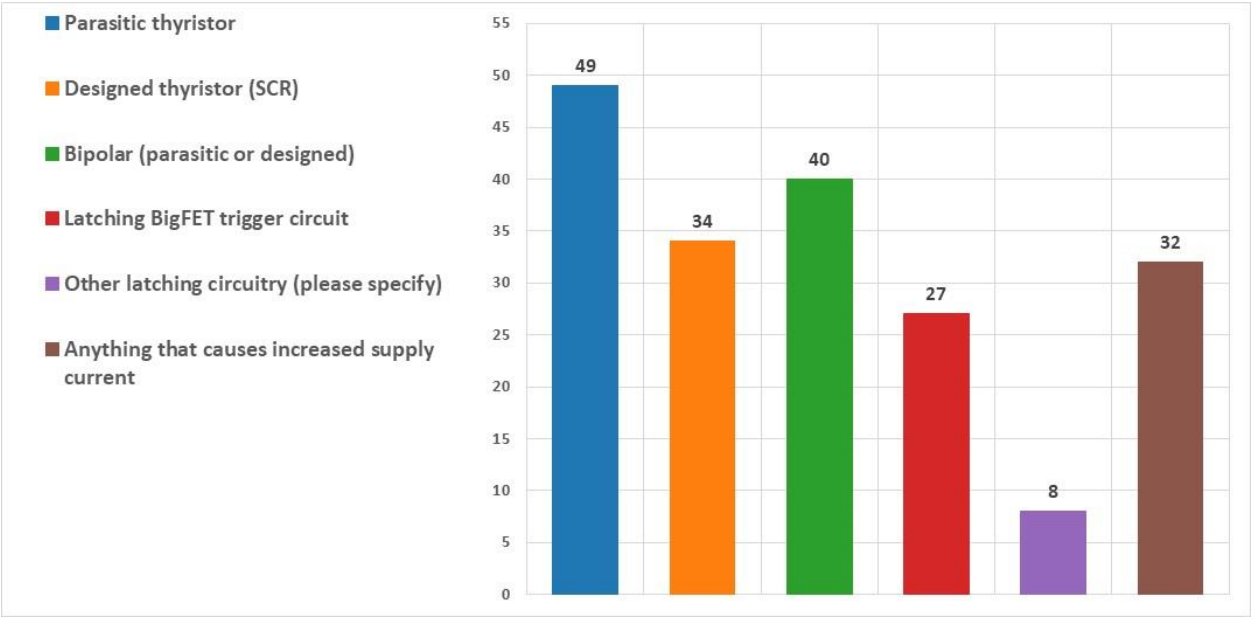


Figure 57 — Pareto of [Q47]

[Q47] "Which of the following circuit elements, if turning on and causing the sustained increased current, should be considered JESD78 failure reasons?"

5.4.2 Failure Criteria and Maximum Stress Voltage (cont'd)

There is considerable disagreement on what should and should not be considered a latch-up failure, but only 5% of the responses stated that current criteria (JESD78F) were sufficient.

MSV is defined as the maximum voltage allowed during latch-up testing to avoid "irreversible damage to the device from a catastrophic breakdown of the silicon device or circuit not related to latch-up". Because latch-up is defined as a sustained low impedance state resulting from the triggering of (exclusively) "a parasitic thyristor structure", any other cause of a destructive low-impedance state may be used as a justification to reduce the voltage applied during the stress by invoking the MSV for the JESD78 test plan. For example, MSV can be invoked to prevent the triggering of single NPN or PNP parasitic bipolar. Referring to Figure 57, a significant number of respondents (40) selected "Bipolar (parasitic or designed)" as valid causes for a JESD78 failure. Because any circuit element considered a failure reason cannot also be used to invoke MSV, one would expect that the same group would find bipolar snapback unacceptable to invoke MSV ([Q88]). However, no such correlation was found.

5.4.3 Injection Levels and Low-voltage Pins

[Q53] and [Q55] poll on minimum current injection and overvoltage requirements that make the product safe for final application. 2/3 of the respondents think that the 100 mA and 1.5 times overstress are the minimum safety requirements. A distant second group suggests that safe levels should be pin function dependent. Answers with a lower or higher value scored less in all cases. This is somewhat in contrast to the responses on [Q51] "As the supply voltage of ICs keeps shrinking, below about 2 V the 100-mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Does this lead to latch-up risks in the application?". The responses are depicted in Figure 58 and show that 2/3 of the respondent's think it is NOT a risk if the intended 100 mA cannot be injected because of a clamping voltage limit, considering the respondents that were aware of this situation.

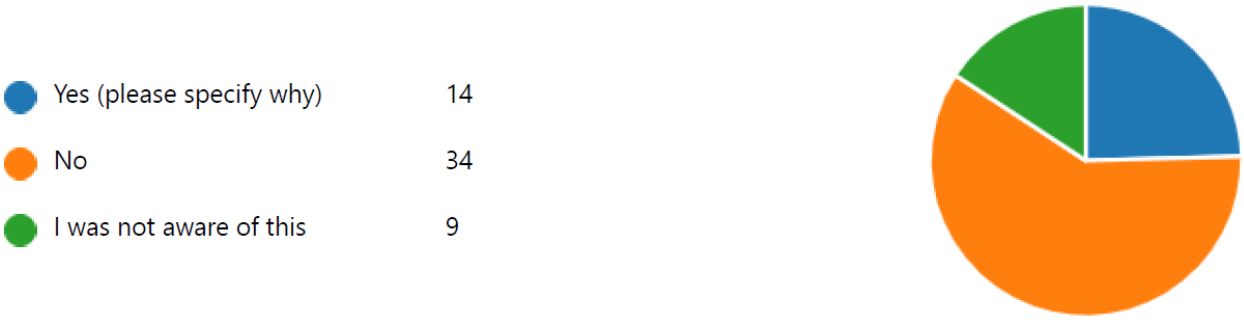


Figure 58 — Pie Chart of [Q51]

[Q51] "As the supply voltage of ICs keeps shrinking, below about 2 V the 100 mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Does this lead to latch-up risks in the application?"

For those that answered, "I was not aware of this", they rarely encountered such pins (correlation with [Q89]: 56% versus 26% baseline).

5.4.3 Injection Levels and Low-voltage Pins (cont'd)

For those that answered "Yes" to [Q51], a summary of the reasons that were provided as write-in responses are listed below. They ranged from strong statements at the top of the list to more tempered reasons at the bottom:

- There is a risk of not detecting a latch-up weakness in the product because the system noise can be higher than the voltage clamping limit.
- The risk of latch-up should be evaluated based on the application (e.g., hot plug).
- The risk of not detecting latch-up for pins operating at 2 V and below is relatively low due to the inherently strict design constraints.

For those that answered yes, the following correlations were found:

- Were more likely to have experienced latch-up related EIPD for parts that passed the JESD78 test (correlation with [Q22]: 64% versus 39% baseline).
- Believed that JESD78 in its current form would not be the preferred future test standard (correlation with [Q44]: 0% versus 14% baseline)
- Believe latch-up occurring during the stress pulse could be considered a failure depending on the specific scenario/application (correlation with [Q91]: 50% versus 32% baseline)
- Believe latch-up design rules should be exclusively driven by an improved version of JESD78 (correlation with [Q61]: 71% versus 47% baseline)
- Believe AMR is not applicable to latch-up (correlation to [Q90]: 62% versus 31% baseline).

That same group was more likely to disagree with the following statements:

- The operational state of an IC used during JESD78 testing is representative of real-world applications (correlation with [Q38]: 64% versus 47% baseline)
- Passing JESD78 testing guarantees latch-up robustness in the field (correlation with [Q41]: 77% versus 61% baseline).
- Design rules should be relaxed for pins operating at under 2 V (correlation with [Q63]: 14% versus 34% baseline)
- Under any scenario, latch-up occurring during a stress pulse would not be considered a failure (correlation with [Q91]: 21% versus 37%)

Possible Interpretation
Those that believe limiting current injection for low-voltage pins (as described in JESD78 in its current form) falls short of being a comprehensive test for all possible ways in which latch-up can be induced in the field look for other ways to address the gap.

Notably absent was a strong positive correlation between those that answered "Yes" to [Q51] and those that test beyond the Table 2 limits ([Q81] and [Q83]).

5.4.4 Application Specific Execution

Many of the questions in the survey ask if the latch-up test standard is sufficient to cover all pin applications. This is evident in [Q42] "If no, what other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?" where the response listed 6 different stress methods with more severe, application specific stimulus, selected by 36 respondents who think JESD78 is not enough to guarantee latch-up robustness in the field.

In contrast, [Q45] highlights that often, power supplies in real-world applications are not capable of sinking current and can only source current. Such supplies could limit positive injection current into the I/O pin in the real-world application. This would make the real-world latch-up risk less severe for some applications than the latch-up standard. The question asks whether the test standard should consider the ability of the application supply to sink current as part of the I-test and adjust if the power supplies in applications are not capable of sinking current and can only source current. A large majority (66%) of respondents answered "Yes" to this question, this is shown in Figure 59.

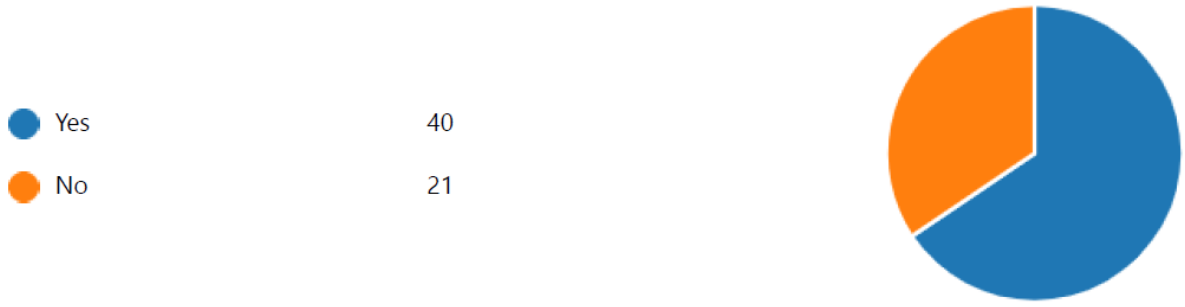


Figure 59 — Pie Chart of [Q45]

[Q45] "Should the standard take into account the ability of a supply to sink current when defining current injection level for qualification?"

Of this "Yes" majority, over half also selected > 100 mA current injection level as the minimum level for company's products safe for final application in [Q53], and 88% indicated that components would be less reliable in the field without JESD78 in [Q32].

It is notable to cross reference the "Yes" majority in [Q45] with [Q13]. [Q13] asks "*Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?*". 50% of the responders who selected YES in [Q45] also answered Yes to [Q13], compared to only 28% of the responders who selected No to [Q45].

Possible Interpretation
Pin application specific injection levels can be higher or lower than the general practice in a company. The majority of respondents currently may disposition pins as safe with a lower injection threshold given the application.

5.4.4 Application Specific Execution (cont'd)

In the write-in comments at the end of the survey, several of the responders who answered "Yes", also called for application specific considerations in stress current.

- "Does the current level (100 mA) still make sense for I/O pins of 2 chips mounted on the same board? Should 100 mA be limited to a hot plug application or external interfaces (not on same board)?"
- "Clarity on how to test the special pins like RF pins, RF pins and voltage regulator / reference"

Referring to [Q44], of the 61% who indicated that JESD78 should be kept and enhanced in the future, there was a majority of respondents who answered "Yes" in [Q45], also preferred to enhance JESD78 with modified test settings, compared to augmenting with new standards.

In summary, a majority of respondents indicate that the risk of latch-up at a pin should be related to the ability of the power supply driving the pin to supply that current.

5.5 Reporting and Design Rules

This part of the analysis deals with the responses to [Q57] through [Q65] of the survey, which are:

- [Q57] How does your company report latch-up test results to customers?
- [Q58] Does the latch-up robustness level given in the datasheet of an IC impact the purchase decision?
  - [Q59] If only for certain applications, please specify which type of applications
- [Q60] What is the most common action that your company takes in case of JESD78 failure?
- [Q61] Should latch-up IC design rules be exclusively driven by the JESD78 requirements?
  - [Q62] If no, please explain why not
- [Q63] As the supply voltage of ICs keeps shrinking, below about 2 V the 100-mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Should design rules be relaxed in such scenario?
  - [Q64] Please specify the above answer
- [Q65] If you pass all latch-up design rules, what does it guarantee?

5.5.1 Reporting

[Q57] asked about reporting of latch-up results. Most of the respondents (about 67%) indicated that latch-up results get reported in qualification reports. Only about 25% of the respondents said they reported the results in their product datasheets, see Figure 60.

With regards to the reporting style, about 60% of the respondents only report passing JESD78. A much smaller number (about 17%) of the respondents also report the achieved immunity level (per the classification provided in the JESD78 standard); and an even smaller number (about 10%) of respondents additionally report the achieved injection current and overvoltage voltage levels.

5.5.1 Reporting (cont'd)

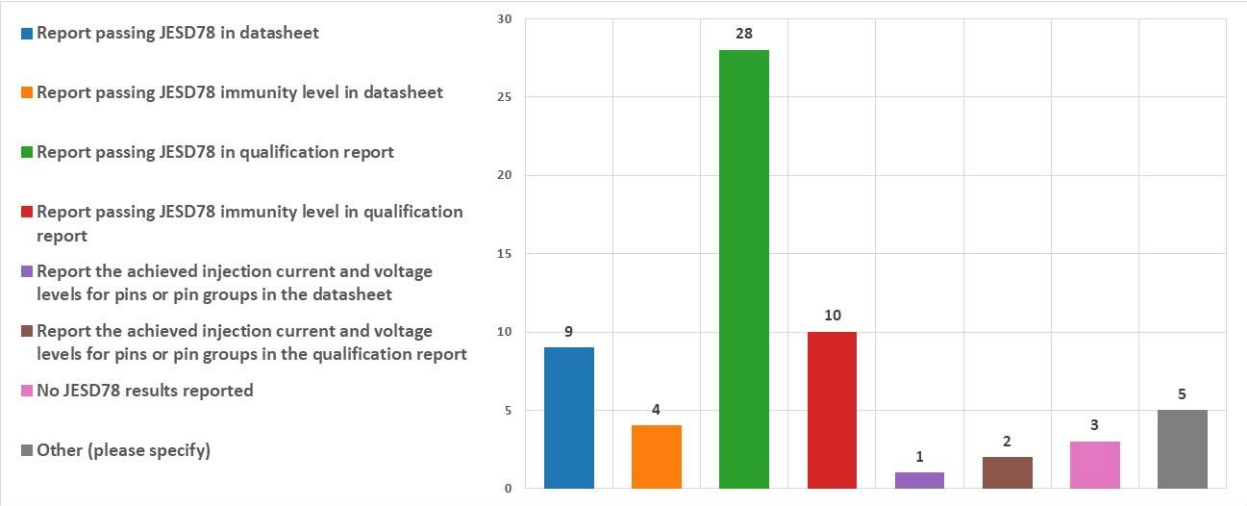


Figure 60 — Pareto of [Q57]

[Q57] "How does your company report latch-up test results to customers?"

Figure 61 shows the responses to [Q58], which asked about impact of the stated latch-up robustness of an IC on the purchase decision. Only about 28% of the respondents said that it would not impact the purchase decision. Two of the write-in answers indicated that automotive applications may be more impacted than others.

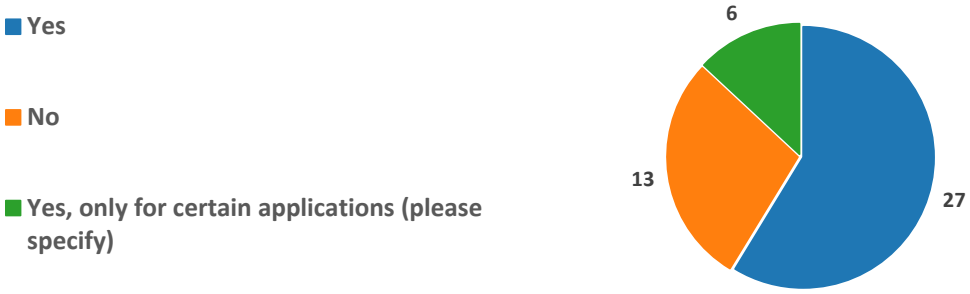


Figure 61 — Pareto of [Q58]

[Q58] "Does the latch-up robustness level given in the datasheet of an IC impact the purchase decision?"

Respondents to [Q58] who said they did not believe that the latch-up robustness level provided in an IC's datasheet would impact the purchase decision were more likely (70% vs. 31% baseline) to agree that JESD78 compliance is just a check box item, and that detailed JESD78 results are not needed (see [Q34]). They also tend to have a stronger belief (40% vs. 21% baseline) that JESD78 test results provided in an IC supplier datasheet or qualification report are not used for system design (see [Q36]). A lot of them (82% vs. 67% baseline) also think that increasing the overvoltage or injection current levels of JESD78 would not decrease the latch-up failures in the field (see [Q37]). They are also more likely (78% vs. 63% baseline) to strictly apply Table 2 voltage limits for low voltage (LV) signal pin testing (see [Q81]), even if this results in little or no current injected during latch-up testing.

5.5.1 Reporting (cont'd)

Figure 62 shows the results of [Q60] which asked about the most common action in case of JESD78 failures. Most of the respondents said they would fix the issue in a design revision.

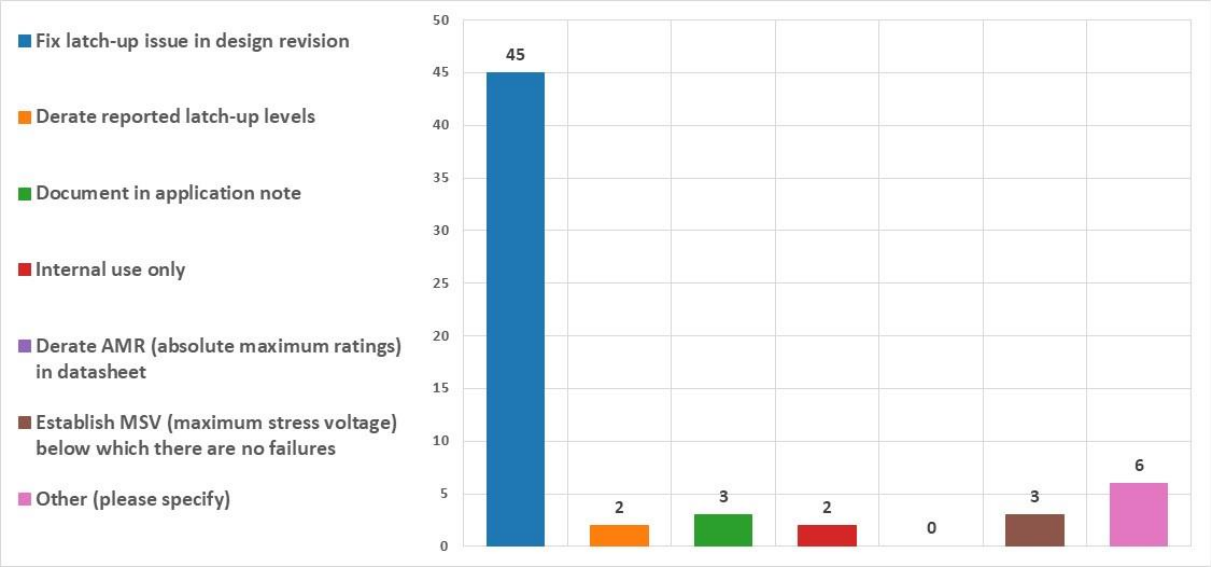


Figure 62 — Pareto of [Q60]

[Q60] "What is the most common action that your company takes in case of JESD78 failure?"

5.5.2 Design Rule Relationship to JESD78

Design rules that govern (typically) the layout implementation of circuits are often derived from the stimuli prescribed by JESD78. For that reason alone, these topics are linked and as a result any change, interpretation, or misinterpretation of the test standard can have a direct impact on design rules derived from it.

As an example, [Q63] poses the question as to whether design rules should be relaxed due the current injection reduction for supply voltages below 2 V. Rules taking this reduction into account can result in designs with a reduced layout footprint and routing resources necessary to pass the qualification.

The responses to [Q63] were split approximately evenly among three groups: an unequivocal "Yes", "It depends on the application", and an unequivocal "No" this is shown in Figure 63. Grouping the "No" with the "It depends on the application" results in 39 of 61 (64%) with at least some reservations for relaxing design rules in this scenario. [Q61] asks the question more broadly by asking "Should latch-up IC design rules be exclusively driven by the JESD78 requirements?", this is shown in Figure 64. By combining the "No" responses with the "Yes with future improved JESD78 specification", the exact same proportion of respondents [39 of 61 (64%)] believe that JESD78 in its current form should not be the exclusive driver of latch-up design rules.

5.5.2 Design Rule Relationship to JESD78 (cont'd)

When asked in [Q65] "If you pass all latch-up design rules, what does that guarantee?", 44 of 61 (72%) respondents selected "Pass JESD78 testing", this is shown in Figure 65. This result suggests that (1) the latch-up design rules for most respondents are driven by the JESD78 test method and targets, and (2) the majority of respondents do not extend the relevance of the JESD78 standard to cover all possible sources of latch-up triggering in the final application. The latter point is reinforced by the very small number of respondents, 7 of 61 (7%), that selected "No latch-up issues in the system"

These results are approximately aligned with the "No" responses to [Q41] ("Does passing JESD78 testing guarantee latch-up robustness in the field?), which was 37 of 62 (60%).

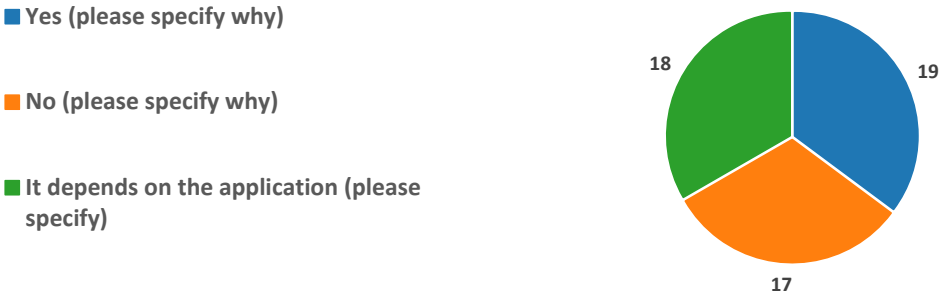


Figure 63 — Pie Chart of [Q63]

[Q63] "As the supply voltage of ICs keeps shrinking, below about 2 V the 100 mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Should design rules be relaxed in such scenario?"

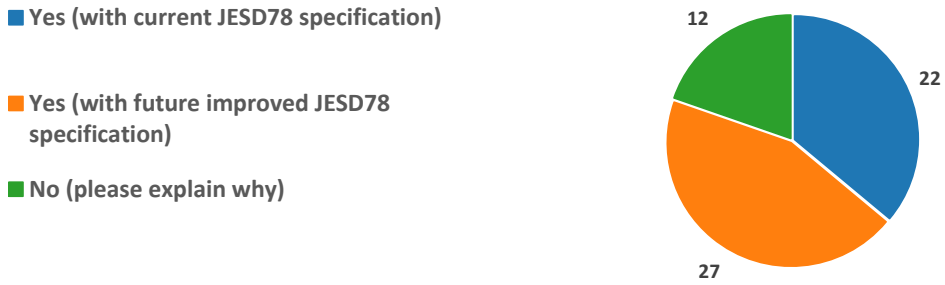


Figure 64 — Pie Chart of [Q61]

[Q61] "Should latch-up IC design rules be exclusively driven by the JESD78 requirements?"

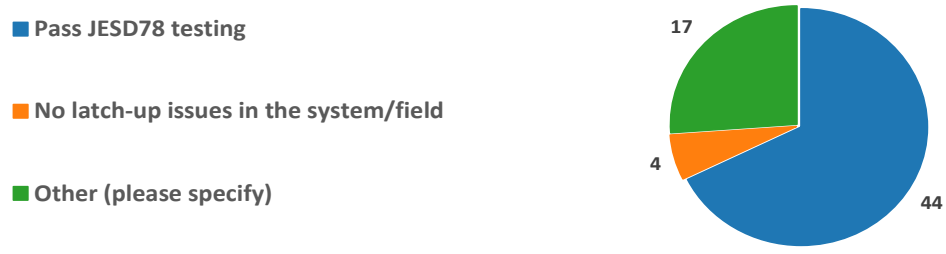


Figure 65 — Pie Chart of [Q65],

[Q65] "If you pass all latch-up design rules, what does it guarantee?"

5.5.2 Design Rule Relationship to JESD78 (cont'd)

To gain insight into the motivation of the responses to [Q61] and [Q63], the write-in responses were analyzed and summarized below.

Analysis of the write-in responses for those that answered "No" to [Q61]:

- Additional rules needed for application-specific cases with faster/higher voltage and current transients.
- Design rules should be driven by real-world applications and stress events.

One respondent indicated that currently the latch-up rules are driven by JESD78 but there are efforts underway to expand the rules to cover latch-up triggering conditions outside of JESD78.

Analysis of the write-in responses to [Q63]:

The "Yes" response justifications can be summarized as:

- To avoid over-design and reduce layout overhead necessary to meet ±100 mA.
- Low-voltage pins have an inherently low-risk environment for latch-up triggering.
- Low voltage devices themselves have some inherent level of latch-up immunity.
- Low voltage devices will suffer permanent damage before reaching ±100 mA.

The "No" responses justification can be summarized as:

- A minimum robustness level should be ensured through design rules independent of the voltage.

There is a consensus that JESD78 does not cover all possible mechanisms of latch-up triggering in a final application and therefore design rules for latch-up should not be limited to the stress conditions prescribed by JESD78.

For the specific case of low-voltage pins, write-in responses suggest that this class of interface has a lower risk of latch-up triggering due to both environmental conditions as well as the devices themselves and that design rules should reflect this to allow for more compact layouts. However, there is a concern that design rule relaxation for low-voltage pins will result in interfaces that do not meet a minimum robustness level.

5.6 Test Execution Details

This clause discusses the responses to questions that are related to execution of JESD78 testing in a broad sense. Topics that will be discussed include questions on latch-up test setup, verification of test programs, part response coverage, and special pin considerations. It is the responses to [Q66] through [Q84] of the survey, which are dealt with in this part of the analysis:

- [Q66] The JESD78 standard requires the following clamping limit to be applied during overvoltage testing:

  (a) I_{clamp} = 100 mA + I_{nom}, or

  (b) I_{clamp} = 1.5 x I_{nom}, whichever one is higher. Does your company follow this requirement?
  - [Q67] Please specify the above answer
- [Q68] At what maximum temperature does your company perform JESD78 testing?
  - [Q69] In case of 'it depends', please specify the above answer.

5.6 Test Execution Details (cont'd)

- [Q70] Which latch-up standard does your company use?
  - [Q71] If you selected 'Older JESD78 or 'AEC Q100-004', please specify the above answer
- [Q72] Which pin types should be exempt from JESD78 testing?
- [Q73] Which pulse duration do you select during JESD78 testing?
  - [Q74] Please specify the above answer
- [Q75] What information is needed to create a JESD78 compliant stress test program?
- [Q76] Do latch-up tester data logs (current and voltage) get reviewed in your company?
- [Q77] How do you systematically ensure that JESD78 testing is executed properly?
- [Q78] What do you systematically measure/monitor during JESD78 testing?
- [Q79] How do you measure/monitor the parameters you selected above?
- [Q80] How does your company test products with signal pins that are exposed to external energy paths (e.g., USB; HDMI; etc.) or have an inductive load?
- [Q81] For low-voltage (LV) signal pins, the applicable voltage clamping limits of JESD78, Table 2 may reduce the injected current below the set target level (e.g., ± 100 mA). With a maximum supply voltage below about 2 V, the injected current may even become zero. Do you strictly apply the Table 2 voltage limits?
  - [Q82] Please specify the above answer
- [Q83] If you characterize LV pins beyond the voltage limits of JESD78, Table 2, do you apply this extended test method for product qualification and document the extended spec limits in the latch-up report?
- [Q84] Do you setup the JESD78 test program to check if the injected signal pin itself suffered from latch-up ("signal pin latch-up")?

5.6.1 Scope of Latch-up Standards

Although the survey was oriented towards Revision E of the JESD78 standard, it is of course relevant to know which standards are actually used. Figure 66 shows that although other test standards and older JESD78 revisions are also used, the most prevalent standard in use is JESD78E. All respondents provided a version for AEC Q100-004 named revision D, which is almost identical to JESD78E. Others stated they use JESD78E or AEC Q100-004_revD depending on what the customer asked for. From [Q23] we conclude that for almost all respondents JESD78 testing is a product qualification requirement.

These replies give good confidence in the relevance of the responses with respect to the survey's goals.

5.6.1 Scope of Latch-up Standards (cont'd)

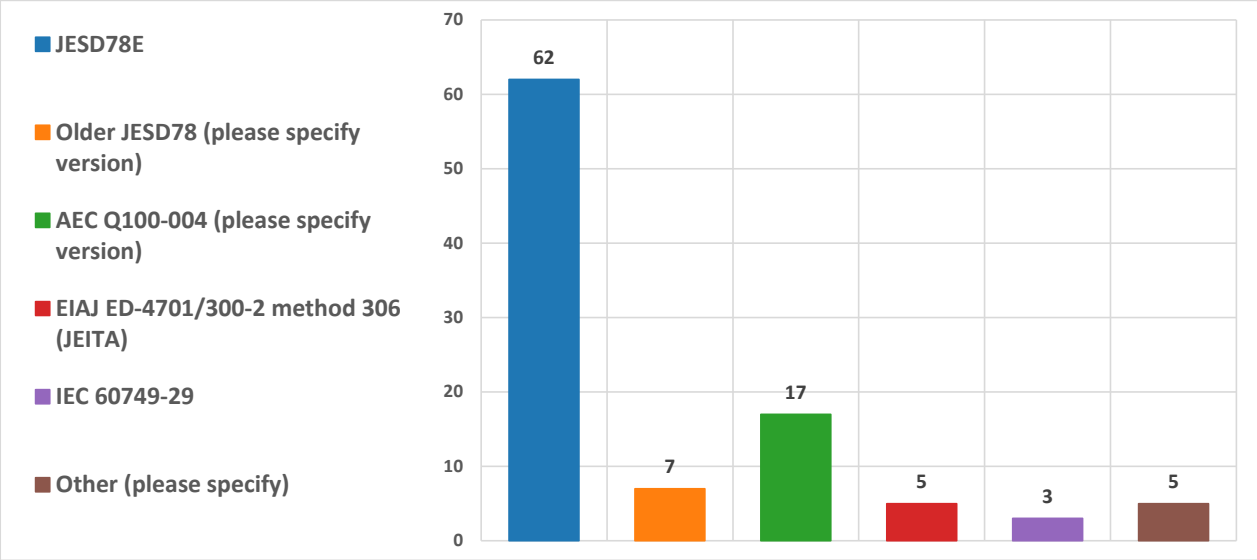


Figure 66 — Pareto of Latch-Up Standards [Q70]

[Q70] "Which latch-up standard does your company use?"

5.6.2 Testing Specification

The JESD78 standard requires the following clamping limit to be applied during overvoltage testing:

(a) I_{clamp} = 100 mA + I_{nom}, or

(b) I_{clamp} = 1.5 x I_{nom}, whichever one is higher.

Of those who answered [Q66] on current clamping, 91% use current clamp for overvoltage as specified by the JESD78 specification for all supplies (72%) or only for PUT (19%). Only 8% use a higher current clamp for supplies, typically this is for special applications. Figure 67 gives a graphical representation of the responses.

5.6.2 Testing Specification (cont'd)

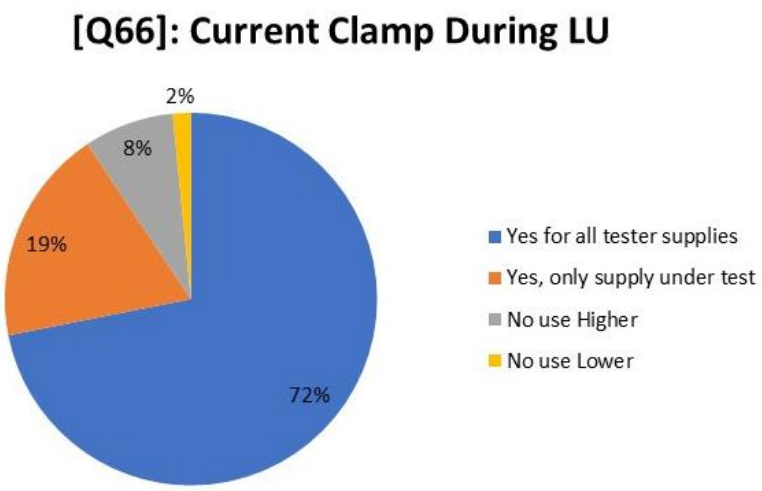


Figure 67 — Pie Chart of [Q66]

[Q66] "The JESD78 standard requires the following clamping limit to be applied during overvoltage testing: (a) I_{clamp} = 100 mA + I_{nom}, or (b) I_{clamp} = 1.5 x I_{nom}, whichever one is higher. Does your company follow this requirement?

[Q68] polls for the test temperature during latch-up testing. Of those who answered, 93% test at either a max ambient (44%) or a max junction (36%) temperature. 13% of the respondents use a combination of these, depending on the application. So, a clear preference for either method cannot be concluded. Figure 68 shows the distribution of the responses. Remarkably, 7% use room temperature only.

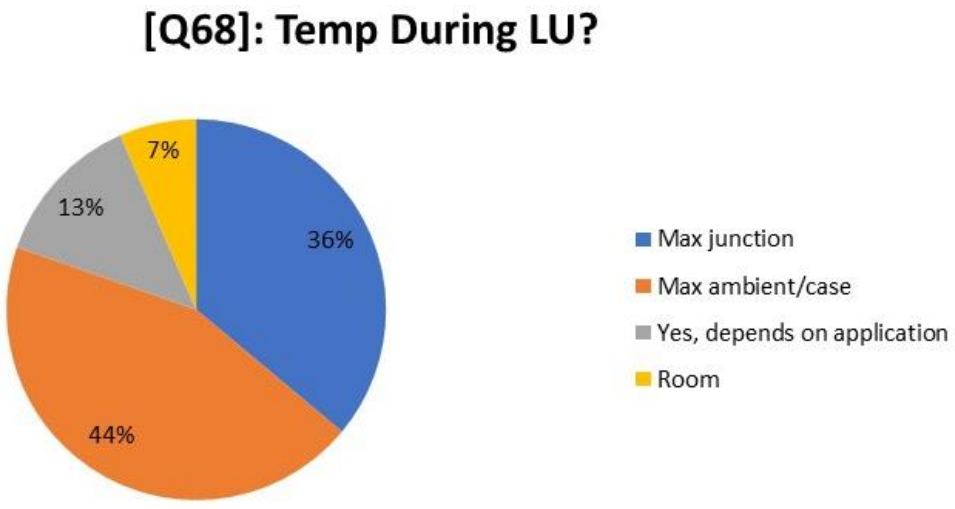


Figure 68 — Pie Chart of [Q68]

[Q68] "At what maximum temperature does your company perform JESD78 testing?"

5.6.2 Testing Specification (cont'd)

Responses to [Q73], on the duration of the stress, are illustrated in Figure 69. Of those that answered [Q73], 81% use a stress time of 3 to 10 ms; 9% a longer duration, ~10% a shorter duration. For those that answered [Q73], 20% did not respond to [Q74]. Please note that if not specified, a default of ~10 ms was assumed.

Some of the textual responses in [Q74] stated:

- Typically, 10 ms, unless we see EIPD - then we reduce it to as low as 200 us if needed.
- Default value is applied, but if there is a "failure", then values may be changed within limits allowed by JESD78 to retest.

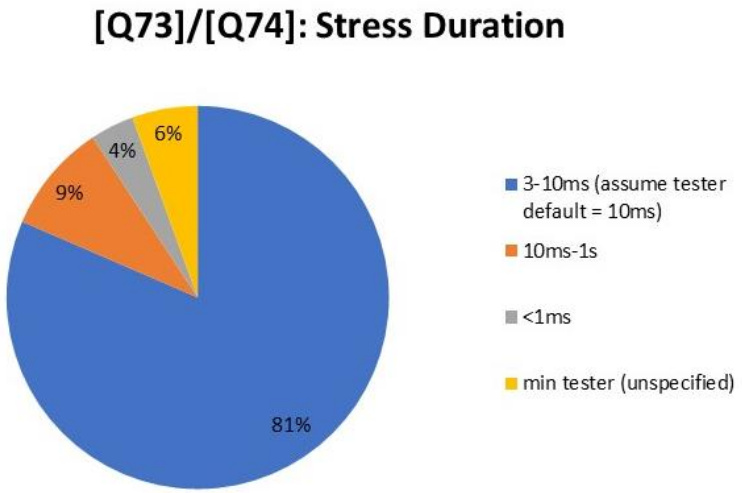


Figure 69 — Pie Chart of [Q73] With Specific Responses from [Q74]

[Q73] "Which pulse duration do you select during JESD78 testing?"

This suggests that in the case of a failure, engineers tend to analyze stress conditions to understand the root cause and/or to look for a condition that allows declaring a 'PASS' result.

Possible Interpretation
In the case of a failure, engineers tend to analyze stress conditions to understand the root cause and/or to look for a condition that allows declaring a 'PASS' result.

5.6.2 Testing Specification (cont'd)

Finally, [Q72] asked about pins that are exempt from JESD78 testing. The responses vary wildly and are summarized in Table 3. These responses suggest that the standard is interpreted very differently, and more clarification may be needed. Note that more than one answer was allowed for [Q72].

Table 3 — Number of Responses on Types of Special Pins

[Q72] What Pins are Exempt from JESD78?	
IO connected to Power / GND in datasheet	10
Connected to RC	18
Probe only	39
Flash programming	20
Clock pins	9
Reset pins	12
Write IN (none, application specific / low current)	12
No response	12

5.6.3 How is the Latch-up Testing Executed

[Q76] through [Q79] try to assess how much effort is put into verifying that the latch-up test is executed correctly. The responses show that a significant effort is put into this. Almost 90% review data logs provided by the tester to verify correct set-up and/or execution and almost half of them additionally use an oscilloscope and/or curve tracing analysis. As an example, the results of [Q77] "How do you systematically ensure that JESD78 testing is executed properly?" are shown in Figure 70. This clearly implies that most users are carefully verifying correct execution of intended stress conditions.

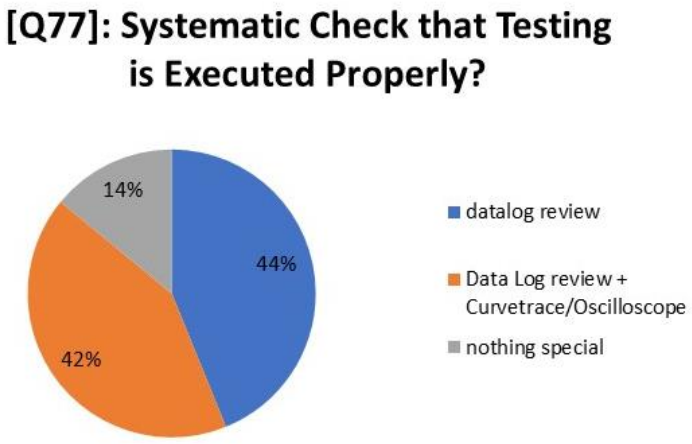


Figure 70 — Pie Chart of [Q77]

[Q77] "How do you systematically ensure that JESD78 testing is executed properly?"

5.6.4 Beyond the Specification

A set of questions was included to study if and when users stressed beyond the required limits. The first question in this series ([Q80]) polled if anything additional was done for pins that will face the outside world in the application, like e.g., USB pins, this is shown in Figure 71. Almost 80% test these pins like all other pins. However, 20% do test beyond the JESD78 requirement, in most cases by applying a different test (cable discharge event (CDE), transmission line pulse (TLP), direct pin injection (DPI)) or at higher JESD78 current injection levels.

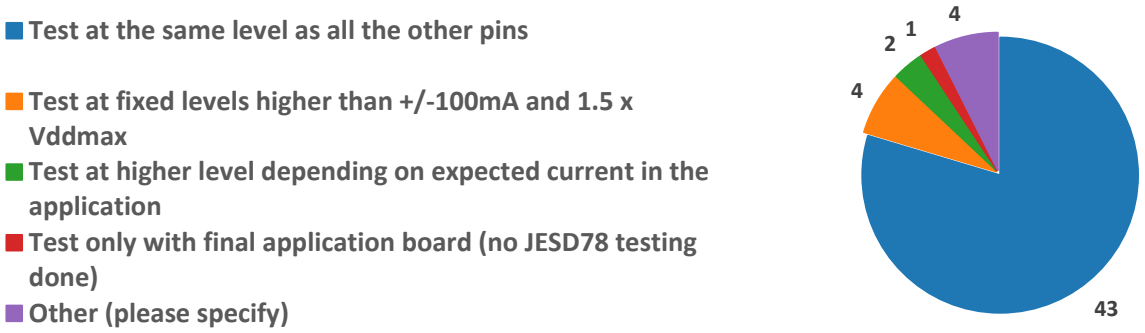


Figure 71 — Pie Chart of [Q80]

[Q80] "How does your company test products with signal pins that are exposed to external energy paths (e.g., USB; HDMI; etc.) or have an inductive load?"

Particular attention went to the treatment of LV pins, since with the present standard such pins may not see significant injected current. When asked if Table 2 of JESD78 was strictly applied for such pins [Q81] about 60% answered 'yes'. The rest at least characterizes to higher levels to allow current injection. From Figure 72 it is clear that less than 20% share this with the customer [Q83].

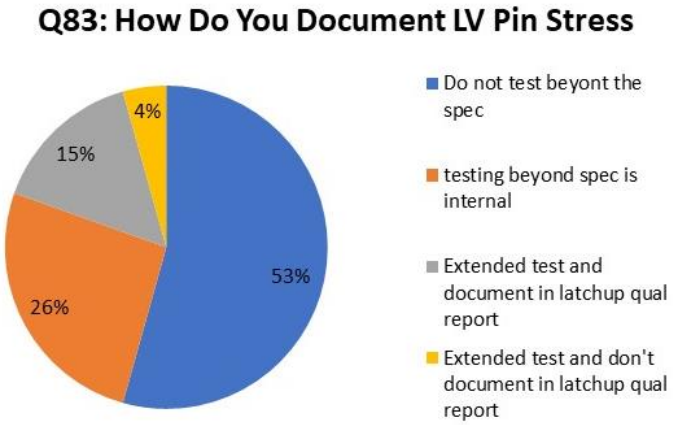


Figure 72 — Pie Chart of [Q83]

[Q83] "If you characterize LV pins beyond the voltage limits of JESD78, Table 2, do you apply this extended test method for product qualification and document the extended spec limits in the latch-up report?"

5.6.4 Beyond the Specification (cont'd)

Most of the 54 respondents said they test such exposed pins at the same level as all other pins. A few respondents test them at higher levels (6) or with additional characterization methods (3), for example TLP, CDE, or system level injection. Note that this summary includes interpreted write-in responses of the "Other" category, not comprehended in the pie chart above.

As supply voltages of IC signal interfaces (I/O domains) have been shrinking to levels below 2 V, the injected current on such low voltage (LV) pins has also been shrinking well below the typical 100 mA target level or has even become zero. That's because the test spec (Table 2 of JESD78E) sets a voltage clamping limit (extending the I/O voltage range by 50% of the full swing either in the positive or negative direction) that scales with the supply voltage. For LV pins, this limit may prevent the ESD diodes (or other similar diodes) in the I/O pads from conducting current. [Q81] addresses this topic directly and the results are shown in Figure 73.

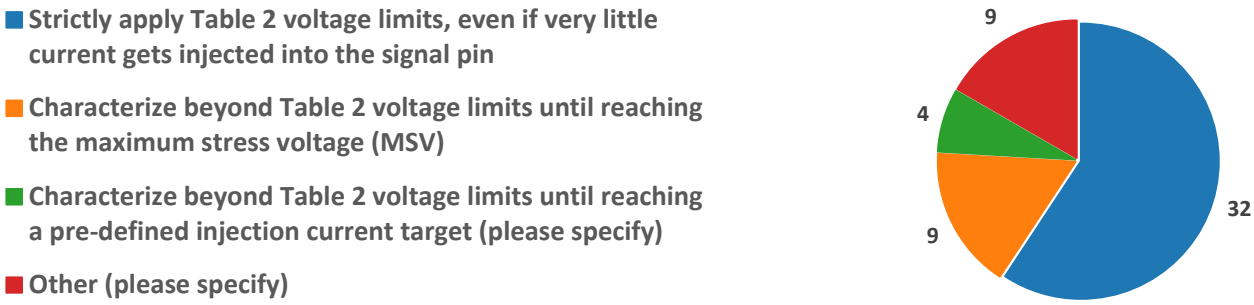


Figure 73 — Pie Chart of [Q81]

[Q81] "For low-voltage (LV) signal pins, the applicable voltage clamping limits of JESD78, Table 2 may reduce the injected current below the set target level (e.g., ± 100 mA). With a maximum supply voltage below about 2 V, the injected current may even become zero. Do you strictly apply the Table 2 voltage limits?"

More than half of the respondents (32/54) said they strictly apply the Table 2 voltage limits, even if very little current gets injected into the signal pin. Eleven respondents (two of them write-ins from the "Other" category) said they would test until reaching the MSV. Nine respondents (five of them write-ins) said they would test to predefined levels, either with higher current or with an increased voltage clamping limit. Some of the write-in comments may provide useful information and are given below (edited for content and length):

- Allow a small increase in clamping voltage above the spec requirement to allow at least some current injection (one respondent).
- Apply a clamping voltage that is at least 1 V higher than the maximum operating voltage (one respondent).
- Test with 200 mA injection current or with 1.5 x V_{DD} voltage limit (one respondent).
- Test with a fixed 100 mA injection current [*presumably above the voltage limit, if needed*] (one respondent).
- For qualification, strictly apply the spec voltage limits (Table 2). For characterization ("exploratory sample"), five respondents said they would go higher - up to twice the maximum operating voltage (one respondent), up to the MSV (three respondents), or up to 300 mA if the MSV allows it (one respondent).

5.6.4 Beyond the Specification (cont'd)

- Strictly test to meet the spec. If no current gets injected, this also means no current would be injected in operation. Forcing 100 mA and going beyond the spec voltage limits is not realistic and may force failures (one respondent).

Several noteworthy correlations between [Q81] and other questions were identified, [Q41] results are repeated here in Figure 74 (from Figure 34) for that comparison.

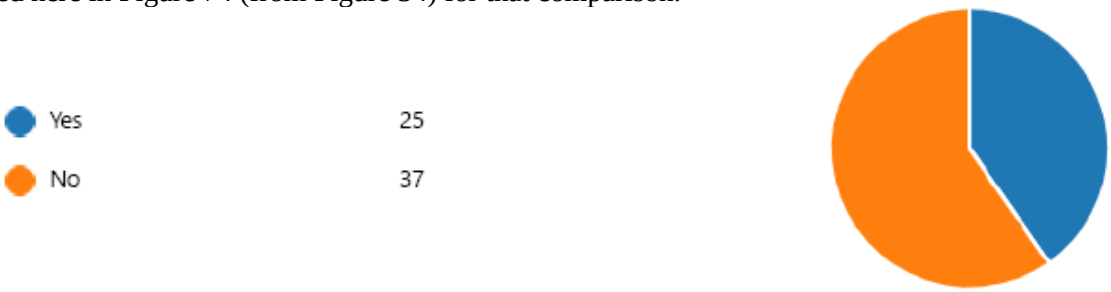


Figure 74 — Pie Chart of [Q41]

[Q41] "Does passing JESD78 testing guarantee latch-up robustness in the field?"

Looking at a correlation between [Q81] and [Q41]: Ten (91%) of the eleven respondents (including two write-ins) who characterize up to the MSV also said that passing JESD78 testing does not guarantee latch-up robustness in the field - a much higher percentage than the general population (66%). Likewise, respondents who strictly apply the Table 2 voltage limits also believe that passing JESD78 testing guarantees latch-up robustness in the field (47% vs. 34% baseline).

Possible Interpretation
Respondents who push LV pin injection beyond the classic spec limits (and up to the MSV) may believe that this is necessary to guarantee latch-up robustness in the field.

Respondents to [Q81] who said they strictly apply the Table 2 voltage limits were also more likely to agree with the following responses to [Q58], [Q61], [Q63], and [Q90]:

- [Q58]: "The latch-up robustness level given in the datasheet of an IC impacts the purchase decision" (72% vs. 58% baseline).

Possible Interpretation
Respondents who believe that ICs with higher latch-up spec level will also see higher sales are less likely to push LV pin injection beyond the classic spec limits.

- [Q61]: "Latch-up IC design rules should be exclusively driven by the JESD78 requirements with current specifications" (45% vs. 31% baseline).
- [Q63]: "Design rules should be relaxed if the 100-mA injection limit could not be reached because of the LV clamping limit or the MSV" (41% vs. 31% baseline).

5.6.4 Beyond the Specification (cont'd)

Possible Interpretation
Respondents who accept LV pins getting little or no current injected by qualification testing (presumably because it may reflect what happens in real applications) believe that design rules should be driven by JESD78 requirements.

- [Q90]: "The pin stress voltage limits are being set so that they do not exceed the product AMR because if damage occurs while exceeding the AMR, it is not a latch-up failure" (77% vs. 67% baseline).

Possible Interpretation
Respondents who make the (wrong) presumption that AMR numbers can be used for defining pin stress voltage limits during latch-up testing do not appreciate the risk of latch-up on low voltage pins.

Another question that addressed the LV pin topic was [Q83], with results as shown in Figure 75.

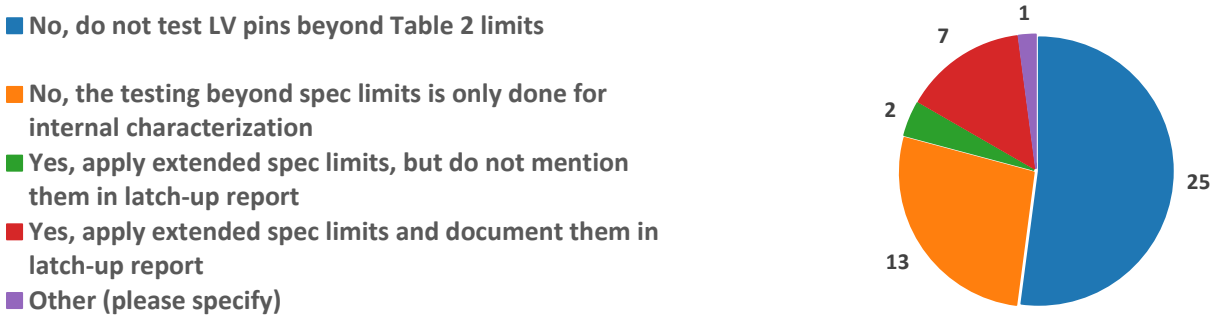


Figure 75 — Pie Chart of [Q83]

[Q83] "If you characterize LV pins beyond the voltage limits of JESD78, Table 2, do you apply this extended test method for product qualification and document the extended spec limits in the latch-up report?"

About half of all the 48 respondents said they would not go beyond the Table 2 voltage limits. Another quarter of respondents said they would only test beyond spec limits for internal characterization. Nine respondents said they would extend their test method for product qualification; seven of those said they would also report the result in the latch-up report.

Possible Interpretation
Almost half of the respondents see merit in characterizing LV pins beyond the JESD78 voltage limits applicable to injection testing. This may indicate a perceived real risk with the current specification preventing current injection on LV pins.

5.6.4 Beyond the Specification (cont'd)

[Q84] addresses a latch-up category that has been published [5], but is not included in JESD78 testing, the latch-up of a stressed I/O to another I/O. This is often referred to as 'signal pin latch-up'. 2/3 of the respondents set up the test program to check for signal pin latch-up. It might be good to extend the standard to include this method to ensure that this is done in a consistent way between different companies.

[Q84] results are shown in Figure 76.

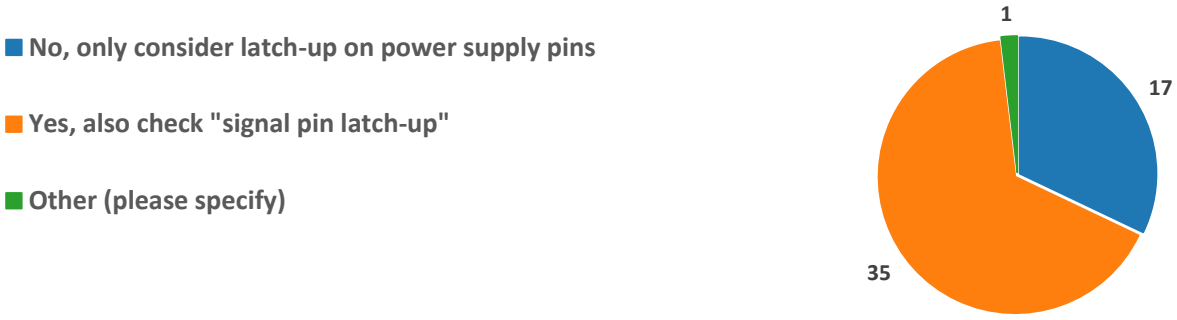


Figure 76 — Pie Chart of [Q84]

[Q84] "Do you setup the JESD78 test program to check if the injected signal pin itself suffered from latch-up ("signal pin latch-up")?"

35 of the 53 respondents (66%) said they would check for signal pin latch-up.

Possible Interpretation
The current JESD78E spec does not explicitly describe a "signal pin latch-up" test setup. The 66% of respondents who said that they already cover this aspect may either be mistaken or believe that it would be important in real system applications.

Respondents to [Q84] who said they would check for signal pin latch-up were also more likely to agree with the following:

- [Q25]: "Use QBS (qualification by similarity) of the worst-case package rather than testing all packages for products that are offered in multiple packages that use the same die" (59% vs. 48% baseline).
- [Q55]: "The existing 1.5 x VDDmax is an appropriate overvoltage stress level for final application" (74% vs. 60% baseline).
- [Q68]: "Perform latch-up testing at the maximum junction temperature rather than at maximum ambient temperature or room temperature" (47% vs. 37% baseline).
- [Q83]: "Testing LV pins beyond the voltage limits of JESD78, Table 2, is only done for internal characterization and results are not included in the test report" (38% vs. 28% baseline).

5.7 Maximum Stress Voltage (MSV)

This part of the analysis deals with the responses to [Q85] through [Q90] of the survey, which addresses the topic of "MSV" including its application and own experience:

- [Q85] The concept of maximum stress voltage (MSV) allows one to differentiate between latch-up and EOS (electrical overstress). The conventional pin voltage limits during JESD78 testing may be reduced to the MSV. How do you determine the MSV?
- [Q86] For determining the MSV, do you confirm that the damage is from a stress mechanism not directly related to latch-up (as required by the JESD78 standard)?
  - [Q87] In case of 'other means', please specify the above answer
- [Q88] Which (irreversible) damage conditions do you find acceptable for invoking the MSV?
- [Q89] How often do you encounter a product where the MSV reduces the injected current below the set target level (e.g., ±100 mA)?
- [Q90] Do you set the pin stress voltage limits so that they do not exceed the product AMR?

5.7.1 How Industry Interprets MSV vs. AMR to Qualify a Proper Latch-Up Stress

Since JESD78 revision D, the concept of a MSV was introduced to prevent failures during latch-up testing that are unrelated to the intent of the test (e.g., gate oxide damage). Therefore, the standard allows the user to set the pin's stress voltages below the prescribed value to a level appropriate for their application.

[Q85] asks how MSV is determined and the first notable result from this question was that no respondents selected "Do not use MSV". On the other hand, 60% of the respondents state they equate MSV to either the technology or product AMR and only 20% determine an MSV empirically. See Figure 77 for a distribution of the results.

Figure 77 — Pareto of [Q85]

[Q85] "How do you determine the MSV?"

5.7.1 How Industry Interprets MSV vs. AMR to Qualify a Proper Latch-Up Stress (cont'd)

[Q86] then asks whether physical failure analysis is used to confirm that the damage is from a stress mechanism not directly related to latch-up, this is shown in Figure 78.

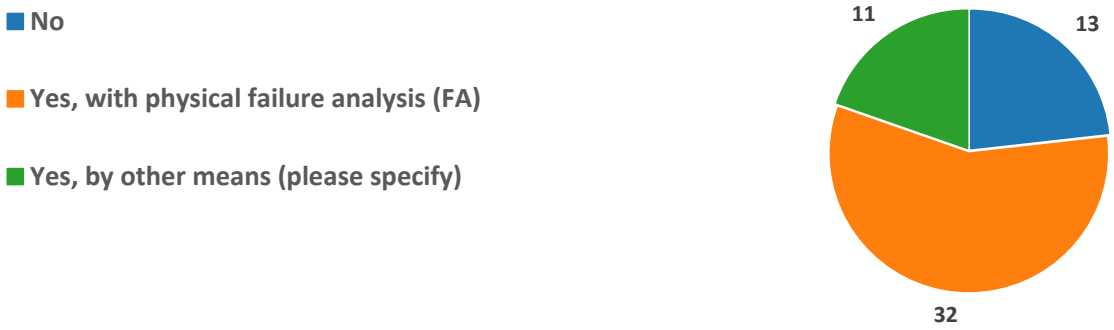


Figure 78 — Pie Chart of [Q86]

[Q86] "For determining the MSV, do you confirm that the damage is from a stress mechanism not directly related to latch-up (as required by the JESD78 standard)?"

The majority [32 of 56 (57%)] of respondents indicated that physical failure analysis was used to confirm the stress mechanism. The remaining 43% either do not confirm the stress mechanism at all or they use a means other than physical failure analysis. The write-in responses from "Yes, by other means" case ([Q87]) fall into one of the two categories listed below:

- MSV is determined through knowledge of the electrical characteristics of individual devices or circuits measured either separately or observed during the latch-up test.
- Setting the MSV below the minimum level at which permanent damage (EOS/EIPD) is observed by post-stress electrical measurements (e.g., ATE, IDD, etc.) after exposure to a JESD78 stress.

Possible Interpretation
Write-in responses above indicate that some respondents incorrectly believe that latch-up cannot cause permanent damage to the device under test.

[Q88] then asks which damage conditions are acceptable to invoke MSV and the results are shown in the pie chart of Figure 79. This question permitted respondents to select multiple answers and a total of 51 individuals responded. The lack of consensus reflected by these results is remarkable. For example, 100% of respondents were expected to select "Gate oxide rupture" while only 58% chose this damage mechanism. Furthermore, a surprisingly large number of respondents selected "Interconnect (metal, bonding, via) failure", when this failure mode is commonly associated with latch-up. Therefore, while the majority of respondents "confirm that the damage is from a stress mechanism not directly related to latch-up" when invoking MSV, the responses to [Q88] suggest that the results of the failure analysis could be misinterpreted in the context of MSV. It is possible that this question was interpreted by many respondents as a case in which it was already determined that latch-up did not occur based on the tester results (i.e., no increase in IDD according to the JESD78 definition). With this assumption, any of the physical damage mechanisms listed in [Q88] would be acceptable to invoke MSV. In general, permanent damage (of any kind) that is *proven not* to be latch-up related invokes MSV, while permanent damage (of any kind) that is *proven to be* latch-up related cannot invoke MSV. Distinguishing between these two categories can be challenging, since theoretically it is possible that the tester did not detect latch-up despite its occurrence, for example, because the high latch-up current prematurely ended as a result of the breakdown itself.

5.7.1 How Industry Interprets MSV vs. AMR to Qualify a Proper Latch-Up Stress (cont'd)

Failure analysis, often including de-processing, will be necessary to correctly categorize the failure. The intent of this question was to query failures that have reached the point of physical failure analysis to determine whether or not the triggering of a parasitic thyristor had occurred.

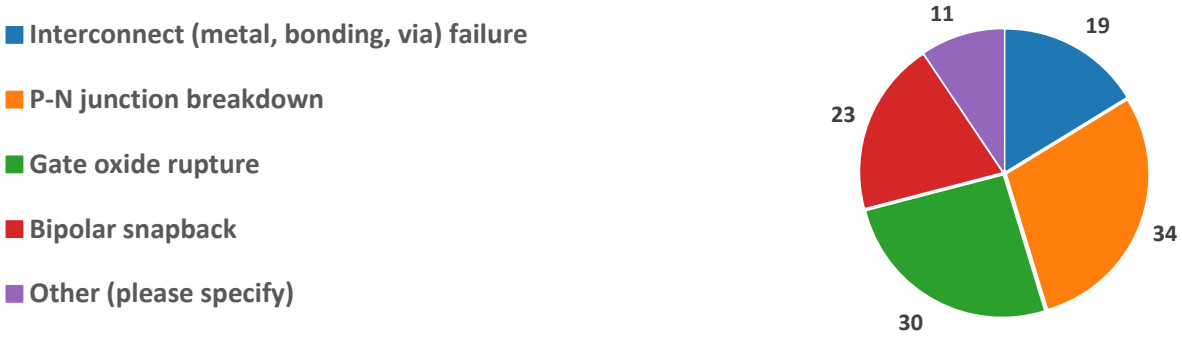


Figure 79 — Pie Chart of [Q88]

[Q88] "Which (irreversible) damage conditions do you find acceptable for invoking the MSV?"

[Q89] asks how often products are encountered in which the MSV limits the injected current below the target level of ±100 mA and the results are shown in Figure 80. Combining the responses of "Most of the time", "Often", and "Sometimes" together accounts for 53% of the population. This indicates that failing to reach the target injection level during a JESD78 test is at the very least not uncommon.

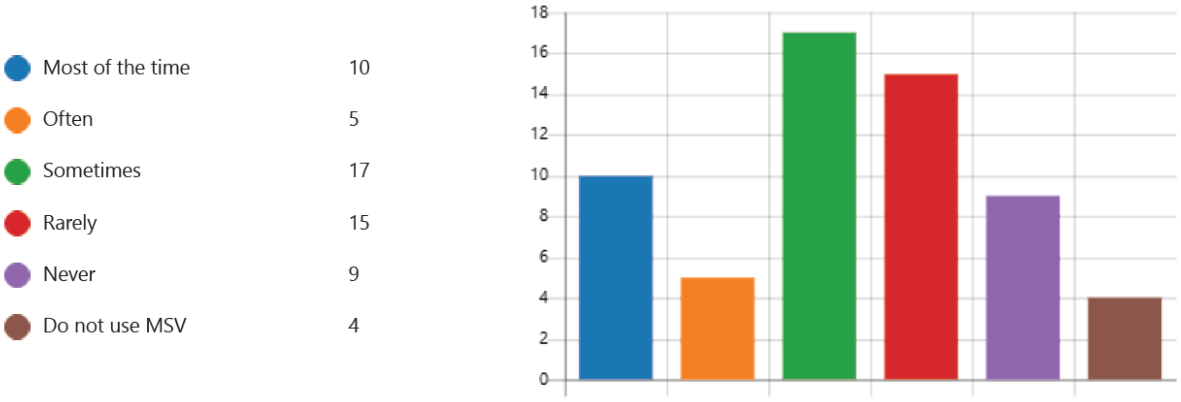


Figure 80 — Pareto of [Q89]

[Q89] "How often do you encounter a product where the MSV reduces the injected current below the set target level (e.g., ±100 mA)?"

5.7.1 How Industry Interprets MSV vs. AMR to Qualify a Proper Latch-Up Stress (cont'd)

[Q90] asks whether the pin stress voltage limits are set so that they do not exceed the product AMR. Although the JESD78 test standard explicitly states that "MSV is NOT the same as the absolute AMR", a large proportion of the survey respondents answered "Yes, if damage occurs while exceeding the AMR, it is not a latch-up failure" as illustrated in Figure 81. Note that setting the pin stress voltage limits so that they do not exceed the product AMR during latch-up testing could result in very little or no stress applied.

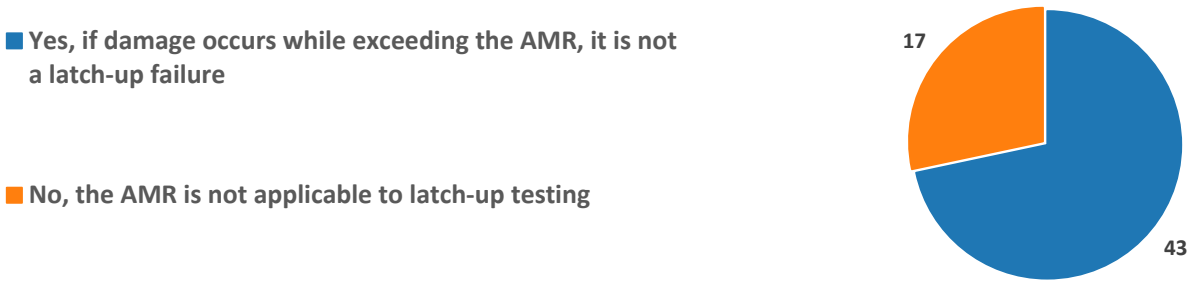


Figure 81 — Pie Chart of Responses to [Q90]

[Q90] "Do you set the pin stress voltage limits so that they do not exceed the product AMR?"

Not surprisingly, those that answered "No, the AMR is not applicable to latch-up testing" were much less likely (6% vs. 22% baseline) to use the product AMR to determine MSV [Q85]. Furthermore, those that use the product AMR to determine MSV [Q85] were much more likely to answer affirmatively to [Q90] (92% vs. 71% baseline).

Those that answered affirmatively to [Q90] were more likely to agree with the following statements:

- Passing JESD78 testing guarantees latch-up robustness in the field (correlation with [Q41]: 51% vs. 40% baseline).
- Latch-up IC design rules should be exclusively driven by the JESD78 requirements (correlation with [Q61]: 46% vs. 35% baseline).

That same group was also less likely to agree with the following statements:

- Latch-up occurring during the stress pulse (but not sustained), could be considered a failure depending on the specific scenario/application (correlation with [Q91]: 16% versus 32% baseline).
- The inability of pins below 2 V to reach the target current injection level of ±100 mA leads to latch-up risks in the application (correlation with [Q51]: 14% versus 25% baseline).

Similarly, for the respondents that use the product AMR to determine MSV [Q85]:

- They were more likely to be unaware of the fact that 2 V (and below) pins will fail to reach the target injection level of ±100 mA (correlation with [Q51]: 45% versus 16% baseline).

Possible Interpretation
Those that equate MSV to AMR have a limited view of all the possible ways in which latch-up can be induced in the field.

5.8 Failure Criteria

This part of the analysis deals with the responses to [Q91] through [Q94] of the survey, which are:

- [Q91] If latch-up occurs during the stress pulse (but not sustained), should that be considered a failure?
  - [Q92] Please specify 'It depends'
- [Q93] What are common causes of rejecting a JESD78 pass/fail result?
- [Q94] Do you use functional test (ATE test) to verify device specification requirements after latch-up testing to confirm pass/fail result from tester?

According to the current reading of the JESD78 standard, a latch-up fault arises when the current consumption takes on a significantly different value after removal of the stress condition in comparison to the situation before the test. "Latch-up-like" conditions can occur *during* the stress pulse, resulting in excessive current draw that is not sustained when the stress is removed. Whether and when a latch-up-like condition during current injection should also be included in the assessment of the device status is considered by [Q91] and [Q92] and is shown in Figure 82.

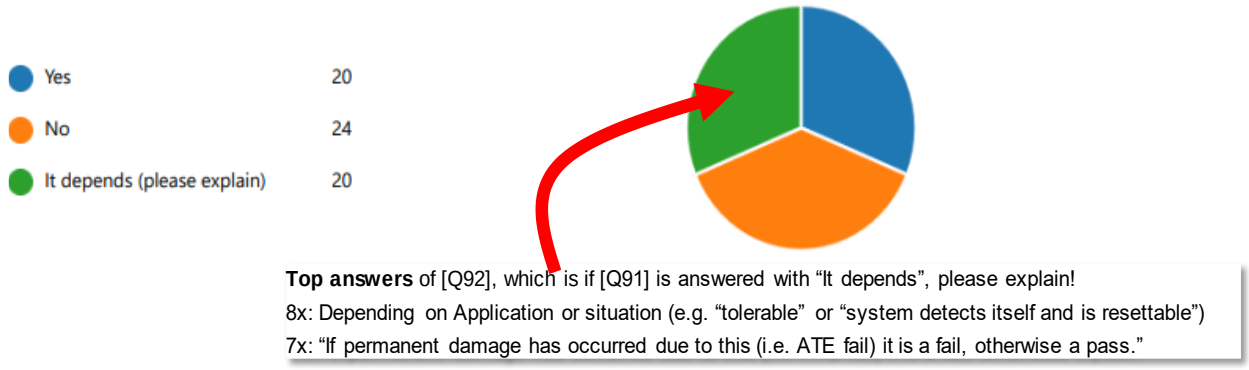


Figure 82 — Pie Chart of [Q91] and [Q92]

[Q91] "If latch-up occurs during the stress pulse (but not sustained), should that be considered a failure?"

[Q92] "Please explain why!"

The phrase "latch-up occurs during the stress pulse" might be contradictory and confusing because by definition of the test standard, latch-up occurs only if excessive current draw persists after the removal of the stress.

It seems, that the majority of the respondents ("Yes" plus "It Depends") indeed considers also looking at the device status during the latch-up test stress! They do not only rely on the condition of the device *after* exposure to the V-test or I-test alone. To rate the latch-up test as either pass or fail in the case of a transient event, most respondents consider either application specific boundary conditions or occurrence of permanent fail.

5.8 Failure Criteria (cont'd)

There could be various conditions, under which a passed JESD78 test should be finally rejected. The answers to [Q93] in Figure 83 describe these conditions.

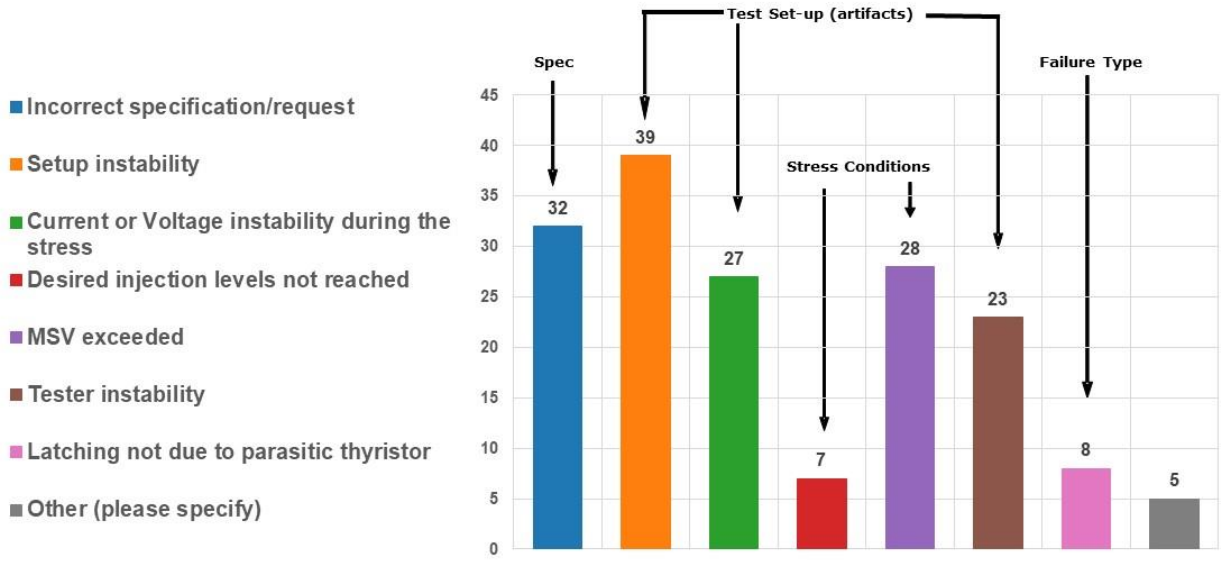


Figure 83 — Pareto of [Q93]

[Q93] "What are common causes of rejecting a JESD78 pass/fail result?"

There exist different classes of criteria, which could lead to a rejection of a pass result, ranging from failure type, test-set-up artifacts, stress conditions, to issues related to product specification. Interestingly, a situation where a latch-up test was rated as pass, but the desired injection levels are not reached is acceptable and should not be rejected!

Finally, the survey asked in [Q94] whether a functional test is applied after latch-up testing for confirming pass/fail result from tester, the results are shown in Figure 84.

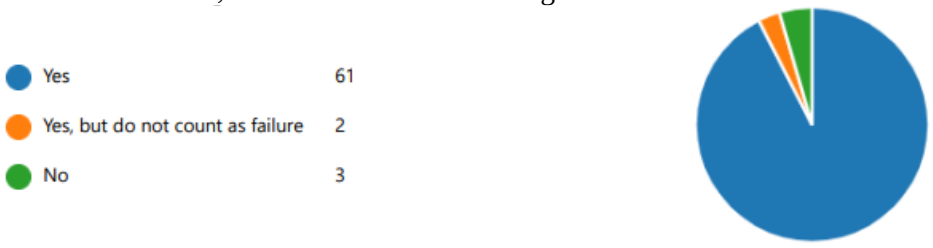


Figure 84 — Pie Chart of [Q94]

[Q94] "Do you use functional test (ATE test) to verify device specification requirements after latch-up testing to confirm pass/fail result from tester?"

The overwhelming majority of respondents perform post-stress functional testing to verify device specification requirements. There were some exceptions: 3 respondents answered 'No' and 2 of those respondents were either a foundry or an OEM. This same group was much more likely to test at room temperature only [Q68]. This might only suggest some practical barriers from performing the test flow in the ideal manner prescribed by the JESD78 standard.

5.8 Failure Criteria (cont'd)

While at face value this result is encouraging, it must be noted that some portion of these respondents might interpret the ATE results incorrectly in the context of MSV. The evidence for this statement comes from a combination of the responses to [Q86], [Q87], and [Q94]. Firstly, a sizable number of respondents answered "No" to [Q86] (13 out of 56 total or 23%) indicating that they do not confirm that damage is from a mechanism unrelated to latch-up to determine MSV. Furthermore, two respondents answered "Yes, but do not count as a failure" to [Q94], which was an unqualified indication that these respondents believe that damage as a result of the JESD78 stress is unrelated to latch-up. Finally, analysis of write-in responses to [Q87] uncovered separate remarks from three different respondents that either implied or explicitly stated that latch-up cannot produce damage, which is a misunderstanding, and if used in determining MSV, may lead to an incorrect pass/fail decision.

Possible Interpretation
Some portion of respondents might believe that latch-up cannot produce damage and if this misunderstanding is used in determining MSV, it may lead to an incorrect pass/fail decision.

5.9 Concluding Questions

This clause summarizes the feedback received in the last part of the survey, which consisted of 2 open text questions:

- [Q95] "Feel free to enter any suggestions/recommendations."
- [Q96] "Please provide your email address to receive a copy of the final report on this survey (open text)."

[Q96] asked to leave an email address. Out of 70 respondents, 52 left in total 55 valid email addresses. The final report will be sent to those email addresses.

[Q95] "Feel free to enter any suggestions/recommendations" solicited feedback from responders on any aspect they thought deserved more attention and or was not present in the survey.

There were 28 respondents that left a total of 47 suggestions related to the content of the survey. They were grouped by topic. Figure 85 shows the Pareto of the distribution of the responses. Not surprisingly, the topics 'levels/injection', 'MSV/AMR' and 'goal' received most attention.

Since these were individual comments, they are provided here for further study sorted by category. In principle, the comments and suggestions are repeated verbatim, except that they may have been broken down if multiple comments were provided by 1 respondent.

It was interesting to note that about 1 out of 4 of the comments were a request for clarification. These were also made visible in Figure 85 and are listed as the first entries in each category.

5.9 Concluding Questions (cont'd)

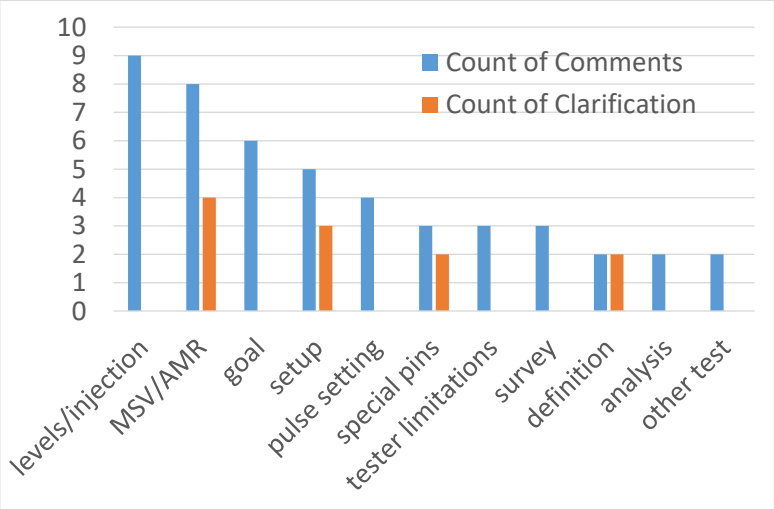


Figure 85 — Pareto of Response Groups

Levels/Injection

1. *I think it would also be appropriate to specify a minimum clamp voltage level above Vmax / below Vmin of say 1 V to give the opportunity for stress currents to flow.*
2. *The purpose of the latch-up test is to inject current by turning on the diode then PNPN. If we want to turn on the diode, we need to address the voltage clamp for decreasing VDD in advanced tech node.*
3. *Given the VDD at low voltage < 1.2 V, negative I-test cannot be performed. Even though the diode could be turned on, it's impossible to inject 100 mA as voltage is clamped. To inject -100 mA, voltage has to drop to -1.3 V for some cases.*
4. *The current injection method requires a current of ±100 mA, so consideration is required.*
5. *The clamping voltage limit on low voltage pins need to be modified. Use of 1.5 x VCC does not show any injection of current.*
6. *Recently problems caused by a combination between IC and poor quality PCB is our concerns. On the other hands, Latch-up by IC gives us no serious problems in our case. Failure criteria condition increasing is not welcomed. Some IC users tend to raise their requirements although they have poor condition in PCB (above-mentioned one). (In particular ASIC companies ....)*
7. *The "testing levels (undershooting VDD voltage levels and/or overshooting VSS voltage levels)" should be suggested with different classifications.*
8. *Also, does 100 mA suit all application?*
9. *Does the current level (100 mA) still make sense for I/O pins of 2 chips mounted on the same board? Should 100 mA be limited to hot plug application or external interfaces (not on same board)?*

5.9 Concluding Questions (cont'd)

MSV/AMR

1. *There is much confusion in the industry about MSV and AMR in relation to latch-up. A document (e.g., user-guide) would be very useful to educate industry about how these terms should be properly applied.*
2. *The MSV definition gives a lot of flexibility, e.g., NOTE 5 in JESD78E P.27, MSV is determined to prevent an EOS-like condition. So, back to earlier statement, does it pass or fail due to EOS of a parasitic bipolar.*
3. *Clear method to determine MSV value.*
4. *I believe that the term "EOS" should be used when discussing LU. As exceeding AMR is required in order to forward bias junctions during I-test, EOS always occurs. Catastrophic damage or another term should be used rather than "EOS".*
5. *determining MSVs can be very painful.*
6. *Please add MSV per pin/supply and pulse width per pin/supply as a reporting requirement.*
7. *The current definition of MSV is burdensome to semiconductor vendors and should be abolished.*
8. *MSV should be aligned with the AMR of pin.*

Goal

1. *The goal of the test should be to identify LU issues in real-world applications. The JESD78 spec should be modified keeping this goal in mind.*
2. *As previously noted, different automotive manufactures have different requirement, but all expects zero defect from the final product. As the chip traces reduce in size latch-up and its parameter effect are going to become more important and proper testing will be vital to selecting of components.*
3. *I agree with you to modify the Latch-up standard for addressing real world stress.*
4. *We consider LU testing according to JESD78 to get an insight into the robustness of a product with respect to a very specific situation (static current injection and overvoltage testing with respect to a certain stress value and stress duration) but nothing more. We believe that this approach is reasonable but does not give customer a carte blanche to exceed the Absolute Maximum Ratings (as specified for each pin in the Datasheet) using the device in his application.*
5. *In general, I have doubts about the real life benefits of a product with high JESD78 LU qualification level. Especially considering the many 'ways out' that the standard offers (for good reasons) in case of a failure. And obviously the fact that often only a fraction of the 100 mA current can be injected before the compliance is reached, makes me also wonder how useful the LU testing actually is. Important question is how LU performance correlates to robustness against real life threats, which are not limited by an MSV setting. Fatal EOS can easily happen, but a real LU event might be actually very unlikely.*
6. *If a given device is finally exposed to very specific stress situations in a system, this stress needs to be specified and quantified and conformity adequately verified. In many situations a result of a LU test may not help to decide if this particular stress on application is a problem to the device or not and may lead to EIPD.*

5.9 Concluding Questions (cont'd)

Setup

1. *In addition, there are often "false failures" caused by setup conditions changing. It would be useful to allow or even recommend that the preconditioning steps (vectors etc.) are re-applied after the stress is removed to allow the device to revert back to its initial operating state. A proper latch-up condition (by definition) cannot be exited using normal device operations.*
2. *Regarding JESD78 itself I'm wondering whether the standard should be more specific about an SoC with multiple power domains. Often provisions are available to power down certain parts (for power reduction) and as consequence certain guard rings may be in that state no longer effective. As far as I know normal practice is to do LU test with all powers on (only), while maybe worst-case situation might be partial power down. Shouldn't this be addressed in the standard?*
3. *Signal pins bias status (GPIO/Differential Pairs) is not clearly defined.*
4. *Noise on GND makes it easier to latch-up, and it is closer to latch-up due to system level ESD.*
5. *The setup of parts to get in stabilization/IDDQ state, this is very painful since the latch-up testers don't have same functional capabilities as real functional testers so it brings up the issue should latch-up be done only on functional testers or on ESD/latch-up specific testers?*

Pulse Settings

1. *In terms of JEDEC78 add something on voltage supply ramping rates to see if mis-triggering,*
2. *The freedom in adapting the Energy Level (pulse Duration) is strange and should be further classified.*
3. *T_r, T_{width}, $T_{cooling}$... are not exactly defined.*
4. *Move current pulse to more of a transient like machine model waveform.*

Special Pins

1. *"There is no clear procedure of JEDEC specifying how we could stress some special pins such as: PWM, LDO, RF, VISO. It would be very appreciated if you could come up with a method to test these pins properly!"*
2. *Clarity on how to test the special pins like RF pins, RF pins and voltage regulator/reference.*
3. *"The application like test (e.g., System level transient latch-up) would be more representative for real-world functionalities of RF products, especially RF pins. Injecting DC current in RF inputs which do not allow any DC in application, is not realistic, thus the JESD78 kind of does not represent the reality of special (RF) pins. Example of RF input pin specification: Maximum voltage, e.g., pin voltage should not go below DC -0.4 V, then DC current injection is not possible.*

Tester Limitations

1. *Tester current limit cannot satisfy the Ultra-large ASIC power supply current.*
2. *Tester Power supply groups limited to 6~7, cannot meet the multi power supply requirement.*
3. *High voltage(> 30 V) cannot be tested. (PMU field)*

Survey

1. *Finally: we could not deal w/ "SEL" (unknown meaning/method.*
2. *It would be helpful if there is webinar planned on the final report.*
3. *Consider quantification of LU related fails in [Q27] in a way that LU issues did indeed partially occur during early LU testing of an early design state but were then fixed for the final product.*

5.9 Concluding Questions (cont'd)

Other Tests

1. *Transient-Induced Latch-up in CMOS Integrated Circuits under system-level ESD/EFT testing should be pushed to be a test standard into the IC industry.*
2. *Another item that may deserve more attention is signal LU, which might especially be interesting in combination with above mentioned partial power down of the device. In fact, LU rules which we have to follow in the design, do take the worst case into account (e.g., high level signal on I/O, while power is off), while, as said, such condition (and signal LU at all) is usually not part of the LU qualification. Should it be? Of course, I would like first to be sure that we talk about real life threats, rather than an interesting phenomenon that is unlikely to harm.*

Definition

1. *Also, supplier sometimes claim if a failure is not caused by the PNPN structure, but parasitic bipolar which is not considered as latch-up. Does it pass or fail?*
2. *When we notice decrease in I_{DD} current, we do not take any step. Clarity needed.*

Analysis

1. *Latch-up testing requires a lot of testing resulting in data on hundreds of pins. The injection current passing levels can vary from pin to pin and device to device. If a software program is available to display the large amount of data in a comprehensible format it utilizes more efficient methods in saving time and assessing consolidated latch-up performance for ICs. This type of summary generated by a software can give realistic information to the customer and applications engineers.*
2. *Voltage shmoo ramping is not useful.*

After reading the comments it is clear that many respondents have concerns on the current way of testing in relation to actual threats an IC may face. Several suggestions for changes are provided in addition to requests for clarification.

6 Conclusions and Recommendations

6.1 How Did the Survey Team Come to Their Conclusions and Recommendations?

The aim of the latch-up survey was to obtain an up-to-date picture of the acceptance, relevance, and concrete application of the latch-up standard JESD78. This goal extended beyond suppliers of semiconductor components, but also to the customer side, i.e., Tier or OEM level. Furthermore, the aim was to get insight into potential improvements and extensions of the JESD78 test method. While the survey itself was created by a larger team, the analysis of the responses was done later by a subgroup of that team.

Very important, the feedback was taken at face value. Without being biased, the conclusions and recommendations as derived below represent an interpretation of the data by the whole analysis team based on given data and bare facts.

To provide the following clause a structure, the team has created a list of observations based on survey data and grouped them together on commonality. Hence the conclusions discuss key take-aways and are not intended to duplicate each finding as worked out in the individual clauses from Clause 5.1 to Clause 5.9.

6.2 Conclusions from the Analysis

To get an impression of the big picture on the main latch-up topics, several “high level” questions were identified and compared with the survey results:

1. What information comes from respondents regarding latch-up fails (in qualification and the field)?
2. What are the expectations from JESD78 testing and how do they refer to reality?
3. Are the recommended qualification levels appropriate?
4. Do we have evidence that the test method is a good predictor of robustness against latch-up in the field?
5. How is the test standard interpreted and executed across the industry?
6. What changes should be made to the standard to better suit the reality of present day and future products?

Detailed analyses of these “high level” topics are worked out as follows:

1. **What information comes from respondents regarding latch-up failures (in qualification and in the field)?**
   - Almost all respondents report a very low number of latch-up fails in JESD78 testing, in qualification, and in the field[1].
   - While the majority of latch-up fails are reported during the JESD78 qualification test and many of these fails result in a re-spin, this accounts for a very small fraction of the total number of re-spins[2].
   - More than 50% of all latch-up fails (field + JESD78 testing) do not require re-spin, but the failure drives alternative mitigations such as board modifications or software changes[3].
   - Observation: There was no real survey question on what exactly is regarded as a “latch-up fail” in the field. There might be different scenarios interpreted as a “latch-up in the field”.

[1] See Clause 5.2.1 [Q06]
[2] See Clause 5.2.1 [Q11]-[Q12]
[3] See Clause 5.3.1 [Q21]-[Q29]

6.2 Conclusions from the Analysis (cont'd)

Although there is a very broad and inconsistent interpretation of what constitutes a latch-up issue, there is agreement that latch-up issues do not occur very often. When they occur, there is usually a different workaround other than a re-spin

2. What are the expectations from JESD78 testing and how do they refer to reality?

- Most respondents believe that the JESD78 standard is useful for preventing system failures in real world scenarios in at least some or all cases, and that removal of JESD78 as a qualification requirement would lead to less reliability in the field[4].
- More than three quarters of the respondents test pins exposed to external energy paths (e.g., USB, HDMI, etc.) in a system in the same way as all other pins on a chip suggesting that JESD78 is expected to provide adequate coverage for such pins[5].
- However, only about 60% of respondents say JESD78 addresses real world stress events, and about 60% of respondents do not believe that passing the JESD78 test guarantees latch-up robustness in the field[6].
- Although the typical JESD78 stress pulse has a width of several milliseconds, respondents say that the test is supposed to address failure mechanisms occurring with longer and shorter pulse widths[7].
- A large number of respondents believe that JESD78 requirements should drive latch-up IC design rules either with the current specification or in a future improved form[8].
- Though not directly asked for, respondents did not provide write-in examples of real-world electrical stress scenarios that would be modeled by JESD78 latch-up testing.

JESD78 is considered useful and should not be removed, but it does not guarantee robustness in the field. Respondents see value in JESD78 testing for modeling real world stress events beyond the specified test conditions.

3. Are the recommended qualification levels appropriate?

- The stress conditions required to achieve immunity level A (≥ 100 mA / 1.5 x V_{DDmax}) are perceived to strike the right balance between reliability and effort[9].
- The fact that LV pins do not reach the target current injection level is not perceived to introduce any field risk by the majority of respondents, although a minority state that the current injection level at such pins might be far too low for certain applications[10].
- 59% of respondents state that the latch-up robustness level impacts purchase decisions[11].

The recommended stress conditions are regarded as sufficient. A failure to meet them could affect purchase decisions. A large majority do not see risk for LV Pins in the application with limited current injection in the qualification test.

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[4] See Clauses 5.3.2, 5.2.2 [Q09], [Q32]
[5] See Clause 5.6.4 [Q80]
[6] See Clause 5.2.3.1 [Q31], [Q41]
[7] See Clause 5.3.2 [Q30]
[8] See Clause 5.5.2 [Q61]
[9] See Clause 5.3.4 [Q53, Q55]
[10] See Clause 5.4.3
[11] See Clause 5.6.4

6.2 Conclusions from the Analysis (cont'd)

4. Do we have evidence that the JESD78 test method is a good predictor of robustness against latch-up in the field?

i. Is there evidence that JESD78 is necessary to ensure latch-up robustness in the field?
- There is a belief that without the JESD78 test, parts would be less reliable, but there is no evidence of an increased field return rate for products qualified as immunity level B[12].
- However, the multitude of ways that a part can be qualified as immunity level A while receiving little or no stress prevents us from drawing any strong conclusions from this result[13].

ii. Is there evidence that JESD78 is sufficient to ensure latch-up robustness in the field?
- The majority opinion is that passing JESD78 ensures robustness to some events, but not all[14].
- It is evident that passing JESD78 testing is insufficient to guarantee latch-up robustness in the field and seems to be more related to the type of stress rather than the levels[15].
- Additional application-specific tests might be required but are performed only by a minority of respondents[16].

It cannot be concluded that JESD78 is a necessary test to ensure latch-up robustness in the field, but there is strong evidence that it is insufficient to replicate a variety of latch-up trigger mechanisms.

5. How is the test standard interpreted and executed across the industry?
- The concept of the "maximum stress voltage" is well-known in the industry but very often misinterpreted and incorrectly applied to JESD78 tests[17].
- 69% of respondents believe that the pin stress voltage should not exceed the product AMR[18].
- There is an incorrect assumption being made by some portion of the industry that latch-up cannot cause permanent damage[19].
- The results of failure analysis are often misinterpreted in the context of MSV[20].
- The majority opinion is that the inability to reach the target current injection level of |100 mA| for low voltage pins does not lead to latch-up risks in the final application[21].
- A minority state that while the latch-up risk might be relatively low for systems operating at 2 V and below, the application conditions of the pin should be considered in evaluating and testing for latch-up robustness[22].
- Some of the respondents are already evaluating their parts with LV pins beyond the limits specified in JESD78, Table 2[23].

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[12] See Clauses 5.3.2 [Q32] and 5.2.1 [Q13]-[Q16]
[13] See Clauses 5.4.3 [Q51], 5.6.1 [Q73], 5.6.4 [Q81], 5.7.1 [Q85], [Q90], 5.8 and 5.9 [Q95]
[14] See Clauses 5.2.1 [Q09], 5.3.2 [Q30]-[Q33], 5.2.3 [Q12], and 5.9 [Q95]
[15] See Clauses 5.3.2 [Q37], [Q41]-[Q43]
[16] See Clause 5.4 [Q43]
[17] See Clause 5.7.1 [Q85], [Q86], [Q88], [Q90]
[18] See Clause 5.7.1 [Q90]
[19] See Clause 5.7.1 [Q86], [Q88]
[20] See Clause 5.7.1 [Q88]
[21] See Clause 5.4.3 [Q51]
[22] See Clause 5.6.4 [Q83]
[23] See Clause 5.6.4 [Q82], [Q83]

6.2 Conclusions from the Analysis (cont'd)

- A failing ATE result after a JESD78 latch-up test is sometimes misused to reduce the stress voltage to a level at which the part will pass, and this level is often the product AMR[24].

The survey revealed that a significant portion of the industry is executing the JESD78 test incorrectly when applying the MSV to their product, including the conclusions drawn from failure analyses and ATE. This is likely due to a general misunderstanding of MSV/AMR as well as an incorrect assumption that latch-up cannot cause permanent damage. While a majority of respondents do not believe that the treatment of low voltage pins by JESD78 will increase the risk for field failures, a minority believe there could be some risk and at the very least the application conditions of the pin should be considered in determining the stress level to apply.

6. What changes should be made to the standard to better suit the reality of present day and future products?

- Nearly one half of the respondents were in favor of a new generic current injection and overvoltage test method that is not limited to latch-up as a root cause[25].
- Additional test methods should be recommended to cover the deficiencies of JESD78 to reproduce real-world latch-up triggers. TLU in particular should be promoted to complement JESD78[26].
- There is an overwhelming consensus that the failure criteria should be broadened outside of triggering a parasitic thyristor.
- There is a lack of consensus on which circuit elements should be considered JESD78 failures, but the majority believes that the failure criteria should include "anything that causes a supply current increase"[27].
- A clear approach to derive MSV[28].
- The limitations of JESD78 should be clearly communicated[29].
- Recommend procedures for testing special pins should be included in future JESD78 revisions[30].
- More guidance is needed on when it is appropriate (and when it is not appropriate) to adjust test parameters upon observing a latch-up failure.
- A majority of respondents want to see a sustained decreased supply current considered as a failure, though currently JESD78 only considers an increased current[31].

Additional test methods should be recommended to cover the deficiencies of JESD78 to address real-world product robustness issues. A clear approach to derive the MSV should be described and communicated. Because MSV can directly impact the stress level applied to a product and is so pervasive across the industry, addressing this issue should be a key takeaway from the survey results. The failure criteria as it relates to the definition of latch-up should be expanded beyond the original intent of triggering a parasitic thyristor. If this definition is expanded in future revisions, it should be accompanied by a thorough understanding and clear communication of the conditions under which MSV can be applied.

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[24] See Clause 5.7.1 [Q86], [Q88], [Q90]
[25] See Clause 5.3.3 [Q49]
[26] See Clauses 5.4.3 [Q42], 5.4.5 [Q44], and 5.10 [Q95]
[27] See Clause 5.5.2 [Q47]
[28] See Clause 5.8.1 [Q76], [Q85], [Q86], [Q88], [Q90], and 5.10 [Q76]
[29] See Clauses 5.4.2 [Q30], and 5.10 [Q95]
[30] See Clause 5.10 [Q95]
[31] See Clause 5.5 [Q46]

6.3 Recommendations for Future Work

Having analyzed the individual feedback of the survey and correlating the findings to the team members' original expectations, the following recommendations are given.

1. A detailed seminar aligned with the revision F release explaining the major changes from revision E and implications to LU testing.
   - In particular, the extension of the definition of LU seems to be a major change as it will limit in which cases MSV can be invoked. For example, damage due to triggering of a single bipolar transistor will now be considered LU with revision F, and MSV treatment could therefore not be applied anymore to resolve this LU failure.
2. Provide better explanation/training on MSV[32].
3. Broaden the definition of LU by incorporating "anything that leads to permanent increase of current"[32].
4. Explore other possible outcomes of LU testing like "permanent decrease of current".
5. Create a JESD78 user guide with practical explanations, hints, and examples.
6. Consider ways to standardize LU testing at an application level (system level ESD, transient LU).
7. Use the survey findings to optimize/extend tester software to help verification of test program/execution.
8. Form a task force to correlate real world LU stress events to JESD78 with the goal to scrutinize the existing JESD78 stress pulse and stress levels.
9. More research/discussion into the applied lower injection limits for LV pins.
   - Point 8 may help significantly with this, if focused on finding real world stress events related to LV pins. This may become increasingly important considering that the strict interpretation of LV pin injection limits already drives relaxation of LU design rules in advanced technology nodes.
10. Examine/eliminate perceived "loopholes" in the JESD78 spec that may be used to significantly limit the applied stress (e.g., LV pin injection limits, MSV, special pin treatment, etc.), although in real life these pins may see higher stress, nevertheless.
    - Point 8 may help significantly with this.
11. Take the application conditions of pins into account when determining the LU stress levels, especially for LV pins or pins where MSV could be invoked. Investigate a potential pin classification method based on their actual application (e.g., system internal vs. system external pins).
12. More guidance on special pins treatment[32].
13. Introduce a new generic "current injection and overvoltage" test method.
    - Such a generic method would for example describe general pulse shapes, injection methods, clamping mechanisms, failure detection methods, etc. Users could refer to it for definitions and specify the parameters they used for reproducing a certain effect.
    - Perhaps a future revision of JESD78 could simply reference a generic test method and wrap the LU specific specifications around it - JESD78 would become much slimmer, essentially a specification of which settings of the generic method are used.
    - The new generic test method could potentially also be used in a broader sense for other test specifications, such as, for example, transient LU in the future.
14. More guidance on when it is appropriate to adjust test parameters upon observing a LU failure.
    - Incremental improvements to debug a LU test program are generally appropriate, but changes that would exploit perceived "loopholes" as mentioned in point 10 should be discouraged.

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[32] Already addressed in JESD78 Revision F. See Clause 6.4

6.3 Recommendations for Future Work (cont'd)

15. Consider adding recommendations regarding LU tester power supplies' ability to sink currents and how this relates to real system applications.
16. Assuming the concept of MSV will remain in future JESD78 test standard revisions, there needs to be a clear delineation of damage mechanisms that can or cannot be used to lower the applied stress voltage.
    - A table could be provided that exhaustively lists damage mechanisms that are considered "latch-up" and those that are not, along with representative failure analysis images and recommendations for additional measurements to confirm or rule out specific failure mechanisms.

6.4 Latest JESD78 Revisions

During the preparation of this report the JESD78 working group has released revision F of the JESD78 document (dated January 2022). And revision F.01 is planned to release simultaneously with the release of this publication. These revisions address some of the topics discussed in this report, and partially implements some of the recommendations. The reader is encouraged to review the latest JESD78 revision that can be found at www.jedec.org. A summary of the changes in JESD78 revision F are listed here:

- The definition of LU has been extended. Historically, latch-up was restricted to the triggering of a parasitic thyristor structure (PNPN). Now the triggered structure is extended to any structure that, once triggered, will cause higher than normal currents to flow between power and ground (e.g., bipolar transistors), and this condition does not end without removing power from the system. This extension is meant to honor that low impedance paths created by these other structures are indistinguishable from the effects of a triggered parasitic thyristor and, from a customer perspective, are just as detrimental to system performance. A current increase by a change of a functional state is still not considered as LU.
- Class II now requires testing to be performed at maximum junction temperature. JESD78E allowed testing at maximum ambient or maximum case temperatures as well. It is also now explicitly stated that Class I testing (i.e., at lower temperature) is not required in addition to Class II testing.
- The two main test categories, "I-test" and "V_{supply} Overvoltage Test," have been changed to "Signal Pin Test" and "Supply Test", respectively.
- The definition of input versus output pins has changed to align with how pins are actually treated during JESD78 testing rather than the simple datasheet pin declarations. Signal pins that are designed or can be configured to receive an external signal during LU testing shall be defined as input pins, otherwise output pins. These are the only two choices.
- Current injection is now achieved either by forcing a current with voltage compliance limit (I-Test) or by applying a voltage with current compliance limit (E-Test). JESD78E only described the I-Test option. This change improves compatibility with the Automotive Electronics Council LU standard Q100-004.
- The MSV concept has been enhanced with a variety of real-life examples on determining MSV in a special annex.
- The problem with the classification and set-up of special pins is addressed by introducing decision diagrams in a special annex, which considers many special pin types such as voltage reference pins, signal pins (formerly called I/O pins) with LDOs and voltage/current sensing pins. JESD78E gave only minimal guidance.
- The concept of "signal pin LU" (i.e., a sustained LU path to or from a signal pin) is touched upon in an informative annex, but a complete incorporation into JESD78 was postponed to a future revision.
- The concept of not allowing any tester supplies to collapse during the applied stress pulse has been extended to all LU tests including the Supply Test. In JESD78E it was only applicable to the Signal Pin Test (or I-test).

Annex A (Informative) Mathematics

A.1 Statistical Meaning

To give an estimate of the statistical relevance of the data collected we consider the margin of error considering the number of responses and confidence level. There are several on-line calculators that can be used for this (see e.g., the SurveyMonkey website [6]). The results are based on the analysis of 70 individual responses that represent the electronics industry. Figure 86 shows the calculated margin of error as a function of the total population for two selected confidence levels. It shows that with the number of responses available the margin of error saturates rather quickly, e.g., to 10% for a 90% confidence level.

This can be interpreted as follows. Suppose for a certain question 60% of the respondents answer ‘yes’. This means that for the full population of the industry we can conclude with 90% confidence that 50-70% of the industry would reply ‘yes’. Alternatively, we can also conclude with 95% confidence that 48-72% would reply ‘yes’.

Since in several cases a single response is often formed by consensus within a (much) larger group of colleagues, this is probably a conservative estimate. Hence, we conclude that the results are statistically relevant.

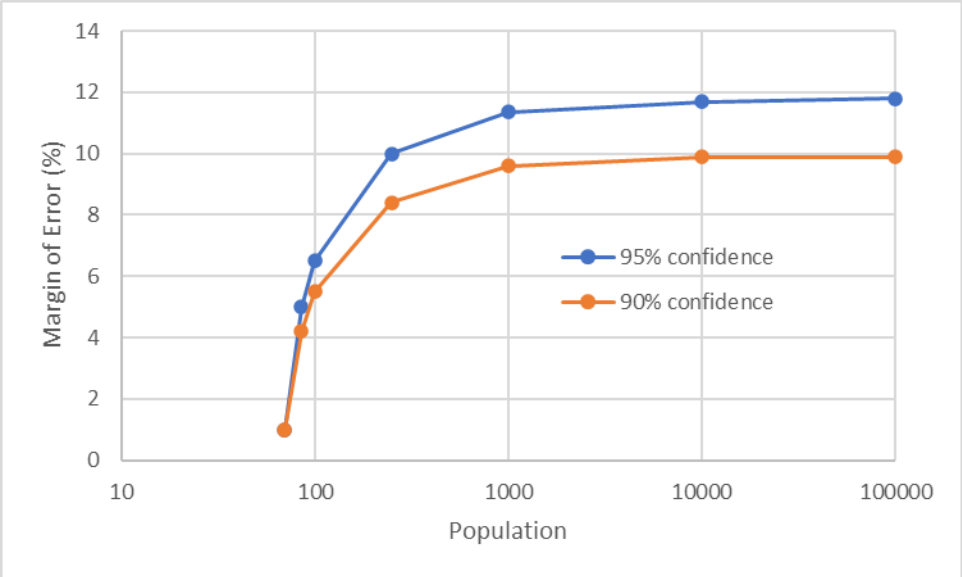


Figure 86 — Margin of Error as Function of Population Size for Two Confidence Levels

A.2 Correlation Metric

It is interesting to compare the responses from two different questions, referred to a "base" and "correlation" questions, to illuminate possible reasons for the response to a certain question. We have defined a metric to quantify such comparisons which can be visualized by the diagrams shown in Figure 87 through-Figure 89.

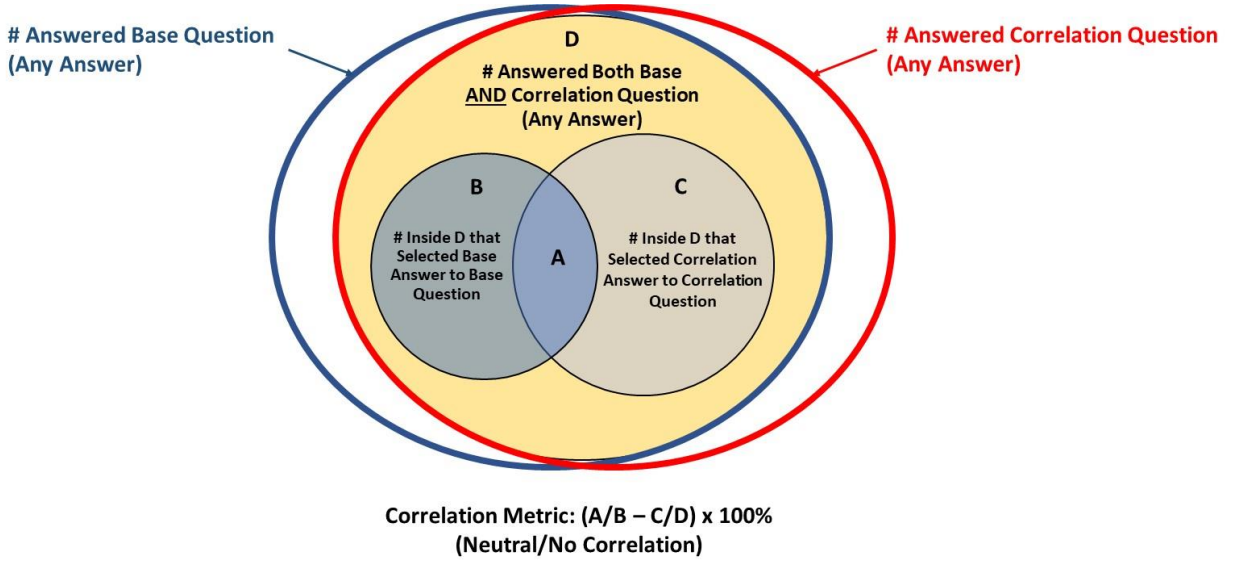


Figure 87 — Correlation Metric: "No Correlation"

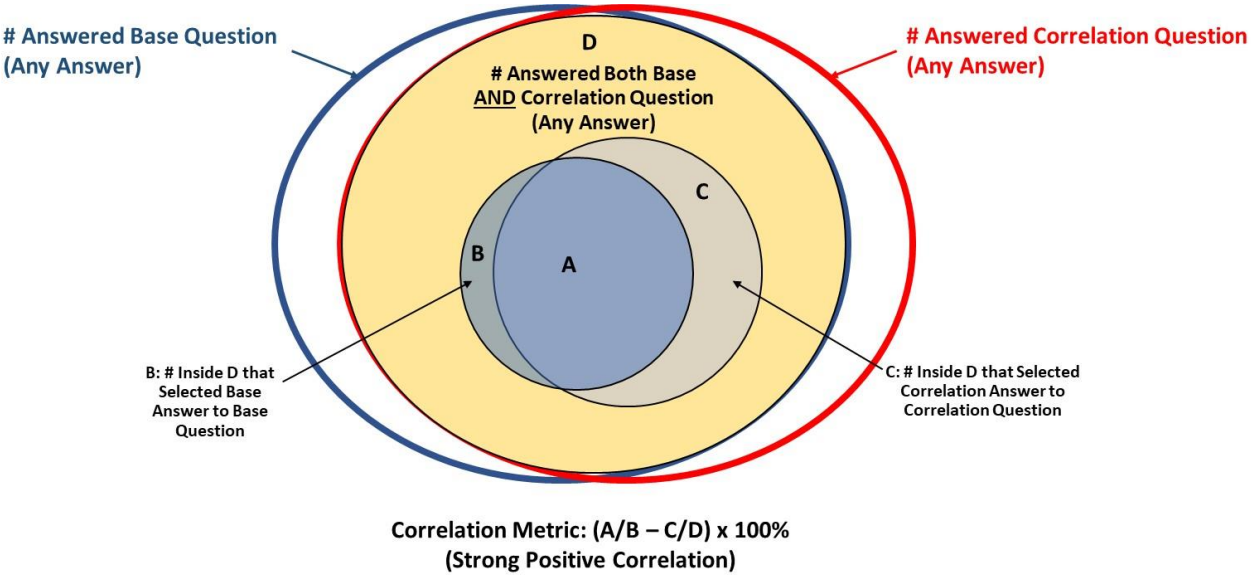


Figure 88 — Correlation Metric: "Strong Positive Correlation"

A.2 Correlation Metric (cont'd)

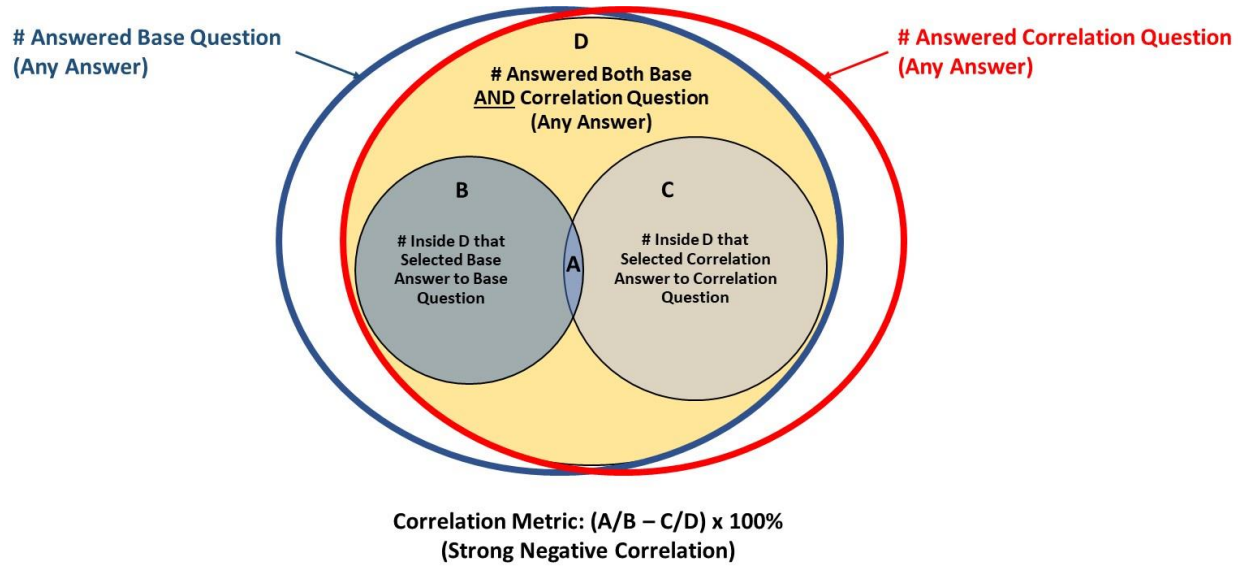


Figure 89 — Correlation Metric: "Strong Negative Correlation"

This correlation metric provides a means of comparing the proportion of the population that selected the base answer to the base question that also selected the correlation answer to the correlation question with the proportion of the general population that selected the correlation question with the correlation answer. The starting point of the comparison is the intersection of the populations that answered both the base and correlation question ("D") and therefore groups "A", "B", and "C" are subsets of "D". Note that the correlation metric is a percentage difference and if the quantity is a positive number, then population B is more likely to select the correlation answer to the correlation question than the general population D. The opposite is true for a negative correlation metric.

As an illustrative example that is relevant for this clause, we can examine the following two question/response pairs:

[Q85] and Response: (referred to as "Base Question" and "Base Response")

- Question: "How do you determine the MSV?"
- Response: "Use product absolute maximum rating (AMR) values."

[Q90] and Response: (referred to as "Correlation Question" and "Correlation Response")

- Question: "Do you set the pin stress voltage limits so that they do not exceed the product AMR?"
- Response: "Yes"

We can use the correlation metric to test the following hypothesis: respondents that use the product AMR to determine MSV are more likely to set the pin stress voltage limits so that they do not exceed the product AMR. The numbers comprising the correlation metric are shown in Table 4.

A.2 Correlation Metric (cont'd)

Table 4 — Correlation Metric for [Q85] and [Q90]

Group	**Number**
Answered Both the Base Question **and** Correlation Question ("D")	59
Selected Base Response ("B")	13
Selected Base Response and Correlation Response ("A")	12
Selected Correlation Response ("C")	42
A/B x 100%	92.3%
C/D x 100% ("Baseline" Percentage Answering w/Correlation Response)	71.2%
CFOM = ([A/B]-[C/D]) x 100%	+ 21.1%

The correlation metric is + 21.1%, which supports this hypothesis. In other words, twelve out of the thirteen (92.3%) respondents who use product AMR values to determine MSV also set the pin stress voltage limits so that they do not exceed the product AMR - a much higher percentage than the general population (71.2%).

As the number of respondents are limited in this survey, we have typically chosen that a minimum population "B" of 10 represent a significant correlation. Furthermore, any correlation metric with magnitudes less than 10% were considered uncorrelated.

Annex B (Informative) Industry Council Survey on Latch-Up

This section provides the original survey as originally published. The formatting does not reflect current JEDEC publication standard.

Industry Council Survey on Latch-up

Introduction

For the past three decades, the JESD78 test standard and related test standards (JESD17, EIAJ ED-4701/306, AEC-Q100-004) have been employed to ensure a safe level of latch-up robustness for semiconductor components prior to large-scale production and subsequent field use. Consequently, JESD78 has been widely accepted as a standard qualification test. For various reasons including technology scaling, increasing amounts of integration, and the complexity and variety of semiconductor components, the standard has faced challenges addressing the needs of the increasingly diverse semiconductor product space. These challenges have prompted the Industry Council on ESD Target Levels, working with the JESD78 Working Group, to investigate the latch-up standard in today's context and ask fundamental questions like: How is the test standard interpreted and executed across the industry? What real life stress events does the test standard consider? Are the recommended qualification levels appropriate? Do we have evidence that the test method is a good predictor of robustness against latch-up in the field? What changes should be made to the standard to better suit the reality of present day and future products?

To this end, an **online survey** was prepared by experts in the industry to help answer these questions. The survey is intended for all individuals in the industry who have some stake in the JESD78 standard including reliability, design, technology, product management, system design, EDA tools, and OEMs. As with any survey, the relevance of the survey results improves with the number of participants, so it is very important to maximize participation. Concerns for confidentiality should not be a barrier for completing the survey as it is **completely anonymous and untraceable** unless the respondent leaves contact information. Respondents that choose to leave a contact email in the survey will receive a copy of the final report from the survey.

Instructions

The survey can be completed by individuals or groups, although to maximize the number of responses, individual participants are preferred. Depending on your role (for example, a test lab), you might have a different list of questions than an individual with a different role (for example, a designer).
The total number of questions ranges between 60 and 100 depending on your role and answers. The survey is divided in 9 sections. Nearly all questions are optional, so partially completed surveys are acceptable. If a question is not applicable or you cannot answer it, it can simply be skipped.
It is estimated that the survey will take approximately 1 hour to complete. The deadline for completion is September 1, 2020.

Radio buttons (for 'choose only one' questions) are indicated by ○
Multiple choice (for 'select all applicable' questions) are indicated by ☐

All questions are numbered sequentially. Mandatory questions are indicated by a *. Most questions are optional. Please skip questions if you do not want to answer or if they are not applicable to you.
Some questions are only applicable depending on the previous answer. That is typically indicated by starting the question like: If yes, ...

Important notes

Due to limitations of the forms tool, the survey cannot be printed or interrupted and saved for completion at a later time. Therefore, it is recommended to print the pdf version and use that to collect your answers. This also allows discussion with your colleagues.

Once you have answers to all questions that you want to address, you open the **on-line survey** and complete the form. Each question starts with [Qxy] indicating the consecutive sequence number in the pdf text. Depending on your answer the actual question number in the survey may differ. Alternatively, you can start the on-line survey and leave it active indefinitely without logging out. While taking the on-line survey, it is possible to go back to previous questions, but there is no 'undo' function.

Links

The online version is available this link:
https://forms.office.com/Pages/ResponsePage.aspx?id=06FuaCu8b0ypLNmcXDAWNd4mfOjifjpOvTIBugeyXKFUMTFCSDQzN1hXRDZHVFJHUlAwSDAwQU5MVy4u
or via this QR code:

1. Affiliation and Background

This section collects some general background information of the respondent

1. Which company do you represent? (Open question)

2. In which country are you working? (Open question)

3. Which market segments does your company serve? *

- ☐ Aerospace
- ☐ Automotive
- ☐ Consumer
- ☐ Industrial
- ☐ Medical
- ☐ Military
- ☐ Other (please specify)

4. What type of business is your company? *

- ☐ Fabless IC Supplier
- ☐ Foundry
- ☐ IC Supplier with Fab
- ☐ IP Provider
- ☐ OEM
- ☐ Test House or Equipment Maker
- ☐ Tier/subsystem
- ☐ Other (please specify)

5. Which IC product types do you support?

- ☐ Very low voltage IC (⩽2V)
- ☐ Low voltage IC (>2 and ⩽5 V)
- ☐ Medium voltage IC (>5 and ⩽12V)
- ☐ High voltage IC (>12V)
- ☐ Analog IC
- ☐ Memory IC
- ☐ Mixed signal IC
- ☐ Power IC
- ☐ RFID/RFIC
- ☐ Other (please specify)

6. How many latch-up related customer complaints does your company receive per year (approximate number)?None

◯ ⩽ 5
◯ 6 to 20
◯ 21 to 50
◯ 51 to 100
◯ > 100
◯ None

7. Are you filling out the survey for the whole company or just a part of it? *

◯ Whole company
◯ Business unit
◯ Product line
◯ Department
◯ Group
◯ Individual

8. Which aspects of the JESD78 test standard are you familiar with?

☐ Pass/Fail criteria
☐ Immunity levels classification
☐ Detailed test procedure
☐ Special pins
☐ Reporting requirements
☐ Maximum stress voltage (MSV)

9. Do you think that the JESD78 standard is useful to prevent system failure caused by over-current or over-voltage in real world scenarios?

◯ Yes, all cases
◯ Yes, some cases (please provide examples)
◯ No

10. Please provide examples of the above reply (open text)

11. Have you experienced latch-up failures?

◯ Yes
◯ No

12. If yes, where have you experienced latch-up failures?

☐ JESD78 testing
☐ Inline screening test (e.g., Burn-in)
☐ Reliability testing other than JESD78 (e.g., HTOL)
☐ Functional test at package-level
☐ Functional test at probe level
☐ System level testing (e.g., IEC 61000-4-x)
☐ Field return
☐ Other (please specify)

2. Case Studies and Field Returns

This section focuses on the occurrence rate and conditions of latch-up failures

13. Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?

◯ Yes, for both I-test and Overvoltage test
◯ Yes, only for I-test
◯ Yes, only for Overvoltage test
◯ No

14. If yes, were the actual stress levels reported to the customer?

◯ Yes
◯ No

15. If yes, did that part have any latch-up related field returns?

◯ Yes (please specify approximate return rate)
◯ No
◯ Too soon to tell (recent qualification)

16. If yes, please specify approximate return rate (open text)

17. If yes, were there any measures taken at the board/system level to mitigate the latch-up risk (e.g., add board-resistor, etc.)?

◯ Yes (please describe)
◯ No

18. If yes, please describe measures taken (open text)

19. For products that have had latch-up failures in the system, what were the operating conditions needed to replicate the failure?

☐ Within maximum operating conditions per datasheet specification

☐ Outside maximum operating conditions, but within absolute maximum ratings (AMR) per datasheet specification

☐ Outside absolute maximum ratings (AMR) per datasheet specification

☐ With System level stress testing (e.g., IEC 61000-4-x)

☐ Other (please specify)

20. For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?

☐ Due to IC design issues (e.g., poor layout), design not fully compliant with latch-up design rules

☐ Due to IC design issues (e.g., poor layout), design compliant with latch-up design rules

☐ Due to a weak board design

☐ Due to the JESD78 test method not sufficiently covering the applied stress type in the system (e.g., transient stress)

☐ Due to the JESD78 test levels (±100mA or 1.5 x Vddmax) not sufficiently covering the applied levels in the system

☐ Other (please specify)

21. What percentage of your company's product re-spins were due to latch-up failures in a system application?

◯ None

◯ ⩽0.1%

◯ >0.1% and ⩽1%

◯ >1% and ⩽5%

◯ >5% and ⩽10%

◯ >10% and ⩽50%

◯ >50%

22. Has your company experienced latch-up EIPD (Electrical Induced Physical Damage) with parts that passed JESD78 testing at the semiconductor supplier?

◯ Yes

◯ No

3. Goal and Testing Strategy

This section focuses on how and why latch-up testing is done

23. Is JESD78 testing a product qualification requirement in your company?

◯ Yes, all products

◯ Yes, only for certain product types (please specify which)

◯ No

◯ No, we do JESD78 testing only as characterization

24. If only for certain product types, please specify (open text)

25. What is the JESD78 test requirement in your company for products that are offered in multiple packages that use the same die?

◯ Test all packages

◯ Test a representative non-production package

◯ QBS (qualification by similarity) of the worst-case package (from a pin count and/or temperature perspective)

◯ Other (please specify)

26. What is the JESD78 test requirement in your company for Multi-Chip Products?

◯ QBS (qualification by similarity) of Multi-Chip Modules with individually qualified dies

◯ QBS (qualification by similarity) of the worst-case Multi-Chip Module (i.e., embedding all dies)

◯ Same qualification procedure as a Single-Chip Module

◯ Other (please specify)

27. What percentage of your company's product has experienced latch-up failures (either in JESD78 qualification testing or in the field)?

◯ None

◯ ⩽0.1%

◯ >0.1% and ⩽1%

◯ >1% and ⩽5%

◯ >5% and ⩽10%

◯ >10% and ⩽50%

◯ >50%

28. What percentage of your company's product re-spins were due to failures during JESD78 qualification test?

◯ None
◯ ⩽0.1%
◯ >0.1% and ⩽1%
◯ >1% and ⩽5%
◯ >5% and ⩽10%
◯ >10% and ⩽50%
◯ >50%

29. What percentage of your company's product re-spins were due to latch-up failures during application related functional or reliability testing (not caught by JESD78 testing)?

◯ None
◯ ⩽0.1%
◯ >0.1% and ⩽1%
◯ >1% and ⩽5%
◯ >5% and ⩽10%
◯ >10% and ⩽50%
◯ >50%

30. What is the goal of the supply overvoltage test and IO (signal pin) injection test in the present JESD78 standard?

☐ Robustness against millisecond time range disturbances
☐ Robustness against nanosecond to microsecond time range disturbances
☐ Robustness against generic external disturbances (voltage-driven/low-impedance source or current-driven/high-impedance source)
☐ Robustness against system-internal disturbances (e.g., transmission line reflections, inductive overshoots, etc.)
☐ Other (please specify)

31. Does the JESD78 testing address real world stress events like HBM and CDM do?

◯ Yes
◯ No

32. If JESD78 testing were removed as a qualification requirement for the industry, what would happen?

◯ Components would be less reliable in the field (please specify why)
◯ It would have no effect (please specify why)

33. Please specify why (open text)

34. Do you require detailed JESD78 information from an IC Supplier?

◯ Yes, detailed information is needed

◯ No, JESD78 compliance is just a check box item

35. Do you scrutinize the JESD78 information provided by an IC Supplier?

☐ Review of the datasheet or qualification report

☐ Require a minimum robustness level for all pins

☐ Review of the vendor's JESD78 test program and pin-by-pin results

☐ Focused test review on high risk pins in the system

☐ Yes, and we repeat JESD78 testing on supplied parts

☐ Other (please specify)

36. How are JESD78 test results provided in an IC Supplier datasheet or qualification report used for system design?

◯ Limit the on-board currents

◯ Limit the on-board overshoots

◯ Limit both the on-board currents and overshoots

◯ Not used

◯ Other (please specify)

37. Would increasing the overvoltage or injection current levels of JESD78 decrease the latch-up failures in the field?

◯ Yes

◯ No

38. Is the operational state of an IC used during JESD78 testing (i.e., low power mode, stable current) representative of real-world applications?

◯ Yes

◯ No (please specify why)

39. If not, please specify why not (open text)

40. If a product has multiple modes of operation, how does your company test for JESD78 latch-up?

☐ In all pin functional modes (e.g., digital and analog on the same IO)

☐ In all IC functional modes (e.g., full power, partial power down, etc.)

☐ In permanent reset mode

☐ In default IC and pin functional mode after reset/power up

☐ Other (please specify)

41. Does passing JESD78 testing guarantee latch-up robustness in the field?

◯ Yes

◯ No

42. If no, what other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?

☐ Cable discharge
☐ Single event latch-up (SEL)
☐ System level stress
☐ Transient latch-up (CDM/System level time scale)
☐ Inductive load switching
☐ Power-up conditions/ground reference differences
☐ Other (please specify)

4. Next steps of Latch-up testing

This section collects inputs for possible new directions of latch-up testing

43. What other types of latch-up tests does your company perform to qualify a product?

☐ Cable discharge
☐ Single event latch-up (SEL)
☐ System level stress
☐ Transient latch-up (CDM/System level time scale)
☐ Inductive load switching
☐ Power-up conditions/ground reference differences
☐ Other (please specify)

44. If new latch-up testing methods were to be developed in the future what would be your preference? *

◯ Keep present JESD78, nothing else needed

◯ Keep present JESD78 and add new standard(s) covering the above selected events

◯ Keep present JESD78 and include new settings/tests covering the above selected events

◯ Replace present JESD78 by a new test method(s) covering the above selected events

◯ Other (please specify)

45. Often, power supplies in applications are not capable of sinking current and can only source current. Such supplies would limit positive injection current into the IO pin in the application. Should the standard take into account the ability of a supply to sink current when defining current injection level for qualification?

◯ Yes

◯ No

46. If a JESD78 stress condition results in a sustained decreased current, should it be considered as a JESD78 failure reason?

◯ Yes

◯ No

47. Which of the following circuit elements, if turning on and causing the sustained increased current, should be considered JESD78 failure reasons?

☐ Parasitic thyristor
☐ Designed thyristor (SCR)
☐ Bipolar (parasitic or designed)
☐ Latching BigFET trigger circuit
☐ Other latching circuitry (please specify)
☐ Anything that causes increased supply current

48. If you selected 'Other latching circuitry', please give examples of latching circuits that should be considered a failure in the above situation (open text)

49. Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?

◯ Yes

◯ No

50. Which conditions should be included in this new test method(s)?

☐ Sustained high current states
☐ System resets
☐ Temperature (room/hot/cold)
☐ Process corners
☐ Other (please specify)

51. As the supply voltage of ICs keeps shrinking, below about 2V the 100mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Does this lead to latch-up risks in the application?

◯ Yes (please specify why)

◯ No

◯ I was not aware of this

52. If yes, please specify why (open text)

53. At what minimum JESD78 current injection level are your company's products safe for final application?

◯ ⩾ |± 10mA|
◯ ⩾ |± 50mA|
◯ ⩾ |± 100mA|
◯ ⩾ |± 200mA|
◯ Depending on pin current capability (please specify)
◯ Depending on pin function (please specify)
◯ Other (please specify)

54. Please specify the above answer (open text)

55. At what minimum JESD78 over-voltage level are your company's products safe for final application?

◯ ⩾ 1.1xVddmax
◯ ⩾ 1.25xVddmax
◯ ⩾ 1.5xVddmax
◯ ⩾ 1.75xVddmax
◯ Depending on supply voltage capability (please specify)
◯ Other (please specify)

56. Please specify the above answer (open text)

5. Reporting and design rules

This section explores how latch-up testing results are reported and used

57. How does your company report latch-up test results to customers?

◯ Report passing JESD78 in datasheet
◯ Report passing JESD78 immunity level in datasheet
◯ Report passing JESD78 in qualification report
◯ Report passing JESD78 immunity level in qualification report
◯ Report the achieved injection current and voltage levels for pins or pin groups in the datasheet
◯ Report the achieved injection current and voltage levels for pins or pin groups in the qualification report
◯ No JESD78 results reported
◯ Other (please specify)

58. Does the latch-up robustness level given in the datasheet of an IC impact the purchase decision?

◯ Yes
◯ No
◯ Yes, only for certain applications (please specify)

59. If only for certain applications, please specify which type of applications (open text)

60. What is the most common action that your company takes in case of JESD78 failure?

◯ Fix latch-up issue in design revision
◯ Derate reported latch-up levels
◯ Document in application note
◯ Internal use only
◯ Derate AMR (absolute maximum ratings) in datasheet
◯ Establish MSV (maximum stress voltage) below which there are no failures
◯ Other (please specify)

61. Should latch-up IC design rules be exclusively driven by the JESD78 requirements?

◯ Yes (with current JESD78 specification)
◯ Yes (with future improved JESD78 specification)
◯ No (please explain why)

62. If no, please explain why not (open text)

63. As the supply voltage of ICs keeps shrinking, below about 2V the 100mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Should design rules be relaxed in such scenario?

◯ Yes (please specify why)
◯ No (please specify why)
◯ It depends on the application (please specify)

64. Please specify the above answer (open text)

65. If you pass all latch-up design rules, what does it guarantee?

☐ Pass JESD78 testing
☐ No latch-up issues in the system/field
☐ Other (please specify)

6. Test execution details

This section asks specific questions on how latch-up tests are executed

66. The JESD78 standard requires the following clamping limit to be applied during overvoltage testing: (a) Iclamp = 100 mA + Inom or (b) Iclamp = 1.5 x Inom, whichever one is higher. Does your company follow this requirement?

◯ Yes, for all tester supplies
◯ Yes, but only for supply under test
◯ No, use higher value (please specify)
◯ No, use lower value (please specify)

67. Please specify the above answer (open text)

68. At what maximum temperature does your company perform JESD78 testing?

◯ Maximum ambient operating temperature per datasheet
◯ Maximum case operating temperature per datasheet
◯ Maximum junction operating temperature per datasheet
◯ Room temperature only
◯ It depends on market segment (please specify)

69. In case of 'it depends', please specify the above answer (open text)

70. Which latch-up standard does your company use? *

☐ JESD78E
☐ Older JESD78 (please specify version)
☐ AEC Q100-004 (please specify version)
☐ EIAJ ED-4701/300-2 method 306 (JEITA)
☐ IEC 60749-29
☐ Other (please specify)

71. If you selected 'Older JESD78' or 'AEC Q100-004', please specify the above answer (open text)

72. Which pin types should be exempt from JESD78 testing?

☐ Pins that are only connected to passive RC components (see JESD78E annex A)
☐ Reset pins
☐ Probe-only pins (i.e., exposed for engineering/debug purposes only)
☐ Flash programming pins (i.e., that are unavailable to the end customer)
☐ Clock pins
☐ IO Pins that are always connected to a VDD or VSS supply in the system, as required by the datasheet
☐ Other (please specify)

73. Which pulse duration do you select during JESD78 testing?

◯ The minimum of the tester (please specify)

◯ The maximum of the tester (please specify)

◯ The default value of the tester (please specify)

◯ Another fixed value (please specify)

◯ Product/pin specific value (please specify)

◯ Other (please specify)

74. Please specify the above answer (open text)

75. What information is needed to create a JESD78 compliant stress test program?

☐ JESD78 standard document

☐ Product datasheet

☐ Product application notes

☐ Product design technology information

☐ Other (please specify)

76. Do latch-up tester data logs (current and voltage) get reviewed in your company?

◯ Yes, in all cases to ensure the test program is correct

◯ Yes, in all cases to ensure the test program is correct and program execution follows the JESD78 standard

◯ Yes, only when test outcome is a failure (either during stress or post stress functional testing)

◯ No

77. How do you systematically ensure that JESD78 testing is executed properly?

☐ Curve trace signal pins to ensure their correct impedance state

☐ Review tester data log (voltage and current pre-/during-/post- stress)

☐ Use oscilloscope to monitor voltage and/or current waveforms on representative pins

☐ Compare vector readback with expected vector stream

☐ No specific checking performed - just execute test program

☐ Other (please specify)

78. What do you systematically measure/monitor during JESD78 testing?

☐ Injected current/overvoltage reaches programmed value

☐ Supply voltage collapse during stress

☐ Abnormal supply and signal pin current/voltage during stress

☐ Voltage/current compliance reached

☐ Post-stress currents decrease

☐ Other (please specify)

79. How do you measure/monitor the parameters you selected above?

◯ Data log review

◯ Oscilloscope

◯ Other (please specify)

80. How does your company test products with signal pins that are exposed to external energy paths (e.g., USB; HDMI; etc.) or have an inductive load?

◯ Test at the same level as all the other pins

◯ Test at fixed levels higher than ± 100mA and 1.5 x Vddmax

◯ Test at higher level depending on expected current in the application

◯ Test only with final application board (no JESD78 testing done)

◯ Other (please specify)

81. For low-voltage (LV) signal pins, the applicable voltage clamping limits of JESD78, Table 2 may reduce the injected current below the set target level (e.g., ± 100 mA). With a maximum supply voltage below about 2V, the injected current may even become zero. Do you strictly apply the Table 2 voltage limits?

◯ Strictly apply Table 2 voltage limits, even if very little current gets injected into the signal pin

◯ Characterize beyond Table 2 voltage limits until reaching the maximum stress voltage (MSV)

◯ Characterize beyond Table 2 voltage limits until reaching a pre-defined injection current target (please specify)

◯ Other (please specify)

82. Please specify the above answer (open text)

83. If you characterize LV pins beyond the voltage limits of JESD78, Table 2, do you apply this extended test method for product qualification and document the extended spec limits in the latch-up report?

◯ No, do not test LV pins beyond Table 2 limits

◯ No, the testing beyond spec limits is only done for internal characterization

◯ Yes, apply extended spec limits, but do not mention them in latch-up report

◯ Yes, apply extended spec limits and document them in latch-up report

◯ Other (please specify)

84. Do you setup the JESD78 test program to check if the injected signal pin itself suffered from latch-up (“signal pin latch-up”)?

◯ No, only consider latch-up on power supply pins

◯ Yes, also check "signal pin latch-up"

◯ Other (please specify)

7. Maximum Stress Voltage (MSV)

Maximum stress voltage (MSV) is a latch-up specific term. The questions assess how this is perceived and used in practice.

85. The concept of maximum stress voltage (MSV) allows one to differentiate between latch-up and EOS (electrical overstress). The conventional pin voltage limits during JESD78 testing may be reduced to the MSV. How do you determine the MSV?

- ◯ Do not use MSV
- ◯ Dedicated MSV test procedure - step up voltage until damage
- ◯ Adjust voltage limits during JESD78 testing until it passes
- ◯ Use product absolute maximum rating (AMR) values
- ◯ Use technology absolute maximum rating (AMR) values (typically provided by fab/foundry)
- ◯ Simulations
- ◯ Other (please specify)

86. For determining the MSV, do you confirm that the damage is from a stress mechanism not directly related to latch-up (as required by the JESD78 standard)?

- ◯ No
- ◯ Yes, with physical failure analysis (FA)
- ◯ Yes, by other means (please specify)

87. In case of ‘other means’, please specify the above answer (open text)

88. Which (irreversible) damage conditions do you find acceptable for invoking the MSV?

- ☐ Interconnect (metal, bonding, via) failure
- ☐ P-N junction breakdown
- ☐ Gate oxide rupture
- ☐ Bipolar snapback
- ☐ Other (please specify)

89. How often do you encounter a product where the MSV reduces the injected current below the set target level (e.g., ± 100mA)?

- ◯ Most of the time
- ◯ Often
- ◯ Sometimes
- ◯ Rarely
- ◯ Never
- ◯ Do not use MSV

90. Do you set the pin stress voltage limits so that they do not exceed the product AMR?

◯ Yes, if damage occurs while exceeding the AMR, it is not a latch-up failure

◯ No, the AMR is not applicable to latch-up testing

8. Failure criteria

This section collects questions on determining pass/fail results of JESD78 testing.

91. If latch-up occurs during the stress pulse (but not sustained), should that be considered a failure?

◯ Yes

◯ No

◯ It depends (please explain)

92. Please specify 'It depends' (open text)

93. What are common causes of rejecting a JESD78 pass/fail result?

☐ Incorrect specification/request
☐ Setup instability
☐ Current or Voltage instability during the stress
☐ Desired injection levels not reached
☐ MSV exceeded
☐ Tester instability
☐ Latching not due to parasitic thyristor
☐ Other (please specify)

94. Do you use functional test (ATE test) to verify device specification requirements after latch-up testing to confirm pass/fail result from tester?

◯ Yes

◯ Yes, but do not count as failure

◯ No

9. Conclusion

This is the last section of the survey. Please take some time to consider entering suggestions, feedback, or recommendations. If you leave your email address you will receive a copy of the final report as soon as it is ready.

95. Feel free to enter any suggestions/recommendations (open text)

96. Please provide your email address to receive a copy of the final report on this survey (open text)

Annex C (Informative) Response Summary

This annex provides the full summary of all responses as provided by MS Forms, made anonymous by removing all references to people, companies or countries.

Textual answers are not provided in the summary, but have been used for the analysis presented in Clause 5. Responses to [Q95] have been presented in full in Clause 5.8.

This annex provides the response summary as originally published. The formatting does not reflect current JEDEC publication standard.

Industry Council Survey on Latch-up

70
Responses

Closed
Status

1. [Q01] Which company do you represent?

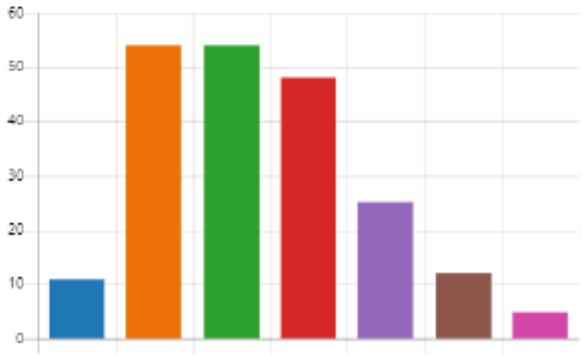
57
Responses

2. [Q02] In which country are you working?

65
Responses

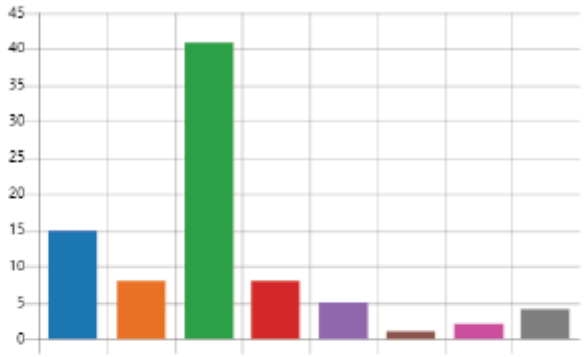
3. [Q03] Which market segments does your company serve?

Aerospace	11
Automotive	54
Consumer	54
Industrial	48
Medical	25
Military	12
Other	5



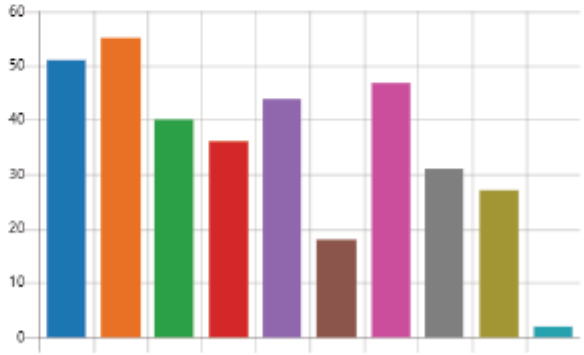
4. [Q04] What type of business is your company?

Fabless IC Supplier	15
Foundry	8
IC Supplier with Fab	41
IP Provider	8
OEM	5
Test House or Equipment Maker	1
Tier/subsystem	2
Other	4



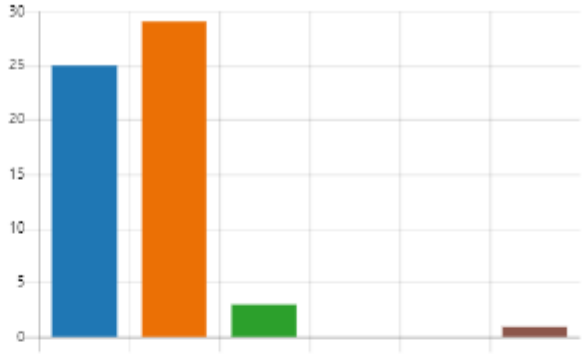
5. [Q05] Which IC product types do you support?

Very low voltage IC (≤ 2V)	51
Low voltage IC (>2 and ≤5 V)	55
Medium voltage IC (>5 and ≤...	40
High voltage IC (>12V)	36
Analog IC	44
Memory IC	18
Mixed signal IC	47
Power IC	31
RFID/RFIC	27
Other	2



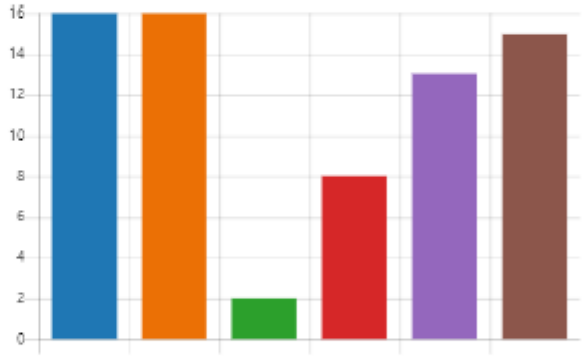
6. [Q06] How many latch-up related customer complaints does your company receive per year (approximate number)?

None	25
< 5	29
6 to 20	3
21 to 50	0
51 to 100	0
> 100	1



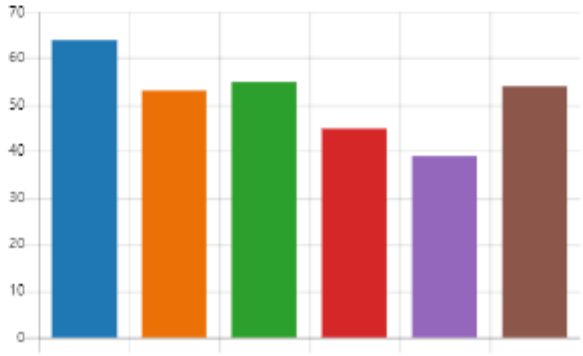
7. [Q07] Are you filling out the survey for the whole company or just a part of it?

Whole company	16
Business unit	16
Product line	2
Department	8
Group	13
Individual	15



8. [Q08] Which aspects of the JESD78 test standard are you familiar with?

Pass/Fail criteria	64
Immunity levels classification	53
Detailed test procedure	55
Special pins	45
Reporting requirements	39
Maximum stress voltage (MSV)	54



9. [Q09] Do you think that the JESD78 standard is useful to prevent system failure caused by over-current or over-voltage in real world scenarios?

Yes, all cases	17
In some cases (please provide ...	44
No	5

10. [Q10] Please provide examples of the above reply

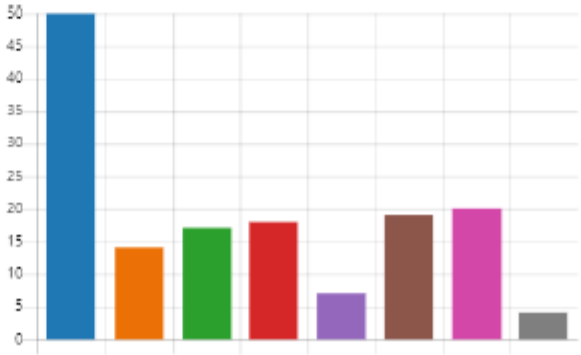
45
Responses

11. [Q11] Have you experienced latch-up failures?

Yes	59
No	10

12. [Q12] If yes, where have you experienced latch-up failures?

JESD78 testing	50
Inline screening test (e.g. Burn...	14
Reliability testing other than J...	17
Functional test at package-level	18
Functional test at probe level	7
System level testing (e.g. IEC 6...	19
Field return	20
Other	4



13. [Q13] Has your company qualified products with Immunity Level B, as defined in Table 1 of JESD78E?

Yes, for both I-test and Overv...	23
Yes, only for I-test	7
Yes, only for Overvoltage test	0
No	28
No answer	9

14. [Q14] If yes, were the actual stress levels reported to the customer?

Yes	25
No	5

15. [Q15] If yes, did that part have any latch-up related field returns?

Yes (please specify approximat...	1
No	17
Too soon to tell (recent qualifi...	6

16. [Q16] If yes, please specify approximate return rate

1
Responses

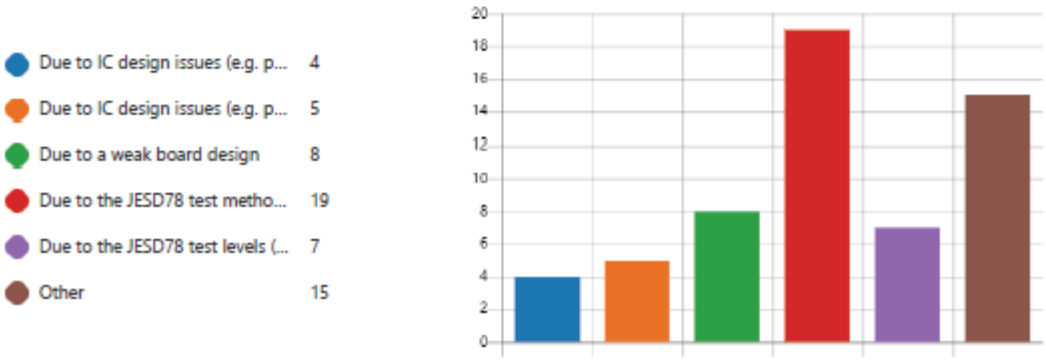
17. [Q17] If yes, were there any measures taken at the board/system level to mitigate the latch-up risk (e.g. add board-resistor, etc.)?

18. [Q18] If yes, please describe the measures taken

0
Responses

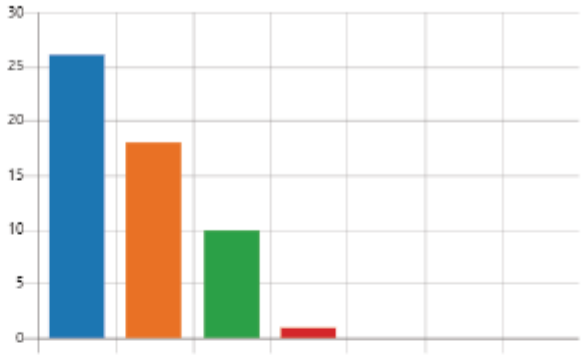
19. [Q19] For products that have had latch-up failures in the system, what were the conditions needed to replicate the failure?

20. [Q20] For products that have had latch-up failures in the system, but had passed JESD78 testing, what was the root cause?



21. [Q21] What percentage of your company's product respins were due to latch-up failures in a system application?

None	26
≤0.1%	18
>0.1% and ≤1%	10
>1% and ≤5%	1
>5% and ≤10%	0
>10% and ≤50%	0
>50%	0



22. [Q22] Has your company experienced EIPD (Electrical Induced Physical Damage) related to latch-up with parts that passed JESD78 testing at the semiconductor supplier?

Yes	20
No	38

23. [Q23] Is JESD78 testing a product qualification requirement in your company?

Yes, all products	55
Yes, only for certain product ty...	7
No	3
No, we do JESD78 testing only...	1

24. [Q24] If only for certain product types, please specify

14
Responses

25. [Q25] What is the JESD78 test requirement in your company for products that are offered in multiple packages that use the same die?

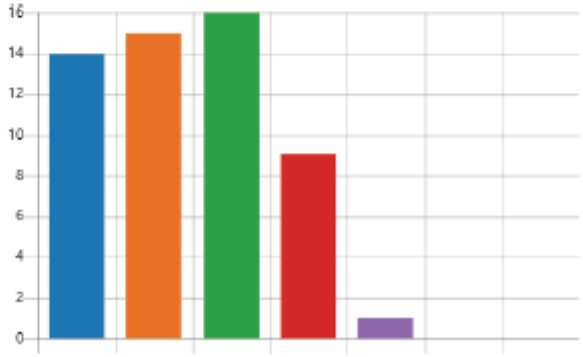
Test all packages	25
Test a representative non-pro...	8
QBS (qualification by similarity...	25
Other	5

26. [Q26] What is the JESD78 test requirement in your company for Multi-Chip Products?

QBS (qualification by similarity...	8
QBS (qualification by similarity...	9
Same qualification procedure ...	33
Other	11

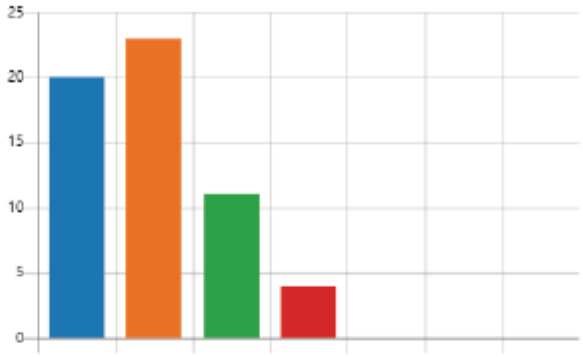
27. [Q27] What percentage of your company's products has experienced latch-up failures (either in JESD78 qualification testing or in the field)?

None	14
≤0.1%	15
>0.1% and ≤1%	16
>1% and ≤5%	9
>5% and ≤10%	1
>10% and ≤50%	0
>50%	0



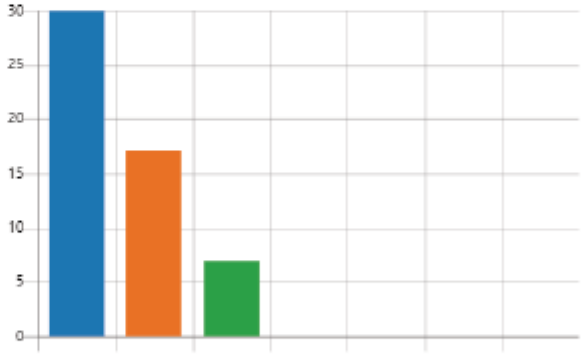
28. [Q28] What percentage of your company's product respins were due to failures during JESD78 qualification test?

None	20
≤0.1%	23
>0.1% and ≤1%	11
>1% and ≤5%	4
>5% and ≤10%	0
>10% and ≤50%	0
>50%	0



29. [Q29] What percentage of your company's product respins were due to latch-up failures during application-related functional or reliability testing (not caught by JESD78 testing)?

None	30
≤0.1%	17
>0.1% and ≤1%	7
>1% and ≤5%	0
>5% and ≤10%	0
>10% and ≤50%	0
>50%	0

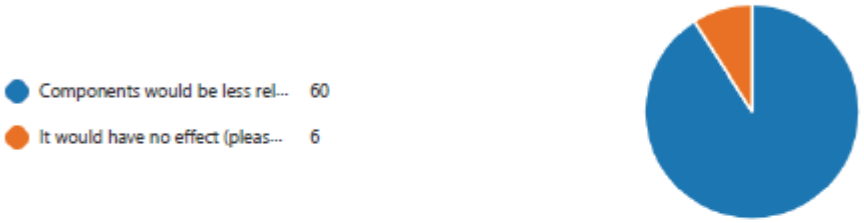


30. [Q30] What is the goal of the supply overvoltage test and IO (signal pin) injection test in the present JESD78 standard?

Robustness against millisecon...	31
Robustness against nanoseco...	13
Robustness against generic ex...	42
Robustness against system-int...	24
Other	4

31. [Q31] Does the JESD78 testing address real world stress events like HBM and CDM do?

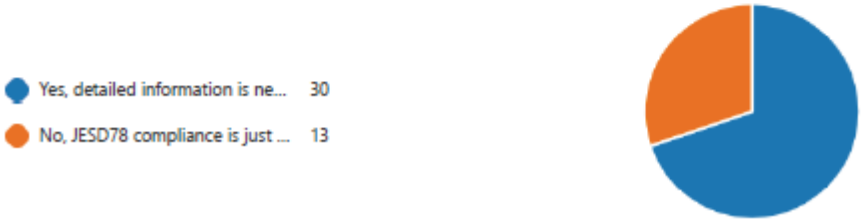
32. [Q32] If JESD78 testing were removed as a qualification requirement for the industry, what would happen?



33. [Q33] Please specify why

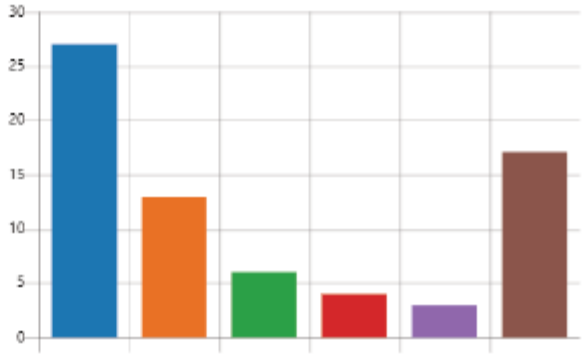
52
Responses

34. [Q34] Do you require detailed JESD78 information from an IC supplier?



35. [Q35] Do you scrutinize the JESD78 information provided by an IC Supplier?

Yes, review of the datasheet or...	27
Yes, require a minimum robust...	13
Yes, review of the vendor's JES...	6
Yes, focused test review on hi...	4
Yes and we repeat JESD78 test...	3
Other	17



36. [Q36] How are JESD78 test results provided in an IC Supplier datasheet or qualification report used for system design?

Limit the on-board currents	2
Limit the on-board overshoots	1
Limit both the on-board curre...	22
Not used	9
Other	9

37. [Q37] Would increasing the overvoltage or injection current levels of JESD78 decrease the latch-up failures in the field?

Yes	18
No	37

38. [Q38] Is the operational state of an IC used during JESD78 testing (i.e. low power mode, stable current) representative of real-world applications?

Yes	32
No (please specify why)	28

39. [Q39] If not, please specify why not

28
Responses

40. [Q40] If a product has multiple modes of operation, how does your company test for JESD78 latch-up?

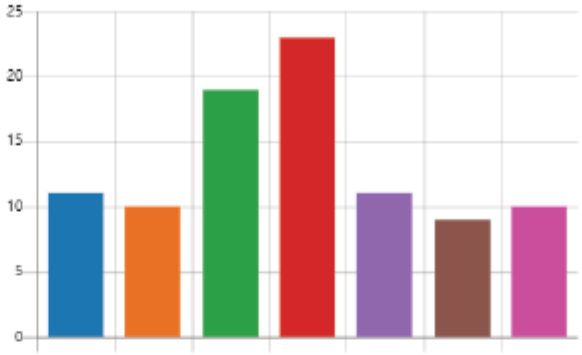
In all pin functional modes (e....	14
In all IC functional modes (e.g....	8
In permanent reset mode	14
In default IC and pin functiona...	25
Other	13

41. [Q41] Does passing JESD78 testing guarantee latch-up robustness in the field?

Yes	25
No	37

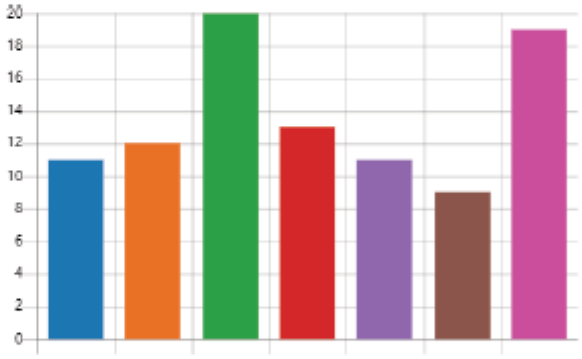
42. [Q42] If no, what other tests should complement the JESD78 testing to guarantee latch-up robustness in the field?

Cable discharge	11
Single event latch-up (SEL)	10
System level stress	19
Transient latch-up (CDM/Syste...	23
Inductive load switching	11
Power-up conditions/ground r...	9
Other	10



43. [Q43] What other types of latch-up tests does your company perform to qualify a product?

Cable discharge	11
Single event latch-up (SEL)	12
System level stress	20
Transient latch-up (CDM/Syste...	13
Inductive load switching	11
Power-up conditions/ground r...	9
Other	19



44. [Q44] If new latch-up testing methods were to be developed in the future what would be your preference?

Keep present JESD78, nothing...	8
Keep present JESD78 and add ...	17
Keep present JESD78 and incl...	29
Replace present JESD78 by a n...	7
Other	9

45. [Q45] Often, power supplies in applications are not capable of sinking current and can only source current. Such supplies would limit positive injection current into the IO pin in the application.
Should the standard take into account the ability of a supply to sink current when defining current injection level for qualification?

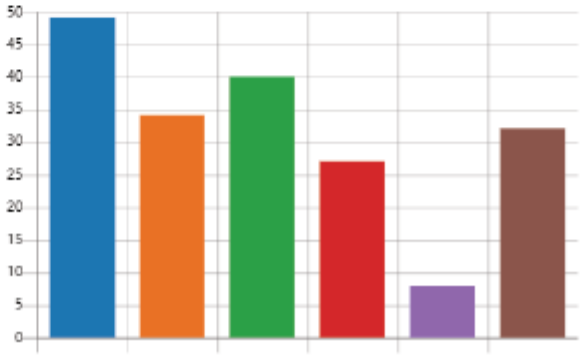
Yes	40
No	21

46. [Q46] If a JESD78 stress condition results in a sustained decreased current, should it be considered as a JESD78 failure reason?

Yes	31
No	26

47. [Q47] Which of the following circuit elements, if turning on and causing the sustained increased current, should be considered JESD78 failure reasons

Parasitic thyristor	49
Designed thyristor (SCR)	34
Bipolar (parasitic or designed)	40
Latching BigFET trigger circuit	27
Other latching circuitry (pleas...	8
Anything that causes increase...	32



48. [Q48] If you selected 'Other latching circuitry', please give examples of latching circuits that should be considered a failure in the above situation

9
Responses

49. [Q49] Is there a need for new test method(s) that specifies generic current injection and overvoltage testing, not limited to latch-up as the root cause?

Yes	26
No	30

50. [Q50] Which conditions should be included in this new test method(s)?

Sustained high current states	21
System resets	18
Temperature (room/hot/cold)	24
Process corners	8
Other	14

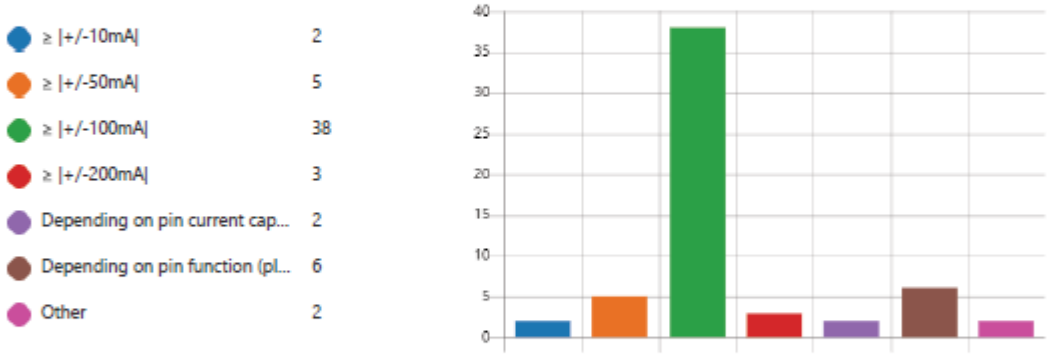
51. [Q51] As the supply voltage of ICs keeps shrinking, below about 2V the 100mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Does this lead to latch-up risks in the application?

Yes (please specify why)	14
No	34
I was not aware of this	9

52. [Q52] If yes, please specify why

16
Responses

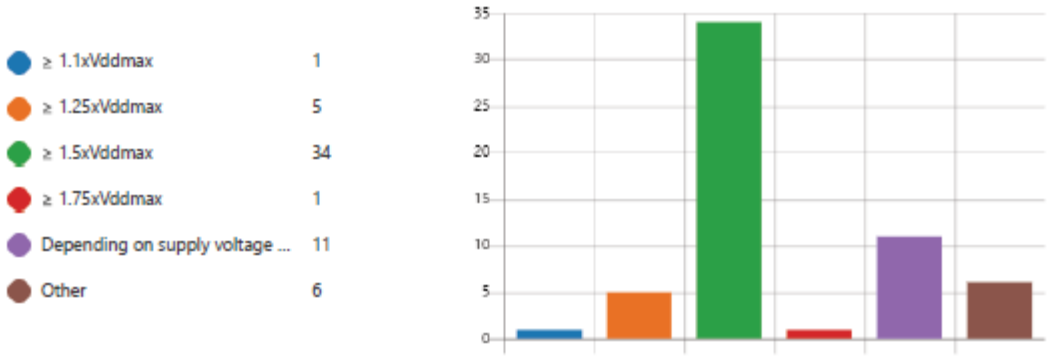
53. [Q53] At what minimum JESD78 current injection level are your company's products safe for final application?



54. [Q54] Please specify the above answer

16
Responses

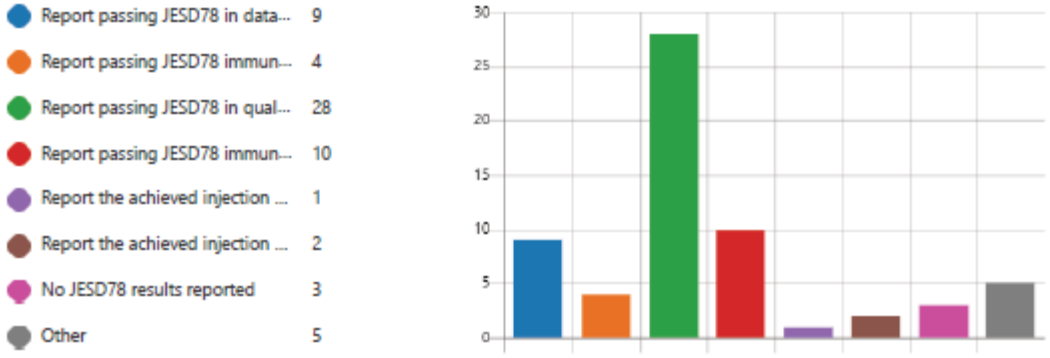
55. [Q55] At what minimum JESD78 over-voltage level are your company's products safe for final application?



56. [Q56] Please specify the above answer

21
Responses

57. [Q57] How does your company report latch-up test results to customers?



58. [Q58] Does the latch-up robustness level given in the datasheet of an IC impact the purchase decision?

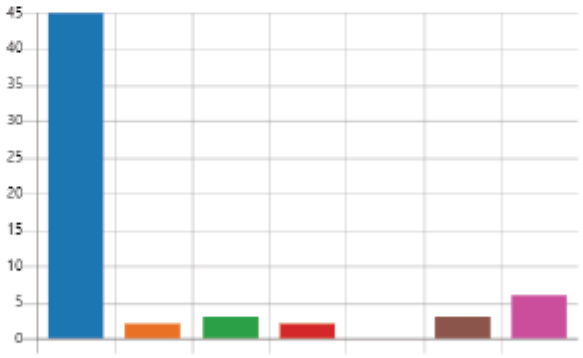
Yes	27
No	13
Yes, only for certain applicatio...	6

59. [Q59] If only for certain applications, please specify which type of applications

8
Responses

60. [Q60] What is the most common action that your company takes in case of JESD78 failure?

Fix latch-up issue in design re...	45
Derate reported LU levels	2
Document in application note	3
Internal use only	2
Derate AMR (absolute maxim...	0
Establish MSV (maximum stres...	3
Other	6



61. [Q61] Should latch-up IC design rules be exclusively driven by the JESD78 requirements?

Yes (with current JESD78 speci...	22
Yes (with future improved JES...	27
No (please explain why)	12

62. [Q62] If no, please explain why not

13
Responses

63. [Q63] As the supply voltage of ICs keeps shrinking, below about 2V the 100mA target injection level of the JESD78 test cannot be reached because of the voltage clamping limit or the MSV. Should design rules be relaxed in such scenario?

Yes (please specify why)	19
No (please specify why)	17
It depends on the application ...	18

64. [Q64] Please specify the above answer

41
Responses

65. [Q65] If you pass all latch-up design rules, what does it guarantee?

Pass JESD78 testing	44
No latch-up issues in the syste...	4
Other	17

66. [Q66] The JESD78 standard requires the following clamping limit to be applied during overvoltage testing: (a) Iclamp = 100 mA + Inom or (b) Iclamp = 1.5 x Inom, whichever one is higher. Does your company follow this requirement?

Yes, for all tester supplies	47
Yes, but only for supply under ...	12
No, use higher value (please s...	5
No, use lower value (please sp...	1

67. [Q67] Please specify the above answer

10
Responses

68. [Q68] At what maximum temperature does your company perform JESD78 testing?

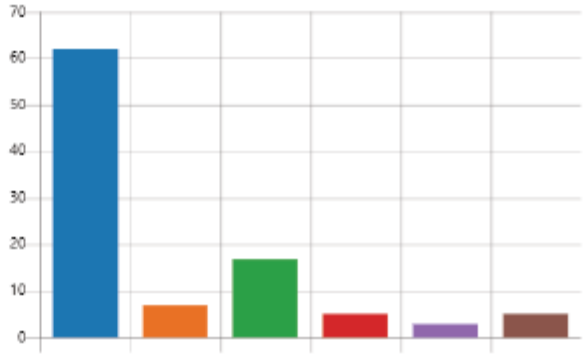
Maximum ambient operating ...	27
Maximum case operating tem...	1
Maximum junction operating t...	22
Room temperature only	4
It depends on market segmen...	8

69. [Q69] In case of 'it depends', please specify the above answer

7
Responses

70. [Q70] Which latch-up standard does your company use?

JESD78E	62
Older JESD78 (please specify v...	7
AEC Q100-004 (please specify ...	17
EIAJ ED-4701/300-2 method 3...	5
IEC 60749-29	3
Other	5

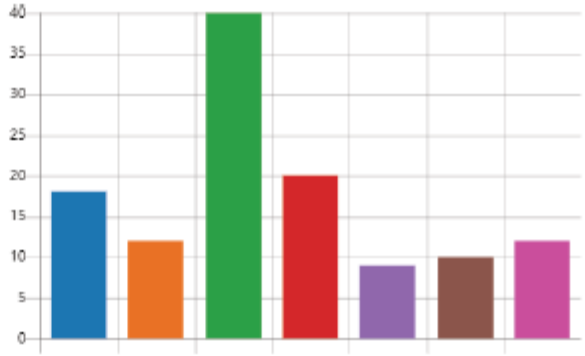


71. [Q71] If you selected 'Older JESD78 or 'AEC Q100-004', please specify the above answer

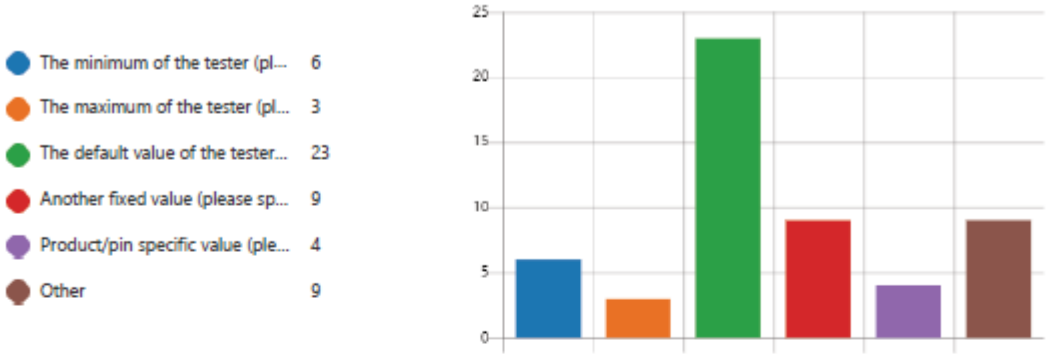
10
Responses

72. [Q72] Which pin types should be exempt from JESD78 testing?

Pins that are only connected t...	18
Reset pins	12
Probe-only pins (i.e. exposed f...	40
Flash programming pins (i.e. t...	20
Clock pins	9
IO Pins that are always connec...	10
Other	12



73. [Q73] Which pulse duration do you select during JESD78 testing?

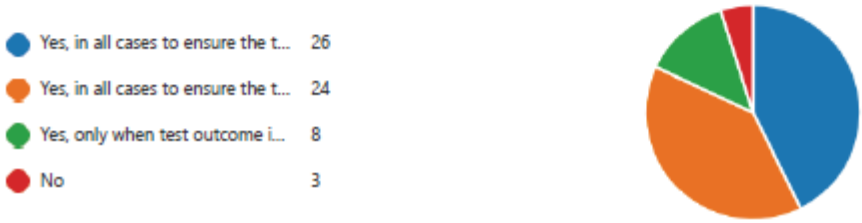


74. [Q74] Please specify the above answer

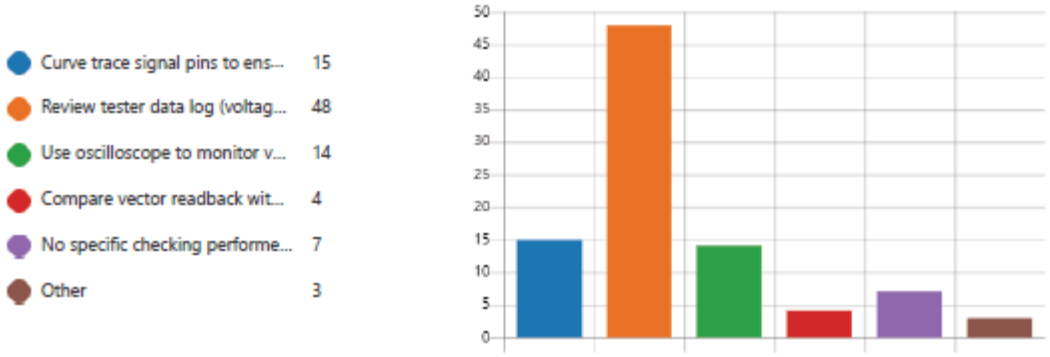
36
Responses

75. [Q75] What information is needed to create a JESD78 compliant stress test program?

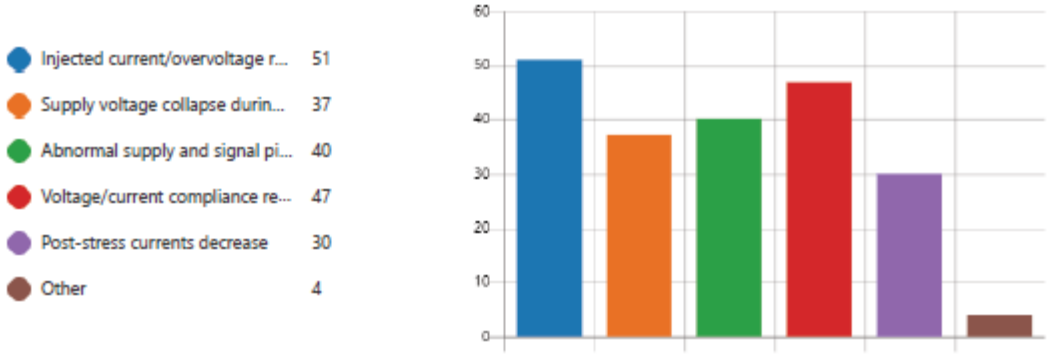
76. [Q76] Do latch-up tester data logs (current and voltage) get reviewed in your company?



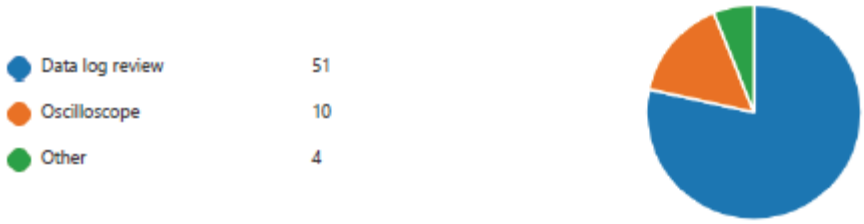
77. [Q77] How do you systematically ensure that JESD78 testing is executed properly?



78. [Q78] What do you systematically measure/monitor during JESD78 testing?



79. [Q79] How do you measure/monitor the parameters you selected above?



80. [Q80] How does your company test products with signal pins that are exposed to external energy paths (e.g. USB; HDMI; etc.) or have an inductive load?

81. [Q81] For low-voltage (LV) signal pins, the applicable voltage clamping limits of JESD78, Table 2 may reduce the injected current below the set target level (e.g. +/- 100 mA). With a maximum supply voltage below about 2V, the injected current may even become zero. Do you strictly apply the Table 2 voltage limits?

82. [Q82] Please specify the above answer

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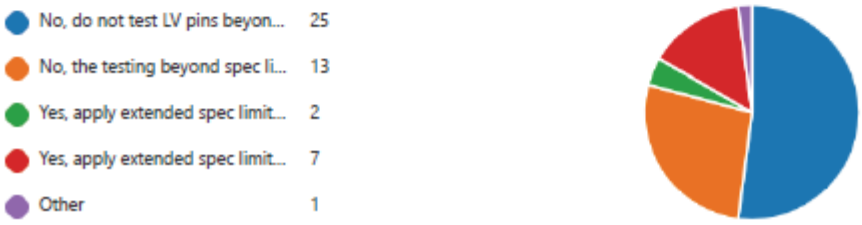
Responses

83. [Q83] If you characterize LV pins beyond the voltage limits of JESD78, Table 2, do you apply this extended test method for product qualification and document the extended spec limits in the latch-up report?

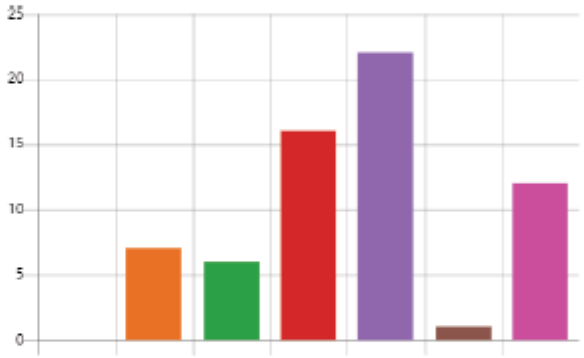


84. [Q84] Do you setup the JESD78 test program to check if the injected signal pin itself suffered from latch-up ("signal pin latch-up")?

No, only consider latch-up on ...	17
Yes, also check "signal pin latc...	35
Other	1

85. [Q85] The concept of maximum stress voltage (MSV) allows one to differentiate between latch-up and EOS (electrical overstress). The conventional pin voltage limits during JESD78 testing may be reduced to the MSV. How do you determine the MSV?

Do not use MSV	0
Dedicated MSV test procedur...	7
Adjust voltage limits during JE...	6
Use product absolute maximu...	16
Use technology absolute maxi...	22
Simulations	1
Other	12



86. [Q86] For determining the MSV, do you confirm that the damage is from a stress mechanism not directly related to latch-up (as required by the JESD78 standard)?

No	13
Yes, with physical failure analy...	32
Yes, by other means (please s...	11

87. [Q87] In case of 'other means', please specify the above answer

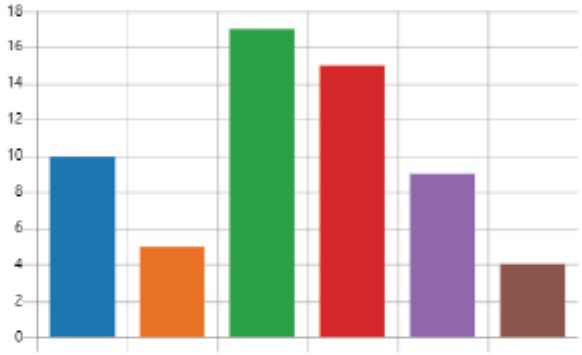
12
Responses

88. [Q88] Which (irreversible) damage conditions do you find acceptable for invoking the MSV?

Interconnect (metal, bonding, ...	19
P-N junction breakdown	34
Gate oxide rupture	30
Bipolar snapback	23
Other	11

89. [Q89] How often do you encounter a product where the MSV reduces the injected current below the set target level (e.g. +/-100mA)?

Most of the time	10
Often	5
Sometimes	17
Rarely	15
Never	9
Do not use MSV	4



90. [Q90] Do you set the pin stress voltage limits so that they do not exceed the product AMR?

Yes, if damage occurs while ex...	43
No, the AMR is not applicable ...	17

91. [Q91] If latch-up occurs during the stress pulse (but not sustained), should that be considered a failure?

Yes	20
No	24
It depends (please explain)	20

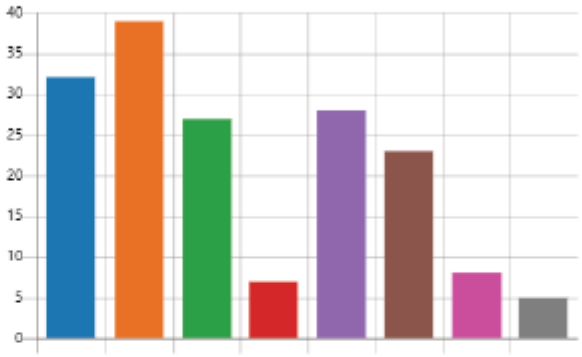
92. [Q92] Please specify 'It depends'

22

Responses

93. [Q93] What are common causes of rejecting a JESD78 pass/fail result?

Incorrect specification/request	32
Setup instability	39
Current or Voltage instability ...	27
Desired injection levels not re...	7
MSV exceeded	28
Tester instability	23
Latching not due to parasitic t...	8
Other	5



94. [Q94] Do you use functional test (ATE test) to verify device specification requirements after latch-up testing to confirm pass/fail result from tester?

Yes	61
Yes, but do not count as failure	2
No	3

95. [Q95] Feel free to enter any suggestions/recommendations

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Responses

96. [Q96] Please provide your email address to receive a copy of the final report on this survey

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Responses

Annex D (Informative) Revision History

Revision	Changes	Date of Release
	Initial Release	DECEMBER, 2022

Standard Improvement Form JEDEC JEP193

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street, Suite 240 S
Arlington, VA 22201

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC