JEDEC STANDARD

IC Latch-Up Test

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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IC LATCH-UP TEST

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Foreword

For almost three decades, characterization of the latch-up sensitivity as per JEDEC's JESD78 specification, or its predecessor JESD17, has been an industry accepted qualification test for integrated circuits (ICs) and semiconductor devices. Meeting a certain level of latch-up immunity in its application, as based on JESD78 specifications, is expected to minimize No Trouble Found (NTF) and Electrically Induced Physical Damage (EIPD) failures due to latch-up. This edition of JESD78 is essentially an entire rewrite of the earlier version, JESD78E.

Latch-up is a state in which voltage and current outside of normal conditions triggers a high current, low impedance state not related to normal functionality, which does not end without removing power from the system. Latch-up may or may not cause physical damage. JESD78 tests for latch-up sensitive structures with two test types, overvoltage on supply pins and current injection into signal pins. Current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).

As device technologies have evolved, products have become increasingly complex in design and varied in functionality. Therefore, it has become desirable to periodically revise this specification to meet the realities of device complexity and improve on the characterization methods. An example of such an adjustment is the introduction of the concept of the maximum stress voltage (MSV) in Revision D, allowing one to characterize latch-up in a way that differentiates EIPD between latch-up and non-latch-up damage. The MSV concept has been enhanced in this version with examples on determining MSV in Annex E. MSV is just one example of the modifications to this standard that will ensure successful performance of latch-up characterization.

Latch-up testing has become an increasingly complex task, often requiring experienced engineering assessment and support. Some of the problems with the previous specification arose with the increasing complexity of today's ICs. Many of today's complex devices have individual pins that cannot be characterized unambiguously as either inputs, outputs, or supply pins. Several pin types require special consideration to determine whether they require a voltage test or a current injection test. Furthermore, some pin types require unique pre-configuration or special data assessment methods to properly perform latch-up testing. Currently, JESD78E gives only minimal guidance to determine the pin category.

Discussions with industry experts have highlighted the need for major revisions and additions to JESD78E. The JESD78 working group, working on the next revision of the specification, decided that the shortcomings required a re-write of the document. This revision – JESD78F – introduces some major changes. One of these is the extension of the term "latch-up" itself. Historically, latch-up was restricted to the triggering of a parasitic thyristor structure (PNPN), but there are also other structures within an integrated circuit that can cause a similar low impedance path when triggered. Further, the effects of the low impedance path created by these other structures are indistinguishable from the effects of a triggered parasitic thyristor and, from a customer perspective, are just as detrimental to system performance. In this revision, the definition of the triggered structure is extended to an ESD protection device or any structure that, once triggered, will cause higher than normal currents to flow between power and ground, for example, bipolar transistors. Please note that current increase by a change of a functional state is still not considered as latch-up.

Foreword (cont'd)

Amongst other changes, the problem with the classification of special pins is addressed by introducing a "decision flow" which considers many special pin types such as voltage reference pins, signal pins (formerly called I/O pins) with LDO's and voltage/current sensing pins. A revised Annex A adds decision diagrams and examples to aid with set-up of these types of pins.

JESD78F defines pre-conditioning of the device-under-test (DUT), the latch-up stress pulse, the detection of latch-up, and the failure criteria. JESD78 defines two different types of latch-up stresses, an overvoltage test applied to supply pins (in this document referred to as Supply Test) and a current injection test applied to signal pins (Signal Pin Test). The Signal Pin Test can be performed either as a test with a current stress pulse (in JESD78E and prior revisions as I-Test) or with a voltage stress pulse (known as E-Test in AEC-Q100-004-Rev-D). The possibility of using an E-Test instead of an I-Test for the current injection to a signal pad is new in this revision, although, in reality, the originally defined I-Test was often performed as an E-Test. Current injection in the Signal Pin Test is achieved either by forcing current with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test). As the current injection test to signal pins can be performed as I-Test or E-Test, the terminology of this current injection test was changed to Signal Pin Test.

This revision does not cover transient-induced latch-up (also known as "Transient Latch-up, TLU") which is covered in ANSI/SP5.4.1-2017. Although the characterization method is in many ways similar, the purpose of JESD78 is to serve as a qualification standard, while transient-induced latch-up is currently a pure characterization methodology of some specific exposed or endangered pins with no specified immunity levels. To distinguish between TLU and "static" JESD78 latch-up, the rise time of the overstress causing latch-up in this document shall be longer than one microsecond.

Significant effort has been put into the ease of use of the document. The document has been re-organized, and the definitions clause (Clause 2) has been extended to describe the new terms and symbols. There have been significant upgrades to existing Annexes and new Annexes added to the document to aid in an improved understanding of the methods that enhance the effectiveness of the stress testing.

JESD78 should be considered as a living document. The JESD78 Working Group hopes that this current revision – JESD78F – will enable smooth latch-up characterization for several years, but further changes, driven by technologies and applications, are already on the horizon.

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IC LATCH-UP TEST

(From JEDEC Board Ballot JCB-22-51, formulated under the cognizance of JC-14.1 Committee on Reliability Test Methods for Packaged Devices.)

1 Scope, Purpose and Limitations

1.1 Scope

This standard establishes the procedure for testing, evaluation and classification of devices and microcircuits according to their susceptibility (sensitivity) to damage or degradation by exposure to a defined latch-up stress. This standard covers a current-injection test (Signal Pin Test) and an overvoltage test (Supply Test). Current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).

All packaged semiconductor devices, thin film circuits, surface acoustic wave (SAW) devices, optoelectronic devices, hybrid integrated circuits (HICs), and multi-chip modules (MCMs) containing any of these devices are to be evaluated according to this standard. This test method is applicable to NMOS, CMOS, bipolar, and all variations and combinations of these technologies including some Silicon-On-Insulator (SOI).

1.2 Purpose

The purpose (objective) of this standard is to establish a test method that will replicate latch-up failures during device operation and provide reliable, repeatable latch-up test results from tester to tester, regardless of device type. Repeatable data will allow accurate classifications and comparisons of latch-up sensitivity levels. The document will also provide guidelines to allow the user to apply engineering judgement when historical testing methods are not compatible with the integrated circuit's functionality.

1.3 Limitations

This standard will only consider direct current injection into and out of a signal pin (formerly called I/O pin), and overvoltage on the power supply pins. Transient induced latch-up will not be addressed. A transient-induced latch-up characterization methodology is defined in the ANSI/ESD Standard Practice SP5.4.1-2017 "Latch-up Sensitivity Testing of CMOS/BiCMOS Integrated Circuits – Transient Latch-up Testing, Device Level".

Latch-up failures will be limited to the detection of a sustained low-impedance path resulting from an applied trigger condition. Other types of potential functional failures, including logic state changes and spurious resets, are not considered by this standard, and are not considered latch-up failures.

2 Terms and Definitions

The following terms and definitions apply to this test method.

cool-down time: The period of time after the post pulse measurement and before the next application of stress.

DUT: The device under test.

dynamic pin: A pin or set of pins that experience a varying voltage or current during stress to other pins, for example, clock pins, crystal pins, etc.

NOTE A dynamic device has dynamic pin(s).

E-Test: A Signal Pin Test method using positive and/or negative voltage trigger pulses with a current compliance, as an alternative to I-Test, to evaluate latch-up sensitivity of an input or an output of a device.

EIPD (Electrically **I**nduced **P**hysical **D**amage**):** Damage to an integrated circuit due to electrical/thermal stress beyond the level which the materials could sustain. This would include melting of silicon, fusing of metal interconnects, thermal damage to package material, fusing of bond wires and other damage caused by excess current or voltage. (Ref: JEP174)

Ground: The common or zero-potential pin(s) of the DUT.

NOTE 1 Ground pins are not latch-up tested.

NOTE 2 A ground pin is sometimes called VSS. However, in some cases there can be multiple V_{SS} pins, in which case these V_{SS} pins may be referenced to a common ground.

I_{limit}: The value of the current limit for the power supplies and pulse sources for both the Signal Pin Test and Supply Test.

NOTE The I_{limit} is sometimes referred to as the current compliance on a power supply.

input pins: A subgroup of signal pins that is designed or can be configured to receive an external signal during latch-up testing. Examples of DUT pins that are typically defined as input pins for latch-up testing are address, data-in, control, clock, or similar pins.

NOTE 1 An input pin gets tied to a specific logic-low voltage level (V_{minOP}) or a specific logic-high voltage level (V_{maxOP}) during latch-up testing.

NOTE 2 Input pins are typically in a high-impedance state. There may be exceptions, for example, high-speed input pins with on-chip impedance matching/termination or input pins that have a weak-pull function enabled.

2 Terms and Definitions (cont'd)

NOTE 3 Pins defined in a datasheet as bi-directional (I/O) pins would also be defined as input pins for latch-up testing if they can be configured to receive an input signal.

NOTE 4 This definition reflects the usage within this latch-up test specification. Datasheets may use a different definition of input pins focusing on actual system applications (see clause 5.4.1).

I_{supply}: The total supply current in each V_{supply} pin (or pin group) with the DUT biased.

I-Test: A Signal Pin Test method using positive and/or negative current trigger pulses with a voltage compliance, as an alternative to E-Test, to evaluate latch-up sensitivity of an input or an output of a device.

latch-up: A Sustained High-Current Event within an integrated circuit caused by the triggering of any structure resulting in a sustained low impedance path that persists even after the removal of the triggering condition.

NOTE 1 Examples of structures causing latch-up include thyristors (PNPN), BJTs (PNP or NPN) and similar structures that are either of a parasitic nature or part of the electrical protection structures. Other structures causing latch-up include active ESD clamp circuits that remain in a triggered condition. Most changes in a functional state related to normal chip operation (for example switching of power modes due to the triggering condition) are not considered latch-up.

NOTE 2 The classical definition of latch-up explicitly refers to a parasitic thyristor (PNPN), whereas this specification document uses a more generic definition to include other latching structures that can be identified by the described test method.

NOTE 3 Latch-up typically occurs between power and ground, but could also involve signal pins as described in Annex H.

NOTE 4 The applied triggering condition can be a voltage or current impulse, an excessive rate of change of current or voltage, or any other abnormal condition that causes latch-up.

latch-up immunity: The ability of an integrated circuit to resist any impulses of current or voltage that might create a latch-up condition.

logic-high: A valid voltage level within the more positive (less negative) of the two ranges of logic levels chosen representing the logic states during setting high and low levels.

logic-low: A valid voltage level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states during setting high and low levels.

maximum stress voltage (MSV): The maximum voltage (duration dependent) allowed to be placed on a given pin during latch-up immunity testing without causing irreversible damage to the device from a permanent physical breakdown of the silicon device or circuit not caused by latch-up.

2 Terms and Definitions (cont'd)

NOTE 1 A positive MSV is higher than the maximum operating voltage and a negative MSV is lower than the minimum operating voltage.

NOTE 2 MSV is NOT the same as the absolute maximum voltage rating (AMR) from the device datasheet. MSV applies to latch-up testing only, protecting the DUT from physical damage from stress mechanisms not directly related to latch-up. An example of an unrelated stress is one exceeding the destructive breakdown voltage of a pin resulting in non-latch-up induced catastrophic breakdown of the silicon device/circuit.

NOTE 3 MSV may be different for each pin and each polarity during testing, depending on process technology and circuit topology. In many medium and high voltage designs, MSV is very rarely the same value as AMR.

NOTE 4 The MSV value depends on the pulse width used during latch-up testing. Shorter pulse widths may allow a higher value for MSV. Therefore, the MSV value chosen should consider the pulse width as well as process technology and circuit topology.

"no connect" pin: A pin that has no internal electrical connection to the die.

NOTE All "no connect" pins are to be left in an open (floating) state and should not be stressed during latch-up testing.

nominal I_{supply} (I_{nom}): The measured dc supply current for each V_{supply} pin (or pin group) with the DUT biased at the maximum operating conditions.

output pins: A subgroup of signal pins that are not configured to receive an external signal during latch-up testing because they drive out a signal or a voltage level.

NOTE 1 Output pins, though left in an open (floating) state during testing of other pin types, should be latch-up tested.

NOTE 2 Output pins are typically in a low-impedance state.

NOTE 3 This definition reflects the usage within this latch-up test specification. Datasheets may use a different definition of output pins focusing on actual system applications (see clause 5.4.1.)

power supply: A component in the test system that supplies voltage and current to the DUT.

preconditioned pin: A device pin that has been placed in a defined state or condition by applying static or dynamic control signals to the DUT or biasing the appropriate steady state control pin(s) in order to put the device into a known, controlled and stable state.

preconditioning vectors: a series of commands sent to an integrated circuit instructing the circuit to perform a specified series of functions or place it into a known state.

2 Terms and Definitions (cont'd)

pre-stress & post-stress current (I_{psPRE} & I_{psPOST}): The pulse supply current corresponding to the Signal Pin Test or Supply Test before (pre-stress) & after (post-stress) pulse application.

NOTE 1 I_{psPRE} & I_{psPOST} can either be a forced value or the limit value depending on the mode of the source (I-Test or E-Test).

NOTE 2 It is also known as parking current in some commercial systems.

pre-stress & post-stress voltage (V_{psPRE} & V_{psPOST}): The pulse supply voltage corresponding to the Signal Pin Test or Supply Test before (pre-stress) & after (post-stress) pulse application. It is not dependent on polarity.

NOTE 1 V_{psPRE} & V_{psPOST} can either be a forced value or the limit value depending on the mode of the source (I-Test or E-Test).

NOTE 2 V_{psPRE} & V_{psPOST} are typically either V_{maxOP} or V_{minOP} for these systems.

NOTE 3 It is also known as parking voltage in some commercial systems.

PUT: Pin Under Test

signal pins: Device pins that carry an electrical signal (information) during stable operation of the device and are not used as supply pins.

Signal Pin Test: A test that injects positive and negative current pulses to the pin under test (PUT) by either injecting a current pulse (I-Test) with a voltage limit or injecting a voltage pulse (E-Test) with a current limit.

steady state control pins: Pins used to place the DUT in the desired configuration (IO configuration pins, reset, power good/OK, enable, other control pins) whose logic or bias state remains constant for the duration of the test. (See Clause 5.4.1)

NOTE Steady state control pins, though remaining in a constant state, may still be latch-up tested with a stress pulse polarity that does not alter their logic state.

Supply Test (previously V_{supply} overvoltage test): A latch-up test that supplies overvoltage pulses to the supply pin (or pin group) under test.

temperature, maximum operating junction (T_{jmax}): The maximum junction temperature of a device to operate within its specifications, as listed in its data sheet and to avoid damage (latent or otherwise). It is frequently specified by device manufacturers for a specific device and/or technology.

2 Terms and Definitions (cont'd)

temperature, junction (T_j): The temperature of a semiconductor junction in a device.

temperature, ambient (T_a): The local air temperature surrounding the device, in an environment controlled only by natural air convection and not materially affected by reflective and radiant surfaces.

temperature, case (T_C): The temperature measured or calculated on the case surface of a device. (As per JESD88F)

NOTE See Clause 3.2 and/or Annex B for further information on measuring/calculating case temperature using ambient or junction.

timing-related input pin: A pin such as clock crystal oscillator, charge pump circuit, etc., required to place the DUT in a stable operating mode. Required timing signals may be applied by the latch-up tester, external equipment, and/or external components as appropriate.

test condition: The test temperature, supply voltage, current limits, voltage limits, clock frequency, input bias voltages and preconditioning vectors applied to the DUT during the latch-up test.

trigger duration: The duration of an applied pulse from the trigger source**.**

trigger pulse: The positive or negative current pulse (Signal Pin Test) or voltage pulse (Supply Test or E-Test) applied to any pin under test for latch-up sensitivity.

tri-state (also known as three-state): Cells or macros whose outputs can be placed in a high-impedance state and can also generate low-impedance V_{maxOP} and V_{minOP} levels. (Ref JESD12-4, 4/87)

V_{limit}: The value of voltage used to limit the actual voltage, and thereby restricts the forced current into and out of a signal pin during latch-up stress.

V_{maxOP}: The maximum operating bias voltage of the PUT given in the device datasheet.

V_{maxSUP}: It is the maximum supply voltage at which a supply is specified to operate in conformance with the applicable device specification; formerly maximum V_{supply} in previous revisions.

V_{minOP}: The minimum operating bias voltage of the PUT given in the device datasheet.

V_{supply} pin (or pin group): A supply pin is any pin that provides current to a circuit. Supply pins typically transmit no information (such as digital or analog signals, timing, clock signals, and voltage or current reference levels). Supply pins are often referred to as power pins.

2 Terms and Definitions (cont'd)

NOTE 1 It is generally permissible to treat supply pins with the same or similar voltage as one V_{supply} pin (or pin group) and connect them to one power supply.

NOTE 2 When combining V_{supply} pins (or pin groups) with the same or similar voltage, combining V_{supply} pins with significantly different supply current levels is not recommended as this would make it difficult to detect significant current changes on low supply current pins.

3 Latch-Up Characterization

A component's susceptibility to a latch-up event is characterized by its response to a stress when either current is injected into a signal pin or when a supply overvoltage occurs operating within the temperature range of the component's specified operating junction temperature. This clause describes the Immunity Levels (A and B) and the temperature classification (II and I) for latch-up characterization.

3.1 Latch-Up Immunity

Product latch-up immunity is characterized by the forced current or voltage value at the signal pin and overvoltage value on the supplies that does not result in latch-up as defined in this test standard. Table 1 defines Immunity Levels A and B at specified ranges for injected current and applied voltage stress levels.

Table 1 --- Latch-Up Immunity Levels

<table>
<tr><th>Immunity Level</th><th>Test</th><th>Absolute Magnitude of Injected Trigger Current
or
Absolute Magnitude of Applied Trigger Voltage</th></tr>
<tr><td rowspan="3">A</td><td>Positive Signal Pin Test (1)</td><td rowspan="2">≥ 100 mA
The actual injected current may be less than 100 mA, if pin voltage preset limits are reached</td></tr>
<tr><td>Negative Signal Pin Test (1)</td></tr>
<tr><td>Supply Test</td><td>1.5 × V_{maxSUP} or MSV, whichever is less
The actual applied voltage may be less than 1.5 × V_{maxSUP} or MSV, if supply current limits are reached</td></tr>
<tr><td>B</td><td colspan="2">If Immunity Level A cannot be achieved</td></tr>
<tr><td colspan="3">(1) In the Signal Pin Test, current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).</td></tr>
</table>

3.1 Latch-Up Immunity (cont'd)

The actual current injected into the signal pin during the Signal Pin Test may be limited by the signal pin design or due to the test methods described in Table 2 for the preset conditions that limit the signal pin voltage during the current injection. Likewise, the actual applied voltage during the Supply Test may be limited by the preset current limit into the supply. If latch-up does not occur in such a condition, then this constitutes a passing test with Immunity Level A. Otherwise, it is classified with Immunity Level B.

3.2 Temperature Classification

Since the likelihood for a latch-up occurrence increases with temperature, latch-up testing shall be performed at a junction temperature (T_j) equivalent to its maximum operating junction temperature (T_{jmax}).

The two latch-up temperature classifications for latch-up testing are:

- Class II – For latch-up testing at T_{jmax}, or the T_{amax}/T_{cmax} equivalent of T_{jmax}. Class I testing is not required if Class II testing achieves Immunity Level A (Table 1).

- Class I – For latch-up stress testing at junction temperatures below Class II. If the passing temperature is below T_{jmax}, the maximum passing temperature shall be reported.

NOTE See Annex B for further information on T_{amax}, T_{cmax} and T_{jmax}.

3.3 Overall Requirements

The requirements to classify latch-up susceptibility are the following:

- Class II.A: Meets Level A latch-up immunity requirements at T_{jmax}
- Class I.A: Meets Level A latch-up immunity requirements at temperatures lower than T_{jmax}
- Class II.B: Meets Level B immunity latch-up requirements at T_{jmax}
- Class I.B: Meets Level B immunity latch-up requirements at temperatures lower than T_{jmax}

NOTE Class II.A in this document is a Revision E Class II enhancement.

4 Apparatus and Material

The apparatus required for this test method includes the following:

4.1 Latch-Up Tester

4.1.1 Hardware Requirements and Capabilities

Test equipment capable of performing the tests as specified in this document consist of the following:

- Bias power supplies having the ability of providing the required voltage and current, plus the ability to monitor the voltage and current being drawn by the DUT. The response time of the supply should also be considered, as to avoid incorrect measurements during transient events.
    - Bias power supplies should also have the capability to drive input pins to their V_{maxOP} or V_{minOP} when not being stressed.
- The stress power supply shall have the ability to force and measure both current and voltage before, during and after stressing of the DUT. The supply shall have the ability to set compliance limits, with adequate response time to avoid over stressing of the DUT. It shall be capable of meeting the timing requirements in Table 5. See Annex F for further discussion on pulse source verification and for possible supply sensitivities that can occur during stressing.
- For devices requiring dynamic testing, the test equipment shall be capable of supplying timing signals. The required timing signals may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate.
- For devices requiring setup vectors to place the device into a state suitable for latch-up testing the test equipment shall be capable of supplying the required vectors. The required timing signals and logic vectors may be applied by the latch-up tester itself, external equipment, and/or external components as appropriate as specified in 5.4.3.

4.1.2 Test Board

Test board options will depend on the test system capabilities and hardware configurations. The common options are listed below.

- Many commercial systems will use generic test boards for both ESD and latch-up testing. Reusability for both ESD and latch-up testing is possible by having only a single board trace from the test system channel pin to the socket pin. The board shall not have any other components that limit the ability to perform latch-up on any pin. Supply and signal pins can be assigned to any tester channel pin. This adds flexibility during debug and failure analysis by having the ability to reassign supply pins to determine the failing supply.

NOTE Some devices may need a latch-up specific board, where high supply current capability is needed on a limited number of V_{supply} pin groups which may be connected via an inner plane

4.1.2 Test Board (cont'd)

- Use of passive or active elements:
  - Series passive or active elements that may limit the magnitude of the injected pulse are strongly discouraged (see Annex A for additional guidance).
  - Parallel passive or active elements used to support control pin regulation or add to the DUT stability are allowed if required for stable device operation. The use of inductors is strongly discouraged (see Annex A for additional guidance).
  - Any use of these elements shall be recorded as part of the latch-up data as described in Annex D.
- Boards for ATE testing or similar device test board for functional and parametric testing can be used for latch-up testing. These boards may have components, such as capacitors and resistors for device stability; thus, the supply pins and signal pins are not easily reassigned. These boards may emulate actual end user system boards.

For all board types, the trace cross-sectional areas should be sufficient to carry expected current levels without excessive IR drops during latch-up testing. During latch-up testing, currents will exceed nominal levels both on supply pins and signal pins.

4.1.3 Temperature Control

Equipment capable of heating (or in some cases cooling) a device to maintain the DUT at the maximum operating junction temperature (T_{jmax}) as specified by the device specification during the latch-up test is required. Refer to Annex B for further details on controlling temperature.

5 Latch-Up Test Procedure

5.1 General Latch-Up Test Overview

This clause describes the standard procedures to stress a component to trigger and detect a latch-up event. Its ability to resist latch-up will determine the device's Immunity Level as described in Table 1.

Two stress methods, called the Signal Pin Test and Supply Test, are used to trigger a possible latch-up event.

- For the Signal Pin Test, current flows into a signal pin by either injecting current while limiting the signal pin voltage, or by applying a voltage with the current limited to the minimum required current level, such as 100 mA for Immunity Level A (see Table 1).

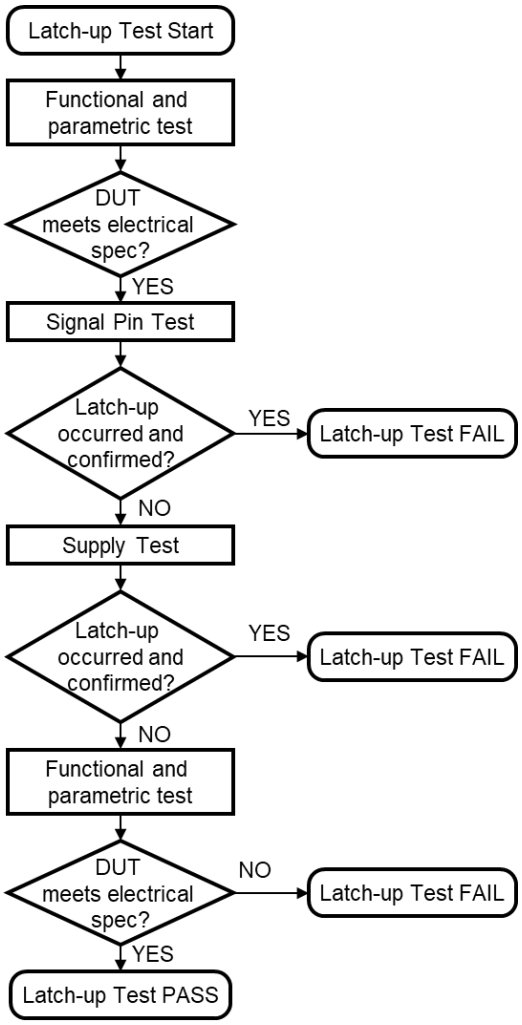
- The Supply Test attempts to trigger latch-up by an overvoltage of the supply at stress levels described in Table 1.

Signal Pin and Supply latch-up tests are required to be performed to meet the Immunity Levels requirements.

5.1 General Latch-Up Test Overview (cont'd)

Figure 1 shows the general latch-up test flow for the Signal Pin Test and Supply Tests. Prior to stressing, complete static and dynamic testing shall be performed on all submitted devices with adequate test coverage to be able to detect any latch-up induced degradation. Parametric and functional results shall be within the limits specified in the datasheet.

NOTE Some failures may only be found when static and dynamic testing is completed at the datasheet high temperature limits.



NOTE The order of the Signal Pin Test and the Supply Test is arbitrary.

Figure 1 — General Latch-Up Test Flow for the Signal Pin Test and Supply Tests.

After latch-up stress the device will be retested to determine if the device continues to meet specification or if any possible damage has occurred.

5.1 General Latch-Up Test Overview (cont'd)

All input and output pins shall be tested with the Signal Pin Test as described in more detail in Clause 5.6 using the limits in Table 2, unless these pins fall into specific cases, listed in Clause 5.4.1. Pins stressed with the Signal Pin Test will be stressed at positive and negative polarities of the current injection, while input pins not under test are all tied to the maximum pin operational voltage V_{maxOP} or all tied to minimum pin operational voltage V_{minOP} (see Table 2), followed by testing with the pins in the opposite states unless these pins fall into specific cases listed in Clause 5.4.1.

The Signal Pin Test can be accomplished by using either a forced pulsed current with voltage limiting (I-Test) or an applied pulsed voltage with limiting current (E-Test). Historically, I-Test has been the stress used most often for latch-up stress testing. E-Test provides an option to Signal Pin stress with forced pulsed voltage. Signal Pin response to the type of pulse may dictate which stress test is appropriate. I-Test and E-Test are considered to be equivalent stress tests as long as the forcing and limiting values are set properly. See Annex G for additional information.

All supply pins shall be tested with the Supply Test, as described in more detail in Clause 5.7 and using the limits in Table 7. Input pins not under test are all at V_{maxOP} or all at V_{minOP} (see Table 2), followed by testing with the pins in the opposite states unless these pins fall into specific cases listed in Clause 5.4.1.

In the latch-up test, all devices shall pass the latch-up criteria specified in Table 3. A failure of any of the devices tested during the Signal Pin Test or Supply Test, or if any of the devices do not meet the electrical specification after stress, constitutes a latch-up failure.

Table 2 — Overview of Latch-Up Tests for a Complete Latch-Up Characterization

Stress Type	Stress Polarity of Trigger	Input Pins Not Under Test (1)
Signal Pin Test (I-Test OR E-Test)	Positive current injection	Maximum pin operational voltage V_{maxOP}
		Minimum pin operational voltage V_{minOP}
	Negative current injection	Maximum pin operational voltage V_{maxOP}
		Minimum pin operational voltage V_{minOP}
Supply Test	Overvoltage	Maximum operational voltage V_{maxOP}
		Minimum operational voltage V_{minOP}

(1) All pins which are not excluded according to Clause 5.4.1.

5.2 Device Handling

Devices used for latch-up testing shall not have been used for any prior stress tests. ESD damage prevention procedures shall be used before, during, and after latch-up testing and post parametric and functional testing.

NOTE See the latest revision of ANSI/ESD S20.20, JESD625, or IEC61340-5-1 for guidance.

5.3 Sample Size

A minimum of three (3) devices shall be subjected to testing using the Signal Pin Test and Supply Test. It is allowed to partition Signal Pin Test and Supply Test, or test combinations by using at least three (3) fresh devices for each partition. All partitions used shall cover all combinations of stresses originally planned for the product.

All devices to be tested shall have passed functional and parametric testing to the device specification requirements.

5.4 Preparation of the Latch-Up Test

5.4.1 Pin Types and Grouping

In preparation for testing, pin grouping and test limits are determined based on the product datasheet.

1) Identify all pins as signal, supply pins or no connects. Whether a pin is tested as a signal pin (Signal Pin Test) or as a supply pin (Supply Test), depends on the functionality and/or the configuration of the pin in the system. For special pins, Annex A gives guidance on how these pins shall be treated. Some examples of special pins are pins connected to passive components, voltage regulators, reference pins or debug pins.
   - Shorted input pins that are connected by a low resistance connection in the package or on the die or by a common bond pad shall be represented by a single pin with all other pins shorted to that pin configured as “no connect pins” to avoid contention. Alternatively, the pins may be shorted on the test board and controlled and stressed by a single supply. These methods may be applied to shorted output pins.
2) Split the group of all signal pins into groups of input pins and output pins. For the purpose of latch-up testing, all signal pins that can be placed in a high-impedance state should be defined as input pins. All pins that are in a low-impedance state (driving out a signal or voltage level) and which cannot be placed in a high-impedance state should be defined as output pins. The product datasheet may provide guidance for this pin categorization. For example, pins that are described as “Input”, “I/O”, or “Bi-Directional” in a datasheet would typically be treated as input pins for latch-up testing. Pins that are described as “Output” in a datasheet would typically be treated as output pins for latch-up testing unless they can be tri-stated, in which case the pins should be defined as input pins.

5.4.1 Pin Types and Grouping (cont'd)

3) Identify the pins that may have special consideration for testing. Some of these pins should still be tested but may need to be tested separately from the primary testing of the signal pins or may need to be preconditioned in special states. These pins typically fall into the following categories:
   - "no connect" pins are not required to be tested.
   - Timing related pins, such as a clock input or crystal oscillator pins required to maintain the device in a stable mode or for dynamic testing. If an alternate means of placing the DUT in stable operating mode can be achieved, then the full Signal Pin Test can be accomplished on the timing related pins.
   - Steady state control pins used to precondition the device in the desired configuration, such as signal pin configuration pins, reset, and power enable, or other control pins, may require special testing. Steady state control pins may be subject to reduced testing with the current stress polarity that does not disrupt the DUT, such as a reset pin that shall be kept in one logic state.

4) For all input and output pins determine the V_{maxOP} and V_{minOP}. Input and output pins with common operating voltages may be grouped as single pin groups for testing. When possible, separating grouped signal pins on a tester supply not used as a device power supply is advised for easier determination of possible failures. V_{maxOP} and V_{minOP} shall be used for the logic-high and logic-low for input pins, and also used to calculate the maximum voltage (compliance limit) for the Signal Pin Test for these pins.

5) All supply pins with the same supply voltage may be grouped into a single supply group. Determine the maximum supply current for each device supply, V_{maxSUP}. See Clause 5.4.2 below.

NOTE: In most test systems, there are insufficient power supplies to provide power individually to each supply pin (group). Grouping of supply pins (groups) allows for efficient use of the power supplies available. More details are given in 5.4.2.

5.4.2 Power Supply Assignments

Some devices may have several power rails that exceed the number of available power supplies in the latch-up test system, therefore, grouping of the supplies will be necessary. In this case, planning of the supply assignment should be optimized to improve the detectability of a latch-up occurrence when several supply groups are assigned to a single power supply on the tester. Therefore, it is recommended to group the device supply pins and assign the power supplies so that device supply rails with small currents are not combined with those with large currents, to avoid masking of a latch-up occurrence on the small current supply rail.

Latch-up testing requires the input pins to be tied to the maximum pin operational voltage (V_{maxOP}) or tied to the minimum pin operational voltage (V_{minOP}), see Table 2. V_{minOP} is typically tied to ground but may be a value other than 0 V if the test system is capable. There are two suggested methods to assign the supply for the bias on the signal pin to V_{maxOP} or V_{minOP}.

1) For optimal latch-up detection, assign a separate supply for the signal pins to bias for V_{maxOP} or V_{minOP}. The advantage is that any latch-up of the signal pin itself (see Annex H) or a state change may be more easily detected.

5.4.2 Power Supply Assignments (cont'd)

2) If V_{maxOP} and V_{maxSUP} are the same, the same power supply may be used for the pin groups.

NOTE If there is a sufficient number of power supplies, it is recommended to use separate supplies for the supply pin power and for the supply to tie the signal pins to V_{maxOP}.

NOTE If the number of power supplies are limited, making it necessary to use the same power supply for V_{maxOP} on the inputs and provide power to the DUT, ensure that the MSV for the signal pins is not exceeded when performing the Supply Test stress. Otherwise, reconfigure the supplies to avoid exceeding the MSV on these input pins to avoid overstress.

5.4.3 Product Pre-Conditioning

To avoid masking a latch-up occurrence, the device shall be in a low power-consuming state or a stable operating mode for latch-up testing. Output pins capable of being put into tri-state should be tested with both positive and negative pulses.

All voltage rails, including internal power supplies, shall be powered up at V_{maxSUP} and all functional blocks shall be supplied.

Typically, either a static signal, a dynamic and/or vector pattern is required to pre-condition the DUT in a stable test mode. Often the static signal, a dynamic and/or vector pattern should be re-run after each latch-up stress to ensure that the initial state of the DUT is well defined.

5.4.4 Device Temperature Set-Up

Proper temperature control for latch-up testing is critical to accurately test a product. Product datasheets typically specify Tjmax. Since Tj can vary spatially across the die in operation, using the datasheet Tjmax for latch-up testing ensures that any latch-up sensitivities are evaluated at the maximum field operating temperature.

If Tjmax is not listed in the product datasheet, it can be calculated from other datasheet temperature specifications such as maximum case temperature (T_c) or ambient operating temperature (T_a) using field thermal resistance coefficients. Annex B provides equations for calculating Tj, T_a and T_c based on dissipated power and thermal resistances (θ).

5.5 Latch-Up Detection Criteria

5.5.1 Latch-Up Detection

A device is considered to have experienced latch-up if it meets the latch-up detection criteria in Table 3 or it is not within the device datasheet specification after both latch-up and ATE testing (Clause 5.8).

5.5.1 Latch-Up Detection (cont'd)

Table 3 — Latch-Up Detection Criteria

Stress Type	Trigger Stress	Latch-Up Detection Criteria
Signal Pin Test(1) (I-Test OR **E-Test)**	Positive current injection	If $\|I_{nom\_pre}\| \leq 25$ mA: LU occurs if $\|I_{nom\_post}\| > \|I_{nom\_pre}\| + 10$ mA(2) or If $\|I_{nom\_pre}\| > 25$ mA: LU occurs if $\|I_{nom\_post}\| > 1.4 \times \|I_{nom\_pre}\|$(2)
	Negative current injection	
Supply Test	Overvoltage	

(1) In the Signal Pin Test, current injection is achieved either by current forcing with voltage compliance limit (I-Test) or by applying voltage with current compliance limit (E-Test).

(2) During I-Test, E-Test or Supply Test, the supply currents for all supply groups are monitored before and after the stress pulse. Comparison of I_{nom_post} to I_{nom_pre} and the criteria above determine if latch-up occurs.

5.5.2 Power Supply Current Limits

Latch-up test equipment power supplies, used for supply pins or for biasing signal pins, generally have current limits (I_{limit}) assigned for device and test fixture protection considerations. When a supply current or signal pin biasing current reaches these power supply limits, the test result may be invalid.

A latch-up event that reaches the I_{limit} could collapse the power supply below the latch-up holding voltage and terminate latch-up before the automated test equipment detects it as a latch-up failure. The stability of the voltage levels of all the tester supplies that measure currents should be monitored during latch-up testing to ensure that the currents are kept below the assigned I_{limit}. This includes tester power supplies used for biasing signal pins at V_{maxOP} or V_{minOP} or for preconditioning of signal pins, for instance.

Unlike bias power supplies used to precondition signal pins during the test, pin drivers (vectors) used to precondition signal pins may not have current measuring capabilities, as they are intended to drive signal pins with a specified pattern. Other stress methods may need to be used to verify latch-up has not occurred on these pins. Use of unmonitored supplies is not recommended and should be limited to devices requiring set-up vectors.

General test procedures and recommendations:

- All monitored tester supply voltages shall remain within their specified range, including the time before, after, and while the current trigger is applied. If a tester supply, including vector supplies cannot be monitored, it shall be reported (see Clause 6).

5.5.2 Power Supply Current Limits (cont'd)

- It is recommended that for each V_{supply} pin (or pin group), the I_{limit} is initially set to at least:
  - I_{nom} plus 2 times the injection current, or
  - 1.4 times I_{nom}, whichever is higher.
- If the voltage of any V_{supply} collapses or reaches its I_{limit} prior to the trigger source being applied and/or while the trigger source is applied to any pin, the Signal Pin Test and/or Supply Test becomes invalid; review of the latch-up test set-up may be required and/or the stress needs to be repeated with a higher I_{limit} setting.

It is permissible to provide any Signal Pin Test and/or Supply Test characterization results obtained with lower I_{limit} settings in the latch-up report. These characterization results can be provided in addition to the required absolute Signal Pin Test and/or Supply Test passing levels with stable tester supplies (see examples in Annex D). Reported entries should include the specific I_{limit} settings used and the corresponding collapsing power supplies during the current trigger. The additional characterization data may appropriately reflect latch-up robustness in system applications exhibiting supply current limitations, similar to these lower I_{limit} settings.

Every product pin tested shall be classified as either a Pass, a Fail or Invalid.

5.6 Signal Pin Test

5.6.1 Signal Pin Test Flow

All signal pins on the package are tested with the Signal Pin Test, with possible exceptions, listed in Clause 5.4.1 or the pin is non-standard requiring an unusual configuration and it may meet the criteria in Annex A.

The Signal Pin Test shall be performed according to the testing matrix summarized in Table 2. Each signal pin will be stressed with both a positive and a negative current injection, with inputs tied to maximum pin operational voltage V_{maxOP} and repeated with inputs tied to minimum pin operational voltage V_{minOP}, in total four combinations. There may be exceptions for pins that cannot be in one of the conditions based on being a preconditioning pin such as control and reset pins, clock pin, crystal pins, etc. Latch-up testing will be performed with the waveforms and timing diagrams specified in Clause 5.6.2 (positive current injection) and Clause 5.6.3 (negative current injection).

The Signal Pin Test can be accomplished by using either a forced pulsed current with voltage limiting (I-Test) or a forced pulsed voltage with current limiting (E-Test). Historically, I-Test has been the stress used most often for latch-up stress testing. E-Test provides an option to stress with forced pulsed voltage. Signal pin response to the type of pulse may dictate which stress test is appropriate. I-Test and E-Test are considered to be equivalent stress tests as long as the forcing and limiting values are set properly.

5.6.1 Signal Pin Test Flow (cont'd)

One suggested Signal Pin Test procedure is given below. It covers all the conditions in the test matrix in Table 2. The testing order of the stress conditions may vary as long as all conditions are met in the test matrix table. The procedure below describes one possible sequence:

1) Positive current injection with non-stressed input pins tied to minimum pin operational voltage V_{minOP}
2) Positive current injection with non-stressed input pins tied to maximum pin operational voltage V_{maxOP}
3) Negative current injection with non-stressed input pins tied to minimum pin operational voltage V_{minOP}
4) Negative current injection with non-stressed input pins tied to maximum pin operational voltage V_{maxOP}

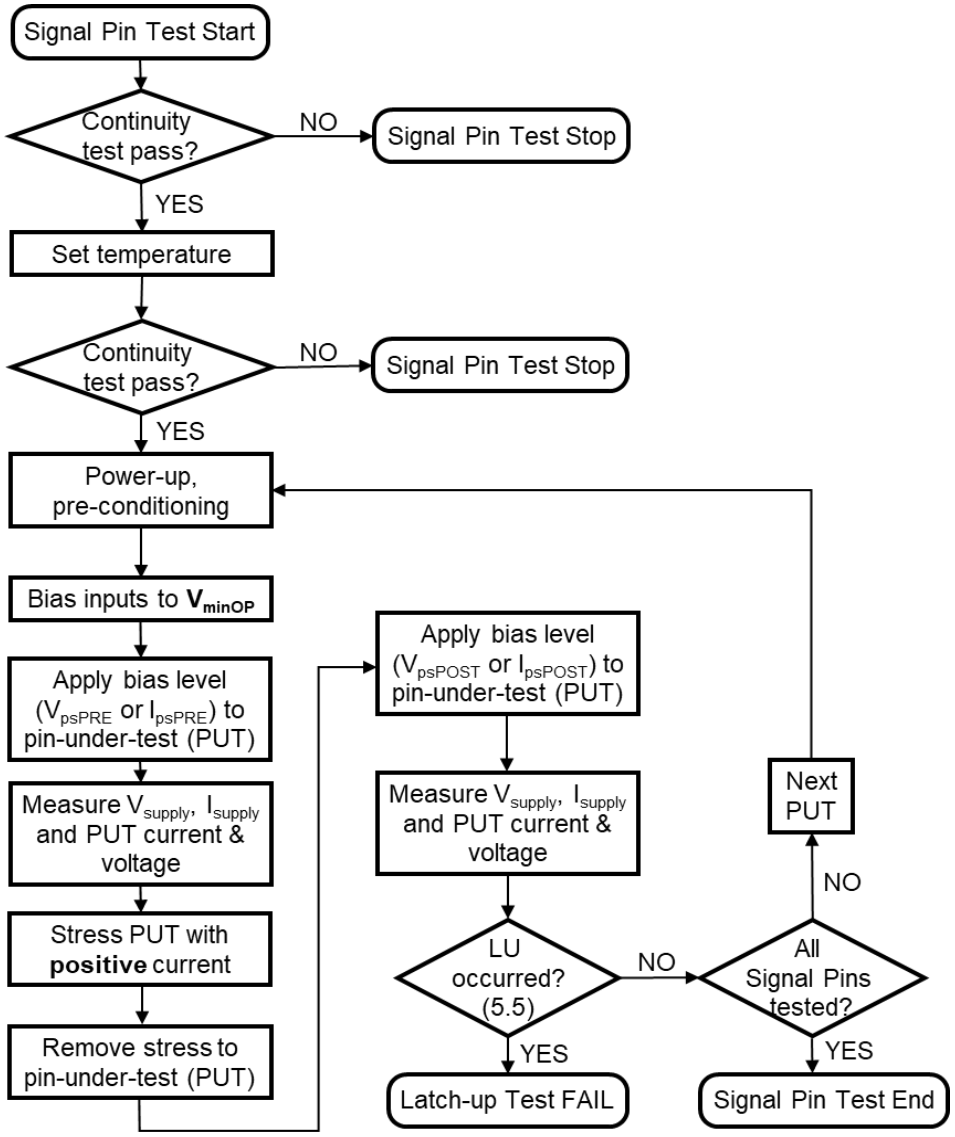


Figure 2 — Signal Pin Test Flow Example: Positive Current Stress with Input Pins Biased to Low (V_{minOP}). Also Applicable to V_{maxOP}.

5.6.1 Signal Pin Test Flow (cont'd)

Step:

1) Insert a device that has met electrical specification in the test socket. Ensure that the desired temperature at the DUT has been reached and has stabilized. Check the DUT continuity to ensure that each pin makes good electrical contact. If the DUT continuity fails, re-seat the DUT in the socket until good contact is achieved.
2) Power up the device per power-up sequence specification.
3) Precondition the device according to Clause 5.4.3.
4) Bias the DUT. All inputs pins that are not used for preconditioning are tied to V_{maxOP} if possible, and output pins should remain floating unless being stressed. See Annex H for additional guidance.

NOTE Input pins used for preconditioning, such as control and reset pins, shall be tested in their defined state. That is, pins that are tied to V_{maxOP} to precondition the DUT can only be tested with V_{maxOP}, and pins that are tied to V_{minOP} to precondition the DUT can only be tested with V_{minOP}.

5) For positive current injection into the PUT, apply a pre-stress voltage (V_{psPRE}) equivalent to V_{maxOP} to the PUT.
6) Measure nominal I_{supply} at V_{maxSUP} for each V_{supply} pin (or pin group).
7) After the wait period, force a positive current trigger into the PUT as specified in Clause 5.6.2. Measure the current and voltage of the Stress Supply and each V_{supply} during the stress period.
8) After completion of the trigger pulse, return the PUT to the level before the application of the trigger pulse (voltage equivalent to V_{maxOP}) and measure the I_{supply} at V_{maxSUP} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in Clause 5.5, latch-up has occurred and the DUT has failed latch-up testing. The power supply shall be removed from the DUT to end latch-up, further testing is stopped if latch-up has occurred.

NOTE If the device is not damaged it is permissible to restart latch-up testing to determine if there are other pins which fail the latch-up test.

9) If latch-up has not occurred, after the necessary cool-down time, continue to the next pin under test and repeat Steps 2-8 until all signal pins are tested for positive current injection.

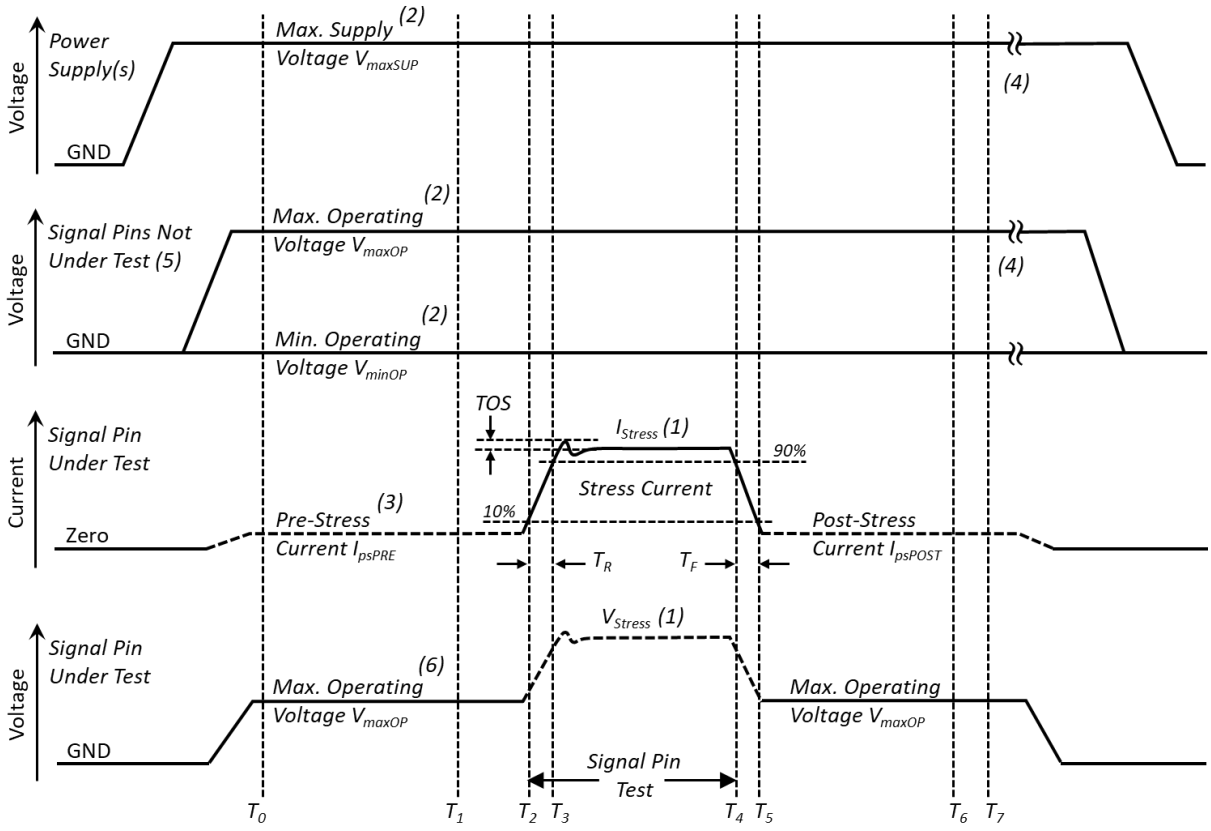
NOTE Signal Pin Tests do not necessarily require the removal of the power supplies and pre-conditioning between the stresses, so it is permitted to repeat only Steps 5–8.

10) Repeat steps 2-9 with inputs pins that are not used for preconditioning tied to V_{minOP} and outputs are floated (Step 5).
11) Repeat steps 2-10 for negative current injection into the PUT, apply a pre-stress voltage (V_{psPRE}) equivalent to V_{minOP} to the PUT (Step 6) and a negative current trigger into the PUT as specified in Clause 5.6.2.
12) It is good practice to perform continuity testing at completion of the stress.

5.6.2 Waveforms for the Positive Signal Pin Tests

Figure 3 and Figure 4 visualize the voltage and current waveforms during a positive Signal Pin Test (I-Test & E-Test), with the waveform current and voltage settings defined in Table 4. The waveform timing parameters for the positive and negative Signal Pin Tests are defined in Table 5.

5.6.2 Waveforms for the Positive Signal Pin Tests (cont'd)



(1) The waveforms when shown in a solid line are the forced voltages or currents and when shown with dashed lines are the measured voltages or currents.

(2) During I-Test the supply currents for all supply groups are monitored before and after the stress pulse. Latch-up occurs if any supply current meets the failure criteria shown in Table 3. In addition, power supply voltages shall not collapse during the stress as per Clause 5.5.2.

(3) The pre-stress and post-stress current I_{psPRE} and I_{psPOST} depend on the state and the circuitry of the PUT.

(4) At the conclusion of the stress, returning all power supplies to ground is an option to reset the DUT. Resetting supplies is recommended for stability during testing.

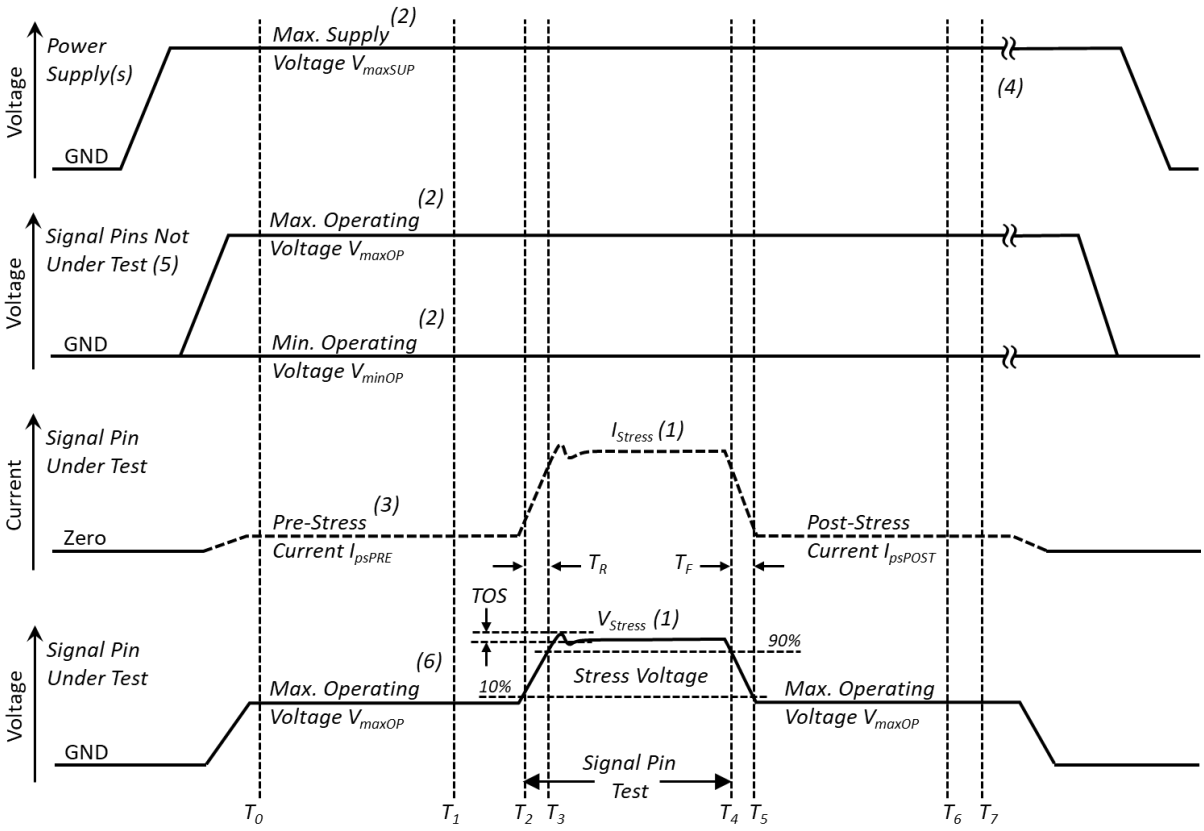
(5) Input pins Not Under Test shall be considered Signal Pins Not Under Test and should be controlled according to Step 4, Clause 5.6.1. Output pins are not included and floated when not under test.

(6) The pin under test should be set to logic high (I_{psPRE} & V_{psPRE}) before positive current trigger. It is permissible to start positive current trigger from logic low (I_{psPRE} & V_{psPRE}) but failing results should be confirmed from the logic high state. Output pins can be omitted from pre/post stress biasing if there is a risk of disturbing the latch-up operating state or risk of damage to the pin.

NOTE In this positive I-Test example, the I_{Stress} reaches the intended trigger level ("Maximum current during trigger" of Table 4), and the V_{limit} ("Maximum voltage during trigger" of Table 4) is not reached. During pre-stress and post-stress, current is being forced into the PUT but is limited at V_{maxOP}. Since the voltage is at a set value, the voltage waveforms are solid lines pre-stress and post-stress. The current is being measured; thus, the current waveforms are drawn as dashed lines. During the stress period, the voltage limit is increased and I_{Stress} reaches its intended trigger level. The current waveform is therefore a solid line during the stress period. The voltage is being measured; thus the voltage waveform is drawn as a dashed line.

Figure 3 — Test Waveform for Positive Signal Pin Test (I-Test)

5.6.2 Waveforms for the Positive Signal Pin Tests (cont'd)



(1) The waveforms when shown in a solid line are the forced voltages or currents and when shown in dashed lines are the measured voltages or currents.

(2) During E-Test the supply currents for all supply groups are monitored before and after the stress pulse. Latch-up occurs if any supply current meets the failure criteria in shown in Table 3. Also, power supply voltages shall not collapse during the stress as per Clause 5.5.2.

(3) The pre-stress and post-stress current I_{psPRE} and I_{psPOST} depend on the state and the circuitry of the PUT.

(4) At the conclusion of the stress, returning all power supplies to ground is an option to reset the DUT. Resetting supplies is recommended for stability during testing.

(5) Input pins Not Under Test shall be considered Signal Pins Not Under Test and should be controlled according to Step 4, Clause 5.6.1. Output pins are not included and floated when not under test.

(6) The pin under test should be set to logic high (I_{psPRE} & V_{psPRE}) before positive voltage trigger. It is permissible to start positive voltage trigger from logic low (I_{psPRE} & V_{psPRE}) but failing results should be confirmed from the logic high state.

NOTE: In this positive E-Test example, the I_{Stress} does not reach the intended trigger level ("Maximum current during trigger" of Table 4) because V_{stress} reaches the V_{limit} ("Maximum voltage during trigger" of Table 4). During the full waveform (including pre-stress, stress, and post-stress), the voltage is at set values, therefore the full voltage waveform is a solid line. The current is being measured; thus, the full current waveform is drawn as a dashed line.

Figure 4 — Test Waveform for Positive Signal Pin Test (E-Test)

5.6.2 Waveforms for the Positive Signal Pin Tests (cont'd)

Table 4 — Pulse Current and Voltage Requirements for the Positive Signal Pin Test

Trigger	Maximum current during trigger (1)	Maximum voltage during trigger (2)
Current pulse (I-Test) OR Voltage pulse (E-Test)	I = 100 mA (Immunity Level A from Table 1)	$V = V_{maxOP} + 0.5 \times (V_{maxOP} - V_{minOP})$ with an upper limit of $1.5 \times V_{maxOP}$ or MSV, whichever is lower in magnitude

(1) In the I-Test, the maximum current is the forced current; in the E-Test the maximum current is a current compliance level (limiting current).
(2) In the I-Test, the maximum voltage is a voltage compliance level (limiting voltage); in the E-Test the maximum voltage is the applied voltage.

Table 5 — Timing Requirements for the Signal Pin Test and the Supply Test

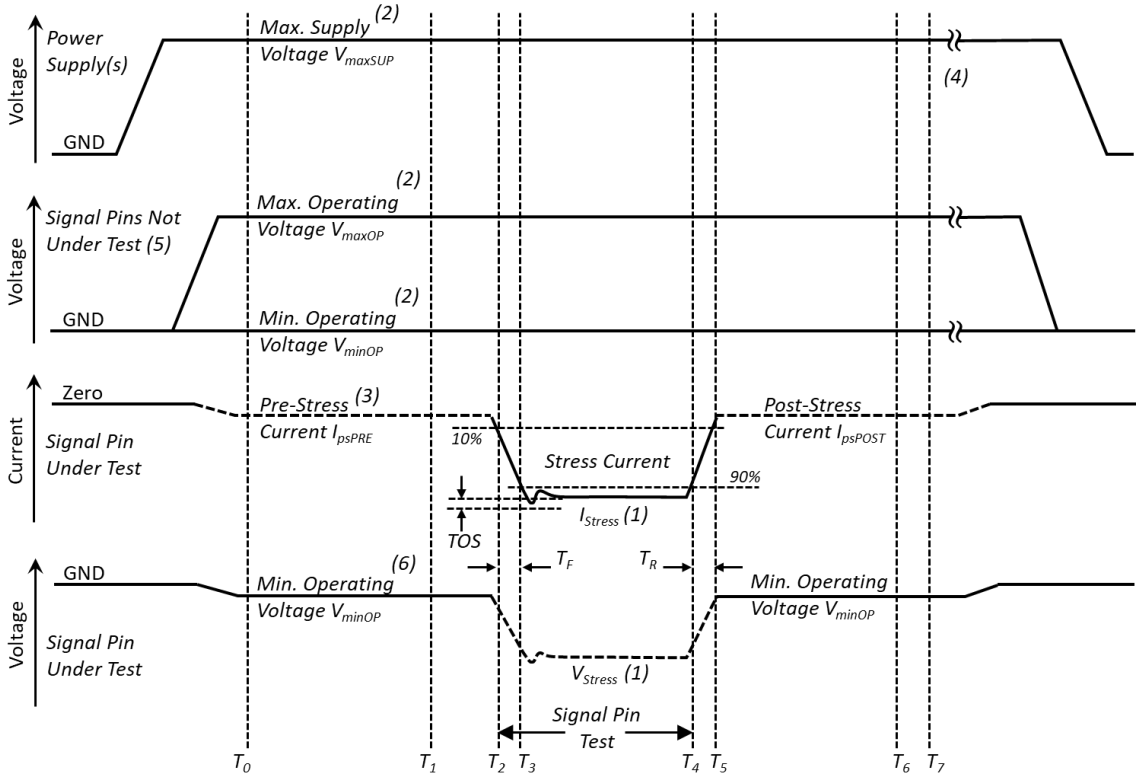
Symbol	Time interval(1)	Parameter	Limits	
			MIN	MAX
t_{wait}	T0 to T1 T5 to T6	Wait time before measuring I_{supply}: The wait time shall be sufficient to allow for power supply ramp up/down and stabilization of I_{supply}	3 ms	5 s
$t_{measure}$	T1 & T6	Measure I_{supply}	Measurement Point	
t_r	T2 to T3	Trigger rise time	1 µs	5 ms
t_{width}	T2 to T4	Trigger duration	$2 \times t_r$ (1)	1 s
t_f	T4 to T5	Trigger fall time	1 µs	5 ms
t_{cool}	T7 to Next Pulse	Cool down time	(3)	
TOS(2)		Trigger over-shoot	± 5% of pulse	

(1) The duration should be verified with an oscilloscope. The pulse should reach and maintain a steady-state value at the target stress level and conform to the waveforms shown in one of the figures of Figure 3 through Figure 6 or Figure 8. This verification should be done:
- during regular, periodic system maintenance/verification,
- after changes in tester hardware or software,
- if a short trigger duration is used (for example, shorter than the tester's default setting),
- if the measured stress level does not meet the target level,
- if latch-up failures are suspected to be caused by waveform anomalies (see Annex F).

(2) For E-Test and Supply Test: Allowed overshoot voltage; or for I-Test: Allowed overshoot current. See Annex F for additional information.
(3) Cool down time should be sufficiently long enough to allow the temperature to stabilize to its pre-trigger value before the next pulse.

5.6.3 Waveforms for the Negative Signal Pin Test – I-Test / E-Test

Figure 5 and Figure 6 visualize the voltage and current waveforms during a negative Signal Pin Test (I-Test and E-Test), with the waveform current and voltage settings defined in Table 6. The waveform timing parameters for the negative Signal Pin Test are identical to the timing parameters of a positive Signal Pin Test; see Table 5.



(1) The waveforms when shown in a solid line are the forced voltages or currents and when shown in dashed lines are the measured voltages or currents.

(2) During I-Test the supply currents for all supply groups are monitored before and after the stress pulse. Latch-up occurs if any supply meets the failure criteria shown in Table 3. Also, power supply voltages shall not collapse during the stress as per Clause 5.5.2.

(3) The pre-stress and post-stress current I_{psPRE} and I_{psPOST} depend on the state and the circuitry of the PUT.

(4) At the conclusion of the stress, returning all power supplies to ground is an option to reset the DUT. Resetting supplies is recommended for stability during testing.

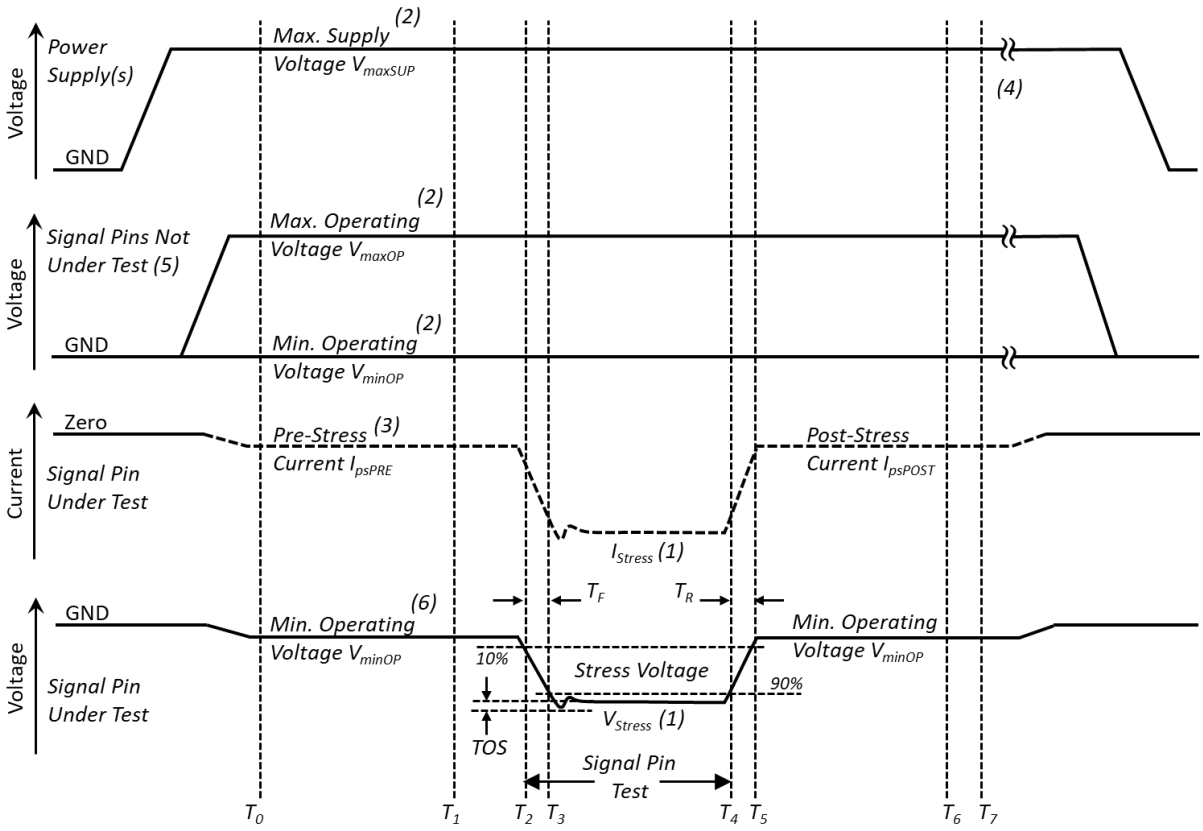
(5) Input pins Not Under Test shall be considered Signal Pins Not Under Test and should be controlled according to Step 4, Clause 5.6.1. Output pins are not included and floated when not under test.

(6) The PUT should be set to logic low (I_{psPRE} & V_{psPRE}) before negative current trigger. Output pins can be omitted from pre/post stress biasing if there is a risk of disturbing the latch-up operating state or risk of pin damage.

NOTE In this negative I-Test example, the I_{Stress} reaches the intended trigger level ("Minimum current during trigger" of Table 6), and the V_{limit} ("Minimum voltage during trigger" of Table 6) is not reached. During pre-stress and post-stress, current is being forced into the PUT but is limited at V_{minOP}. Since the voltage is at a set value, the voltage waveforms are solid lines pre-stress and post-stress. The current is being measured; thus the current waveforms are drawn as dashed lines. During the stress period, the magnitude of the voltage limit is increased, and I_{Stress} reaches its intended trigger level. The current waveform is therefore a solid line during the stress period. The voltage is being measured; thus the voltage waveform is drawn as a dashed line.

Figure 5 — Test Waveform for Negative Signal Pin Test (I-Test)

5.6.3 Waveforms for the Negative Signal Pin Test – I-Test / E-Test (cont'd)



(1) The waveforms when shown in a solid line are the forced voltages or currents and when shown in dashed lines are the measured voltages or currents.

(2) During E-Test the supply currents for all supply groups are monitored before and after the stress pulse. Latch-up occurs if any supply current meets the failure criteria shown in Table 3. Also, power supply voltages shall not collapse during the stress as per Clause 5.5.2.

(3) The pre-stress and post-stress current I_{psPRE} and I_{psPOST} depend on the state and the circuitry of the PUT.

(4) At the conclusion of the stress, returning all power supplies to ground is an option to reset the DUT. Resetting supplies is recommended for stability during testing.

(5) Input pins Not Under Test shall be considered Signal Pins Not Under Test and should be controlled according to Step 4, Clause 5.6.1. Output pins are not included and floated when not under test.

(6) The PUT should be set to logic low (I_{psPRE} & V_{psPRE}) before negative current trigger. Output pins can be omitted from pre/post stress biasing if there is a risk of disturbing the latch-up operating state or risk of damage to the pin.

NOTE: In this negative E-Test example, the I_{Stress} does not reach the intended trigger level ("Minimum current during trigger" of Table 6) because V_{Stress} reaches the V_{limit} ("Minimum voltage during trigger" of Table 6). During the full waveform (including pre-stress, stress, and post-stress), the voltage is at set values, therefore the full voltage waveform is a solid line. The current is being measured; thus the full current waveform is drawn as a dashed line.

Figure 6 — Test Waveform for Negative Signal Pin Test (E-Test)

5.6.3 Waveforms for the Negative Signal Pin Test – I-Test / E-Test (cont'd)

Table 6 — Pulse Current and Voltage Requirements for the Negative Signal Pin Test

Trigger	Minimum current during trigger (1)	Minimum voltage during trigger (2)
Current pulse (I-Test) OR Voltage pulse (E-Test)	I = -100 mA (Table 1)	V = $V_{minOP} - 0.5 \times (V_{maxOP} - V_{minOP})$ with a lower limit of $-0.5 \times V_{maxOP}$ or MSV, whichever is greater in magnitude

(1) In the I-Test, the maximum negative current is the forced current; in the E-Test the maximum negative current is a current compliance level (limiting current).

(2) In the I-Test, the maximum negative voltage is a voltage compliance level (limiting voltage); in the E-Test the maximum negative voltage is the applied voltage.

5.7 Supply Test

5.7.1 Supply Test Flow

All supply pins or supply pin groups on the package are tested with the Supply Test.

The Supply Test shall be performed according to the testing matrix summarized in Table 2. Each supply pin or supply pin group will be stressed with biased inputs tied either to V_{maxOP} voltage or to (V_{minOP}) voltage for a total of two (2) combinations. Latch-up testing will be performed with the waveforms and timing diagrams specified in Clause 5.7.2.

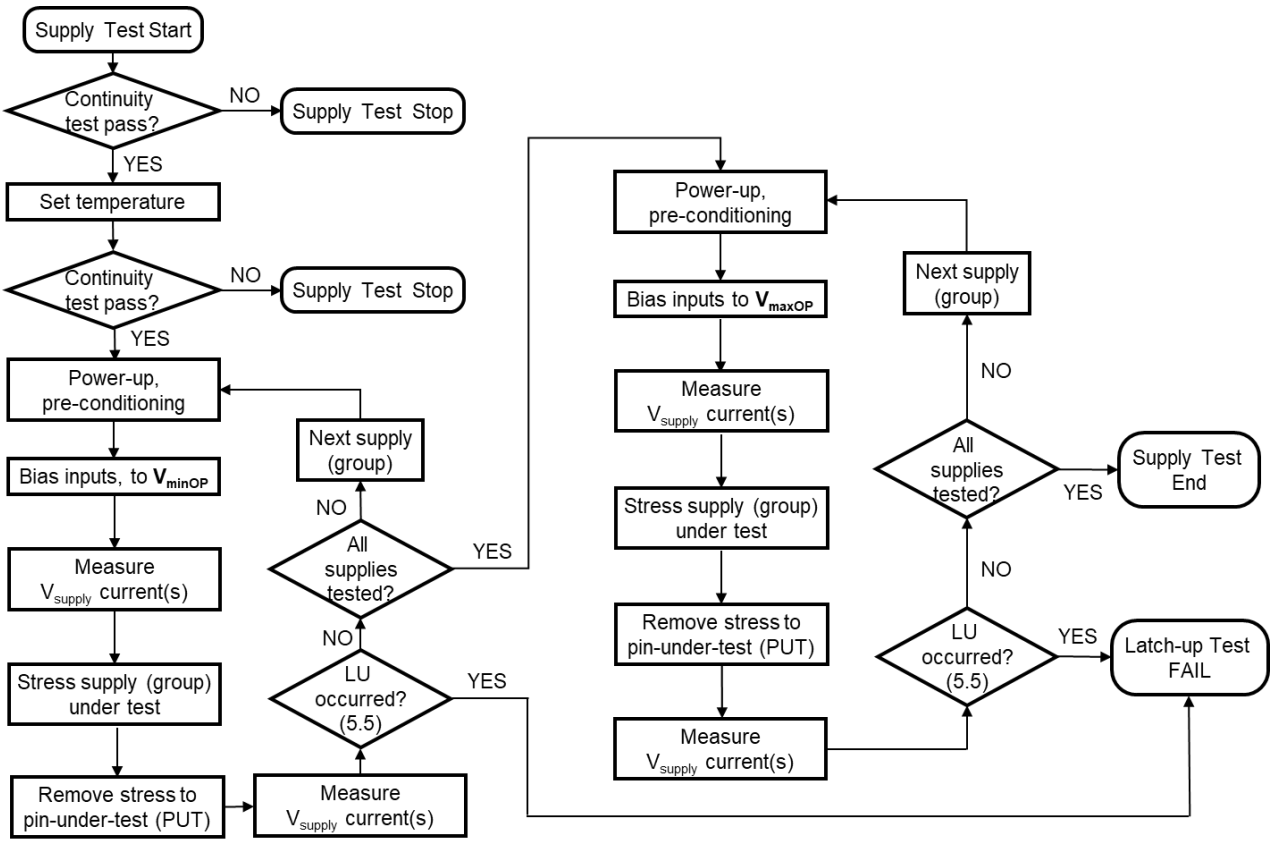
For supply voltages that are negative with respect to ground, overvoltage stress will be in the negative direction.

When performing the Supply Test on power supplies providing power to inputs, the threshold for a high state on the inputs will rise in proportion to the power supply. It is important to ensure that the V_{maxOP} on the inputs remain above the increased logic high threshold or the circuit may change states and create a false latch-up indication.

If a latch-up failure occurs when the input pin(s) fall below the valid logic-high threshold, engineering judgment shall be used to determine whether the failure is a valid latch-up condition, or a failure caused by a change in state.

One suggested detailed Supply Test procedure is given below and in Figure 7. It covers all the conditions in the test matrix in Table 2. The testing order of the stress conditions may vary as long as all conditions are met in the test Matrix table, Table 2. The procedure below describes one possible sequence for performing all Supply Tests with inputs tied to V_{minOP} and with inputs and tied to V_{maxOP}.

5.7.1 Supply Test Flow (cont'd)



NOTE The order of the V_{minOP}/V_{maxOP} setting is arbitrary.

Figure 7 — Supply Test Flow Example: Power Supply Stress with Input Pins Biased to Low (V_{minOP}) and to High (V_{maxOP})

Step:

1) Insert a device that has met electrical specification in the test socket. Ensure that the desired temperature at the DUT has been reached and has stabilized. Check the DUT continuity to ensure that each pin makes good electrical contact. If the DUT continuity fails, re-seat the DUT in the socket until good contact is achieved.
2) Power up the device per power-up sequence specification.
3) Precondition the device according to Clause 5.4.3.
4) Inputs pins that are not used for preconditioning are tied to either V_{maxOP} or V_{minOP} and outputs are floated during stress.
5) Measure nominal I_{supply} at V_{maxSUP} for each supply pin (or supply pin group).
6) After the wait period, apply a voltage trigger into the V_{supply} pin (or pin group) as specified in Clause 5.7.2 and as described in Table 7. Measure the current and voltage of the Stress Supply and V_{supply}(s) during the stress period.

5.7.1 Supply Test Flow (cont'd)

7) After the trigger source has been removed, return the V_{supply} pin (or pin group) to the level before the application of the trigger pulse (voltage equivalent to V_{maxOP}) and measure the I_{supply} at V_{maxSUP} for each V_{supply} pin (or pin group). If any I_{supply} is greater than or equal to the failure criteria specified in Clause 5.5, latch-up has occurred and the DUT has failed latch-up testing. The power supply shall be removed from the DUT to end latch-up, further testing is stopped if latch-up has occurred.

NOTE If the device has failed latch-up, but is not physically damaged, it is permissible to restart the latch-up testing to continue testing the other V_{supply} pins to determine if there are other pins that fail latch-up testing.

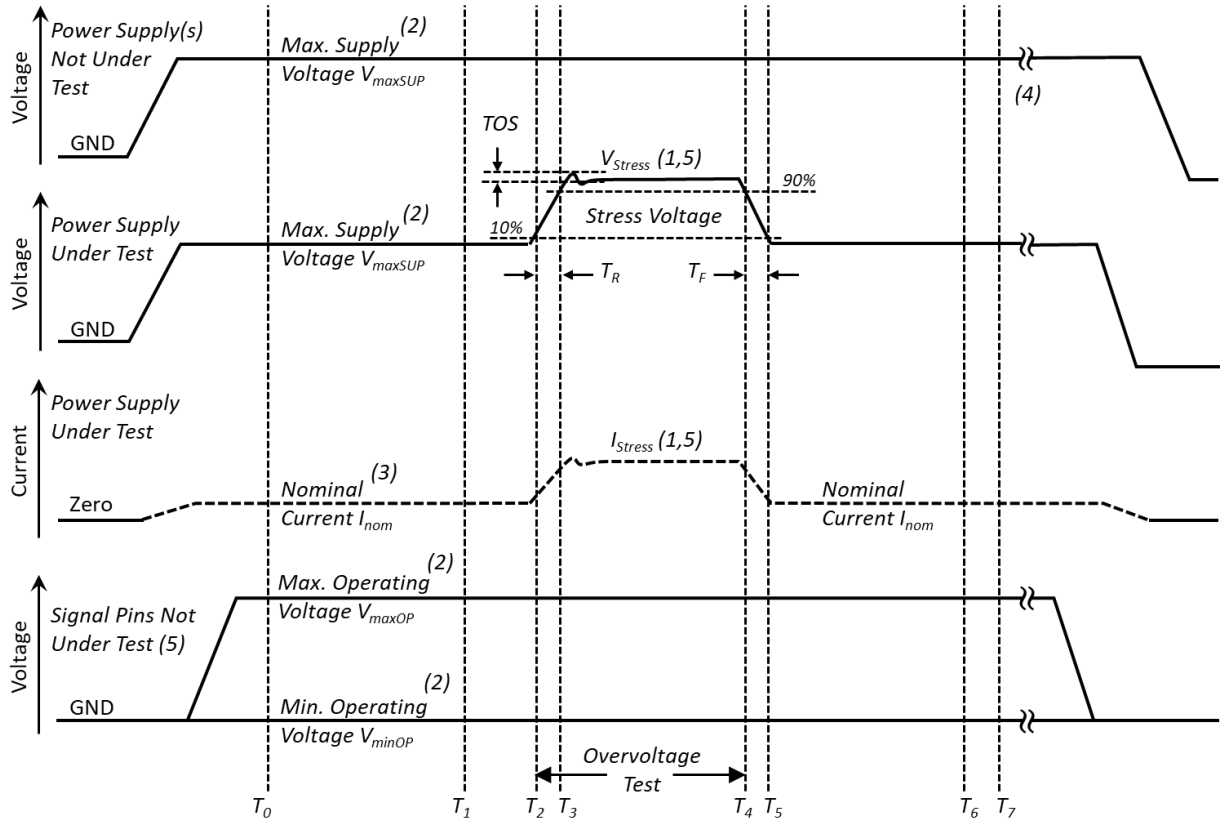
8) If latch-up has not occurred, after the necessary cool-down time, continue to the next supply pin or supply pin group under test and repeat steps 2 through 8 until all supply pins or supply pin groups are tested for the Supply Test.

9) Repeat steps 2 through 10 with input pins tied to V_{minOP}. Input pins needed for preconditioning may be left in the proper preconditioning state. Outputs are left floating (similar to Step 5).

10) It is good practice to perform continuity testing at completion of the stress run at temperature.

5.7.2 Waveforms for the Supply Test

Figure 8 visualizes the voltage settings (waveform) during a Supply Test, with the waveform voltage and current settings defined in Table 7. The waveform timing parameters for the Supply Test are defined in Table 5.



(1) The waveforms when shown in a solid line are the forced voltages or currents and when shown in dashed lines are the measured voltages or currents.

(2) During the Supply Test, the supply currents for all supply groups are monitored before and after the stress pulse. Latch-up occurs if any supply current meets the failure criteria shown in Table 3. Also, power supply voltages shall not collapse during the stress as per Clause 5.5.2.

(3) The pre-stress and post-stress current I_{psPRE} and I_{psPOST} depend on the state and the circuitry of the V_{supply} pin (or pin group).

(4) At the conclusion of the stress, returning all power supplies to ground is an option to reset the DUT. Resetting supplies is recommended for stability during testing.

(5) Input pins Not Under Test shall be considered Signal Pins Not Under Test and should be controlled according to Step 4, Clause 5.7.1. Output pins are not included and floated when not under test.

NOTE In this Supply Test example, the V_{Stress} reaches the intended Trigger Voltage of Table 7, and the I_{limit} is not reached. During the full waveform (including pre-stress, stress, and post-stress), the voltage is at set values, therefore the full voltage waveform is a solid line. The current is being measured; thus the full current waveform is drawn as a dashed line.

Figure 8 — Test Waveform for the Supply Test

5.7.2 Waveforms for the Supply Test (cont'd)

Table 7 — Pulse Current and Voltage Requirements for the Supply Test

Trigger	Trigger Voltage	Trigger Current Limit
Voltage pulse	1.5 × V_{maxSUP} or MSV, whichever is less. (Table 1)	a) $I_{limit} = 100\ mA + I_{nom} = 100\ mA + \sum_{\substack{all\ supplies\ in\ supply\ group\ i}} I_{nom,i}$ or b) $I_{limit} = 1.5 \times I_{nom} = 1.5 \times \sum_{\substack{all\ supplies\ in\ supply\ group\ i}} I_{nom,i}$ whichever is higher.
NOTE The values in the table are minimum requirements to pass the test. The limit values can be higher which, in many cases, may more easily detect a latch-up susceptibility.		

5.8 Functional and Parametric Test After Latch-Up Stress

Functional and parametric testing is required to detect damage from short duration latch-up events or other electrical stress that may occur during latch-up testing.

- Latch-up events triggered during Supply Tests or Signal Pin Tests may damage the device, and the damage could end the latch-up event before the latch-up tester detects the failure (short-duration latch-up). A failure in the functional and parametric test may be the only indication of this kind of latch-up.
- Latch-up Signal Pin Tests could directly damage the DUT through an overstress event not associated with an actual latch-up event.
- Functional and parametric testing can be used as part of the failure analysis to determine the source of damage.
- These types of damage (undetected short-duration latch-up events and non-latch-up induced catastrophic damage) may prevent proper control of the device during automated latch-up testing and could invalidate some latch-up test results for some pins on the device.

Some guidelines to assess the functional and parametric result after a latch-up stress are:

- If the functional and parametric test failure is suspected to be caused by an ESD issue (not latch-up stress), repeat the latch-up test with fresh samples and ensure proper ESD handling guidelines are followed.
- If the functional and parametric test failure is suspected to be caused by non-latch-up induced catastrophic damage during latch-up stress, adjust the trigger pulse according to Table 3, and repeat the latch-up test with fresh samples.

5.8 Functional and Parametric Test After Latch-Up Stress (cont'd)

- If samples latch-up tested to the Immunity Level A conditions in Table 1 still fail, then with fresh samples, the Signal Pin Test can be adjusted to a value at which the integrated circuit can pass the latch-up test and post parametric and functional tests per device datasheet specification.

5.9 Failure Analysis

A variety of failure analysis methods can be useful in analysis of failures from latch-up testing. The situation is most straight forward for latch-up failures which result in physical damage. Fused metal lines can point to the failed circuits. In cases with melted silicon, the damage can show the exact position of an unintended SCR (pnpn) structure. Optical and thermal emission microscopy can be especially useful for finding suspect circuitry in cases both with and without physical damage. Failure analysis can also be used to separate true latch-up failures from simple electrical overstress. In all cases, failure analysis requires considerable engineering judgement and may be guided by the experience and resources available.

5.10 DUT Disposition

Latch-up testing is potentially destructive. Devices used for latch-up testing shall not be used or considered as salable devices.

6 Report Requirements

Suppliers will report:

- The version of JEDEC JESD78 followed during the testing.
- Latch up immunity capability: state the goal of the test and the highest sustained actual stress current for the Signal Pin Test (if Level A or higher) plus state the goal of the test and the highest actual stress voltage for the Supply Test (if Level A or higher), on a device or pin-by-pin basis.
- Integrated circuit classification per Clause 3 and Table 1.
- Number of samples used for each stress condition.
- Signal Pin Test method (I-Test or E-Test) used. If both methods were used, specify which one on a pin-by-pin basis.
- V_{limit} value(s) used (1.5 x V_{maxOP} and/or MSV).
- The I_{limit} settings per supply pin (or supply pin group).
- Any passive or active elements used.
- Specify any unmonitored tester and vector supplies.
- Report test temperature. Specify measured maximum temperature as ambient, case, or junction. Ambient or case temperatures shall achieve Tjmax for Class II testing.

Appropriate data shall be recorded for correlation in case the test has to be rerun. Example of recorded data may include clock frequency (for dynamic devices), pulse width, vector set used for preconditioning, temperature, trigger conditions, supply current limits (I_{limit}) and the latch-up I_{supply} current. Recorded data is especially important for failing pins. Also, for pins that would never have detected latch-up on the application, those pins should be recorded as special pins per Annex A.

Examples for recording and reporting data are shown in Annex D.

Annex A (Informative) Special Pins

A.1 Purpose

Integrated Circuits have become increasingly complex in the types of circuits contained in any individual device. A number of these circuit/pin types have required engineering effort to determine the proper manner to set up and perform latch-up testing. Additionally, devices and test hardware can be damaged by simply applying standard testing methodology.

This annex intends to provide guidance to test these non-standard pin types/configurations. It is not expected to address every possible case and new cases are expected to be added to future revisions of the specification. It is recommended to test all pins without limitations before using allowable limitations described in this annex.
Complex integrated circuits contain individual pins that do not fit cleanly into the categories Signal or Supply Pins.

- Many pin types require special consideration to determine whether the Supply or Signal Pin Test should be run.
- Some pin types require unique pre-configuration or special data assessment methods to properly perform latch-up testing.
- Failure to heed this guidance may result in destructive damage to devices and hardware for certain pin types.
- Some pin types can be tested with relaxed requirements due to lower latch-up risk.

A.2 Pins Creating Latch-Up Challenges

Categories of Signal pins

- Signal pins supplied from internal power domains.
- Pins connected though passive components (resistor or capacitor).
- Differential inputs (Op amps, comparators, diff amps).
- Input/Output pair with inverter between them.
- Multi-mode pins with multiplexed digital and/or analog circuits.
- RF pins with an inductive connection to ground.
- Temp sensing diode pins.

Dual Purpose signal/supply pins

- Pins that act as signal and supply.

A.2 Pins Creating Latch-Up Challenges (cont'd)

Categories of Supply and associated pins

- Voltage or current reference pins.
- Voltage sense pins.
- Current sense pins.
- Onboard DC regulators.
- Onboard Switched mode regulators.
- Circuits with multiple supply sources.
- Power supplies with one-time elevated write voltage for non-volatile programming.
- Power supplies with specific relationships.

A.3 Definitions

Current Reference - is an electronic component or circuit that by forcing a built-in reference voltage through an integrated resistor produces a constant DC output current regardless of variations in external conditions such as temperature, barometric pressure, humidity, voltage demand, or the passage of time.

Current Sense Pins – current sense pins are pin pairs used to detect a differential voltage across a small value resistor and amplify this voltage. The magnitude of the voltage is proportional to the amount of current flowing through the resistor. The current sense resistor could be located near the most positive voltage source (high side) or near the most negative voltage source (low side). In the case of a high side current sense pin pair, there is the added requirement that the pins have to measure the small differential voltage on the resistor with a much larger common mode voltage produced by the most positive voltage. ESD protection for high side current sense pin pairs normally consists of a common mode protection element (pin pair to ground) and differential protection elements (between pin pairs). This type of ESD protection can complicate latch-up testing.

External Ballast Control Pin – An output pin that controls an external ballast transistor (MOS or bipolar) when used as a driver for an on-chip regulator. When the ballast transistor is bipolar, the output drives the base and when the transistor is MOS, the output drives the gate. A pull-up/pull-down resistor and compensation network is typically connected to this output.

LDO Regulator (Low Dropout Regulator) - an LDO regulator is a DC linear voltage regulator which can regulate the output voltage even when the supply voltage is very close to the output voltage**.** Use of internal LDO on devices requires special considerations for latch-up testing.

Switched Voltage Regulator Pin – Any product pin that will be used to implement a switched mode power supply, and which is intended to be connected to an external component such as a power FET, inductor, or capacitor. These pins are typically associated with floating high voltage supplies and will require special handling during latch-up testing.

A.3 Definitions (cont'd)

Voltage Reference - is an electronic component or circuit that produces a constant DC output voltage regardless of variations in external conditions such as temperature, barometric pressure, humidity, current demand, or the passage of time.

Voltage Sense Pin(s) – A pin used to monitor a voltage level on a component for purposes of voltage regulation of an external power supply.

A.4 Special Pin Guidance

This clause will give guidance on developing test plans for some specific device pins requiring extra care during latch-up testing. Flow charts are used extensively to demonstrate the thought process needed for developing special pin test plans.

The flow chart for each individual special pin type contains a numbering scheme for each path of the flow chart (see Clause A.2). For instance, Figure 9 (Pins Connected through Passive Components) highlights six different possible paths, each being numbered 1A-1F. Some of these numbers will be referenced in the Special Pin Application Examples starting in Figure 25.

A.4 Special Pin Guidance (cont'd)

Signal Pin Categories:

Pins Connected through Passive Components – It is recommended to avoid using passive components for these pin types on the product's latch-up test board. These cases may be susceptible to coupled injection particularly if the traces extend beyond the application system or if poor system design practices are used (long traces). Many integrated circuit pins connect to passive components only: resistors, capacitors, and inductors. In some instances, these components are needed for device stability and it is necessary that the passive components be attached to the device during latch-up testing. Reasonable arguments can be made for the elimination of testing for pins that are connected to passive (resistor, capacitor) components only, or reduction of stress levels for passive components that come between the integrated circuit and active signal lines/power supplies/ground. Since the possibility of latch-up being initiated by injected or coupled transients is a real concern, the elimination of all latch-up testing on a pin should be avoided, unless the risk associated with the actual system is fully understood.

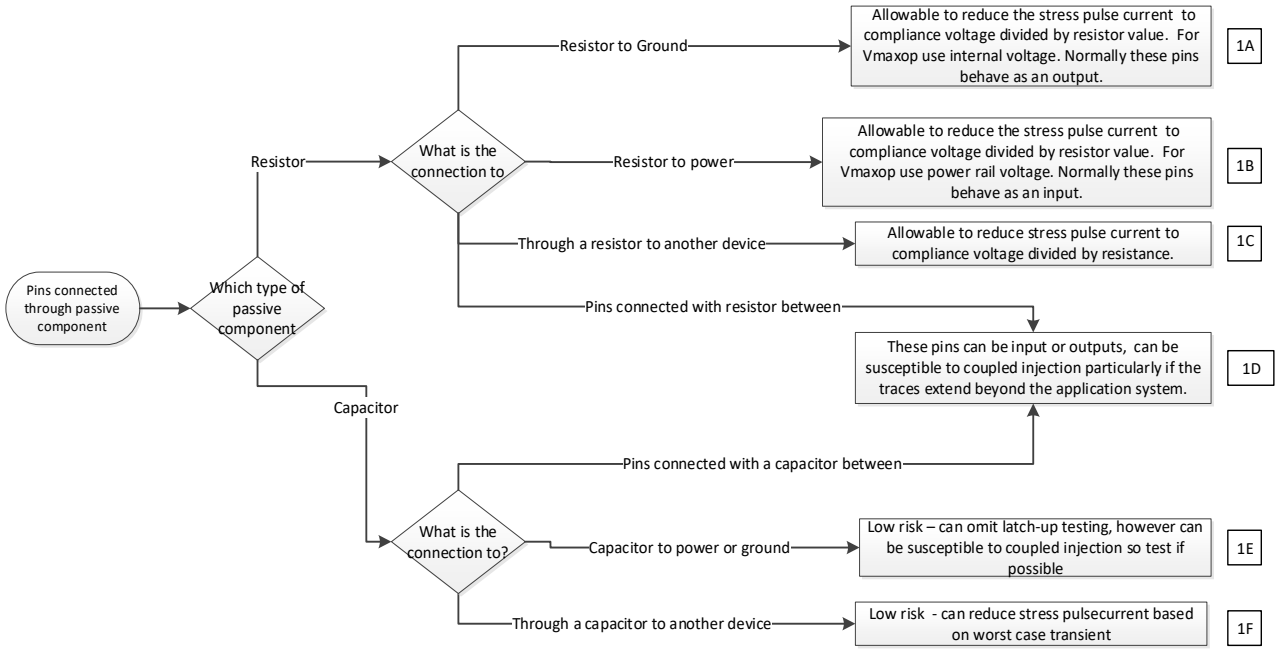


Figure 9 --- Pins Connected through Passive Components

A.4 Special Pin Guidance (cont'd)

Differential Inputs: Op Amp inputs, clock oscillators, Comparators – These pin types can have a high risk of causing unintentional damage to the component and/or test hardware if not handled properly.

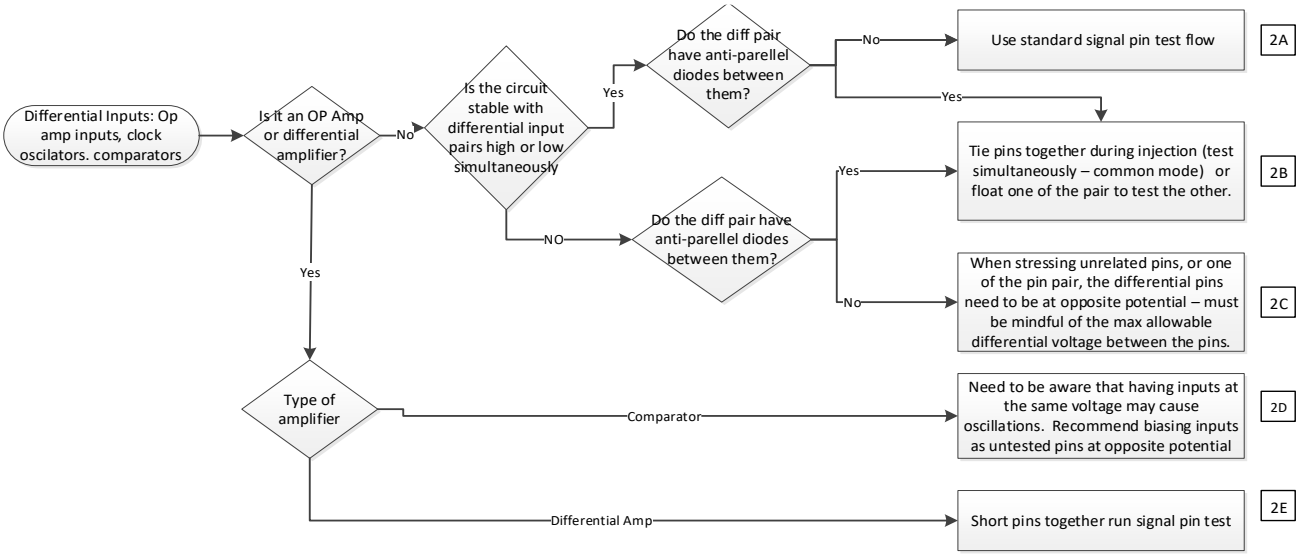


Figure 10 --- Differential Inputs: Op Amp inputs, Clock Oscillators, Comparators

Inputs, Outputs, IOs powered by internal power domain - These pins require special consideration to avoid electrical overstress or to miss an actual latch-up event occurrence.

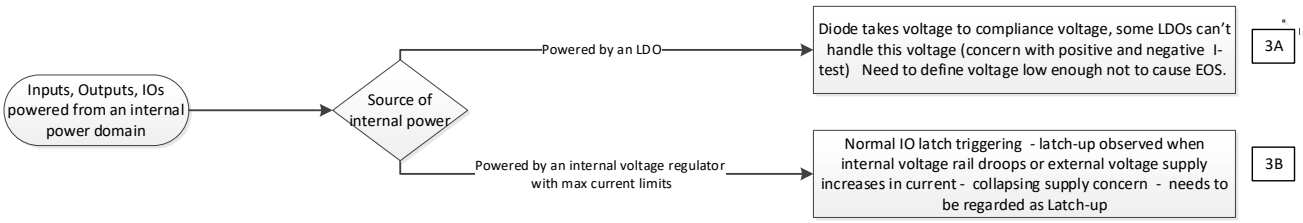


Figure 11 --- Inputs, Outputs, IOs powered by internal power domain

Input/Output Pair with an inverter between them - Requires modification of V_{maxOP} or V_{minOP} biasing.

Figure 12 --- Input / Output Pair with an Inverter In-Between

A.4 Special Pin Guidance (cont'd)

Multi-mode pins with multiplexed digital and/or analog circuits - Pins with multiple functions need to be assessed for latch-up in each mode if latch-up protection is inside of the Multiplex circuits.

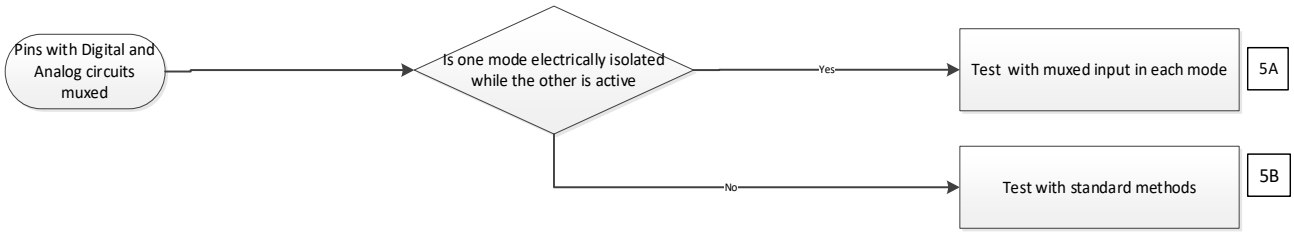


Figure 13 --- Pins with Digital and/or Analog Circuits Multiplexed

RF pins with an inductive connection to ground - RF pins may be particularly sensitive to excessive current.

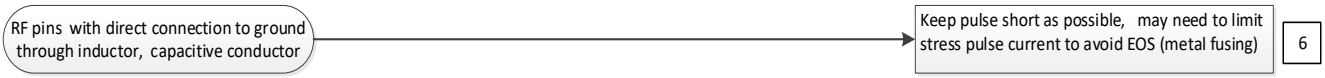


Figure 14 --- RF pins with direct connection to Ground

Temperature sensing diode pins - Thermal diode pins typically are in pairs(anode/cathode).

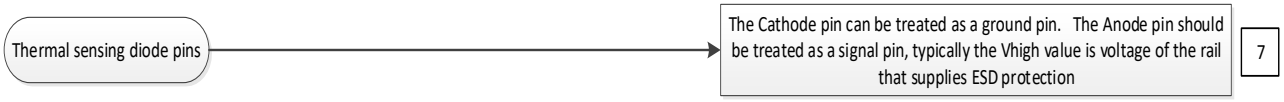


Figure 15 --- Temperature Sensing Diode Pins

A.4 Special Pin Guidance (cont'd)

Dual Signal / Supply Categories:

Multi-mode Signal/Supply pins - Certain pins may act as a signal pin or a supply pin dependent on the usage case.

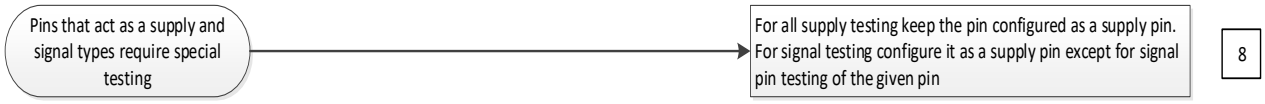


Figure 16 --- Multi-mode Signal/Supply Pins

<u>Supply and Associated Pin Categories:</u>

Voltage and Current Reference Pins - These pins are often labeled with power supply-like naming, but usually need to be tested as Signal Pins.

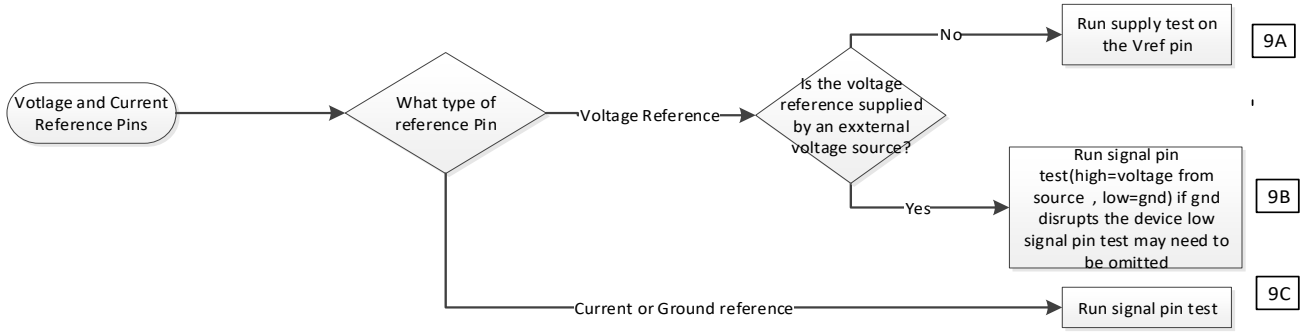


Figure 17 --- Voltage and Current Reference Pins

Voltage Monitor and Sense Pins - These pins are often labeled with power supply-like naming, but usually need to be assessed with Signal Pin Test.

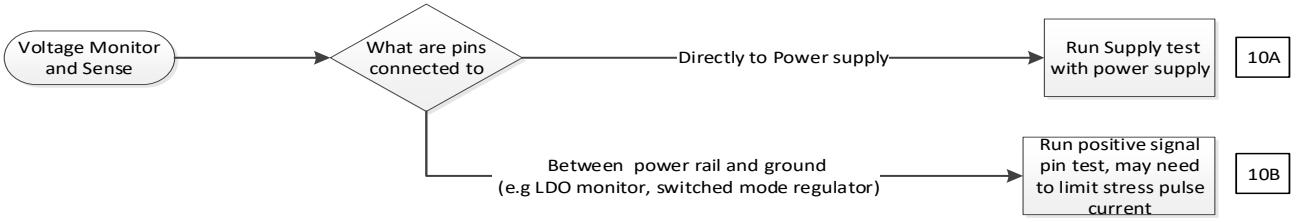


Figure 18 --- Voltage Monitor and Sense Pins

A.4 Special Pin Guidance (cont'd)

Current Sense Pins - Current sense pins require special handling to avoid device damage**.**

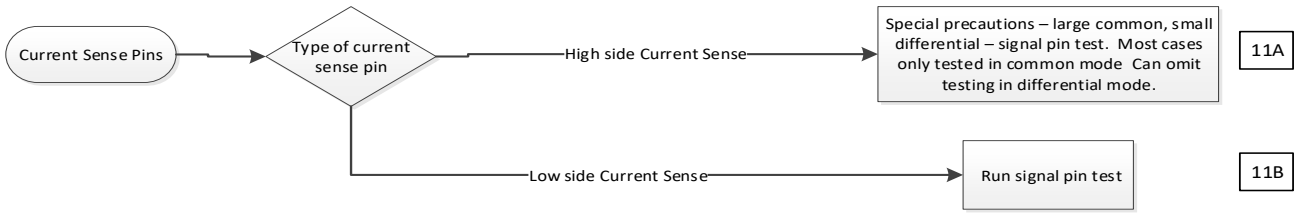


Figure 19 --- Current Sense Pins

Table 8 --- DC Regulator Cross References

Pin Name Cross Reference Table		
Function	**Integrated regulator**	**Gate Driver/regulator**
Switch pin	SW or PH or LX (device output)	HS or LX or PH (normally a power supply)
High side driver	Internal	HO or HDRV
Low side driver or grounding FET	Internal	LO or LDRV
Boot	C_{boot}, Boot, Boost	HB or VB

A.4 Special Pin Guidance (cont'd)

DC Voltage Regulators - There are a number of special cases that arise with devices that contain DC voltage regulators that may supply internal or external circuits. Signal Pin Test and/or Supply Test may be required.

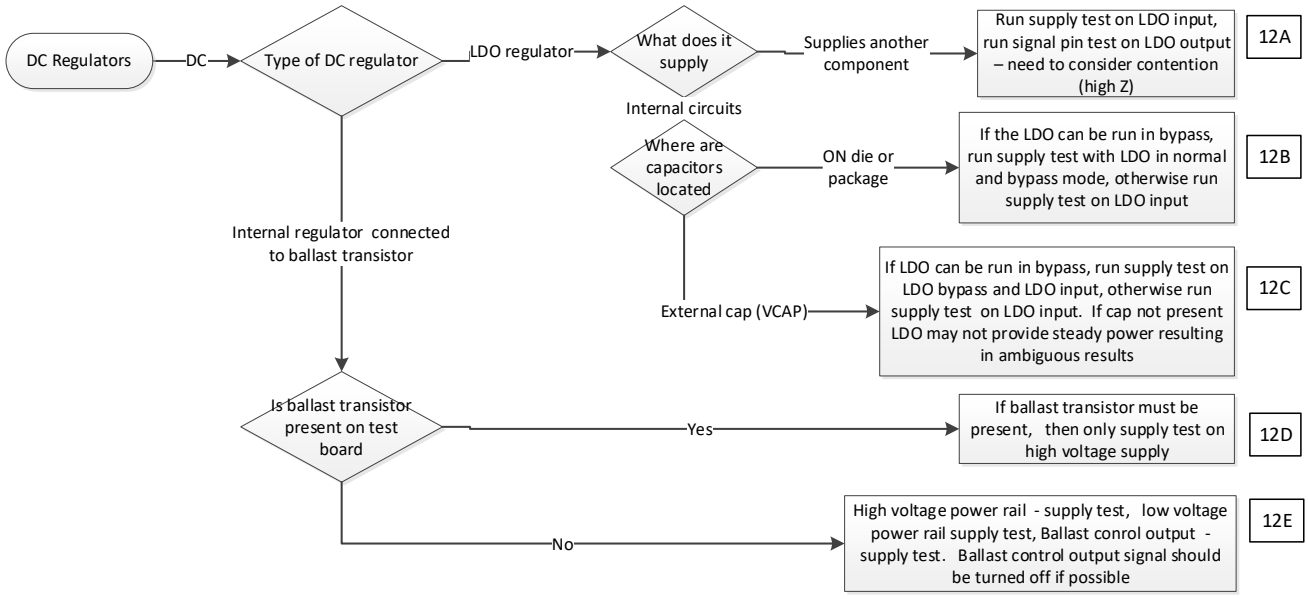


Figure 20 --- DC Voltage Regulators

A.4 Special Pin Guidance (cont'd)

Switched voltage regulators - This flow chart shows a range of general cases - particularly for Case 11B where there are many variants which may require engineering assessment. Components with switched voltage regulators have the potential for device damage if handled improperly. Some of these specific constraints can be addressed in the component specification.

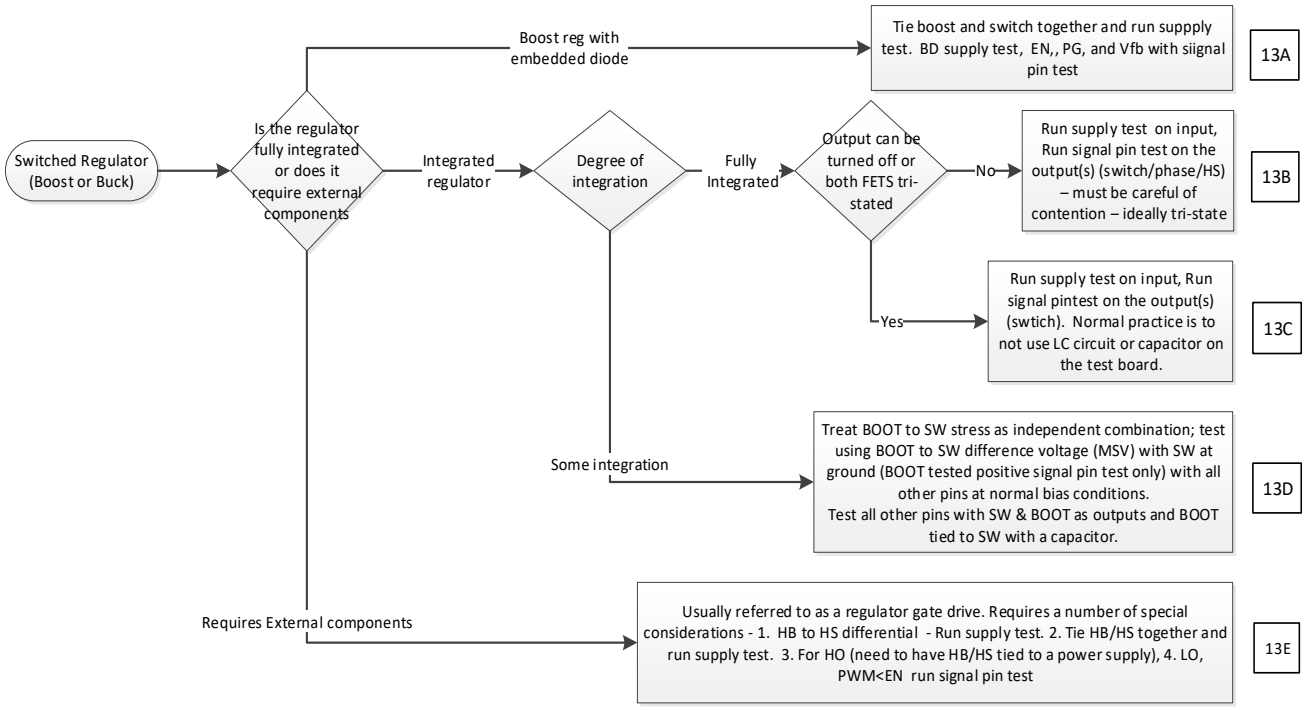


Figure 21 --- Switched Voltage Regulators

Circuits with multiple supply sources – Components can have more than one power supply for a given portion of circuitry.

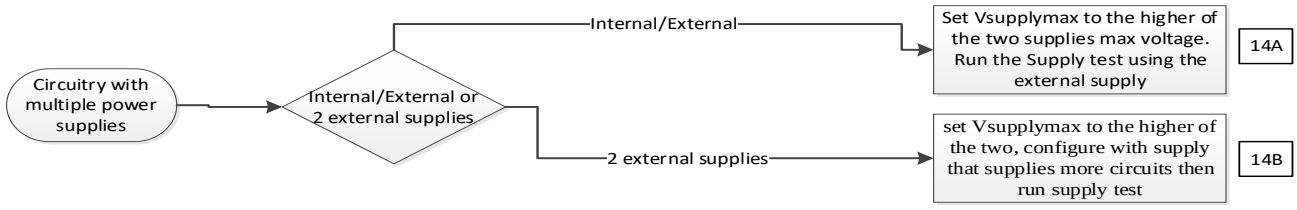


Figure 22 --- Circuits with Multiple Supply Sources

A.4 Special Pin Guidance (cont'd)

Power supplies with a one-time elevated write voltage for non-volatile programming

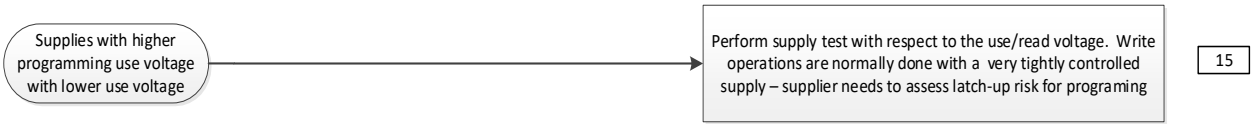


Figure 23 --- Non-Volatile Programming Pins

Power supplies with specific relationships

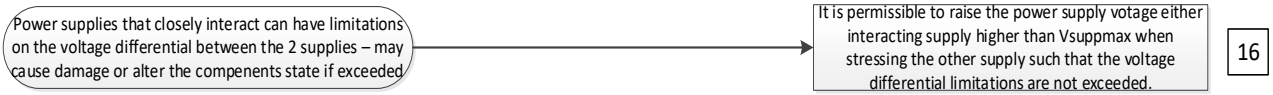


Figure 24 --- Power Supplies with Specific Relationships

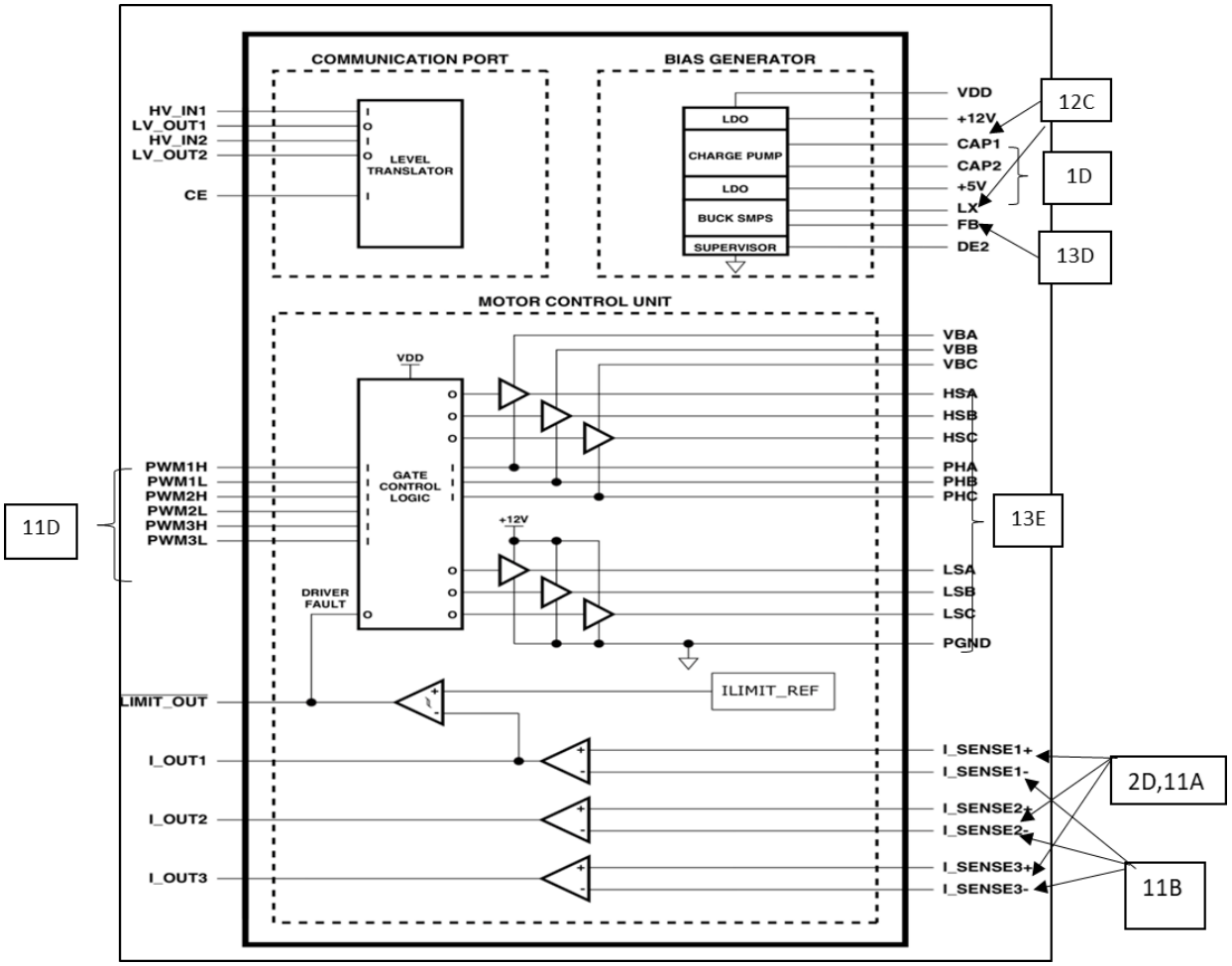


Figure 25 --- Example 1: Complex Microcontroller

A.4 Special Pin Guidance (cont'd)

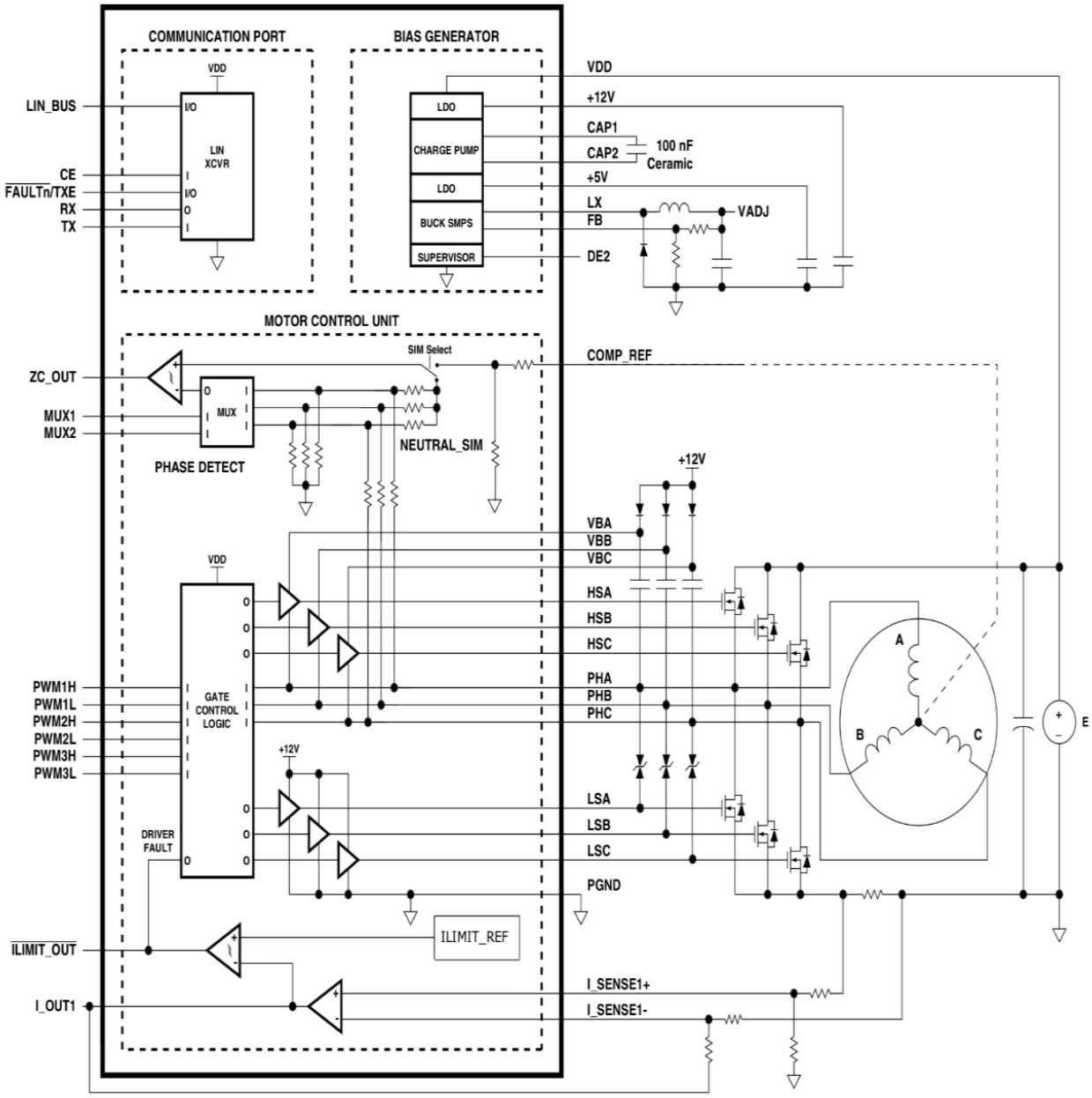


Figure 26 --- Example 1: as used in a Typical Application

A.4 Special Pin Guidance (cont'd)

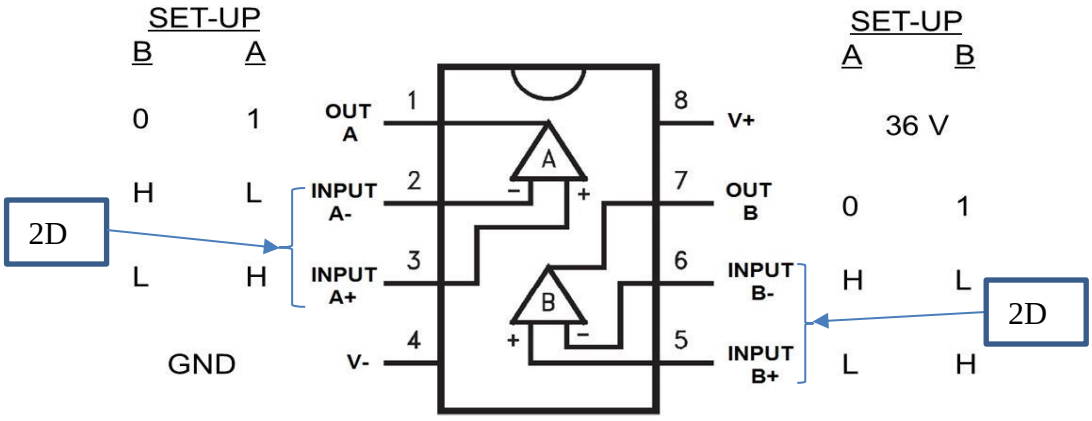


Figure 27 --- Example 2: Differential Comparator

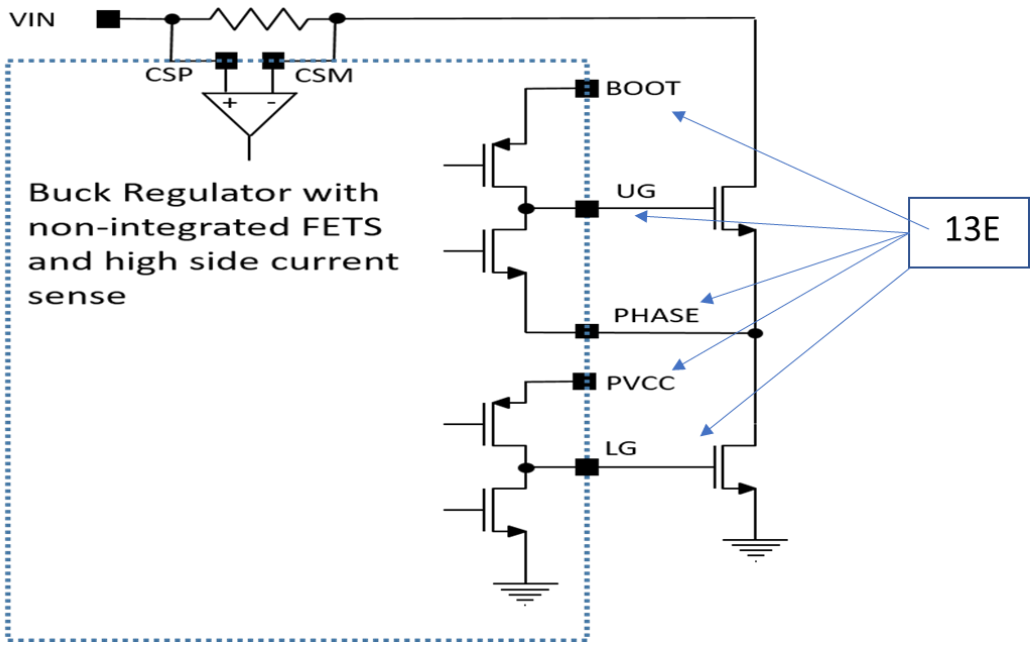


Figure 28 --- Example 3: Non-integrated Regulator

A.4 Special Pin Guidance (cont'd)

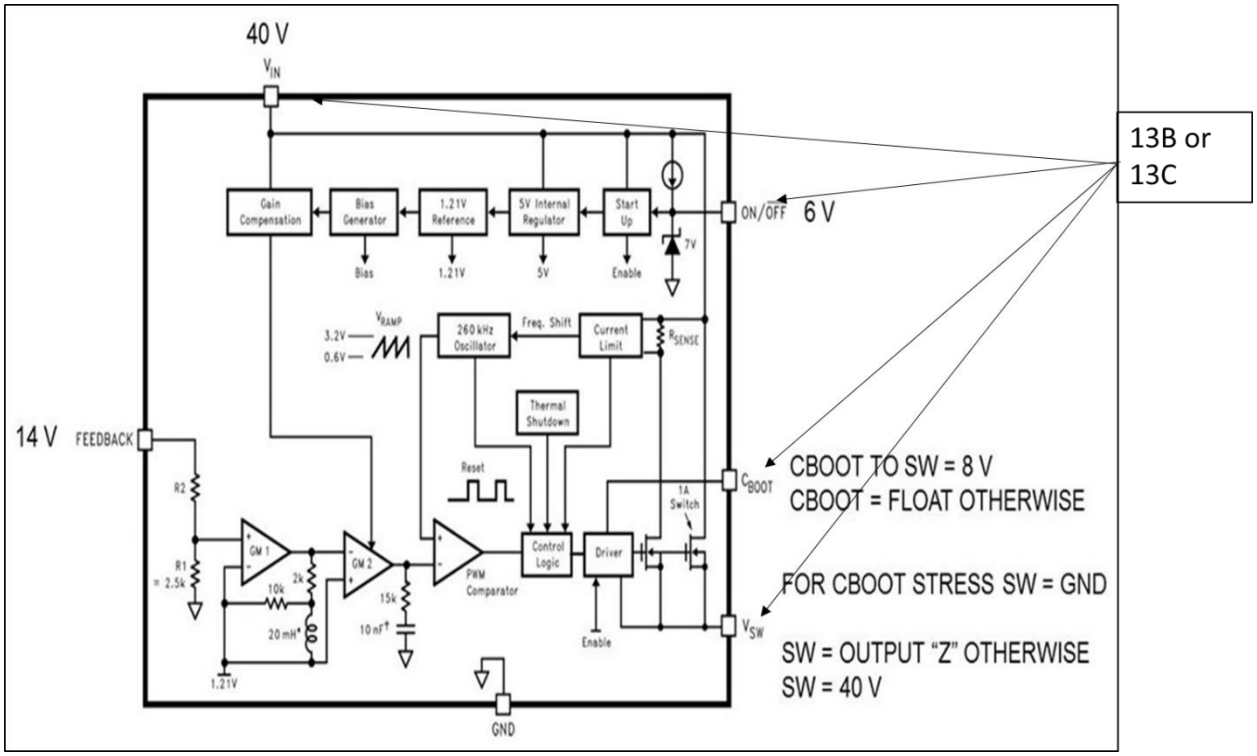


Figure 29 --- Example 4: Integrated Regulator

Annex B (Informative) Calculations for Junction, Ambient or Case Temperature

Device datasheets will typically specify maximum junction, case or ambient temperature required for operating a part. Datasheets will typically also specify maximum operating voltage, current consumption and or power consumption. If only one temperature (junction, ambient or case) is specified, the other temperatures can be calculated using the power consumption and appropriate heat transfer coefficients for the operating condition.

Operating conditions of interest for this specification are field operation and latch-up test conditions. As an example, the power consumption in the field for T_{jmax} calculation is typically higher than during latch-up testing. Similarly, the heat transfer coefficient for a forced air system blowing on the surface of a DUT during latch-up testing can be higher than field operation of the part in still air or with a fan cooled heatsink. When performing temperature calculations, it is important to use the power consumption and heat transfer values applicable to the test condition.

In the following, methods for calculating ambient (T_a), case (T_c) or junction (T_j) temperature are determined by using three parameters.

The first parameter, P_{LU} (power latch-up test) or P_{FIELD} (power in the field), is the average power consumption defined as the product of nominal supply voltage and nominal supply current under in the field or latch-up test condition applicable to the calculation. For field operation calculations, voltage, power consumption and temperature are the datasheet maximums. For the latch-up test condition calculations, the power consumption just prior to application of the trigger is used in conjunction with the desired test temperature and voltage.

The second and the third parameters are θ_{ja} and θ_{jc}, the thermal resistances relative to ambient and package case, respectively. As with power consumption, the thermal resistance should be appropriate to the test condition of field operation or latch-up testing.

However, it should be noted that the thermal resistance for junction to case, θ_{jc}, and junction to ambient, θ_{ja}, during latch-up testing may not be the same as during field operation. Awareness of the differences in heat transfer coefficients during latch-up testing and in the field is important for achieving the proper latch-up test temperature. A description of methods frequently used to achieve T_{jmax} during latch-up testing are described below.

B.1 Calculating Operating Ambient Temperature T_a or T_j from One Known Temperature

If the operating ambient temperature is T_a, the operating junction temperature is Tj, the device power consumption under latch-up test condition is P_{LU}, and the ambient environment to transistor junction thermal resistance is θja, the following equation is used for calculating T_a from the required Tj, or vice versa. It should be noted that for field operations, the dynamic power consumption and the transistor junction leakage at Tjmax will affect P_{FLD}. For field operation calculations temperature calculations, substitute P_{FLD} for $P_{LU.}$

$$T_a = T_j - P_{LU} \times \theta_{ja}$$

or

$$T_j = T_a + P_{LU} \times \theta_{ja}$$

B.2 Calculating Operating Case Temperature T_c or T_j from One Known Temperature

If the operating case temperature is T_c, the operating junction temperature is Tj, the device power consumption under latch-up test condition is P_{LU}, and the ambient environment to transistor junction thermal resistance is θ_{jc}, the following equation is used for calculating T_c from the required Tj or vice versa. For field operation calculations temperature calculations, substitute P_{FLD} for $P_{LU.}$

$$T_c = T_j - P_{LU} \times \theta_{jc}$$

or

$$T_j = T_c + P_{LU} \times \theta_{jc}$$

B.3 Temperature Monitoring and Control Equipment

Some form of temperature monitoring is needed to ensure that the DUT is at the proper temperature prior to initiating latch-up stress.

Devices having the capability to monitor temperature using an on die thermal diode or other built in temperature monitoring functionality can use this capability to monitor Tj. Any on die thermal monitor should be properly calibrated to ensure the monitor is accurate.

It may not be possible to directly measure Tj for some DUT types. If this is the case, other monitoring methods can be used to control Tj. Typically, this requires other temperature parameters such as package temperature, forced air stream temperature or the temperature of a conductive heat transfer surface used to heat or cool the DUT. If these methods are used, it is necessary to calculate the thermal resistance between the monitored parameter and Tj. Examples of monitoring and control equipment include the following:

B.3 Temperature Monitoring and Control Equipment (cont'd)

- Use of thermocouples or other temperature sensors embedded in the package and/or in contact with the die that can be used to characterize the effect of temperature forcing systems and measure package or die surface temperature. If package temperature is measured and the case to junction thermal resistance during test is known, package temperature can then be used to monitor Tj. Similarly, if the thermal resistance between the die surface and Tjmax is known, die surface temperature can be used for temperature monitoring. See Annex B.1 and B.2 for a description of how to calculate Tj based on T_C and thermal resistance.
- Temperature controlled forced air heating and cooling systems – When using a temperature controlled forced air system, the temperature of the air impinging on the package may be the only monitor available. If the thermal resistance between the temperature of the forced air and Tj is known through pre-characterization and/or thermal modeling, the temperature of the forced air can be used to represent Tj. This approach can be used when power dissipation of a DUT is low during test and heat dissipation wait periods are used after preconditioning to allow operational heat to dissipate. When initiating or changing temperature set points of forced air systems, adequate time should be allotted to allow the junction temperature to reach thermal equilibrium with the forced air and stabilize at the desired Tj.
- Robotic and automated handlers – Robotic and automated handlers frequently use on die temperature monitors such as thermal diodes to measure and provide analog or digital feedback to the handler. These handlers actively control the heating and/or cooling source for maintaining the desired latch-up Tj. If no die-on-die thermal monitor capability is available, the handler set point should be set at Tjmax.
- Other Temperature Control methods (for example., hotplates, cold plates, Peltier devices, radiant heaters, etc.):
    - When using any temperature control system, heat will flow into and out of the surfaces of the DUT at the points of heat transfer.
    - It is typically necessary to apply temperatures above (when heating) or below (when cooling) the desired Tj set point to account for the thermal gradient between the heat transfer surface or temperature monitoring point and the DUT transistors.
    - Thermocouples, pre-characterization and/or thermal modeling, as described above, can be used to accurately predict and control Tjmax based on the temperature offset between the hottest junction on the die and the set point of the thermal control method.
    - Conductive and radiant temperature control methods will often have a slow response time for set point changes. Adequate time should be allotted to allow the junction temperature to stabilize at the desired T_{jmax} when using these types of systems for thermal monitoring and control.

B.4 Device Temperature Control

B.4.1 Temperature Control Methodology

Latch-up testing should be performed in the lowest low power state possible so that latch-up current changes can be detected. In some cases, the physical configuration of the latch-up tester prevents use of heat dissipation methods and ambient conditions that a device would see in field operation. For devices with higher power consumption during field operation than the low power state used for latch-up testing, the DUT should often be heated to achieve maximum operating temperature due to the low power consumption. It is therefore not unusual for latch-up temperature control to differ from temperature control in field operation.

For devices with high power consumption during latch-up testing, it may be necessary to cool the part to maintain the temperature needed for latch-up testing. It is also possible that both cooling and heating are necessary for parts that consume high power during pre-conditioning for latch-up, but then go into a low power state when latch-up stress is applied. As an example, the device could be cooled for the preconditioning pattern burst, and then heated for the duration of the low power state when latch-up stress is applied.

Any temperature control method used during latch-up testing should account for any heat applied to the DUT (typically conductive or forced convection), any thermal dissipation from the DUT, power consumption in low power states and power transients that occur during device preconditioning. Use of cooling systems, minimization of self-heating and use of cool down periods or reduced clock frequencies for preconditioning can be used as mitigation techniques to cool the device during preconditioning and allow the temperature to stabilize at the desired temperature when latch-up stresses are applied.

B.4.2 Class II Testing

Since the likelihood of latch-up occurring increases with temperature, Class II latch-up testing must be performed at the maximum temperature specified in the product data sheet.

Product datasheets typically specify maximum operating junction temperature (T_{jmax}). This typically applies to the hottest junction on the die. However, some product datasheets define maximum operating temperature in terms of maximum case temperature (T_{cmax}) or maximum ambient temperature (T_{amax}).

When reporting the Class II test temperature, the latch-up test report should indicate T_{jmax}, T_{amax} or T_{cmax} applicable to the product datasheet. Using T_{cmax} or T_{amax} as a set point for temperature control during latch-up testing can result in inaccurate temperature control if the temperature control methods used for field operation differ from those used during latch-up testing. If a datasheet specifies T_{cmax} or T_{amax} and not T_{jmax}, an equivalent T_{jmax} can be calculated using the methods discussed in this Annex. The calculated equivalent T_{jmax} can then be used as the set point for the latch-up testing temperature control method used to achieve Class II test temperatures.

B.4.3 T_{jmax} Determination

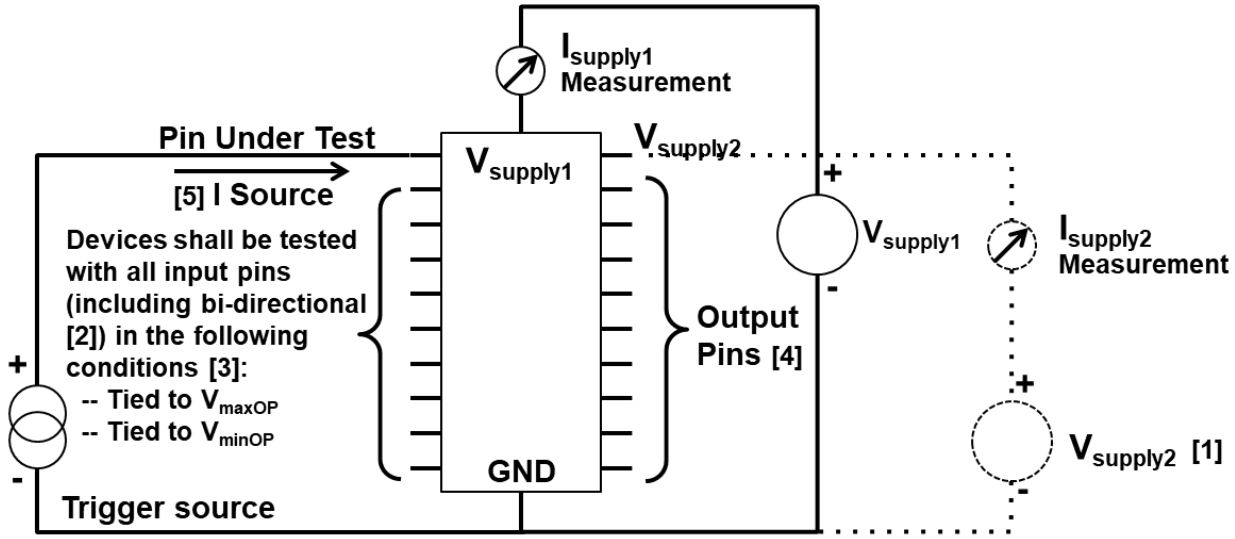
Proper temperature control for Class II latch-up testing is critical to accurately test a product. T_j can vary spatially across the die during operation. Datasheet T_{jmax} typically refers to the hottest junction on the die. Using the datasheet T_{jmax} (or its equivalent) for latch-up testing ensures that any latch-up sensitivities for the hottest junction are evaluated at the maximum field operating temperature.

If T_{jmax} is not listed in the product datasheet, it can be calculated from the applicable datasheet temperature specification, such as T_{cmax} or T_{amax}, using the appropriate thermal resistance coefficients and dissipated power. This Annex provides equations for calculating T_j, T_a and T_c based on dissipated power and thermal resistance (θ).

The thermal resistance for junction to case (θ_{jc}) and junction to ambient (θ_{ja}) during latch-up testing may not be the same as during field operation. Awareness of the differences in heat transfer coefficients and dissipated power during latch-up testing and in the field is important for achieving the proper latch-up test temperature.

Annex C (Informative) Equivalent Circuits for Latch-Up Testing

Positive Signal Pin Test (I-Test):



NOTE 1 DUT biasing includes additional V_{supply} sources as required.

NOTE 2 DUT is preconditioned so that all signal pins are placed in a valid state per Clause 5.1. Signal pins in the output state are open circuit, except when being latch-up tested.

NOTE 3 V_{maxOP} and V_{minOP} are per the device specification. When bias levels are used in respect to a non-digital device, it means the maximum high (V_{maxOP}) or minimum low (V_{minOP}) voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

NOTE 4 Output pins are open circuit except when latch-up tested.

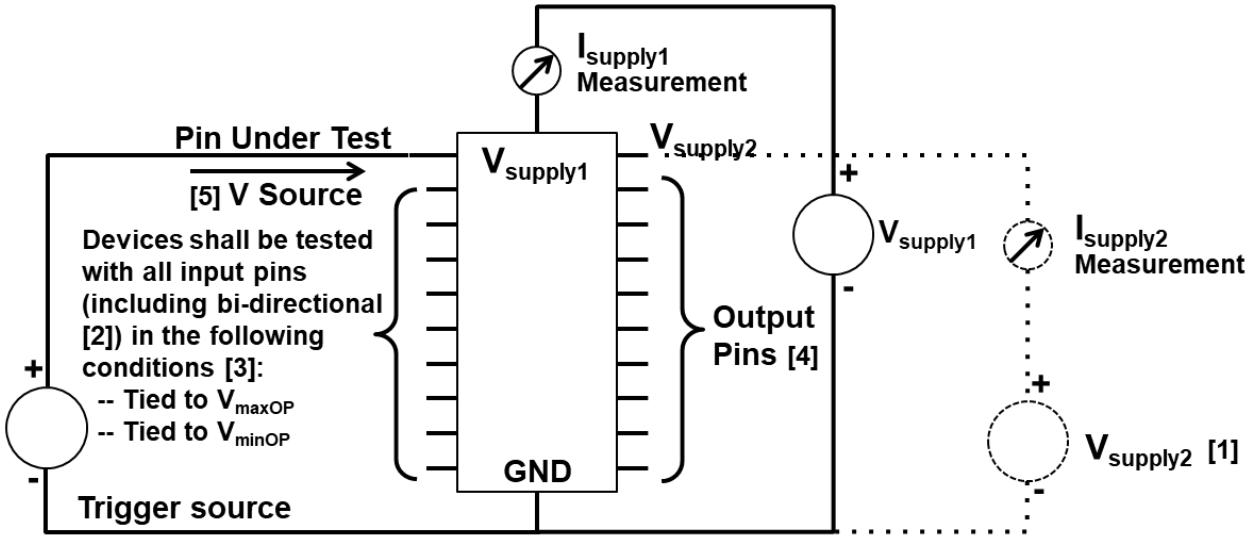
NOTE 5 The trigger test condition is defined in Figure 3 and Table 4.

NOTE 6 Dynamic devices may have timing signals applied per Clause 4.1.1.

Figure 30 — Equivalent Circuit for Positive Current Pulse Signal Pin Test Latch-Up Testing

Annex C (Informative) Equivalent Circuits for Latch-Up Testing (cont'd)

Positive Signal Pin Test (E-Test):



NOTE 1 DUT biasing includes additional V_{supply} sources as required.

NOTE 2 DUT is preconditioned so that all signal pins are placed in a valid state per Clause 5.1. Signal pins in the output state are open circuit, except when being latch-up tested.

NOTE 3 V_{maxOP} and V_{minOP} are per the device specification. When bias levels are used with respect to a non-digital device, it means the maximum high (V_{maxOP}) or minimum low (V_{minOP}) voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

NOTE 4 Output pins are open circuit except when latch-up tested.

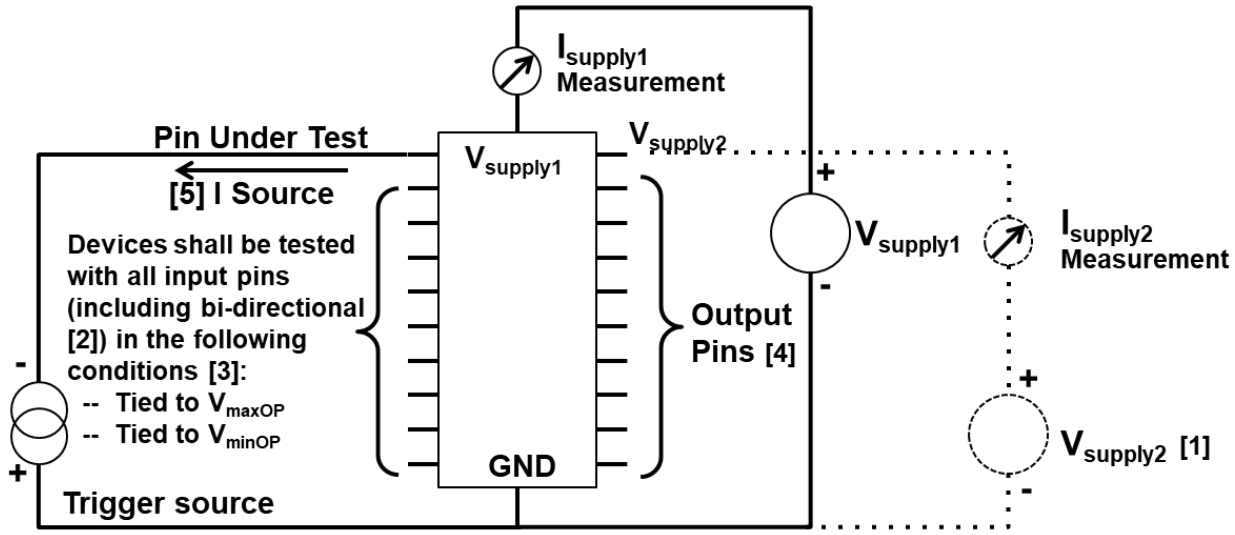
NOTE 5 The trigger test condition is defined in Figure 4 and Table 4.

NOTE 6 Dynamic devices may have timing signals applied per Clause 4.1.1.

Figure 31 — Equivalent Circuit for Positive Voltage Pulse Signal Pin Test Latch-Up Testing

Annex C (Informative) Equivalent Circuits for Latch-Up Testing (cont'd)

Negative Signal Pin Test (I-Test):



NOTE 1 DUT biasing includes additional V_{supply} as required.

NOTE 2 DUT is preconditioned so that all signal pins are placed in a valid state per Clause 5.1. Signal pins in the output state are open circuit, except when being latch-up tested.

NOTE 3 V_{maxOP} and V_{minOP} shall be per the device specification. When bias levels are used with respect to a non-digital device, it means the maximum high (V_{maxOP}) or minimum low (V_{minOP}) voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

NOTE 4 Output pins are open circuit except when latch-up tested.

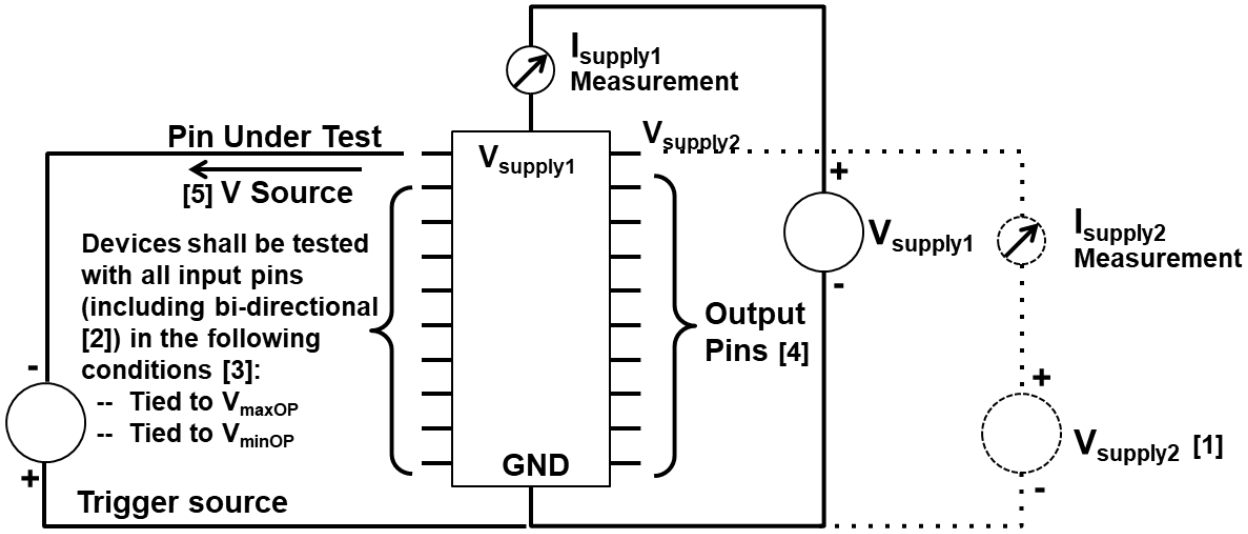
NOTE 5 The trigger test condition is defined in Figure 5 and Table 6.

NOTE 6 Dynamic devices may have timing signals applied per Clause 4.1.1.

Figure 32 — Equivalent Circuit for Negative Current Pulse Signal Pin Test Latch-Up Testing

Annex C (Informative) Equivalent Circuits for Latch-Up Testing (cont'd)

Negative Signal Pin Test (E-Test):



NOTE 1 DUT biasing includes additional V_{supply} as required.

NOTE 2 DUT is preconditioned so that all signal pins are placed in a valid state per Clause 5.1. Signal pins in the output state are open circuit, except when being latch-up tested.

NOTE 3 V_{maxOP} and V_{minOP} shall be per the device specification. When bias levels are used with respect to a non-digital device, it means the maximum high (V_{maxOP}) or minimum low (V_{minOP}) voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

NOTE 4 Output pins are open circuit except when latch-up tested.

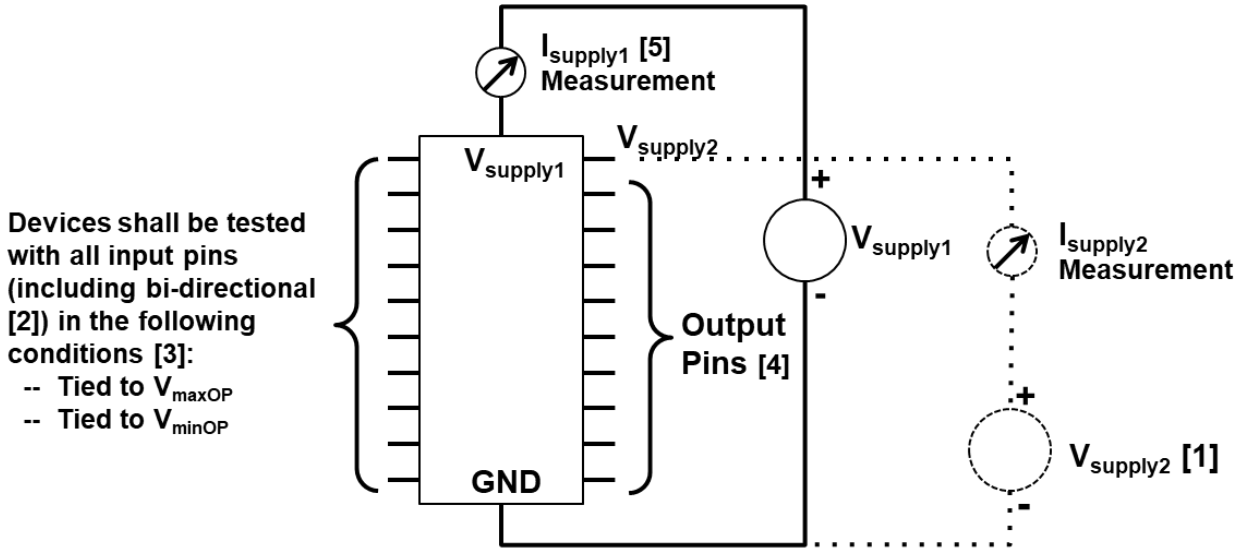
NOTE 5 The trigger test condition is defined in Figure 6 and Table 6.

NOTE 6 Dynamic devices may have timing signals applied per Clause 4.1.1.

Figure 33 — Equivalent Circuit for Negative Voltage Pulse Signal Pin Test Latch-Up Testing

Annex C (Informative) Equivalent Circuits for Latch-Up Testing (cont'd)

Supply Test Method:



NOTE 1 DUT biasing includes additional V_{supply} sources as required.

NOTE 2 DUT is preconditioned so that all signal pins are placed in a valid state per Clause 5.1. Signal pins in the output state are open circuit.

NOTE 3 V_{maxOP} and V_{minOP} shall be per the device specification. When bias levels are used with respect to a non-digital device, it means the maximum high (V_{maxOP}) or minimum low (V_{minOP}) voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

NOTE 4 Output pins are open circuit.

NOTE 5 The trigger test condition is defined in Figure 8 and Table 7.

NOTE 6 Dynamic devices may have timing signals applied per Clause 4.1.1.

Figure 34 — Equivalent Circuit for Supply Test Latch-Up Testing

Annex D (Informative) Reporting Data Examples

Example #1 for reporting data:

a) Test was performed at 125°C case temperature equivalent to Tjmax = 140°C (Class II). Tjmax is estimated to be 140°C.

b) Signal pin group #1 (V_{maxOP} = 4 V) passes +100 mA/-200 mA I-Test with limit voltage at MSV of 5 V.

c) Signal pin group #2 (V_{maxOP} = 4 V) passes +200 mA/-100 mA I-Test with limit voltage at 6 V (1.5 x V_{max}).

d) Supply groups pass 1.5 x V_{maxSUP} except the 3 V (V_{maxSUP} = 3.15 V) and the 0.9 V (V_{maxSUP} = 0.93 V) groups that pass MSV values of 4 and 1.2 V, respectively.

e) Standby pin was not tested due to product conditioning requirement.

f) Immunity Level A achieved.

Example #2 for reporting data with a collapsing tester supply:

a) Test was performed at 130°C case temperature equivalent to Tjmax = 150°C (Class II).

b) Signal pin group passes +100 mA/-100 mA I-Test with I_{limit} of 200 mA for VDD_IO, which collapsed during positive injection.

c) Retest with higher I_{limit} signal pin group passes +75 mA/-100 mA I-Test with I_{limit} of 800 mA for VDD_IO.

d) There are two supply groups. Supply1 passes at 1.5 x V_{maxSUP}. Supply2 hits an I_{limit} of 500 mA. Raising the I_{limit} to 750 mA allows the supply to pass the stress.

e) Signal pins used as control pins were not tested due to product conditioning requirement.

f) Immunity Level B achieved.

Example #3 for reporting data with collapsing tester supply and reaching damage level when trying to increase I_{limit} to avoid supply collapse:

a) Test was performed at 125°C case temperature (Class II).

b) Signal pin group passes +100 mA/-100 mA I-Test with I_{limit} of 1200 mA for VDD_IO, which collapsed during positive injection. Further increasing I_{limit} caused damage.

c) Retest with lower I_{limit} signal pin group passes +80 mA/-100 mA I-Test with I_{limit} of 700 mA for VDD_IO.

d) Supply groups pass 1.5 x V_{maxSUP}.

e) Signal pins defined as clock pins were not tested due to product conditioning requirement.

f) Immunity Level B achieved.

Annex E (Informative) Determining MSV

The goal of the latch-up stress is to force a current or voltage, which could occur during normal use, and verify that parasitic structures are not forced into a regenerative, high current state. The role of MSV for the supply test is straightforward. It is not as obvious for the Signal Pin Test, especially when the test is performed as an I-Test. The significance of MSV is most evident when there is no diode between the PUT and either supply or ground. This Annex will offer methods to determine MSV for signal pins. These examples are not all encompassing, but do cover many, if not most, of the normal situations found in latch-up stressing. See Clause 2 for the definition of MSV pins.

Definitions used in this Annex:

Lower Statistical Limit (LSL) - Is the minimum acceptable limits of a device parameter.

Upper Statistical Limit (USL) - Is the maximum acceptable limits of a device parameter.

BV - Breakdown Voltage

- As used here, it is the threshold for non-latch-up induced failure.
- The beginning of catastrophic failure shown as the yellow failure probability curve in Figure 35.

MSV = $V_{maxOP} + \Delta V$

ΔV = (xx) * (LSL BV – V_{maxOP}) **xx** = fraction of difference to use, for example, 0.8 or 0.75.

Understanding where the MSV value falls within the spectrum of electrical stress on a device is shown in Figure 35. The MSV value will always be in a band of voltage that lies between AMR (Absolute Maximum Rating) or its synonym, (V_{ABSMAX}) and the breakdown voltage (BV). Generally, AMR is a value determined to be a voltage that is guardbanded from the voltage region that can cause catastrophic breakdown (BV). The guardband may be quite wide or very narrow depending on the process technology and its intended operation.

The goal of latch-up testing is to demonstrate the possibility of a latch-up risk. Many pins will have diodes to supply and ground making the stressing simple, as long as the value of the V_{limit} (MSV) is sufficient to turn-on the diodes and allow the pulse current to flow. Most of the difficulty in getting this stress to work occurs when there is no diode between the PUT and either supply or ground. It is necessary that the value of V_{limit} (MSV) be high enough to demonstrate that the part has been stressed to its maximum value but still not to a point of catastrophic damage.

Annex E (Informative) Determining MSV (cont'd)

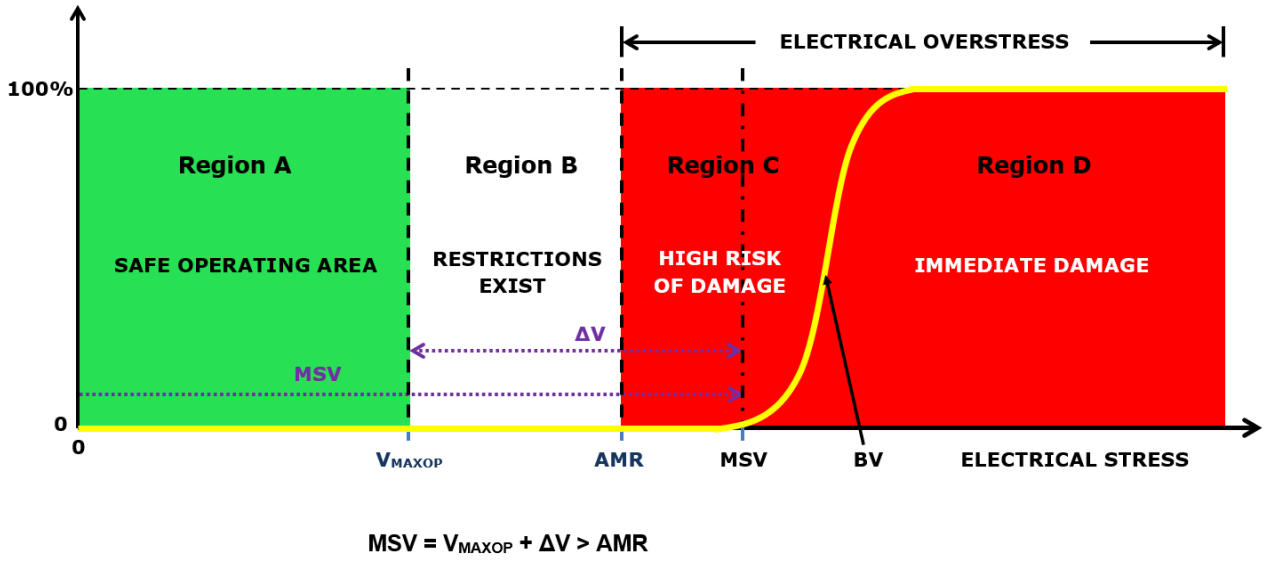


Figure 35 --- Electrical Stress Chart for Latch-Up Stress and MSV

Some methods to determine MSV that have been used are shown below.

Method #1 - Experimentally determine the optimum value using characterization data.

This method is normally used when one wants to maximize the MSV value and be as close as is practical to catastrophic device breakdown. It will require more experimentation. Taking a part with a pin set-up verified to represent, at least, one workable set-up. Depending on how extensive the experiment to find the MSV value, using a starting point in the range of catastrophic damage may give the best results. Starting at some point on the yellow curve in Figure 35, pick an MSV value and test 3 to 6 parts. If any fail, replace them and reduce the MSV until no parts fail. The MSV can then be said to be the highest level without failure.

Example 1: 5 V Technology

An important part of this technique is to establish a viable stress program. Generally, the stress program starts with an MSV at 8.25 V (1.5 x V_{maxOP}) but this setting creates damaged pin(s). Process characterization data indicate an LSL BV to be 8.1 V. Progressively reducing the MSV in 0.05 V steps from 8.25 V and stressing three parts at each voltage level, the level that had no failure was 8.0 V. This value is the MSV for the stress. It is possible that with this value that there is a small probability of a failure occurring during qualification testing.

Annex E (Informative) Determining MSV (cont'd)

Example 2: 40 V Technology

The LSL BV for this product is 42 V and the USL BV is 46 V. For this product, the starting point was selected to be 44 V. With a voltage window of a minimum of 2 volts, the step size was chosen to be 0.5 V. After the stress program was verified to work stably at a lower voltage (V_{maxOP}), the stepping began. The stress had 2/3 fail at 44 V, 43.5 V with 1/3 fail at 43V and 42.5 V. There were no failures at 42 V and the qualification testing was completed.

Method #2 - Using transistor or diode characterization data a variation of Method #1.

This is a less aggressive way to optimize the stress on the pin/part using technologies above 1.5V. The process characterization data are statistically distributed and are bounded by the highest BV (USL) and the lowest BV (LSL). As shown above in Method #1, there is a risk that even using a value 90% of the difference from (LSL BV – V_{maxOP}) may not be stable or dependable. Scaling back to a value approximately 80% (LSL BV – V_{maxOP}) may be less troublesome and time consuming. Setting these values may require someone with knowledge of the pin output/input architecture. There is also the possibility that ESD designers may have built snapback ESD protection structures in the zone, LSL BV-V_{maxOP}. It is important that these pins be adequately tested for latch-up, for stresses which could occur during normal operation. Discussions with ESD Designers should take place prior to finalizing MSV and latch-up stressing.

Example 1: 5V Technology

In most mainstream 5V technologies, the breakdown voltage (BV) of transistors is between 8.0 V and 9.5 V. Selecting the MSV, in this situation, can be in a range 70% -- 90% (LSL BV – V_{maxOP}). When applying the JESD78 1.5 X V_{maxOP}, the value would be 8.25 V. It may be OK if LSL BV is 9.5 V. If LSL BV is 8.1 V, then a safe MSV might be 7.3 V (70% LSL BV – V_{maxOP}).

One potential problem with picking a value above 7.0 V is the possibility that the ESD designer may have designed an ESD structure for the I/O's that triggers in that voltage range. If the submitter knows the I/O design and/or the Lab asks the question, this problem can be avoided.

Example 2: 16 V Technology

In technologies above about 10 V, the JESD78 rule (1.5 x V_{MAXOP}), does not work well. For this example, the 16 V is the nominal voltage and the V_{maxOP} is 18 V. If the JESD78 rule is applied, then the MSV is 27 V. The technology BV at LSL is 24 V. In this case, the MSV should be in the range of 22 V to 23 V. Either of these choices is workable with 22 V being more conservative since it gives some margin for error during stressing.

Annex E (Informative) Determining MSV (cont'd)

Example 3: ±15 V Technology

As with Example 2, this part has power supplies greater than 10 V. Both the positive and negative supplies have the same magnitude, ±15 V (V_{maxOP} & V_{minOP}) with a ground. This requires a set-up with MSV considerations. The supply will, with JESD78 requirements, be ±22.5 V, which is too high. The BV is, in either polarity, ±21 V. This MSV can be selected by using either a percentage of the difference between V_{maxOP} and BV or fixed value known to work in these types of technologies. The percentage could be 80% of the difference and MSV is 19.8 V. Using a fixed value (as described below) of 4 V yields an MSV of 19 V. Both should be low enough to prevent breakdown as long as temperature compensation is considered. Be aware, using the minimum voltage equation in Table 6 yields a value of -30 V for the negative MSV which is far too high in magnitude.

Method #3 - Using MSV values at a fixed voltage above V_{maxOP} and below V_{minOP}.

This method works well in more automated stress set-up environments. This is also dependent on voltage range. Silicon process technologies now range from ≤ 0.8 V to > 1000 V. When considering fixed values, the process technology needs to be considered. In the range from 2 V to 10 V, one might consider values enough greater than diode drop generally in the range of ±1.3 V to ±1.8 V to allow the full pulse current into the PUT. These values should not encroach into the region of breakdown. The same approach may work for higher voltages (> 10 V) where the adder can be larger; something in the range of 3 V to 5 V depending on the specific process.

Example 1: 5 V Technology

In the 5V technology, as described above in Method #1 Example 1, the JESD78 default may sometimes lead to an MSV that is too high. If one wants to simplify the stressing methodology for both the submitter and Lab personnel, a fixed value can be assigned by technology. In this case, an adder equal to 1.5 V will result in a value low enough to avoid a catastrophic breakdown and provide enough headroom to get the diode to turn on and stress current injected as expected.

Example 2: 36 V Technology

In a voltage range like this one with the V_{maxOP} at 40 V, the JESD78 default value for stress is 60 V. The technology LSL BV is 46 V. The JESD78 default is far too high to be used. Most technologies in this voltage range can tolerate up to 5 V over V_{maxOP}. Caution should be taken to understand the technology; there are some older high voltage processes that LSL BV is only 1 V to 3 V above V_{maxOP}.

Example 3: 5 V Technology (negative stress)

When doing negative stress, one wants to trigger the diode. This diode voltage can vary between -0.7 V to -1.3 V. Setting a common value for negative stress generally works well. The value making the most sense is V_{minOP} – 1.5 V. This method will work for most technologies from 1.2 V to 100 V. There may be exceptions to this rule, but it is a good starting point.

Annex E (Informative) Determining MSV (cont'd)

Method #4 - MSV for very low voltage products (< 1.3V)

This method, a variation of Method #1 & Method #3, is normally used when the MSV value using the standard JESD78 value for stressing (1.5 x V_{MAXOP}) is less than a diode voltage. In this situation during stress, the V_{limit} value (MSV) is too small to allow the pulse into a normal pin. The standard does not explicitly say to go higher than 1.5 x V_{maxOP} but if one has the headroom, Method #3 style experiments could be conducted to see if there is a safe MSV value at or above a diode voltage. The percentage of the 100 mA pulse current allowed into a PUT may not be 100%. The pulse current allowed could be a benchmark for other products in the technology. If any value, a diode voltage above the 1.5 x V_{maxOP}, causes catastrophic damage using a current pulse (I-Test), it may be reasonable to try a voltage pulse (E-Test) to understand the level of current allowed and if the pin can tolerate 1.5 x V_{maxOP}.

Example 1: 0.9 V Technology

A 0.9 V technology can be difficult to effectively stress. Using the JESD78 default (1.5xV_{maxOP}) with a 1.1 V (V_{maxOP}) is 1.65 V. The difference is less than a diode voltage. When tested with JESD78 default values there is very little current forced into the pins. There is no requirement that one needs to go over the JESD78 default. There is no requirement that one needs to go over the JESD78 default, however in this case, the LSL BV is 1.8 V and could be tested high enough to get a diode voltage to get an appropriate stress response. Using a version of Method #1 might give a feel for the margin the part might have in the field.

Example 2: 0.8 V Technology

A 0.8 V technology can be very difficult to effectively stress. Using the JESD78 default with a 1.0 V (V_{maxOP}) results in an MSV at 1.5 V. This MSV is at the LSL BV of the technology. If stressed at 1.5 V the part/pin has a possibility of catastrophic failure. Even without a failure there may not be a diode voltage triggered and therefore little stress current. Setting the MSV lower will not lead to an effective stress. If one ventured into the breakdown voltage area, non-catastrophic failure may or may not be latch-up. If thought to be latch-up, temperature variation might help resolve the failure type.

Method #5 - Using V_{ABSMAX} or V_{ABSMIN} for MSV

NOTE This method of determining MSV should be avoided.

Most V_{ABSMAX} / V_{ABSMIN} (AMR) values are normally less than a diode voltage above / below the V_{minOP} / V_{minOP}. Using V_{ABSMAX} / V_{ABSMIN} (AMR) will result in a "no current forced" into a pin scenario; this is not a latch-up stress test.

There may be those exceedingly rare exceptions in products where V_{maxOP} equals V_{ABSMAX} and possibly the LSL BV. In these scenarios, care should be taken with MSV and subsequent stressing. One may need to use Method #3 to determine what would work without causing catastrophic damage.

Breakdown Voltage (BV) less than 1 V above AMR should be proven with characterization data.

Annex F (Informative) Pulse Source Verification

F.1. Introduction

Understanding pulse source properties is important for proper latch-up testing. The latch-up trigger can be either a voltage pulse or a current pulse. Current pules are used for Signal Pin Tests when performed as an I-Test. Voltage pulses are used for the power supply overvoltage test, and for signal pins tests when performed as an E-Test. For Signal Pin Testing the choice between I-Test and E-Test is discussed in Clause 5.6 / Annex G.

For both voltage and current pulses, the pulse magnitude is specified by two parameters, the forced value and a limit, or compliance value. For a current pulse, the forced value is the intended current and the compliance value is the maximum voltage allowed. Compliance values prevent unintended damage to the device under test. For example, performing a 100 mA positive I-Test on an open drain buffer will create catastrophic damage due to excessive stress if performed without a voltage limit, because there is no forward bias diode current path to carry the current. For a voltage pulse, the forced value is the intended voltage and the compliance value is the maximum current allowed.

It is important to be able to verify properties of the pulse sources to ensure meaningful latch-up test results. Since latch-up stress conditions can vary widely, it is important to verify pulse properties under conditions appropriate for the devices to be latch-up tested. Pulse properties shall be evaluated both when the forced value, voltage or current is actually reached during the pulse, and when the compliance value is exceeded before the force value is reached.

The parameters to compare the measured waveforms against are in Table 5 and in the timing diagrams, Figure 3 to Figure 8. Parameters to verify are pulse height, rise time for positive pulses, fall times for negative pulses, pulse duration and any overshoot magnitudes. Pulse parameters should be determined under conditions where the forced value can be obtained and under conditions where the limit value is reached.

Latch-up trigger pulses are a series of several steps, as shown in the timing diagrams in Figures 3 through 8. The sequence starts by transitioning to a pre-trigger state, time period T_0 to T_2 in the timing diagrams. After all test voltages stabilize and pre trigger currents are measured the pulse transitions to the trigger state, time period T_3 to T_4 in the timing diagrams. After the specified trigger duration, the pulse source transitions to the post-trigger state, time period T_5 to T_7. The pre-trigger and post-trigger voltage and current conditions are often called the “Parking” conditions. The pulse settings during the pre and post trigger periods can affect the pulse properties during the transition to the trigger period and during the trigger period. For example, the maximum allowed current during the pre or post trigger periods will determine pulse source range as much as the maximum allowed current during the actual trigger period. It is therefore important to carefully chose pre and post trigger values that match the values which will be used during actual latch-up testing when doing pulse verification measurements.

F.2. Verification Test Setup

The verification test setup is shown in Figure 36. The voltage measurement is shown as two voltage probes using two channels of the oscilloscope, to measure the voltage differential across the loads. A true differential probe and a single oscilloscope channel can also be used instead. If it can be shown that the voltage on the low side of the Load is sufficiently close to ground potential, a single voltage probe can be used. If the Load is a linear resistance, as will be discussed below, the current probe can be eliminated and the current can simply be calculated from the voltage measurement. For best results, the Load should be mounted in the latch-up test setup in as similar a manner to a standard device under test as possible.

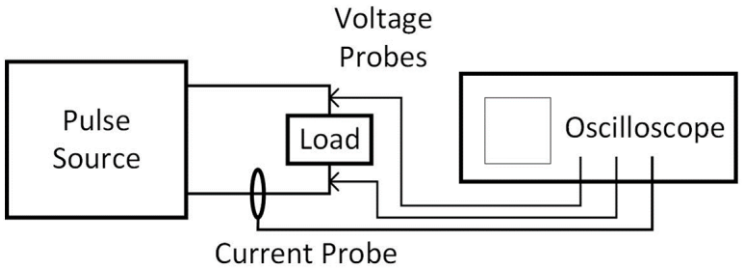


Figure 36 --- Verification Test Set-up

The measurement instruments should be chosen to be appropriate for the measurements to be made. Latch-up voltage stress can vary from about 1 V to over 100 V, and currents can vary from several mA to several hundred mA. Latch-up trigger pulses are of relatively long duration. Current probes should therefore have a bandwidth that extends from DC to at least 10 MHz. All measurement instruments should be calibrated yearly or according to organization quality standards.

F.3. Standard Pulse Source Verification

Standard pulse source verification should be done with resistive loads. The resistive loads can be discrete resistors, with power ratings that will not change value significantly during the pulse for the intended current/voltage ranges, or an electronic load in constant resistance mode.

Basic functionality should be checked, with the pulse sources not in compliance. For current pulses, a low value resistor should be used; for example, in the one to several ohm range. For voltage pulses, a high value resistor should be used; for example, in the 1000 to 10,000 ohm range. These tests do not, however, give good guidance of pulse source behavior during true latch-up testing.

More meaningful verification results can be obtained by selecting the load resistance value to match device properties to be measured. As discussed above, latch-up test currents range from a few mA to 100's of mA and voltages range from 1 V to over 100 V. 100 mA is the most common test current for signal pins. The pairing of stress current level and voltage depends strongly on the product and technology being tested. High performance logic integrated circuits in advanced technologies require current levels in the 10's of mA at voltage levels of just a few volts. High voltage analog products require testing in the 10's of mA to several hundred mA, but at voltages which can exceed 100 V. To properly mimic the behavior of a device under test the load resistor value should be chosen carefully.

F.4. I-Test

Forcing current, with a voltage limit is used for I-Test of signal pins and the resistor choice for I-Test will be covered first.

Table 9 gives samples of the choice of resistor values for a positive I-Test for a variety of technologies, based on the standard operating voltage for the technology or product. The first two columns of the table give the nominal technology voltage, as well as the V_{maxOP} for the technology. Both are datasheet values. The development of the table will be explained using a 5 V technology as an example. In I-Test a specified current is injected, often 100 mA but different values may be chosen for some technologies. Column 3 shows some typical values. During positive I-Test of a signal pin; the pulse source needs to provide a voltage in excess of the diode drop above the power supply voltage. This determines the expected voltage value for the stress pulse, shown in Column 4. From the intended stress current and expected stress voltage a resistor value, which will mimic product impedance during latch-up test, can be calculated. If the power supply voltage is set at 5.5 V during the latch-up test and the I-Test stress current is set at 100 mA, this current can be expected at approximately 6.7 V, or a few tenths of a volt above a diode drop over the power supply voltage. To mimic this device under test impedance a 67-ohm resistor can be chosen (6.7 V / 0.1 A). This value can be used to verify pulse properties when the pulse source is not in compliance. Sample test resistor values are given in Column 5.

To prevent damage if the intended current cannot be made to flow, a voltage limit is set. For positive stress this can be 1.5 x V_{maxOP}, or MSV if there are technology limitations. Sample values are shown in Column 6.

To verify pulse source properties when the source is in compliance, the resistor value shall be increased so that the intended stress current will not be reached during pulse verification. To ensure that the in-compliance test is well beyond the compliance limit, the resistance for the in-compliance test can be doubled. Samples are shown in Column 7.

F.4 I-Test (cont'd)

Table 9 --- Samples of Verification Resistor Values for Positive I-Test Pulse Verification for Different Technologies Being Tested

Technology Voltage[1] (V)	V_{maxOP}[2] (V)	Intended Stress Current[3] (mA)	Expected Voltage at Injected Current[4] (V)	Test Resistance (Not Voltage Limited)[5] (Ω)	Voltage Limit[6] (V)	Test Resistance (Voltage Limited)[7] (Ω)
1.5	1.65	50	2.85	57	3*	114
3.3	3.6	100	4.8	48	5.4†	96
5	5.5	100	6.7	67	8.25†	134
20	22	50	24	480	28*	960
90	95	100	99	990	100*	1980

1) Nominal power supply voltage from datasheet.

2) Maximum of recommended power supply range from datasheet.

3) Intended I-Test stress current.

4) Voltage at which the intended stress current can be expected assuming a diode to the power supply. This will be V_{MAX}, plus a diode drop, plus several tenths of a volt. Diodes in high voltage technologies have lower doping levels and therefore have higher series resistors. Driving the intended stress current may require a diode drop plus 2 or more volts above the V_{MAX}.

5) The resistance value to use to verify pulse performance for I-Test when not in voltage compliance. This value is obtained by dividing the voltage in Column 4 by the current in Column 3.

6) The voltage compliance value to be used during I-Test. For medium voltage technologies, this can be 1.5 x V_{maxOP}. For very low voltage technologies this can be V_{maxOP}, plus a diode drop, plus several tenths of a volt so that current can be successfully injected. For both very low and high voltage technologies this is often MSV. (* Determined by MSV, † Determined by 1.5 x V_{maxOP}.).

7) The resistance value to use to check pulse properties with the pulse source in voltage compliance. The resistance can be chosen by doubling the value in Column 5.

For negative I-Test, in most technologies, there is a diode to VSS or similar ground power pin. For these technologies, reaching a voltage compliance with a negative I-Test is seldom an issue.

F.4 I-Test (cont'd)

Sample values for testing non-compliance pulse shapes are shown in Table 10. If verification of in compliance pulse shapes are needed, appropriate resistance can be calculated as done for Table 9.

Table 10 --- Samples of Verification Resistor Values for Negative I-Test Pulse Verification for Different Technologies Being Tested

Technology Voltage[1] (V)	V_{maxOP}[2] (V)	-0.5 x V_{maxOP}[3] (V)	Intended Stress Current[4] (mA)	Expected Voltage at Injected Current[5] (V)	Suggested Voltage Limit During Negative Stress[6] (V)	Test Resistance (Not Voltage Limited)[7] (Ω)
1.5	1.65	-0.825	50	-1.1	-1.5	22
3.3	3.6	-1.65	100	-1.2	-1.65	12
5	5.5	-2.75	100	-1.2	-2.75	12
20	22	-11	50	-1.1	-3	22
90	95	-47.5	100	-1.2	-3	12

NOTE All Values Assume a Diode to Substrate.

1) Nominal power supply voltage from datasheet.

2) Maximum of recommended power supply range from datasheet.

3) -0.5 x V_{maxOP} is the traditional negative current limit for negative I-Test. For low V_{maxOP} this value is often insufficient to inject significant current for a viable latch-up test.

4) Intended I-Test stress current.

5) Voltage at which the intended stress current can be expected. This will usually be a negative diode drop, minus several tenths of a volt.

6) Suggested voltage limits during pulse verification. For medium voltage technologies this can be the traditional -0.5 x V_{maxOP}. For the lowest voltage technologies -0.5 x V_{maxOP} will not be sufficient to adequately forward bias the signal pin to V_{SS} diode, and a larger value is used. For high voltage technologies -0.5 x V_{maxOP} is too high a value and a more realistic value should be chosen, but still large enough to inject negative current into the signal pin.

7) The resistance value to use to verify pulse performance for I-Test when not in voltage compliance. This value is obtained by dividing the voltage in Column 5 by the current in Column 4.

F.5. E-Test and Supply Test

Forcing voltage, with a current limit, is used for E-Test of signal pins and for Supply Test (formerly power supply overvoltage test). The choice of test resistor will focus on E-Test of signal pins. The resistor values to verify pulse source performance during E-Test should be an adequate verification for pulse sources used for the overvoltage test of power supplies.

Since latch-up is current driven, the goal of E-Test is to actually force a current into signal pins, even though the pulse source is being used in force voltage mode. The difference is that the current that is intended to be driven is entered as a current limit, rather than a forced value.

Table 11 gives examples of choosing appropriate test resistors for a variety of technologies for positive E-Test. Column 1 and Column 2 give the devices nominal voltage and the maximum recommended operating voltage. Both are datasheet values. The next column is the intended forced current, but for E-Test is the current limit for the pulse source. Assuming that there is a diode to the power supply on signal pins the current should be injected at a diode drop plus several tenths of a volt about the V_{maxOP} value. These values are given in Column 4. The suitable test resistor value can be calculated from the expected voltage and the intended injection current. Sample resistor values are given in Column 5 of Table 11.

The actual voltage to force during E-Test depends on the technology. At medium voltages such as 3.3 V and 5 V it is often possible to use the traditional value of 1.5 x V_{maxOP}. For very low voltage technologies this will not be enough to exceed a diode drop above the power supply voltage, so a slightly higher value will be needed. The value should not exceed the MSV value. For high voltage technologies 1.5 x V_{maxOP} is often well beyond what the technology can sustain without causing damage.

F.5 E-Test and Supply Test (cont'd)

In these cases, the MSV value should be used. Sample values for the forced voltage are shown in Column 6 of Table 11. To test pulse source properties when the current limit value is not exceeded the resistor value for current limited testing can simply be doubled and is shown in Column 7.

Note that the values in Table 11 are the same as the values in Table 9, only the column headings have been changed.

Table 11 --- Samples of Verification Resistor Values for Positive E-Test Pulse Verification for Different Technologies Being Tested

Technology Voltage[1] (V)	V_{maxOP}[2] (V)	Intended Stress Current (Current Limit)[3] (mA)	Expected Voltage at Injected Current[4] (V)	Test Resistance (Current Limited)[5] (Ω)	Forced Voltage[6] (V)	Test Resistance (Not Current Limited)[7] (Ω)
1.5	1.65	50	2.85	55	3*	110
3.3	3.6	100	4.8	46	5.4†	92
5	5.5	100	6.7	65	8.25†	130
20	22	50	24	440	28*	880
90	95	100	99	990	100*	1980

1) Technology voltage from datasheet.

2) Maximum recommended power supply voltage from datasheet.

3) Intended stress current, which for E-Test is the pulse source compliance limit.

4) Voltage at which the intended stress current could be expected assuming a diode to power supply. This value is usually V_{maxOP}, plus a diode drop, plus several tenths of a volt.

5) Resistance to test pulse properties in compliance. This value is obtained by dividing the voltage in Column 4 by the current in Column 3.

6) This is the voltage to force during the test for pulse properties for E-Test. (***** Determined by MSV, † Determined by 1.5 x V_{maxOP}.).

7) Resistance to test pulse properties not in compliance. This value is obtained by doubling the values in Column 5.

For negative E-Test of signal pins, similar factors are considered as for negative I-Test.

F.5 E-Test and Supply Test (cont'd)

Table 12 --- Samples of Verification Resistor Values for Negative E-Test Pulse Verification for Different Technologies Being Tested

Technology Voltage[1] (V)	V_{maxOP}[2] (V)	-0.5 x V_{maxOP}[3] (V)	Intended Stress Current (Current Limit)[4] (mA)	Expected Voltage at Injected Current[5] (V)	Suggested Forcing Voltage During Negative Stress[6] (V)	Test Resistance (Not Voltage Limited)[7] (Ω)
1.5	1.65	-0.825	50	-1.1	-1.5	22
3.3	3.6	-1.65	100	-1.2	-1.65	12
5	5.5	-2.75	100	-1.2	-2.75	12
20	22	-11	50	-1.1	-3	22
90	95	-47.5	100	-1.2	-3	12

NOTE All values assume a diode to substrate

1) Nominal power supply voltage from datasheet.

2) Maximum of recommended power supply range from datasheet.

3) -0.5 x V_{maxOP} is the traditional negative current limit for negative I-Test. For low V_{maxOP} this value is often insufficient to inject significant current for a viable latch-up test.

4) Intended stress current, which for E-Test is the pulse source compliance limit.

5) Voltage at which the intended stress current could be expected assuming a diode to power supply. This value is usually V_{maxOP}, plus a diode drop, plus several tenths of a volt.

6) Suggested voltage limits during pulse verification. For medium voltage technologies this can be the traditional -0.5 x V_{maxOP}. For the lowest voltage technologies -0.5 x V_{maxOP} will not be sufficient to adequately forward bias the signal pin to V_{SS} diode, and a larger value is used. For high voltage technologies -0.5 x V_{maxOP} is too high a value and a more realistic value should be chosen, but still large enough to inject negative current into the signal pin.

7) The resistance value to use to verify pulse performance for I-Test when not in voltage compliance. This value is obtained by dividing the voltage in Column 5 by the current in Column 4.

F.6. Specialized Pulse Source Verification

In some situations, especially when there is an unusual latch-up failure, it may be desirable to evaluate pulse source properties with loads other than a resistor. In most cases the test load of interest would be a Zener diode, with a breakdown voltage similar to the voltage at which the device in question would experience a forward diode situation. Care should be taken to ensure that the diode chosen for pulse source verification can handle the intended current at the Zener breakdown voltage. When using a load other than a linear resistor, it is necessary to measure both voltage across the load and current through the load. For negative injection verification, when a diode to VSS is expected, either a standard diode or a Zener diode can be used.

F.7. Sample Pulse Measurements

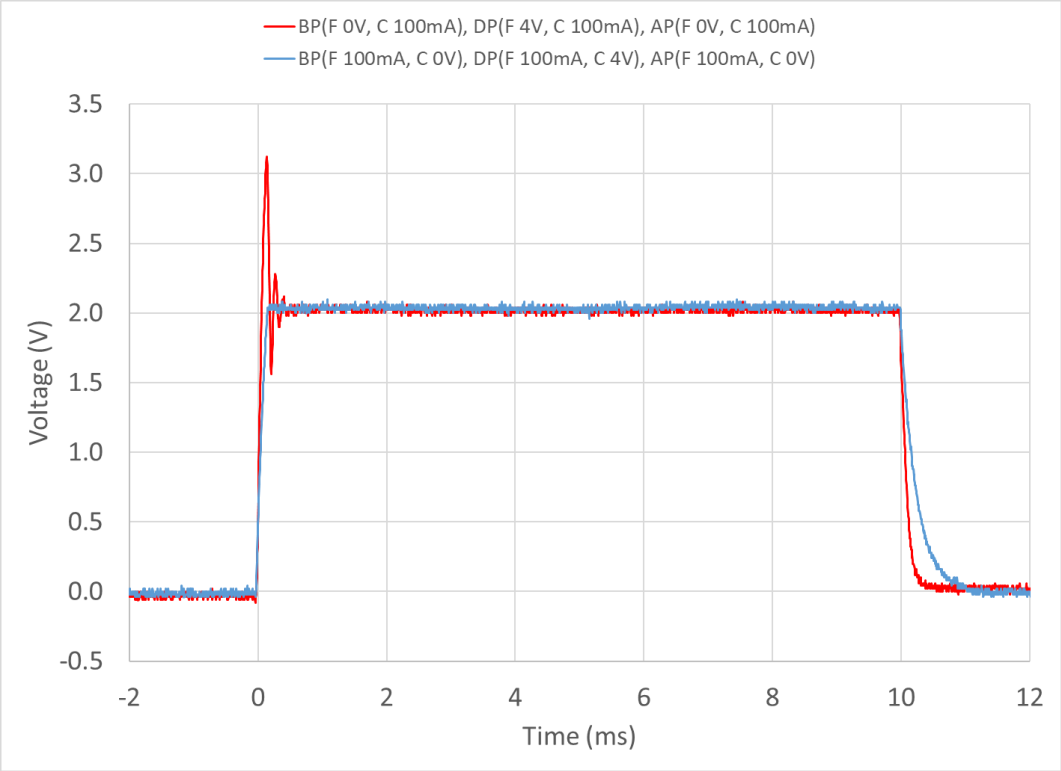
The most obvious waveform parameter to observe when capturing latch-up stress waveforms is the plateau value, after any initial transients, to verify accuracy of the pulse magnitude. Transients on both the rising and falling edges of a pulse can also be important and cause false failures.

The following example illustrates the type of anomalies which can be uncovered by capturing a pulse using the measurement technique described in this Annex. The intent is to force 100 mA through a 20 ohm resistor for 10 ms, with no current before and after the pulse. Two methods will be used, one forcing voltage with a current compliance, and one forcing current with a voltage compliance. It is important to describe not just the pulse source conditions during the pulse, but also before and after the pulse.

- Forcing Voltage
  - Before Pulse: Force 0 V with 100 mA compliance.
  - During Pulse: Force 4 V with 100 mA compliance.
  - After Pulse: Force 0 V with 100 mA compliance.
- Forcing Current
  - Before Pulse: Force 100 mA with 0 V compliance.
  - During Pulse: Force 100 mA with 4 V compliance.
  - After Pulse: Force 100 mA with 0 V compliance.

The results of the measurements are shown in Figure 37. It is clear for the case of forcing voltage and allowing the current compliance during the pulse to limit the current produces considerable voltage overshoot and ringing on the rising edge of the pulse. In the case of forcing current, using voltage compliance before and after the pulse to limit the current results in a better-behaved waveform.

F.7 Sample Pulse Measurements (cont'd)



NOTE The legend describes the pulse supply's force (F) and compliance (C) values before the pulse (BP), during the pulse (DP) and after pulse (AP).

Figure 37 --- Comparison of 2 Pulses Intended to Create a 100-mA Pulse Through a 20 Ohm Resistor

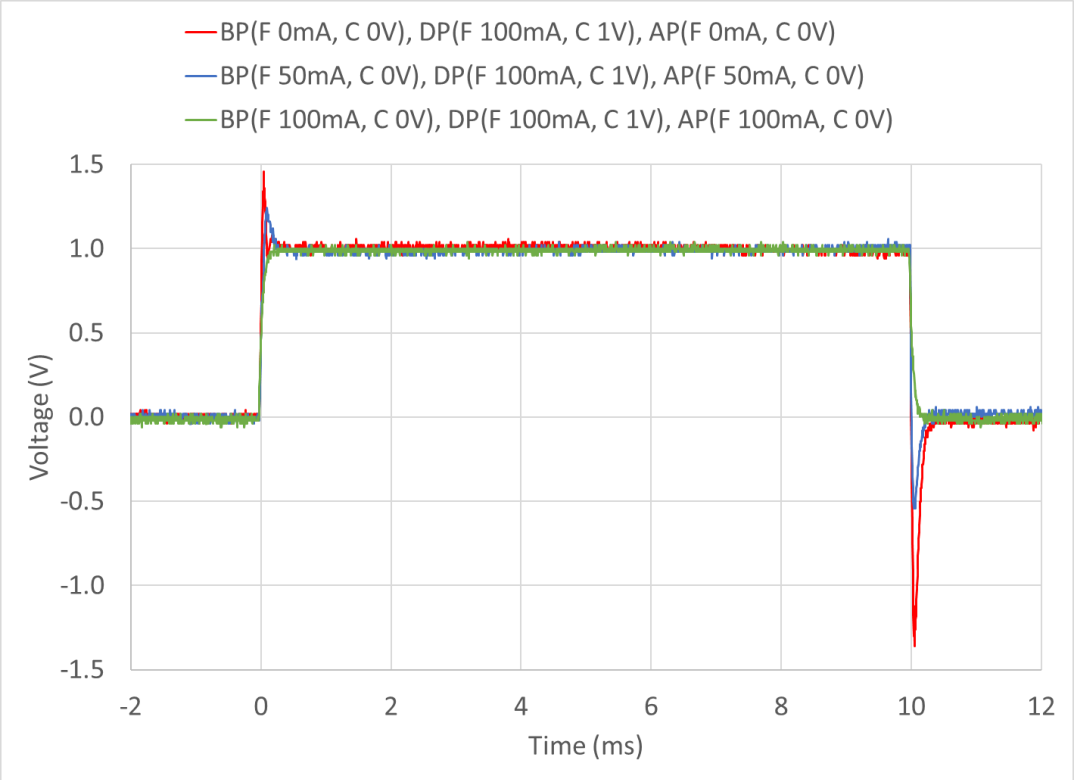
A second example shows how the pulse source conditions before and after the pulse can have serious consequences on the quality of the pulse. All three of the following pulses are intended to try to force 100 mA into a 1 kΩ resistor, but with a 1 V compliance limit. All three pulses will be voltage limited.

- Case 1
  - Before Pulse: Force 0 mA, with 0 V compliance
  - During Pulse: Force 100 mA, with 1 V compliance
  - After Pulse: Force 0 mA, with 0 V compliance
- Case 2
  - Before Pulse: Force 50 mA, with 0 V compliance
  - During Pulse: Force 100 mA, with 1 V compliance
  - After Pulse: Force 50 mA, with 0 V compliance
- Case 3
  - Before Pulse: Force 100 mA, with 0 V compliance
  - During Pulse: Force 100 mA, with 1 V compliance
  - After Pulse: Force 100 mA, with 0 V compliance

F.7 Sample Pulse Measurements (cont'd)

The results are shown in NOTE The legend describes the pulse supply's force (F) and compliance (C) values before the pulse (BP), during the pulse (DP) and after pulse (AP).

Figure 38. In each case the conditions during the pulse are the same, forcing 100 mA with a compliance voltage of 1 V. The only difference between the three cases is that the forced current before and after the pulse are different. The cases in which the before and after forced currents are 0 mA and 50 mA produce overshoot on the rising edge, and even more undershoot on the falling edge. Either of these anomalies could produce false latch-up failures. In the case in which the forced current before and after the pulse is the same as that forced during the pulse, the pulse was well behaved.



NOTE The legend describes the pulse supply's force (F) and compliance (C) values before the pulse (BP), during the pulse (DP) and after pulse (AP).

Figure 38 --- Comparison of 3 Pulses Intended to Create a 100-mA Pulse Through a 1 kΩ Resistor

Annex G (Informative) Signal Pin Test – I-Test vs E-Test – How to Decide Which is Best

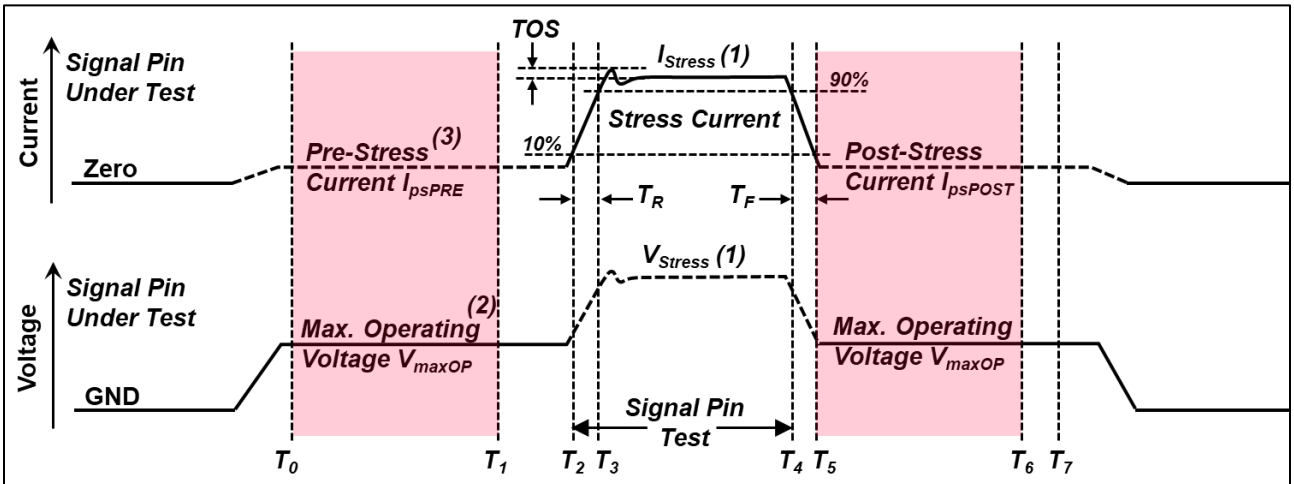
Revision F of JESD78 is the first revision to allow the use of both I-Test and E-Test to complete stressing on signal pins. E-Test is a Signal Pin Test that was originally used as an alternative stress in the Automotive Electronics Council (AEC) Q100 Standard. E-Test has gradually been adopted in a limited fashion for conditions that I-Test could not stress effectively. I-Test has been the workhorse for Latch-up testing.

Situations where E-Test has been shown to be effective are shown below. This is not an all-inclusive list but is a compendium from industry latch-up testing experts.

- **Controlled V Ramp:** In many latch-up testing situations it is necessary to control the slew rate supplied to the pin under test. Some test equipment / pulse supplies cannot control the ramp rate when in current mode but can control the ramp rate when in voltage mode. If the product pin(s) is sensitive to slew rate, E-Test could be the best solution.
- **High Impedance Inputs:** Many devices have inputs that are designed in such a way that static latch-up stress sees a high impedance. This pin condition could be inherent to the pin or a preferred condition for stressing. If I-Test is used for these types of pins, the pulse source tries to force 100 mA, but the voltage limit is reached. The current forced into the pin is normally small, on the order of 1 – 10 mA. Sometimes if MSV is set too high, the pin may be damaged. Using E-Test may give a more accurate and controllable forcing of the maximum current which can be sustained at 1.5 x V_{maxOP} or MSV. The pulse current value reached with E-Test is likely a more realistic value of what is forced. The current forced is likely not 100 mA but the maximum possible current given the pin design characteristics.
- **Low Voltage Products:** In many of the latest technology products with power supply voltages at or below 1.3 V, there can be concerns with the ability to get to a diode voltage that is less than the breakdown voltage even using 1.5 x V_{maxOP}. I-Test in this situation is workable but very little current is injected with the possibility of uncontrolled rise time of the current pulse and possible overshoots. Using E-Test can give a look at the pulse current allowed 1.5 x V_{maxOP} or MSV. While there is no requirement to exceed 1.5 x V_{maxOP} during qualification, good engineering practice would be to try MSV values higher than 1.5 x V_{maxOP} to see if a diode is turned-on and see if the pin does not latch-up.
- **Bipolar Inputs / Outputs:** E-Test was shown to be effective when a device has bipolar inputs and/or outputs. The inputs can be emitters. When these pins are pulsed with current, they can amplify the current or burn out the emitter-base junction. Outputs with open collectors can sometimes be sensitive to pulse currents (I-Test), even with a reasonable MSV, can create a catastrophic failure. It is more effective to try an E-Test and measure the current. Even using E-Test can create the possibility of catastrophic failure, so, care should be taken with the pulse current clamp, I_{psPRE} and I_{psPOST} settings. I-Test can be used but care should be taken not to create catastrophic failures.

Annex H (Informative) Controlling Pin Under Test During Pre- and Post-Stress

Normally, the signal pin under test is simply used as an injection point to determine if latch-up can be triggered when the signal pin under test experiences a transient. There are other situations however, where the signal pin under test can also be part of the parasitic thyristor or SCR contained within the I/O structure or in combination with an adjacent I/O structure. In this scenario, it is important to carefully consider the pre and post stress conditions of the signal pin under test, so as to not artificially limit the current during the pre and post stress regions which may mask a potential latch-up problem. This is called Signal Pin Test applying to signal pins to ground, signal pins to power supply or pin to pin latch-up.



(1) The waveforms when shown in a solid line are the forced voltages or currents and when shown with dashed lines are the measured voltages or currents.

(2) During I-Test, E-Test or Supply Test, the supply currents for all supply groups are monitored for latch-up occurrence. Failure occurs if any supply current exceeds the limit shown in Table 3. In addition, power supply voltages shall not collapse during the stress as per Clause 5.5.2.

(3) The pre-stress and post-stress current I_{psPRE} and I_{psPOST} depend on the state and the circuitry of the PUT.

Figure 39 –- Pre-Stress and Post-Stress Current and Voltage Control

Looking at the latch-up testing waveform for positive pin stress shown in Figure 39, there are three regions of interest, pre-stress, stress, and post-stress. In the stress region shown, a current (voltage) is forced into the signal pin under test, and the resultant voltage (current) is also measured. In the pre-stress and post-stress regions the maximum operating voltage (V_{maxOP}) is applied to the signal pin under test, and there is also a current value (I_{psPRE} & I_{psPOST}) associated with the supply used to drive the pin. This current value is often called the parking current, a term used on one series of testers. If the current value is too low, it may mask a potential latch-up event within the pin or between the pin and an adjacent pin.

Consider the scenario where the maximum operating voltage is applied to the signal pin under test resulting in a low-level leakage current. Next, the stress pulse is applied which triggers an SCR between the signal pin under test and system ground. Further, the SCR current also causes other parasitic devices to conduct, resulting in current flow from the power supply to ground.

Annex H (Informative) Controlling Pin Under Test During Pre- and Post-Stress (cont'd)

After the pulse is removed, the pin is returned to the maximum operating voltage (V_{maxOP}) with a current value below the level needed to sustain the latch-up event. In this scenario, the current value (I_{psPOST}) will cause the SCR to turn off and a possible latch-up event will be missed. It is important to keep in mind that this scenario is only possible in a real-world application if the signal pin can be connected to low impedance source, capable of sustaining the latch-up. The above situation can occur for either positive or negative I-Test or E-Test. In Summary, when testing a signal pin that can be connected to a low impedance source, it is important that the current value on the supplies used to drive the pin to the maximum operating voltage be high enough to allow a potential latch-up event to be detected, and not result in limiting the voltage during the post-stress phase of the test to a level below the maximum operating voltage.

Example 1(a): Positive I-Test (+100 mA) with SCR between PUT and VSS

Table 13 --- Example 1(a) Pre-Stress Conditions

Pin or Pin Group	Voltage or Current Source	Voltage Limit	Actual Voltage	Current Limit	Actual Current	Comment
VDDIO	Voltage Source	3.6 V	3.6 V	500 mA	10 mA	$I_{supply1}$
Signal Pins not under stress	Voltage Source	3.6 V	3.6 V	100 mA	1 mA	$I_{supply2}$
PUT	Current Source	3.6 V	3.6 V	80 mA(1)	45 pA	I_{psPRE}
VSS	Voltage	0 V	0 V	unlimited	11 mA	typically, not measured

Table 14 --- Example 1(a) Post-Stress Conditions

Pin or Pin Group	Voltage or Current Source	Voltage Limit	Actual Voltage	Current Limit	Actual Current	Comment
VDDIO	Voltage Source	3.6 V	3.6 V	500 mA	10 mA	$I_{supply1}$
Signal Pins not under stress	Voltage Source	3.6 V	3.6 V	100 mA	1 mA	$I_{supply2}$
PUT	Current Source	3.6 V	3.6 V	80 mA(1)	**50 mA**	I_{psPOST}
VSS	Voltage	0 V	0 V	unlimited	**61 mA**	typically, not measured

Annex H (Informative) Controlling Pin Under Test During Pre- and Post-Stress (cont'd)

Example 1(b): Positive I-Test (+100 mA) with SCR between PUT and VSS

Table 15 --- Example 1(b) Pre-Stress Conditions

Pin or Pin Group	Voltage or Current Source	Voltage Limit	Actual Voltage	Current Limit	Actual Current	Comment
VDDIO	Voltage Source	3.6 V	3.6 V	500 mA	10 mA	$I_{supply1}$
Signal Pins not under stress	Voltage Source	3.6 V	3.6 V	100 mA	1 mA	$I_{supply2}$
PUT	Current Source	3.6 V	3.6 V	40 mA(1)	45 pA	I_{psPRE}
VSS	Voltage	0 V	0 V	unlimited	11 mA	typically, not measured

Table 16 --- Example 1(b) Post-Stress Conditions

Pin or Pin Group	Voltage or Current Source	Voltage Limit	Actual Voltage	Current Limit	Actual Current	Comment
VDDIO	Voltage Source	3.6 V	3.6 V	500 mA	10 mA	$I_{supply1}$
Signal Pins not under stress	Voltage Source	3.6 V	3.6 V	100 mA	1 mA	$I_{supply2}$
PUT	Current Source	3.6 V	2.9 V	40 mA(1)	40 mA	I_{psPOST} reaching current limit setting
VSS	Voltage	0 V	0 V	unlimited	51 mA	typically, not measured

Example 1 interpretation: The increased PUT post-stress current (I_{psPOST}) as compared to the pre-stress current (I_{psPRE}) indicates a sustained latch-up event on the PUT. In addition, the actual voltage reading of the PUT current source dropped, indicating supply droop. JESD78E would not have flagged this as a latch-up failure because the I_{supply} values do not increase (see Clause 4.2.1.4 and Table 2). This would be flagged as a failure per this version.

Annex H (Informative) Controlling Pin Under Test During Pre- and Post-Stress (cont'd)

Example 2: Negative I-Test (-100 mA) with SCR between PUT and another signal pin not under stress

Table 17 --- Example 2 Pre-Stress Conditions

Pin or Pin Group	Voltage or Current Source	Voltage Limit	Actual Voltage	Current Limit	Actual Current	Comment
VDDIO	Voltage Source	3.6 V	3.6 V	500 mA	10 mA	$I_{supply1}$
Signal Pins not under Stress	Voltage Source	3.6 V	3.6 V	100 mA	1 mA	$I_{supply2}$
PUT	Current Source	0 V	0 V	80 mA(1)	-1 µA	I_{psPRE}
VSS	Voltage	0 V	0 V	unlimited	11 mA	typically, not measured

Table 18 --- Example 2 Post-Stress Conditions

Pin or Pin Group	Voltage or Current Source	Voltage Limit	Actual Voltage	Current Limit	Actual Current	Comment
VDDIO	Voltage Source	3.6 V	3.6 V	500 mA	10 mA	$I_{supply1}$
Signal Pins not under Stress	Voltage Source	3.6 V	3.6 V	100 mA	**51 mA**	$I_{supply2}$
PUT	Current Source	0 V	0 V	80 mA(1)	**-50 mA**	I_{psPOST}
VSS	Voltage	0 V	0 V	unlimited	11 mA	typically, not measured

(1) If the PUT current value were set to a value that is lower than the holding current of the SCR (for example, in the microamp range), the latch-up event may not be sustained beyond the duration of the stress pulse, and the post-stress conditions would look identical to the pre-stress conditions. If it is desired to detect signal pin latch-up, the PUT force current during pre and post stress regions (also known as, "parking current") should be set to a value in the same range as the stress current (for example, 100 mA).

Example 2 Interpretation: JESD78E would consider this as a latch-up failure because the $I_{supply2}$ value increases beyond the limit set by the failure criteria (Table 2.).

Annex I (Informative) Differences Between JESD78F.01 and its Predecessors

Differences between JESD78F.01 and JESD78F (January 2022)

Clause	Description of change
1	Made clarifying wording change in second paragraph.
2	Made clarifying wording change in MSV definition.
5	Added clarifying note to Clause 5.1
5	Fixed several formatting errors in Figure 2
5	Added clarifying note to Figure 3
5	Added clarifying note to Figure 4
5	Added clarifying note to Figure 5
5	Added clarifying note to Figure 6
5	Added clarifying note to Figure 8
5	Changed title of Table 5
5	Removed voltage reference in TOS clause of Table 5
5	Added clarifications to footnote 1 of Table 5
5	Added clarifying note to Table 5 footnote 2
5	Removed four boxes from flowchart in Figure 7 that did not pertain
6	Fixed typographical error in tenth bullet; “Class I” to “Class II”
Annex F	Fixed typographical error in paragraph describing Figure 38; “a compliance voltage of 0 V” to “a compliance voltage of 1 V”

Differences between JESD78F and JESD78E (April 2016)

Clause	Description of change
Foreword	New. Added to explain overall purpose of JESD78F resulting from the extensive re-write of JESD78E
1	Re-organized with numerous revisions. Moves Classification to later clauses.
2	Several additions, revisions. Examples include dynamic pin in place of dynamic devices, E-Test, EIPD, and several others.
3	New - replaces Clause 3 of JESD78E on Apparatus and material. Includes Table 1 (previously in Clause 1). Table 1 revised. Includes clause on Temperature Classification and Overall requirements
4	Previous Clause 3 is moved to clause 4 with major changes. Changes include clauses on Hardware requirements & capabilities, Test board, and renaming of Heat source clause to Temperature Control.
5	New clause title replacing previous Clause 4 of JESD78E. Extensive re-write with changes to tables, figures (for example Table 1, Table 2). Several new clauses, too numerous to list.
6	Clause re-titled from Summary to Report Requirements. Numerous changes.
Annex A	New Title. Extensive and exhaustive re-write with major additions.
Annex B	New Title. Extensive re-write with major additions.
Annex C	New clause with new title. Clauses and figures on Equivalent Circuits moved to this clause. Revisions to figures
Annex D	New. Examples added.
Annex E	New. Extensive discussion and exhaustive explanation of MSV

Differences between JESD78F and JESD78E (April 2016) (cont'd)

Annex F	New. Extensive discussion and exhaustive explanation on Pulse Source Verification.
Annex G	New. Provides guidance on appropriate test for Signal Pins.
Annex H	New. Provides guidance on control of Pin states for pre and post stress conditions.
Annex I	New. Replaces Annex D of JESD78E

Differences between JESD78E and JESD78D

Clause	Description of change
Table 1	Reduced number of groups in Column 2; Added Column 4 for Immunity Level
2	cool –down time: replaced Figure 4 with Figure 6
2	maximum stress voltage (MSV): Revised text.
2	NOTE 1: Revised text.
2	NOTE 2: Revised text.
2	Vsupply pin (or pin group): Revised text.
Figure 1	Revised figure
4.1	Moved Table 3 of JESD78D to later clause.
4.2	Added 4.2.1 to explain consideration of supply current limits
Figure 2	Revised timing diagram and text.
Figure 3	Revised timing diagram and text
Table 3	Table 3 of JESD78D revised with new limits and moved to 4.2.2
Figure 4	Figure 5 of JESD78D revised. Moved to clause preceding 4.2.2.
Figure 5	Figure 6 of JESD78D revised. Moved to clause preceding 4.2.2
Figure 6	Figure 4 of JESD78D. Revised.
Table 4	New table for Vsupply overvoltage level.
Figure 7	Revised and moved to 4.2.5
4.2.5	Added Ilimit settings to reporting list
Annex C	Revised with examples of recording data
Annex D	Changed Annex D to show differences between JESD78E and JESD78D
D.1	Differences between JESD78D and JESD78C
D.2	Differences between JESD78C and JESD78B
D.3	Differences between JESD78B and JESD78A
D.4	Differences between JESD78A and JESD78

Differences between JESD78D and JESD78C

Clause	Description of change
1	Added note to scope.
1.2	Added new text (replaced all text from previous version).
2	Added term and definition for maximum stress voltage (MSV).
4.2.5	Added new text (replaced all text from previous version).
Table 1	Renumbered Table 1 to Table 2.
Table 2	Renumbered Table 2 to Table 3.

Differences between JESD78D and JESD78C (cont'd)

Table 2	Table 2 (previously Table 1) changes: 1) Column 4 (Test temperature classification) – Combine Class I and Class II groups together to shorten the table, 2) Column 6 (Trigger test conditions for pin or supply group under test) – Text change to reflect elimination of levels and substitution with recommended characterization conditions, 3) Column 7 (Failure criteria) – Rename the column as latch-up detection criteria, 4) Footnotes 2 - Grammar correction, 5) Footnotes 3, 4 – Text change to show conditions for using maximum stress voltage (MSV); clarification of trigger current and limiting voltage polarities
5	Changed title from "Failure criteria" to "Latch-up detection criteria"
5	Replaced 1st paragraph with new text.
Annex C	Changed Annex C to Annex D. Added new Annex C.

Differences between JESD78C and JESD78B

Clause	Description of change
2	changed "testing of dynamic devices" to "dynamic devices". Definition replaced; placement changed to be alphabetical.
4.1	2nd paragraph replaced first 2 sentences.
4.1	Figure 1, replaced reference to 1.3 to 1.2
4.1	Table 1, Under "trigger test conditions" replaced reference to 1.3 to 1.2 (4 places)
4.1	Table 1, footnote 2, replaced.
4.1	Table 1, footnote 6, replaced.
4.2.2	In item 4, replaced reference to 1.3 to 1.2.
5	Clause in its entirety replaced with new material.

Differences between JESD78B and JESD78A

Clause	Description of change
1	Clause 1.1 combined with clause 1 to conform to JM7 Style Manual
1.2	Replace paragraph to clarify description of Class II
1.2	Clause 1.2 renumbered to 1.1 (changed references accordingly)
1.3	Clause 1.3 renumbered to 1.2 (changed references accordingly) Annex B
Annex B	Changed to Annex C. Added new Annex B.

Differences between JESD78A and JESD78

At time of publication, information on differences between these two revisions was not available.

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Standard Improvement Form JEDEC JESD78F.01

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

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3. Other suggestions for document improvement:

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