JEDEC STANDARD

N-Channel MOSFET Hot Carrier Data Analysis

JESD28-1

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N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS

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N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS

(From JEDEC Board Ballot JCB-01-47, formulated under the cognizance of the JC-14.2 Subcommittee on Wafer-Level Reliability.)

1 Scope

The purpose of this addendum is to provide data analysis examples that may be useful in analyzing MOSFET n-channel hot-carrier-induced degradation data. This addendum is not a standard but a reference that suggests possible alternative hot-carrier data analysis techniques.

The examples presented in this document are restricted to dc testing. While devices are often operated under ac or pulsed conditions, it is beyond the scope of this addendum to predict ac degradations or dc lifetimes of integrated circuits.

The described analysis examples are restricted to devices of a single gate length and temperature. Characterization of a semiconductor process over a wide range of gate lengths and temperatures, is implemented by repeated use of the analysis techniques described within this addendum.

2 Applicable standards

JESD-28, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier Induced Degradation Under DC Stress*

JESD-60, *A Procedure for Measuring P-Channel MOSFET Hot-Carrier Induced Degradation at Maximum Gate Current Under DC Stress*

JESD-77A, *Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices*

3 Terms and definitions

3.1 MOSFET Drain Stress Voltage ($V_{DS,stress}$)

The voltage that is applied between the drain contact and the source contact of a MOSFET during stress.

3.2 MOSFET Gate Stress Voltage ($V_{GS,stress}$)

The voltage that is applied between the gate contact and the source contact of a MOSFET during stress.

3.3 MOSFET Drain Stress Current ($I_{D,stress}$)

The current at the drain contact under the MOSFET stress bias conditions $V_{DS,stress}$ and $V_{GS,stress}$.

3 Terms and definitions (cont'd)

3.4 MOSFET Substrate Stress Current ($IB_{,stress}$)

The current at the bulk contact under the MOSFET stress bias conditions $V_{DS,stress}$ and $V_{GS,stress}$.

3.5 MOSFET Drain Voltage at Usage Condition ($V_{DS,use}$)

The drain voltage for the technology under worst case operating condition.

3.6 MOSFET Gate Voltage at Usage Condition($V_{GS,use}$)

The worst-case degradation gate voltage at $V_{DS,use}$ (See JESD-28).

3.7 MOSFET Drain Current at Usage Condition ($I_{D,use}$)

The current at the drain contact under the MOSFET usage bias conditions $V_{DS,use}$ and $V_{GS,use}$.

3.8 MOSFET Substrate Current at Usage Condition ($I_{B,use}$)

The current at the bulk contact under the MOSFET usage bias conditions $V_{DS,use}$ and $V_{GS,use}$.

3.9 The Specified Failure Criterion (Y_{TAR})

The specified degradation failure criteria for a particular measured parameter.

3.10 Time to Reach the Specified Failure Criterion (t_{TAR})

The elapsed time for the degradation in a particular measured parameter to reach the failure criterion (*TAR*).

4 Measurement conditions and parameters

It is assumed that the hot electron measurements have been performed according to JEDEC specification JESD-28. These analysis methods can be applied to degradations in linear transconductance (Gm), threshold voltage (Vt), linear drain current (I_{Dlin}), saturated drain current (I_{Dsat}) or other transistor parameters.

4.1 Stress and usage conditions

The device is to be stressed using $V_{DS,stress}$ and $V_{GS,stress}$ and the measured parameters are $I_{D,stress}$ and $I_{B,stress}$. $I_{D,stress}$ and $I_{B,stress}$ are the initial values of these parameters and are measured at time equal zero during stress test.

It is also necessary to measure the usage conditions for the MOSFET. In this case the applied bias conditions are $V_{DS,use}$ and $V_{GS,use}$ and the measured parameters are $I_{D,use}$ and $IB_{,use}$. An identical applied nominal bulk voltage should be the used in both the stress and usage measurements.

4.1 Stress and usage conditions (cont'd)

It is preferable to perform all stressing measurements on transistors with identical widths. However, it is sometimes necessary to relate degradations in test transistors of various widths. For this reason, the transistor width *W* parameter is displayed in most model equations and is not combined with other constants.

5 Data requirements

Data collection methods are described in Section 6 of JESD-28.

For n-channel MOSFET devices the degradation data typically displays power law behavior where the absolute value of the percentage change *Y(t)* in a parameter as a function of time *t* is given by:

$$|Y(t)| = Ct^n \quad \textbf{(1)}$$

A linear regression of log(|*Y(t)*|) versus log(*t*) provides the fit coefficients *n* and *C*. The time to failure t_{TAR} of each stressed transistor can be determined by algebraically rearranging Equation 1 to give:

$$t_{tar} = \left(\frac{Y_{TAR}}{C} \right)^{1/n} \quad \textbf{(2)}$$

where Y_{TAR} is the specified degradation failure criteria.

This process is repeated for each stressed transistor, and an individual value t_{TAR} determined.

NOTE LDD devices can saturate during stress and this possibility should be considered when performing data fits as noted in JESD-28.

6 Analysis methodologies

There are three analysis methods commonly used. Each method has equal validity and are based on the same carrier heating model. In this model the probability of a carrier achieving enough energy to cause device damage is directly related to the exponent of the lateral electric field. Each analysis methodology involves the characterization of several transistors at various stress bias conditions. The objective is to predict the time for a certain parameter degradation at usage bias condition. The analysis methods are:

- Substrate/drain current ratio method
- Drain-source voltage acceleration method
- Substrate current method

Whichever method is chosen a 2-sided confidence interval (e.g. 80%) can be constructed about the data set. The confidence bounds will indicate the likelihood that repeating the experiment will produce result passing the use condition requirement. (If the confidence interval is excessively large consider increasing the sample size of stressed units or the number of stress conditions.)

These methods are described in detail .

6.1 Substrate/drain current ratio method

Stressing experiments are performed on a number of transistors, each at different stress bias conditions. A minimum of three stress conditions, with at least five transistors per stress condition is required. For each transistor, the stress conditions are $V_{DS,stress}$ and $V_{GS,stress}$ and the following parameters are obtained:

$$t_{TAR};\ Y_{TAR};\ I_{D,stress};\ I_{B,stress};\ I_{D,use};\ I_{B,use} \text{ and } n.$$

The failure time model is given by

$$t_{tar} I_{D,stress} = HW \left(\frac{I_{B,stress}}{I_{D,stress}} \right)^{-m} \quad \textbf{(3)}$$

where H and m are fit parameters and W is the transistor width. If measurements are performed on transistors of equal width, then the quantity W can be combined with the fit parameter H. Rearranging Equation 3 gives:

$$\frac{t_{tar} I_{D,stress}}{W} = H \left(\frac{I_{B,stress}}{I_{D,stress}} \right)^{-m} \quad \textbf{(4)}$$

Taking the logarithm of both sides of Equation 4 yields:

$$\log\left(\frac{t_{tar} I_{D,stress}}{W} \right) = \log H - m \times \log\left(\frac{I_{B,stress}}{I_{D,stress}} \right) \quad \textbf{(5)}$$

A linear regression analysis is performed to obtain fit parameters H and m. Figure 1 displays a plot of this relationship. According to theory, m should be 3, but values may vary depending on stress conditions and technology. In a stress experiment with typical stress bias voltage conditions, a moderate variation in $I_{B,stress}/I_{D,\ stress}$ results in a large variation in failure times, t_{TAR}. The quantity on the left hand side of Equation 5 is thus dominated by the failure times t_{TAR} with other terms relatively constant.

Once the constants H and m are determined, the time to failure at usage condition is estimated using Equation 4 to give:

$$t_{tar,use} = HW \frac{1}{I_{D,use}} \left(\frac{I_{B,use}}{I_{D,use}} \right)^{-m} \quad \textbf{(6)}$$

6.1 Substrate/drain current ratio method (cont'd)

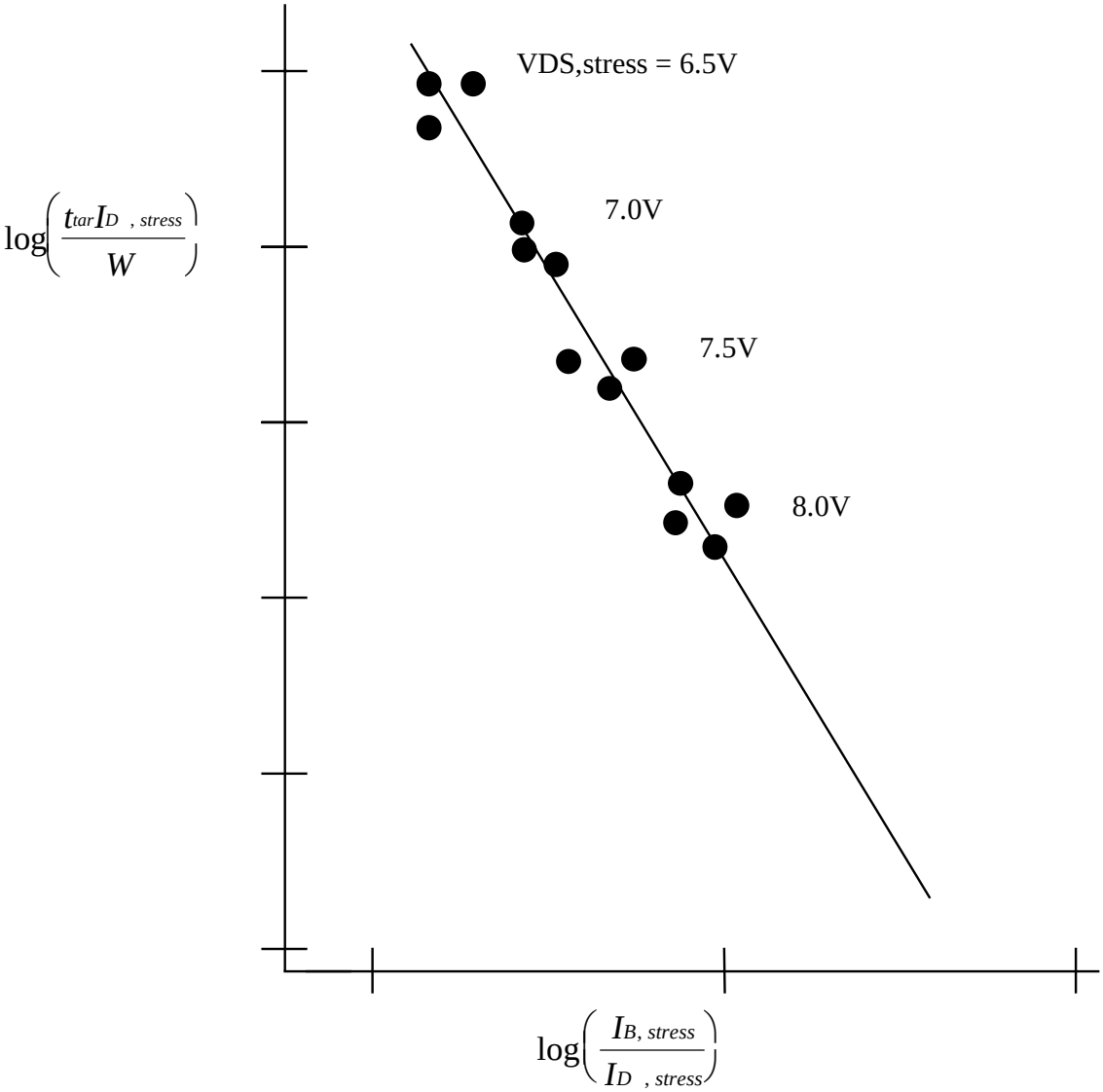

Figure 1 — Example data for substrate/drain current ratio method

6.2 Drain-source voltage acceleration method

In this method the stress is performed on a number of transistors, each at a different stress condition $V_{DS,stress}$ and $V_{GS,stress}$. For each transistor, the time to reach the failure criteria is obtained (t_{tar}):

The time to failure is given by:

$$t_{tar} = t_o \exp\left(\frac{B}{V_{DS,stress}}\right) \quad \textbf{(7)}$$

where t_O and B are fit parameters. Figure 2 displays a typical plot showing this relationship. Taking the natural logarithm of both sides of Equation 7 yields the following relationship:

$$\ln t_{tar} = \ln t_o + B\left(\frac{1}{V_{DS,stress}}\right) \quad \textbf{(8)}$$

A linear regression analysis of Equation 8 yields the fit coefficients t_O and B. The failure time $t_{tar,use}$ at usage bias conditions is found by substituting $V_{DS,use}$ for $V_{DS,stress}$ in Equation 8.

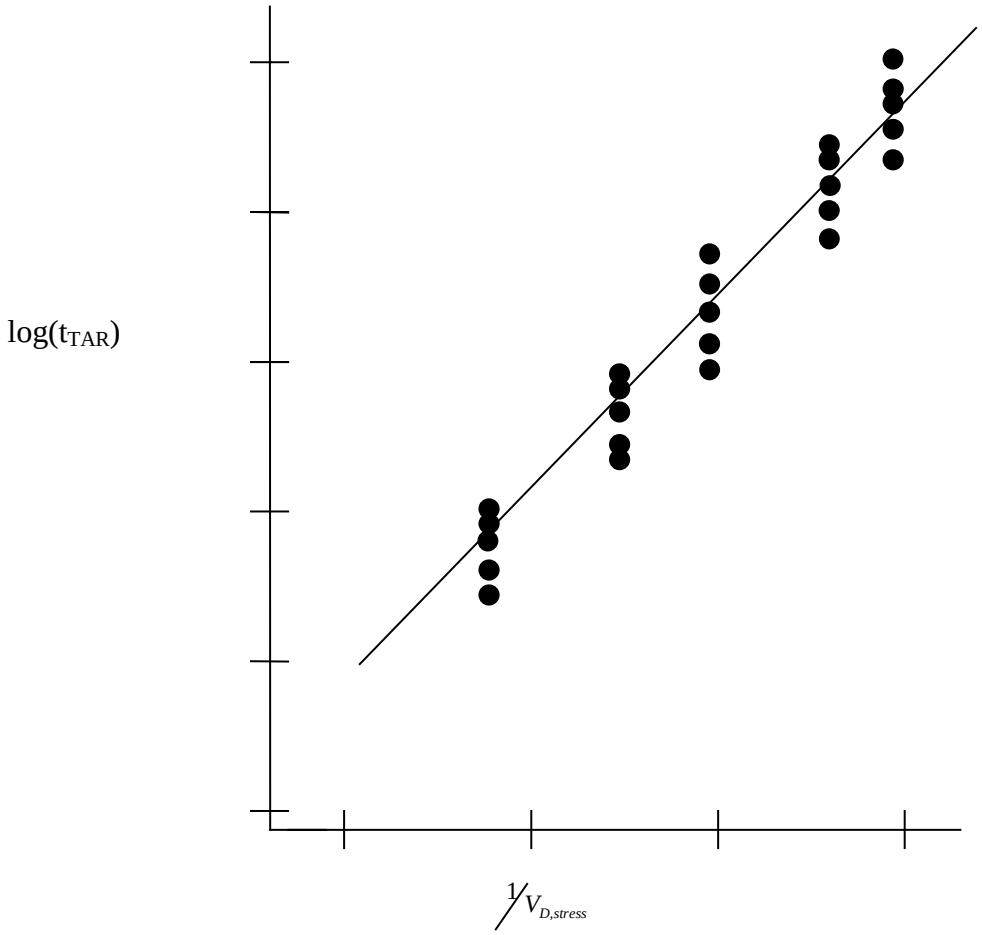

Figure 2 — Example data for drain-source voltage acceleration method

6.3 Substrate current method

Again stress experiments are performed on a number of transistors, each at a different stress bias condition. For each transistor, the stress conditions are $V_{DS,stress}$ and $V_{GS,stress}$ and the following parameters are obtained:

t_{tar}; $I_{B,stress}$ and $I_{B,use}$.

The time to failure is given by

$$t_{tar} = C\left(\frac{I_{B,stress}}{W}\right)^{-b} \quad \textbf{(9)}$$

where C and b are fit parameters, and W is the transistor width. Figure 3 displays this relationship. Taking the logarithm of both sides of Equation 9 yields the following:

$$\log t_{tar} = \log C - b \cdot \log\left(\frac{I_{B,stress}}{W}\right) \quad \textbf{(10)}$$

Again a linear regression is performed on Equation 10 to obtain the fit coefficients C and b.

The time to failure at usage bias conditions is found from

$$t_{tar,use} = C\left(\frac{I_{B,use}}{W}\right)^{-b} \quad \textbf{(11)}$$

where $I_{B,use}/W$ in brackets is the substrate current per unit width at the usage condition averaged over the number of stressed transistors.

6.3 Substrate current method (cont'd)

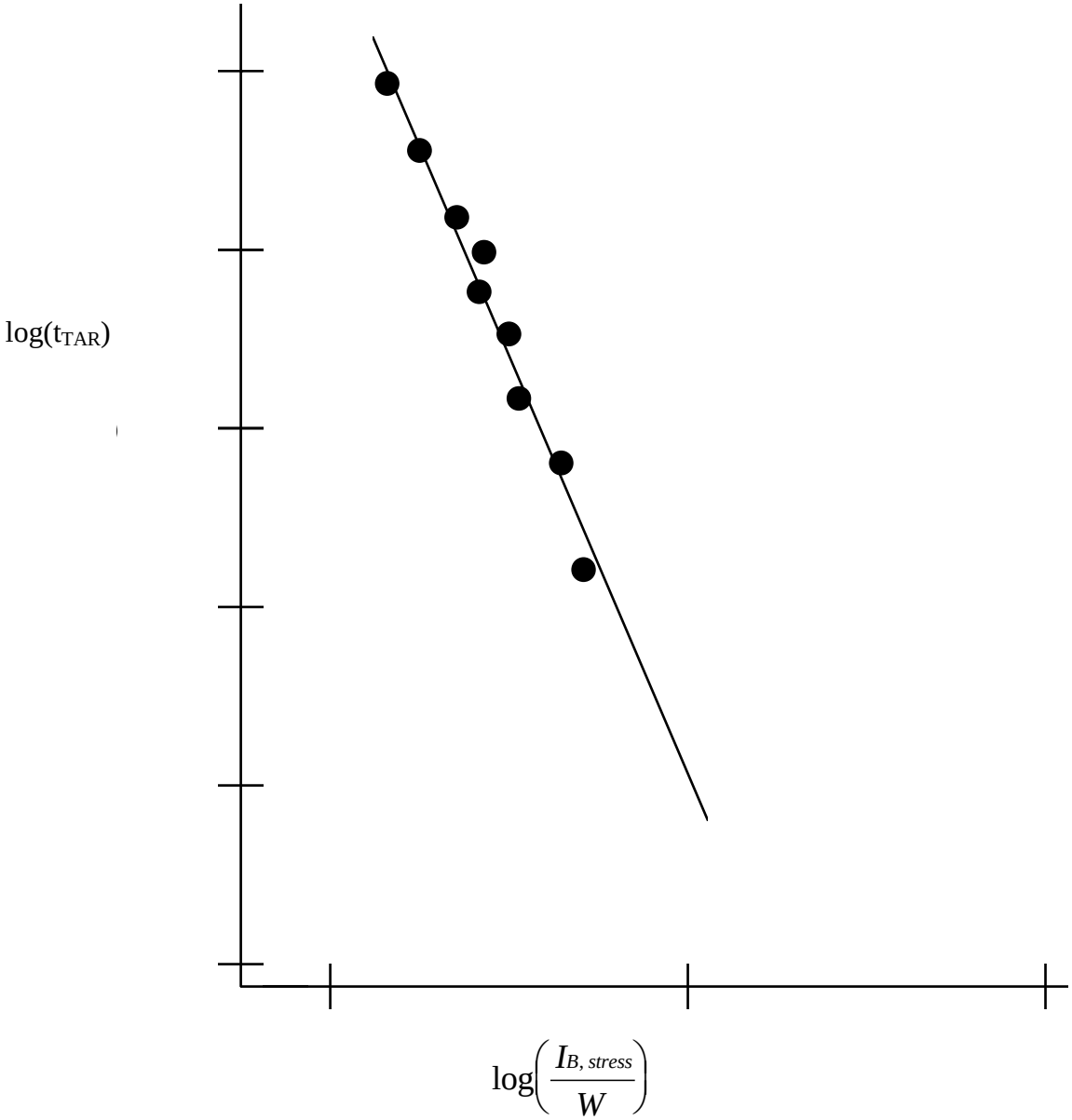

Figure 3 — Example data for the substrate current method


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