EIA/JEDEC STANDARD

Standard for Description of Low-Voltage TTL-Compatible, 5 V-Tolerant CMOS Logic Devices

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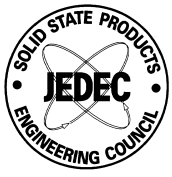

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CONTENTS

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(From JEDEC Council Ballot JCB–95–72, formulated under the cognizance of JC–40 Committee on Digital Logic.)

1 INTERFACE STANDARD

1.1 Purpose:

To provide a standard for Low–Voltage 5 V –tolerant CMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

1.2 Scope:

This standard defines dc interface and switching parameters for a high–speed, low–voltage 5 V–tolerant CMOS digital logic family. This standard covers specifications for CMOS Logic series as defined in Section 2.

2 DEFINITIONS

CMOS Series

Includes devices that utilize CMOS technology.

5 V–tolerant defined within this specification means that leakage current is negligible when inputs, or outputs in the high–impedance state are exposed to voltages exceeding V_{DD}, guaranteed to 5.5 V.

Includes devices whose input logic levels are TTL–compatible.

Compliant with JEDEC standard 8–A.

Prefix

Prefix “74” immediately preceding family name indicate the operating temperature range. 74XXX refers to the Commercial (COM’L) version of devices which are specified over –40 °C to 85 °C.

3 STANDARD SPECIFICATIONS

3.1 Absolute Maximum Continuous Ratings (Notes 1 and 2):

Supply Voltage, V_{DD} . . . . . –0.5 V to 4.6 V
dc input voltage, V_{IN} (except I/O pins) . . . . . –0.5 V to 6.0 V
dc output voltage, V_{OUT} (including I/O pins) output in high or low state . . . . –0.5 V to V_{DD} + 0.5 V
dc output voltage, V_{OUT} (including I/O pins) output in 3–state . . . . . –0.5 V to + 6.0 V
dc input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
dc output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) . . . . . ±50 mA
dc current into any output in the low state, I_{OL} . . . . . 50 mA
dc current into any output in the high state, I_{OH} . . . . . –50 mA
dc supply current per supply pin . . . . . ±100 mA
dc ground current per ground pin . . . . . ±100 mA
Storage temperature range . . . . . –65 °C to 150 °C

Note 1: Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

Note 2: Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

3.2 Recommended Operating Conditions:

Symbol	Parameter	MIN	MAX	Unit
V_{DD}	Supply voltage	2.7	3.6	V
V_{IN}	Input voltage	0	5.5	V
V_{OUT}	Output voltage outputs active	0	V_{DD}	V
V_{OUT}	Output voltage outputs disabled	0	5.5	V
T_A	Operating free–air temperature	–40	85	°C
$\Delta t/\Delta v$	Input transition rise or fall rate (Note 1)	0	10	ns/V

Note 1: As measured between 0.8 V and 2 V.

3.3 dc Specifications:

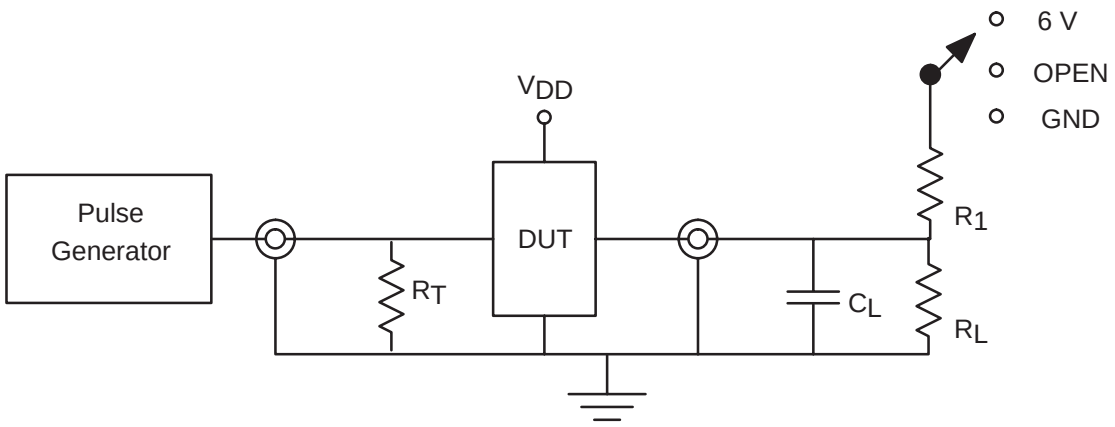
Symbol	Parameter	Test Conditions		74 Series		Unit
				MIN	MAX	
V_{IH}	High–level input voltage	2.7 V ≤ V_{DD} ≤ 3.6 V		2.0		V
V_{IL}	Low–level input voltage	2.7 V ≤ V_{DD} ≤ 3.6 V			0.8	V
V_{OH}	High–level output voltage	V_{DD} = 2.7 V, V_I = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{DD} – 0.2		V
		V_{DD} = 3 V, V_I = V_{IH} or V_{IL}	I_{OH} = –12 mA I_{OH} = –24 mA	2.4 2.0		V
V_{OL}	Low–level output voltage	V_{DD} = 2.7 V, V_I = V_{IH} or V_{IL}	I_{OL} = 100 µA		0.2	V
		V_{DD} = 3 V, V_I = V_{IH} or V_{IL}	I_{OL} = 12 mA I_{OL} = 24 mA		0.4 0.55	V
I_I	Input current	V_{DD} = MAX, V_I = 5.5 V or GND			±5	µA
I_{OZ}	Off–state output current (Notes 1, 3)	V_{DD} = MAX, 0 V ≤ V_O ≤ 5.5 V	V_I = V_{IH} or V_{IL}		±10	µA
I_{OFF}	Power–off leakage current	V_{DD} = 0V, 0V ≤ (V_I, V_O or $V_{I/O}$) ≤ 5.5V			100	µA
I_{DD}	Static supply current	V_{DD} = MAX, V_I = V_{DD} or GND			(Note 2)	µA
		V_{DD} = MAX, 3.6 V ≤ (V_I or V_O) ≤ 5.5 V			(Note 2)	µA
ΔI_{DD}	Static supply current per input at a specified level	V_I = V_{DD} – 0.6 V, other inputs at V_{DD} or GND, V_{DD} = 2.7 V to 3.6 V (Note 3)			500	µA

Note 1 – For I/O pins, I_{OZ} includes the input leakage current.

Note 2 – Refer to manufacturer's data sheet.

Note 3 – For bus–hold type pins refer to manufacturer's data sheet.

4 TEST CIRCUITS AND SWITCHING WAVEFORMS



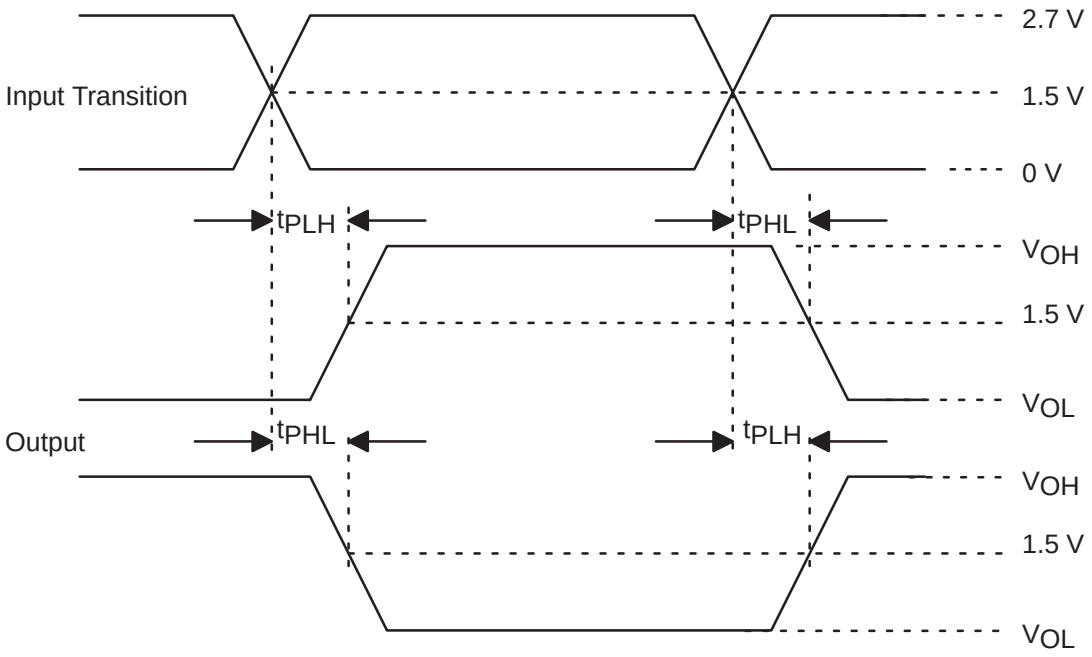
Test	Switch
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	GND
t_{PZL}	6 V
t_{PHZ}	GND
t_{PLZ}	6 V

C_L = 50 pF or equivalent (includes jig and probe capacitance).

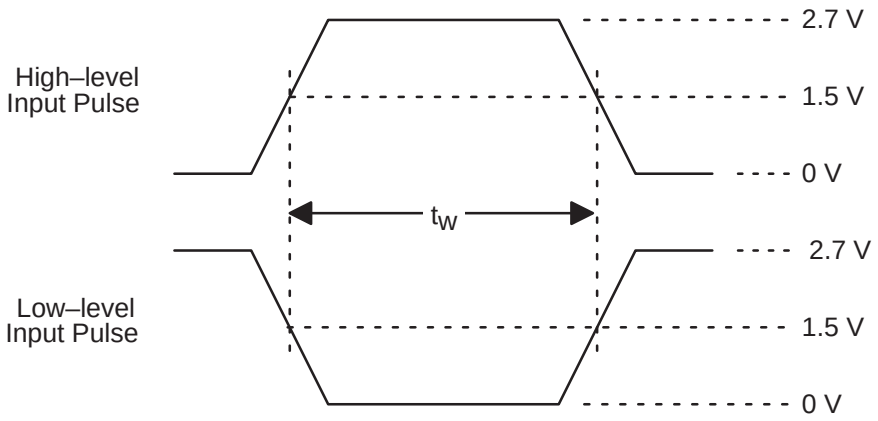
$R_L = R_1$ = 500 Ω or equivalent.

$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω).

PROPAGATION DELAY MEASUREMENTS



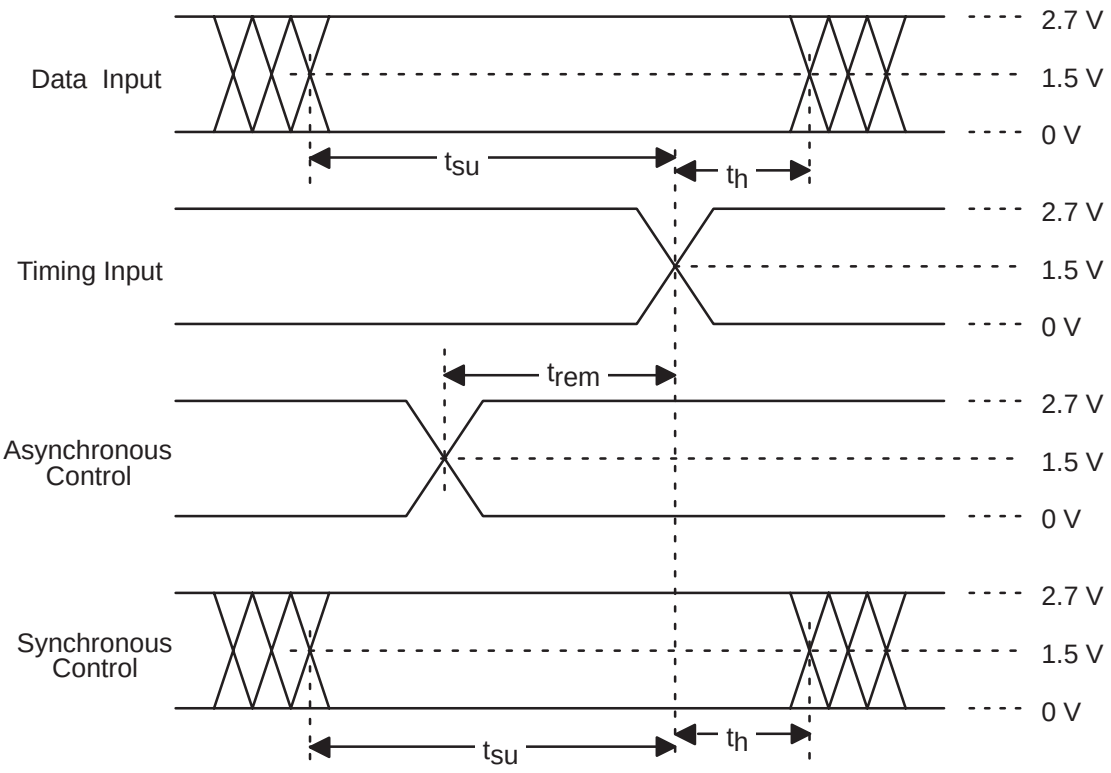
PULSE DURATION (WIDTH) MEASUREMENTS



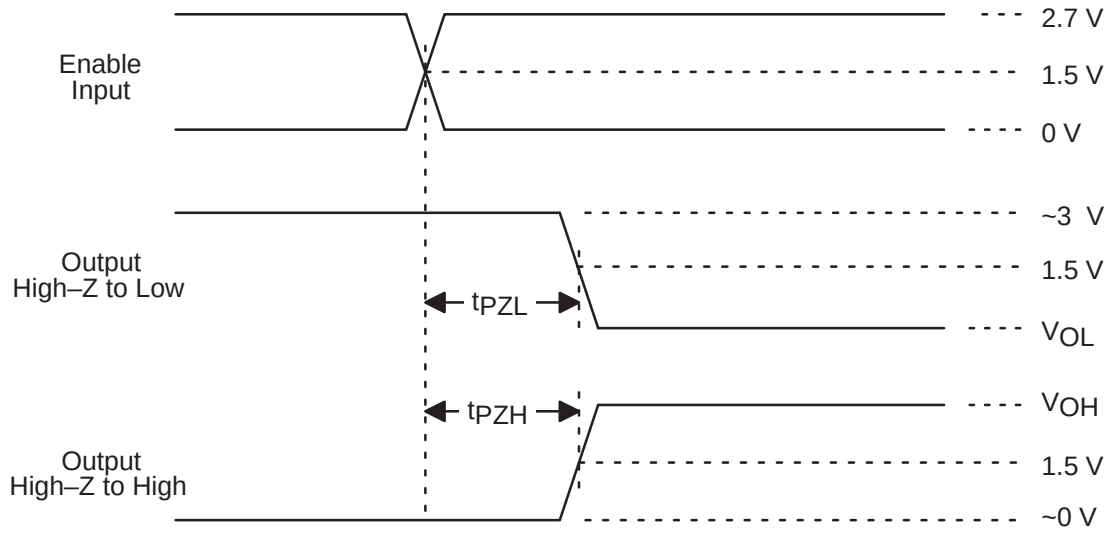
Output requirements: Device must follow truth table
$V_{OL} \leq V_{OL}$ max
$V_{OH} \geq V_{OH}$ min

Input Conditions: $t_r = t_f$ = 2.5 ns (or as fast as required) from 10% to 90% of 0 V to 2.7 V.

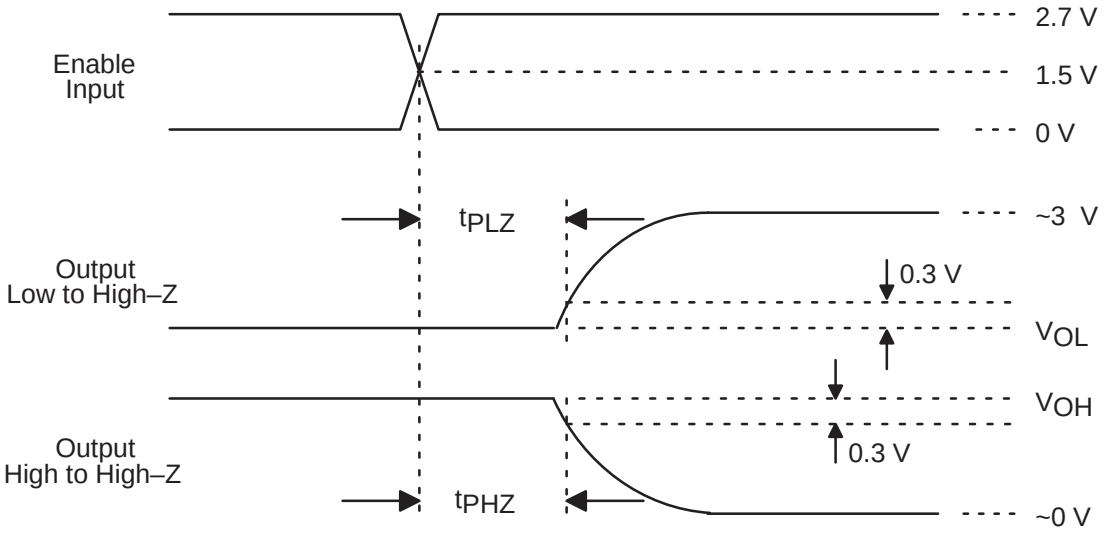
SETUP AND HOLD TIME MEASUREMENTS



ENABLE TIME MEASUREMENTS



DISABLE TIME MEASUREMENTS



5 REFERENCE TO OTHER APPLICABLE JEDEC STANDARDS AND PUBLICATIONS

JEDEC Standard No. 8–A	Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits