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DDR2 DIMM Clock Skew Measurement Procedure Using A Clock Reference Board

JEP152

MAY 2007

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Published by

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DDR2 DIMM Clock Skew Measurement Procedure Using a Clock Reference Board

Contents

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(From JEDEC Board Ballot, JCB-04-84A, Formulated under the cognizance of the JC-45.1 Subcommittee on RDIMM.)

1 Scope

This document is the work product of the JC-45.1 “DDR2 DIMM Clock Skew Measurement” task group.

The purpose of this document is to define procedures to measure clock parameters on registered DIMMs using the DDR2 Clock Reference Board. It is NOT the intent of this document to set specification values or validation requirements.

2 Differential vs. Single-ended probing

This document describes measurements with both single-ended and differential probes. There are several pros and cons of each method:

- hard to calibrate and keep calibrated four probes at once.
- more chances for human error with four probes.
- roughly half the effort with four single-ended probes if Vix measurement is required
- differential probes are perceived to be more accurate especially when close-by GND contact for the single ended probes is not availible.
- single ended jitter measurements can be more accurate than those with differential probes, especially if the bandwidth of the single ended probes is higher.

3 Measurement of skew, jitter and slew rate using differential probes

3.1 Test equipment and setup

- Oscilloscope with minimum bandwidth of 3 GHz and 8— Gigasamples/s,
- Two differential probes with minimum bandwidth of 3 GHz, resulting in a probe tip bandwidth of no less than 2.5 GHz
- PC2-3200/4300 JEDEC CRB Clock Reference Board (=CRB) by CST,
- DC Power Supply for 3.3 V to CRB

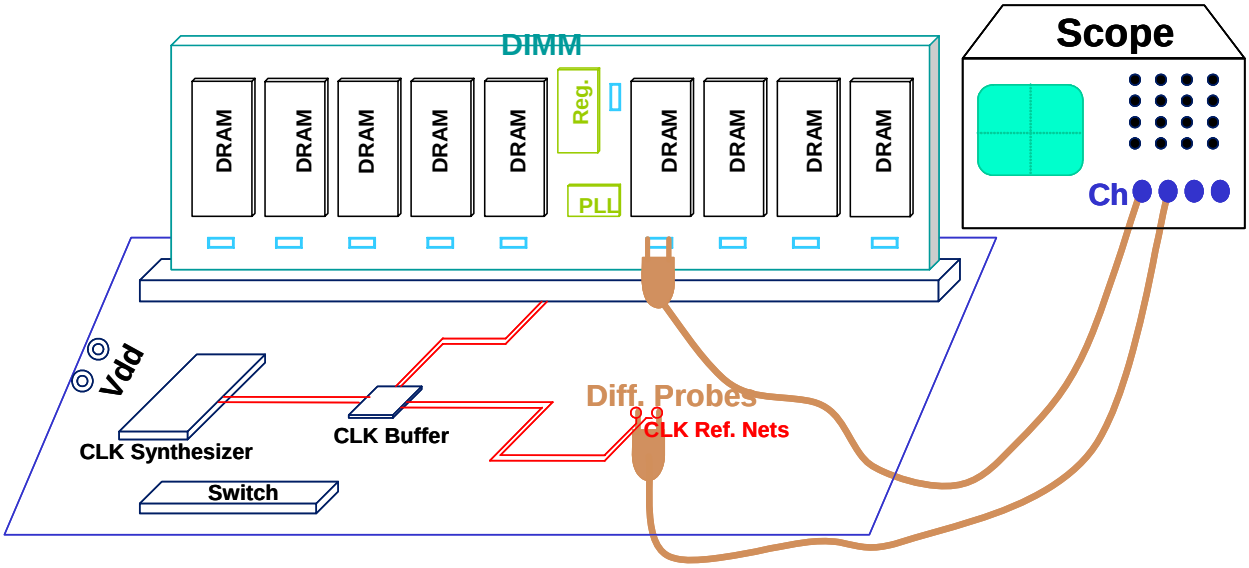

Figure 1 — Measurement setup with differential probes

3 Measurement of skew, jitter and slew rate using differential probes (cont'd)

3.2 Preparation

1) Allow instruments to warm up (> 20 min),
2) Disconnect all probes from the scope,
3) Perform the scope calibration,
4) Attach differential probes 1& 2 to CH1 & CH2[1] of the scope,
5) Perform the probes calibration[2] using the calibration fixture delivered with the scope,
6) determine equipment jitter as decribed in Annex A
7) Attach wires of equal length & less than 10 mm to the (PLL-in, DRAMs & register) termination resistors of the DIMM under test (not required for "direct attach" probes),
8) Plug the DIMM into the CRB socket,
9) Set the CRB power supply voltage,
10) Check the value of supplies at the CRB & DIMM test points (centermost decoupling capacitor on the top egde of the DIMM),
11) Ensure that switches on the CRB are set at the right position (measurement frequency (see CRB Manual, page TBD),
12) Make sure that the probes are properly de-skewed (see CRB Manual, page TBD),
13) Connect the CH1 to the CKref probe points of the CRB.

1. Other channels may be used, however the text assumes the suggested assignments.

2. A good check on the proper de-skewing of the oscilloscope probes is to follow this same procedure, exchanging the roles of CH1 and CH2. Next, switch CH3 and CH4. If you do not get the same answer for all measurements, the probes have not been properly de-skewed, OR the frequency responses of the two channel + probe combinations are insufficiently matched. This step should be performed as often as neccessarry depending on the actual drift of the measurement setup.

3 Measurement of skew, jitter and slew rate using differential probes (cont'd)

3.3 Data Aquisition

1) Attach the probe (CH2) to the first DRAM clock termination resistor.
2) Use Auto-trigger mode, and a timebase setting sufficient to capture at least 100 clock cycles per acquisition. Use gain setting such that the waveform fills the scope screen.
   a) Acquire one (or more) acquisitions of the two channels CH1 and CH2 such that 10,000[1] clock cycles are captured (accumulated) making sure that there are at least 3 samples per transition. Then analyze the waveform data as outlined in 3.4 through 3.6. This analysis may be performed with built-in functions/software of the oscilloscope or the data may be transfered to perform the analysis elswhere.
3) Repeat steps 1 and 2 with each of the other termination resistors on the DIMM including the one for the register(s) , taking special care to assure proper polarity on the differential probe.

3.4 Skew[2]

1) Obtain by non-linear interpolation, the time t_{X+} of positive going threshold crossing for each of the recorded signals from CH1 and CH2. Do this by first finding the pair of points on an upward slope straddling V_{TH} = 0 V, and then by interpolating the time at which the line or curve[3] passing through neighboring point intersects the threshold voltage.
2) Being careful to associate correctly the values from CH1 with those from CH2, calculate the difference between these values of "time of crossing". Thus a single estimate for t_{D+} is given by the difference:

$$t_{D+} = t_{X+}(\mathrm{CH2@V_{TH}}) - t_{X+}(\mathrm{CH1@V_{TH}})$$

3) In a nearly identical fashion as for step 1, obtain by nonlinear interpolation, the time t_{X-} of negative going threshold crossing for each of the recorded signals for CH1 and CH2.

---

1. Note that typical PLL specifications use only 1,000 samples to measure skew, jitter etc. A sample size of 10,000 was chosen to improve repeatability of the measurement results.

2. From several real-time digital oscilloscope vendors, this measurement, or one very similar, is "built-in" as an explicit measurement of "skew" between two signals.

3. It is a standard procedure to up-sample between the two straddling points (using the nearest neighboring points on either side) to obtain a new set of data in the region of the crossing. The two new straddling points from the new set are determined, and a final linear interpolation used to estimate the time of threshold crossing.

3 Measurement of skew, jitter and slew rate using differential probes (cont'd)

3.4 Skew (cont'd)

4) In a nearly identical fashion as for step 2, being careful to associate correctly the values from CH1 with those from CH2, calculate the difference between these values of "time of crossing". Thus a single estimate for t_{D-} is given by the difference:

$$t_{D-} = t_{X-}(\mathrm{CH2@V_{TH}}) - t_{X-}(\mathrm{CH1@V_{TH}})$$

5) Repeat steps 1 through 4, for the remaining threshold crossings in the recorded signals, forming an average value for the each of t_{D+} and t_{D-}, until an average of at least N = 100 values for each is obtained. These average values constitute the final values for the measured skew $t_{sk(LH)}$ and $t_{sk(HL)}$ of the clock at this DRAM/register with respect to the reference clock. Record these values.

$$t_{sk(LH)} = \frac{1}{N} \cdot \sum_{N} t_{D+}$$

$$t_{sk(HL)} = \frac{1}{N} \cdot \sum_{N} t_{D-}$$

6) The termination resistor is typically some distance away from the CK/$\overline{\mathrm{CK}}$ balls or pins of the DDR2 SDRAM or register; a flight time of 50 ps per 12 mm is a reasonable estimate for the required correction. The deltas need to be determined from the net topology and may be obtained from the DIMM design specification of the DIMM under test.

3 Measurement of skew, jitter and slew rate using differential probes (cont'd)

3.5 Jitter

1) Obtain by non-linear interpolation, the positive going time of threshold (Vth = 0 V) crossing for the recorded CH2 signal. Do this by first finding the pair of points on an upward slope straddling Vth = 0 V, and then interpolating the time at which the line is estimated to intersect the threshold (same as step 1 in 3.4). Record each of these values as T^{+}_{n}.

2) In a fashion nearly identical to step 1, obtain by nonlinear interpolation, the next negative going time of threshold crossing the recorded CH2 signal. Thus a single value for T^{-}_{n} is given by the time of downward crossing of CH2@Vth for the nth time (same as step 3 in 3.4).

3) Repeat steps 1 and 2, for the remaining threshold crossings in the recorded signals, thus obtaining two arrays of values T^{+}_{n} and T^{-}_{n} (for n = 1 to N) where N is the total number of clock cycles in acquired CH2 recorded signal, and is about 10,000.

4) Two other arrays of half-period values are obtained from the T^{+}_{n} and T_{n}^{-} values by forming the difference between adjacent T^{+}_{n} and T^{-}_{n}, thus $HP^{+}_{n} = T^{+}_{n} - T^{-}_{n}$ and $HP_{n}^{-} = T^{-}_{n} - T^{+}_{n+1}$. See Figure 2.

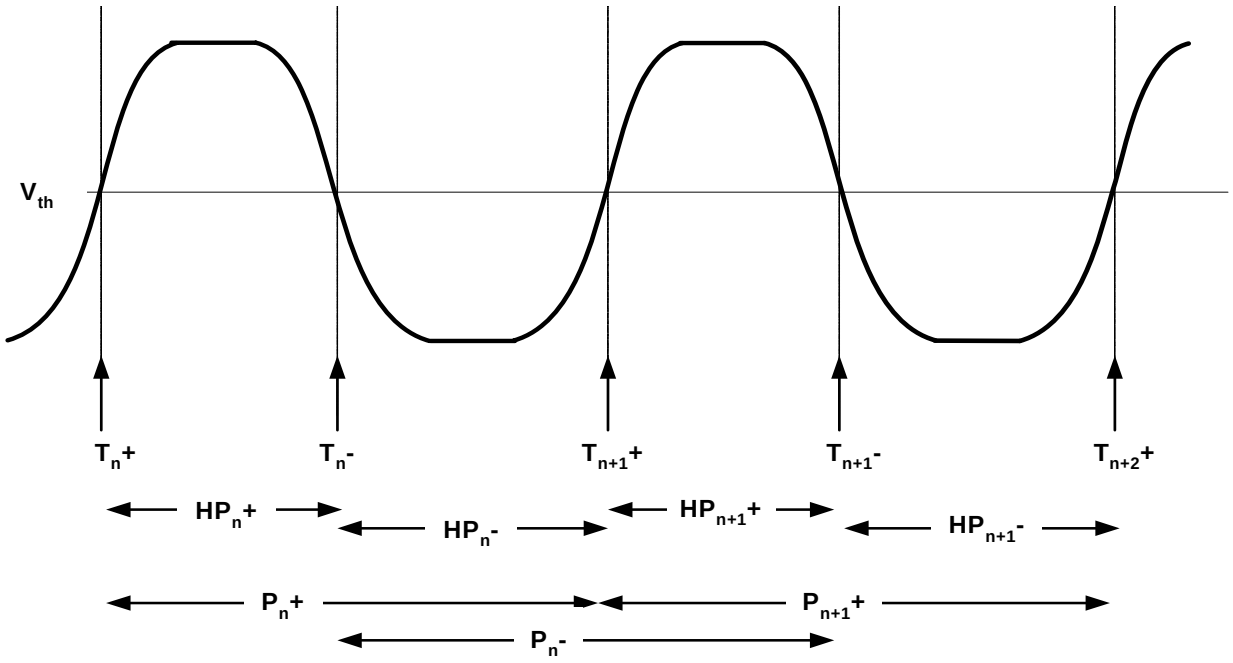

Figure 2 — Graphic relationship between T^{+-}_{n}, HP^{+-}_{n} and P^{+-}_{n}

3 Measurement of skew, jitter and slew rate using differential probes (cont'd)

3.5 Jitter (cont'd)

5) Yet one more array of period values is obtained from the transition time values T^+_n by forming the difference between adjacent T^+_n entries; thus $P^+_n = (T^+_n) - (T^+_{n+1})$. See Figure 2.

6) Now create a new array as follows: using the array of P^+ values, calculate:

$$Tj(P^+)m = \frac{max\{P^+_{(1000m)} \ldots P^+_{(1000m+999)}\} - min\{P^+_{(1000m)} \ldots P^+_{(1000m+999)}\}}{2}$$

for each non-overlapping window of 1,000 cycles in the array. For an array with 10,000 cycles, there will be 10 (m = 0 ... 9) non-overlapping windows with 1,000 cycles each.

7) Compute the average value of the $Tj(P^+)m$ array. Report this number as $t_{jit(per)}$[1].

$$t_{\mathrm{jit(per)}} = \frac{1}{10} \sum_{m=0}^{9} Tj(P^+)m$$

8) Repeat steps 6 and 7 for each array HP^+ and HP^- to obtain $Tj(HP^+)$ and $Tj(HP^-)$.

3.6 Slew rate

1) Obtain by non-linear interpolation, the positive going time t_{X+} of threshold (V_{TH1} = -250 mV) crossing and the positive going time t_{X+} of threshold (V_{TH2} = 500 mV) crossing for the recorded CH2 waveform. Do this for each threshold by first finding the pair of points on an upward slope straddling the threshold, and then by interpolating the time at which the line or curve[2] passing through both point intersects the threshold. Thus a single estimate for sr+ is given by the ratio:

$$sr+ = \frac{V_{\mathrm{TH2}} - V_{\mathrm{TH1}}}{t_{\mathrm{X+}}(\mathrm{CH2@V_{TH2}}) - t_{\mathrm{X+}}(\mathrm{CH2@V_{TH1}})}$$

1.the calculation of jitter used here differs slightly from the definition of jitter in the PLL specifications e.g. JESD65. In the PLL specification one would calculate not half of the delta between min and max, one would calculate the max and min deviation from the average of all measurements. It is believed that the difference is negligible. The advantage of using this formula is that this function is readily availible on most scopes.

2.It is a standard procedure to up-sample between the two straddling points (using the nearest neighboring points on either side) to obtain a new set of data in the region of the crossing. The two new straddling points from the new set are determined, and a final linear interpolation used to estimate the time of threshold crossing.

3 Measurement of skew, jitter and slew rate using differential probes (cont'd)

3.6 Slew rate (cont'd)

2) As for step 1, obtain by non-linear interpolation, the negative going time t_{X-} of threshold crossing for each of the thresholds (V_{TH3} = 500 mV and V_{TH4} = -250 mV). Thus a single estimate for sr- is given by the ratio:

$$sr\text{-} = \frac{V_{TH4} - V_{TH3}}{t_{X+}(CH2@V_{TH4}) - t_{X+}(CH2@V_{TH3})}$$

3) Repeat steps 1 and 2, for the remaining events (zero crossings in the up-sampled difference waveform) forming an average value for each of the measurements, until an average of at least N = 100 values is obtained. These average values constitute the final values for the measurement of SR+ and SR- for this node. Record these values.

$$SR+ = \frac{1}{N} \cdot \sum_{N} sr+$$

$$SR- = \frac{1}{N} \cdot \sum_{N} sr-$$

4) By choosing different levels for V_{TH} a more accurate value for "slew rate" could be obtained; especially for high slew rates. However the purpose of the procedure is to produce values that can directly be compared to the DDR2 SDRAM input requirements. This is the reason why V_{TH} values consistent with the DDR2 data sheet were chosen. Only if the measurement result is in the range of 1 V/ns to a little bit above 2 V/ns (differential), the accurancy is relevant. If the measured value is higher than 2 V/ns then this fact alone is enough to judge the DIMM performance with respect to system timing budgets.

4 Measurement of skew, jitter, slew rate and crosspoint voltage using single-ended probes

4.1 Test equipment and setup

- Oscilloscope with min bandwidth of 3 GHz and 8 Gigasamples/s,
- Four single-ended probes with minimum bandwidth of 3 GHz resulting in a probe tip bandwidth of no less than 2.5 GHz
- PC2-3200/4300 JEDEC CRB Clock Reference Board (=CRB) by CST,
- DC Power Supply for 3.3 V to CRB

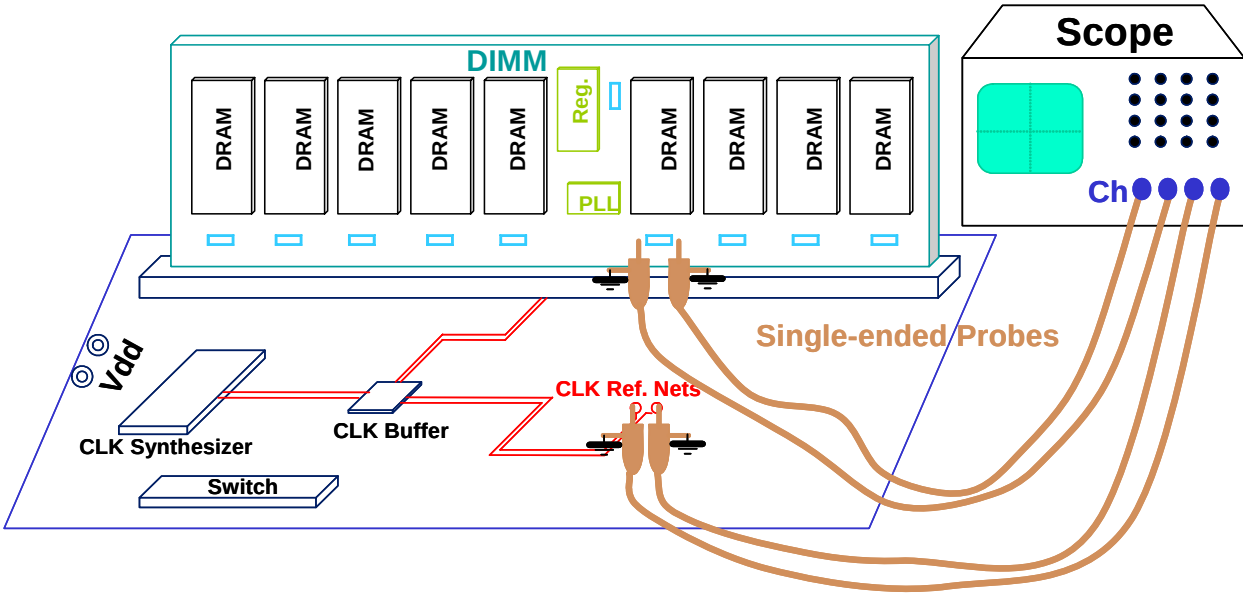

Figure 3 — Measurement setup with single-ended probes

4 Measurement of skew, jitter, slew rate and crosspoint voltage using single-ended probes (cont'd)

4.2 Preparation

1) Allow instruments to warm up (> 20 min),
2) Disconnect all probes from the scope,
3) Perform the scope calibration,
4) Attach probes 1 through 4 to CH1 through CH4 of the scope,
5) Perform the probes calibration[1] using the calibration fixture delivered with the scope,
6) Determine equipment jitter as decribed in Annex A
7) Attach wires of equal length & less than 10 mm to the (PLL-in, DRAMs & register) termination resistors of the DIMM under test (not required for "direct attach" probes),
8) Plug the DIMM into the CRB socket,
9) Set the CRB power supply voltage,
10) Check the value of supplies at the CRB & DIMM test points (centermost decoupling capacitor on the top egde of the DIMM),
11) Ensure that switches on the CRB are set at the right position (measurement frequency (see CRB Manual, page TBD),
12) Make sure that the probes are properly de-skewed (see CRB Manual, page TBD),
13) Connect the CH1 to CK and CH2 to $\overline{CK}$ of the CKRef probe points of the CRB[2].

1. A good check on the proper de-skewing of the oscilloscope probes is to follow this same procedure, exchanging the roles of CH1 and CH2. Next, switch CH3 and CH4. If you do not get the same answer for all measurements, the probes have not been properly de-skewed, OR the frequency responses of the two channel + probe combinations are insufficiently matched. This step should be performed as often as neccessarry depending on the actual drift of the measurement setup.
2. Other channels may be used, however the text assumes the suggested assignments.

4 Measurement of skew, jitter, slew rate and crosspoint voltage using single-ended probes (cont'd)

4.3 Data aquisition

Step 1: Attach probe CH3 to CK and probe CH4 to $\overline{CK}$ at the first DRAM clock termination resistor.

Step 2: Use Auto-trigger mode, and a timebase setting sufficient to capture at least 100 clock cycles per acquisition. Acquire one (or more) acquisitions of channels CH1 through CH4 such that 10,000[1] clock cycles are captured making sure that there are at least 3 samples per transition. Use gain setting such that the waveform fills the scope screen.

Step 3: If there are fewer than 50 points on the rising and falling edges (20%-80% region) of either waveforms (which will typically be the case), digitally up-sample the four digital waveforms to obtain >50 samples in this region. (note: either windowed sin(x)/x or cubic upsampling filters may be used. The factor can be determined a priori, knowing the nominal risetime and the sampling rate of the oscilloscope).

Step 4: Subtract the two up-sampled signals from CH1 and CH2 to obtain a waveform representing the difference signal WD1 = W(RefCK) – W(RefCK).

Subtract the two up-sampled signals from CH3 and CH4 to obtain a waveform representing the difference signal WD2 = W(CK) – W($\overline{CK}$).

Step 5: Analyze the waveform data as outlined in 4.4 through 4.7. This analysis may be performed with built-in functions/software of the oscilloscope or the data may be transfered to perform the analysis elswhere.

Step 6: Repeat steps 1 through 5 with each the other termination resistors on the DIMM including the one for the register(s) , taking special care to assure that CH3 is consistently connected to CK and CH4 is connected to $\overline{CK}$

1. Note that typical PLL specifications use only 1,000 samples to measure skew, jitter etc. A sample size of 10,000 was chosen to improve repeatability of the measurement results.

4 Measurement of skew, jitter, slew rate and crosspoint voltage using single-ended probes (cont'd)

4.4 Skew

1) Obtain by linear interpolation, the positive going time t_{X+} of zero-crossing for WD1 and WD2 (by first finding the pair of points straddling the V_{TH} = 0 V level, and then interpolating the time at which a line through them would have passed through zero).
2) Measure the time from the zero crossing of WD1 to the zero crossing of WD2. Thus a single estimate for t_{D+} is given by the difference:

$$t_{D+} = t_{X+}(\mathrm{WD2@V_{TH}}) - t_{X+}(WD1@\mathrm{V_{TH}})$$

3) Repeat step 1 and 2 but for a negative going zero-crossing t_{X-}. The values obtained are a single estimate for t_{D-}:

$$t_{D-} = t_{X-}(\mathrm{WD2@V_{TH}}) - t_{X-}(WD1@\mathrm{V_{TH}})$$

4) Repeat steps 1 through 3 for the remaining events (zero crossings in the up-sampled difference waveform) forming an average value for each of the measurements, until an average of at least N = 100 values is obtained. These average values constitute the final values for the measurement of skew $t_{sk(LH)}$ and $t_{sk(HL)}$ of the clock at this DRAM/register with respect to the reference clock. Record these values.

$$t_{sk(LH)} = \frac{1}{N} \cdot \sum_{N} t_{D+}$$

$$t_{sk(HL)} = \frac{1}{N} \cdot \sum_{N} t_{D-}$$

5) The termination resistor is typically some distance away from the CK/$\overline{\mathrm{CK}}$ balls or pins of the DDR2 SDRAM or register; a flight time of 50 ps per 12 mm is a reasonable estimate for the required correction. The deltas need to be determined from the net topology and may be obtained from the DIMM design specification of the DIMM under test.

4 Measurement of skew, jitter, slew rate and crosspoint voltage using single-ended probes (cont'd)

4.5 Jitter

Measure the jitter of WD2 using the same procedure as is used with a differential probe. Begin with step 3 in section 3.5 of the differential procedure and use WD2 instead of CH2.

4.6 Slew rate

Measure the slewrate of WD2 using the same procedure as is used with a differential probe. Begin with step 1 in section 3.6 of the differential procedure and use WD2 instead of CH2.

4.7 Crosspoint voltage

1) Obtain by linear interpolation, the positive going time of zero-crossing for this difference signal Wdiff2 (by first finding the pair of points straddling the 0V level, and then interpolating the time at which a line through them would have passed through zero).

   NOTE This is the same as step 1 in 4.4.

2) With this time, using either (CK or $\overline{CK}$) of the up-sampled channel waveforms, determine the voltage associated with this time. (a good consistency check is to assure both upsampled channel waveforms yield the same result). This voltage is a single estimate for Vix+.

3) Repeat step 2, but for a negative going zero-crossing. The value obtained is a single estimate for Vix-.

4) Repeat steps 1, 2 and 3, for the remaining events (zero crossings in the up-sampled difference waveform) forming an average value for each of the measurements, until an average of at least 100 values is obtained. These average values constitute the final values for the measurement of Vix+ and Vix- for this differential clock termination resistors on the DIMM. Record this value.

Annex A Measuring equipment jitter

The basic idea is simple, and it is worth stating outside the definition of the precise steps comprising the method. It is to measure the jitter between two channels while presenting the same (analog) clock or data signal to both of the input channels.

The beauty of this concept is that it is simple and unpretentious. Everyone can easily grasp that at the actual point(s) probed, there can be no jitter between the point and itself. The only difference between the two channels is therefore the probes, the scope channel amplifiers and the two different recording devices (presumably ADCs). As such, in a perfect world there should be no jitter, and therefore in the real world the jitter that is observed is jitter due to the measurement (apparatus and method) itself.

Now, beware, that does not mean that the measured jitter “is” exactly the jitter introduced by the instrument. It is indeed closely related, but it ís not exactly equal to this, as will be shown. Jitter measurements can be categorized into several kinds:

1) relative signal measurements (comparing timing of two separate signals or two different differential signals.) such as skew measurements
2) relative edges in the same signal, such as half-period, period and cyclecycle jitter measurements.

The implication of the Instrument induced jitter for each of these cases is different, even though the mechanisms contributing to the intrinsic jitter are the same.

Annex A Measuring equiptment jitter (cont'd)

A.1 Procedure using single-ended probes

Step 1: Attach the four single-ended probes to CH1 through CH4. Attach the probe of CH1 **and** CH3 to the CK test point of the CRB[1]. Attach CH2 **and** CH4 to the CK# test point of the CRB (This is not as easy as it sounds, but important).

Step 2: Each channel should have the same vertical scale setting.

Step 3: Follow steps similar to 2 through 4 in 4.3. to obtain the waveforms WD1 and WD2.

Step 4: Calculate the arrays $T1^+$ and $T2^+$ using the method outlined in 3.4 steps 1 though 3 using successively WD1 and WD2 instead of CH2 as the set of positive going transition times of the waveforms through zero.

Step 5: Calculate the jitter of the skew between the two signals by forming the array JS:

$$JS_{\mathrm{n}} = {T1^+}_n - {T2^+}_n - \frac{1}{N} \cdot \sum_{n=1}^{N} \{{T1^+}_n - {T2^+}_n\}$$

NOTE the third term pepresents the skew of the probes (plus some multiple of the clock period); The mean of JS is zero.

Step 6: Determine and report "equipment jitter" or "intrinsic skew jitter" σ_{ISJ} as standard deviation of the distribution JS .

$$\sigma_{\mathrm{ISJ}} = \sigma(JS) = \sqrt{\frac{1}{N} \cdot \sum_{n=1}^{N} \{JS_n\}^2}$$

A.2 Procedure using differential probes

Step 1: Attach the two differential probes to CH1 and CH2. Attach the both probes CK/ CK# test point of the CRB. (This is not as easy as it sounds, but important).

Step 2: Each channel should have the same vertical scale setting.

Step 3: Follow steps 4 through 8 of the procedure for single ended probes above CH1 instead of WD1 and CH2 instead of WD2

1.Equipment jitter might be dependent on the slewrate of the signal at the test point. As such it might be required to measure equipment jitter at all test points. It is believed though that the test point at the CRB is representative for all test points under consideration. This is to be seen. Especially in cases where one clock output drives four SDRAMs the slewrate at the SDRAM clock input might be higher than the one at the CRB test point. In those cases it might be advisable to report "equipment jitter" at several test points.

Annex B Overscaling

Common engineering judgment and many measurement procedures suggest that best measurement results will be achieved if the attenuation/gain of the scope is set such that the signal just fills the screen. This procedure is no exeption (see 3.3 step 2).

However for jitter measurements it has been shown that gain settings higher than the above recommended may be beneficial to reduce equipment jitter. The reason lies in the fact that higher gain settings may increase the slew rate and will therefore reduce the uncertainty in the zero crossing of a signal.

Drawbacks of overscaling include:

- potential large signal saturation effects within the analog path of the test equipment;

- fewer data points in the transition region causing increased numerical noise when the trantition time is interpolated.

Therefore it is recommended to use overscaling with caution and only in special cases. A factor of 2x the recommneded gain should work for most equipment. When overscaling is used, this fact should be reported along with the test results.

To find the gain setting that minimizes equipment jitter for a certain test point and probe, measure “equipment jitter” (see Annex A) for successivly higher gain settings between 1x and 2x of the recommended (signal fills the screen) setting.

Annex C Correlation bewteen equipment/instrument jitter, observed jitter and 'true' jitter

Assuming we have already obtained or can obtain a figure for intrinisic equipment jitter σ_{ISJ} (as per appendix A) for a given signal, scope and probe. It is possible to make a better estimate of the jitter really present in a measurement of period or half-period jitter. This procedure describes the basic relations between the intrinsic skew jitter, observed jitter and the true jitter. Little attempt is made to thoroughly justify the procedure; the procedure is simply described so an estimate can be made. Given the intrinsic skew jitter σ_{ISJ}, which is an RMS figure, you can approximate the relationship between the true jitter between two real signals as:

$$\sigma_{skew,observed}^2 = \sigma_{skew,true}^2 + \sigma_{ISJ}^2$$

where σ_{ISJ} is the intrinsic skew jitter associated with a specific probe, scope and signal shape. In other words the jitter observed for the skew between two signals is a combination of the true jitter between the signals and the instrumentationís contribution to the measurement. This contribution from the instrumentation is assumed to contribute incoherently with the true jitter and may be approximated by the "intrinsic skew jitter". The skew measurement consists of the difference between two time measurements, in exactly and analogous fashion to the way the σ_{ISJ} is obtained. That ís why we can approximate the instrumentation's contribution in this case to be the intrinsic skew jitter. So the true skew jitter can be estimated as:

$$\sigma_{skew,true} = \sqrt{\sigma_{skew,observed}^2 - \sigma_{ISJ}^2}$$

A period measurement also consists of the difference of two time measurements. So it does not require a great leap of imagination to see that the relationship is the same, and the instrumentation contributes jitter in proportion to the intrinsic skew jitter for this measurement. Thus the true period jitter can be approximated as:

$$\sigma_{period,true} = \sqrt{\sigma_{period,observed}^2 - \sigma_{ISJ}^2}$$

Half-period jitter is also a subtraction of two time measurements. (The following equations assume that intrinsic skew jitter has similar value for rising and falling edges):

$$\sigma_{halfperiod+,true} = \sqrt{\sigma_{halfperiod+,observed}^2 - \sigma_{ISJ}^2}$$

$$\sigma_{halfperiod-,true} = \sqrt{\sigma_{halfperiod-,observed}^2 - \sigma_{ISJ}^2}$$

Annex C Correlation bewteen equipment/instrument jitter, observed jitter and 'true' jitter (cont'd)

Now, in the context of the jitter measurements in 3.5 and 4.5 for providing jitter figures with a confidence level of 99.9% (or an expected peak variation for 1000 measurements), we are left with the problem of how to translate this measured figure to RMS, adjust it and translate it back to a value corresponding to a peak (PP_{1000}) over 1000 measurements. This can be done very simply provided the distribution measured is approximately Gaussian which is almost always the case. The approxmation for the translation from peak per thousand to RMS is:

$$PP_{1000} = \Psi(0.001) = 6.581053515471 \cdot \sigma \cong 6.6 \cdot \sigma$$

where, Ψ is the confidence interval for a Gaussian distribution (with $\sigma = 1$) as a function of inverse confidence (or "1.0 - confidence level"). Now the figure for the confidence interval at 10^{-3} is in fact known to high precision. For our purposes 6.6 seems sufficient. So were we to translate to RMS, and adjust for true RMS jitter, and translate back to PP_{1000} we would have the following:

$$PP_{1000\ \text{skew, true}} \cong 6.6 \cdot \sqrt{\left(\frac{PP_{1000\ \text{skew, observed}}}{6.6}\right)^2 - \sigma_{ISJ}{}^2}$$

The relationships for period jitter and half period jitter then become:

$$t_{\text{jit(per)min, true}} = 3.3 \cdot \sqrt{\left(\frac{t_{\text{jit(per)min, observed}}}{3.3}\right)^2 - \sigma_{ISJ}{}^2}$$

$$Tj(HP^+)_{\text{min, true}} \cong 3.3 \cdot \sqrt{\left(\frac{Tj(HP^+)_{\text{min, observed}}}{3.3}\right)^2 - \sigma_{ISJ}{}^2}$$

$$Tj(HP^-)_{\text{min, true}} \cong 3.3 \cdot \sqrt{\left(\frac{Tj(HP^-)_{\text{min, observed}}}{3.3}\right)^2 - \sigma_{ISJ}{}^2}$$

where "observed" refers to the value obtained from the measurements according sections 3.5 and 4.5. Note that $t_{jit(per)}$min, Tj(HP+)min, Tj(HP-)min represent half of the peak to peak jitter (6.6 --> 3.3).

Annex D Correlating clock reference boards and normalized skew

Although great care has been taken to assure that all clock reference boards have the same properties, it needs to be conceded that they consist of a number of complex active and passive components which can result in noticable deviations. At the same time each clock reference board is delivered with a “bare PLL plug-in card”. This is a DIMM like card that has a 1 inch clock lead-in net which is differentially terminated with 120 ohms and a 1 pF capacitor soldered on top of the resistor to represent a typical PLL input capacitance. (This card has originally been designed as tool to characterize PLL prototypes).

Measurements on a small number of samples yielded variation of -30 ps to +20 ps skew using the same “bare PLL plug-in card” in different clock reference boards. On the other hand: measuring several PLL plug-in cards in the same clock reference boards resulted in less than +/- 5 ps spread in measurements. This suggests that the PLL plug-in card is a good vehicle to correlate clock reference boards.

NOTE ***Positive*** skew means that the clock at the point under test is ***later*** than the clock at the test point of the reference net on the CRB; ***Negative*** skew means that the clock at the point under test is ***earlier*** than the clock at the test point of the reference net on the CRB.

D.1 Correlation Procedure

1) Install “bare” PLL plug-in card in the first clock reference board.
2) Measure clock skew to the plug-in card termination resistor.
3) Repeat step 2 - two more times.
4) Record average of measurements as the “correlation number”.
5) Repeat steps 1 through 4 to find the correlation number for the second clock reference board.
6) Subtract correlation numbers for the two clock reference boards and report result as the correlation offset.

Annex D Correlating clock reference boards and normalized skew (cont'd)

D.1.1 Alternate method using a DIMM (e.g., if plug-in card is not available)

1) Install a DIMM in the first clock reference board.
2) Measure clock skew to the PLL input termination resistor.
3) Repeat step 2 - two more times.
4) Record average of measurements as the "correlation number".
5) Remove DIMM from first clock reference board and insert in second clock reference board
6) Follow steps 1 through 4 to find the correlation number for the second clock refrence board.
7) Subtract correlation numbers for the two clock reference boards and report result as the correlation offset.

NOTE 1 There are two main differences between the methods. One is that the first method is quicker and easier. It does not require shipment of boards as part of the process. The second difference is that the first method is measuring two different target boards while the second method measures the same target board with both reference boards. All plug-in cards are believed to be the same (within 5 ps), so this should not be an issue. In the case of disagreement, the second method will govern.

NOTE 2 It is absolutely critical to make sure that all measurements are done at the same location on the plug-in card (or DIMM). Failure to do so will invalidate the results of the measurement.

D.2 Normalized Skew

As the measurements on bare PLL plug-in cards are considered the most repeatable ones, we define here the term "normalized skew". When reporting "normalized skew" the measured skew numbers from test points on a DIMM are adjusted to reflect the (assumed) skew of the clock reference board that was used for the measurement.

Alternatively the actual measurement data may be reported along with the skew number obtained from measuring a bare PLL plug-in card with the same clock reference board.

Using this method, the bare PLL plug-in card becomes the true "reference"!

CST keeps a number of PLL plug-in cards from the initial batch as "golden" reference. Future batches of the PLL plug-in card might have a systematic deviation from the golden batch. This deviation should be marked on those future cards.

Annex E Differences between revisions

Revision	Section	Changed
Ballot JC42.5-03-265 counted in December 2003	several	Text in Blue
Ballot JC45.1-04-056 counted in March 2004 Text in RED	3.3, 4.3	Recommended gain setting added
	3.5	Jitter Procedure added
	4.5	Jitter Procedure added
	5	Appendices added.
1st BoD ballot version 4-13-2004 (JCB-04-84)	last	this revision log added
	Appen-dix D	Tab-stops added
	3.5	footnote added to refer to patent disclosure
	begin	table of contents added
5-13-2004 ballot draft	3.5	simplified jitter procedure added
	3.2, 4.2	added footnote on how often to calibrate/de-skew
	Apen-dix C	section for “true” jitter added
	Appen-dix A	symbol for σ_{ISJ} introduced
	Appen-dix E	Section added including “normalized skew”
5-18-2004 ballot JC45.1-04-144	Appen-dix E	added note to define “positive” and “negative” skew. spelled out “first” and “second” “clock reference board.”
6-23-2005 current BoD ballot		Appendix “Determination of estimated jitter boundaries for a mea-surement of 1,000 samples” removed. Appendix E becomes D
	3.5	removed footnote refering to patent disclosure
	3.5	Moved “Simplified Jitter Procedure” to chapter 3.5, replacing the previous “Jitter” chapter.
	all	changed all font colors to black
	3.5, 4.5	renamed Tj(P+) to $t_{jit(per)}$ in accordance with JESD65
	3.4, 4.4	TD+ and TD- were placed by tsk(LH) and tsk(HL) in accordance with JESD65

Standard Improvement Form **JEDEC JEP152**

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1. I recommend changes to the following:

☐ Requirement, paragraph number _____

☐ Test method number _____ Paragraph number _____

The referenced paragraph number has proven to be:

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2. Recommendations for correction:

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