JEDEC STANDARD

Standard Test Loads For Dual-Supply Level Translation Devices

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STANDARD TEST LOADS FOR DUAL-SUPPLY LEVEL TRANSLATION DEVICES

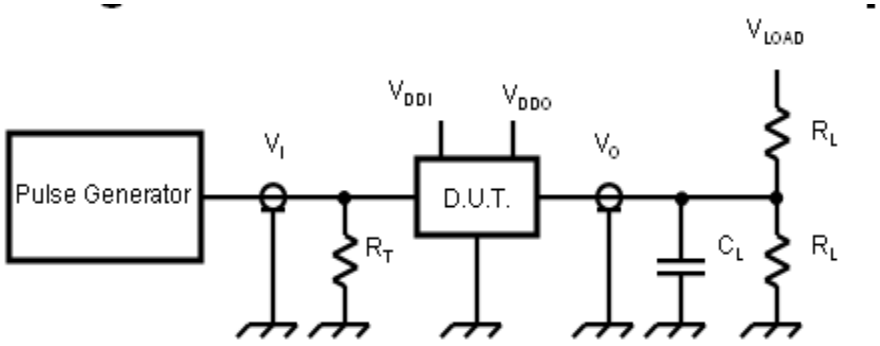
(From JEDEC Board Ballot JCB-05-86, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines ac test loads for dual-supply level translation devices. Uniform test loads enable easy comparison of electrical parameters of dual-supply level translation devices across functions, logic families and IC suppliers.This standard is only intended to apply to devices released subsequent to the publication of this document.

2 Test setup

Figure 1 shows the test setup for measurement of AC parameters. The DUT represents the dual-supply level translation device. V_{DDI} is the supply voltage associated with the input port and V_{DDO} is the supply voltage associated with the output port.



R_L = Load Resistor
C_L = Load Capacitor
R_T = Termination Resistance (should be equal to the output impedance, Z_O, of the pulse generator)

NOTE The test fixture design should follow high speed digital design practices appropriate for the waveforms being measured. The goal is to minimize the effect of the test environment on the measured results

Figure 1 — Test setup

2 Test setup (cont'd)

2.1 Input signal characteristics

The amplitude of the input signal to the DUT can range from 0 to V_{DDI}. The transition time of the input signal should not exceed the value shown in Table 1 for the respective V_{DDI} values.

Table 1 — Input voltage levels for different supply voltages

V_{DDI}	Maximum V_I	t_r or t_f
1.1 to 1.3 V	V_{DDI}	≤ 2ns
1.4 to 1.6 V	V_{DDI}	≤ 2ns
1.65 to 1.95 V	V_{DDI}	≤ 2ns
2.3 to 2.7 V	V_{DDI}	≤ 2ns
2.7 V	V_{DDI}	≤2.5ns
3.0 to 3.6 V	V_{DDI}	≤2.5ns
4.5 to 5.5 V	V_{DDI}	≤ 6ns

NOTE Input edge-rates t_r and t_f are measured from 10% to 90% of the input signal.

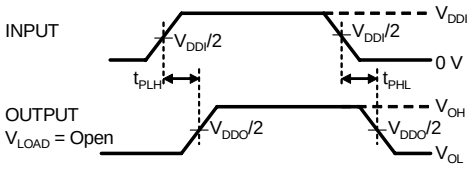
2.2 Values of C_L and R_L for Different Supply Voltage Nodes

A load of R_L=2kΩ and C_L=15pF is used for V_{DDO} values of 1.1 V to 5.5 V as shown in Table 2.

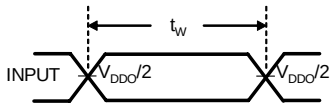
Table 2 — Capacitive and resistive loads for different V_{DDO} values

V_{DDO}	C_L	R_L
1.1 to 1.3 V	15 pF	2kΩ
1.4 to 1.6 V	15 pF	2kΩ
1.65 to 1.95 V	15 pF	2kΩ
2.3 to 2.7 V	15 pF	2kΩ
2.7 V	15 pF	2kΩ
3.0 to 3.6 V	15 pF	2kΩ
4.5 to 5.5 V	15 pF	2kΩ

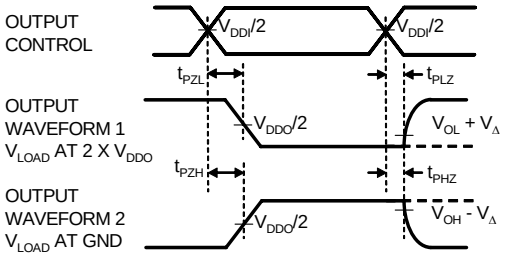
3 Test waveforms and measurement points



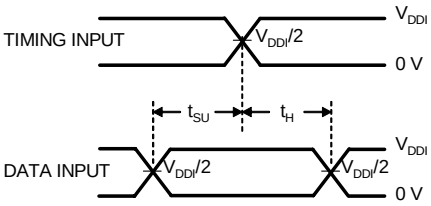
MEASUREMENT 1. PROPAGATION DELAY TIMES



MEASUREMENT 3. PULSE DURATION (WIDTH) MEASUREMENTS



MEASUREMENT 2. ENABLE AND DISABLE TIMES



MEASUREMENT 4. SETUP AND HOLD TIMES

Figure 2 — Test waveforms

Table 3 — Test measurement points for inputs

V_{DDI}	Measurement Point For Inputs
1.1 to 1.3 V	$V_{DDI}/2$
1.4 to 1.6 V	$V_{DDI}/2$
1.65 to 1.95 V	$V_{DDI}/2$
2.3 to 2.7 V	$V_{DDI}/2$
2.7 V	$V_{DDI}/2$
3 to 3.6 V	$V_{DDI}/2$
4.5 to 5.5 V	$V_{DDI}/2$[a]

a. For TTL devices, the measurement point is 1.5 V

3 Test waveforms and measurement points (cont'd)

Table 4 — Test measurement points for outputs

V_{DDO}	Measurement Point For Outputs	V_{Δ}
1.1 to 1.3 V	$V_{DDO}/2$	0.1 V
1.4 to 1.6 V	$V_{DDO}/2$	0.1 V
1.65 to 1.95 V	$V_{DDO}/2$	0.15 V
2.3 to 2.7 V	$V_{DDO}/2$	0.15 V
2.7 V	$V_{DDO}/2$	0.3 V
3 to 3.6 V	$V_{DDO}/2$	0.3 V
4.5 to 5.5 V	$V_{DDO}/2$[a]	0.3 V

a. For TTL devices, the measurement point is 1.5 V

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1. I recommend changes to the following:

☐ Requirement, paragraph number _____

☐ Test method number _____ Paragraph number _____

The referenced paragraph number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

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3. Other suggestions for document improvement:

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