JEDEC STANDARD

Addendum No. 2 to JESD79-3 - for 1.25 V DDR3U-800, DDR3U-1066, DDR3U-1333, and DDR3U-1600

JESD79-3-2

OCTOBER 2011

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by
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1.25 V DDR3U-800, DDR3U-1066, DDR3U-1333, and DDR3U-1600

(From JEDEC Board Ballot, JCB-11-39, formulated under the cognizance of the JC-42.3 Subcommittee on Volatile RAM.)

1 Scope

The JESD79-3 document defines the DDR3 SDRAM, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments with the exception of what is stated within this addendum.

The purpose of this addendum is to define the DDR3U specifications that supersede the DDR3 specifications in the JESD79-3. The use of DDR3-800, DDR3-1066, DDR3-1333, and DDR3-1600 titles in JESD79-3 are to be interpreted as DDR3U-800, DDR3U-1066, DDR3U-1333, and DDR3U-1600, respectively, when applying towards DDR3U definition; unless specifically stated otherwise.

2 DDR3U VDD/VDDQ Requirements

Table 1 — Recommended DC Operating Conditions - DDR3U (1.25 V) operation

Symbol	Parameter/Condition	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	1.19	1.25	1.31	V	1,2,3,4
V_{DDQ}	Supply voltage for Output	1.19	1.25	1.31	V	1,2,3,4
NOTE 1 Maximum DC value may not be greater than 1.31 V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g., 1 sec). NOTE 2 If maximum limit is exceeded, input levels shall be governed by DDR3L specifications depending on the value. NOTE 3 Under these supply voltages, the device operates to this DDR3U specifcation. NOTE 4 Once initialized for DDR3U operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation (see Figure 1).						

Table 2 — Recommended DC Operating Conditions - DDR3L (1.35 V) operation

Symbol	Parameter/Condition	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	1.283	1.35	1.45	V	1,2,3,4
V_{DDQ}	Supply voltage for Output	1.283	1.35	1.45	V	1,2,3,4
NOTE 1 Maximum DC value may not be greater than 1.425 V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g., 1 sec). NOTE 2 If maximum limit is exceeded, input levels shall be governed by DDR3 specifications. NOTE 3 Under these supply voltages, the device operates to this DDR3L specifcation. Once initialized for DDR3L operation, DDR3U operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3U operation (see Figure 1).						

DDR3U SDRAM is 1.5V endurant.

DDR3U SDRAM operation at 1.5V is not supported.

2 DDR3U VDD/VDDQ Requirements (cont'd)

Table 3 — Absolute Maximum DC Ratings

Symbol	Parameter/Condition	Rating	Units	Notes
V_{DD}	Voltage on VDD pin relative to Vss	-0.4V ~ 1.6V	V	1,3
V_{DDQ}	Voltage on VDDQ pin relative to Vss	-0.4V ~ 1.6V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4V ~ 1.6V	V	1
TSTG	Storage Temperature	-55 to +100	^{o}C	1,2

NOTE 1 Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 VDD and VDDQ must be within 250 mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.

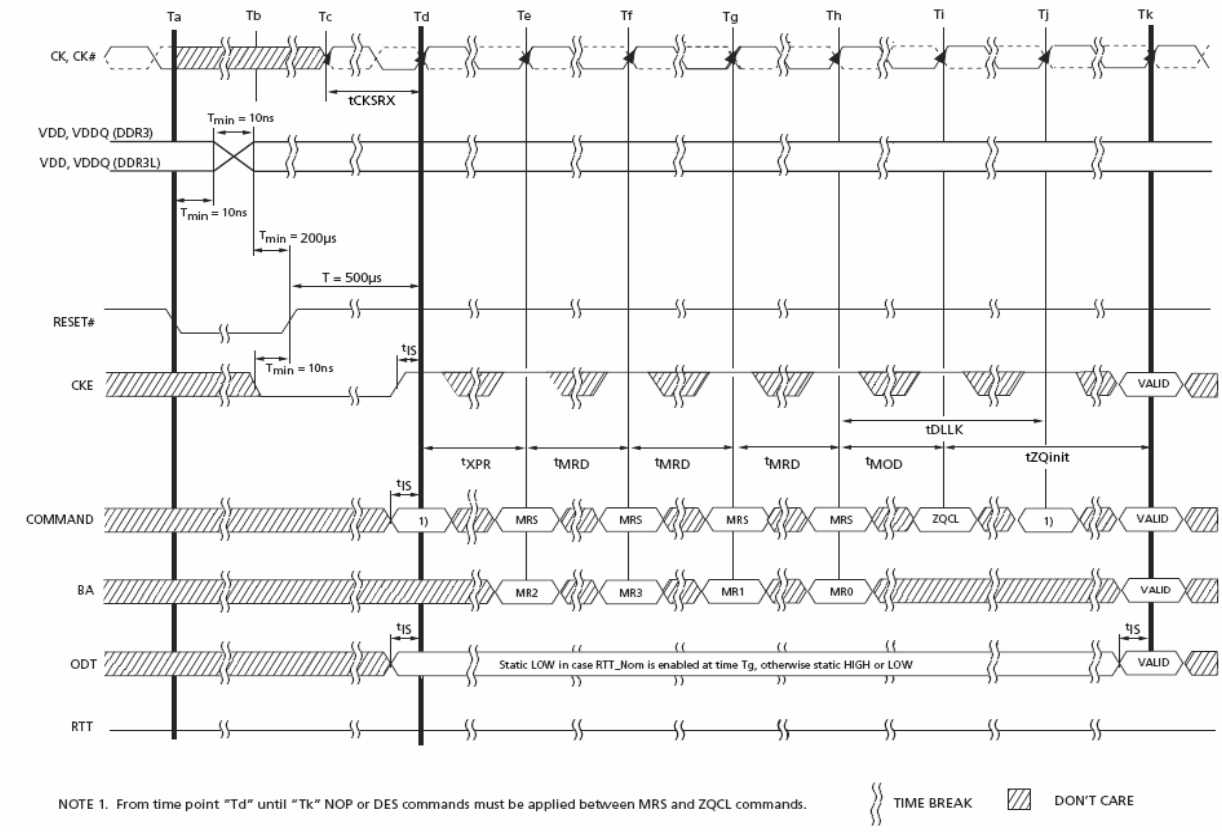

Figure 1 — VDD/VDDQ Voltage Switch Between DDR3U and DDR3L

3 1.25 V DDR3U AC and DC Logic Input Levels for Single-Ended Signals

3.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 4 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3U-800, DDR3U-1066		DDR3U-1333, DDR3U-1600		Unit	Notes
		Min	Max	Min	Max		
VIH.CA(DC90)	DC input logic high	Vref + 0.090	VDD	Vref + 0.090	VDD	V	1
VIL.CA(DC90)	DC input logic low	VSS	Vref - 0.090	VSS	Vref - 0.090	V	1
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	Vref + 0.150	Note 2	V	1, 2, 5
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	Note 2	Vref - 0.150	V	1, 2, 5
VIH.CA(AC130)	AC input logic high	Vref + 0.130	Note 2	Vref + 0.130	Note 2	V	1, 2, 5
VIL.CA(AC130)	AC input logic low	Note 2	Vref - 0.130	Note 2	Vref - 0.130	V	1, 2, 5
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefCA(DC).

NOTE 2 See JESD79-3, 9.6 “Overshoot and Undershoot Specifications” (9.6.1).

NOTE 3 The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 12.5 mV).

NOTE 4 For reference: approx. VDD/2 +/- 12.5 mV.

NOTE 5 These levels apply for 1.25 V operation only. If the device is operated at 1.35 V the appropriate levels in JESD79-3-1, VIH/L.CA(DC90), VIH/L.CA(AC160), VIH/L.CA(AC135), etc.) apply. The 1.35 V levels VIH/L.CA(DC90), VIH/L.CA(AC160), VIH/L.CA(AC135) etc.) do not apply when the device is operated in the 1.25 voltage range.

3.2 AC and DC Input Levels for Single-Ended Data Signals

Table 5 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3U-800, DDR3U-1066		DDR3U-1333, DDR3U-1600		Unit	Notes
		Min	Max				
VIH.DQ(DC90)	DC input logic high	Vref + 0.090	VDD	Vref + 0.090	VDD	V	1
VIL.DQ(DC90)	DC input logic low	VSS	Vref - 0.090	VSS	Vref - 0.090	V	1
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	Note 2	-	-	V	1, 2, 5
VIL.DQ(AC150)	AC input logic low	Note 2	Vref - 0.150	-	-	V	1, 2, 5
VIH.DQ(AC130)	AC input logic high	Vref + 0.130	Note 2	Vref + 0.130	Note 2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	Note 2	Vref - 0.130	Note 2	Vref - 0.130	V	1, 2, 5
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefDQ(DC).

NOTE 2 See JESD79-3, 9.6 “Overshoot and Undershoot Specifications” (9.6.1).

NOTE 3 The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 12.5 mV).

NOTE 4 For reference: approx. VDD/2 +/- 12.5 mV.

NOTE 5 These levels apply for 1.25 V operation only. If the device is operated at 1.35 V, the appropriate levels in JESD79-3-1 VIH/L.DQ(DC90), VIH/L.DQ (AC160), VIH/L.DQ(AC135), etc.) apply. The 1.35 V levels VIH/L.DQ(DC90), VIH/L.DQ(AC160), VIH/L.DQ(AC135), etc.) do not apply when the device is operated in the 1.25 voltage range.

3.3 1.25 V DDR3U Electrical Characteristics and AC Timing

Table 6 — Timing Parameters by Speed Bin[a]

Parameter	Symbol	DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing											
Data setup time to DQS, DQS# referenced to Vih.DQ(ac) / Vil.DQ(ac) levels	tDS(base) AC150	100		50		-		-		ps	Refer to JESD79-3 d, 17
Data hold time from DQS, DQS# referenced to Vih.DQ(dc) / Vil.DQ(dc) levels	tDH(base) DC90	160		110		75		55		ps	Refer to JESD79-3 d, 17
Data setup time to DQS, DQS# referenced to Vih.DQ(ac) / Vil.DQ(ac) levels	tDS(base) AC130	145		110		60		40		ps	Refer to JESD79-3 d, 17
Command and Address Timing											
Command and Address setup time to CK, CK# referenced to Vih.CA(ac) / Vil.CA(ac) levels	tIS(base) AC150	225		150		90		70		ps	Refer to JESD79-3 b, 16
Command and Address hold time from CK, CK# referenced to Vih.CA(dc) / Vil.CA(dc) levels	tIH(base) DC90	285		210		150		130		ps	Refer to JESD79-3 b, 16
Command and Address setup time to CK, CK# referenced to Vih.CA(ac) / Vil.CA(ac) levels	tIS(base) AC130	370	-	310	-	215		195		ps	Refer to JESD79-3 b, 16, 27
NOTE 1 The following general notes from page 20 apply to Table 6: NOTE 2 VDD =VDDQ = 1.25V ± 0.06V											

a. The setup and hold parameters in Table 6 apply for 1.25 V operation only. If the device is operated at 1.35 V, the respective parameters in JESD79-3-1 (tIS(base, AC160), tIS(base, AC135), tIH(base, DC90), tDS(base, AC 160), tDS(base, AC135), tDH(base, DC90) etc.) apply. The 1.35 V setup/hold parameters (tIS(base, AC160), tIS(base, AC135), tIH(base, DC90), tDS(base, AC160), tDS(base, AC135), tDH(base, DC 90) etc.) do not apply when the device is operated in the 1.25 voltage range

3.3 1.25 V DDR3U Electrical Characteristics and AC Timing (cont'd)

Table 7 — ADD/CMD Setup and Hold Base-Values for 1 V/ns

Unit [ps]	DDR3U-800	DDR3U-1066	DDR3U-1333	DDR3U-1600	Reference
tIS(base) AC150	225	150	90	70	$V_{IH/L.CA(ac)}$
tIH(base) DC90	285	210	150	130	$V_{IH/L.CA(dc)}$
tIS(base) AC130	225+145	150+160	90+125	70+125	$V_{IH/L.CA(ac)}$
NOTE (AC/DC referenced for 1 V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)					

3.4 Address / Command Setup, Hold and Derating

Table 8 — Derating values DDR3U-800/1066/1333/1600 tIS/tIH - ac/dc based AC150

ΔtIS, ΔtIH derating in [ps] AC/DC based AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV																
		CK,CK# Differential Slew Rate														
		4.0 V/ns		**3.0 V/ns**		**2.0 V/ns**		**1.8 V/ns**		**1.6 V/ns**		**1.4 V/ns**		**1.2 V/ns**		**1.0 V/ns**	
		ΔtIS	**ΔtIH**	**ΔtIS**	**ΔtIH**	**ΔtIS**	**ΔtIH**	**ΔtIS**	**ΔtIH**	**ΔtIS**	**ΔtIH**	**ΔtIS**	**ΔtIH**	**ΔtIS**	**ΔtIH**	**ΔtIS**	**ΔtIH**
CMD / ADD-Slew rate V/ns	**2.0**	75	45	75	45	75	45	81	53	87	61	93	69	99	79	105	95
	1.5	50	30	50	30	50	30	59	38	65	46	71	54	77	64	83	80
	1.0	0	0	0	0	0	0	8	8	16	16	22	24	28	34	34	50
	0.9	0	-3	0	-3	0	-3	8	5	16	13	24	21	30	31	36	47
	0.8	-1	-8	-1	-8	-1	-8	8	1	16	9	24	17	32	27	38	43
	0.7	0	-13	0	-13	0	-13	8	-5	16	3	24	11	32	21	40	37
	0.6	-1	-20	-1	-20	-1	-20	7	-12	15	-4	23	4	31	14	39	30
	0.5	-10	-30	-10	-30	-10	-30	-2	-22	6	-14	14	-6	22	4	30	20
	0.4	-25	-45	-25	-45	-25	-45	-12	-37	-9	-29	-1	-21	7	-11	15	5

3.4 Address / Command Setup, Hold and Derating (cont'd)

Table 9 — Derating values DDR3U-800/1066/1333/1600 tIS/tIH - AC/DC based AC130

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC130 Threshold -> VIH(ac)=VREF(dc)+130mV, VIL(ac)=VREF(dc)-130mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD- slew rate V/ns	**2.0**	65	45	65	45	65	45	71	53	77	61	83	69	89	79	95	95
	1.5	44	30	44	30	44	30	53	38	59	46	65	54	71	64	76	80
	1.0	0	0	0	0	0	0	8	8	16	16	22	24	28	34	34	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	33	31	39	47
	0.8	5	-8	5	-8	5	-8	13	1	21	9	29	17	37	27	43	43
	0.7	8	-13	8	-13	8	-13	16	-5	24	3	32	11	40	21	48	37
	0.6	12	-20	12	-20	12	-20	20	-12	28	-4	36	4	44	14	52	30
	0.5	10	-30	10	-30	10	-30	18	-22	26	-14	34	-6	42	4	50	20
	0.4	5	-45	5	-45	5	-45	13	-37	21	-29	29	-21	37	-11	45	5

Table 10 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 150mV [ps]		t_{VAC} @ 130mV [ps]	
	min	max	min	max
> 2.0	TBD	-	TBD	-
2.0	TBD	-	TBD	-
1.5	TBD	-	TBD	-
1.0	TBD	-	TBD	-
0.9	TBD	-	TBD	-
0.8	TBD	-	TBD	-
0.7	TBD	-	TBD	-
0.6	TBD	-	TBD	-
0.5	TBD	-	TBD	-
< 0.5	TBD	-	TBD	-

Table 11 — Data Setup and Hold Base-Values

Units [ps]	DDR3U-800	DDR3U-1066	DDR3U-1333	DDR3U-1600	Reference
tDS(base) AC150	100	50	-	-	$V_{IH/L.DQ(ac)}$
tDH(base) DC90	160	110	75	55	$V_{IH/L.DQ(dc)}$
tDS(base) AC130	145	110	60	40	$V_{IH/L.DQ(ac)}$
NOTE (AC/DC referenced for 1 V/ns DQ slew rate and 2 V/ns DQS slew rate)					

Table 12 — Derating values DDR3U-800/1066 tDS/tDH - ac/dc based AC150

ΔtDS, ΔDH derating in [ps] AC/DC based [a] AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	75	45	75	45	75	45	-	-	-	-	-	-	-	-	-	-
	1.5	50	30	50	30	50	30	59	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-3	0	-3	8	5	16	13	24	21	-	-	-	-
	0.8	-	-	-	-	-1	-8	8	1	16	9	24	17	32	27	-	-
	0.7	-	-	-	-	-	-	8	-5	16	3	24	11	32	21	40	37
	0.6	-	-	-	-	-	-	-	-	15	-4	23	4	31	14	39	30
	0.5	-	-	-	-	-	-	-	-	-	-	14	-6	22	4	30	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-11	15	-5

a.Cell contents shaded in red are defined as ‘not supported’.

Table 13 — Derating Values for DDR3U-800/1066/1333/1600 tDS/tDH - ac/dc based AC 130

ΔtDS, ΔDH derating in [ps] AC/DC based [a] Alternate AC125 Threshold -> VIH(ac)=VREF(dc)+125mV, VIL(ac)=VREF(dc)-125mV																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	65	45	65	45	65	45	-	-	-	-	-	-	-	-	-	-
	1.5	44	30	44	30	44	30	53	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	3	-3	3	-3	11	5	19	13	27	21	-	-	-	-
	0.8	-	-	-	-	5	-8	13	1	21	9	29	17	37	27	-	-
	0.7	-	-	-	-	-	-	16	-5	24	3	32	11	40	21	48	37
	0.6	-	-	-	-	-	-	-	-	28	-4	36	4	44	14	52	30
	0.5	-	-	-	-	-	-	-	-	-	-	34	-6	42	4	50	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	37	-11	45	5

a.Cell contents shaded in red are defined as ‘not supported’.

Table 14 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	DDR3U-800/1066 (AC150) t_{VAC} [ps]		DDR3U-800/1066/1333/1600 (AC130) t_{VAC} [ps]	
	min	max	min	max
> 2.0	TBD	-	TBD	-
2.0	TBD	-	TBD	-
1.5	TBD	-	TBD	-
1.0	TBD	-	TBD	-
0.9	TBD	-	TBD	-
0.8	TBD	-	TBD	-
0.7	TBD	-	TBD	-
0.6	TBD	-	TBD	-
0.5	TBD	-	TBD	-
< 0.5	TBD	-	TBD	-

3.5 1.25 V DDR3U Input/Output Capacitance

Table 15 — Input / Output Capacitance

		DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Input/output capacitance (DQ,DM,DQS,DQS#, TDQS,TDQS#)	C_{IO}	1.5	2.5	1.5	2.5	1.5	2.3	1.5	2.3	pF	1,2,3
Input capacitance, (CTRL, ADD, CMD input-only pins)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.3	pF	2,3,4

1.Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS

2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.25V, VBIAS=VDD/2 and on-die termination off.

3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

4. C_I applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.

3.6 1.25 V DDR3U Electrical Characteristics and AC Timing

Table 16 — Timing Parameter by Speed Bin

		DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Asynchronous RTT turn-on delay (Power-down with DLL frozen)	tAONPD	2	10	2	10	2	10	2	10	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	10	2	10	2	10	2	10	ns	

3.7 1.25 V DDR3U Output Driver DC Electrical Characteristics

Table 17 — Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω ; entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.2	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.85	1.0	1.2	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.5	R_{ZQ}/7	1, 2, 3
	RON_{34Pu}	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.5	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.85	1.0	1.2	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.2	R_{ZQ}/7	1, 2, 3
40 Ω	RON_{40Pd}	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.2	R_{ZQ}/6	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.85	1.0	1.2	R_{ZQ}/6	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.5	R_{ZQ}/6	1, 2, 3
	RON_{40Pu}	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.5	R_{ZQ}/6	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.85	1.0	1.2	R_{ZQ}/6	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.2	R_{ZQ}/6	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5 × V_{DDQ}	-12		+12	%	1, 2, 4

Notes:1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

2. The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.

3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 ´ V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 ´ V_{DDQ} and 0.8 ´ V_{DDQ}.

4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}: Measure RON_{Pu} and RON_{Pd}, both at 0.5 * V_{DDQ}:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

3.8 1.25 V DDR3U On-Die Termination (ODT) Levels and I-V Characteristics

Table 18 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 W +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	$RTT_{120Pd240}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.2	R_{ZQ}	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.85	1.00	1.2	R_{ZQ}	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.5	R_{ZQ}	1, 2, 3, 4,
		$RTT_{120Pu240}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.5	R_{ZQ}	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.85	1.00	1.2	R_{ZQ}	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.2	R_{ZQ}	1, 2, 3, 4,
		RTT_{120}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.7	$R_{ZQ}/2$	1, 2, 5,
0, 0, 1	60 Ω	$RTT_{60Pd120}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.2	$R_{ZQ}/2$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.85	1.00	1.2	$R_{ZQ}/2$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.5	$R_{ZQ}/2$	1, 2, 3, 4,
		$RTT_{60Pu120}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.5	$R_{ZQ}/2$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.85	1.00	1.2	$R_{ZQ}/2$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.2	$R_{ZQ}/2$	1, 2, 3, 4,
		RTT_{60}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.7	$R_{ZQ}/4$	1, 2, 5,

Table 18 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 W +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 1	40 Ω	RTT_{40Pd80}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.2	$R_{ZQ}/3$	1, 2, 3, 4,
			0.5 × V_{DDQ}	0.85	1.00	1.2	$R_{ZQ}/3$	1, 2, 3, 4,
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.5	$R_{ZQ}/3$	1, 2, 3, 4,
		RTT_{40Pu80}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.5	$R_{ZQ}/3$	1, 2, 3, 4,
			0.5 × V_{DDQ}	0.85	1.00	1.2	$R_{ZQ}/3$	1, 2, 3, 4,
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.2	$R_{ZQ}/3$	1, 2, 3, 4,
		RTT_{40}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.7	$R_{ZQ}/6$	1, 2, 5,
1, 0, 1	30 Ω	RTT_{30Pd60}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.2	$R_{ZQ}/4$	1, 2, 3, 4,
			0.5 × V_{DDQ}	0.85	1.00	1.2	$R_{ZQ}/4$	1, 2, 3, 4,
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.5	$R_{ZQ}/4$	1, 2, 3, 4,
		RTT_{30Pu60}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.5	$R_{ZQ}/4$	1, 2, 3, 4,
			0.5 × V_{DDQ}	0.85	1.00	1.2	$R_{ZQ}/4$	1, 2, 3, 4,
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.2	$R_{ZQ}/4$	1, 2, 3, 4,
		RTT_{30}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.7	$R_{ZQ}/8$	1, 2, 5,
1, 0, 0	20 Ω	RTT_{20Pd40}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.2	$R_{ZQ}/6$	1, 2, 3, 4,
			0.5 × V_{DDQ}	0.85	1.00	1.2	$R_{ZQ}/6$	1, 2, 3, 4,
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.5	$R_{ZQ}/6$	1, 2, 3, 4,
		RTT_{20Pu40}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.5	$R_{ZQ}/6$	1, 2, 3, 4,
			0.5 × V_{DDQ}	0.85	1.00	1.2	$R_{ZQ}/6$	1, 2, 3, 4,
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.2	$R_{ZQ}/6$	1, 2, 3, 4,
		RTT_{20}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.7	$R_{ZQ}/12$	1, 2, 5,
Deviation of V_M w.r.t. $V_{DDQ}/2$, DV_M				-6		+6	%	1, 2, 5, 6,

Notes:1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see JESD79-3 section on voltage and temperature sensitivity.

2.The tolerance limits are specified under the condition that V_{DDQ} = V_{DD} and that V_{SSQ} = V_{SS}.

3.Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 ´ V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.2 ´ V_{DDQ} and 0.8 ´ V_{DDQ}.

4.Not a specification requirement, but a design guide line.

5.Measurement definition for *RTT*:
Apply $V_{IH(ac)}$ to pin under test and measure current $I(V_{IH(ac)})$, then apply $V_{IL(ac)}$ to pin under test and measure current $I(V_{IL(ac)})$ respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(VIH(ac)) - I(VIL(ac))}$$

6.Measurement definition for V_M and DV_M:
Measure voltage (V_M) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1\right) \times 100$$

Table 19 — Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	R_{ZQ}/4	NA	0.05	0.10	
	R_{ZQ}/12	NA	0.10	0.20	
t_{AONPD}	R_{ZQ}/4	NA	0.05	0.10	
	R_{ZQ}/12	NA	0.10	0.20	
t_{AOF}	R_{ZQ}/4	NA	0.05	0.10	
	R_{ZQ}/12	NA	0.10	0.20	
t_{AOFPD}	R_{ZQ}/4	NA	0.05	0.10	
	R_{ZQ}/12	NA	0.10	0.20	
t_{ADC}	R_{ZQ}/12	R_{ZQ}/2	0.20	0.25	

3.9 1.25 V DDR3U Single Ended Output Slew Rate

Table 20 — Output Slew Rate (single-ended)

		DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	1.75[2)]	5[1)]	1.75[2)]	5[1)]	1.75[2)]	5[1)]	1.75[2)]	5[1)]	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Note 1): In two cases, a maximum slew rate of 6 V/ns applies for a single DQ signal within a byte lane.
Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
Case_2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.
Note 2): The minimum spec of 1.5 V/ns is ok if DRAM input/output capacitance Cio max is less than 2.2 pF.

3.10 1.25 V Differential Output Slew Rate

Table 21 — Differential Output Slew Rate

		DDR3U-800		DDR3U-1066		DDR3U-1333		DDR3U-1600		Units
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Differential Output Slew Rate	SRQdiff	3.5[1)]	12	3.5[1)]	12	3.5[1)]	12	3.5[1)]	12	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

For Ron = RZQ/7 setting

Note 1) The minimum spec of 3.0 V/ns is ok if DRAM input/output capacitance Cio max is less than 2.2 pF.

3.11 1.25 V DDR3U AC and DC Logic Input Levels for Differential Signals

Table 22 — Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

Symbol	Parameter	DDR3U-800, 1066, 1333, & 1600		Unit	Notes
		Min	**Max**		
V_{IHdiff}	Differential input high	+ 0.180	note 3	V	1
V_{ILdiff}	Differential input logic low	Note 3	- 0.180	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (VIL(ac) - Vref)	V	2

1. Used to define a differential signal slew-rate.

2. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to JESD79-3, “Overshoot and Undershoot Specifications”.

Table 23 — Allowed time before ringback (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV		tDVAC [ps] @ |VIH/Ldiff(ac)| = 260mV	
	min	max	min	max
> 4.0	TBD	-	TBD	-
4.0	TBD	-	TBD	-
3.0	TBD	-	TBD	-
2.0	TBD	-	TBD	-
1.8	TBD	-	TBD	-
1.6	TBD	-	TBD	-
1.4	TBD	-	TBD	-
1.2	TBD	-	TBD	-
1.0	TBD	-	TBD	-
< 1.0	TBD	-	TBD	-


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