JEDEC STANDARD

POD18 - 1.8 V Pseudo Open Drain I/O

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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POD18 - 1.8 V PSEUDO OPEN DRAIN I/O

(From JEDEC Board Ballot JCB-06-27, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.8 V Pseudo Open Drain I/Os. The 1.8 V Pseudo Open Drain interface, also known as POD18, is primarily used to communicate with GDDR3 SGRAM devices.

2 Operating conditions

Table 1 — DC Electrical Characteristics and Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.7	1.8	1.9	V
I/O Supply Voltage	VDDQ	1.7	1.8	1.9	V
I/O Reference Voltage	VREF	0.69 * VDDQ	0.70 * VDDQ	0.71 * VDDQ	V
Input High (Logic 1) Voltage	VIH (DC)	VREF + 0.15	-		V
Input Low (Logic 0) Voltage	VIL (DC)	-	-	VREF - 0.15	V
Input Leakage Current Any Input 0V <= V_{IN} <= VDD (All other pins not under test = 0V)	Il	-5	-	5	µA
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz	-5	-	5	µA
Output Logic LOW	VOL (DC)	-	-	0.76	V

Table 2 — AC Input Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input High (Logic 1) Voltage; DQ	VIH (AC)	VREF + 0.250	-	-	V
Input Low (Logic 0) Voltage; DQ	VIL (AC)	-	-	VREF - 0.250	V
Clock Input Differential Voltage; CK & CK#	VID (AC)	0.5	-	VDDQ + 0.5	V
Clock Input Crossing Point Voltage; CK & CK#	VIX (AC)	VREF - 0.15	0.70 * VDDQ	VREF + 0.15	V

2 Operating conditions (cont'd)

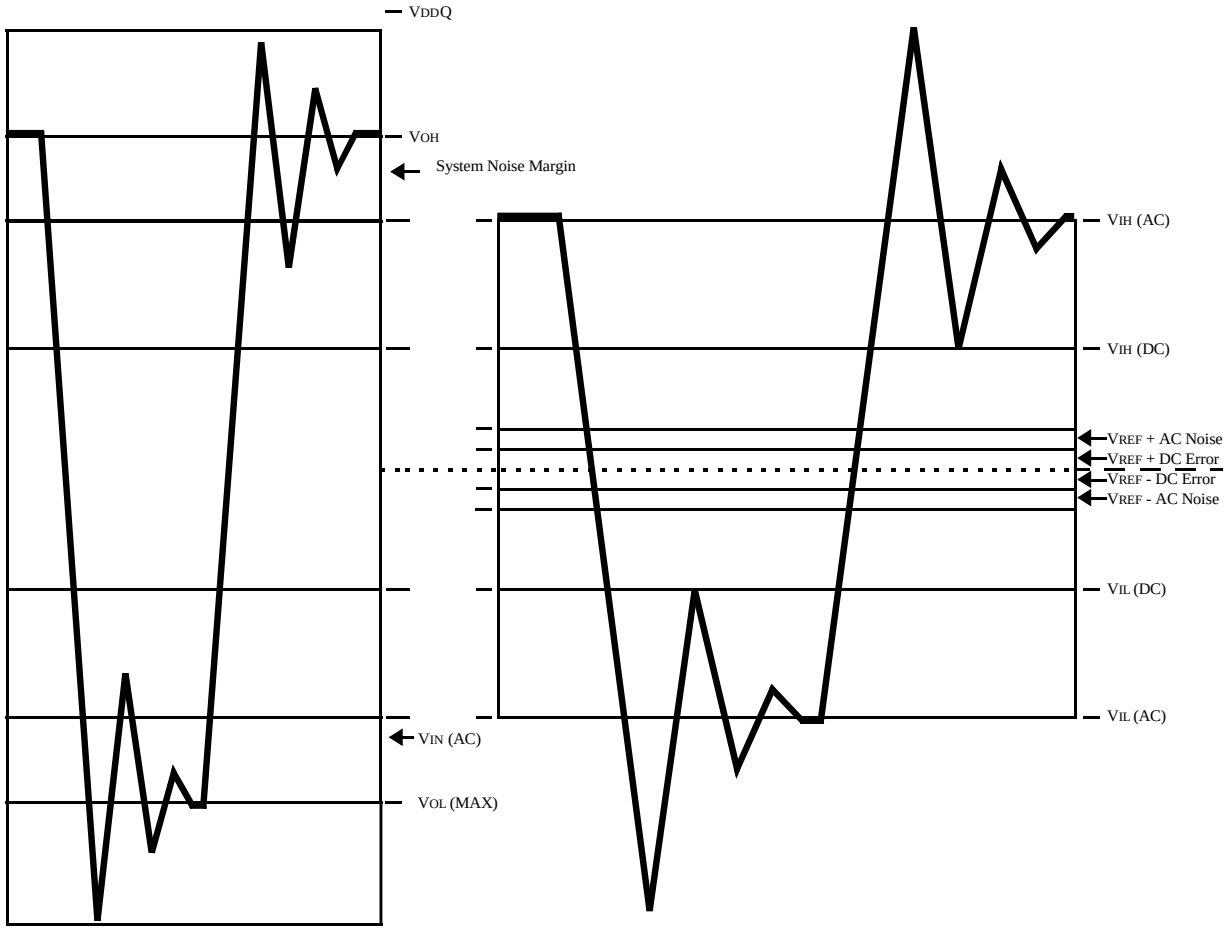


Figure 1 — Input and Output Voltage Waveform

2 Operating conditions (cont'd)

Table 3 — Clock Input Operating Conditions

Parameter	Symbol	Min		Max	Unit
Clock Input Mid-Point Voltage ; CK and CK#	VMP (DC)	1.16	1.26	1.36	V
Clock Input Voltage Level; CK and CK#	VIN(DC)	0.42		VDDQ + 0.3	V
Clock Input Differential Voltage ; CK and CK#	VID (DC)	0.22		VDDQ	V
Clock Input Differential Voltage ; CK and CK#	VID (AC)	0.5		VDDQ + 0.5	V
Clock Input Crossing Point Voltage ; CK and CK#	VIX (AC)	VREF - 0.15	0.70 * VDDQ	VREF + 0.15	V

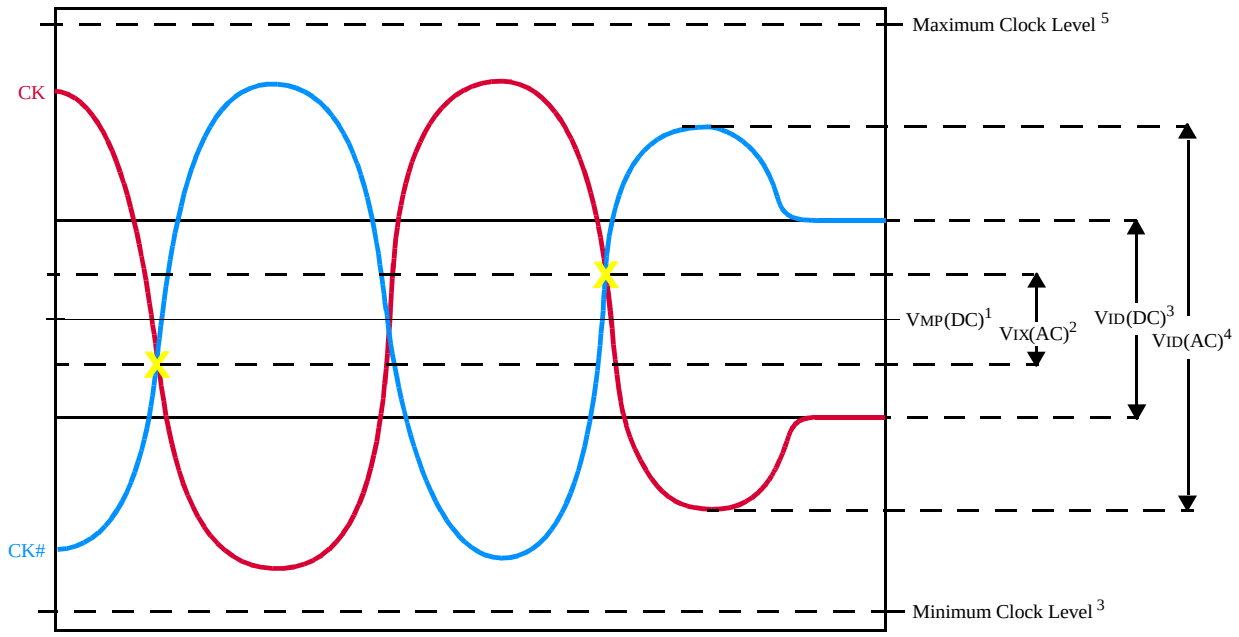


Figure 2 — Clock Input Waveform

NOTE 1 This provides a minimum of 1.16V to a maximum of 1.36V, and is always 70% of VDDQ.

NOTE 2 CK and CK# must cross in this region.

NOTE 3 CK and CK# must meet at least VIN(DC) MIN when static and is centered around VMP(DC).

NOTE 4 CK and CK# must have a minimum 500mV peak-ot-peak swing.

NOTE 5 CK and CK# may not be more positive than VDDQ + 0.3V or lower than 0.42V

NOTE 6 For AC operations, all DC clock requirements must be satisfied

NOTE 7 Numbers in diagram reflect nominal values.

2 Operating conditions (cont'd)

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1) Nominal 1.8V (VDD/VDDQ)
2) Power the device and calibrate the output drivers & termination to eliminate process variation at 25 °C.
3) Reduce temperature to 10 °C recalibrate.
4) Reduce temperature to 0 °C and take the fast corner measurement.
5) Raise temperature to 75 °C and recalibrate
6) Raise temperature to 85 °C and take the slow corner measurement

Table 4 — 40 Ohm Drive Characteristics

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN(mA)	MAX(mA)
0.1	2.144	3.366
0.2	4.268	6.516
0.3	6.373	9.454
0.4	8.449	12.185
0.5	10.505	14.715
0.6	12.542	17.051
0.7	14.540	19.400
0.8	16.509	21.828
0.9	18.449	24.219
1.0	20.341	26.580
1.1	22.203	28.913
1.2	24.017	31.222
1.3	25.783	33.508
1.4	27.480	35.813
1.5	29.119	38.213
1.6	30.671	40.551
1.7	31.387	42.900
1.8	31.648	45.176

Pull-Up Characteristic at 40 ohms		
Voltage (V)	MIN(mA)	MAX(mA)
0.1	-2.377	-2.946
0.2	-4.705	-5.829
0.3	-6.984	-8.644
0.4	-9.283	-11.383
0.5	-11.524	-14.038
0.6	-13.803	-16.599
0.7	-16.015	-19.051
0.8	-18.285	-21.630
0.9	-20.302	-24.143
1.0	-22.223	-26.605
1.1	-24.066	-29.005
1.2	-25.773	-31.353
1.3	-27.344	-33.619
1.4	-28.683	-35.803
1.5	-29.731	-37.883
1.6	-30.691	-39.882
1.7	-31.544	-42.003
1.8	-32.311	-44.063

2 Operating conditions (cont'd)

Table 5 — On Die Termination Values

Pull-Up Characteristic at 60 ohms		
Voltage (V)	**MIN (mA)**	**MAX (mA)**
0.1	-1.58	-1.96
0.2	-3.14	-3.89
0.3	-4.66	-5.76
0.4	-6.19	-7.59
0.5	-7.68	-9.36
0.6	-9.20	-11.07
0.7	-10.68	-12.70
0.8	-12.19	-14.42
0.9	-13.53	-16.10
1.0	-14.82	-17.74
1.1	-16.04	-19.34
1.2	-17.18	-20.90
1.3	-18.23	-22.41
1.4	-19.12	-23.87
1.5	-19.82	-25.26
1.6	-20.46	-26.59
1.7	-21.03	-28.00
1.8	-21.54	-29.38

Pull-Up Characteristic at 120 ohms		
Voltage (V)	**MIN (mA)**	**MAX (mA)**
0.1	-0.79	-0.98
0.2	-1.57	-1.94
0.3	-2.33	-2.88
0.4	-3.09	-3.79
0.5	-3.84	-4.68
0.6	-4.60	-5.53
0.7	-5.34	-6.35
0.8	-6.09	-7.21
0.9	-6.77	-8.05
1.0	-7.41	-8.87
1.1	-8.02	-9.67
1.2	-8.59	-10.45
1.3	-9.11	-11.21
1.4	-9.56	-11.93
1.5	-9.91	-12.63
1.6	-10.23	-13.29
1.7	-10.51	-14.00
1.8	-10.77	-14.69

Pull-Up Characteristic at 240 ohms		
Voltage (V)	**MIN (mA)**	**MAX (mA)**
0.1	-0.40	-0.49
0.2	-0.78	-0.97
0.3	-1.16	-1.44
0.4	-1.55	-1.90
0.5	-1.92	-2.34
0.6	-2.30	-2.77
0.7	-2.67	-3.18
0.8	-3.05	-3.60
0.9	-3.38	-4.02
1.0	-3.70	-4.43
1.1	-4.01	-4.83
1.2	-4.30	-5.23
1.3	-4.56	-5.60
1.4	-4.78	-5.97
1.5	-4.96	-6.31
1.6	-5.12	-6.65
1.7	-5.26	-7.00
1.8	-5.39	-7.34

3 Additional Background Information

The POD18 I/O system is optimized for small systems with data rates up to 2.0 Gbps. The system allows a single Master device to control one, two or four slave devices. The POD18 driver uses a 40 Ohm output impedance that drives into a 60 Ohm equivalent terminator tied to VDDQ. Single, dual and quad load systems are shown as follows:

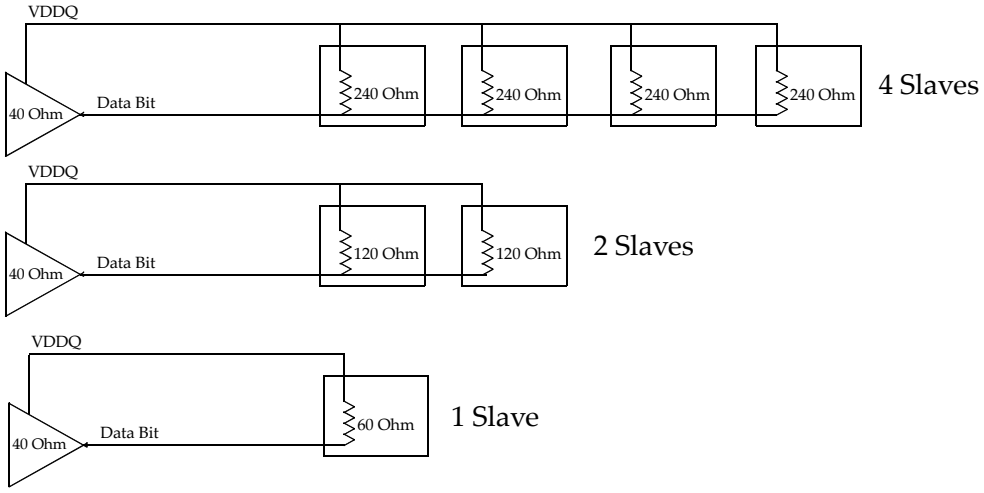


Figure 3 — System Configurations

The POD18 Master I/O cell is comprised of a 40 Ohm driver and a terminator of 60 Ohms. The Master POD18 cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 4.

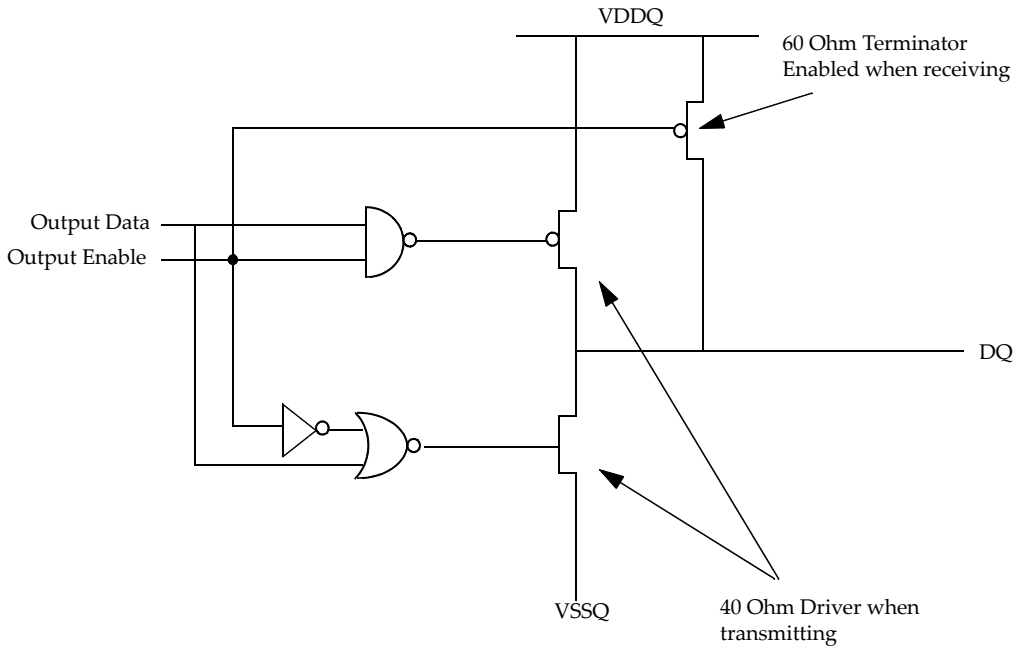


Figure 4 — Master I/O Cell

3 Additional Background Information (cont'd)

The POD18 Slave I/O cell is comprised of a 40 ohm driver and programmable terminator of 60, 120 or 240 ohms. The Slave POD18 cell's terminator is disabled when the output driver is enabled or any other Slave output driver is enabled. The basic cell is shown in Figure 5.

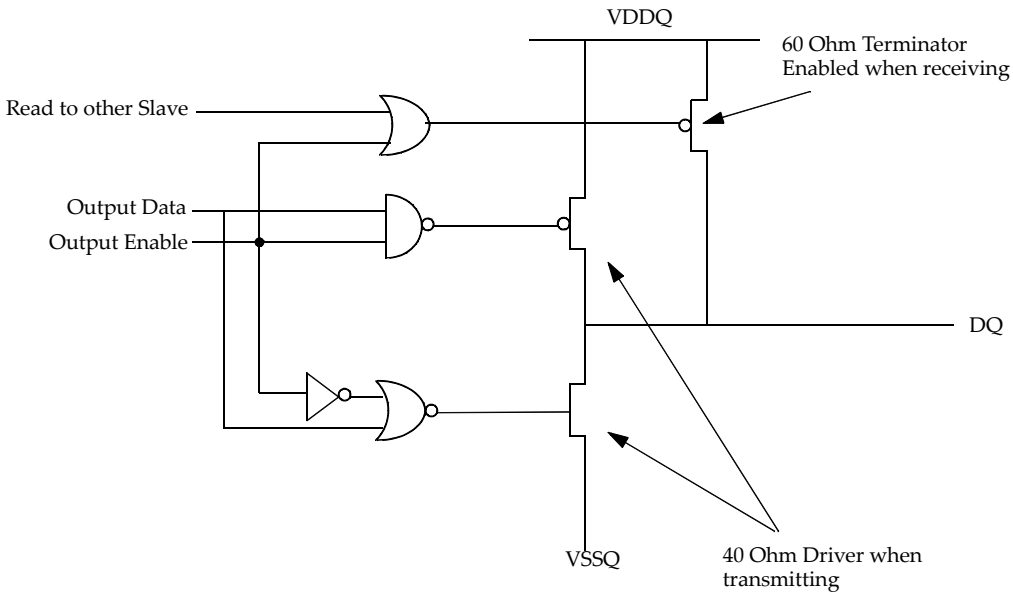


Figure 5 — Slave I/O Cell

The POD18 Master and Slave I/O cells are intended to have their driver and terminators combined together to minimize the area needed to implement the cell and reduce input capacitance. This is possible by using six 240 Ohm driver/terminator sub cells that are connected in parallel. The combinations used are as follows.

Table 6 — POD18 I/O Sub Cells

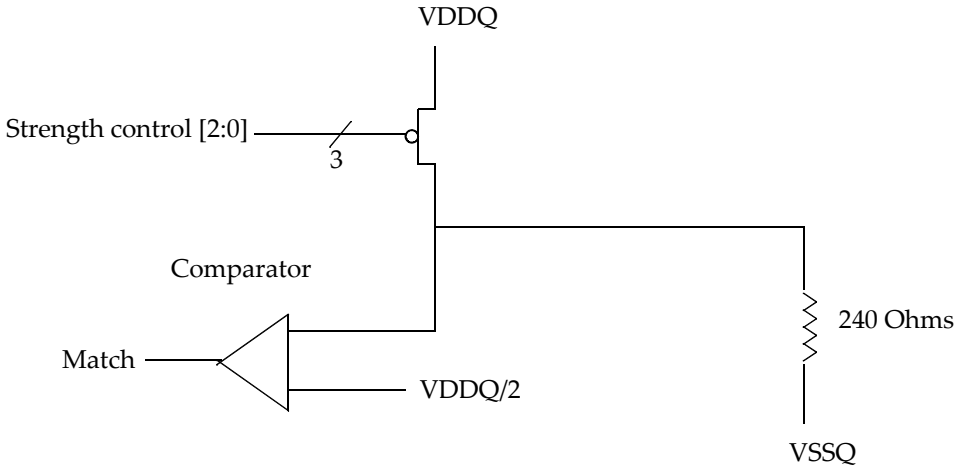
# of 240 ohm sub cells enabled	Resulting Impedance	Use
1	240 Ohms	4 Slave loads
2	120 Ohms	2 Slave loads
4	60 Ohms	1 Slave load or Master terminator
6	40 Ohms	Master or Slave Driver

3 Additional Background Information (cont'd)

To ensure that the target impedance is achieved the POD18 I/O cell is designed to be calibrated to an external 1% precision resistor.

The following procedure may be used to calibrate the cell:

1) First calibrate the PMOS device against a 240 Ohm resister to VSS via the ZQ pin as illustrated in Figure 6.
   - •Set Strength Control to minimum setting
   - •Increase drive strength until comparator detects data bit is greater than VDDQ/2
   - •PMOS device is calibrated to 240 Ohms
2) Then calibrate the NMOS device against the calibrated 240 Ohm PMOS device as illustrate in Figure 7
   - •Set Strength Control to minimum setting
   - •Increase drive strength until comparator detects data bit is less than VDDQ/2
   - •NMOS device is now calibrated to 240 Ohms.



When Match PMOS leg is calibrated to 240 ohms

Figure 6 — PMOS Calibration

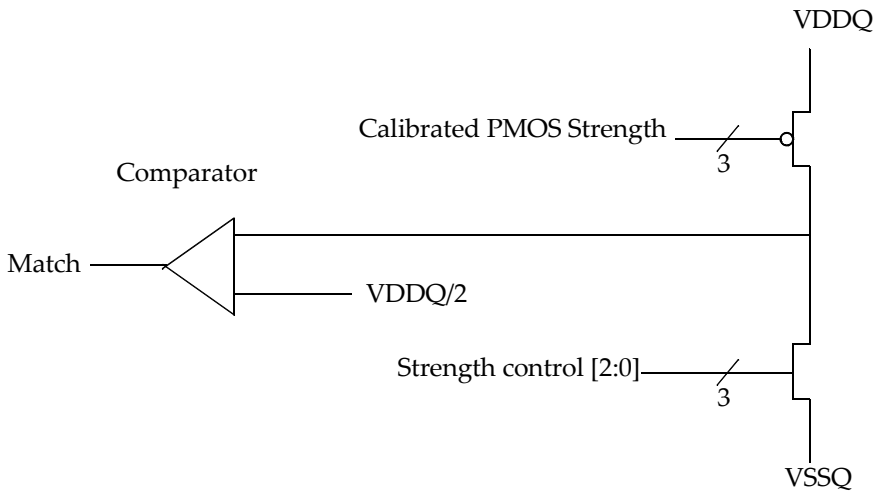


Figure 7 — NMOS Calibration

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