JEDEC STANDARD

POD10 - 1.0 V PSEUDO OPEN DRAIN INTERFACE

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POD10 - 1.0 V PSEUDO OPEN DRAIN INTERFACE

(From JEDEC Board Ballot JCB-11-45, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This document defines the 1.0 V Pseudo Open Drain Interface family of interface standards, POD10, which are generally expected to be implemented with differential amp-based input buffers that, when in single-ended mode, employ an externally supplied (or internal supplied) reference voltage controlled trip-point.

Although this specification is named for the nominal value of VDDQ to be used, it is the input trip-point value that provides for inter operability of POD10 compliant devices. Physics dictates variations in output driver characteristics and termination values in different interconnect network topologies. Drivers and terminators appropriate in a point-to-point interconnect scheme are not necessarily suitable in a multi-drop bus application. Multiple Classes of POD10 are expected to reside within the family of POD10 interfaces in order to accommodate various device and market applications. The various classes standardized within the context of POD10 are documented in the appendices of this document (e.g. POD10/Class A, POD10/Class B, POD10/Class C, etc.)

In all cases, drivers and terminators are expected to produce a roughly symmetric swing about the input trip-point of POD10 receivers. Unlike the signals on other interfaces, such as HSTL, that are designed to produce signals that swing symmetrically about VDDQ/2, the signals on a POD10 interconnect line are not generally expected to pull to VSS. POD10 input buffers are generally expected to be supported by pull-up-only parallel input termination. POD10 output drivers are therefore expected to demonstrate an asymmetric output drive impedance. In point-to-point applications, for example, if the output drivers were expected to demonstrate a nominal 60 ohm pull-up drive impedance then the pull-down drivers would be expected to produce a 40 ohm pull-down drive impedance.

The core of this standard defines the dc and ac single-ended and differential operating conditions for POD10 input buffers as well as the terms and definitions necessary to describe the characteristics and behavior of output drivers. Section 2 in this document documents the subset of values common to all Classes of POD10 and documents specification items left to definition within a specific Class. The values specific to each particular class of POD10 are found in the appendices. (Note it does not follow that all specification values defined in a given Class are necessarily different from the matching parameter in other Class within POD10. Multiple Classes may reuse a given specification value if appropriate to the Class requirements.)

Inasmuch as additional classes may be added to this specification at the will of the authorizing committee and the JEDEC Board of Directors, the reader is advised to check the JEDEC website (http://www.jedec.org) for the latest release of the specification.

2 Core POD10 interface specifications

Table 2-1 — DC operating conditions

Parameter	Symbol	POD10			Unit	Note
		Min	Typ	Max		
Device Supply Voltage	VDD	n/a	n/a	n/a	V	1
Output Supply Voltage	VDDQ	CDV	1.0	CDV	V	2
Reference Voltage	VREF	CDV	CDV	CDV	V	3
DC Input Logic HIGH Voltage	VIH (DC)	CDV		CDV	V	
DC Input Logic LOW Voltage	VIL (DC)	CDV		CDV	V	
Input Leakage Current Any Input 0 V <= V_{IN} <= VDDQ (All other pins not under test = 0 V)	II				µA	4
Output Leakage Current (DQs are disabled; 0 V <= Vout <= VDDQ)	Ioz				µA	4
Output Logic LOW Voltage	VOL (DC)			0.42	V	

NOTE 1 The POD10 interface may be implemented on any device without regard to VDD. Although VDD can generally be expected to greater than or equal to VDDQ, compliant devices may support VDD values lower than VDDQ.

NOTE 2 POD10 compliant devices are expected to tolerate PCB designs with separate VDD and VDDQ power regulators.

NOTE 3 The source of Reference Voltage and control of Reference Voltage, and association of Reference Voltage with specific I/O pins may be determined control mechanisms specified by the device vendor.

NOTE 4 These parameters are expected to be standardized by product type and are therefore left blank intentionally here.

Notice: CDV means Class Dependent Value. See specific Class tables for further details.

Table 2-2 — AC operating conditions.

Parameter	Symbol	POD10			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage	VIH (AC)	CDV			V	
AC Input Logic Low Voltage	VIL (AC)			CDV	V	

Notice: CDV means Class Dependent Value. See specific Class tables for further details.

2 Core POD10 interface specifications (cont'd)

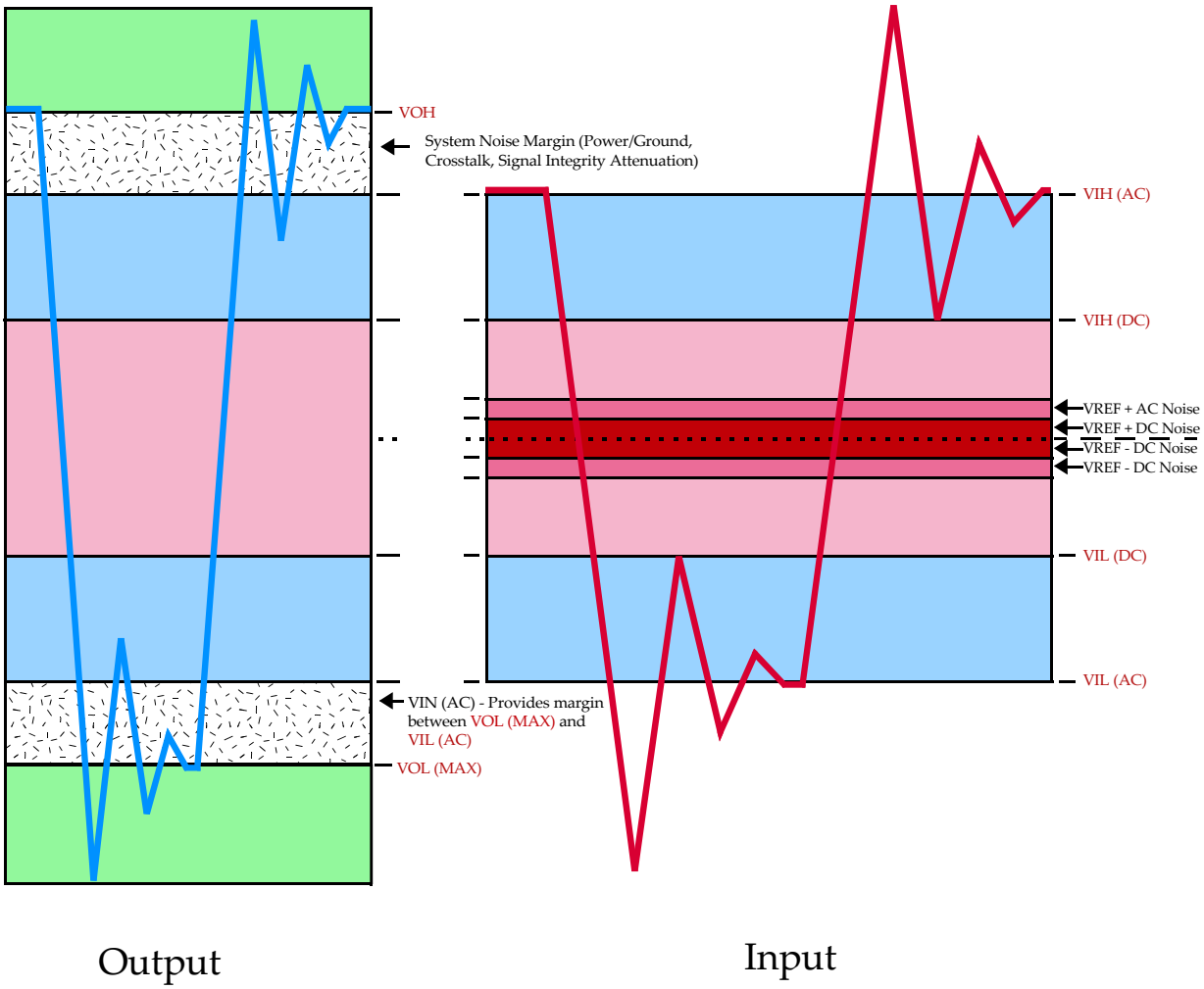

Figure 2-1 — Voltage waveform

2 Core POD10 interface specifications (cont'd)

Table 2-3 — Differential input operating conditions

Parameter	Symbol	POD10		Unit	Note
		Min	Max		
Dif Input Mid-Point Voltage; Pin and Pin#	VMP (DC)	CDV	CDV	V	1
Dif Input Differential Voltage; Pin and Pin#	VID (DC)	CDV		V	1, 3
Dif Input Differential Voltage; Pin and Pin#	VID (AC)	CDV		V	1, 2, 3
Single-ended Input Voltage; Pin and Pin#	VIN	CDV	CDV	V	1
Single-ended Input Voltage Slew Rate; Pin and Pin#	VINS	CDV		V/ns	4
Dif Input Crossing Point Voltage; Pin and Pin#	VIX (AC)	CDV	CDV	V	2
Allowed time before ringback to VID (AC)	t_{DVAC}			ps	2, 9

NOTE 1 "Pin" and "Pin#" represent the true and compliment pins of a differential input pair.
NOTE 2 For AC operations, all DC requirements must be satisfied as well.
NOTE 3 VID is the magnitude of the difference between the input level in Pin and the input level on Pin#.
NOTE 4 The slew rate is measured between VREF crossing and VIX (AC).
NOTE 5 The Pin and Pin# input reference level (for timing referenced to Pin and Pin#) is the point at which Pin and Pin# cross.
NOTE 6 Figure 2-3: illustrates the exact relationship between (Pin-Pin#) and VID(AC), VID(DC) and t_{DVAC}
NOTE 7 Ringback voltage on Pin or Pin# below VID(DC) is not allowed.
NOTE 8 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of Pin operating conditions and Pin related parameters.
NOTE 9 This parameter is expected to be standardized by product type and is therefore left blank intentionally here.

Notice: CDV means Class Dependent Value. See specific Class tables for further details.

2 Core POD10 interface specifications (cont'd)

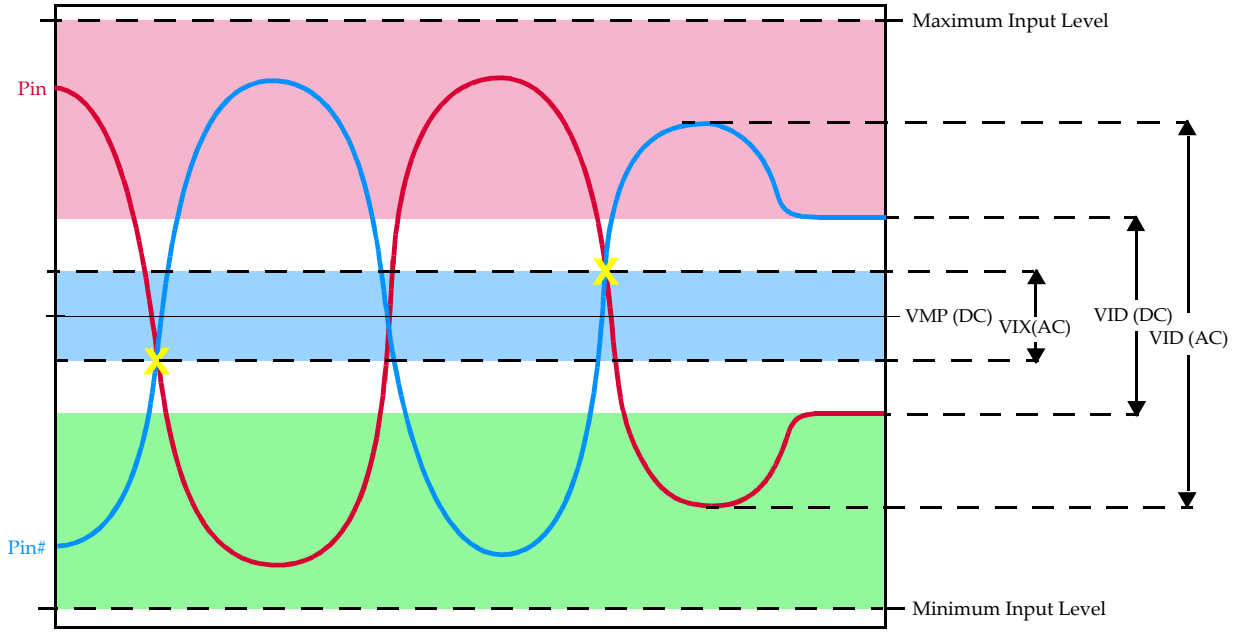

Figure 2-2 — Pin waveform

2 Core POD10 interface specifications (cont'd)

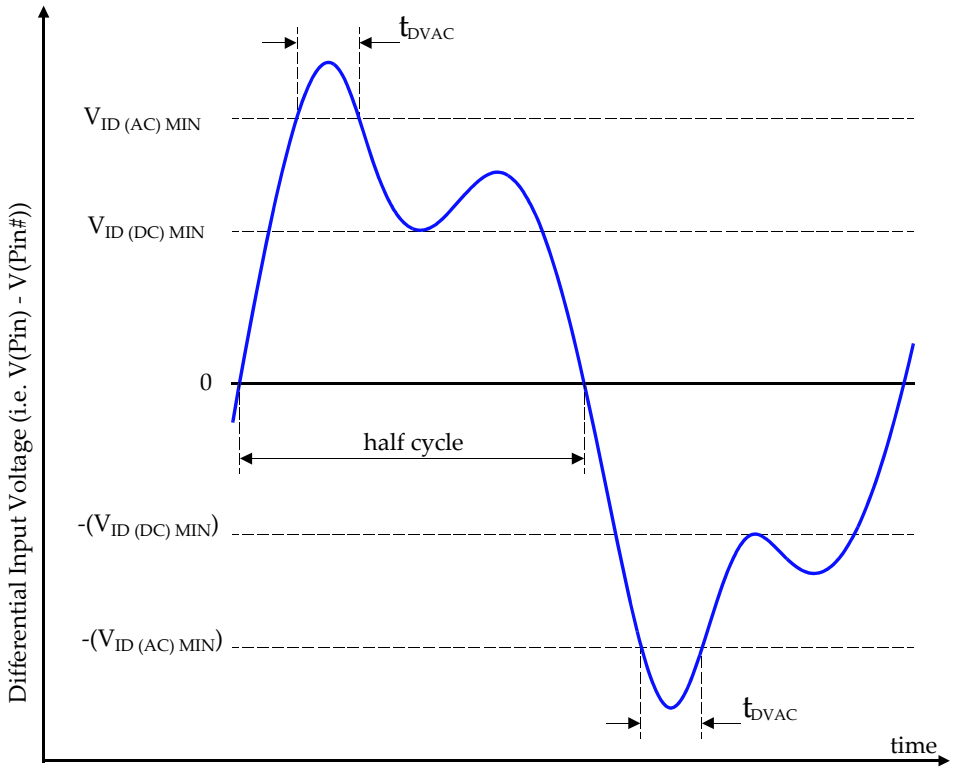

Figure 2-3 — Definition of differential ac-swing and "time above ac-level" t_{DVAC}

The Driver and Termination impedances should be characterized under the following test conditions:

1) Set VDDQ to Nominal.
2) Power the compliant device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3) Reduce temperature to the device low operating temperature limit plus 10 °C and recalibrate.
4) Reduce temperature to low operating temperature limit and take the fast corner measurement.
5) Raise temperature to the device high operating temperature limit minus 10 °C and recalibrate.
6) Raise temperature to high operating temperature limit and take the slow corner measurement.
7) Reiterate 2 to 6 with VDDQ at Max limit.
8) Reiterate 2 to 6 with VDDQ at Min limit.

3 Drive strength and termination issues

Inasmuch as the POD10 interface can be useful for interconnecting many sorts of high speed devices, operating in significantly divergent price/performance and power domains, compliant devices are not required to offer on-die input termination. Nevertheless on-die input termination is expected to be the norm for POD10 compliant devices.

In order to achieve sufficient precision in drive strength and termination impedance over process, temperature and voltage variations, compliant devices are generally expected to implement some sort of impedance control scheme on output drivers and on-die input terminators, if present. Best practices dictate drivers and terminators maintain their target impedance (+/- 20% or better) over a voltage of VDDQ * 0.20 to VDDQ * 0.80. Specific device types with particular interface speed requirements are expected to establish specific control schemes and precision requirements within the POD10 framework that are appropriate to their target applications.

Annex A (normative) POD10/Class A

POD10/Class A is intended for point-to-point interconnect applications.

Table A-1 — DC operating conditions

Parameter	Symbol	POD10			Unit	Note
		Min	Typ	Max		
Device Supply Voltage	VDD	n/a	n/a	n/a	V	1
Output Supply Voltage	VDDQ	0.97	1.0	1.03	V	2
Reference Voltage	VREF	0.69 * VDDQ	0.70 * VDDQ	0.71 * VDDQ	V	3, 4
DC Input Logic HIGH Voltage	VIH (DC)	VREF + 0.07		VDDQ + 0.12	V	
DC Input Logic LOW Voltage	VIL (DC)	-0.12		VREF - 0.07	V	
Input Leakage Current Any Input 0V <= V_{IN} <= VDDQ (All other pins not under test = 0V)	II				µA	5
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz				µA	5
Output Logic LOW Voltage	VOL (DC)			0.42	V	

NOTE 1 The POD10 interface may be implemented on any device without regard to VDD. Although VDD can generally be expected to greater than or equal to VDDQ, compliant devices may support VDD values lower than VDDQ.

NOTE 2 POD10 compliant devices are expected to tolerate PCB designs with separate VDD and VDDQ power regulators.

NOTE 3 The design of POD10 anticipates boards that use POD10 compliant devices will control AC noise to 50 mV pk-pk or less.

NOTE 4 The source of Reference Voltage and control of Reference Voltage, and association of Reference Voltage with specific I/O pins may be determined control mechanisms specified by the device vendor.

NOTE 5 These parameters are expected to be standardized by product type and are therefore left blank intentionally here.

Table A-2 — AC operating conditions

Parameter	Symbol	POD10			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage	VIH (AC)	VREF + 0.13			V	
AC Input Logic Low Voltage	VIL (AC)			VREF - 0.13	V	

Annex A (normative) POD10/Class A (cont'd)

Table A-3 — Differential input operating conditions

Parameter	Symbol	POD10		Unit	Note
		Min	Max		
Dif Input Mid-Point Voltage; Pin and Pin#	VMP (DC)	VREF - 0.07	VREF + 0.07	V	1
Dif Input Differential Voltage; Pin and Pin#	VID (DC)	0.14		V	1, 3
Dif Input Differential Voltage; Pin and Pin#	VID (AC)	0.26		V	1, 2, 3
Single-ended Input Voltage; Pin and Pin#	VIN	0.23	VDDQ + 0.12	V	1
Single-ended Input Voltage Slew Rate; Pin and Pin#	VINS	3		V/ns	4
Dif Input Crossing Point Voltage; Pin and Pin#	VIX (AC)	VREF - 0.07	VREF + 0.07	V	2
Allowed time before ringback to VID (AC)	t_{DVAC}			ps	2, 9

Notes:

NOTE 1 "Pin" and "Pin#" represent the true and compliment pins of a differential input pair.
NOTE 2 For AC operations, all DC requirements must be satisfied as well.
NOTE 3 VID is the magnitude of the difference between the input level in Pin and the input level on Pin#.
NOTE 4 The slew rate is measured between VREF crossing and VIX (AC).
NOTE 5 The Pin and Pin# input reference level (for timing referenced to Pin and Pin#) is the point at which Pin and Pin# cross.
NOTE 6 Figure 2-3: illustrates the exact relationship between (Pin-Pin#) and VID(AC), VID(DC) and t_{DVAC}
NOTE 7 Ringback voltage on Pin or Pin# below VID(DC) is not allowed.
NOTE 8 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of Pin operating conditions and Pin related parameters.
NOTE 9 This parameter is expected to be standardized by product type and is therefore left blank intentionally here.

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