JEDEC STANDARD

1.2 V HIGH-SPEED LVCMOS (HS_LVCMOS) INTERFACE

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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1.2 V HIGH-SPEED LVCMOS (HS_LVCMOS) INTERFACE

(From JEDEC Board Ballot JCB-11-48, formulated under the cognizance of the JC-16 Committee on Interface Technology.)

1 Scope

This standard defines the dc and ac input levels, output levels, and input overshoot and undershoot specifications for the 1.2 V High-speed LVCMOS (HS_LVCMOS) interface. The non-terminated interface has a switching range that is nominally expected to be 0 V to 1.2 V and is primarily intended to support communications with Wide I/O SDRAM devices.

2 1.2 V High-speed LVCMOS (HS_LVCMOS) interface specifications

2.1 Recommended DC operating conditions

Table 1 — Recommended DC operating conditions

	Min.	Typ.	Max.	Unit	
VDD	1.14	1.20	1.30	V	Input Buffer Power
VDDQ	1.14	1.20	1.30	V	I/O Buffer Power

2.2 Input level

Table 2 — Input level

Parameter	Symbol	Min	Max	Unit
Input high level (AC)	VIH(AC)	0.80*VDD(or VDDQ)	VDD(or VDDQ)+0.2	V
Input low level (AC)	VIL(AC)	-0.2	0.20*VDD(or VDDQ)	V
Input high level (DC)	VIH(DC)	0.70*VDD(or VDDQ)	VDD(or VDDQ)+0.2	V
Input low level (DC)	VIL(DC)	-0.2	0.30*VDD(or VDDQ)	V

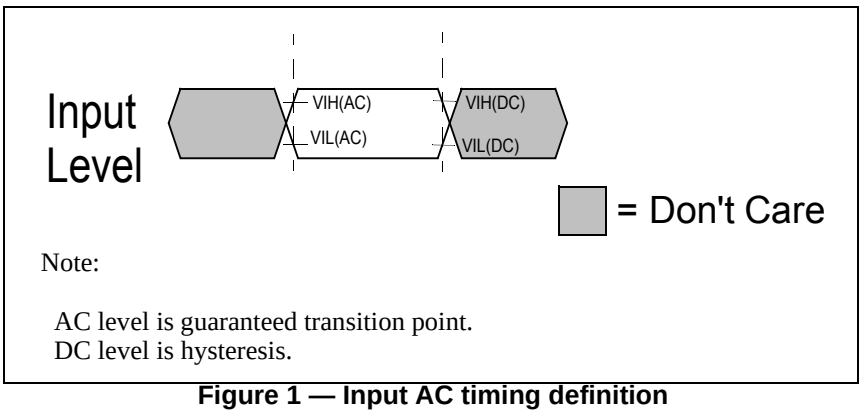

Figure 1 — Input AC timing definition

2.3 Output measurement level

Table 3 — Output measurement Level

Parameter	Symbol	Min	Max	Unit
Output high voltage	VOH	0.80 * VDDQ	-	V
Output low voltage	VOL	-	0.20 * VDDQ	V

2.4 AC input over/undershoot

Table 4 — AC input over/undershoot

Parameter	Specification
Maximum peak amplitude allowed for overshoot area	0.35 V
Maximum peak amplitude allowed for undershoot area	0.35 V
Maximum overshoot area above VDD/VDDQ	0.8 V ns
Maximum undershoot area below VSS/VSSQ	0.8 V ns

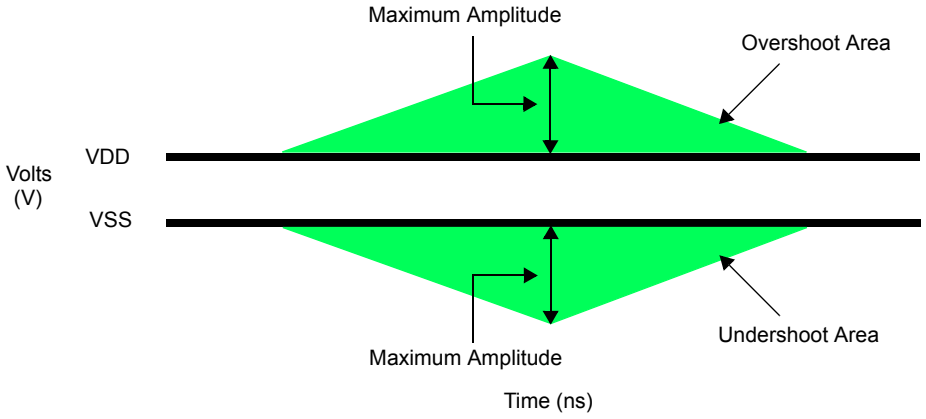

Figure 2 — AC overshoot and undershoot definition for input pins

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