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Guideline for Characterizing Solder Bump Electromigration under Constant Current and Temperature Stress

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Contents

GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS

(From JEDEC Board Ballot JCB-07-109, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This document describes a method to test the electromigration (EM) susceptibility of solder bumps, including other types of bumps, such as solder capped copper pillars, used in flip-chip packages. The method is valid for Sn/Pb eutectic, high Pb, and Pb-free solder bumps. The document discusses the advantages and concerns associated with EM testing, as well as options for data analysis. The tests are performed on packaged bump electromigration test devices. The bump electromigration test techniques described in this document can be used to assess the electromigration reliability of different types of solder bumps and metallizations, to make materials decisions, and to establish maximum bump current specifications. Thermal migration is also known to exist, but is outside the scope of this document.

2 Introduction

2.1 Bump electromigration failure mechanism

Electromigration of solder bumps is a failure mechanism that leads to increased resistance sometimes accompanied by events such as formation of intermetallic compounds (IMC), voids and cracks that can disrupt the solder joint and silicon and/ or package metallization leading into the bump. The resistance increase can ultimately lead to an open circuit. The stress drivers for this failure mechanism are current density and elevated temperature. The failure mechanisms for bump electromigration can be varied and depend on the metals present both on the silicon side and the substrate side.

2.2 Model for solder bump electromigration

Black's model (equation 1), which has been applied for many years to semiconductor die metallization, has also been applied to solder bump electromigration [1].

$$TTF \propto J^{-n} \exp\left(\frac{E_a}{kT}\right) \tag{1}$$

This equation contains a model parameter relating to temperature (T): the thermal activation energy, E_a. It also contains a model parameter relating to current density (J): the current density exponent, n. In order to verify that Black's model applies to the type of bump structures being tested, or to derive a new model, testing at multiple stress temperatures and current densities is needed. Extraction of these model parameters from the test results is addressed later in this publication.

2.3 Overview of the test

The electromigration test described in this document is performed in an oven at constant temperature and with a constant current source. The resistance of the bump electromigration structure (EM device) is measured using a 4-point measurement technique with the measurement points as close to the bump as possible. The EM device is considered to have failed when its resistance change (either absolute value or percent increase) reaches a predetermined value. The test is ideally continued until most of the test structures have met the predetermined failure criterion. The test structure may consist of a single bump or a chain of bumps.

3 Terms and definitions

anode: A circuit element to which positive bias is applied.

NOTE For the purpose of this document, when the die is the anode the electron flow is from the substrate through the solder bump to the die.

cathode: A circuit element to which negative bias is applied.

NOTE For the purpose of this document, when the die is the cathode the electron flow is from the die through the solder bump to the substrate.

censored data: A set of data for which a portion of the test samples had testing discontinued prior to failing or survived until the end of the test.

intermetallic compound (IMC): A substance formed when solder comes in contact with another metal at elevated temperature.

NOTE The IMC is composed of multiple constituents from the solder and the other metal. This material has unique mechanical and electrical properties, which are different from those of the initial solder and the other metallization.

simple daisy chain: A daisy chain consisting of a single series of bumps in a chain.

NOTE A current through the series of bumps will alternate in direction in successive bumps. The number of bumps where electrons flow out of the die and the number of bumps where electrons flow into the die are equal.

substrate, (package): A platform that mechanically supports a bumped silicon die within a package and electrically connects the solder bump landing pads to external terminals, using layered dielectric materials and conductive traces.

suspended items; suspensions: Items that had testing discontinued prior to failing or that survived until the end of the test.

under-bump metallization (UBM): A patterned, thin-film stack of material that provides 1) an electrical connection from the silicon die to a solder bump; 2) a barrier function to limit unwanted diffusion from the bump to the silicon die; and 3) a mechanical interconnection of the solder bump to the die through adhesion to the die passivation and attachment to a solder bump pad.

3 Terms and definitions (cont'd)

Wheatstone bridge: A 4-arm bridge forming a diamond, all of whose arms are predominantly resistive, with three resistors of known values in three of the arms and the unknown resistor in the fourth.

NOTE 1 A voltage source, e.g., a battery, is connected across two opposite points of the diamond and a current-detecting instrument (e.g., a galvanometer) is connected across the other two points. The values of one or two of the known resistors are varied until no current flows through the galvanometer. The bridge is then balanced and the value of the unknown resistor can be calculated in terms of the other three.

NOTE 2 A method using the Wheatstone bridge for monitoring resistance of solder bumps in electromigration tests has greater sensitivity to resistance change than other methods. Net resistance changes due to electromigration of only the solder bumps, excluding the Al or Cu traces, can be deduced by this method.

4 Test structures

4.1 Materials and process factors

Bump electromigration is strongly dependent on several factors. These include the following: bump composition; bump fabrication method (e.g., electroplated, printed paste, or evaporated [2]); composition of the under bump metallization (UBM) on the silicon [3]; the UBM layer thicknesses [4]; and the substrate type; and substrate pre-solder layers--e.g., Ni/Au, Copper/Organic Solder Protect (OSP), Copper/Solder on Pad (SOP)--and their thickness [5,6]. The semiconductor die metallization, passivation or repassivation composition, and test structure details, including via openings and design features, may also have a significant effect on Joule heating and current crowding. As such, it is very important that the test structure and materials accurately replicate the product design being assessed. If not, deviations from the product design need to be clearly described.

4.2 Bump geometry and structures

Bump geometry and structures can affect bump EM performance based on effects of current crowding. Important geometrical considerations in bump electromigration are: bump height and diameter; UBM size; UBM stack composition and layer thicknesses; passivation type and opening dimension; the silicon top metal pad size and thickness; semiconductor die metallization and thickness into the bump structure; and substrate pad size and composition. As mentioned above, to accurately evaluate product, the test structure should reflect these key attributes. If this is not done, the parts under test may not accurately represent current density and current crowding considerations for that product. It should also be noted that the bump geometry and structure used in any specific test vehicle may not represent the current carrying capability of any other geometries or structures.

4.3 Distribution of current to the bump(s)

It has been well established that confinement of the current within the bump, or current crowding, plays a significant role in void formation and bump failure during bump electromigration testing [7-11]. Current crowding can lead to damage initiation where the current density is at its peak. Thus bumps with nominally identical sizes and composition can exhibit different degrees of damage for the same applied current. Bumps with different current distributions can perform differently in an electromigration test even when stressed with the same conditions.

4 Test structures (cont'd)

4.3 Distribution of current to the bump(s) (cont'd)

Consequently, different current distributions may yield different values of maximum bump current. For this reason, it is important that the EM test structures represent as closely as possible the configuration that will be used in the product. However, since much higher currents and temperatures are used in the electromigration test than would be used in a product, the silicon and package metal current feed lines must be made large enough that the metal lines do not experience electromigration failures due to large amounts of joule heating or affect the resistance measurement of the bump during the test. Due to these considerations, the metallization geometries and linewidths used in the product cannot effectively be used in the test structure. Nevertheless, the distribution of current to the bump should be arranged so that it matches actual product as closely as possible.

A metric sometimes used to assess current crowding is the ratio of the peak current density to the average current density in the bump (called the current crowding ratio) [4]. Modeling can be performed in order to evaluate the current crowding ratio in the test structure and to assess its relationship to product. It is important when presenting bump electromigration data that the details of the test structure be included in the report so that the reader can determine whether the test structure is representative of the current distribution in the actual product. In fact, a variety current distribution configurations may need to be tested in order to adequately cover the range of product configurations intended.

4.4 Resistance of the test structure

The contact resistance of an individual solder bump interconnection is very low, typically between 5-20 mΩ. The resistance of external wiring connections to the pads above and below the bump will generally be much larger than the contact resistance, on the order of a few tenths of an ohm to over 1 ohm. This external parasitic resistance will depend on temperature and may also degrade during the course of an electromigration stress test. As mentioned previously, Joule heating in the external wiring can introduce additional complications into the test. This external parasitic resistance can be reduced by increasing the wire width and thickness; however, this may result in a test device structure which is very different from product designs. For single bump test structures, the external wiring resistance may not present a difficulty for current drive. However, for multi-bump chain structures with one or few voltage taps, it is important to reduce the wiring resistance as much as possible, increasing the proportion of bump contact resistance to the total resistance. In EM testing one needs to balance the ability to accelerate the test through use of a robust test structure versus testing a structure which is non-representative of product structures and current distributions.

4.5 Types of test structures

There are typically two basic types of structures used in EM: a) a single bump and b) daisy chain (a chain of multiple bumps).

4.5.1 Single-bump structures

This structure measures the resistance of a single bump. The chip and substrate bump pads form the bump terminals, which are connected to both a current force connector and a voltage sense connector on each side. The resistance measured is that of the bump plus the series resistance of the connecting wires. Ideally, most of the resistance would be in the bump itself.

4.5 Types of test structures (cont'd)

4.5.1 Single-bump structures (cont'd)

As a practical matter, the series connections up to the place where the current force and voltage sense lines diverge can account for a significant fraction of the total resistance of the structure. Due to the 3-dimensional distribution of current in pads and bumps, the exact location of the current and voltage taps can influence the measured resistance. Since bump resistance can be of the same order as wiring resistance, the lines on the device or substrate cannot be regarded as having the same voltage potential. Setting the voltage taps slightly away from the bump, along the current feed line, adds some unwanted wiring resistance to the measured value but assures that all parts of the bump and pad structure are included. For feeding the stress current to the tested bump, several bumps should be used to prevent premature failure of the non-tested bumps.

Advantages of the single bump structure

- Accurate single bump resistance
- Defined stress current direction
- Easier failure analysis since there is only one bump to investigate
- A resistance change, □R, of the structure can be used as a measure for bump degradation

Disadvantages of the single bump structure

- Low statistical confidence of the lower tail of the failure distribution unless a very large sample size is used
- Role of defects may not be observable because of the small test population

4.5.2 Daisy chains

Daisy chains consist of multiple bumps in the EM test structure. In daisy chains, alternate bumps are stressed with current flowing in opposite directions. That is, electrons flow out of the silicon in one bump and out of the substrate in the adjacent bump. For this document, a "simple daisy chain" is defined as a structure which the current flow goes through a single bump in one direction, then through a second bump in the opposite direction, etc. Such a structure is illustrated in Figure 1. Thus the current through each bump in a simple daisy chain is the same. Analyzing daisy chain data is less straight-forward than analyzing data from single bumps. In analyzing daisy chain bump EM data, it is sometimes assumed that the majority of the resistance increase of the chain is due to one strongly degraded bump (e.g. weakest link model [12]). If this is assumed, it should be confirmed through failure analysis. Assuming a weakest link model, testing a daisy chain using a small increase in resistance as the failure criterion should yield the time to serious degradation of the fastest degrading bump. Data analysis procedures for daisy chains are discussed in 7.2.

For the purpose of this document, the cathode terminal is the negative terminal. When the die is the cathode, electrons flow from the die to the substrate. The anode terminal is the positive terminal. When the die is the anode, electrons flow from the substrate to the die. It should be noted that some of the literature reverses this definition, and care must be taken to understand the direction of electron flow. A simple daisy chain can possibly have failures of both cathode and anode bumps. If one is interested only in the time to failure of a product (which presumably contains anode and cathode bumps in approximately equal numbers), this mixing of failure modes may be acceptable.

4.5 Types of test structures (cont'd)

4.5.2 Daisy chains (cont'd)

However, it may give a bimodal distribution of the failure data or possible increase the apparent spread (e.g., standard deviation) of failure times. If it is desired to distinguish the degradation from the two current directions, a daisy chain is needed that uses multiple bumps current flow in one direction and a single bump for current flow in the other direction. Such a structure is described in more detail in 4.7.

Due to their higher total resistance, Joule heating is generally more significant in daisy chains than in single-bump structures. Care must be taken in the structure lay-out so that heating is uniform for the whole chain and that the temperature can be effectively monitored. If the temperature is not uniform for all bumps, erroneous results can occur. If the structure is spread out over a large area, the ratio of metal line resistance to bump resistance can be quite high. Ideally, the total structure resistance would be less than a few tenths of an ohm, which limits the number of bumps that can be effectively used in a chain.

Advantages of daisy chains

- Defect-driven early bump failures can be detected more easily
- Better statistical confidence for the lower tail of the failure distribution
- Using chains of varying length, advanced statistical analysis can yield more information and shorter test times
- Taps can be added to the test structure to isolate failures and to continue stressing the remaining surviving bumps in the chain.

Disadvantages of daisy chains

- Difficulty in separating failures from each current direction without detailed failure analysis. This shortcoming can be addressed with a structure which contains multiple bumps in one direction of current flow and one bump in the other direction.
- In order to focus on one direction of electron flow, the total number of bumps in the structure can become quite large
- It can be more difficult to identify the failed bump. Failure Analysis is facilitated if all bumps are in a single line.
- Most of the chain resistance is due to the interconnect rather than the bump. Therefore, small increases in bump resistance are very difficult to detect.

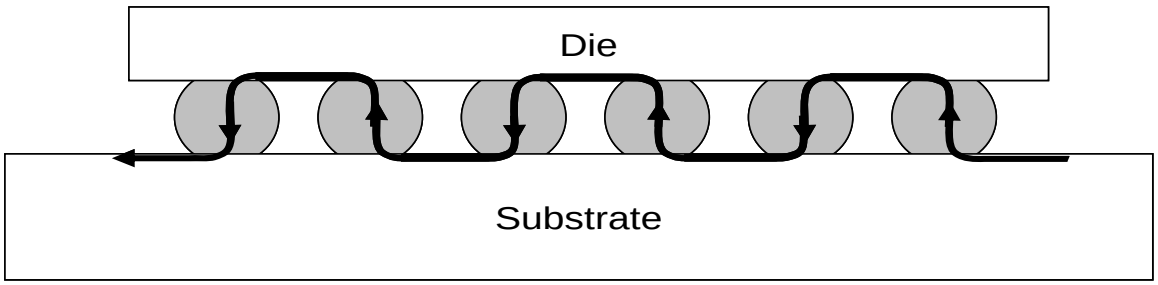

Figure 1 — Diagram of a simple daisy chain EM structure

4.6 Electromigration of the interconnect

In order to get bump electromigration to occur in a reasonable period of time, very high currents are required. Typical stress currents range from a few hundred milliamps (mA) to over one ampere. Furthermore, stressing at temperature higher than regular operating temperature is necessary. The highest temperature allowed in the EM test varies with the solder alloy system, substrate and metallization. The highest device temperature could be about 25^{o} C below the melting point of the solder alloy. Silicon metallization and organic packages are typically not designed to handle such high currents and temperatures. So special care must be taken to size the silicon and package metallization to be able to withstand the highest combination of current, temperature, and test duration expected. The metallization should be designed such that negligible resistance change due to electromigration occurs. Otherwise, metallization electromigration might be mistaken for bump electromigration.

4.7 Bump polarity

Studies have established that the electromigration damage could occur in bumps with current flow from the die side to the substrate side or from the substrate side to the die side. Therefore, in order to excite failures of only one polarity of bump, a special test structure is needed. A common design for such a structure is to have multiple bumps providing current to the bump of interest. Three or more bumps are generally adequate provided that the current is distributed among them in a reasonably uniform manner. The maximum current in any of the feed bumps should be significantly less than that in the test bump. An illustration of such a structure is shown in Figure 2.

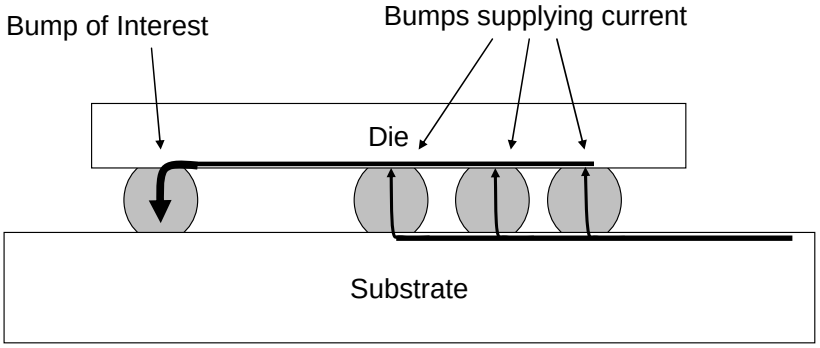

Figure 2 — Bump current supply illustration

Simple daisy chain with equal numbers of bumps with the same current flowing in each direction can also be used provided that the failure time of bumps of interest is known to be significantly shorter than that of the bumps with opposite polarity. Careful failure analysis is needed after the test to ensure the failure occurs only in the bumps with the polarity of interest.

4.8 Joule heating and temperature measurement

If one analyzes electromigration data with Black's equation it becomes apparent that measurement of the actual device temperature is critical. A one degree Celsius error in temperature measurement can, in some instances, cause more than a 20% error in the derived value of current exponent n. Because of the high currents involved, the power dissipation of the test structure can be substantial. Oven temperature is not an adequate measure of device temperature; the actual device temperature must be measured. When using a daisy chain, it is important that the temperature of all the bumps be uniform. Temperature uniformity can be accomplished with careful design and assessed through thermal modeling or through the use of several temperature sensing structures beneath the entire length of the chain.

4.8 Joule heating and temperature measurement (cont'd)

The effect of Joule heating can be minimized in several ways. Multiple thermal bumps to dissipate heat through the substrate are helpful, particularly if the substrate is a good heat conductor. Thermal vias within the substrate can also be utilized. Heat spreaders or heat sinks on the die also serve to decrease the Joule heating. Forced convection in the oven is desirable in order to minimize heating as well as to achieve temperature uniformity across the oven.

Temperature measurement of the device can be accomplished in several ways. Some electromigration test systems allow calibration of the temperature coefficient of resistance (TCR) of the actual electromigration test structure and then use this resistance as a measure of the device temperature. For bump EM devices, this measurement can be tricky because of the extremely low resistance of the device. Another method is to place a silicon metallization resistor on the die. If the die contains multiple metal levels, it may be possible to place the resistor directly beneath the EM test structure. If not, the resistor should be placed as close as possible to the test structure, perhaps even surrounding it. If the temperature sensor is not directly beneath the EM test structure, thermal modeling should be done to determine the difference between the temperature of the temperature sensor and that of the EM structure. If the test structure is a fully-processed silicon die, a thermal diode can be included beneath the EM test structure. Calibrating the temperature sensing devices is discussed in a later section.

5 Stress conditions

The stressors for electromigration are current density and temperature.

5.1 Current density

The stress currents used depend on the solder type and bump geometry. Typical current densities used in bump EM tests are in the range of $3x10^3$ to $2x10^4$ A/cm^2, based on dividing the current by the smallest cross-sectional area, which usually is the device passivation opening. For typical bump geometries, this translates into currents on the order of 250 mA to 1.5 A. The tradeoff is that lower currents lead to longer tests and higher currents create a higher temperature rise due to Joule heating. It has been reported that very high stress currents can lead to localized melting of the solder, which must be avoided. It has also been reported that there can be different failure modes found between the lower and higher stress currents used in the test and that the higher stress currents may not be representative of EM effects in product in the field [13].

In order to obtain the Black's equation parameter, n, it is recommended that at least three currents be used. In order to get the optimal line fit from the data points, it is best to have the data points equally spaced on the log(time to fail) vs. log(current density) plot. Thus, it is desirable to choose currents which are equally spaced on a log scale.

5.2 Temperature

The maximum stress temperature depends on the type of solder being tested. It is important not to be close to the melting point of the solder so the device temperature should be kept to a minimum of 25 °C below the melting point. There is also some evidence in the literature that the diffusion characteristics of Sn/Pb solder change at a fairly low temperature (110 – 140 °C) [14-16] leading to the concern that EM tests done at higher temperatures may not adequately represent the EM that occurs at lower temperatures. Of course, the lower the temperature, the longer the test time. The maximum operating junction temperature of many products is now on the order of 110 °C. Therefore, this is probably the minimum practical stress temperature.

In order to obtain the Black's equation parameter E_a, it is recommended that at least three temperatures be used. In order to get the optimal line fit from the data points, it is best to have the temperatures equally spaced on a 1/ (kT) scale.

6 Temperature calibration and measurement

Since device temperature measurement is so important to obtaining accurate results, care must be taken in temperature calibration and temperature measurement.

6.1 Calibrating the oven

All temperature measurements should be made with the oven loaded with test boards as it will be during the actual EM test, see JESD22-Bxxx (Characterization and Monitoring of thermal Stress Test Oven Temperatures). The boards affect airflow and temperature gradients. Measure the temperature at or near the center of the array of test boards with a calibrated temperature measuring device. Set the oven to the desired stress temperature (with no EM devices in it) and measure the actual temperature. If the temperature controller can be set to agree with the actual temperature, do this. Otherwise note the temperature offset so it can be taken into account later.

With test boards present, measure the temperature throughout the oven to assess the temperature variation from top to bottom, side to side, and end to end (wherever the EM devices will reside). This is often accomplished using thermocouples which have been calibrated using the calibrated temperature measuring device. Ideally, the total temperature variation will be less than ± 1 °C. The higher the temperature variation, the more scattered the failure data will be.

6.2 Calibrating the temperature sensing devices (temperature sensors)

6.2.1 Resistors

Some electromigration test equipment allows temperature coefficient of resistance (TCR) measurements to be made automatically. If not, set the oven at a temperature approximately 30 °C below the desired operating temperature and allow the temperature to stabilize. Then measure the resistance of the temperature sensor, see JESD33 (Standard Method of Measuring and Using Temperature Coefficient of Resistance of a Metallization Line). This measurement is typically performed by holding the current constant (as is done in an electromigration test) and measuring the voltage. The lowest practical temperature sensor current should be used to avoid Joule heating.

6.2 Calibrating the temperature sensing devices (temperature sensors) (cont'd)

6.2.1 Resistors (cont'd)

If it is later calculated that the power consumed by the temperature sensor during calibration results in a temperature rise of more than 0.2 °C, a correction should be made to the TCR results. 4-point measurement of the temperature sensor is preferred.

Raise the oven temperature 5-10 °C and repeat the procedure. The temperature of the final measurement should be made at or just below the oven temperature to be used in the test. Although the resistance vs. temperature is quite linear, taking one data point near the test temperature minimizes any error due to extrapolation. A plot of resistance vs. oven temperature is made from which the TCR of the individual temperature sensors can be calculated.

6.2.2 Diodes

If thermal diodes are used, a similar procedure is used for calibration. When operated at a fixed current, a diode exhibits a nearly linear voltage-temperature (V-T) relationship with temperature sensitivities of around -2mV/^{o}C. The optimal current does depend on the area of the diode and is a trade-off between noise level and sensitivity. The advantage of a diode sensor is that it can be as small as 5□m x 5□m, so thermal gradients within the sensor are minimal. Calibration of the diode consists of measuring the voltage at a constant current at a minimum of three temperatures in the vicinity of the desired operating temperature and determining the V-T curve at that current. A 4-point measurement is preferable. A plot of voltage vs. oven temperature is made for each sensor diode, from which the temperature coefficient of voltage of the diode is calculated.

6.2.3 EM devices as temperature sensors

Although the preferred method of temperature measurement utilizes separate resistor or diode temperature sensors, an alternative approach is to perform TCR measurements on the EM devices themselves prior to the start of stress. A disadvantage of this method is that only the initial stress temperature can be determined with any confidence. Device degradation will occur during the course of thermal and electrical stress on the device, potentially affecting the TCR of the device and invalidating the calibration. For this reason, if the EM devices themselves are utilized for temperature calibration, then only the initial stress temperature is to be used for data analysis.

6.3 Determining the temperature rise of the EM devices

The oven is set to a temperature slightly below the desired stress temperature and allowed to stabilize. Then the temperature sensors are activated and allowed to stabilize. After the temperature sensor on the die has reached a constant resistance, the associated EM device is powered using the same stress current that will be used in the EM test. The resistance of the temperature sensor will increase due to local heating of the die by the EM device. Once the temperature sensor resistance has stabilized at the new temperature, turn off the EM device and allow the temperature sensor to re-stabilize at the oven temperature. The temperature sensor resistance should return to very near its original value.

A similar methodology can also be used for diode temperature sensors.

6.3 Determining the temperature rise of the EM devices (cont'd)

Using the previously obtained TCR for the particular temperature sensor and the resistance increase data, the temperature rise due to the EM device can be calculated. Ideally, this measurement and calculation would be done for all devices in the oven. In addition to differences in stress current, temperature and airflow variations within the oven as well as thermal resistance variations between devices and sockets can result in variations in temperature rise of the devices. If the variation in temperature between devices is small enough, an average temperature rise can be used for purposes of data analysis. If large device temperature variations are observed, then the data analysis can correct for individual device temperature differences.

6.3.1 Temperature variation across the die

If the temperature sensor is not located directly below the EM device, the EM device may be at a different temperature than the temperature sensor. This situation is most likely to occur if the temperature rise of the device due to Joule heating is more than several degrees C. Thermal modeling of the heat dissipation in the die can be used to estimate and correct for this temperature difference.

6.4 Setting the oven temperature

The ideal situation is to have a separate oven for each stress current. Then all the devices in the oven will be at approximately the same temperature. Then the oven temperature is simply the desired device temperature minus the temperature rise calculated in the previous section.

If multiple currents are to be used in the oven, each current will produce a different device temperature. If three currents are used, often the middle current is used to set the oven for the desired device temperature. The devices with other stress currents will be at temperatures above and below the desired temperature. These temperature differences will be accounted for during data analysis.

7 Performing the test

7.1 Sample size

Ideally, a sample size of 30 would be used at each combination of temperature and current since a large sample size and a greater number of failures improve the confidence limits. A minimum sample size of 15 is recommended.

7.2 Preconditioning

Products will be subjected to the temperature stress of soldering onto the circuit boards. To simulate product conditions, the samples should be preconditioned per JESD22-A113 before the test is started. Unless there is specific concern about moisture absorption before reflow affecting the results, moisture soak is not required. If the product is expected to experience more reflows or different temperatures than those specified in the JESD22-A113, then the preconditioning of the test devices should replicate that of the product.

7.3 Arranging the samples in the oven

If multiple tests (e.g., multiple currents, different geometries, different UBM's etc.) are to be run in an oven and average device temperatures are used, the samples from each leg of the test should be evenly distributed throughout the oven to prevent stratification due to temperature gradients in the oven. This precaution is not necessary if individual device temperatures are used in the data analysis. In that case, keeping the devices from each leg close to each other may be preferable in order to minimize temperature variation between them.

7.4 Resistance measurement

Electromigration resistance monitoring consists of making resistance measurements of the EM device throughout the test and comparing these with the initial resistance of the device. For accurate measurements of bump resistance, it is necessary to use a 4-point measurement scheme in which separate voltage tap connections are utilized to sense the voltage across the test bump interconnection. The initial resistance is the resistance of the device at the device stress temperature (the oven temperature plus the temperature rise due to Joule heating of the device) at the commencement of the test. Therefore, the device should be powered at the desired stress current until its temperature stabilizes before the measurement of initial resistance is made. It should be noted that if very sensitive failure criterion is selected, one cannot necessarily use the initial resistance measurement. Judgment must be used in selecting the 'real" initial resistance since over the first hours on test since the time-zero resistance varies due to possible IMC growth within the bump and its associated interfaces.

The resistances involved in bump electromigration tests are generally considerably smaller than that in metal line and via electromigration tests. Therefore, the sensitivity required of the equipment is greater. For example, for a stress current of 0.2 ampere and an EM structure resistance of 0.1 ohm, the measured voltage is 20 mV. A resistance change of 0.03 ohm would result in a measured voltage change of 6 mV. Therefore extremely sensitive voltage measurement is necessary in order to accurately measure resistance differences of one milliohm. Commercially available systems exist which have such capability.

Another measurement technique is the Wheatstone bridge method. This method allows accurate detection of a few milliohms of resistance change [17]. The method has been used successfully for measuring both single bump and bump chain structures.

A method which can increase the system capacity is having several single bump structures connected in series using the same constant current source. The resistance of each bump is measured individually through a 4-point measurement. Such an arrangement requires logic that will shunt the power supply around a bump when that bump reaches the failure criterion

7.5 Test duration and resistance monitoring

Ideally, the stress parameters of temperature and current will result in failures occurring from a few tens of hours to a few thousand hours. In order to obtain accurate time to failure information, 4-point resistance measurements of the test structures should be made approximately every hour, at least in the beginning. Some test equipment allows measurements to be made in equal log (time) intervals. If this method is used taking 230 readings per decade yields a 1% resolution in the time of failure. To reach the t_{50} for log normal or $t_{63.2}$ for Weibull distributions, it is recommended that each leg of the test should be continued until at least 65% of the test devices have failed.

7.6 Setting the failure criterion

Low resistance is the main characteristic of solder bump connection. Failure is identified with an increase in resistance or complete loss of electrical continuity. However, the failure criterion used can be dependent on the UBM, solder and subsequent intermetallic formation found in the specific test structure. Intermetallics can form (between the UBM and solder and/ or between the substrate and solder) which increase the resistance of the test structure without being an imminent electromigration failure. Therefore, caution should be used in selection of the failure criterion. The failure criterion should reflect void formation rather than just intermetallic formation and growth. There are three types of failure criteria commonly used in electromigration tests. The merits of each for use in bump EM testing are discussed.

7.6.1 Percentage increase in resistance

The percentage increase in resistance criterion considers a failure any test structure whose resistance increases by x% over its initial resistance. In standard EM work, x is typically 10 or 20. Because of the extremely small resistance of single bump structures, the lowest practical value for x may be 50% or 100% where degradation is more pronounced. Also with certain solder bump structures, there is formation of IMC which has a higher resistivity than the original materials. This information should be factored into the failure criterion. The percentage increase method is most effective if all the structures have very close to the same initial resistance. If the initial resistance of the structures is not the same the % increase method can result in varying failure criteria for the bumps.

With a chain, perhaps 95% of the initial resistance is due to silicon and package conductors. Variations within the silicon and package processes can lead to a 15% variation in these resistances. For example, suppose that in a chain, the total bump resistance is 20 mΩ and the nominal total conductor resistance is 200 mΩ. The chain resistance can vary from 190 mΩ to 250 mΩ. If one selects a 20% increase in resistance as the failure criterion, some chains will fail when the resistance has increased 38 mΩ and some when the resistance has increased 50 mΩ. In terms of the total bump resistance of 20 mΩ, this is a range of 190% to 250% increase in bump resistance. Thus, using a percentage change in chain resistance can result in a varying failure criterion for the bumps in a chain.

7.6.2 Actual increase in resistance

The increase in resistance criterion considers a failure any test structure whose resistance increases by a certain amount over its initial resistance. A consideration for use of this method over the percentage resistance change criterion is that variation in the initial resistance of samples can be tolerated without incurring differences in the failure criterion between test samples.

The actual value of the resistance change chosen for the failure criterion depends on several factors. The product application determines what maximum bump resistance can be tolerated by the chip design. For example, analog applications may have more stringent demands than digital applications. Even when the stressed bump exhibits a fairly low increase in resistance, the bump may have degraded to the point that thermo-mechanical stability is no longer assured. The resistance characteristic often becomes noisy as voiding begins to occur, which may be an indication of the onset of instability.

7.6 Setting the failure criterion (cont'd)

7.6.3 Absolute resistance

For some product operation the absolute allowable contact resistance is known and as such, it may be most appropriate for the failure criterion to be the absolute bump resistance.

7.7 Test details to be included in report

Because the materials and geometry of the test structure affect the electromigration results, the following information should be included in the report of bump electromigration results.

Materials and geometries
- Silicon metallization: materials, thicknesses, and dimensions of all metal layers
- For each UBM layer: material, thickness, and deposition technique
- UBM size
- Passivation or repassivation opening size (where UBM contacts silicon metallization)
- Passivation/repassivation materials and thicknesses
- Bump composition
- Bump deposition method
- Bump height, both non-reflowed and after attaching to substrate
- Bump pitch
- For each layer of substrate metallization: material, thickness, and deposition technique
- Substrate pre-solder composition, thickness, and deposition method, if applicable
- Substrate solder resist opening (if applicable)
- Substrate metal pad size
- Substrate material
- Substrate internal metallization composition

Test structure
- Number of bumps in chain
- Diagram of bumps in test structure—e.g. number of anode bumps per cathode bump
- Number of metal levels in the silicon
- Diagram of how current is distributed to the bumps under test
- Feed structures for the current into the bump
- Method of measuring device temperature
- Placement of the temperature sensor with respect to the EM test structure

Failure criterion

Frequency of device resistance measurements

For each oven
- Temperature variation across oven

For each unique test condition
- Initial device resistance at the stress condition (average and spread)
- Device current
- Oven temperature
- Temperature rise of device due to Joule heating
- Device temperature
- Sample size
- Bump details (materials, UBM, passivation)
- Substrate details

8 Data analysis

Analyzing EM lifetime data involves first selecting a statistical distribution and fitting it to the time-to-fail data, and then calculating the model parameters for current and temperature acceleration (e.g., Black's model). Once these tasks are accomplished, the results can be extrapolated to the product use conditions. A variety of procedures for carrying out these analyses have been published in other JEDEC documents [18-20]. However, analysis of bump EM data requires some special considerations.

Electromigration models, such as Black's model, are expressed in terms of current density. For solder bumps, it is not clear how to determine the current density. A common method is to divide the current by the cross sectional area of the passivation opening. However, there is evidence that the lifetime of solder bumps does not scale with the area of the passivation opening [21]. Also, as voids and cracks begin to form, the cross sectional area constantly changes. Therefore, a better method of applying models is to use current rather than current density. After all, the objective is to find the lifetime of the solder bump at an applied current.

Another factor in analyzing bump EM data is that there are likely to be a significant number of suspended data points. There are two reasons for this. 1) The currents and temperatures for accelerated bump EM testing are severely limited by the melting point of the solder. Therefore the failure times tend to be fairly long and the test often must be terminated before all devices have failed. 2) When chains are used, common analysis methods (described later in this section) suspend the remaining bumps in the chain when one fails, assuming there is no provision to electrically jumper around the failed bump, (see 3.5.2). Therefore, analyzing bump EM data requires techniques which account well for suspended data.

8.1 Choosing the failure distribution

In principle, the distribution function should have a physical basis and closely match the experimental failure distribution. It is desirable to utilize a failure distribution with a minimum of parameters that has straightforward physical meaning and which allows analytical mathematical analysis. Two common distributions that have been used to describe electromigration failures are lognormal and Weibull. Based on the data, one needs to verify which distribution is the best fit. Once the failure distribution is selected it should be used to determine all pertinent projections for that set of data.

8.1.1 Lognormal distribution

The lognormal distribution has historically been the distribution of choice for analyzing metal line and via electromigration. This distribution applies to multiplicative degradation failure mechanisms such as electromigration. Recently, work has been published that uses a 3-parameter lognormal distribution to fit electromigration data. The argument is that there is an initiation, or incubation, time before voids form that are large enough to cause significant resistance increase [22].

8.1.2 Weibull distribution

The Weibull distribution is popular because of the flexibility with which the distribution can be made to fit a wide variety of experimental failure data. The Weibull distribution is an example of an extreme value distribution, where the system contains many independent elements and failure of any one element causes failure of the system. With bump electromigration, particularly using chains, there may be situations that justify the use of the Weibull distribution. As with the lognormal distribution, a 3-parameter Weibull distribution can be used to model a situation in which there is an incubation time in formation of voids.

8.1 Choosing the failure distribution (cont'd)

8.1.3 Cautions in choosing the failure distribution

Because the failure data will need to be extrapolated to much lower failure percentages, it is important to choose the failure distribution which best fits the experimental data with statistical significance. Ideally, plots will be made using lognormal, Weibull, and any other applicable distributions. Then the fit of the model to the data should be determined statistically (e.g., correlation coefficient, log likelihood, etc.). If one distribution fits the experimental data significantly better than the other, then that distribution may be preferred.

It is important to note that in extrapolating data to a lower failure percentage, the Weibull distribution gives lower times to failure than does the lognormal. Therefore, if the lognormal distribution is used, the maximum allowed current predicted will be higher than if the Weibull distribution is used. So it is important to verify that the data fit a lognormal distribution very well, particularly in the low failure percentage region, if that distribution is used in making maximum current predictions. Otherwise, the maximum allowed current could be overestimated by a significant amount.

8.1.4 Cautions for 3-parameter distributions

Three-parameter distributions contain an incubation time term (before which time no failures occur). A problem with using a 3-parameter distribution to analyze EM data is that the incubation time can depend on the stress current and the stress temperature. Therefore, the incubation time parameter will need to be extrapolated to use conditions. In order to perform a valid extrapolation, many additional stress temperatures and currents should be used. Even then, it is not clear that an unambiguous extrapolation will be obtained.

8.2 Special considerations for analysis of chain data

When a chain of bumps is tested, one must make a decision on how to count chain failures. Prior to analysis of chain data, it is necessary to determine if all bumps in the chain have the same probability of failure. Each link in a series chain contains a pair of bumps, but the interconnect bump structure may be very different between the die side and substrate side of the interconnections. In such situations, there may be a large difference between failure rates for electron flow out of the die (where the die is the "cathode" or negative terminal) and electron flow into the die (where the die is the "anode" or positive terminal). Unless the failure rates for the two polarities are similar, one mode will dominate, and therefore the number of independent tests in a chain is half the total number of bumps in the chain. As discussed elsewhere, special chain structures can also be fabricated to contain multiple "feed" bumps within the chain, thus assuring that bumps of only one polarity will fail. We shall call bumps which are of the failing polarity "active" bumps.

A common assumption for a series chain is that changes in the resistance of one and only one bump resistance dominates the total change in resistance. This is generally referred to as a weakest link model. Some ways to implement the weakest link model are described in the next section. If it is determined that more than one bump in the chain are increasing in resistance, then an alternative analysis method must be devised.

8.2 Special considerations for analysis of chain data (cont'd)

For tests on series chain structures, choice of failure criteria is particularly challenging. If an open (or high resistance value) is used as a failure criterion, then it can be assumed that one and only one bump has failed in the chain, in which case the weakest link model is valid. If a more sensitive failure criterion is used, then it is not clear if the resistance change can be associated with a single bump or if several bumps are each undergoing a small resistance change. If there is uncertainty as to how the resistance change is distributed among the bumps, it is possible to compare results using two analysis methods: 1) weakest link model; and 2) assuming an equal resistance change in all bumps (i.e., not suspending any bumps when a chain fails). A decision needs to be based on the test structure, a statistical analysis of the data, and failure analysis of the bumps to determine if the resistance increase is due to one bump or the series of bumps in the chain.

Using bump chains and analyzing them and assuming a weakest link model has the advantage that the early failure portion of the distribution is sampled. Thus the extrapolation to the failure percentage used for the product life specification is less than if single bump structures are used. This is an important consideration because of the hazards in doing extrapolation when the exact failure distribution is unknown.

8.3 Assigning cumulative distribution function (CDF) values to the failure data

For this discussion, it is assumed that the individual bump failures can be described with a single failure mode or mechanism. The sample failure times are determined, using defined failure criteria such as that defined in 6.6. These failure times constitute a sampling of the parent cumulative distribution function (CDF). A probability plot utilizes a special scale associated with a particular distribution (such as lognormal or Weibull). If the experimental data fall on a straight line in the plot, then the sampled distribution corresponds well to the assumed distribution in the probability plot. To make a probability plot, the failure times are listed in increasing order, and CDF values assigned, usually in units of percentage failed. The assignment of CDF values is referred to as ranking.

There are many ways to estimate the median rank values, including solving the cumulative binomial equation, beta and F distribution transformations, and Benard's approximation [23]. The simplest approximation for the median rank (MR) for the jth failure of N samples is Benard's approximation:

$$MR = \left(\frac{j - 0.3}{N + 0.4} \right) \tag{2}$$

where j is the order number of the failure (an integer from 1 to N).

A more accurate method utilizes the F distribution, given by the following formulas,

$$\begin{aligned} MR &= 1/(1 + \left(\frac{N - j + 1}{j} \right) F_{0.5;m,n}) \\ m &= 2(N - j + 1) \\ n &= 2j \end{aligned} \tag{3}$$

where F denotes the F-distribution. (In an Excel spreadsheet program, the FINV function can be used, with the arguments 0.5, m, and n, determined for the jth failure of N samples.)

8.3 Assigning cumulative distribution function (CDF) values to the failure data (cont'd)

As mentioned earlier, bump electromigration data can contain a significant number of suspended data points. Suspensions can occur during the test due to equipment failure or termination of the test before all devices have failed. When a series bump chain is tested, there can be many suspensions throughout the test. For when one bump in a chain fails, the rest of the bumps are removed from test at that time (unless there are provisions for bypassing the failed devices).

When there are suspended data, the methods above for determining the CDF are not directly applicable. In particular, when there are suspensions the values of j in the above equations are no longer integers. There are methods for determining the (non-integer) values of the j's and applying median ranks which can be applied to censored data sets [24, 25]. Another method commonly used when dealing with suspended data is the Kaplan-Meier estimator [26]. For electromigration data on daisy chains a method known as the Weakest Link Approximation [27] is often used. Another technique used to analyze electromigration chain data is Deep Censoring [28]. One of these methods, or an alternative method for dealing with suspended data, can be used to determine the CDF values.

8.4 Plotting the data

Once the CDF values have been determined, the data are fit to a straight line to extract distribution parameters (regression analysis). CDF values can be plotted on the ordinate (vertical axis) or on the abscissa (horizontal axis). Regardless of the choice, for consistency, it is important to perform the regression analysis in the same way. The fitting procedure can be done in variety of ways, including rank regression on Y, rank regression on X, and maximum likelihood estimation (MLE). There are also a number of commercially available software packages that are designed to perform this analysis.

When using rank regression, It is preferred that the CDF values be treated as the independent variable, and that regression analysis is performed on the experimental failure times (i.e., fitting to minimize error in failure times). Rank regression minimizes the squares of the distances of the data points to the fitted line. So it appears to fit the data points better than the MLE method, which can be misleading since the rank regression method gives weight to points in the tails of the distribution. The correlation coefficient indicates the goodness of fit of the data to the calculated line. A poor correlation coefficient or curvature in the data may indicate a multi-modal distribution or that the incorrect distribution was chosen.

An advantage of the MLE approach is that it handles suspensions better than rank regression, particularly when dealing with a data set which has few exact failure times. Rank regression can only handle so-called "type 2" censoring, where the test is ended at or shortly after a preset number of fails. The rank regression approach is poorly suited for cases where surviving parts are removed prior to the end of the test, or there is a substantial time gap between the last fail and the end of test. On the other hand, MLE is best for large sample sizes [23]. The results for small sample sizes (<30) can be very biased, depending upon the failure distribution.

Deciding between rank regression and MLE can present a dilemma [29]. Whenever possible, both MLE and rank regression analysis should be performed and the results compared. If the results are consistent with each other, then there is higher confidence that the data fits the chosen statistical distribution. If the results differ, then it may be prudent to use the method which gives the more conservative estimate of the lifetime at the desired failure percentage [30].

8.4 Plotting the data (cont'd)

When regression or MLE analysis is complete, the distribution parameters can be extracted. For the lognormal distribution, the time required for 50% of the samples to have failed is called t_{50}. Unlike the normal distribution, the shape parameter for the lognormal distribution does not have simple physical meaning as the standard deviation of the distribution about the mean, but it does provide a measure of the "width" of the distribution. The term commonly used for the lognormal distribution shape parameter is sigma (σ), but it is not the standard deviation.

When analysis is done using the Weibull distribution, the parameters obtained are the characteristic time, η (time at which 63.2% of the devices have failed) and the shape parameter, β. The shape parameter will be greater than unity for a wearout mechanism such as electromigration. The higher the β, the more tightly the failures are distributed in time.

8.5 Dealing with bimodal distributions

When more than one failure mechanism is present in the test device structures, a single failure distribution may not be appropriate to describe the failure rates. In such cases, the cumulative distribution function will not be a straight line, instead exhibiting kinks and regions which may have different slopes. For a bimodal distribution, the region at short times corresponds to the timeframe during which the "weak mode" failure mechanism dominates. The region occurring at the longest times corresponds to the timeframe during which the "strong mode" failure mechanism dominates. At intermediate times, both failure modes compete.

For a large number of data points, it can be concluded with confidence that CDF curves with kinks indicate that multiple failure modes are present. However, for a small number of data points, it is possible that random events may lead to a kinked CDF curve, even though only one failure mode is present. Due to the difficulty in assessing these statistics, additional failure analysis or simulations may be needed to determine single or bi-modality of the specific data. If tests are performed on daisy chains with different numbers of device elements, Monte Carlo simulation can be used to determine the statistical parameters for each failure mode, and estimate the fraction of the total population which is failing in each mode [27, 31].

8.6 Extracting model parameters

In classical acceleration theory, the time to fail is "accelerated" by a multiplicative factor that depends only on the stress condition. This acceleration factor, the empirical derivation of which is described in this document, is a constant that depends only on the stress conditions. Therefore, the sigma (lognormal distribution) or the shape parameter (Weibull distribution) should be the same for each stress cell. A common sigma (lognormal) or common shape parameter (Weibull) constraint should be imposed in the data analyses. Once t_{50} and the constrained common σ (using the lognormal distribution) are known for each data set, the methods in Reference [20] are used to extract the Black's equation parameters E_a and n. As pointed out earlier in this section, for solder bumps the parameter n is more reasonably interpreted as the exponent for current rather than for current density. Both the best estimates and confidence bounds for these parameters should be determined. Typically 90% or 95% confidence intervals are used. Similar techniques apply for the Weibull distribution with characteristic time η and constrained common shape parameter β. It should be noted that Black's equation can apply to any percent fail and not just the typical t_{50}.

Care should be taken to weight the t_{50} of the experimental stress properly. For example, if there are 10 fails at one stress condition, and 2 fails in another, introducing a 5:1 weighting factor is prudent.

9 Failure analysis / Physical analysis

The goal of failure analysis is to detect and identify the location, mode, and mechanism for the observed electrical failure. It is an important to identify the failing solder bumps (if it is a daisy chain) and to validate if the encountered failures are truly attributed to electromigration. This is especially important if multi-modal distributions are observed.

In many cases, it is not readily obvious if the failure is within the test cable/connector, test board, solder attachment or internal package interconnect, therefore an electrical verification is always recommended as a first step. This step is even more important if the failure criterion (i.e., resistance change) is small, and therefore susceptible to other experimental fluctuations and uncertainties.

The typical failure analysis flow for board level analysis is depicted in Figure 3. The common tools and equipment involved include, but are not limited to:

- Scanning Acoustic Microscope
  - Check for delamination, voids, etc.
- X-Ray Inspection
- Mechanical Tools [e.g. grinding tools] and Cross-sectioning Equipment
  - Expose solder bump degradation signature
- Scanning Electron Microscope (SEM)
  - Inspect solder bump degradation signature at high magnification.
- Surface Analysis Tools [e.g., Energy Dispersive X-ray, Auger, Secondary Ion Mass Microscopy etc.]
  - Check for material signature

Information about these techniques can be found in Microelectronics Failure Analysis Desk Reference, 5th Edition [32].

Finally, following the flow from beginning to end does not guarantee an analysis with root cause identified. In practice, failure analysis is multi-disciplinary and therefore experience of the failure analyst and expertise drawn from different areas of science and engineering are required for successful determination of root cause [33, 34].

9 Failure analysis / Physical analysis (cont'd)

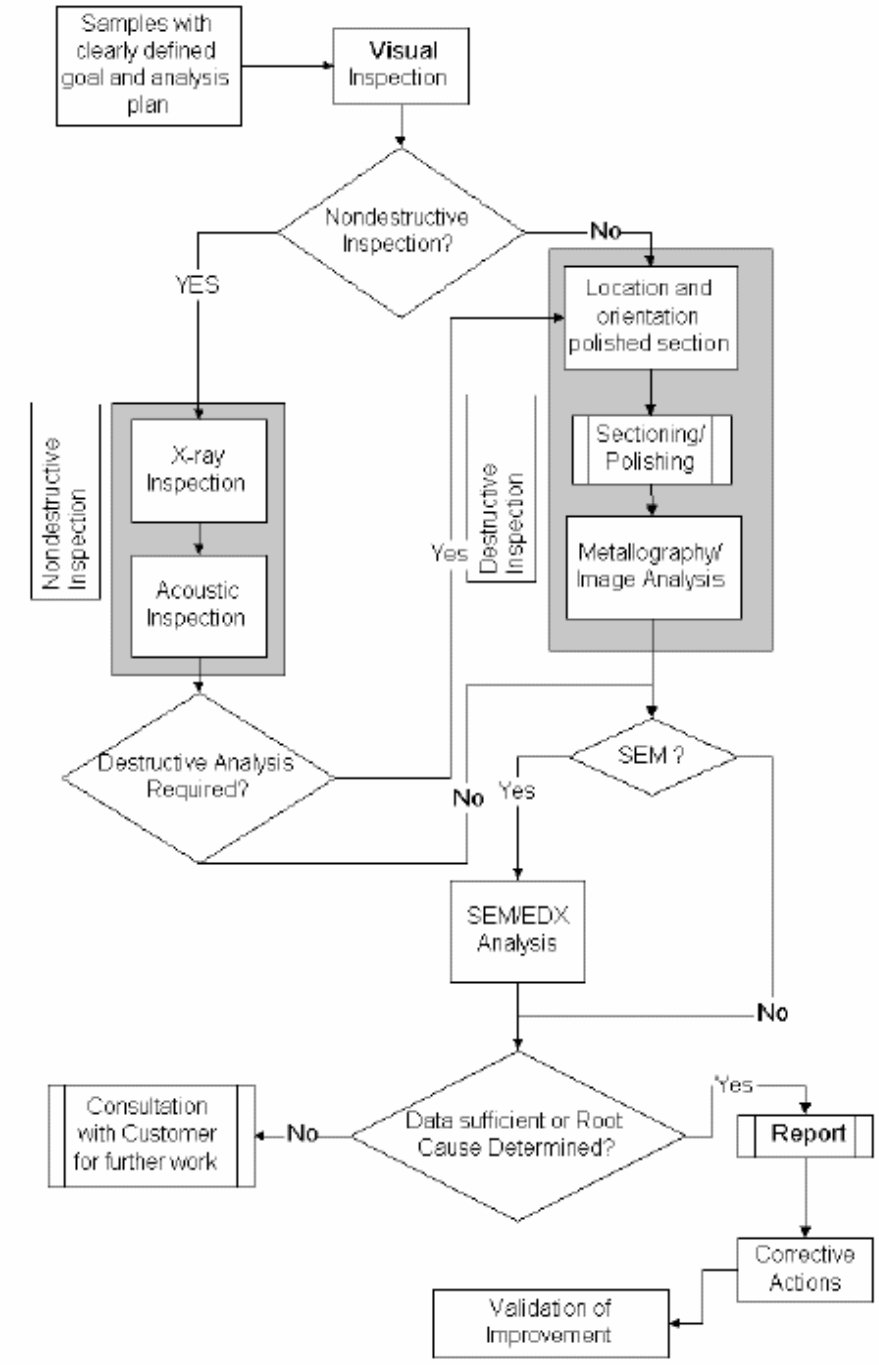

Figure 3 — Typical Failure Analysis Process Flow for Board Level Analysis [32]

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Annex A Method of determining maximum allowable bump current at a given temperature

This Annex gives an example of one method of calculating the maximum allowable DC bump current at a given (constant) bump temperature and for a given lifetime.

The electromigration testing and data analysis described in this document yields the following information

1. Best estimates and confidence limits for t_{50} and σ (if a lognormal distribution is used) or $t_{63.2}$ and β (if a Weibull distribution is used). These values are obtained for each unique combination of current and device temperature.
2. Best estimates and confidence limits for the acceleration parameters (E_a and n if Black's model applies).

The maximum current density specification for metal line and via electromigration typically requires that fewer than x% of metal lines (or vias) fail at a predetermined lifetime, t_{use}. A similar criterion is applied to bump electromigration: less than x% of bumps is allowed to fail at a predetermined lifetime.

A method for determining an estimate for the maximum allowable DC current at a given device temperature is illustrated in the case where Black's model for temperature and current density acceleration has been shown to apply. An analogous method can be used if another acceleration model has been demonstrated to apply. The analysis below also assumes that the geometry of the bumps, and the current distribution to the bumps, in the tests at different currents and temperatures is constant, allowing the current to be substituted for the current density. This is an important assumption because, as was pointed out in clause 7, the current density is not constant within a bump. The analysis below is done for a lognormal failure distribution.

Black's equation states:

$$t_{50} = A \cdot J^{-n} \cdot e^{\frac{E_a}{kT}} \tag{A1}$$

where t50 is the time at which 50% of the parts have failed, k is Boltzmann's constant, T is temperature in kelvins, and J is the (uniform) current density. n is the current density exponent, and E_a is the thermal activation energy. A is a constant which depends on the material properties. Black's equation can be applied to any percent of parts failing by using the standard deviation (σ) of the lognormal distribution.

$$t_{x\%} = t_{50} \cdot e^{z \cdot \sigma} = A \cdot J^{-n} \cdot e^{\frac{E_a}{kT}} \cdot e^{z \cdot \sigma} \tag{A2}$$

where $t_{x\%}$ is the time at which x% of the EM structures have failed, and z is the standard normal variable for the cumulative distribution function (CDF) up to the fraction x.

Annex A Method of determining maximum allowable bump current at a given temperature (cont'd)

For each unique stress temperature and stress current, equation (A2) can be written as

$$t_{x\%}(I_{acc},T_{acc}) = A \cdot I_{acc}^{-n} \cdot e^{\frac{E_a}{kT_{acc}}} \cdot e^{z\cdot\sigma} \quad \text{(A3)}$$

where

$t_{x\%}(I_{acc},T_{acc})$ is the time at which x% of the EM test structures have failed at a given stress current (I_{acc}) and device temperature (T_{acc})
A is a constant (unknown)
I_{acc} is the current used in the EM test
T_{acc} is the device temperature in the EM test (K)
n is the current exponent in Black's equation
E_a is the thermal activation energy in Black's equation
k is Boltzmann's constant (8.62×10^{-5} eV/K)
$t_{x\%}$ is determined from the experimental data (e.g., t_{50} and σ for the lognormal distribution)

A similar equation can be written for the use temperature:

$$t_{x\%}(I_{use},T_{use}) = A \cdot I_{use}^{-n} \cdot e^{\frac{E_a}{kT_{use}}} \cdot e^{z\cdot\sigma} \quad \text{(A4)}$$

where

$t_{x\%}(I_{use},T_{use})$ is t_{use}: the expected lifetime (to x% failing) of the part at use temperature (T_{use}) and maximum allowable current (I_{use})

I_{use} is the maximum allowable current at T_{use} (unknown)

I_{use} and *A* are the unknowns in these two equations. z is the same in both equations since the value of x must be the same for both. Divide equation (A3) by (A4) to eliminate the constant *A*. This also eliminates the factor $\exp(z\times\sigma)$. Solving for I_{use}, we obtain

$$I_{use} = I_{acc} \cdot \left[\frac{t_{x\%}(I_{acc},T_{acc})}{t_{x\%}(I_{use},T_{use})} \cdot e^{\frac{E_a}{k}\cdot\left(\frac{1}{T_{use}}-\frac{1}{T_{acc}}\right)} \right]^{\frac{1}{n}} \quad \text{(A5)}$$

This equation is applied to each unique (I_{acc},T_{acc}) combination.

Before applying this equation, one must decide the values to use for E_a and *n*. If there are a large amount of data (e.g., at least 3 different currents and 3 different temperatures each with a sample size of >30) and multiple lots, then using the best estimate values may be appropriate. If the data is limited, then it is more prudent to use a lower y% confidence limit for each parameter, which will reduce the value of maximum current, I_{use}, obtained. The value of y is typically 90% or 95%.

Annex A Method of determining maximum allowable bump current at a given temperature (cont'd)

Suppose there are N unique (I_{acc},T_{acc}) combinations. Then N values of I_{use} are obtained. Presumably, if the data are good and the acceleration model accurate, these values should be reasonably consistent. As with metallization EM, the maximum current specified, I_{use}, should have some safety margin built in. One way to do this is to take the minimum of the N I_{use} values and make the specification some percentage lower than that. If only one lot has been tested, the specification should be considerably below the lowest calculated I_{use} because it is not known if the lot has higher or lower than average EM lifetime. If multiple lots are used, then analysis of the variation between lots can also be incorporated in setting the maximum current.

In applying DC maximum current design rules to a product application, it should be noted that the signal bump interconnections typically carry small current; only the power and ground bump interconnections carry large current. Among the power and ground bumps, there can be both spatial and temporal distribution of currents across the die. Therefore, additional statistical and modeling techniques can be applied in specific product applications.

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