JEDEC STANDARD

Thermal Modeling Overview

JESD15

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METHODOLOGY FOR THE THERMAL MODELING OF COMPONENT PACKAGES

Introduction

In recent years, the role of thermal modeling in the thermal characterization of component packages has greatly increased in importance. Unlike thermal tests, in which the basic practices have achieved a certain level of maturity, thermal modeling methods and software are undergoing rapid advancement.

Hence this document and the associated series of documents are intended to promote the continued development of modeling methods, while providing a coherent framework for their use by defining a common vocabulary to discuss modeling, creating requirements for what information should be included in a thermal modeling report, and specifying modeling procedures, where appropriate, and validation methods.

This document provides an overview of the methodology necessary for performing meaningful thermal simulations for packages containing semiconductor devices. The actual methodology components are contained in separate detailed documents.

METHODOLOGY FOR THE THERMAL MODELING OF COMPONENT PACKAGES

(From JEDEC Board Ballot JCB-08-27, formulated under the cognizance of the JC-15.1 Committee on Thermal Characterization.)

1 Scope

The modeling methodology described herein is distributed among several documents so that the appropriate combination of documents can be selected to meet specific thermal simulation requirements. This document provides the OVERVIEW. The rest of the documents are grouped as shown below:

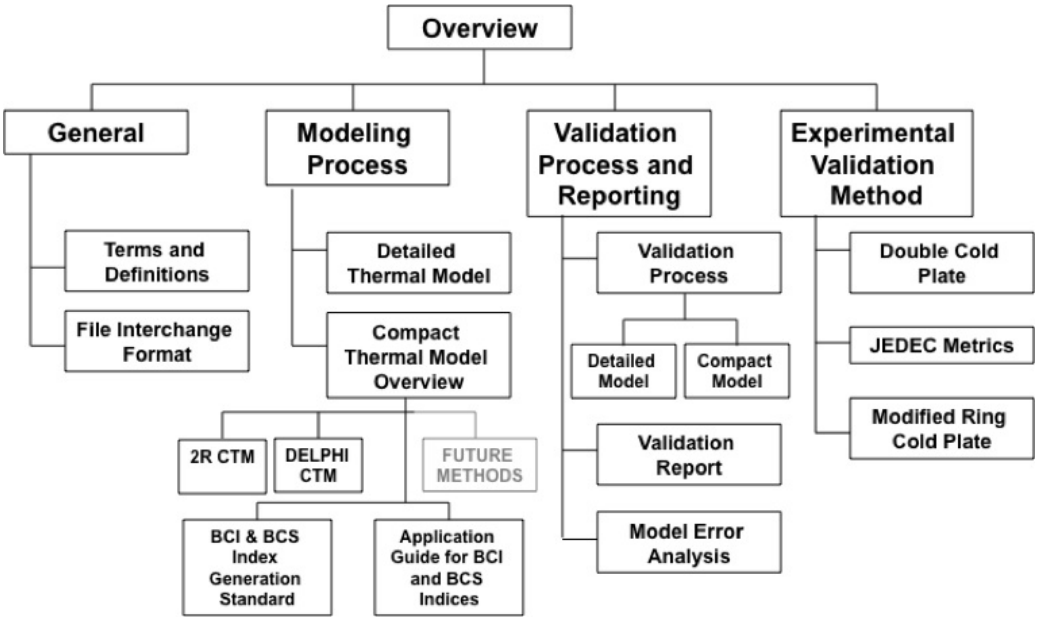

Figure 1 — Diagram indicating modular structure of component modeling documents

Because modeling methodologies and validation methods will change as technology changes, additional documents will be added to these groups as the needs arise and standards established. As appropriate, each of these documents will contain terminology and symbolic definitions specific to the material covered by the individual document.

2 Normative References

1. JESD51, *Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)*, Dec. 1995.

2. JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, May 200*5*.

3 Rationale

The junction temperature of a semiconductor device greatly influences the performance, reliability, and cost of the device. In recent years, thermal modeling has assumed increased importance in characterizing individual components and predicting their junction temperature in both standard test and application environments.

This document and the subsequent documents it calls on, provide a consistent framework for reporting thermal model results and the modeling and validation methods used. In particular cases documents provide guidance in the use of particular modeling methods.

The data can be used for package design evaluation, device (i.e., chip/package combination) characterization, reliability predictions, system-level thermal analyses, etc.

4 Purpose

The output of a model is typically a junction temperature. However, it is common to extract temperatures and fluxes from many locations in a model.

If the situation being modeled consists of a component in a simulated JEDEC test environment, it is possible to extract thermal resistances and thermal characterization parameters[1,2].

5 Results Presentation

The results of a model are not meaningful unless all the pertinent assumptions are provided along with them. The reporting requirements will depend upon the type of modeling methodology. The reporting requirements are presented in the documents in category Modeling Process.

Furthermore, the accuracy of a model should be demonstrated by using the appropriate Validation Process and Method. These documents will indicate the reporting requirements related to these procedures.

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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