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Terms, Definitions, and Letter Symbols for Microelectronic Devices

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TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES

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TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES

CONTENTS (*continued*)

Foreword

This standard will prove to be a useful guide for users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronic devices. It lists and defines the most common physical and electrical terms applicable to these devices and shows the industry-standard symbols and abbreviations that have been established for such terms.

Where applicable, reference is made to standardization documents of the following organizations:

American National Standards Institute, Inc. (ANSI)
Electronic Industries Association (EIA and JEDEC)
Institute of Electrical and Electronics Engineers (IEEE)
International Electrotechnical Commission (IEC)
National Institute of Standards and Technology (NIST)

The material contained in this standard was formulated under the cognizance of EIA/JEDEC Committee JC-10 on Terms, Definitions, and Symbols and approved by the JEDEC Board of Directors.

The text of this standard is based on JESD99B dated May 2007, which it replaces, and JEDEC Board ballots JCB-09-88 and JCB-11-56.- Annex A briefly shows entries that have been changed.

SECTION 1: PHYSICAL TERMS

1.1 Definitions of physical terms applicable to integrated circuits in general

ac test: The process of verifying the specified timing of a device.

NOTE Testing of propagation delays, minimum setup and hold times, minimum pulse durations, etc., can be performed by using test vectors applied at specified operating frequency of the device. Propagation delays of critical logic paths for system operation can be measured individually. (Ref. JESD12-1B.)

active device: A device in which at least one circuit element is an active circuit element.

application-specific integrated circuit (ASIC): An integrated circuit developed and produced for a specific application or function and for a single customer.

NOTE ASICs generally use standard cell or gate array design methodology.

application-specific standard product (ASSP): An integrated circuit developed and produced for a specific application or function but made available for multiple customers.

artwork: The original, accurately scaled, oversize drawings and plastic overlays of the microcircuit topological layout that are used to produce the master mask plates.

NOTE Artwork has largely been supplanted by computer-produced drawings and masks.

assembly, microelectronic: An assembly of unpackaged (uncased) microcircuits and/or packaged microcircuits, which may also include discrete devices, so constructed on a packaging interconnect structure that for the purpose of specification, testing, commerce, and maintenance, the package is considered to be an indivisible component. (Ref. JESD30-B.)

NOTE 1 The passive and/or active discrete and microelectronic devices may be mounted on either one or two sides of the packaging interconnect structure, and the external terminals usually exit from one side of the assembly.

NOTE 2 Many package sizes, shapes, and external terminal forms are possible.

asynchronous circuit: A circuit whose changes of state are not controlled by a single clock. (Ref. JESD12-1B.)

autodoping: The introduction of impurities from the substrate into the epitaxial layer during the process of epitaxy.

base (of a package): The part of a package that includes the surface on which a chip is intended to be mounted.

beam lead: A thick-film lead formed on and attached to the chip interconnection pattern and projecting cantilevered beyond the chip periphery for attachment to a substrate.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

bipolar-and-CMOS (BiCMOS) technology: A technology for combining bipolar transistors and silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

bipolar-and-CMOS-and-DMOS (BCD) technology: A technology for combining bipolar transistors, silicon-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices, and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.

bipolar-and-FET (BiFET) technology: A technology for combining bipolar transistors and junction-gate field-effect transistors (JFET) in a single-chip integrated circuit.

bipolar-and-MOS (BiMOS) technology: A technology for combining bipolar transistors and metal-gate metal-oxide-semiconductor (MOS) or metal-gate complementary metal-oxide-semiconductor (CMOS) field-effect devices in a single-chip integrated circuit.

bipolar technology: A technology for producing devices in which electrical conduction depends on the flow of both majority and minority carriers.

body (of a semiconductor device): The semiconductor portion of a device limited by the physical extent of the crystalline or amorphous semiconductor material and including any associated oxide layers and metallization.

bond, ball: A thermocompression bond in which the attachment wire has been fed through a capillary tube and its exposed end melted into a ball that has been attached under pressure to the bonding pad.

bond, chip: The attachment of the circuit chip to a hybrid or package substrate.

NOTE The attachment serves as a mechanical support, a thermal path, and sometimes an electrical contact.

bond, die: Synonym for “semiconductor chip bond”.

bond, face: A bond directly between a chip bonding pad and a mounting substrate for the purpose of making electrical contact.

bond, stitch: A thermocompression bond in which a capillary tube is used for both feeding the wire and forming the bond.

bond, thermocompression: A bond in which two members are joined through the combined application of heat and pressure.

bond, ultrasonic: A bond in which two members are joined through the combined application of pressure and an ultrasonic oscillatory lateral motion.

bond, wedge: A thermocompression bond in which a wedge-shaped tool is used to apply pressure to the wire being attached.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

bond, wire: The attachment between a bonding wire and a chip bonding pad or package terminal.

bonding wire: A wire that is bonded to a chip bonding pad in order to connect the chip to any other point within the device package.

boundary scan: A design methodology in which the I/O buffers of a circuit or functional block are observed and controlled by scan cells. (Ref. JESD12-1B.)

NOTE The boundary scan standard was developed by the Joint Test Action Group (JTAG) and is embodied in ANSI/IEEE Std 1149-1.

case: Synonym for “package”.

channel: A region of semiconductor material in which current flow is influenced by a transverse electrical field.

NOTE 1 A channel may physically be an inversion layer, a diffused layer, or bulk material.

NOTE 2 The type of channel, i.e., p-channel or n-channel, is determined by the type of majority carrier during conduction.

charge pump: (1) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected in series with that source to make available a voltage greater than that of the source.

NOTE This type of dc-to-dc converter is sometimes called a voltage doubler or, when several stages are cascaded, a voltage multiplier.

(2) A dc-to-dc converter in which a capacitor is charged from a voltage source and then electrically reconnected to make available a voltage whose polarity is opposite to that of the source.

chip: A separated part of a wafer (or, in some cases, a whole wafer) intended to perform a function or functions in a device.

chip, beam-lead: A chip employing electrical terminations in the form of tabs extending beyond the edge of the chip for direct bonding to a mounting substrate.

chip carrier: A package whose chip cavity or mounting area occupies a major fraction of the package area and whose terminals consist of metal pad surfaces (on leadless versions) or leads formed around the sides and under the package or out from the package (on leaded versions).

NOTE The term “chip carrier” has been replaced by “quad flatpack” (for terminals on three or four sides) and “small-outline package” (for terminals on one or two sides).

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

chip, face-down: A chip whose electrical terminations are on the side that is intended to be attached to the mounting substrate.

chip, face-up: A chip whose electrical terminations are on the side opposite the one that is intended to be attached to the mounting substrate.

chip, flip: A chip with bump contacts spaced around the device and intended for face-down mounting.

circuit element: Any constituent part of a circuit that contributes directly to its operation and performs a definable function.

NOTE 1 Examples include transistors, resistors, capacitors, inductors, and interconnections.

NOTE 2 The definition in JESD12-1B excludes interconnections.

circuit element, active: A circuit element that contributes qualities to a circuit function other than those contributed by a passive circuit element, e.g., rectification, switching, gain, or conversion of energy from one form to another.

NOTE 1 Examples include diodes, transistors, active integrated circuits, and light-sensing or light-emitting devices.

NOTE 2 Active physical circuit elements may also be used to act as passive physical circuit elements, e.g., to provide resistance and/or capacitance to a circuit function.

circuit element, parasitic: A circuit element that is an unavoidable adjunct of one or more other circuit elements.

circuit element, passive: A circuit element primarily contributing resistance, capacitance, inductance, ohmic interconnection, or a combination of these to a circuit function.

NOTE Examples include resistors, capacitors, inductors, passive filters, and interconnections.

clock distribution network: The structure by which clock signals are distributed within a device. (Ref. JESD12-1B.)

clock skew: The difference in the arrival times of a common clock edge at any two circuit elements. (Ref. JESD12-1B.)

CMOS-and-DMOS (C/DMOS) technology: A technology for combining complementary metal-oxide-semiconductor (CMOS) field-effect devices and double-diffused metal-oxide-semiconductor (DMOS) field-effect transistors in a single-chip integrated circuit.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

complementary integrated circuit technology: The technology, as applied to integrated circuits, whereby active elements of both polarities are fabricated as single-chip elements on or within the same substrate.

NOTE For example, a complementary bipolar semiconductor integrated circuit is one that employs both npn and pnp bipolar transistors in the same semiconductor substrate, and a complementary MOS integrated circuit is one that employs both n-channel and p-channel field-effect transistors in the same semiconductor substrate.

complementary metal-oxide semiconductor (CMOS) technology: A technology for combining p-channel and n-channel metal-oxide-semiconductor field-effect transistors in a single-chip integrated circuit.

component (1) **(general):** A constituent part.

NOTE 1 Examples include source and drain regions as components of transistors, lead frames and dice/dies as components of packaged integrated circuits, resistors and integrated circuits as components of printed circuit boards, motherboards as components of computers, LCD screens as components of monitors, ac and dc components of complex waveforms, and loops and algorithms as components of software programs.

NOTE 2 Unless the context identifies the thing of which a component is a part, a descriptive prepositional phrase identifying the thing should follow the word “component”.

(2) (of a hybrid integrated circuit): A part that is mounted within the package and that contributes to the composition of the circuit.

NOTE For electronic components, a distinction is made between integrated components and discrete components.

component, active (of a hybrid integrated circuit): A component in which at least one circuit element is an active circuit element.

component, discrete (of a hybrid integrated circuit): A discrete device that serves as a component of a hybrid integrated circuit.

component, integrated (of a hybrid integrated circuit): An integrated circuit, completed or partially completed, that serves as a component of a hybrid integrated circuit.

component, passive (of a hybrid integrated circuit): A component in which all circuit elements are passive.

connection, electrical (within a semiconductor device): An electrically conducting element that functions as a pathway between other elements, including terminals, and whose primary purpose is to conduct electric current in a confined manner.

NOTE The connection may either consist of a separate conductive entity such as a wire or metallic film or be an integral part of the body.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

contact, bump; ball contact; raised pad; pedestal: (1) A contacting pad that rises substantially above the surface level of the chip.

(2) A raised pad on the substrate that contacts a flat land area of the chip.

critical path: A signal path that determines the performance of a design.

crossover: A crossing where a portion of an interconnect pattern passes over a portion of another interconnect pattern and is separated from it by a thin dielectric layer.

crossunder: A crossing where a conductive path fabricated into the active substrate for the sole purpose of interconnection passes under a portion of an interconnect pattern and is separated from it by a thin dielectric layer.

customer-specific standard product (CSSP): An integrated circuit developed and produced for a single customer but for multiple applications or functions.

custom integrated circuit: An integrated circuit developed or produced to conform to unique requirements.

NOTE The terms “full custom” and “semicustom” refer to layout methodologies. The choice of term is subjective, depending on the interpretation of the ratio of unique layouts to standard macrocell layouts from a library.

dc test: A test during which only steady-state voltages and currents are applied to the device.

NOTE DC tests are generally used to determine input levels, output levels, or dissipation characteristics of devices.

deposition: The process of applying a material to a substrate by means of vacuum, electrical, chemical, screening, or vapor methods.

deposition, vapor-phase: The deposition of conductive, resistive, insulating, or semiconductor films onto a substrate from a source material in the vapor phase by physical deposition or chemical reaction.

device: A piece of equipment, a mechanism, or another entity designed to serve a special purpose or perform a special function.

NOTE 1 In JEDEC documents, the word “device” is often used as an abbreviated reference to the type or types of solid-state devices that are within the scope of those documents. Context could indicate otherwise; e.g., in the phrase “the device used to hold the device under test”, the first usage of the word “device” refers to a mechanism; the second to a solid-state device.

NOTE 2 Contrast with “component”.

die (pl. dice; dies): Synonym for “chip”.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

diffusion, impurity: A process used to introduce desired impurities into a semiconductor crystal to alter its electrical properties; it is accomplished by introducing suitable dopants to the surface of the semiconductor wafer under precisely controlled conditions, usually at high temperatures.

diode, barrier: Synonym for "diode, Schottky".

diode, hot-electron: Synonym for "diode, Schottky".

diode, Schottky: A diode formed by depositing a metal film on a semiconductor surface of sufficiently high resistivity to form an energy barrier.

NOTE A Schottky diode is sometimes used as part of a bipolar transistor structure.

diode, semiconductor: In its simplest form, any p-n junction but, in microcircuits, often a modified bipolar transistor.

NOTE Modifications include shorting the base to the collector, shorting the emitter to the collector, using the emitter-base diode with the collector open, or using the collector-base diode with the emitter open.

discrete (semiconductor) device: A semiconductor device that is specified to perform an elementary electronic function and is not divisible into separate components functional in themselves.

NOTE 1 Diodes, transistors, rectifiers, thyristors, and multiple versions of these devices are examples. Other semiconductor structures having the physical complexity of integrated circuits but performing elementary electronic functions (e.g., complex Darlington transistors) are usually considered to be discrete semiconductor devices.

NOTE 2 If a semiconductor device is not considered to be an integrated circuit in both complexity and functionality, it is considered to be a discrete device.

discretionary wiring: A technique for interconnecting subarrays on a single wafer in which each subarray is electrically tested by probing and the desired array function is attained by the use of a metallization pattern that connects only usable subarrays.

dislocation: An atomic imperfection or fault in the crystalline lattice structure.

NOTE 1 The two types are edge dislocations (if a row of atoms is removed or displaced and the slippage is at right angles to the displacement) and screw dislocations (if the slippage is parallel).

NOTE 2 If dislocations appear at the surface of the crystal, they are sometimes referred to as surface dislocations.

dopant: A chemical element that is introduced into the lattice structure as an impurity to form desired properties.

NOTE Examples are phosphorus and boron used to create n- and p-regions, respectively, in silicon.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

double-diffused MOS (DMOS) technology: A technology for producing silicon-gate metal-oxide semiconductor field-effect transistors such that 1) the threshold voltage, V_T, is determined by the intersection of two doping profiles, and 2) the device channel length is defined by the diffusion characteristics rather than by a photolithographic self-aligned gate structure.

electrode (of a semiconductor device): An element that performs one or more functions of emitting or collecting electrons or holes, or of controlling their movements by an electric field.

electrostatic-discharge-sensitive device: A discrete device or integrated circuit that may be permanently damaged by electrostatic potentials encountered in routine handling, testing, and shipping.

NOTE In documents of the IEC and CENELEC, the abbreviation ESDS stands for "electrostatic-discharge-sensitive device"; in the USA, ESDS stands merely for "electrostatic discharge sensitive" or "electrostatic discharge sensitivity", and "ESDS device" is not further abbreviated. The abbreviation ESD stands for "electrostatic discharge".

element, distributed circuit: The physical realization of an element incorporating more than one primary electrical characteristic (resistance, capacitance, inductance, gain, etc.) dispersed along the length of the element.

embedding: A process using polymers or similar materials that can be hardened to produce a body enclosing, and in contact with, the electronic assembly, for example, casting, potting, dip-coating, and transfer molding.

epitaxial layer: A monocrystalline layer formed by epitaxy, which is normally of a different conductivity type or resistivity from the substrate material.

epitaxial peak: An irregular raised point of epitaxial material on an epitaxial surface.

epitaxy: Deposition of a monocrystalline layer of material on a substrate material such that the layer thus formed has the same crystal orientation as the substrate.

NOTE Examples are silicon on silicon and silicon on sapphire.

etch pit: A small peak or hole produced by chemical etching at the site of an imperfection in a semiconductor or other surface and caused by the differing etch rate at the point of imperfection.

etchant: A solution used for etching.

etching: A process in which a controlled quantity or thickness of material is removed (often selectively) from a surface by chemical reaction, electrolysis, or other means.

etching, plasma: A process in which material is removed by a reaction with chemically active radicals created by an ion bombardment in a glow discharge.

NOTE A mask is usually used in order to remove only selected areas.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

fan-in: The number of output ports on a net. (Ref. JESD12-1B.)

fan-out: The number of input ports on a net. (Ref. JESD12-1B.)

fault coverage: The percentage of possible faults detected by a set of test vectors. (Ref. JESD12-1B.)

fault simulation: The process of applying test vectors to a circuit or circuit model to obtain fault-coverage information. (Ref. JESD12-1B.)

film (of a film integrated circuit): A layer of solid material formed by any deposition process upon the substrate or upon other films deposited on the substrate.

film, plated: A film obtained through chemical and/or electrochemical deposition.

film technology, thick-: The technology with which electronic circuits or elements are formed by applying a liquid, solid, or paste coating through a screen or mask in a selective pattern onto a supporting material.

NOTE This technology also includes films deposited by any other means when the films so formed are five micrometers or greater in thickness.

film technology, thin-: The technology with which electronic circuits or elements are formed by vapor deposition, vacuum deposition, or sputtering of films onto a supporting material.

NOTE This technology also includes similar techniques when the films so formed are less than five micrometers in thickness.

film, thick (of a film integrated circuit): A film produced by a printing process, serigraphy, or other related techniques.

film, thin (of a film integrated circuit): A film produced by an accretion process such as vapor-phase deposition or sputtering.

firing: A process of thick-film formation whereby the screened film is subjected to a precisely controlled high-temperature condition that oxidizes and vaporizes organic binders and modifies the film microstructure to achieve desired properties, including adherence to the substrate.

fixed interconnect pattern: A metallization pattern that interconnects circuit elements and is defined by a single, predesigned mask.

flatpack: A package whose leads project parallel to, and are designed primarily to be attached parallel to, the seating plane. (Ref. JESD30C.)

NOTE The term “flatpack” has been replaced by “quad flatpack” (for terminals on three or four sides) and “small-outline package” (for terminals on one or two sides).

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

floating node: A signal line that is not actively forced to a defined high or low level. (Ref. JESD12-1B.)

NOTE In a high-impedance state, the charge (or lack of charge) is trapped at the node with no path to supply or ground voltages.

foil: A relatively thin layer of solid material that can be handled independently of a substrate.

functional block: A part of a circuit having a defined function that can be designated by a single symbol in a schematic representation. (Ref. JESD12-1B.)

functional density: The number of gates used divided by the entire chip area. (Ref. JESD12-1B.)

NOTE Units are gates used per unit area.

functional simulation: The process of exercising a particular netlist and functional models by applying input stimuli to observe the functional responses without regard to timing. (Ref. JESD12-1B.)

functional test: The process of verifying the specified functions of a device without regard to timing. (Ref. JESD12-1B.)

gate equivalency of a function (GEF): The number of gate equivalents used to implement a function. (Ref. JESD12-1B.)

gate equivalent (for CMOS): The minimum circuitry necessary to implement a two-input NAND gate. (Ref. JESD12-1B.)

gate equivalent (for ECL): One-eleventh of the minimum circuitry necessary to implement a single-bit full-adder. (Ref. JESD12-1B.)

gate, (logic): A combinational logic function consisting of a number of inputs and outputs and performing one of the Boolean functions AND, OR, exclusive OR, NAND, NOR, or exclusive NOR.

NOTE For the purpose of specifying complexity, (1) buffers and inverters are counted as gates and (2) exclusive OR and exclusive NOR gates, some high-input-count gates, and memory functions are counted as multiple gates.

geometry, process: The minimum allowable drawn dimensions for designing an integrated circuit using a specified technology. (Ref. JESD12-1B.)

heat sink; heat dissipator: A separable element or integral part of the package that aids in dissipating the heat produced within the package.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

integrated circuit (IC): A circuit in which all or some of the circuit elements are inseparably associated and electrically interconnected so that it is considered to be indivisible for the purposes of construction and commerce. (Ref. IEC 748-1.)

NOTE 1 JEDEC and IEC standards on semiconductor integrated circuits generally refer to integrated circuits that are designed as microcircuits.

NOTE 2 To further define the nature of an integrated circuit, additional qualifiers may be prefixed. Examples include
#

– single-chip integrated circuit,

– multichip integrated circuit,

– thin-film integrated circuit,

– thick-film integrated circuit,

– hybrid film integrated circuit, and

– hybrid semiconductor integrated circuit.

integrated circuit, active hybrid film: A hybrid film integrated circuit in which at least one circuit element is active.

integrated circuit, analog: A type of linear integrated circuit intended to be used so that the output is a continuous mathematical function of the input.

NOTE An operational amplifier is an example of an analog integrated circuit.

integrated circuit, application-specific: See “application-specific integrated circuit”.

integrated circuit, binary: A digital integrated circuit limited to two logic states at each of its input and output terminals.

NOTE The high-impedance state of a three-state output is not considered to be a logic state.

integrated circuit, custom: See “custom integrated circuit”.

integrated circuit, digital: A type of integrated circuit that is intended to accept particular logic states, changes between logic states, or sequences of logic states at its input terminals, and convert these to logic states at its output terminals according to a set of logic equations or function tables.

integrated circuit, film (FIC): An integrated circuit whose circuit elements, including the interconnections, are exclusively film elements formed on the surface of an insulating substrate.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

integrated circuit, hybrid (HIC): An integrated circuit that contains two or more of a single type or a combination of types of the following elements, with at least one of the elements being active: film microcircuit, monolithic microcircuit, discrete semiconductor device, passive chip, or passive element printed or deposited on a substrate. (Ref. JESD93.)

integrated circuit, hybrid film: A film integrated circuit in which the main parts of the circuit elements are produced as film elements on a substrate and that is completed by mounting additional components on the substrate or elsewhere in the package.

integrated circuit, hybrid semiconductor: A semiconductor integrated circuit in which the main parts of the circuit elements are produced as semiconductor circuit elements and that is completed by mounting additional components in the package.

integrated circuit, interface: An integrated circuit that accomplishes the linkage of two systems or parts of a system that would otherwise be incompatible.

NOTE The signals present at the inputs and the outputs of the interface integrated circuit may take any one of the following forms:

a) digital inputs, analog outputs;

b) analog inputs, digital outputs;

c) analog inputs, analog outputs; or

d) digital inputs, digital outputs. (In this case, the levels of the digital signals at the inputs and the outputs are dissimilar.)

Some circuits of types a, b, and c may also be classified as linear integrated circuits.

integrated circuit, linear: Through common usage, an integrated circuit that is not purely digital.

NOTE Some circuits of this type may also be classified as interface integrated circuits.

integrated circuit, monolithic (semiconductor): Deprecated synonym for “integrated circuit, single-chip”.

integrated circuit, multichip: A semiconductor integrated circuit containing two or more chips (dice).

NOTE The use of the term “polylithic semiconductor integrated circuit” is deprecated.

integrated circuit, pad-limited: An integrated circuit whose chip size is determined by the number of pads required. (Ref. JESD12-1B.)

integrated circuit, passive hybrid film: A hybrid film integrated circuit in which all circuit elements are passive.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

integrated circuit, semiconductor: A semiconductor device designed as an integrated circuit.

integrated circuit, silicon-compiled: An integrated circuit generated entirely by a silicon compiler. (Ref. JESD12-1B.)

integrated circuit, single-chip: An integrated circuit or microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate. (Ref. JESD93.)

integrated circuit, thick-film: A film integrated circuit whose circuit elements are thick-film elements.

integrated circuit, thin-film: A film integrated circuit whose circuit elements are thin-film elements.

NOTE Usually, thin-film elements are formed by vacuum-deposition techniques, possibly supplemented by other deposition techniques.

integrated circuit, very-high-speed (VHSIC): An integrated circuit meeting the following goals for speed and density established by the U.S. Department of Defense:

Goal	Phase 1	Phase 2
Minimum product of operating frequency and equivalent gate density	5×10^{11} Hz C gates / cm^2	1×10^{13} Hz C gates / cm^2
Minimum clock frequency	25 MHz	100 MHz

interconnect layer: A conductive layer used for electrical interconnection of circuit elements on an integrated circuit. (Ref. JESD12-1B.)

ion implantation: A method for doping semiconductors wherein the desired dopant is ionized and accelerated by an electric field, penetrates the surface, and is deposited within the semiconductor material.

isolation, dielectric: Electrical isolation of one or more elements of a single-chip semiconductor integrated circuit, achieved by surrounding the elements with an insulating barrier such as semiconductor oxide.

isolation, junction: Electrical isolation of one or more elements of a single-chip semiconductor integrated circuit, achieved by surrounding the element(s) with a region of the conductivity type that forms a junction and reverse-biasing that junction.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

layer, accumulation: A surface region of a semiconductor device whose conductivity type is the same as that produced by the net fixed charge density of ionized donors and acceptors and whose net carrier density is higher than that necessary for neutralization due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

layer, buried: A distinguishable region introduced under a semiconductor circuit element, for example, under the collector region of a transistor to reduce the series collector resistance.

layer, depletion (associated with a surface): A surface region of a semiconductor device whose conductivity type is the same as that produced by the net fixed charge density of ionized donors and acceptors but whose net carrier density is insufficient for neutralization due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

layer, depletion (associated with a p-n semiconductor junction): A region whose conductivity type on each side of the junction is the same as that produced by the net fixed charged density of ionized donors and acceptors but whose net carrier density is insufficient for neutralization due to the built-in potential barrier of the p-n junction and, if present, an applied reverse bias.

layer, diffused: The region of a semiconductor into which impurity dopants have been diffused to a concentration of at least the background concentration.

NOTE The region is often delineated by a p-n junction.

layer, enhancement: Synonym for “accumulation layer”.

layer, inversion: A surface region of a semiconductor device whose conductivity type has been reversed from that produced by the net fixed charge density of ionized donors and acceptors due to charge carrier attraction.

NOTE The charge carrier attraction may be caused by a field-plate voltage such as in field-effect transistors or by unwanted charge residing in surface states, insulating layers, or surface ionic species.

lead frame (of a package): A metal frame providing external terminals and mechanical support to align them.

load, input: The load (usually specified in unit loads) represented by a given input. (Ref. JESD12-1B.)

load, output: The load on an output (usually specified in unit loads). (Ref. JESD12-1B.)

logic feedback: A circuit configuration in which the output of a logic circuit controls an input signal to the same circuit. (Ref. JESD12-1B.)

LSI: Large-scale integration.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

mask: A patterned screen of any of several materials and types used in shielding selected areas of a semiconductor, photosensitive layer, or substrate from radiation during processing, so that the unshielded areas can be further processed to reproduce the chosen pattern.

NOTE The type of mask can be designated either by type (e.g., oxide mask or metal mask) or by function (e.g., diffusion mask or vapor-deposition mask).

master slice: An unmetalized wafer containing arrays of circuit elements as determined by subsystem requirements.

NOTE These circuit elements can be interconnected in a variety of ways to achieve different functions.

metal-insulator-semiconductor (MIS) technology: A technology for producing circuits and circuit elements having the form of a semiconductor-insulator-metal layered structure.

NOTE Field-effect transistors, capacitors, varactors, nonlinear resistors, variable-threshold diodes, and similar circuit elements can be produced with this technology.

metallization: A thin-film conductor or network of such conductors used to interconnect microcircuit elements.

metallization, bottom: The metallization on the bottom surface of a chip that permits bonding it to a mounting substrate.

metallization, multilayer: A metallization pattern in which the conductive network is fabricated in more than one plane and separated, except at desired contact points, by thin dielectric films.

metal-nitride-oxide-semiconductor (MNOS) technology: A subcategory of metal-insulator-semiconductor (MIS) technology in which the insulation employed is a nitride-oxide layer.

metal-oxide-semiconductor (MOS) technology: A subcategory of metal-insulator-semiconductor (MIS) technology in which the insulator employed is an oxide of the semiconductor substrate material.

NOTE The term MOS is often misused to include other categories of insulated-gate technology such as MNOS (metal-nitride-oxide-semiconductor) and SIS (silicon-gate-insulator-semiconductor).

microcircuit: A microelectronic device that has a high circuit-element and/or component density and that is considered to be a single unit. (Ref. IEC 748-1.) (See also “integrated circuit”.)

microcircuit, analog: Synonym for “integrated circuit, analog”.

microcircuit, binary: Synonym for “integrated circuit, binary”.

microcircuit, digital: Synonym for “integrated circuit, digital”.

microcircuit, film: Synonym for “integrated circuit, film”.

microcircuit, hybrid: Synonym for “integrated circuit, hybrid”.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

microcircuit, interface: Synonym for “integrated circuit, interface”.

microcircuit, linear: Synonym for “integrated circuit, linear”.

microcircuit, logic: Synonym for “integrated circuit, digital”.

microcircuit module: An assembly of microcircuits, or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions and so constructed that, for the purpose of specification, testing, commerce, and maintenance, it is considered to be indivisible.

microcircuit, multichip: Synonym for “integrated circuit, multichip”.

microelectronics: That field of science and engineering that deals with highly miniaturized electronic components and their use. (Ref. IEC 748-1.)

minimization: The process of eliminating redundancy in logic implementation. (Ref. JESD12-1B.)

model: A representation of an electronic circuit. (Ref. JESD12-1B.)

morphology, integrated: The structural characterization of an electronic component in which the current- or signal-modifying areas, patterns, or volumes have lost their identities in the integration of electronic materials, in contrast to an assembly of devices performing the same function.

morphology, translational: The structural characterization of an electronic component in which the areas or patterns of resistive, conductive, dielectric, and active materials in or on the surface of the structure can be identified in a one-to-one correspondence with devices assembled to perform an equivalent function.

MSI: Medium-scale integration.

multilayer(-connection) film circuit: A circuit having more than one layer of film interconnections separated by at least one insulating film or gap.

no (internal) connection (NC): A terminal that has no internal connection and that can be used as a support for external wiring without disturbing the function of the device, provided that the voltage applied to this terminal (by means of the wiring) does not exceed the highest supply voltage rating of the circuit.

NOTE 1 If higher voltages are acceptable, this should be stated.

NOTE 2 The IEC equivalent term is “blank terminal”; nevertheless, the IEC abbreviation is NC.

nonusable terminal (NU): A terminal that is not to be used in normal applications and that may or may not have an internal connection.

optimization (of logic): The process by which a given logic representation is reduced to a superior equivalent functional representation with respect to some system or chip-level design objective such as speed, device utilization, level of logic, etc. (Ref. JESD12-1B.)

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

oxide, deposited: An oxide layer formed on a surface by methods not requiring the substrate to participate in the reaction.

NOTE Various methods such as pyrolysis, evaporation, or sputtering may be employed.

oxide, grown: An oxide layer formed on a semiconductor surface by the reaction of the semiconductor material with oxygen.

oxide step: A sharp variation of the plane of the oxide on the surface of a planar device.

package (of a semiconductor device): An enclosure for one or more semiconductor chips (dice), film elements, or other components, that allows electrical connection and provides mechanical and environmental protection.

pad, bonding: An area on a chip to which a connection can be made.

pad cell area: The physical area available for external electrical and mechanical interface. (Ref. JESD12-1B.)

parametric test: The process of verifying the specified dc parameters of a device. (Ref. JESD12-1B.)

passivation: The formation of an insulating layer directly over a semiconductor surface to protect the surface from contaminants, moisture, and particles.

NOTE Usually an oxide of the semiconductor is used; however, deposition of other materials is also used.

passive device: A device in which all circuit elements are passive.

photoresist: A photosensitive film used in conjunction with photolithography forming a protective mask on a wafer or substrate surface to effect selective process action (e.g., diffusion, etching, etc.).

pinhole: An imperfection in the form of a small hole that penetrates through a layer of material. (Ref. IPC-T-50.)

planar (device and **process):** A type of semiconductor device and the process technology used to fabricate it, in which all of the p-n junctions terminate at approximately the same geometric plane on the surface of the semiconductor.

NOTE Devices using similar technologies, but having one or more diffused areas lying in a slightly different, parallel plane, are also considered planar (e.g., buried collector).

protective coating: A layer of insulating material applied over the circuit elements for the purpose of mechanical and environmental protection and prevention of contamination.

radiation hardening: (1) Increasing the ability of a device to survive one or more types of radiation.

(2) The process whereby the ability of a device to survive one or more types of radiation is increased.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

reactive ion etching (RIE): A plasma etching process using a relatively low gas pressure and high electric field, in which material is removed primarily by chemical reaction with active radicals although some material may also be removed physically by ion bombardment.

NOTE 1 A mask is usually used in order to remove only selected areas.

NOTE 2 By convention the wafer is mounted on the "hot" RF electrode.

registration mark; alignment mark; fiducial mark: A mark, on a wafer or substrate, that is used for aligning successive processing masks.

resistor, bulk-collector: A semiconductor resistor formed by isolating a region of the epitaxial material that, in other regions, forms the collectors of the transistors.

resistor, diffused: The normal semiconductor resistor formed by diffusing a junction-isolated region of proper length, width, and sheet resistance to provide the desired resistance value.

resistor, film: A resistor formed by deposited films, usually metal, on an insulating substrate or the semiconductor oxide on an integrated-circuit chip surface.

resistor, pinch: A semiconductor resistor formed by diffusing the opposite conductivity type, normally during the emitter diffusion, into a portion of the diffused resistor length in order to obtain a very high sheet resistance.

scan cell: A bistable element that includes one or more ports used to observe and control that element's state when the port or ports are enabled. (Ref. JESD12-1B.)

scan, full: A methodology of design in which every bistable element is a scan cell. (Ref. JESD12-1B.)

scan, partial: A methodology of design in which some, but not all, bistable elements are scan cells. (Ref. JESD12-1B.)

Schmitt trigger: A digital circuit designed to have significant hysteresis, i.e., the difference between the positive-going and negative-going input threshold voltages, and usually having only one input.

NOTE Schmitt triggers have one hysteresis-causing mechanism. Sometimes this mechanism is applied to a single transistor having multiple inputs and performing a basic logic function as in a TTL NAND gate. These gates have been called NAND Schmitt triggers. It is necessary for all their inputs to be simultaneously above the positive-going threshold voltage to cause the output to go high.

Other integrated circuits have one or more inputs each having its own hysteresis-causing mechanism. These are not usually called Schmitt triggers per se. A NAND gate each of whose inputs separately has hysteresis might be called a NAND gate with Schmitt-trigger inputs.

The latter device differs from the NAND Schmitt triggers in that one input at a time can reach its positive-going threshold voltage, then drop back staying above the negative-going threshold voltage. When the last input reaches its positive-going threshold voltage, the output goes low.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

screen-printing (of a thick-film circuit): The deposition of conductive, resistive, or insulating films onto a substrate by pressing pastes (“inks”) through screens.

semiconductor device (general term)**:** A device whose essential characteristics are due, in whole or in part, to the flow of charge carriers within a semiconductor.

NOTE For specification purposes, a semiconductor device must be considered to be either a discrete semiconductor device or an integrated circuit.

semiconductor (material) (within a semiconductor device): A material in which the electric current is made up of both negative and positive mobile charge carriers (conduction electrons and holes).

semiconductor (nonspecific)**:** A substance whose conductivity due to the charge carriers of both signs is normally in the range between that of metals and insulators and in which the charge carrier density can be changed by external means.

sheet resistance: The electrical resistance of a diffused layer or of a thin sheet of material with uniform thickness as measured across opposite sides of a square pattern.

NOTE Sheet resistance is usually expressed in ohms per square.

signal, analog: A signal that is used in such a manner that any change in magnitude of some characteristic conveys information.

NOTE The characteristic may be the amplitude, phase, frequency, etc., of a quantity such as voltage, current, impedance, etc.

signal, digital: A signal that is used in such a manner that changes between ranges in a finite set of nonoverlapping ranges of the magnitude of some characteristic convey information.

NOTE 1 The characteristic may be the amplitude, phase, frequency, etc., of a quantity such as voltage, current, impedance, etc.

NOTE 2 For convenience, each range of values can be represented by a single value, i.e., the nominal value.

silicon-gate-insulator-semiconductor (SIS) technology: A technology similar to metal-insulator-semiconductor (MIS) technology except that the gate is silicon instead of metal.

silicon-nitride-oxide-semiconductor (SNOS) technology: A subcategory of silicon-gate-insulator-semiconductor (SIS) technology in which the insulation employed is a nitride-oxide layer.

silicon-on-sapphire (SOS) technology: The technology whereby monocrystalline films of silicon are epitaxially deposited onto a single-crystal sapphire substrate to provide the basic structure for the fabrication of dielectrically isolated active and/or passive elements.

silicon-oxide-nitride-oxide-semiconductor (SONOS) technology: A subcategory of silicon-gate-insulator-semiconductor (SIS) technology in which the insulation employed is an oxide-nitride-oxide layer.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

solid-state (within the scope of JEDEC): Relating to, or utilizing, those electrical, magnetic, optical, thermal, and/or chemical properties of semiconductors that are based on the arrangement or behavior of atoms, ions, molecules, nucleons, electrons, holes, and/or imperfections.

solid-state circuit: Synonym for "integrated circuit, single-chip".

solid-state component: A solid-state device that is, or is intended to be, a constituent part of a higher order assembly.

NOTE Examples of solid-state components include DRAMs as parts of memory modules and microprocessors as parts of motherboards.

solid-state device: An electronic device whose operation depends on the properties of the integral solid semiconductor materials.

NOTE 1 Examples of solid-state devices include discrete transistors, discrete thyristors, discrete transient voltage suppressors, discrete semiconductor pressure sensors, integrated circuits, modules consisting mainly of integrated circuits such as multichips and hybrids, and memory modules such as DIMMs and SIMMs.

NOTE 2 Electromechanical devices, e.g., solenoids, breakers, wire relays, are not considered to be solid-state devices.

solid-state drive: A nonvolatile storage device including a controller and one or more solid-state memories, typically using traditional hard disk drive (HDD) interfaces (protocol and physical) and form factors.

solid-state industry: Those companies and organizations whose primary function is associated with design, fabrication, assembly, test, inspection, and/or distribution of solid-state devices.

solid-state memory: An integrated circuit, or a portion thereof, whose primary function is storage.

solid-state physics: The study of the physical properties of solids, with special emphasis on the electrical, magnetic, optical, thermal, and chemical properties of semiconducting materials in relation to their electronic structure.

solid-state technology: The applied sciences and skills of developing and manufacturing solid-state devices.

space-charge region (of a semiconductor device): A functional region in which the net charge density is significantly different from zero. (Ref. ANSI/IEEE Std 100.)

NOTE 1 The net charge is caused by electrons, holes, and ionized acceptors and donors.

NOTE 2 The space-charge regions of a semiconductor device include accumulation (enhancement), depletion, and inversion layers.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

sputter cleaning; back sputtering: A process in which material is physically removed from a designated surface by bombardment of ions generated in a plasma.

NOTE The gas used is generally inert or nonreactive, e.g., argon or helium.

sputtering: A process for forming thin films in which ion bombardment is used to free particles from a solid source that are then deposited onto another nearby surface.

SSI: Small-scale integration.

standard product, (integrated circuit): An integrated circuit developed and produced for multiple applications or functions and made available for multiple customers.

subelement: A distinguishable portion of a microcircuit element.

EXAMPLE The emitter, collector, and base of an integrated bipolar transistor are subelements of an integrated circuit.

substrate (of a film integrated circuit): A piece of material forming a supporting base for film circuit elements and possibly additional components.

substrate (of a semiconductor device): (1) The part of the original material that remains essentially unchanged when the device elements are formed upon or within the original material.

NOTE 1 The original material may be a layer of semiconductor material cut from a single crystal, a layer of semiconductor material deposited on a supporting base, or the supporting base itself.

(2) The original semiconductor material being processed.

NOTE 2 The intended meaning will usually be clear from the context in which the term is used. If necessary, distinction can be made between the “original substrate” and the “remaining substrate”.

substrate, active: A substrate in which active elements are implemented within the substrate material.

substrate, passive: A substrate that serves primarily as a structural support or mounting surface for functional circuit elements.

surface state: The energy levels associated with charge that resides on the surface of a semiconductor.

surface-state charge density: The net charge density on the surface of a semiconductor.

NOTE Both the charge density and the energy levels may be influenced by such factors as the insulation layer, surface discontinuities, chemicals, ultraviolet radiation, and electrical or magnetic fields.

synchronous circuit: A circuit whose changes of state are controlled by a single clock signal. (Ref. JESD12-1B.)

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

terminal (of a semiconductor device): An externally available point of connection.

NOTE The use of the term “termination” as a synonym is deprecated because that term denotes the external elements connected to the terminal.

tester strobe time: The time interval from the beginning of a test clock cycle to the instant when an output of a device is observed and compared to an expected result. (Ref. JESD12-1B.)

test pattern: A circuit or elements processed in the semiconductor wafer to act as test sites for monitoring fabrication processes.

three-state bus: A bus on which each output port can be placed at a logic high level or a logic low level or in a high-impedance state. (Ref. JESD12-1B.)

topology: The surface layout design of a microcircuit, applied chiefly to the preparation of the masks used in fabrication.

transistor, bipolar: A transistor in which electrical conduction depends on the flow of both majority and minority carriers.

transistor, collector field-effect: A modified junction field-effect transistor, used as a constant-current source, whose gate is connected to the substrate.

NOTE The channel is formed from the epitaxial material that in other regions forms the collectors of the bipolar transistors.

transistor, field-effect (FET): A transistor in which the conduction is due entirely to the flow of majority carriers and can be varied by an electric field produced by an auxiliary source.

transistor, insulated-gate field-effect (IGFET): A field-effect transistor having one or more gate electrodes that are electrically insulated from the channel.

transistor, junction-gate field-effect (JFET): A field-effect transistor having one or more gates that form p-n junctions with the channel.

transistor, lateral: A transistor whose emitter-base and collector-base junctions are formed in separate topological areas of a microcircuit and in which the charge carriers flow between these junctions in a plane parallel to the surface.

transistor, metal-oxide-semiconductor field-effect (MOSFET): An insulated-gate field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material.

transistor, substrate pnp: A pnp transistor formed from the base and collector regions of a normal npn bipolar transistor and the substrate.

transistor, unipolar: A transistor in which the electrical conduction is due entirely to the flow of majority carriers.

1.1 Definitions of physical terms applicable to integrated circuits in general (cont'd)

undercut: The reduction of the cross section of a material caused by etching action spreading beneath the edge of the photoresist or other masking films.

unipolar technology: A technology for producing devices in which electrical conduction is due entirely to the flow of majority carriers.

untestable circuit: A circuit that contains logic functions that cannot be tested because of the lack of controllability or observability. (Ref. JESD12-1B.)

via: An electrically conducting path that passes through an insulating material and connects conducting layers in two or more planes.

VLSI: Very-large-scale integration.

wafer: A slice or flat disk, either of semiconductor material or of such a material deposited on a substrate, in which circuits or devices are simultaneously processed and subsequently separated into chips if there is more than one device.

window: A hole formed by etching through an oxide or insulating layer on a semiconductor for the purpose of diffusion into or deposition onto a selected area of the semiconductor.

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits

array density (of a gate array): The number of available gates divided by the entire chip area. (Ref. JESD12-1B.)

NOTE Units are gates per unit area.

array, logic: Synonym for “gate array integrated circuit”.

available gates (in a gate array): The total number of potentially usable, unconnected gate equivalents in a given array area. (Ref. JESD12-1B.)

behavioral description: The algorithms or equations defining a function. (Ref. JESD12-1B.)

cell-based integrated circuit: An integrated circuit fabricated with a unique full set of mask information and comprising one or more macrocells that can be selectively placed and interconnected to perform an electrical function. (Ref. JESD12-1B.)

cell compiler: A tool that automatically generates the physical layout to meet the specified parameters and that may generate a symbol and timing and functional models. (Ref. JESD12-1B.)

channeled gate array: A gate array configuration that contains a predetermined and dedicated area for logic interconnection. (Ref. JESD12-1B.)

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

channelless gate array: A gate array configuration that contains no predetermined and dedicated area for logic interconnection. (Ref. JESD12-1B.)

core-limited integrated circuit: An integrated circuit whose chip size is determined by the gate core area required for functional implementation. (Ref. JESD12-1B.)

design module: A software description of a functional block describing its function and performance. (Ref. JESD12-1B.)

device-level description: A structural description using circuit elements as primitives. (Ref. JESD12-1B.)

distributed delay model: A model constructed from primitive models, each having specified delay. (Ref. JESD12-1B.)

embedded gate array: A gate array masterslice in which some of the array circuit elements are replaced by one or more cell-based functions. (Ref. JESD12-1B.)

field-programmable gate array (FPGA): A gate array integrated circuit that can be electrically programmed. (Ref. JESD12-1B.)

field-programmable logic array (FPLA): Synonym for “programmable logic array”.

field-programmable logic sequencer (FPLS): Synonym for “programmable logic sequencer”.

flattened [nonhierarchical] layout: A geometric description in which all geometrics are contained at the lowest hierarchical level. (Ref. JESD12-1B.)

flattened [nonhierarchical] netlist: A netlist in which all logic elements are connected at the lowest hierarchical level. (Ref. JESD12-1B.)

floorplanning: The process of defining the physical placement of circuit elements. (Ref. JESD12-1B.)

functional library: The functional models of a set of macros. (Ref. JESD12-1B.)

gate array integrated circuit: A digital integrated circuit containing a fixed topology of circuit elements used to form macrocells and macro functions that are or can be interconnected to implement a logic function. (Ref. JESD12-1B.)

gate capacity (of a gate array): Synonym for “usable gates”. (Ref. JESD12-1B.)

gate core area (of a cell-based integrated circuit): The physical area occupied by the logic gates and intercell routing excluding the pad cell area. (Ref. JESD12-1B.)

gate core area (of a gate array): The physical area occupied by the available logic gates and intercell routing excluding the pad cell area. (Ref. JESD12-1B.)

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

gate core density (of a cell-based integrated circuit): The number of gates in the gate core area divided by the gate core area. (Ref. JESD12-1B.)

NOTE Units are gates per unit area.

gate core density (of a gate array): The number of available gates in the gate core area divided by the gate core area. (Ref. JESD12-1B.)

NOTE Units are gates per unit area.

gate-level description: A structural description using logic gates as primitives. (Ref. JESD12-1B.)

gate utilization (in a gate array): The ratio of the number of used gates to available gates.

NOTE Gate utilization is usually expressed as a percentage.

geometric description: A representation of a function in terms of its physical implementation. (Ref. JESD12-1B.)

hard macro: Synonym for “macrocell”.

hardware accelerator: A system using software-configurable hardware to speed up software models that are used to model the network being simulated. (Ref. JESD12-1B.)

NOTE The objective is to achieve faster simulation than can be achieved with software simulators.

hierarchical description: A description containing two or more nested levels of primitives. (Ref. JESD12-1B.)

hierarchical layout: The layout of a design that exists in multiple hierarchical levels. (Ref. JESD12-1B.)

interactive layout: The manual modification or influence used in the pattern layout, cell placement, or interconnect routing in an otherwise automatic layout tool. (Ref. JESD12-1B.)

logic synthesis: The process of transforming behavioral, structural, or register-transfer-level descriptions into structural descriptions based on a given set of implementation criteria. (Ref. JESD12-1B.)

macrocell: A characterized fixed layout and interconnection of primitives that implement an electrical function. (Ref. JESD12-1B.)

NOTE Characterization may be done either by measurement of fabricated devices or by computer simulation or by both. Characterization may include the following aspects: physical dimensions, logic functionality, testability, layout-rule compliance, ac and dc electrical performance, and reliability.

macrocell area: The physical cell area contained within a polygon (often a rectangle) that circumscribes the cell. (See also “unit gate size”.) (Ref. JESD12-1B.)

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

macro function: An interconnection of primitives and/or macrocells that implements an electrical function but has no predetermined physical layout. (Ref. JESD12-1B.)

module generator: A tool that, when given a high-level description of a desired function and relevant parameters, produces a specified implementation (for example, behavioral, structural, or geometric description, etc.) of the function to be used within an integrated circuit design. (Ref. JESD12-1B.)

NOTE Some functions commonly produced by module generators are RAM, ROM, ALU, and datapath.

net (of a circuit): A unique interconnection of specific circuit elements. (Ref. JESD12-1B.)

NOTE The primary inputs and primary outputs are considered to be circuit elements.

netlist: A list of all nets of a circuit. (Ref. JESD12-1B.)

netlist translation: The conversion of a netlist from one format to another. (Ref. JESD12-1B.)

parameterized macrocell: A macrocell produced by a module generator. (See also “module generator”.) (Ref. JESD12-1B.)

parameterized macro function: A macro function produced by a module generator. (See also “module generator”.) (Ref. JESD12-1B.)

partition: The process by which a design is mapped into multiple components or functional blocks within a device. (Ref. JESD12-1B.)

pin-to-pin delay model: A model for which delays are specified from input pin(s) to output pin(s). (Ref. JESD12-1B.)

primary input: An input driven from outside of the circuit boundary. (Ref. JESD12-1B.)

primary output: An output driving outside the circuit boundary. (Ref. JESD12-1B.)

primitive (building block): A basic building block for a specified level of design hierarchy. (Ref. JESD12-1B.)

process-programmable gate array: A gate array integrated circuit that is programmed as part of the integrated circuit manufacturing process. (Ref. JESD12-1B.)

NOTE Process-programmable gate arrays are characterized by the ability to inventory partially fabricated wafers prior to interconnection.

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

programmable logic array (PLA): (1) An integrated circuit consisting of an array of combinational logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions. (Ref. IEC 748-2.)

NOTE The PLA is typically a large set of AND gates driving several OR gates.

(2) A cell that emulates a programmable logic array that has been programmed in a custom integrated circuit.

programmable logic sequencer (PLS): (1) An integrated circuit consisting of an array of combinational and sequential logic elements (circuits) with a fixed interconnection pattern in which connections can be made or broken after manufacture to perform specific logic functions.

(2) A cell that emulates a programmable logic sequencer that has been programmed in a custom integrated circuit.

register-transfer-level (RTL) description: A hybrid between a behavioral description and a structural description at the level of clocked registers. (Ref. JESD12-1B.)

scan insertion: The conversion of bistable elements into scan cells. (Ref. JESD12-1B.)

schematic capture: Use of a computer system to enter a graphical representation of the functional blocks and the interconnections of a circuit. (Ref. JESD12-1B.)

silicon compiler: A design automation system that, when given a high-level description (behavioral, register transfer level, etc.) of desired functionality, will generate sufficient information for manufacture and verification of an integrated circuit design. (Ref. JESD12-1B.)

soft macro: Synonym for “macro function”.

standard cell: A macrocell used in the context of cell-based integrated circuits. (Ref. JESD12-1B.)

structural description: A definition of a function in terms of an interconnection of primitives. (Ref. JESD12-1B.)

switch-level description: A structural description using switches as primitives. (Ref. JESD12-1B.)

symbol library: The graphical symbols for a set of macrocells and/or macro functions. (Ref. JESD12-1B.)

test synthesis: Creation and insertion of test circuitry to improve testability of a design.

timing library: The timing models of a set of macrocells and/or macro functions. (Ref. JESD12-1B.)

timing simulation: The process of exercising the functional and timing models of a particular netlist by applying input stimuli to observe the timing responses. (Ref. JESD12-1B.)

tool: A program that performs a function within a design automation system. (Ref. JESD12-1B.)

1.2 Definitions of physical terms applicable to gate arrays or cell-based integrated circuits (cont'd)

top-down design: The process of designing a circuit hierarchically starting at the highest level followed by detailed design at a lower level. (Ref. JESD12-1B.)

uncommitted logic array: Synonym for “gate array integrated circuit”.

unit gate size (of a gate array): A physical space occupied by a single gate equivalent, including any area allocated to power connections, signal connections, and isolation requirements. (Ref. JESD12-1B.)

unit load: A measure of load (usually capacitance) equal to that presented by a specified input of a specified primitive. (Ref. JESD12-1B.)

used gate (in a gate array): A single gate equivalent that has been interconnected and is employed in the functioning of the circuit. (Ref. JESD12-1B.)

usable gates (in a gate array): The typical number of gate equivalents that can be used in a given gate array size. (Ref. JESD12-1B.)

wire length: The total amount of interconnect of a net (specified in units of either length or capacitance). (Ref. JESD12-1B.)

SECTION 2: PARAMETRIC AND DESCRIPTIVE TERMS

2.1 General guidelines for letter symbols and abbreviations

2.1.1 Definitions of letter symbols and abbreviations

abbreviation: A shortened form of a word or expression.

letter symbol (for a quantity or a unit): One or more letters written successively and without spacing, in a specified style and often provided with additional marks, by convention representing a quantity or a unit. (Ref. ANSI Y10.1 and IEC 27-1.)

NOTE In a few special cases, nonalphanumeric signs are considered as letters in this connection, e.g., the sign ° (degree), which is used as a letter symbol for a unit of angle and in the letter symbol °C for a unit of temperature.

quantity symbol: A letter symbol that is used to represent a physical quantity or a relationship between quantities.

unit symbol: A letter symbol that is used in place of the name of a unit.

2.1.2 Criteria and conventions for letter symbols and abbreviations

2.1.2.1 Primary (quantity) symbols

The letter symbol used to designate a quantity or parameter shall be a single letter. This single letter, referred to as the primary symbol, may be modified by subscripts or superscripts. See “secondary (quantity) symbols”.

Table 2.1-1 illustrates primary symbols and unit symbols. Table 2.1-3 and Table 2.1-4 illustrate principles of application when combined with secondary symbols.

NOTE The terms “primary” and “secondary” are used as synonyms for “kernel” and “additional marks”, respectively, as defined in ANSI Y10.1 and IEC 21-1 and used in the definition of “letter symbol” in 2.1.1; they are not to be confused with the terms “chief” and “reserve”.

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.1 Primary (quantity) symbols (cont'd)

Table 2.1-1 — Primary symbols

Term	Primary (quantity) symbol	SI unit of measurement	Unit symbol[1)]
Amplification (voltage or current)	*A* (uppercase only)	(numeric)[2)]	[2)]
Capacitance	*C* (uppercase only)	farad	F
Current	*I*, *i*	ampere	A
Frequency	*f* (lowercase only)	hertz	Hz
Gain (power)	*G* (uppercase only)	decibel[3)]	dB[3)]
Impedance	*Z*, ***z***	ohm	Ω
Inductance	*L* (uppercase only)	henry	H
Power	*P*, *p*	watt	W
Resistance	*R*, *r*	ohm	Ω
Temperature	*T* (uppercase only)	kelvin or degree Celsius	K or ^{o}C
Time	*t* (lowercase only)	second	s
Voltage	*V*, *v*	volt	V

1) The unit symbols are often used with the SI (metric) system of multiplier prefixes, for example, µA for microampere.

2) Alternatively, voltage and current amplification may be expressed in decibels (unit symbol dB) provided the impedances associated with the ratio are equal.

3) Alternatively, power gain may be expressed as a dimensionless ratio.

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.2 Secondary (quantity) symbols

A subscript or superscript, referred to as a secondary symbol, may be used to modify the primary symbol. The secondary symbol is used to designate special values of state, points, parts, times, etc. An abbreviation may be used as a subscript (secondary symbol).

Symbol subscripts shall be written on one line only. If there is more than one secondary symbol modifying the primary symbol, all such symbols shall be placed on the same (subscripted) line.

Terminal and value abbreviations shall be as shown in Table 2.1-2.

For currents and voltages, the first subscript designates the terminal at which the current is measured, or the terminal where the potential is measured with respect to the reference terminal, which is sometimes designated by the second subscript. Conventional current into the terminal is positive.

NOTE The terms “primary” and “secondary” are used as synonyms for “kernel” and “additional marks”, respectively, as defined in ANSI Y10.1 and IEC 27-1 and used in the definition of “letter symbol” in 2.1.1; they are not to be confused with the terms “chief” and “reserve”.

Table 2.1-2 — Commonly used specific subscript abbreviations

Term	Secondary symbol
Bias	B
Common-mode	C (second subscript)
Differential	D (second subscript)
High logic level	H
Input	I (first subscript)
Low logic level	L
Maximum (peak) value[1)]	M[1)] (final subscript)
Output	O (first subscript)
Offset	O (second subscript)
Single-ended	S (second subscript)
Short-circuit	S (second subscript)
High-impedance state	Z

1) This refers to the peak value of a waveform, not to the maximum-limit value. (See Figure 2.1-1.)

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.3 Primary and secondary symbol combined

A letter symbol containing both primary and secondary letters has a unique meaning. This meaning cannot necessarily be inferred from the individual meanings of the primary and secondary symbols forming the combination.

Table 2.1-3 and Table 2.1-4 show the significance of uppercase and lowercase letters. Figure 2.1-1 illustrates the meaning of the various combinations using, as an example, output voltage with a dc and an ac component.

Table 2.1-3 — Symbol capitalization for current, voltage, and power

<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="2">Primary symbol</th></tr>
<tr><th>Lowercase (i, v, p)</th><th>Uppercase (I, V, P)</th></tr>
<tr><td rowspan="7">Secondary symbols (subscripts)</td><td rowspan="2">Lowercase</td><td rowspan="2">Instantaneous value of alternating component</td><td>With no additional subscript: root-mean-square value of alternating component</td></tr>
<tr><td>With additional subscript m: peak value of alternating component</td></tr>
<tr><td rowspan="5">Uppercase</td><td rowspan="5">Instantaneous total value</td><td>With no additional subscript: direct current value</td></tr>
<tr><td>With additional subscript M: peak total value</td></tr>
<tr><td>With additional subscript (AV): average value</td></tr>
<tr><td>With additional subscript (RMS): total value</td></tr>
<tr><td>With additional subscript (PP): peak-to-peak value</td></tr>
</table>

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.3 Primary and secondary symbol combined (cont'd)

Table 2.1-4 — Symbol capitalization for capacitance and four-pole matrix parameters

		Primary symbol	
		Lowercase (*g, h, r, s, z,* etc.)	**Uppercase (*A, C, G, R, Z,* etc.)**
Secondary symbols (subscripts)	Lowercase	Small-signal values of: resistance and impedance inherent within the device (e.g., r_i, $\mathbf{z}_o$) and s parameters (e.g., s_i, s_o)	Small-signal values of: amplification, capacitance, and gain (e.g., A_{vd}, C_o, G_{pe})
	Uppercase	Large-signal and static values of: conductance, resistance, and impedance inherent within the device (e.g., g_{FS}, r_I, $\mathbf{z}_O$) and s parameters (e.g., s_I, s_O)	Large-signal and static values of: amplification, capacitance, and gain (e.g., A_{VD}, C_O, G_{PE}) and resistance and impedance in external circuits (e.g., R_I, Z_O)

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.3 Primary and secondary symbol combined (cont'd)

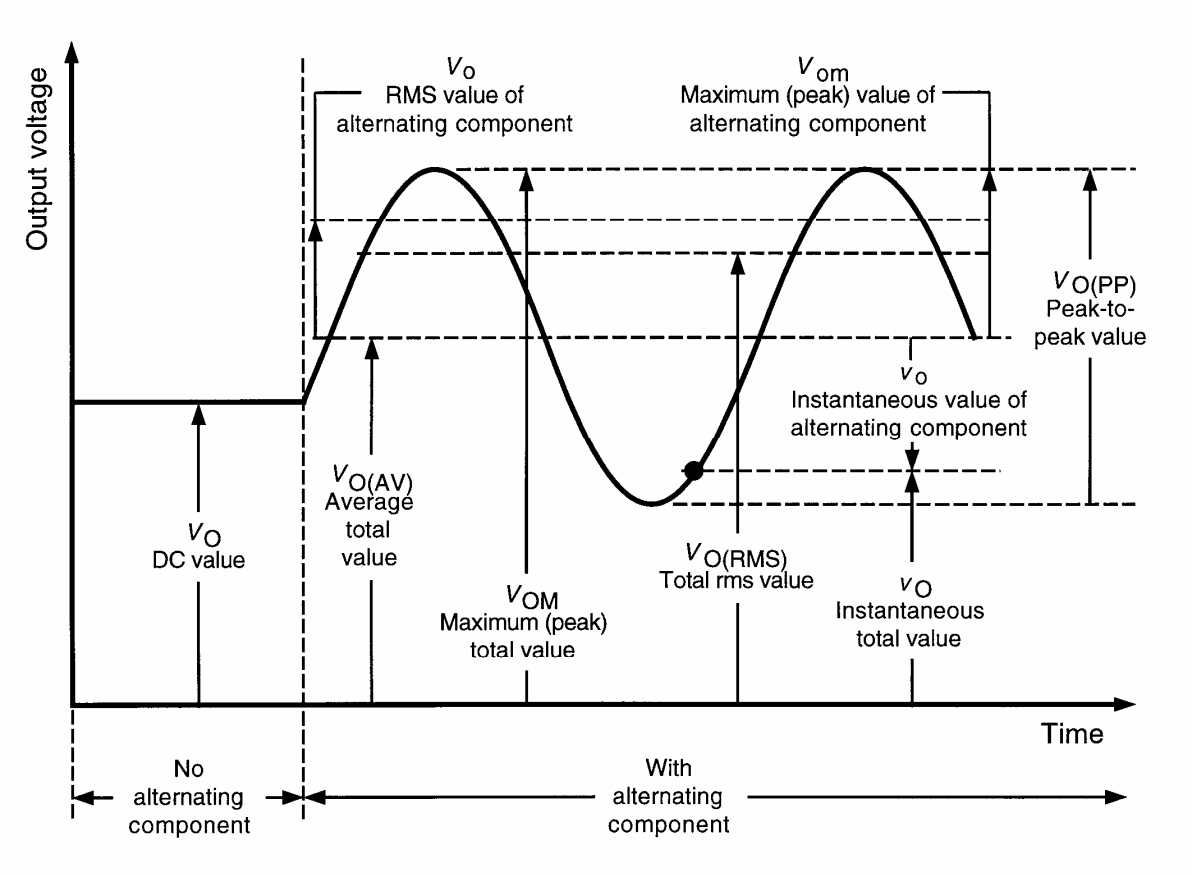

Figure 2.1-1 — Illustration of the proper use of symbols

2.1.2.4 Descriptive information

Descriptive information concerning a letter symbol may be added in parentheses after and on the same line as the secondary symbol. The abbreviations “max” and “min” are excluded from this rule. When these designate limit values, they are not considered to be part of the symbol itself.

2.1.2.5 Symbols for supply voltages and currents

Symbols for supply voltages and currents are normally constructed using the same letter for both the first and second subscript, e.g., V_{CC}, V_{DD}, I_{CC}, and I_{DD}.

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.6 Unit symbols

The letter symbol used in place of a unit name shall be taken from a recognized standard such as ANSI/IEEE Std 260.1, ANSI/IEEE Std 268, NIST Special Publication 330, or IEC 27 and shall be used in accordance with the rules given therein. Some of the most important rules are listed below.

1) Do not use an attachment to a unit symbol (e.g., a subscript or postscript) as a means of giving information about the special nature of the quantity under consideration. Such information should be conveyed instead by the quantity symbol.

2) Unit symbols are to be in lowercase letters (e.g., cd) unless the unit name has been derived from a proper name, in which case the first letter of the symbol is capitalized (e.g., W, Hz). International (SI) prefix symbols representing multipliers of 10^6 or greater are uppercase, those representing 1000 or less are lowercase. Symbols retain their prescribed case regardless of surrounding typography.

3) Always leave a space between numerical values and unit symbols (e.g., 10 V, 5 mA, 50 kΩ, 25 °C) except when used as an adjective modifier to a noun, in which case a hyphen should be inserted between the number and the symbol (e.g., a 12-V battery). However, no space is used between a number and the symbols for degree, minute, and second of plane angle (e.g., 12°45′10″).

4) Do not use compound prefixes formed by juxtaposition of two or more SI prefixes. For example, use 1 pF, not 1 μμF. If outside the range covered by SI prefixes, which extend from yocto (10^{-24}) to yotta (10^{24}), use powers of ten applied to the base unit.

5) Division may be indicated using a slash (e.g., V/Ω) and this procedure may be extended to cases where the numerator and/or denominator are themselves products or quotients; but, in such a combination, a slash should not be followed by a multiplication sign or a division sign on the same line unless parentheses are inserted to avoid ambiguity. For example, write W/(sr·m^2) or W·sr^{-1}·m^{-2} or (W/sr)/m^2, but not W/sr/m^2 or W/sr·m^2.

6) Multiplication may be indicated using either a raised dot or a space between pairs of symbols (e.g., N·m, N m). In systems with limited character sets, a period may be used in place of the raised dot. The space may be omitted provided that special care is taken when the symbol for one of the units is the same as the symbol for a prefix; e.g., mN means millinewton and therefore must not be used for meter newton.

2.1.2 Criteria and conventions for letter symbols and abbreviations (cont'd)

2.1.2.7 Abbreviations

Short words are not usually abbreviated unless their abbreviation has been established by long practice.

An abbreviation is usually written with no spaces between the letters of the abbreviation. The use of hyphens and virgules (slant bars) is avoided where practicable.

Periods are used after abbreviations only when necessary to avoid misinterpretation of an abbreviation or at the end of a sentence.

Uppercase or lowercase letters may be used as appropriate except where the use of a particular case has been established by long practice. When used as secondary symbols, the parts of a multiletter abbreviation shall not be a mixture of uppercase and lowercase letters.

Subscripts and superscripts are not used in abbreviations.

Abbreviations shall be used only when their meanings are unquestionably clear. When in doubt, spell it out.

Abbreviations for word combinations shall be used as such and shall not be separated for use singly.

The same abbreviation shall be used for all tenses and the singular and plural forms of a given word.

2.1.2.8 Typefaces

In textbooks and technical publications, the use of italic type is recommended for quantity symbols, whether uppercase or lowercase. Numerals, abbreviations, and unit symbols shall be printed in roman (upright) type. Characters used as subscripts should be set in the same type style that they would be if they were not subscripts; i.e., use roman type for all subscripts except when quantity symbols are used as subscripts (e.g., G_p, α_{VIO}).

For data sheets, specifications, and technical reports prepared on a typewriter, the use of conventional typewriter typefaces is acceptable for symbols that are ordinarily italicized.

2.2 Terms and definitions applicable to all integrated circuits

2.2.1 General concepts

characteristic: (1) An inherent and measurable property of a device. (Ref. IEC 134.)

NOTE Such a property may be electrical, mechanical, thermal, hydraulic, electromagnetic, or nuclear and may be expressed as a value for stated or recognized conditions.

(2) A set of related values, usually shown in graphical form. (Ref. IEC 134.)

interconnection unit capacitance: The capacitance per unit length attributable to a specified interconnection layer. (Ref. JESD12-1-B.)

latch-up: A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition.

NOTE 1 The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative.

NOTE 2 Latch-up will not damage the device provided that the current through the low-impedance path is sufficiently limited in magnitude or duration.

maximum rating: A rating that establishes either a limiting capability or a limiting condition beyond which damage to the device may occur. (Ref. IEC 747-1.)

NOTE 1 A limiting condition may be either a maximum or a minimum.

NOTE 2 IEC 747-1 refers to such a limiting condition as a “rating (limiting value)”.

rating: The nominal value of any electrical, thermal, mechanical, or environmental quantity assigned to define the operating conditions under which a component, machine, apparatus, electronic device, etc., is expected to give satisfactory service. (Ref. IEC 747-1.)

NOTE “Rating” is a generic term, but also see “maximum rating”.

simultaneously switching outputs: Multiple output buffers that change state within a defined short time interval. (Ref. JESD12-1-B.)

terminal capacitance (deprecated)**:** The term “terminal-to-ground capacitance” is preferred.

trigger pulse (1) **(general):** A positive or negative current or voltage pulse applied to any terminal or node in an attempt to induce a specific effect.

NOTE A clock signal or other periodic input for the normal functioning of a device is sometimes called a trigger pulse.

(2) **(in latch-up testing):** A positive or negative current pulse or voltage pulse applied to any terminal under test in an attempt to induce latch-up. (Ref. JESD78B.)

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.2. Boundary concepts

"A" limit*: The more positive (less negative) limit of a range of some quantity.

"B" limit*: The less positive (more negative) limit of a range of some quantity.

maximum limit: (1) The higher-magnitude limit of a range of some quantity.

(2) For logic levels† and temperatures only, the more positive (less negative) limit.

minimum limit: (1) The lower-magnitude limit of a range of some quantity.

(2) For logic levels† and temperatures only, the less positive (more negative) limit.

2.2.3 Stability characteristics

drift: The maximum absolute change in a parameter over a period of time.

NOTE The change may or may not be normalized to the initial value of the parameter. The specific term should be "(parameter) drift".

regulation: The absolute change in a parameter for a change of a circuit variable from one level to another level.

NOTE The change is usually normalized as a percentage but need not be normalized. The specific term should be "(circuit variable) regulation".

sensitivity: The change in a parameter divided by the change in a circuit variable other than temperature.

NOTE This quotient is the average value over the total change of the circuit variable. The change in the parameter may or may not be normalized to a reference value of the parameter. The specific term should be "(circuit variable) sensitivity".

temperature coefficient: The change in a parameter divided by the change in temperature.

NOTE This quotient is the average value over the total temperature change. The change in the parameter may or may not be normalized to a reference value of the parameter. The specific term should be "temperature coefficient of (parameter)".

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* These terms and definitions are taken from documents of the International Electrotechnical Commission (e.g., IEC 748-2). Their use is recommended for logic levels involving negative quantities and generally when an algebraic limit, rather than a magnitude limit, is intended.

† For logic levels involving negative quantities, the use of "A" and "B" limits is recommended instead of maximum and minimum.

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.4 Voltage, current, and power

dc power dissipation (P_D): The total dc power supplied to a device less any power delivered from the device to a load.

input clamp current (I_{IK}): An input current in a region of relatively low differential resistance that serves to limit the voltage swing.

input clamp voltage (V_{IK}): An input voltage in a region of relatively low differential resistance that serves to limit the voltage swing.

input protective voltage (V_{IP}): An input voltage in a region of relatively low differential resistance that serves to limit the voltage swing for the purpose of input protection.

leakage current (I_{Ikg}): The current that results from nonideal conditions.

NOTE Examples of such conditions include surface contamination or rupture of an insulator and cracks or metal inclusions in semiconductor junctions.

off-state current (I_{off}): The current into a circuit node when the device or a portion of the device affecting that circuit node is in the off state.

NOTE When additional subscripts are used, the off-state current is identified by "off" in parentheses following the additional subscripts, e.g., $I_{O(off)}$ for off-state output current.

output clamp current (I_{OK}): An output current in a region of relatively low differential resistance that serves to limit the voltage swing.

output clamp voltage (V_{OK}): An output voltage in a region of relatively low differential resistance that serves to limit the voltage swing.

2.2.5 Junction temperature, thermal resistance, and virtual junction

junction temperature (T_J): The temperature of a semiconductor junction.

NOTE In data sheets it is common practice to use this term to mean virtual-junction temperature.

thermal resistance, case-to-ambient ($R_{\theta CA}$ or R_{thCA}*): The thermal resistance (steady-state) from the device case to the ambient.

thermal resistance, junction-to-ambient ($R_{\theta JA}$ or R_{thJA}*): The thermal resistance (steady-state) from the virtual junction(s) of a semiconductor device to the ambient.

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* If a probability of misinterpretation exists because other letter symbols are combined with the subscripts of R_{th}, the subscript "th" should be enclosed in parentheses, i.e., $R_{(th)}$.

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.5 Junction temperature, thermal resistance, and virtual junction (cont'd)

thermal resistance, junction-to-case ($R_{\theta JC}$ or R_{thJC}*): The thermal resistance (steady-state) from the virtual junction(s) of a semiconductor device to a stated location on the case.

thermal resistance, steady-state (R_{θ} or R_{th}*): The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium.
(Ref. ANSI/IEEE Std 100.)

virtual junction: The theoretical point or region in a simplified model of the thermal and electrical behavior of a semiconductor device at or in which all the power dissipation within the device is assumed to occur.

virtual-junction temperature; internal equivalent temperature (T_J or T_{VJ}): The temperature of the virtual junction.

2.2.6 Types of outputs

NOTE All the outputs described in this subclause can be categorized as either bipolar or unipolar. Figures 2.2-1 and 2.2-2 show the hierarchy in these two families. A given output can be described using any of the names that apply to it; care should be exercised to select the most descriptive name, considering its construction and application.

active-pulldown output: A bipolar (three-state or totem-pole) output whose source-current capability significantly exceeds its sink-current capability.

active-pullup output: A bipolar (three-state or totem-pole) output whose sink-current capability significantly exceeds its source-current capability.

bipolar output: An output having internal connections through two active devices to two supply voltages so that, according to the relative states of the active devices, the output can source or sink current through the load.

bridge (output): Synonym for “full-bridge (output)”.

emitter follower: An output circuit whose output load is connected in the emitter circuit of a transistor and whose input is applied between the base and the remote end of the emitter load, which may be at ground potential.

NOTE The term “emitter follower”, as applied to linear circuits, usually refers to passive-pulldown or passive-pullup (bipolar) outputs; as applied to emitter-coupled logic (ECL) circuits, to open-emitter (unipolar) outputs.

* If a probability of misinterpretation exists because other letter symbols are combined with the subscripts of R_{th}, the subscript “th” should be enclosed in parentheses, i.e., $R_{(th)}$.

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.6 Types of outputs (cont'd)

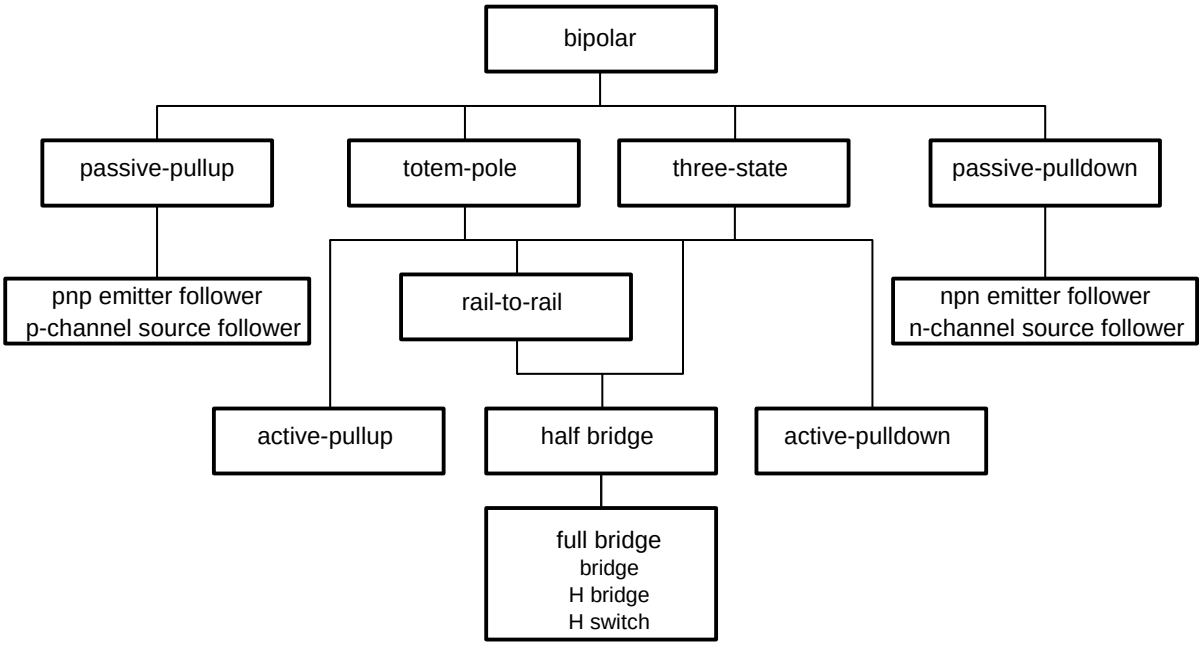


Figure 2.2-1 — Hierarchy of bipolar outputs

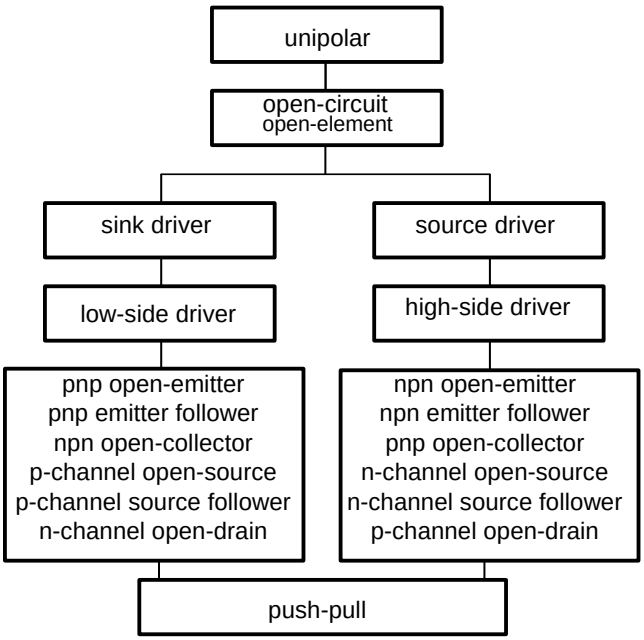


Figure 2.2-2 — Hierarchy of unipolar outputs

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.6 Types of outputs (cont'd)

full-bridge (output): Two half-bridge outputs with the load connected between them.

NOTE The outputs are normally operated in a complementary fashion; i.e., as one output goes high, the other goes low. If one or both outputs are three-state outputs or if the operation is not complementary, the load current can be turned off.

half-bridge (output): A bipolar (three-state or totem-pole) power-driver output.

H bridge: Synonym for “full-bridge (output)”.

high-side driver: A source driver whose primary connection within the integrated circuit is through an active device to a positive supply voltage.

H switch: Synonym for “full-bridge (output)”.

NOTE The term “H switch” is usually applied to forward-off-reverse-switching (using one or two three-state outputs) or forward-reverse-switching applications.

low-side driver: A sink driver whose primary connection within the integrated circuit is through an active device to the circuit common.

open-circuit output (of an integrated circuit): A unipolar output whose only connection within the integrated circuit is through an active device, usually a transistor, to one of the supply voltages.

NOTE 1 For the purpose of this definition, the presence of any parasitic components and freewheeling, flyback, and clamp diode is ignored.

NOTE 2 When the active device is in its on state, the output voltage approaches the voltage of the supply to which it is connected (through the active device); when the device is in its off state, the output impedance to any other terminal of the integrated circuit is high and the output voltage is determined by the external circuit to which the output is connected.

NOTE 3 Outputs of this generic class are usually classified according to the name of the element of the active device to which they are connected within the integrated circuit, e.g., open-collector output, open-drain output, etc.

NOTE 4 For graphic symbols, see “sink driver” and “source driver”.

open-collector output: An open-circuit output whose internal connection is to the collector of a bipolar transistor.

NOTE For graphic symbols, see “sink driver” (for npn) or “source driver” (for pnp).

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.6 Types of outputs (cont'd)

open-drain output: An open-circuit output whose internal connection is to the drain of a field-effect transistor.

NOTE For graphic symbols, see “sink driver” (for n-channel outputs) or “source driver” (for p-channel outputs).

open-element output (of an integrated circuit): Synonym for “open-circuit output (of an integrated circuit)”.

open-emitter output: An open-circuit output whose internal connection is to the emitter of a bipolar transistor.

NOTE For graphic symbols, see “source driver” (for npn) or “sink driver” (for pnp).

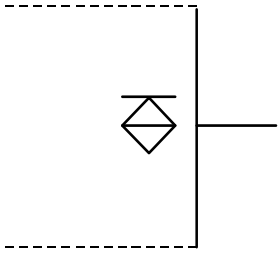
open-source output: An open-circuit output whose internal connection is to the source of a field-effect transistor.

NOTE For graphic symbols, see “source driver” (for p-channel outputs) or “sink driver” (for n-channel outputs).

passive-pulldown output: An output similar to an open-circuit except that, in addition to having an internal connection through an active device to a supply voltage, it also has an internal connection through a passive device, usually a resistor, to a second supply voltage that is more negative (less positive) than the first supply voltage.

NOTE According to the state of the active device, the output voltage can swing between levels approaching the two supply voltages.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



NOTE The bar above the diamond indicates that the output is at the high logic level when the active device is in its on state.

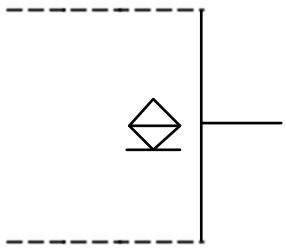
2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.6 Types of outputs (cont'd)

passive-pullup output: An output similar to an open-circuit output except that, in addition to having an internal connection through an active device to a supply voltage, it also has an internal connection through a passive device, usually a resistor, to a second supply voltage that is more positive (less negative) than the first supply voltage.

NOTE According to the state of the active device, the output voltage can swing between levels approaching the two supply voltages.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



NOTE The bar below the diamond indicates that the output is at the low logic level when the active device is in its on state.

push-pull output: (1) Two open-circuit outputs operating in complementary fashion so that as the resistance of one increases, the resistance of the other decreases

(2) Originally a synonym for “totem-pole output”, this usage is now deprecated.

NOTE The term “push-pull output” is usually applied to linear circuits.

rail-to-rail driver: A bipolar (three-state or totem-pole) output that can swing between voltage levels that are essentially equal to the supply voltages.

NOTE This is typically accomplished by driving the active devices from boost voltages or charge pumps.

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

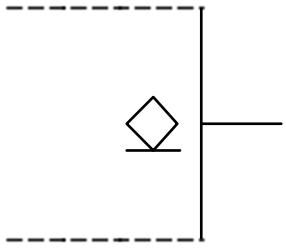
2.2.6 Types of outputs (cont'd)

sink driver, (current-): A unipolar output whose primary connection within the integrated circuit is through an active device to the least positive (most negative) supply voltage (typically the circuit common).

NOTE 1 When the active device is in its on state, the output voltage approaches the voltage of the supply to which it is connected by the active device; when the device is in its off state, the output is pulled up to the most positive (least negative) supply voltage through the external circuit to which the output is connected.

NOTE 2 Examples of sink drivers are npn open-collector, pnp emitter-follower, pnp open-emitter, n-channel open-drain, p-channel open-source, and p-channel source-follower outputs.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



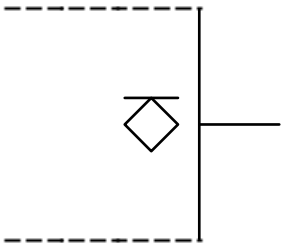
NOTE The bar below the diamond indicates that the output is at the low logic level when the active device is in its on state.

source driver, (current-): A unipolar output whose primary connection within the integrated circuit is through an active device to the most positive (least negative) supply voltage.

NOTE 1 When the active device is in its on state, the output voltage approaches the voltage of the supply to which it is connected by the active device; when the device is in its off state, the output is pulled down to the least positive (most negative) supply voltage through the external circuit to which the output is connected.

NOTE 2 Examples of source drivers are pnp open-collector, npn emitter-follower, npn open-emitter, p-channel open-drain, n-channel open-source, and n-channel source-follower outputs.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



NOTE The bar above the diamond indicates that the output is at the high logic level when the device is in its on state.

2.2 Terms and definitions applicable to all integrated circuits (cont'd)

2.2.6 Types of outputs (cont'd)

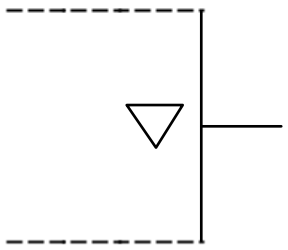
source follower: An output circuit whose output load is connected in the source circuit of a field-effect transistor and whose input is applied between the gate and the remote end of the source load, which may be at ground potential.

NOTE The term “source follower” as applied to linear circuits, usually refers to passive-pulldown or passive-pullup (bipolar) outputs; as applied to logic circuits, to open-source (unipolar) outputs.

three-state output: A bipolar output both of whose active devices can be caused to be in the off state at the same time, thus presenting a high-impedance state at the output similar to the off state of an open-circuit output.

NOTE When the active devices are not in their simultaneous off states, the output acts like a totem-pole output.

Graphic symbol (ref. ANSI/IEEE Std 91 and IEC 617-12):



totem-pole output: A bipolar output whose active devices are so controlled that as the resistance of one increases, the resistance of the other decreases so that, according to the relative states of the two active devices, the output voltage can swing between levels approaching the two supply voltages.

NOTE 1 The term “totem-pole output”, as commonly used, does not include three-state outputs.

NOTE 2 No standard qualifying symbol, as part of a graphic symbol, exists to designate the totem-pole output. In ANSI/IEEE Std 91 and IEC 617-12 these outputs are identified by the absence of a qualifying symbol.

unipolar output: An output that, depending on its design, can either source or sink current, but not both.

2.3 Terms and definitions applicable to digital integrated circuits

2.3.1 General digital concepts

bistable logic function: A sequential logic function that has two and only two stable internal output states. (Ref. ANSI/IEEE Std 91.)

combinational logic function: A logic function in which there exists one and only one resulting combination of states of the outputs for each possible combination of input states.
(Ref. ANSI/IEEE Std 91.)

NOTE The words “combinative” and “combinatorial” have also been used in place of combinational.

function table: A tabulation relating all output digital levels to all necessary or possible input digital levels for sufficient successive time intervals (t_n, t_{n+1}) to completely characterize the static and dynamic functions of the digital integrated circuit.

NOTE 1 Digital levels may be expressed in electrical values directly or by predefined symbolic equivalents.

NOTE 2 Contrast with “truth table”.

high level: A level within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states. (Ref. ANSI/IEEE Std 91.)

logic function: A definition of the relationships that hold among a set of input and output logic variables. (Ref. ANSI/IEEE Std 91.)

logic level: Any level within one of two nonoverlapping ranges of values of a physical quantity used to represent the logic states. (Ref. ANSI/IEEE Std 91.)

NOTE A logic variable may be equated to any physical quantity for which two distinct ranges of values can be defined. In this standard, these distinct ranges of values are referred to as logic levels and are denoted as the high level and the low level.

logic state: One of two possible abstract states that may be taken on by a logic (binary) variable.
(Ref. ANSI/IEEE Std 91.)

low level: A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states. (Ref. ANSI/IEEE Std 91.)

negative logic: The representation of the logic 1-state and the logic 0-state by the low and high levels, respectively. (Ref. ANSI/IEEE Std 91.)

noise margin: The maximum voltage amplitude of extraneous signal that can be algebraically added to the noise-free worst-case “input” level without causing the output voltage to deviate from the allowable logic voltage level.

NOTE The term “input”, as used here, refers to logic input terminals, power supply terminals, or ground reference terminals.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.1 General digital concepts (cont'd)

positive logic: The representation of the logic 1-state and the logic 0-state by the high and the low levels, respectively. (Ref. ANSI/IEEE Std 91.)

sequential logic function: A logic function in which there exists at least one combination of input states for which there is more than one possible resulting combination of states at the outputs.
(Ref. ANSI/IEEE Std 91.)

NOTE The outputs are functions of variables in addition to the present states of the inputs, such as time, previous internal states of the element, etc.

truth table: A tabulation relating all output logic states to all necessary or possible combinations of input logic states for sufficient successive time intervals (t_n, t_{n+1}) to completely characterize the static and dynamic functions of the digital integrated circuit, expressed in logic states or appropriate symbols.

NOTE Contrast with "function table".

0-state: The logic state represented by the binary number 0 and usually standing for an inactive or false logic condition. (Ref. ANSI/IEEE Std 91.)

1-state: The logic state represented by the binary number 1 and usually standing for an active or true logic condition. (Ref. ANSI/IEEE Std 91.)

2.3.2 Voltage

data-retention supply voltage (of an SRAM offering a data-retention mode) ($V_{CC(DR)}$, $V_{DD(DR)}$, etc.): The supply voltage in the data-retention mode.

high-level input voltage, "A" limit (V_{IHA}); high-level input voltage, maximum (V_{IH}max): The most positive (least negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

high-level input voltage, "B" limit (V_{IHB}); high-level input voltage, minimum (V_{IH}min): The least positive (most negative) value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

high-level output voltage (V_{OH}): The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

hysteresis voltage (V_{hys}): The difference between the positive-going and the negative-going input threshold voltages.

input threshold voltage (V_{IT}): The input voltage level that, when crossed, enables an output to change its logic state.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.2 Voltage (cont'd)

low-level input voltage, "A" limit (V_{ILA}); low-level input voltage, maximum (V_{IL}max): The most positive (least negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

low-level input voltage, "B" limit (V_{ILB}); low-level input voltage, minimum (V_{IL}min): The least positive (most negative) value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

low-level output voltage (V_{OL}): The voltage level at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

negative-going input threshold voltage (V_{IT-}): The input threshold voltage when the input voltage is falling.

positive-going input threshold voltage (V_{IT+}): The input threshold voltage when the input voltage is rising.

2.3.3 Current

data-retention supply current (of an SRAM offering a data-retention mode) ($I_{CC(DR)}$, $I_{DD(DR)}$, etc.**):** The supply current in the data-retention mode.

high-impedance-state output current (I_{OZ}): The current into* the output terminal with input conditions applied that, according to the product specification, will establish a high-impedance state at the output.

high-level input current (I_{IH}): The current into* an input terminal when a specified high-level voltage is applied to that input.

high-level output current (I_{OH}): The current into* the output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

low-level input current (I_{IL}): The current into* an input terminal when a specified low-level voltage is applied to that input.

low-level output current (I_{OL}): The current into* the output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

short-circuit output current (I_{OS}): The current into* an output terminal when the output is short-circuited to ground with input conditions applied that, according to the product specification, will establish the output logic furthest from ground potential.

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* Current out of a terminal is considered to be a negative quantity.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.3 Current (cont'd)

supply current, high-level output (I_{CCH}, I_{DDL}, I_{EEL}, etc.**):** The current into* a supply terminal of an integrated circuit when the output is (all outputs are) at a high-level voltage.

supply current, low-level output (I_{CCH}, I_{DDL}, I_{EEL}, etc.**):** The current into* a supply terminal of an integrated circuit when the output is (all outputs are) at a low-level voltage.

2.3.4 Resistance

on-state resistance (r_{on}): The resistance between specified terminals with input conditions applied that, according to the product specification, will establish minimum resistance (the on-state) between those terminals.

2.3.5 Time intervals and clock frequency

clock frequency, maximum (f_{max}): The highest frequency at which a clock input of an integrated circuit can be driven while maintaining proper operation.

delay time (t_d): The time interval between a specified reference point on one waveform and a specified reference point on another waveform.

NOTE This classification is provided essentially as a catch-all for those time intervals not otherwise easily classifiable.

disable time (of a three-state, open-collector, open-emitter, open-drain, or **open-source output) (t_{dis}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

disable time from the high level (of a three-state or **H-type open-circuit** output) (t_{PHZ}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined high level to a high-impedance (off) state.

NOTE Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "high-to-low-level propagation time" and the symbol t_{PHL} are frequently used with these outputs for this parameter.

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* Current out of a terminal is considered to be a negative quantity.

** Open-collector, open-emitter, open-drain, and open-source outputs are collectively referred to as open-circuit outputs. For the purposes of these definitions, the subclassification H-type is used for pnp open-collector, npn open-emitter, p-channel open-drain, and n-channel open-source outputs because, without the aid of external components, the only on-state level they can produce is the high level. The subclassification L-type is used for npn open-collector, pnp open-emitter, n-channel open-drain, and p-channel open-source outputs for analogous reasons.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.5 Time intervals and clock frequency (cont'd)

disable time from the low level (of a three-state or **L-type open-circuit** output) (t_{PLZ}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from the defined low level to a high-impedance (off) state.

NOTE Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "low-to-high-level propagation time" and the symbol t_{PLH} are frequently used with these outputs for this parameter.

disable transition time from the high level (of a three-state or **H-type open-circuit** output) (t_{THZ}):** The transition time between specified reference points on the output voltage waveform with the output changing from the defined high level to a high-impedance (off) state.

NOTE Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "high-to-low-level transition time" and the symbol t_{THL} are frequently used with these outputs for this parameter.

disable transition time from the low level (of a three-state or **L-type open-circuit** output) (t_{TLZ}):** The transition time between specified reference points on the output voltage waveform with the output changing from the defined low level to a high-impedance (off) state.

NOTE Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "low-to-high-level transition time" and the symbol t_{TLH} are frequently used with these outputs for this parameter.

enable time (of a three-state, open-collector, open-emitter, open-drain, or **open-source output) (t_{en}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to either of the defined active levels (high or low).

enable time to the high level (of a three-state or **H-type open-circuit** output) (t_{PZH}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined high level.

NOTE Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term low-to-high-level propagation time and the symbol t_{PLH} are frequently used with these outputs for this parameter.

** Open-collector, open-emitter, open-drain, and open-source outputs are collectively referred to as open-circuit outputs. For the purposes of these definitions, the subclassification H-type is used for pnp open-collector, npn open-emitter, p-channel open-drain, and n-channel open-source outputs because, without the aid of external components, the only on-state level they can produce is the high level. The subclassification L-type is used for npn open-collector, pnp open-emitter, n-channel open-drain, and p-channel open-source outputs for analogous reasons.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.5 Time Intervals and clock frequency (cont'd)

enable time to the low level (of a three-state or **L-type open-circuit** output) (t_{PZL}):** The propagation time between specified reference points on the input and output voltage waveforms with the output changing from a high-impedance (off) state to the defined low level.

NOTE Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "high-to-low-level propagation time" and the symbol t_{PHL} are frequently used with these outputs for this parameter.

enable transition time to the high level (of a three-state or **H-type open-circuit** output) (t_{TZH}):** The transition time between specified reference points on the output voltage waveform with the output changing from a high-impedance (off) state to the defined high level.

NOTE Because H-type open-circuit outputs are used with pull-down components that cause the outputs to go low when the outputs are turned off, the term "low-to-high-level transition time" and the symbol t_{TLH} are frequently used with these outputs for this parameter.

enable transition time to the low level (of a three-state or **L-type open-circuit** output) (t_{TZL}):** The transition time between specified reference points on the output voltage waveform with the output changing from a high-impedance (off) state to the defined low level.

NOTE Because L-type open-circuit outputs are used with pull-up components that cause the outputs to go high when the outputs are turned off, the term "high-to-low-level transition time" and the symbol t_{THL} are frequently used with these outputs for this parameter.

fall time (t_f): Synonym for "transition time, high-to-low level".

hold time (t_h): The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTE 1 The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

NOTE 2 The hold time may have a negative value, in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

** Open-collector, open-emitter, open-drain, and open-source outputs are collectively referred to as open-circuit outputs. For the purposes of these definitions, the subclassification H-type is used for pnp open-collector, npn open-emitter, p-channel open-drain, and n-channel open-source outputs because, without the aid of external components, the only on-state level they can produce is the high level. The subclassification L-type is used for npn open-collector, pnp open-emitter, n-channel open-drain, and p-channel open-source outputs for analogous reasons.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.5 Time intervals and clock frequency (cont'd)

propagation (delay) time (t_{pd}): The time interval between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

propagation (delay) time, high-to-low-level output (t_{PHL}): The time interval between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

NOTE In IEC 748-2, the reference points on both the input and output waveforms have the same value, which is midway between the maximum low-level input voltage (V_{IL}max) and the minimum high-level input voltage (V_{IH}min).

propagation (delay) time, low-to-high-level output (t_{PLH}): The time interval between the specified reference points on the input and output voltage waveforms with the specified output changing from the defined low level to the defined high level.

NOTE In IEC 748-2, the reference points on both the input and output waveforms have the same value, which is midway between the maximum low-level input voltage (V_{IL}max) and the minimum high-level input voltage (V_{IH}min).

pulse duration [width] (t_w): The time interval between the specified reference points on the two transitions of the pulse waveform.

rise time (t_r): Synonym for “transition time, low-to-high level”.

setup time (t_{su}): The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTE 1 The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

NOTE 2 The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is to be expected.

skew (time) (general) **(t_{sk}):** The magnitude of the time difference between two events that ideally would occur simultaneously.

skew (time), bank ($t_{sk(b)}$): The output skew time between outputs with a single driving input terminal.

skew (time), input ($t_{sk(i)}$): The magnitude of the difference in propagation delay times between two inputs and a single output of an integrated circuit at identical operating conditions. (See Figure 2.3-1.)

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.5 Time intervals and clock frequency (cont'd)

skew (time), inverting ($t_{sk(inv)}$): The skew time between two outputs of a single integrated circuit with all driving inputs switching simultaneously and the outputs switching in opposite directions while driving identical loads.

skew (time), limit ($t_{sk(l)}$): The difference between (1) the greater of the maximum specified values of propagation delay times t_{PHL} and t_{PLH}, and (2) the lesser of the minimum specified values of propagation delay times t_{PHL} and t_{PLH}.

skew (time), output ($t_{sk(o)}$): The skew time between specified outputs of a single integrated circuit with all driving inputs switching simultaneously and the outputs driving identical loads.

skew (time), output, high-to-low ($t_{sk(HL)}$): The skew time between specified outputs of a single logic device switching from the high level to the low level while driving identical loads. (See Figure 2.3-1.)

NOTE Each input-to-output propagation delay time is measured individually, and the difference is the skew time.

skew (time), output, low-to-high ($t_{sk(LH)}$): The skew time between specified outputs of a single logic device switching from the low level to the high level while driving identical loads. (See Figure 2.3-1.)

NOTE Each input-to-output propagation delay time is measured individually, and the difference is the skew time.

skew (time), part-to-part ($t_{sk(pp)}$): The magnitude of the difference in propagation delay times between any specified terminals of two integrated circuits at identical operating conditions.

skew (time), process ($t_{sk(pr)}$): The part-to-part skew time between corresponding terminals of two samples of an integrated circuit from a single manufacturer.

skew (time), pulse ($t_{sk(p)}$): The magnitude of the difference between the propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch. (See Figure 2.3-1.)

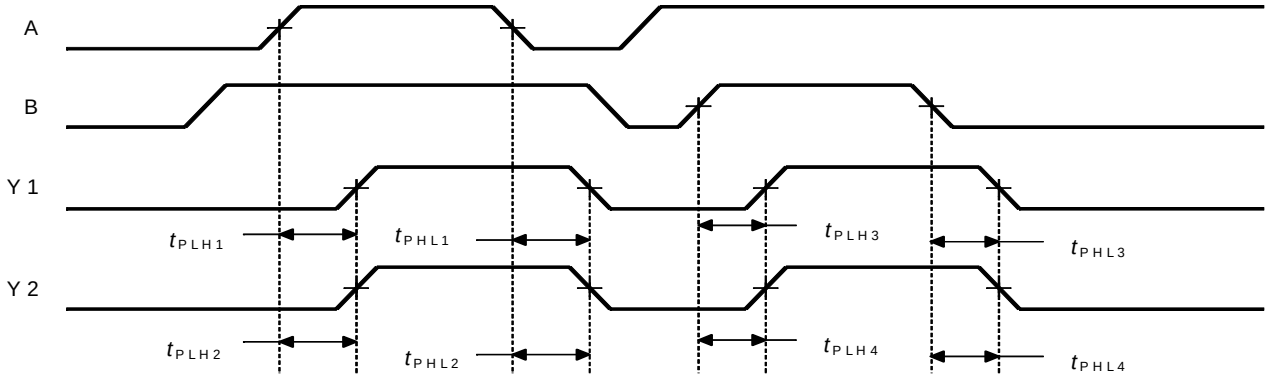
transition time (t_t): The time interval between two specified levels, one near the beginning and one near the end of the same pulse edge.

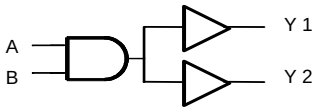
transition time, high-to-low-level (t_{THL}): The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

transition time, low-to-high-level (t_{TLH}): The time interval between the specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

2.3 Terms and definitions applicable to digital integrated circuits (cont'd)

2.3.5 Time intervals and clock frequency (cont'd)





The values of $t_{sk(LH)}$ are calculated from the following expressions:

$| t_{PLH1} - t_{PLH2} |$ and
$| t_{PLH3} - t_{PLH4} |$

The values of $t_{sk(HL)}$ are calculated from the following expressions:

$| t_{PHL1} - t_{PHL2} |$ and
$| t_{PHL3} - t_{PHL4} |$.

The values of $t_{sk(i)}$ are calculated from the following expressions:

$| t_{PLH1} - t_{PLH3} |$,
$| t_{PHL1} - t_{PHL3} |$,
$| t_{PLH2} - t_{PLH4} |$, and
$| t_{PHL2} - t_{PHL4} |$.

The values of $t_{sk(p)}$ are calculated from the following expressions:

$| t_{PLH1} - t_{PHL1} |$,
$| t_{PLH2} - t_{PHL2} |$,
$| t_{PLH3} - t_{PHL3} |$, and
$| t_{PLH4} - t_{PHL4} |$.

Figure 2.3-1 — Skew times

2.4 Terms and definitions applicable to linear (analog) integrated circuits

2.4.1 General linear concepts

balanced amplifier: An amplifier in which the quiescent dc output voltage (or, if the output is a differential output, the difference between the two quiescent dc output voltages) has been reduced to zero or other specified level.

differential inputs: A pair of ungrounded input terminals between which a signal is applied.

differential outputs: A pair of ungrounded output terminals between which the output signal appears.

quiescent current: The dc current through a terminal when no signal is applied.

quiescent voltage: The dc voltage at a terminal when no signal is applied.

2.4.2 Amplification and gain

automatic gain control range (AGC range): The maximum change in gain expressed in dB that may be achieved by application of a specified range of the dc voltages to the AGC input.

power gain, (insertion) (G_P and G_p)*: The ratio (usually expressed in dB) of (1) the signal power delivered to the load after insertion of a transducer between the source and the load to (2) the signal power that was delivered to the load when the load was connected directly to the source.

power gain, transducer (G_T and G_t)*: The ratio (usually expressed in dB) of the signal power delivered to the load to the signal power available from the source.

voltage amplification, common-mode (A_{VC} and A_{vc})*: The ratio of the change in voltage at the output terminal with respect to ground (or change in voltage between the output terminals) to the change in common-mode input voltage with the differential input voltage held constant.

voltage amplification, differential (A_{VD} and A_{vd})*: The ratio of the change in voltage at the output terminal with respect to ground (or change in voltage between the output terminals) to the change in differential input voltage with the common-mode input voltage held constant.

voltage amplification, single-ended (A_{VS} and A_{vs})*: The ratio of the change in single-ended output voltage of a differential amplifier to the change in single-ended input voltage.

voltage gain: Commonly used as a synonym for “voltage amplification”.

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* As prescribed in Table 2.1-4, uppercase subscripts indicate large-signal quantities; lowercase subscripts indicate small-signal quantities.

2.4 Terms and definitions applicable to linear (analog) integrated circuits (cont'd)

2.4.3 Frequency, time, and transient response

bandwidth (*B* or BW): The range of frequencies within which the gain of the amplifier is not more than 3 dB below the value of the midband gain.

NOTE Midband gain is the gain at a specified frequency or the average gain over a specified frequency range.

bandwidth, maximum output swing (B_{OM}): The range of frequencies within which the maximum output voltage swing is above the specified value at a specified load impedance.

bandwidth, unity gain: The range of frequencies within which the open-loop amplification is greater than unity.

cutoff frequency: The frequency at which the voltage amplification is 3 dB below the voltage amplification at a specified frequency.

delay time (t_d, t_{dr}, and t_{df}): The time interval between a step-function change of the input signal level and the instant at which the magnitude of the output signal passes through a specified value (normally 10% for t_{dr} or 90% for t_{df}) close to its initial value. (See Figure 2.4-1.) (Ref. IEC 748-3.)

fall time (t_f): For a step-function change of the input signal level, the time interval between the end of the delay time (normally 90%) and that instant at which the magnitude of the output signal first passes through a specified value (normally 10%) close to its final value. (See Figure 2.4-1.) (Ref. IEC 747-3.)

overload recovery time (t_{or}): The time interval required for an amplifier to recover its ability to perform amplification within stated specification limits after the output voltage amplitude has been distorted by the application of a specified input voltage in excess of rated amplitude or rated rate of change.

overshoot factor: The ratio of (1) the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to (2) the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal. (Ref. IEC 748-3.)

phase margin (ϕ_m): The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop voltage amplification is unity.

ripple time (t_{rip}, $t_{rip(r)}$, and $t_{rip(f)}$): For a step-function change of the input signal level, the time interval between the end of the rise time or fall time and that instant at which the magnitude of the output signal reaches for the last time a specified level range ($\pm\varepsilon$) containing the final output signal level. (See Figure 2.4-1.) (Ref. IEC 747-3.)

rise time (t_r): For a step-function change of the input signal level, the time interval between the end of the delay time (normally 10%) and that instant at which the magnitude of the output signal first passes through a specified value (normally 90%) close to its final value. (See Figure 2.4-1.) (Ref. IEC 747-3.)

2.4 Terms and definitions applicable to linear (analog) integrated circuits (cont'd)

2.4.3 Frequency, time, and transient response (cont'd)

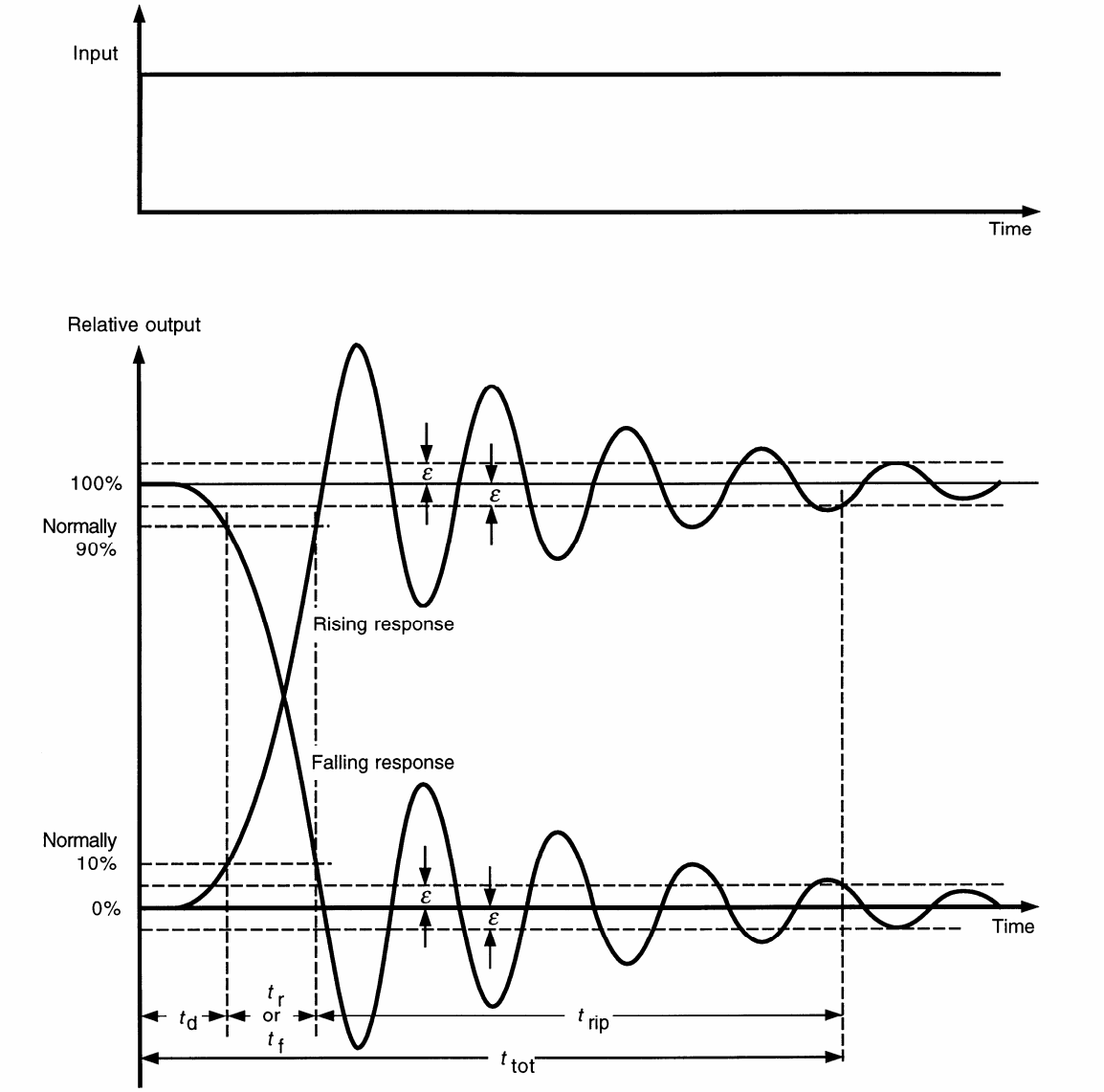

Figure 2.4-1 — Example of response times of linear amplifiers

settling time: Synonym for "total response time".

slew rate (SR): The time rate of change of the closed-loop amplifier output voltage for a step-signal input.

NOTE Slew rate is normally measured between specified output levels using the largest input voltage step for which amplifier performance remains linear with feedback adjusted for unity amplification.

total response time (t_{tot}, $t_{tot(r)}$, and $t_{tot(f)}$): The sum of delay time, rise or fall time, and ripple time. (See Figure 2.4-1.) (Ref. IEC 747-3.)

2.4 Terms and definitions applicable to linear (analog) integrated circuits (cont'd)

2.4.4 Input voltage

common-mode input voltage (V_{IC}): The average of the voltages at two input terminals of a circuit.

common-mode input voltage range (V_{ICR}): The range of common-mode input voltage that, if exceeded, will cause the total harmonic distortion of the output signal resulting from the common-mode input to exceed a specified maximum value.

differential input voltage (V_{ID}): The voltage applied between two input terminals of a circuit.

input offset voltage (V_{IO}): The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other specified level.

single-ended input voltage (V_{IS}): The signal voltage that is applied to one input of a differential amplifier with the other input terminal at signal ground.

single-ended input voltage range (V_{ISR}): The range of single-ended input voltage that, if exceeded at any input terminal, will cause the total harmonic distortion of the output signal resulting from the single-ended input to exceed a specified maximum value.

2.4.5 Output voltage

ac unbalanced voltage: The difference between the peak values of the ac voltages at the two outputs when the circuit is operating in the maximum-output-voltage-swing condition.

common-mode output voltage (V_{OC}): (1) The average of the voltages at two output terminals of a circuit.
(2) The ac voltage between two output terminals (or the output terminals and ground for circuits with one output) when ac signals of identical phase and amplitude are applied to the input terminals.

differential output voltage (V_{OD}): The voltage between two output terminals of a circuit.

maximum output voltage swing (V_{OM}): The peak positive or negative output voltage swing, referred to zero, that can be obtained without waveform clipping.

maximum peak-to-peak output voltage swing ($V_{O(PP)}$): The maximum peak-to-peak output voltage that can be obtained without waveform clipping when the quiescent dc output voltage is set at a specified reference level.

output offset voltage (V_{OO}): The dc voltage between two output terminals (or the output terminal and ground for circuits with one output) when the input terminal(s) are grounded.

quiescent output voltages (V_O): The dc voltage at an output terminal with reference to a common terminal, normally ground, when no signal is applied to the input.

2.4 Terms and definitions applicable to linear (analog) integrated circuits (cont'd)

2.4.5 Output voltage (cont'd)

single-ended output voltage (V_{OS}): The signal voltage between one output terminal and ground of a circuit having differential outputs.

2.4.6 Current

input bias current (I_{IB}): The current into* the input or the average of the currents into* the inputs when the device is in the quiescent or balanced state.

input offset current (I_{IO}): The difference between the currents into* the input terminals of a differential-input device in the balanced state.

maximum output current swing (I_{OM}): The peak positive or negative output current swing, referred to zero, that can be obtained without waveform clipping.

short-circuit output current (I_{OS}): The output current with the output shorted to ground or other specified point.

2.4.7 Resistance and impedance

input impedance, common-mode (z_{ic}): The parallel equivalent of the small-signal impedances between each input terminal of a differential amplifier and ground.

input impedance, differential (z_{id}): The small-signal impedance between two ungrounded input terminals of a differential amplifier.

input impedance, single-ended (z_{is}): The small-signal impedance between one input terminal of a differential amplifier and ground with the other input terminal ac-grounded.

input resistance (r_i): The small-signal resistance between an input terminal and ground or between differential input terminals.

output impedance, differential (z_{od}): The small-signal impedance between two ungrounded output terminals of a differential amplifier.

output impedance, single-ended (z_{os}): The small-signal impedance between one output terminal of a differential amplifier and ground with the other output terminal ac-grounded.

output resistance (r_o): The small-signal resistance between an output terminal and ground or between differential output terminals.

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* Current out of a terminal is considered to be a negative quantity.

2.4 Terms and definitions applicable to linear (analog) integrated circuits (cont'd)

2.4.8 Rejection ratio and sensitivity

common-mode rejection ratio (k_{CMR} or CMRR): The ratio of the differential voltage amplification to the common-mode voltage amplification.

supply voltage rejection ratio (k_{SVR}): The absolute value of the ratio of the change in one supply voltage (with all remaining supply voltages held constant) to the resulting change in input offset voltage.

NOTE 1 See the reciprocal definition under “supply voltage sensitivity”.

NOTE 2 This is sometimes referred to as “power supply rejection ratio”.

NOTE 3 The abbreviations SVRR and PSRR are often used in place of symbol k_{SVR}; however, symbol k_{SVR} is preferred.

supply voltage sensitivity (k_{SVS}): The absolute value of the ratio of the change in input offset voltage to the corresponding change in value of one supply voltage with all remaining supply voltages held constant.

NOTE See the reciprocal definition under “supply voltage rejection ratio”.

2.4.9 Temperature coefficient

temperature coefficient of input bias current (α_{IIB}): The change in input bias current divided by the change in temperature.

NOTE This quotient is the average value for the total temperature change. The change in input bias current is usually not normalized to the initial value of input bias current.

temperature coefficient of input offset current (α_{IIO}): The change in input offset current divided by the change in temperature.

NOTE This quotient is the average value of the total temperature change. The change in input offset current is usually not normalized to the initial value of input offset current.

temperature coefficient of input offset voltage (α_{VIO}): The change in input offset voltage divided by the change in temperature.

NOTE This quotient is the average value for the total temperature change. The change in input offset voltage is usually not normalized to the initial value of input offset voltage.

2.4 Terms and definitions applicable to linear (analog) integrated circuits (cont'd)

2.4.10 Noise and distortion

average noise figure; average noise factor ($\overline{F}$ or $\overline{\mathrm{NF}}$): The ratio of (1) the total output noise power within an output frequency band when the noise temperature of all input terminations is at the reference noise temperature, T_0, at all frequencies that contribute to the output noise to (2) that part of (1) caused by the noise of the signal-input termination within the signal-input frequency band. (Ref. IEC 747-1.)

NOTE 1 The abbreviation $\overline{\mathrm{NF}}$ is often used in place of symbol $\overline{F}$; however, symbol $\overline{F}$ is preferred.

NOTE 2 This ratio may be expressed logarithmically in decibels (dB).

noise temperature (T_n): The uniform physical absolute temperature at which a network (and all its sources, if a multiport) would have to be maintained, if it (and its sources) were passive, in order to make available (or deliver) the same random noise power per unit bandwidth (spectral density) at a given frequency that is actually available (or delivered) from the network. (Ref. IEC 747-1.)

reference noise temperature (T_0): A specified absolute temperature to be assumed as a noise temperature at the input ports of a network when calculating certain noise parameters and for normalizing purposes. (Ref. IEC 747-1.)

NOTE A reference noise temperature of 290 K is considered to be standard in the USA.

spot noise figure; spot noise factor (*F* or NF): The ratio of (1) the total output noise power per unit bandwidth (spectral density) at a single output frequency when the noise temperature of all input terminations is at the reference noise temperature, T_0, at all frequencies that contribute to the output noise to (2) that part of (1) caused by the noise of the signal-input termination at the signal-input frequency. (Ref. IEC 747-1.)

NOTE 1 The abbreviation NF is often used in place of symbol *F*; however, symbol *F* is preferred.

NOTE 2 This ratio may be expressed logarithmically in decibels (dB).

tangential sensitivity (S_T): The input signal power to a circuit that produces a 6-dB signal-to-noise ratio at the output.

total harmonic distortion (THD): The ratio, expressed as a percentage, of the rms voltage of all harmonics present in the output to the total rms voltage of the output, for a pure sine-wave input.

2.5 Terms and definitions applicable to interface integrated circuits

2.5.1 General interface concepts and types

analog-to-digital [A/D] converter (ADC): See 2.5.2.1.

analog gate: A gate whose output signal is a linear function of one or more input signals.

buffer: An isolating circuit used to minimize the effects of a driven circuit on the driving circuit. (Adapted from ANSI/IEEE Std 100 and ANSI X3-172.)

bus driver: A line driver used for fan-out to multiple receivers via a transmission line.

bus receiver: A line receiver intended to be driven from a bus.

clock driver: A driver intended for use with clock signals.

comparator, differential voltage: A device that compares an input voltage with a reference voltage and indicates which is greater by means of a digital output.

decoder: A matrix of logic elements that selects one or more output channels according to the combination of input signals present. (Ref. ANSI/IEEE Std 100.)

differential line receiver: A line receiver that has a differential input.

differential video amplifier: A video amplifier with differential input and differential output terminals.

digital-to-analog [D/A] converter (DAC): See 2.5.2.1.

driver: An amplifier or gate with increased ability to drive a load.

encoder: A network or system in which only one input is excited at a time and each input produces a unique combination of output signals. (Ref. ANSI/IEEE Std 100.)

interface integrated circuit: See 1.2, “integrated circuit, interface”.

line driver: A circuit designed for driving a data transmission line.

line receiver: A circuit designed for receiving data from a transmission line.

logic-level converter; logic-level translator: A circuit used to convert logic voltage levels of one family to corresponding logic levels of another family, such as from ECL to TTL.

party-line driver: Synonym for “bus driver”.

peripheral driver: A circuit designed to interface a digital device with an external nondigital device such as a lamp, light-emitting diode, or data bus.

2.5 Terms and definitions applicable to interface integrated circuits (cont'd)

2.5.1 General interface concepts and types (cont'd)

sense amplifier, memory: A circuit used to sense the output level of a storage element of a memory and to convert it to a form compatible with the logic output elements.

sink LED decoder driver: A circuit that decodes input currents and sinks current from individual light-emitting diodes in a common-anode configuration.

source LED decoder driver: A circuit that decodes input signals and provides current to drive individual light-emitting diodes in a common-cathode configuration.

time-division multiplexing: The process in which each modulation wave modulates a separate pulse subcarrier, the pulse subcarriers being spaced so that no two pulses occupy the same time interval. (Ref. ANSI/IEEE Std 100.)

transceiver: A driver and receiver pair, usually with the driver output connected to the input of the receiver of the same pair.

universal asynchronous receiver transmitter (UART): A circuit used in asynchronous data communications applications to provide all the necessary logic to recover data in a serial-in, parallel-out fashion and to transmit data in a parallel-in, serial-out fashion.

NOTE The UART is usually full-duplex; i.e., it can transmit and receive simultaneously with the option to handle various data word lengths.

video amplifier: A circuit designed to provide useful gain at frequencies for dc up to several megahertz.

2.5.2 Analog-to-digital and digital-to-analog converters

The content of 2.5.2 is based on IEC 748-4.

2.5.2.1 General terms

analog-to-digital [A/D] converter (ADC): A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of which exclusively represents a fractional part of the total analog input range. (See Figure 2.5-1.)

NOTE This quantization procedure introduces inherent errors of ± ½ LSB (least significant bit) in the representation because, within this fractional range, only one analog value can be represented free of error by a single digital output code.

analog-to-digital processor: An integrated circuit providing the analog part of an analog-to-digital converter.

NOTE Provision of external timing, counting, and arithmetic operations is necessary for implementing a full analog-to-digital converter.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

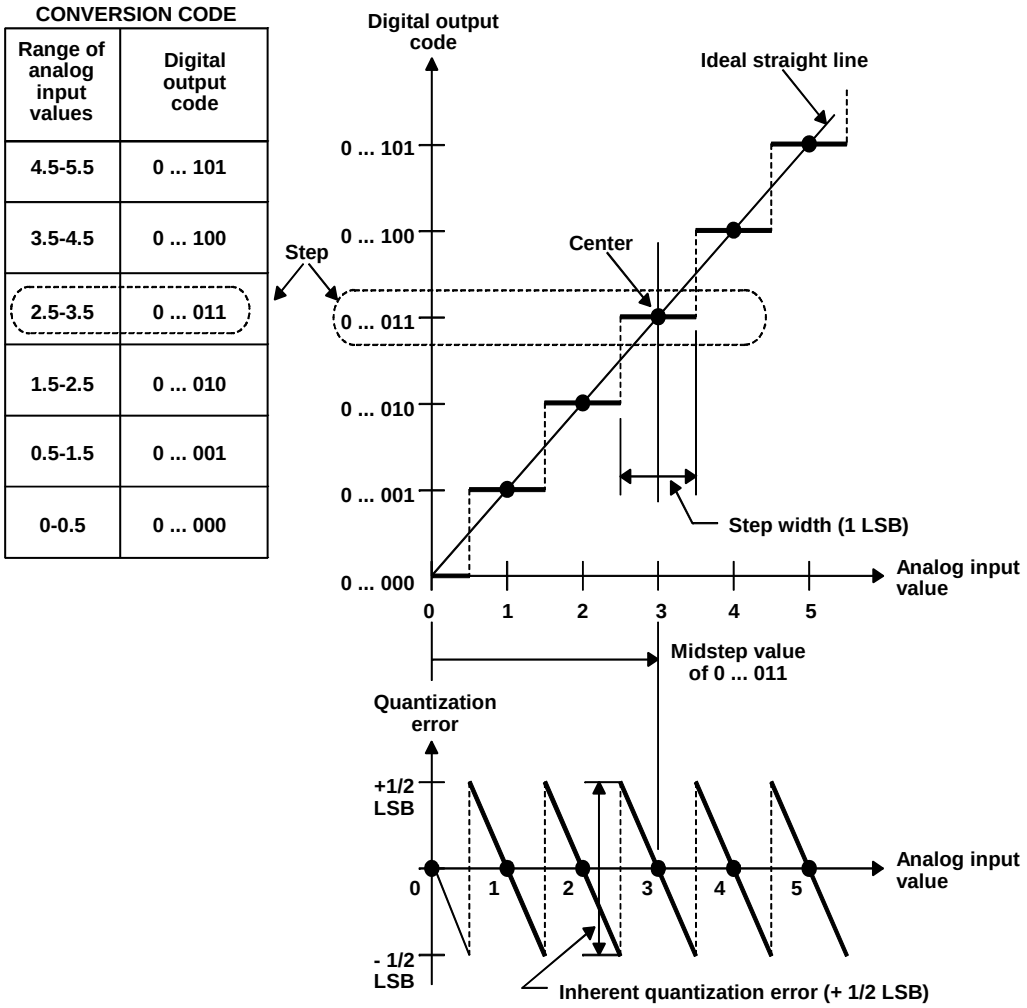


Figure 2.5-1 — Elements of transfer diagram for an ideal linear ADC

companding DAC: A DAC whose transfer function complies with a compression or expansion law.

NOTE 1 The corresponding ADC normally consists of such a companding DAC and additional external circuitry.

NOTE 2 The compression or expansion law is usually a logarithmic function, e.g., A-law or :-law.

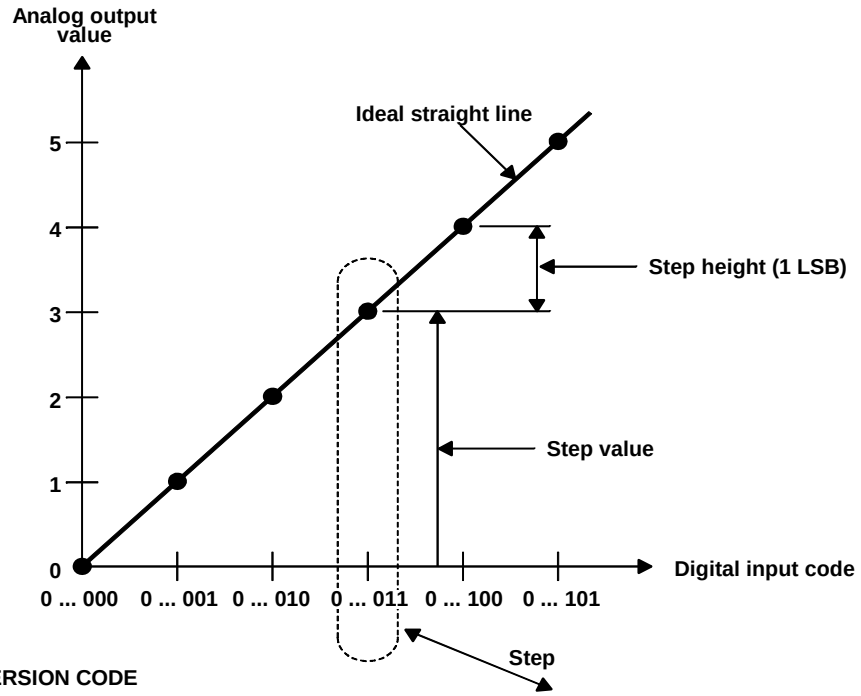
conversion code (1) **(of an ADC):** The set of correlations between each of the fractional parts of the total analog input range and the corresponding digital output codes (See Figure 2.5-1.)

NOTE Examples of ADC output code formats are straight binary, 2s complement, and binary-coded decimal.

(2) **(of a DAC):** The set of correlations between each of the digital input codes and the analog output values. (See Figure 2.5-2.)

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)



CONVERSION CODE

Digital input code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog output value	0	1	2	3	4	5

Figure 2.5-2 — Elements of transfer diagram for an ideal linear DAC

digital-to-analog [D/A] converter (DAC): A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values. (See Figure 2.5-2.)

NOTE Examples of input code formats are straight binary, 2s complement, and binary-coded decimal.

full scale (of a unipolar ADC [DAC]): A term used to refer a characteristic to that step within the transfer diagram whose nominal midstep [step] value has the highest absolute value.
(See Figure 2.5-3a for a linear unipolar ADC.)

NOTE 1 The subscript for the letter symbol of a characteristic at full scale is “FS”.

NOTE 2 In place of a letter symbol, the abbreviation “FS” is commonly used.

full scale, negative (of a bipolar ADC [DAC]): A term used to refer a characteristic to the negative end of the transfer diagram, that is, to the step whose nominal midstep [step] value has the most negative value. (See Figure 2.5-3b and Figure 2.5-3c.)

NOTE 1 The subscript for the letter symbol of a characteristic at negative full scale is “FS–” (e.g., $V_{FS–}$, $I_{FS–}$).

NOTE 2 In place of a letter symbol, the abbreviation “FS–” is commonly used.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

full scale, positive (of a bipolar ADC [DAC]): A term used to refer a characteristic to the positive end of the transfer diagram, that is, to the step whose nominal midstep [step] value has the most positive value. (See Figure 2.5-3b and Figure 2.5-3c.)

NOTE 1 The subscript for the letter symbol of a characteristic at positive full scale is "FS+" (e.g., V_{FS+}, I_{FS+}).

NOTE 2 In place of a letter symbol, the abbreviation "FS+" is commonly used.

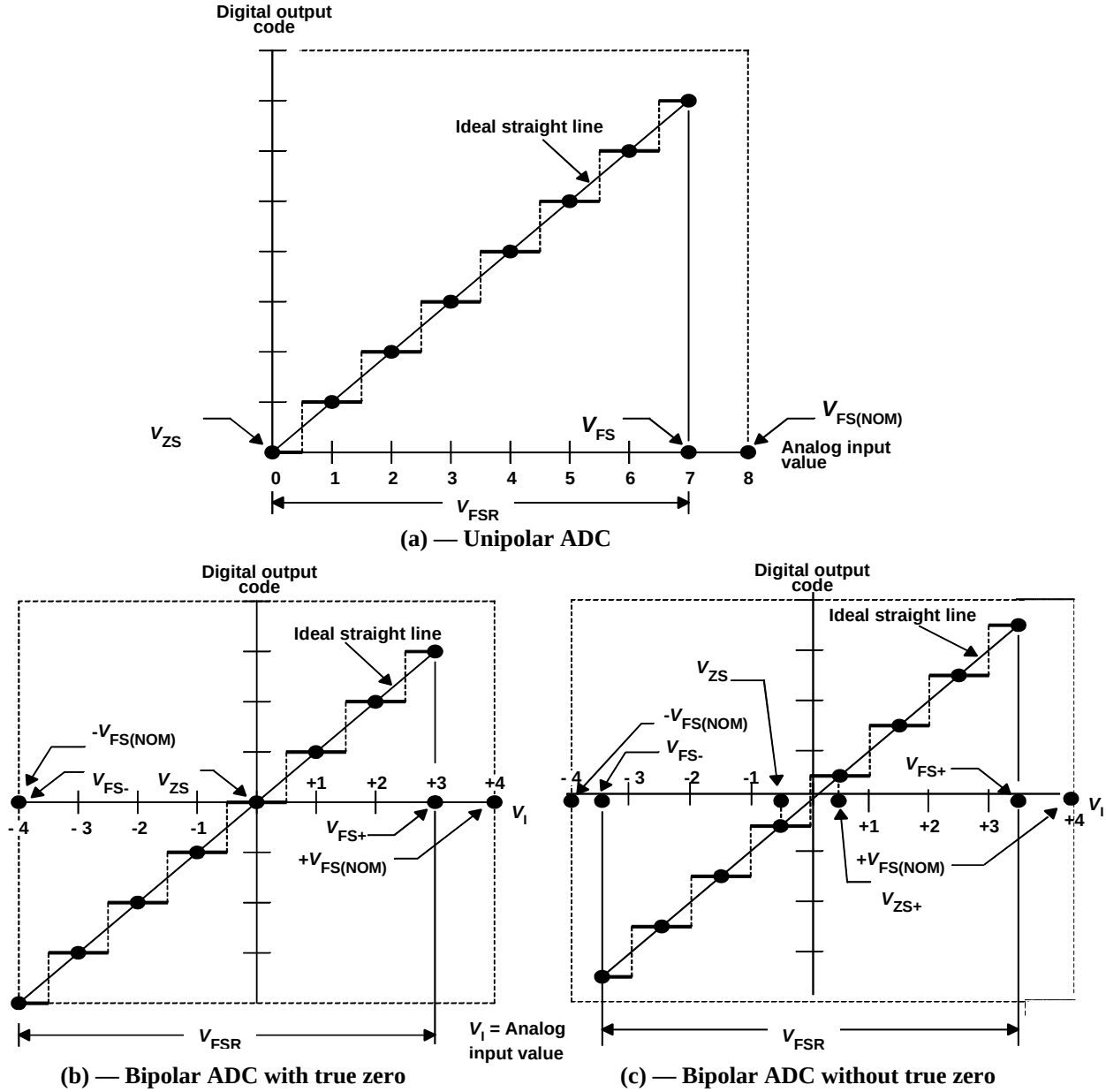


Figure 2.5-3 — Ideal straight line, full-scale value and zero-scale value (shown for ideal linear ADCs)

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

full-scale range, nominal (of a linear ADC or **DAC) (V_{FSRnom}** or **I_{FSRnom}):** The total range in analog values that can be coded with uniform accuracy by the total number of steps, with this number rounded up to the next higher power of 2. (See Figure 2.5-3.)

NOTE In place of the letter symbols "V_{FSRnom}" and "I_{FSRnom}", the abbreviation "FSR(nom)" is commonly used.

EXAMPLE Using a straight binary n-bit code format, it follows that

FSR(nom) = 2^n x (nominal value of step width), for an ADC, and

FSR(nom) = 2^n x (nominal value of step height), for a DAC.

full-scale range, (practical) (of a linear ADC or **DAC) (V_{FSR}** or **I_{FSR}) (V_{FSRpr}** or **I_{FSRpr}):** The total range of analog values that correspond to the ideal straight line. (See Figure 2.5-3.)

NOTE 1 The qualifying adjective "practical" may nearly always be deleted from this term, provided that the term "nominal full-scale range" is not also shortened by deleting "nominal". This permits use of the shorter letter symbols or abbreviations. (See note 2.)

NOTE 2 In place of the letter symbols "V_{FSR}" and "I_{FSR}", the abbreviation "FSR" is commonly used; in place of the letter symbols "V_{FSRpr}" and "I_{FSRpr}", the abbreviation "FSR(pr)" is commonly used.

NOTE 3 The (practical) full-scale range has only a nominal value because it is defined by the end points of the ideal straight line.

EXAMPLE Using a straight binary n-bit code format, it follows that

FSR = (2^n – 1) x (nominal value of step width), for an ADC, and

FSR = (2^n – 1) x (nominal value of step height), for a DAC.

full-scale value, nominal (V_{FSnom} or **I_{FSnom}):** An analog value derived from the nominal full-scale range:

— for a unipolar converter, $V_{FSnom} = V_{FSRnom}$; ($I_{FSnom} = I_{FSRnom}$)

— for a bipolar converter, $V_{FSnom} = ½\ V_{FSRnom}$; ($I_{FSnom} = ½\ I_{FSRnom}$). (See Figure 2.5-3.)

NOTE 1 In some data sheets, this analog value is used as a reference value for adjustment procedures or as a rounded value for the full-scale range.

NOTE 2 In place of the letter symbols "V_{FSnom}" and "I_{FSnom}", the abbreviation "FS(nom)" is commonly used.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

gain point (of an adjustable ADC [DAC]): The point in the transfer diagram corresponding to the midstep [step] value of the step for which gain error is specified (usually full scale), and in reference to which the gain adjustment is performed. (See Figure 2.5-4 [Figure 2.5-5].)

NOTE Gain adjustment causes only a change of the slope of the transfer diagram, without changing the offset error.

ideal straight line (of a linear ADC [DAC]): In the transfer diagram, a straight line between the specified points for the most positive (least negative) and most negative (least positive) nominal midstep [step] values. (See Figure 2.5-1 and Figure 2.5-3 [Figure 2.5-2].)

NOTE The ideal straight line passes through all the points for nominal midstep [step] values.

linear ADC: An ADC having steps ideally of equal width excluding the steps at the two ends of the total range of analog input values.

NOTE Ideally, the width of each end step is one half the width of any other step. (See Figure 2.5-1.)

linear DAC: A DAC having steps ideally of equal height. (See Figure 2.5-2.)

LSB: (1) The abbreviation for "least significant bit", that is, for the bit that has the lowest positional weight in a natural binary numeral.

EXAMPLE In the natural binary numeral "1010", the rightmost bit "0" is the LSB.

(2) The unit symbol for the magnitude of the analog resolution of a linear converter, which serves as a reference unit to express the magnitude of other analog quantities of that same converter, especially of analog errors, as multiples or submultiples of the magnitude of the analog resolution.

EXAMPLE "½ LSB" means an analog quantity equal to one half of the analog resolution.

NOTE The unit symbol LSB refers to the fact that, for a natural binary code, the analog resolution corresponds to the nominal positional weight attributed to the least significant bit of the binary numeral. In this case, the identity "1 LSB equals the analog resolution" leads, for an n-bit resolution, to

$$1\,\mathrm{LSB} = \frac{\mathrm{FSR}}{2^n - 1} = \frac{\mathrm{FSR(nom)}}{2^n}$$

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

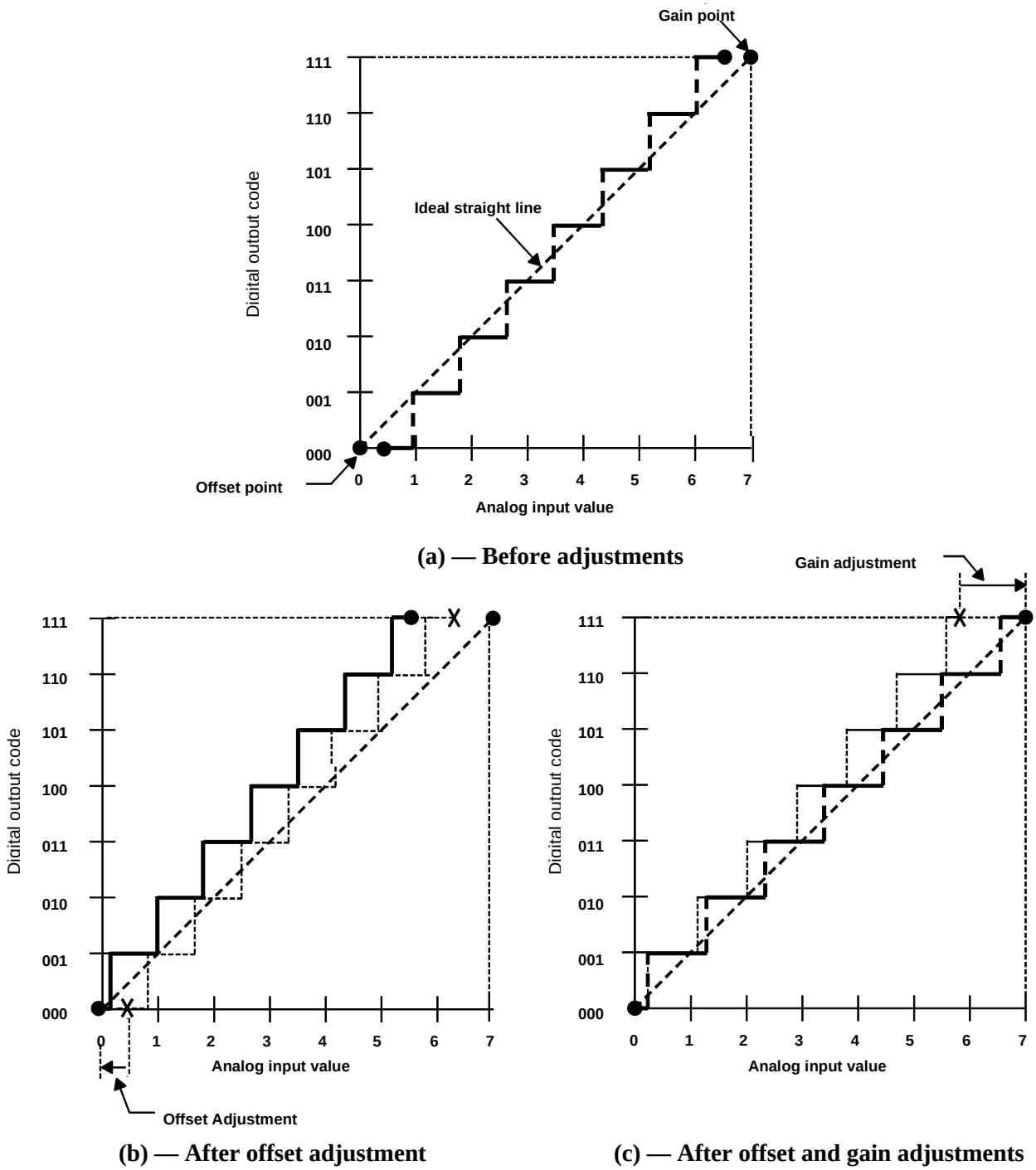


Figure 2.5-4 — Adjustment in offset point and gain point of an ADC

NOTE In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

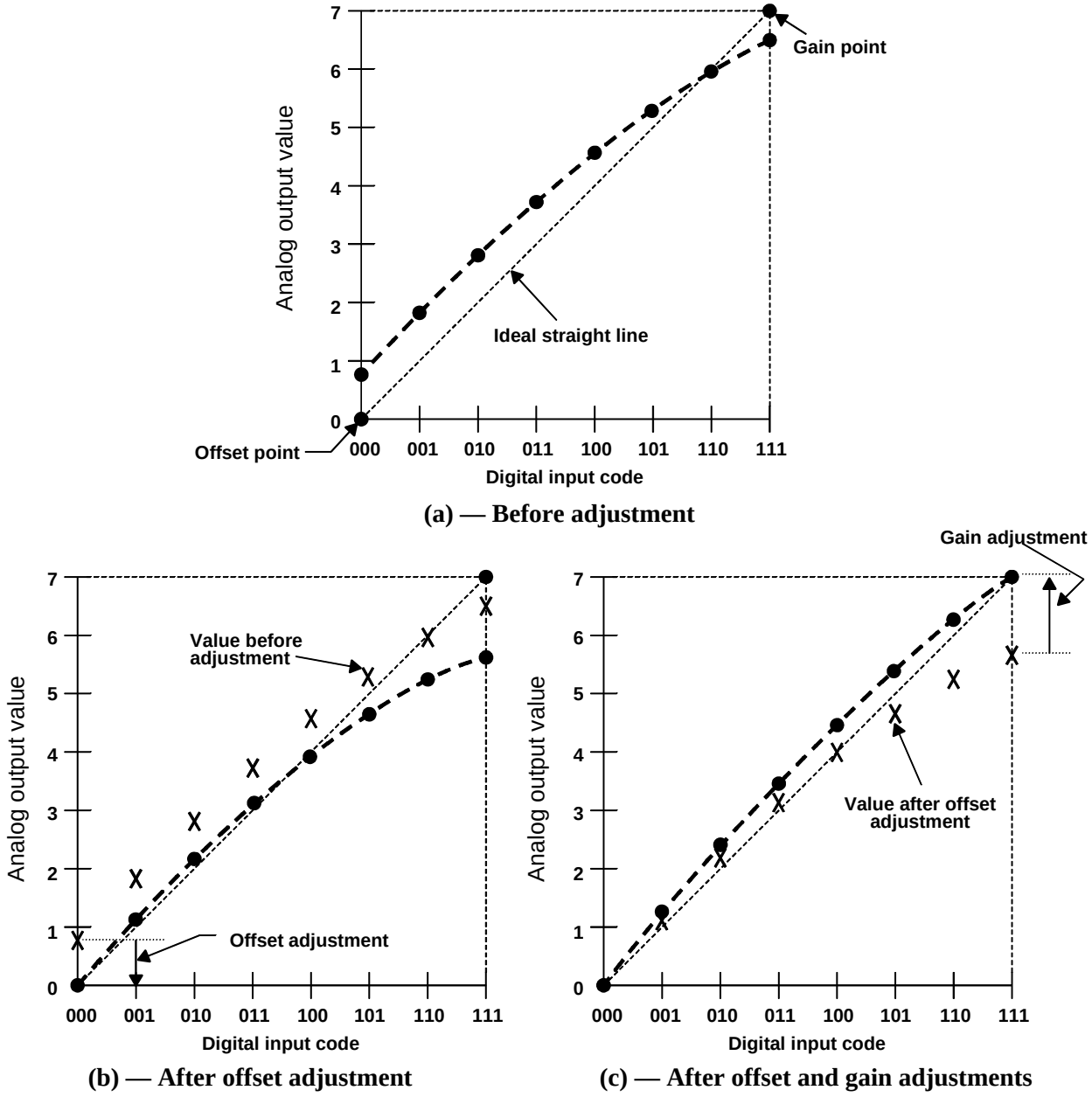


Figure 2.5-5 — Adjustment in offset point and gain point of an ADC

NOTE In the above examples, the offset point is referred to the step with the digital code 000, and the gain point is referred to the step with the digital code 111.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

midstep value (of an ADC): The analog value for the center of the step excluding the steps at the two ends of the total range of analog input values.

NOTE For the end steps, the midstep value is defined as the analog value that results when the analog value for the transition to the adjacent step is reduced or enlarged, as appropriate, by half the nominal value of the step width. (See Figure 2.5-1.)

midstep value, nominal (of an ADC): A specified analog value within a step that is ideally represented free of error by the corresponding digital output code. (See Figure 2.5-1.)

missing code (of an ADC): An intermediate code that is absent when the changing analog input to an ADC causes a multiple code change in the digital output. (See Figure 2.5-6.)

monotonicity (of an ADC [a DAC]): A property of the transfer function that ensures the consistent increase or decrease of the digital [analog] output in response to a consistent increase or decrease of the analog [digital] input. (Figure 2.5-7 illustrates nonmonotonic conversion.)

NOTE An intermediate increment with the value of zero does not invalidate monotonicity.

multiplying DAC: A DAC having at least two inputs, at least one of which is digital, and whose analog output value is proportional to the product of the inputs.

nonlinear ADC [DAC]: An ADC [DAC] with a specified nonlinear transfer function between the nominal midstep [step] values and the corresponding step widths [heights].

NOTE The function may be continuously nonlinear or piecewise linear.

offset point (of an adjustable ADC [DAC]): The point in the transfer diagram corresponding to the midstep [step] value of the step about which the transfer diagram rotates when the gain is adjusted. (See Figure 2.5-4 [2.5-5].)

NOTE Offset adjustment must be performed with respect to this point so that it causes only a parallel displacement of the transfer curve.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

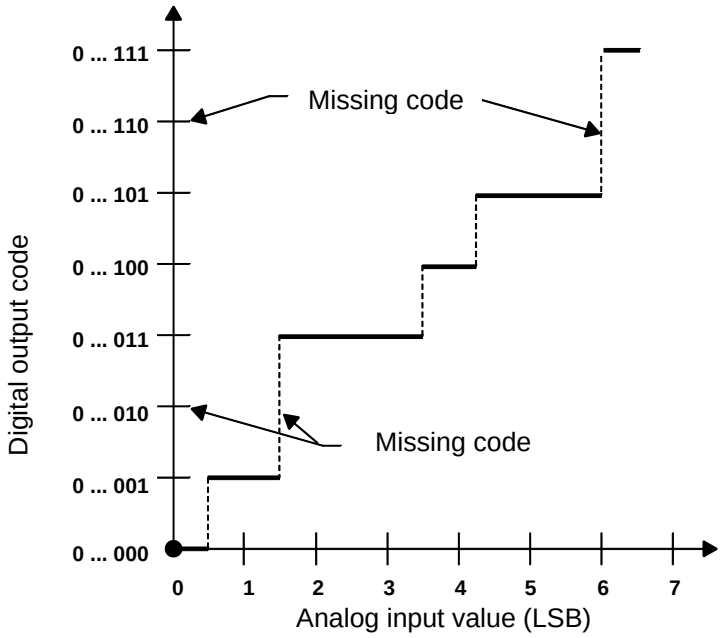
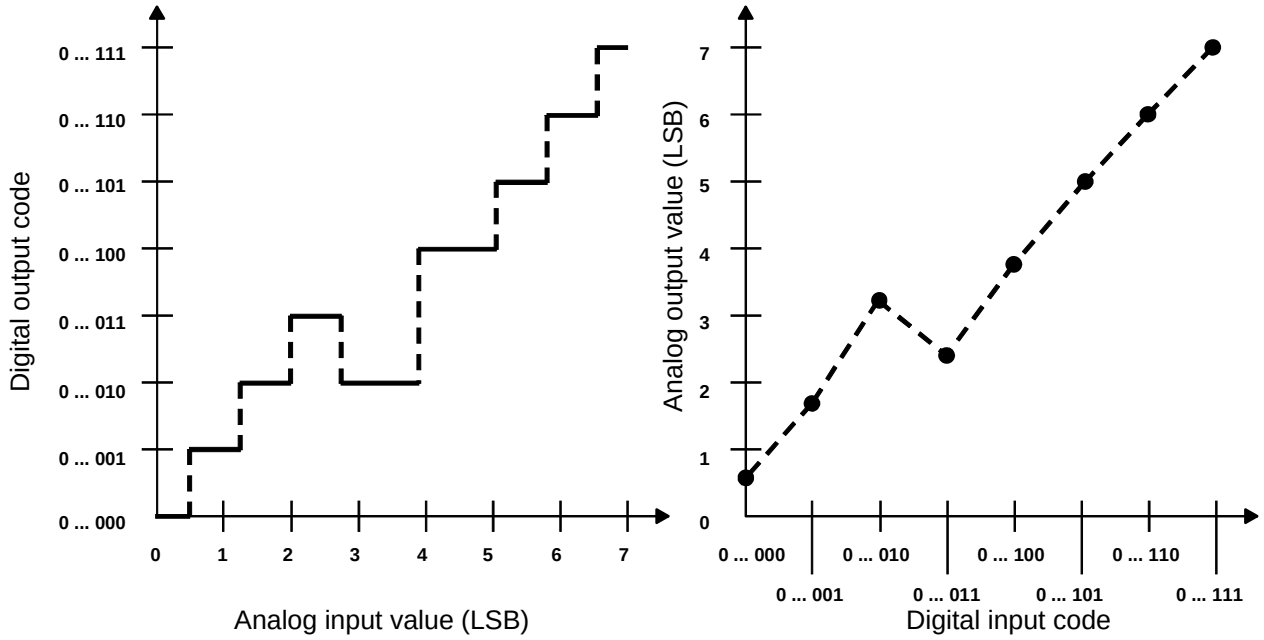


Figure 2.5-6 — Missing code of an ADC



(a) — ADC **(b) — DAC**

Figure 2.5-7 — Nonmonotonic conversion of an ADC or DAC

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

resolution (general term)

NOTE 1 Resolution as a capability can be expressed in different forms (see "resolution, analog", "resolution, numerical", and "resolution, relative").

NOTE 2 Resolution is a design parameter and therefore has only a nominal value.

NOTE 3 The terms for these different forms may all be shortened to "resolution" if no ambiguity is likely to occur (for example, when the dimension of the term is also given).

resolution (of an ADC): The degree to which nearly equal values of the analog input quantity can be discriminated.

resolution (of a DAC): The degree to which nearly equal values of the analog output quantity can be produced.

resolution, analog (of a linear or **nonlinear ADC [DAC]):** The nominal value of the step width [height].

NOTE For a linear ADC [DAC], the constant magnitude of the analog resolution is often used as the reference unit LSB.

resolution, numerical: The number (n) of digits in the chosen numbering system necessary to express the total number of steps.

NOTE 1 The numbering system is normally a binary or a decimal system.

NOTE 2 In the binary-coded-decimal numbering system, the term "5 digit" refers to an additional decimal digit with the highest positional value, but limited to the decimal figures "0" or "1" as it is represented by only a single bit. This additional digit serves to double the range of values covered by the other "n" digits.

resolution, relative (of a linear ADC or **DAC):** The ratio of the analog resolution to the full-scale range (practical or nominal).

NOTE This ratio is normally expressed as a percentage of the full-scale range (% of FSR or % of FSR(nom)). For high resolutions (high value of n), it is of little importance whether this ratio refers to the practical or nominal full-scale range.

step (of an analog-to-digital or **digital-to-analog conversion):** Any of the individual correlations in the conversion code or any part of the diagram equating to an individual correlation in the transfer diagram.

NOTE 1 For an ADC, a step represents both a fractional range of analog input values and the corresponding digital output code. (See Figure 2.5-1.)

NOTE 2 For a DAC, a step represents both a digital input code and the corresponding discrete analog output value. (See Figure 2.5-2.)

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.1 General terms (cont'd)

step height [step size] (of a DAC): The absolute value of the difference in step values between two adjacent steps in the transfer diagram. (See Figure 2.5-2.)

NOTE For companding DACs, the term "step size" is in general use.

step value (of a DAC): The value of the analog output representing a digital input code. (See Figure 2.5-2)

step value, nominal (of a DAC): A specified step value that exactly represents the corresponding digital input code. (See Figure 2.5-2.)

step width (of an ADC): The absolute value of the difference between the two ends of the range of analog values corresponding to one step. (See Figure 2.5-1.)

temperature coefficients of analog characteristics (α)

NOTE 1 The letter symbol for the temperature coefficient of an analog characteristic consists of the letter symbol α with a subscript referring to the relevant characteristic, e.g., α_{EG} for the temperature coefficient of the gain error.

NOTE 2 Temperature coefficients of analog characteristics are usually specified in "parts per million (relative to the full-scale value) per degree Celsius", that is, in "ppm/^{o}C".

zero scale (of an ADC [a DAC] with true zero): A term used to refer a characteristic to the step whose nominal midstep [step] value equals zero. (See Figure 2.5-3a and Figure 2.5-3b.)

NOTE 1 The subscript for the letter symbol of a characteristic at zero scale is "ZS".

NOTE 2 In place of a letter symbol, the abbreviation "ZS" is commonly used.

zero scale, negative (of an ADC or **DAC with no true zero):** A term used to refer a characteristic to the negative step closest to analog zero. (See Figure 2.5-3c.)

NOTE 1 The subscript for the letter symbol of a characteristic at negative zero scale is "ZS–", e.g., V_{ZS-}, I_{ZS-}.

NOTE 2 In place of a letter symbol, the abbreviation "ZS–" is commonly used.

zero scale, positive (of an ADC or **DAC with no true zero):** A term used to refer a characteristic to the positive step closest to analog zero. (See Figure 2.5-3c.)

NOTE 1 The subscript for the letter symbol of a characteristic at positive zero scale is "ZS+", e.g., V_{ZS+}, I_{ZS+}.

NOTE 2 In place of a letter symbol, the abbreviation "ZS+" is commonly used.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.2 Static performance

accuracy: See 2.5.2.4.

asymmetry, full-scale (of a DAC with a bipolar analog range) (ΔI_{FSS} or ΔV_{FSS}): The difference between the absolute values of the two full-scale analog values.

compliance, current (of a DAC) ($\Delta I_{O(op)}$): The permissible range of output current within which the specifications are valid.

compliance, voltage (of a DAC) ($\Delta V_{O(op)}$): The permissible range of output voltage within which the specifications are valid.

errors: See 2.5.2.4.

supply voltage sensitivity (of a DAC) (k_{SVS}): The change in full-scale output current (or voltage) caused by a change in supply voltage.

NOTE This sensitivity is usually expressed as the ratio of the percentage change of full-scale current (or voltage) to the percentage change of supply voltage.

2.5.2.3 Dynamic performance

conversion rate (of an externally controlled ADC) (f_c): The number of conversions per unit time.

NOTE 1 The maximum conversion rate should be specified for full resolution.

NOTE 2 The conversion rate is usually expressed as the number of conversions per second.

NOTE 3 Because of settling or recovery time, the maximum specified conversion rate is smaller than the reciprocal of the worst-case conversion time.

conversion time (of an ADC) (t_c): The time elapsed between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog value.

delay time, (digital) (of a linear or **a multiplying DAC) (t_d** or **t_{dd}):** The time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value, ignoring glitches. (See Figure 2.5-8.)

NOTE For a multiplying DAC, the full term and the additional subscript *d* must be used to distinguish between the digital and the reference delay times.

delay time, reference (of a multiplying DAC) (t_{dr}): The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output passes a specified value that is close to its initial value. (See Figure 2.5-10.)

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.3 Dynamic performance (cont'd)

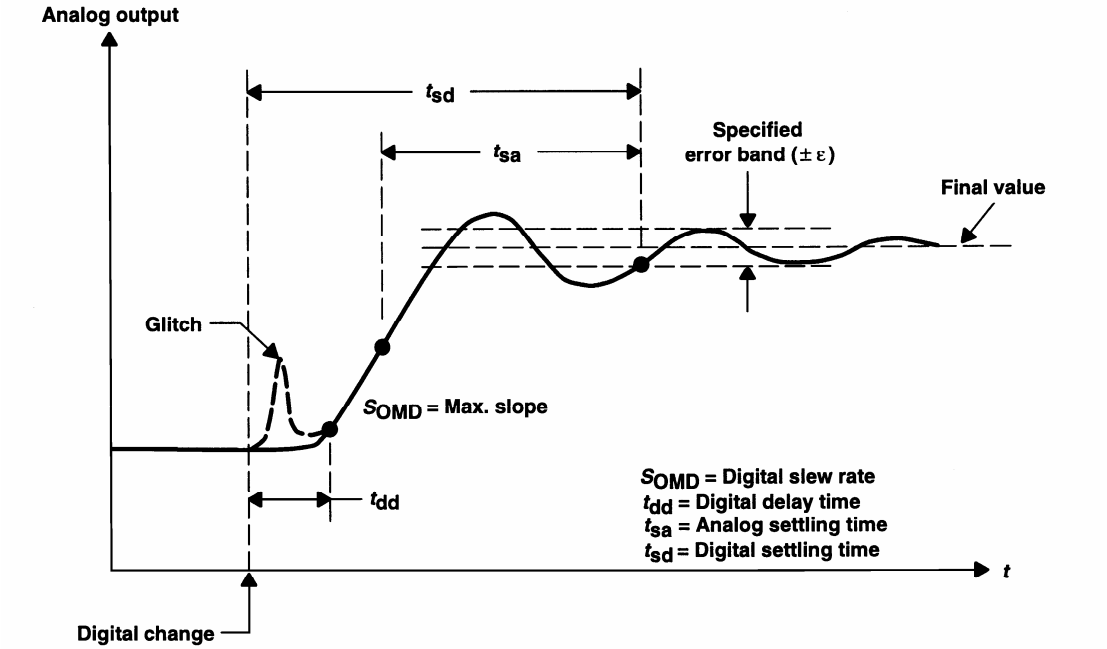


Figure 2.5-8 — Output characteristics of a linear or a multiplying DAC for a step change in the digital input code

feedthrough capacitance (of a multiplying DAC) (C_F): The value of the capacitance for a specified value of resistance in an equivalent circuit for the calculation of the feedthrough error.

NOTE The equivalent circuit consists of a high-pass R-C filter between the reference input and analog output.

feedthrough error: See 2.5.2.4.

glitch (of a DAC): A short, undesirable transient in the analog output following a code change at the digital input. (See Figure 2.5-8.)

glitch area (of a DAC): The time integral of the analog value of the glitch transient.

NOTE 1 Usually, the maximum specified glitch area refers to a specified worst-case code change.

NOTE 2 Instead of a letter symbol, the abbreviation “GA” is in use.

glitch energy (of a DAC): The time integral of the electrical power of the glitch transient.

NOTE 1 Usually, the maximum specified glitch energy refers to a specified worst-case code change.

NOTE 2 Instead of a letter symbol, the abbreviation “GE” is in use.

pedestal (error): See 2.5.2.4.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.3 Dynamic performance (cont'd)

ramp delay, steady-state (of a multiplying DAC) ($t_{d(ramp)}$): The time separation between the actual curve of the analog output and the theoretical curve (with no delay) for a ramp in reference voltage, after the settling time to steady-state ramp has elapsed. (See Figure 2.5-9.)

settling time, analog (of a DAC) (t_{sa}): The time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for the last time a specified error band about its final value. (See Figure 2.5-8 and Figure 2.5-10.)

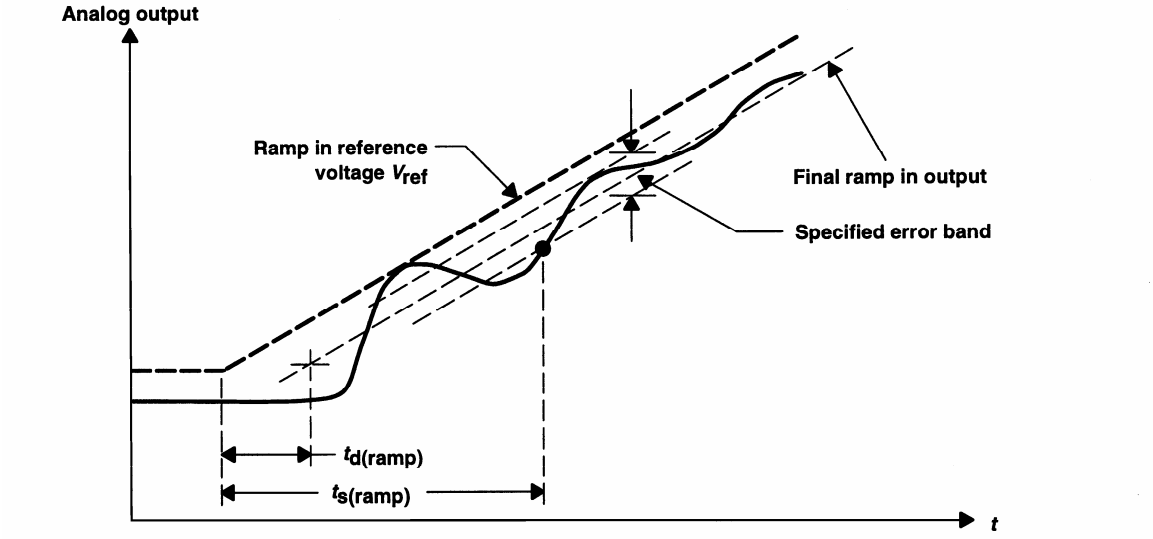
settling time, (digital) (of a linear or **a multiplying DAC) (t_s** or **t_{sd}):** The time interval between the instant when the digital input changes and the instant when the analog output value enters for the last time a specified error band about its final value. (See Figure 2.5-8.)

NOTE For a multiplying DAC, the full term and the additional subscript *d* must be used to distinguish between the digital and the reference settling times.

settling time, reference (of a multiplying DAC) (t_{sr}): The time interval between the instant when a step change of the reference voltage occurs and the instant when the analog output enters for the last time a specified error band about its final value. (See Figure 2.5-10.)

NOTE Specifications for the reference settling time are usually given for the highest allowed step change in reference voltage.

settling time to steady-state ramp (of a multiplying DAC) ($t_{s(ramp)}$): The time interval between the instant a ramp in the reference voltage starts and the instant when the analog output value enters for the last time a specified error band about the final ramp in the output. (See Figure 2.5-9.)



$t_{d(ramp)}$ = Steady-state ramp delay
$t_{s(ramp)}$ = Settling time to steady-state ramp delay

Figure 2.5-9 — Output characteristics for a ramp in reference voltage of a multiplying DAC

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.3 Dynamic performance (cont'd)

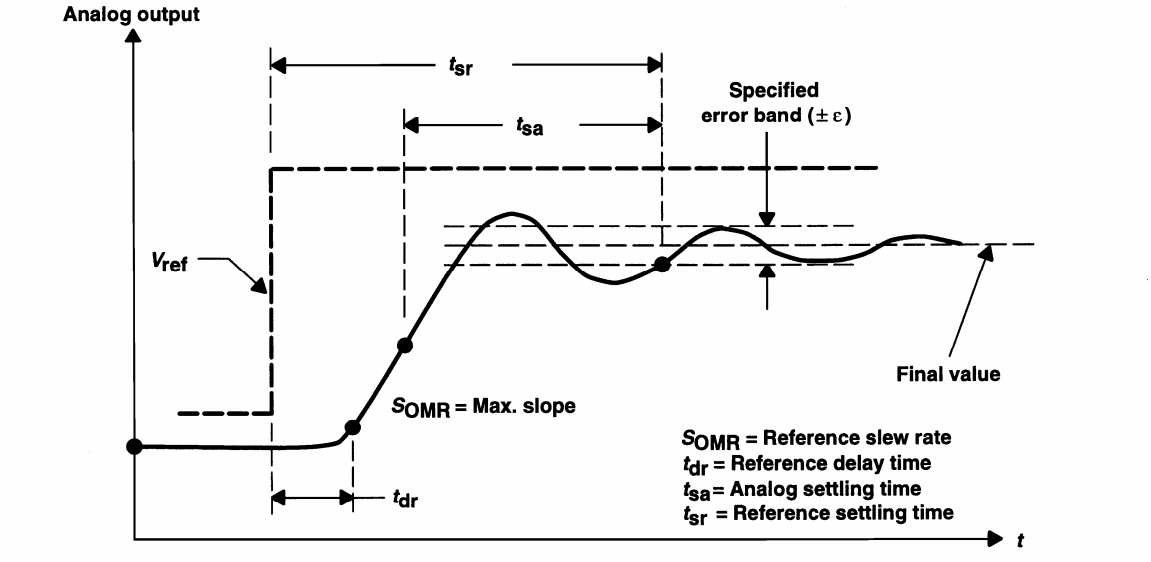


Figure 2.5-10 — Output characteristics for a step change in reference voltage of a multiplying DAC

skewing time, internal (of a DAC): The difference in internal delay between the individual output transitions for a given change of digital input.

NOTE The internal (as well as external) skew has a major influence on the settling time for critical changes in the digital input, e.g., a 1-LSB change from 011...111 to 100...000, and is an important source of commutation noise.

slew rate, (digital) (of a linear or **a multiplying DAC) (S_{OM}** or **S_{OMD}):** The maximum rate of change of the analog output value when a change of the digital input code causes a large step change of the analog output value. (See Figure 2.5-8.)

NOTE 1 For a multiplying DAC, the full term and the additional subscript D must be used to distinguish between the digital and the reference slew rates.

NOTE 2 The abbreviations “SR” and “SR(dig)” are also used.

slew rate, reference (of a multiplying DAC) (S_{OMR}): The maximum rate of change of the analog output following a large step change of the reference voltage. (See Figure 2.5-10.)

NOTE The abbreviation “SR(ref)” is also used.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy)

The definitions in this section describe the errors as the difference between the actual value and the nominal value of the analog quantity. As such they may be expressed in conventional units (for example, millivolts) or as multiples or submultiples of 1 LSB. An error can also be expressed as a relative value, for example, in "% of FSR". In this case, it is common practice to use the same term as for the analog value.

absolute accuracy error: Synonym for "total error".

feedthrough error (of a multiplying DAC) (E_F): An error in analog output, due to variation in the reference voltage, that appears as an offset error and is proportional to the frequency and amplitude of the reference signal.

NOTE 1 The specification for the feedthrough error is given for the digital input for which the offset error is specified, and for a reference signal of specified frequency and amplitude.

NOTE 2 This error may also be expressed as a peak-to-peak analog value.

full-scale error (of a linear ADC [DAC]) (E_{FS}): The difference between the actual midstep [step] value and the nominal midstep [step] value at specified full scale.

NOTE Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

gain error (of a linear ADC [DAC]) (E_G): The difference between the actual midstep [step] value and the nominal midstep [step] value in the transfer diagram at the specified gain point after the offset error has been adjusted to zero. (See Figure 2.5-11.)

NOTE 1 The terms "gain error" and "offset error" should be used only for errors that can be adjusted to zero. Otherwise, the terms "zero-scale error" and "full-scale error" should be used.

NOTE 2 Usually the specified steps for the specification of gain error and offset error are the steps at the end of the practical full-scale range.

NOTE 3 The midstep value of a step is defined (for an ADC) as the value for a point ½ LSB apart from the adjacent transition.

instability, long-term (accuracy) ($\Delta E_{(\Delta t)}$ or $\Delta E_{(t)}$): The additional error caused by the ageing of the components and specified for a relatively long period of time.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy) (cont'd)

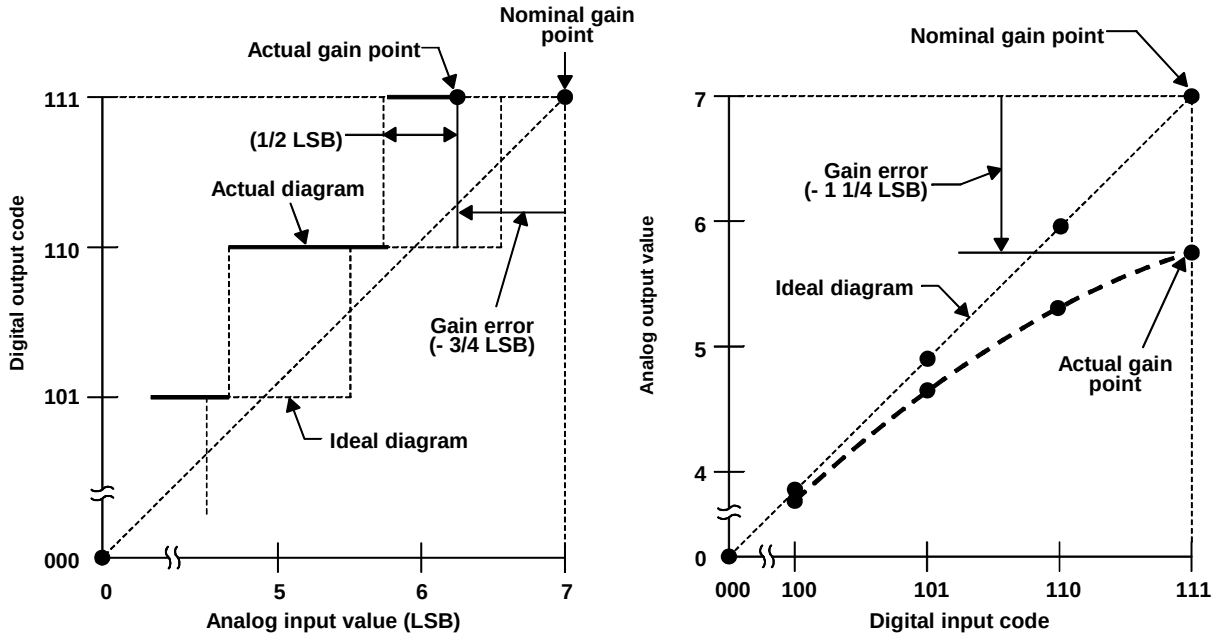


Figure 2.5-11 — Gain error of a linear, 3-bit-binary-coded converter (specified at step 111), after correction of the offset error

linearity error, best-straight-line (of a linear and adjustable ADC) ($E_{L(adj)}$): The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 2.5-12a.)

NOTE 1 The inherent quantization error is not included in the best-straight-line linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±½ LSB.

NOTE 2 For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 2.5-12a.)

linearity error, best-straight-line (of a linear and adjustable DAC) ($E_{L(adj)}$): The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to minimize the magnitude of the extreme values of this difference. (See Figure 2.5-12b.)

NOTE For a uniformly curved transfer diagram, the extreme values will be very close to half of the magnitude of the end-point linearity error. (See Figure 2.5-12b.)

linearity error, differential (of a linear ADC [DAC]) (E_D): The difference between the actual step width [height] and the ideal value (1 LSB). (See Figure 2.5-13.)

NOTE A differential linearity error greater than 1 LSB can lead to missing codes in an ADC or to nonmonotonicity of an ADC [a DAC]. (See Figure 2.5-6 and Figure 2.5-7.)

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy) (cont'd)

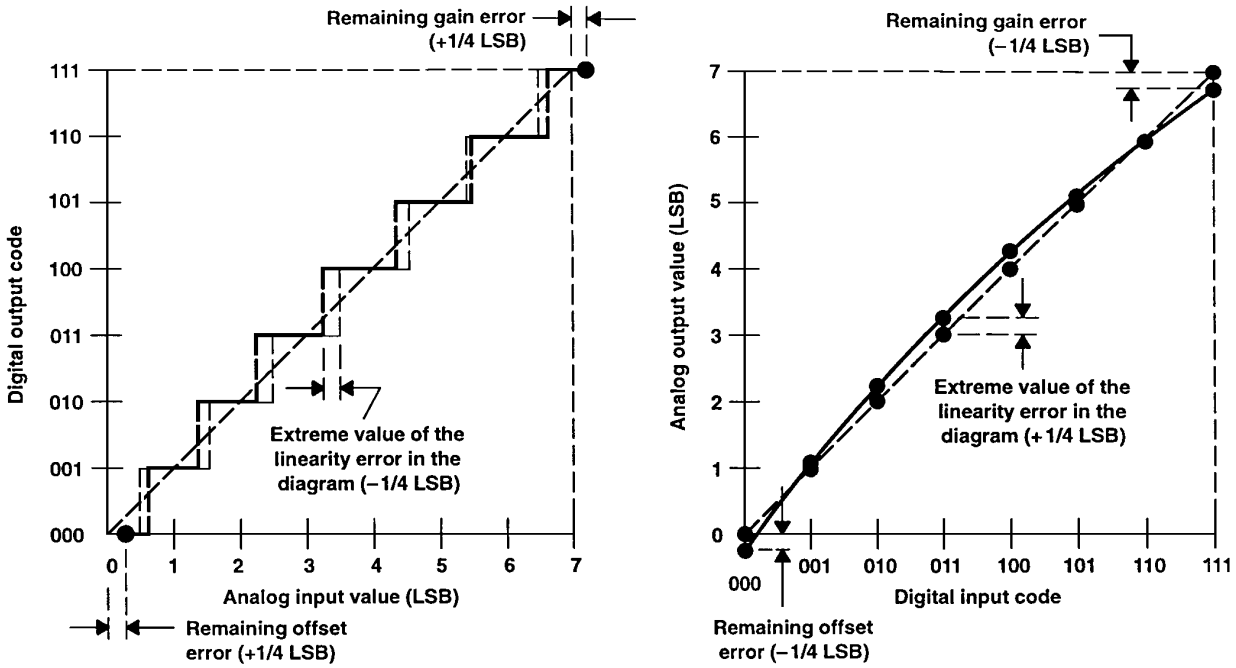


Figure 2.5-12 — Best straight-line linearity error of a linear, 3-bit binary-coded converter

linearity error, end-point (of a linear and adjustable ADC) (E_L): The difference between the actual analog value at the transition between any two adjacent steps and its ideal value after offset error and gain error have been adjusted to zero. (See Figure 2.5-14a.)

NOTE 1 The shortened term "linearity error" is commonly used and is sufficient if no ambiguity with the term "best-straight-line linearity error" is likely to occur.

NOTE 2 The inherent quantization error is not included in the linearity error of an ADC. The ideal value for the transition corresponds to the nominal midstep value ±½ LSB.

linearity error, end-point (of a linear and adjustable DAC) (E_L): The difference between the actual step value and the nominal step value after offset error and gain error have been adjusted to zero. (See Figure 2.5-14b.)

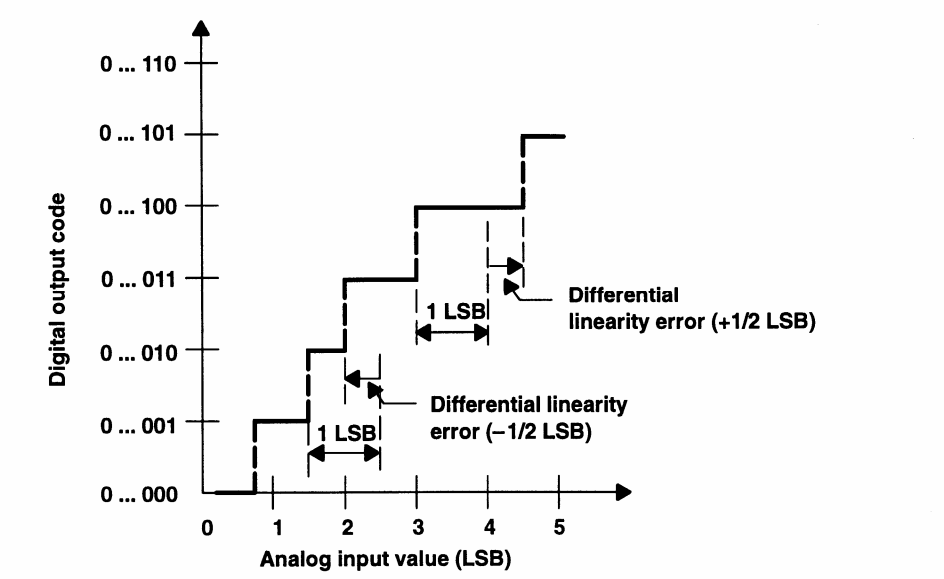
NOTE The shortened term "linearity error" is commonly used and is sufficient if no ambiguity with the term "best-straight-line linearity error" is likely to occur.

offset error (of a linear ADC [DAC]) (E_O): The difference between the actual midstep [step] value and the nominal midstep [step] value at the offset point. (See Figure 2.5-15.)

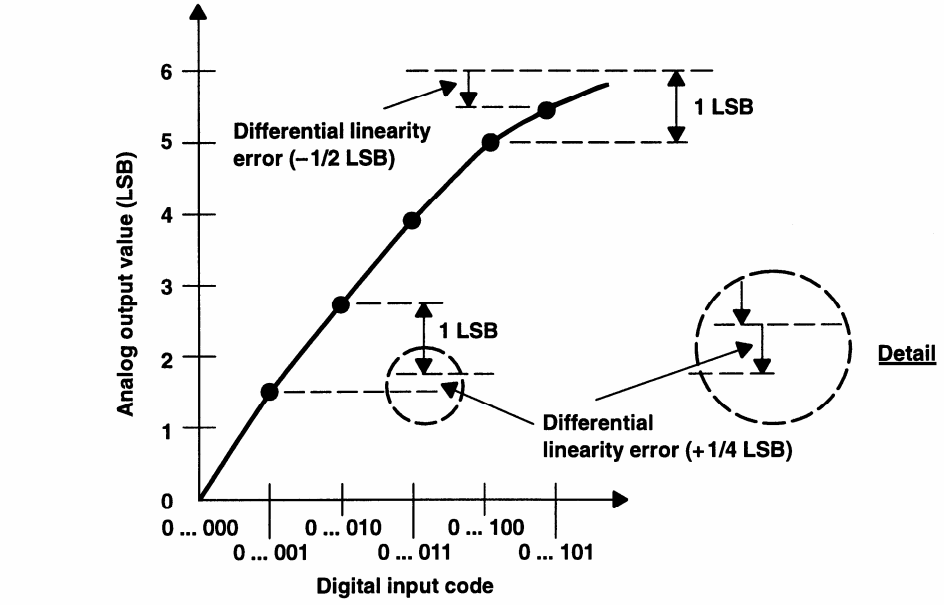
NOTE See notes 1, 2, and 3 under "gain error".

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy) (cont'd)



(a) — ADC

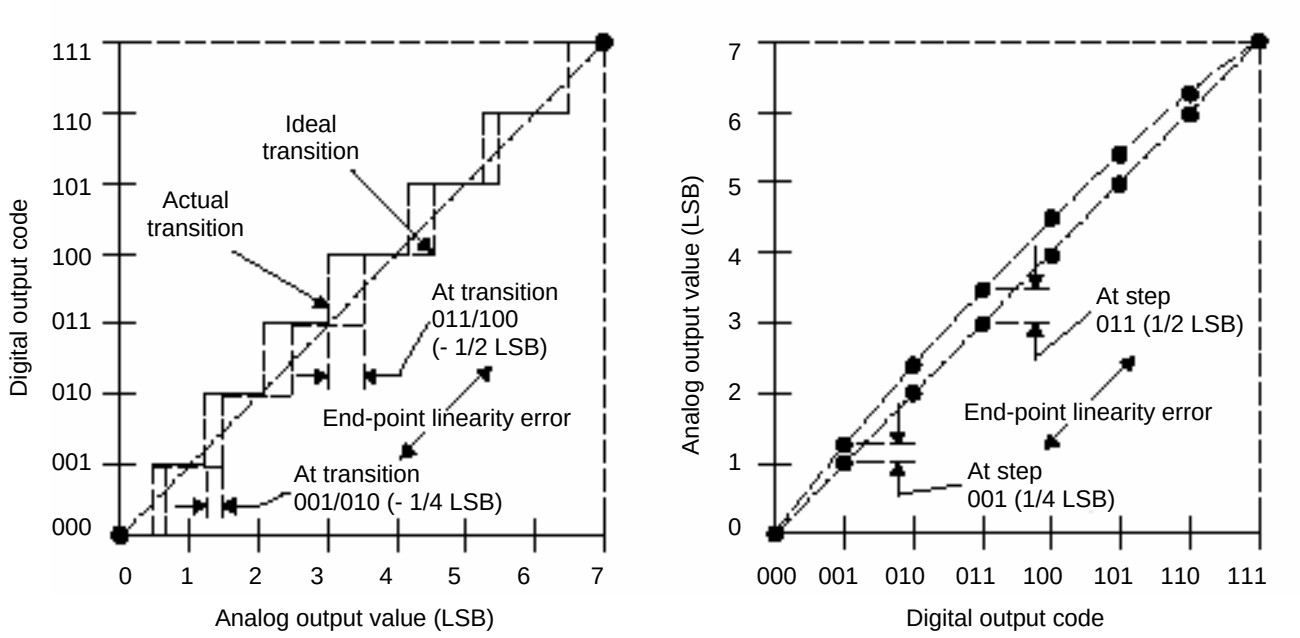


(b) — DAC

Figure 2.5-13 — Differential linearity error of a linear converter

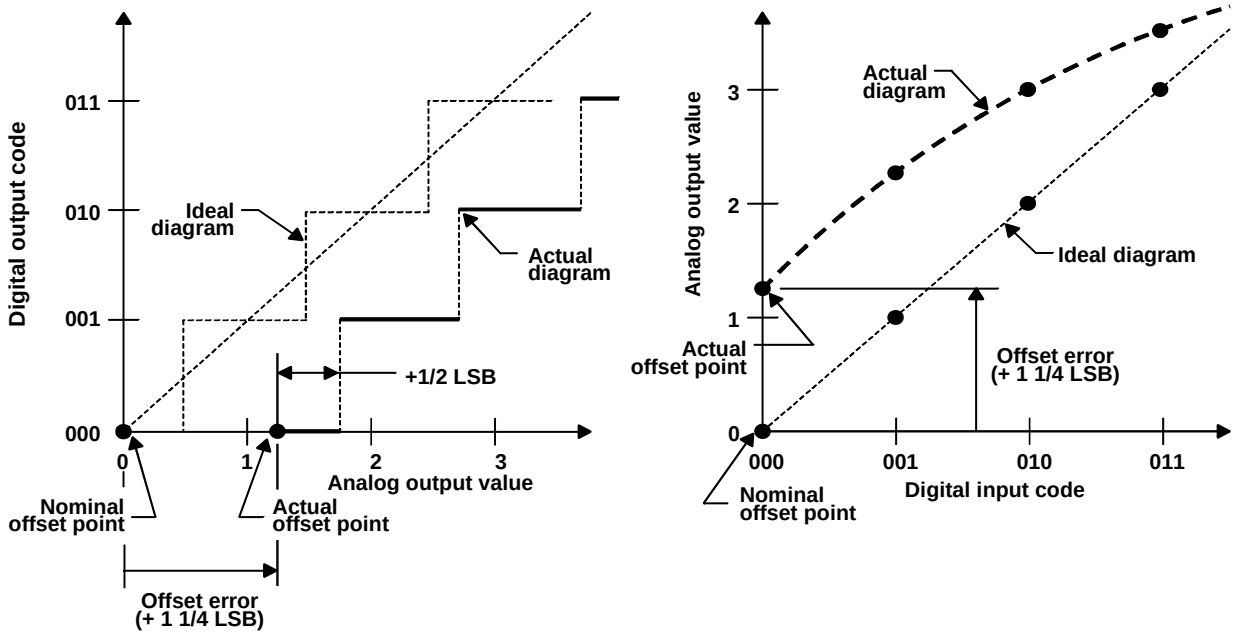
2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy) (cont'd)



(a) — ADC **(b) — DAC**

Figure 2.5-14 — End-point linearity error of a linear, 3-bit binary-coded converter (offset error and gain error are adjusted to the value zero)



(a) — ADC **(b) — DAC**

Figure 2.5-15 — Offset error of a linear, 3-bit binary-coded converter (specified at step 000)

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy) (cont'd)

pedestal (error) (E_p): A dynamic offset error produced in the commutation process.

quantization error, inherent (of an ideal ADC): Within a step, the maximum (positive or negative) possible deviation of the actual analog input value from the nominal midstep value.

NOTE 1 This error follows necessarily from the quantization procedure. For a linear ADC, its value equals ±½ LSB. (See Figure 2.5-1.)

NOTE 2 Use of the term "resolution error" in place of "inherent quantization error" is deprecated, because "resolution" as a design parameter has a nominal value only.

roll-over error (of an ADC with decimal output and **autopolarity) (E_{RO}):** The difference in output readings with the analog input switched between positive and negative values of the same magnitude (close to full scale).

total error; absolute accuracy error (of a linear ADC) (E_T): The maximum difference (positive or negative) between an analog value and the nominal midstep value within any step. (See Figure 2.5-16a.)

NOTE 1 If this error is expressed as a relative value, the term "relative accuracy error" should be used rather than "absolute accuracy error" or "total error".

NOTE 2 This error includes all contributions from offset error, gain error, linearity error, and the inherent quantization error.

total error; absolute accuracy error (of a linear DAC) (E_T): The difference (positive or negative) between the actual step value and the nominal step value for any step. (See Figure 2.5-16b.)

NOTE 1 If this error is expressed as a relative value, the term "relative accuracy error" should be used rather than "absolute accuracy error" or "total error".

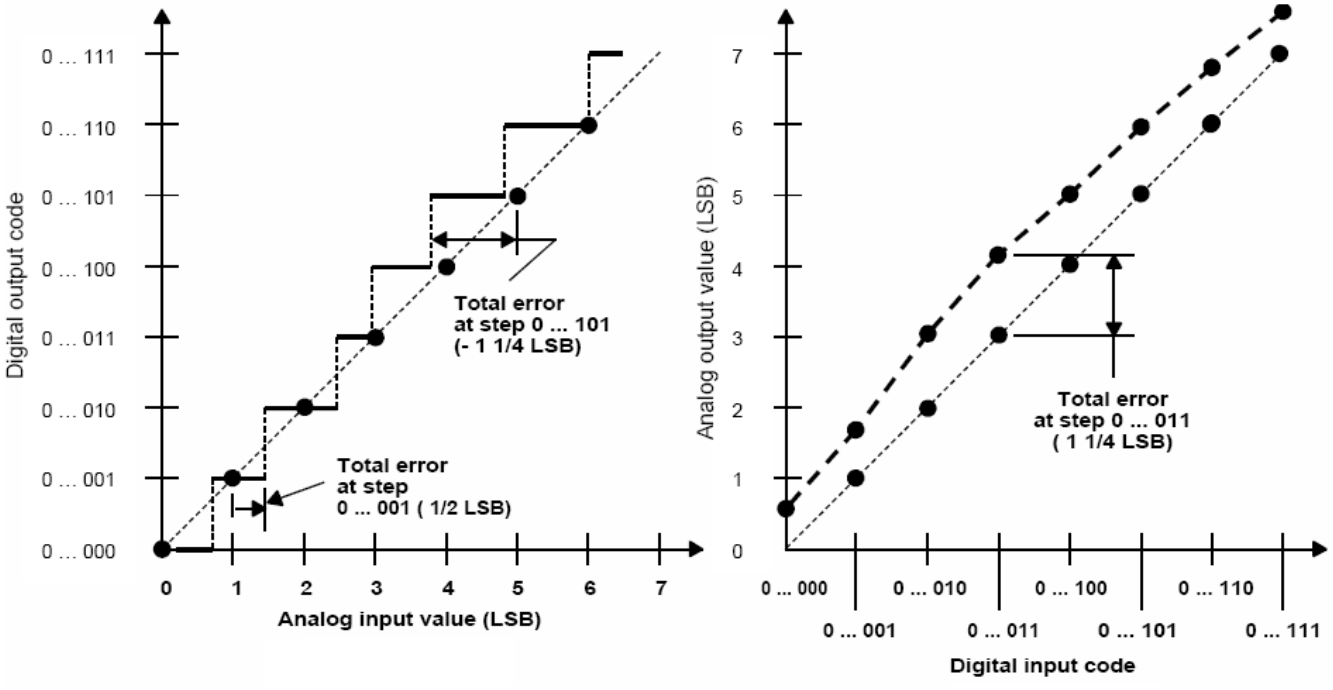
NOTE 2 This error includes all contributions from offset error, gain error, and linearity error.

zero-scale error (of a linear ADC [DAC]) (E_{ZS}): The difference between the actual midstep [step] value and the nominal midstep [step] value at specified zero scale.

NOTE Normally, this error specification is applied to converters that have no arrangement for an external adjustment of offset error and gain error.

2.5.2 Analog-to-digital and digital-to-analog converters (cont'd)

2.5.2.4 Errors, (accuracy) (cont'd)



(a) — ADC **(b) — DAC**

Figure 2.5-16 — Absolute accuracy error, total error of a linear converter

2.6 Terms and definitions applicable to voltage regulator integrated circuits

2.6.1 General voltage regulator concepts

foldback current limiting: A type of overload protection for voltage regulators wherein, under overload conditions, the load current is reduced to some low level relative to a limiting load current.

latch-up (of a voltage regulator): A condition in which a regulator has been driven into the foldback limiting mode and will not respond to the removal of the overload.

series control element (series pass element): A circuit element (usually a transistor), in series with the load, that controls the output voltage by dropping a variable portion of the input voltage.

shutdown mode: A condition in which the series control element of the regulator is turned off.

NOTE This is an optional feature usually employed for remote control.

voltage regulator: A circuit or portion of a circuit that provides isolation between the load and the supply to be regulated so that the load voltage remains relatively independent of load current or input voltage fluctuations.

2.6 Terms and definitions applicable to voltage regulator integrated circuits (cont'd)

2.6.2 Regulation, drift, and temperature coefficient

line regulation ($\Delta V_{O(\Delta VI)}$): The change in output voltage, usually expressed as a percentage of output voltage, for a change in input voltage.

load regulation ($\Delta V_{O(\Delta IL)}$ and $\Delta V_{O(\Delta IO)}$): The change in output voltage, usually expressed as a percentage of output voltage, for a change in load current.

output voltage drift ($\Delta V_{O(\Delta t)}$): The change in output voltage, usually expressed as a percentage of output voltage, over a period of time.

temperature coefficient of output voltage (α_{VO}): The change in output voltage, usually expressed as a percentage of the output voltage, divided by the change in temperature.

NOTE This is the average value for the total temperature change.

2.6.3 Voltage level

current-limit sense voltage: The current-sense voltage at which current limiting occurs.

current-sense voltage: The voltage that is a function of the load current and is normally used for control of the current-limiting circuitry.

feedback sense voltage: The voltage that is a function of the output voltage and is used for feedback control of the regulator.

input-output voltage differential ($V_I - V_O$): The difference between the input voltage and the output voltage.

input voltage (V_I): The supply voltage to be regulated.

output voltage (V_O): The regulated voltage presented at the output of a regulator (or current-sensing resistor, if used).

reference voltage (V_{ref}): The voltage that is compared with the feedback sense voltage to control the regulator.

2.6 Terms and definitions applicable to voltage regulator integrated circuits (cont'd)

2.6.4 Current

load current (I_L): The current that is supplied to the load by the regulator.

output current (I_O): Synonym for "load current".

short-circuit current limit (I_{OS}): The output current of the regulator with the output shorted to ground.

shutdown current ($I_{L(sd)}$ and $I_{O(sd)}$): The load current available during the shutdown mode.

standby current ($I_{I(standby)}$): The supply current drawn by the regulator with no output load and no reference voltage load.

2.6.5 Noise

output noise voltage (V_n): The rms output noise voltage with constant load and no input ripples.

peak-to-peak noise voltage ($V_{N(PP)}$): The peak-to-peak output noise voltage with constant load and no input ripples.

ripple rejection (k_{VIO}): The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

2.6.6 Impedance

output impedance (z_o): The small-signal impedance between the regulator output terminal and ground.

2.6.7 Time

line-transient recovery time (t_{RVI}): The time interval between a step-function change of the input level and that instant at which the magnitude of the output level enters for the last time a specified level range containing the final output level.

load-transient recovery time (t_{RIL} and t_{RIO}): The time interval between a step-function change of the load current and that instant at which the magnitude of the output level enters for the last time a specified level range containing the final output level.

2.7 Terms and definitions applicable to charge-transfer devices

2.7.1 Types of charge-transfer devices

bucket-brigade device (BBD): A charge-transfer device that stores charge in discrete regions in a semiconductor and transfers this charge as a packet through a series of switching devices that interconnect these regions.

NOTE This term and its abbreviation may be preceded by bipolar, JFET, MOS, SIS, etc., according to the technology used for the switching devices.

bulk-channel charge-coupled device (BCCD): Synonym for "buried-channel charge-coupled device".

buried-channel charge-coupled device (BCCD): A charge-coupled device that confines the flow of charges to a channel lying beneath the surface of the semiconductor.

charge-coupled device (CCD): A charge-transfer device that stores charge in potential wells and transfers this charge almost completely as a packet by translating the position of the potential wells.

charge-coupled image sensor: A charge-coupled device in which an optical image is converted into packets of charge that can be transferred as the electrical analog of the image.

charge-transfer device (CTD): A device in which operation depends on the movement of discrete packets of charge along or beneath the semiconductor surface or through the interconnections on the semiconductor surface.

conductivity-connected charge-coupled device (C^4D): A charge-coupled device that uses doped regions between the potential wells and hence becomes a hybrid between the charge-coupled device and a bucket-brigade device.

junction-gate charge-coupled device: A buried-channel charge-coupled device that uses a diffused junction to isolate the transfer gate.

n-channel charge-coupled device: A charge-coupled device fabricated so that the charges stored in the potential wells are electrons.

overlapping-gate charge-coupled device: A charge-coupled device formed so that adjacent transfer gates overlap and are insulated from one another.

p-channel charge-coupled device: A charge-coupled device fabricated so that the charges stored in the potential wells are holes.

peristaltic charge-coupled device: Synonym for "buried-channel charge-coupled device".

Schottky-barrier charge-coupled device: A buried-channel charge-coupled device that uses a Schottky barrier junction to isolate the transfer gate.

2.7 Terms and definitions applicable to charge-transfer devices (cont'd)

2.7.1 Types of charge-transfer devices (cont'd)

surface-channel charge-coupled device (SCCD): A charge-coupled device in which potential wells are created at the semiconductor-insulator interface and charge is transferred along that interface.

three-phase [four-phase] [multiphase] charge-coupled device: A charge-coupled device in which the direction of the charge packet flow is determined by the sequence of the three [four] [five or more] clock phases.

two-phase charge-coupled device: A charge-coupled device with asymmetrical potential wells that provide a unidirectional flow of charge packets under the control of two sequential clock phases.

2.7.2 General concepts of charge-transfer device

background charge: A synonym for “bias charge”, used mainly in imaging devices. (See Figure 2.7-1c.)

bias charge; circulating bias charge (for analog signal applications): A charge that defines the no-signal level. (See Figure 2.7-1b and Figure 2.7-1c.)

NOTE This charge is inserted into all potential wells electrically or by radiation.

buried channel: A transfer channel beneath the surface of a semiconductor.

charge packet: The portion of the total charge that is transferred from one position to the next position.

charge-regeneration stage (of a digital circuit): A region of a charge-transfer device that is used to refresh stored digital information.

empty zero; real zero: A condition in which there is no bias charge or low-level charge.

floating region; floating diffusion: A high-conductivity doped region without ohmic connection into or from which charge packets are transferred by overlapping or adjacent transfer gates.

NOTE A floating region can be used as the sense node for the charge signal in detection or regenerating circuits.

floating gate: A gate electrode that has no ohmic connection and is isolated from the semiconductor by an insulating layer or junction.

NOTE 1 The potential on the floating gate depends on the quantity of electrical charge stored in a potential well under the surface.

NOTE 2 Floating gates are typically used in signal detection or regeneration circuits.

2.7 Terms and definitions applicable to charge-transfer devices (cont'd)

2.7.2 General concepts of charge-transfer devices (cont'd)

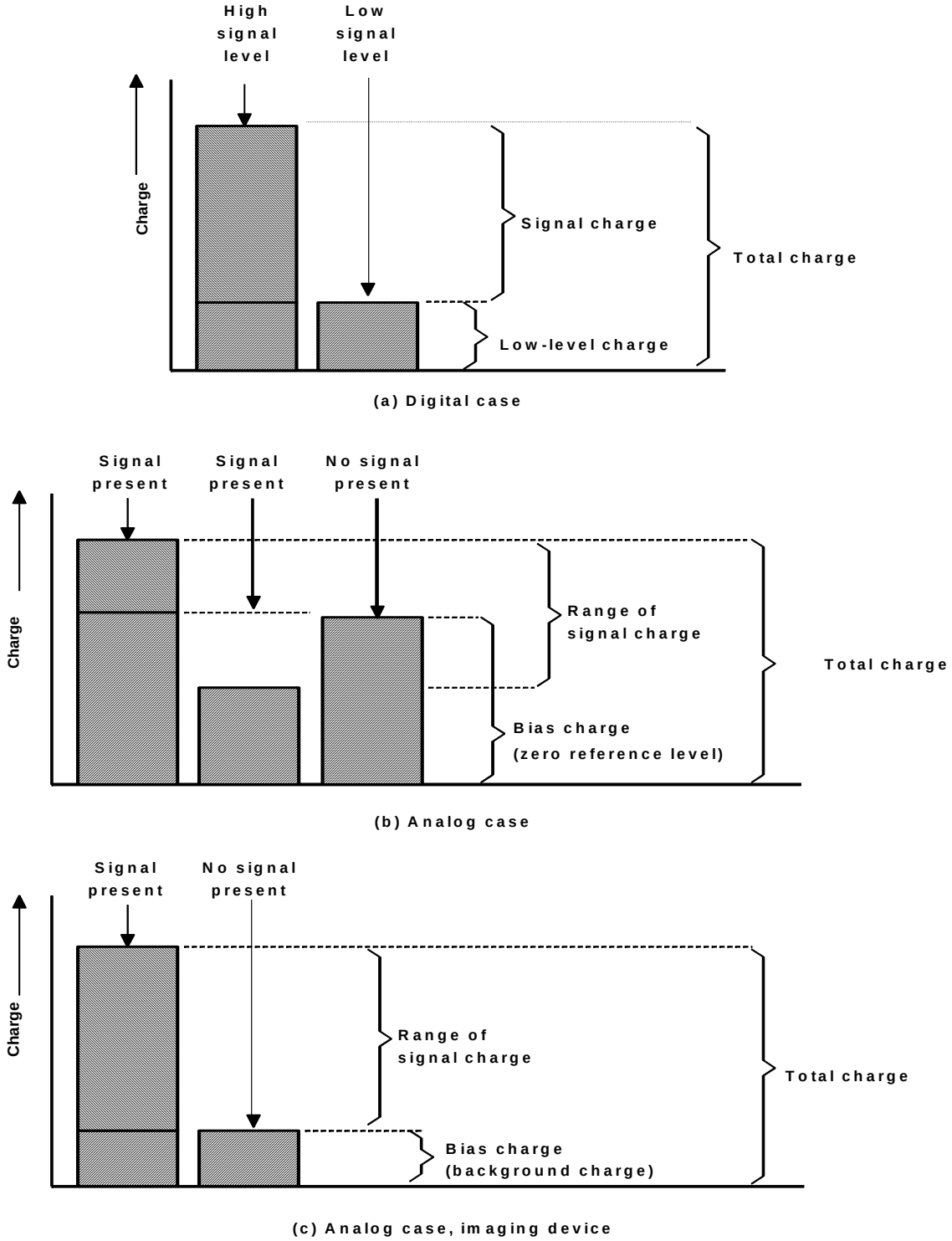


Figure 2.7-1 — Diagram illustrating CTD charge nomenclature

2.7 Terms and definitions applicable to charge-transfer devices (cont'd)

2.7.2 General concepts of charge-transfer devices (cont'd)

low-level charge (for digital signal applications): A charge that defines the low level of the digital signal. (See Figure 2.7-1a.)

NOTE 1 This charge is inserted into all potential wells, usually electrically but occasionally by radiation.

NOTE 2 The term “fat zero” has often been used but is deprecated.

potential well (of a charge-coupled device): The region around a local potential-energy minimum that is formed in the semiconductor of a charge-coupled device under control of the voltage applied to the transfer gate and confines any mobile charges that may be present.

signal charge: A quantity of electric charge representing the signal. (See Figure 2.7-1.)

storage gate: A gate electrode, isolated from the channel by an insulating layer or junction, to which voltage is applied in order to store charge.

surface channel: A transfer channel created at the semiconductor-insulator interface.

total charge (in a bucket-brigade device): The total electric charge stored in a potential well or in a discrete region of the device. (See Figure 2.7-1.)

transfer channel: The region of a charge-transfer device within which the charge flow is confined.

transfer gate: A gate electrode, isolated from the channel by an insulating layer or junction, to which voltage is applied in order to transfer charge.

2.7.3 Efficiencies, inefficiencies, and loss

average charge-transfer efficiency: The n^{th} root of overall charge-transfer efficiency, where n is the number of transfers.

charge-transfer efficiency (CTE) (η): The fraction of the signal charge that is transferred from one storage region to the next storage region.

charge-transfer inefficiency (CTI) (ε): The fraction of the signal charge that fails to be transferred from one storage region to the next storage region.

NOTE A synonym is “incomplete charge-transfer coefficient”.

2.7 Terms and definitions applicable to charge-transfer devices (cont'd)

2.7.3 Efficiencies, inefficiencies, and loss (cont'd)

charge-transfer loss (δ): The fractional loss of signal charge that occurs when a charge packet is transferred from one storage region to the next storage region and that packet is preceded by one or more packets of zero charge.

NOTE The loss of charge is that charge necessary to replenish all interface states or bulk traps that have emptied since the last passage of charge through the device. It is not charge that is left behind as it is in the case of charge-transfer inefficiency.

overall charge-transfer efficiency: The fraction of the input signal charge that is transferred as a packet to the output.

transfer inefficiency product ($n\varepsilon$): The product of the number of transfers (n) and the charge-transfer inefficiency (ε).

2.7.4 Input signals and dynamic range

charge-handling capacity; full-well capacity: The maximum amount of charge that can be stored in a potential well and transferred without overflow into adjacent wells.

dynamic range: The range of useful linear operation expressed as the ratio of the saturation input signal to the noise equivalent signal.

noise equivalent signal: The rms input signal or illumination power level needed to increase the output power to twice the value obtained with no input signal or illumination.

saturation input signal (for analog signal applications): The maximum input signal or illumination power that can be transferred with a specified degree of linearity.

saturation input signal (for digital signal applications): The input signal or illumination power that is required to produce full-well-capacity charge packets.

saturation output signal (for digital signal applications): The output signal that is produced by full-well-capacity charge packets.

2.7 Terms and definitions applicable to charge-transfer devices (cont'd)

2.7.5 Dark current (charge-coupled image sensors)

average dark current density (J_D): The average dark current per unit area within the active area of the device.

NOTE Depending on the type of device, the active area may be defined as either the area of transfer channel or the overall area including channel-defining regions. Other names used are “average leakage current density” and “average thermal generation current density”.

dark current (I_D): The output current under dark conditions.

dark current spike: A variation of the dark current that exceeds some specified level above the average value.

2.7.6 Transfer time

charge-transfer time: The time required to move a specified fraction of a charge packet from one storage region to the next.

Annex A (informative) Differences between JESD99C and JESD99-A

This table briefly describes most of the changes made to entries that appear in this standard, JESD99B, compared to its predecessors, JESD99B, (May 2007) and JESD99-A (May 2000). If the change to a concept involves any words added or deleted, it is included. Some spelling changes and punctuation changes are not included. Most package outline definitions have been deleted; these are now covered by JESD30.

A.1 Differences between JESD99C and JESD99B

Subclause	Term and description of change
1.1	Added the following terms and definitions: **component (general), device, solid-state (within the scope of JEDEC), solid-state circuit, solid-state component, solid-state device, solid-state drive, solid-state industry, solid-state memory, solid-state physics,** and **solid-state technology**
1.1	dice, dies: Added the alternative term "dies".
2.2.1	Added the following terms and definitions: **trigger pulse (general) and trigger pulse (in latch-up testing)**.

A.2 Differences between JESD99B and JESD99-A

Page	Term and description of change
1- 1	Deleted clause 1.1. It is replaced by the Index.
1- 1	Renumbered clause 1.2 as 1.1.
1- 1	**application-specific integrated circuit (ASIC):** New definition.
1- 1	**application-specific standard product (ASSP):** Added new term and definition.
1- 1	**array, logic (uncommitted logic array):** Moved as separate terms to new 1.2.
1- 1	**artwork:** Editorially shortened note.
1- 1	**assembly, microelectronic:** Editorially shortened note.
1- 3	**chip carrier**: Deleted abbreviation "**(CC)"**, deleted "low-profile" from definition, and replaced notes with the note from JESD30C.
1- 4	**circuit element:** Deleted "excluding interconnections" from definition. In notes, added inductors and interconnections as examples while still noting that definition in JESD12-1B excludes interconnections. This makes this definition consistent with the one for "circuit element, passive".
1- 4	**clock skew:** Made minor editorial changes.
1- 5	**customer-specific standard product (CSSP):** Added new term and definition.
1- 6	**custom integrated circuit:** Added new term and definition.
1- 6	**device, microelectronic:** Deleted. Was circular with "microcircuit" and not correct.
1- 9	**firing:** Added "including adherence to the substrate".
1- 9	**flatpack:** Deleted abbreviation "**(FP)"**, deleted "low-profile" from definition, and replaced notes with the note from JESD30C.
1-10	**functional test:** Made minor editorial changes.
1-10	**integrated circuit (IC):** Added "(Ref. IEC 748-1.)"
1-11	**integrated circuit, film (FIC):** Inserted word "exclusively" before "film elements".
1-11	**integrated circuit, hybrid (HIC):** Replaced definition with one from JESD93.
1-12	**integrated circuit, pad-limited:** Made minor editorial changes.
1-12	**integrated circuit, single-chip:** Replaced definition with one from JESD93.
1-13	**integrated circuit, very-high-speed (VHSIC):** Changed "goals of speed" to "goals for speed".
1-15	**metallization:** Replaced definition with one consistent with JESD33B.

Annex A Differences between JESD99C and JESD99-A (cont'd)

Page	Term and description of change
1-15	**metal-oxide-semiconductor (MOS) technology:** Corrected penultimate word in note from "insulation" to "insulator".
1-15	**microcircuit:** Added "(Ref. IEC 748-1.)"
1-16	**microelectronics:** Added "(Ref. IEC 748-1.)"
1-16	**optimization (of logic):** Qualified term and made editorial change.
1-17	**oxide, deposited:** Editorially rearranged the note as was done for JESD88B.
1-17	**oxide step:** Changed "an integrated circuit" to "a planar device".
1-17	**pinhole:** Replaced the definition with a similar one from J-STD-002B.
1-19	**semiconductor device** (general term)**:** Inserted phrase "in whole or in part" in definition. Deleted note 1. "NOTE 2" became "NOTE".
1-20	**space-charge region (of a semiconductor device):** Added "functional" as in JESD77B. Added new note 1. "NOTE" became "NOTE 2".
1-20	**standard product, (integrated circuit):** Added new term and definition.
1-23	Renumbered clause 1.3 as 1.2.
1-23	**array, logic:** Moved here from 1.1.
1-24	**gate array integrated circuit:** Changed "may" to "can".
1-24	**gate core area (of a cell-based integrated circuit):** Deleted "available", which had been inserted in error.
1-27	**programmable logic sequencer (PLS):** Inserted "an array of".
1-28	**uncommitted logic array:** Moved here from 1.1.
2- 3	**Secondary (quantity) symbols:** In the note, corrected "IEC 21-1" to "IEC 27-1".
2- 9	**characteristic:** Split into definitions (1) and (2),
2-10	**maximum limit:** In (2), added "s" to "temperature".
2-11	**thermal resistance, junction-to-ambient ($R_{\theta JA}$ or R_{thJA}):** Made minor editorial changes.
2-12	**thermal resistance, junction-to-case ($R_{\theta JC}$ or R_{thJC}):** Made minor editorial changes.
2-17	**source driver, (current-):** In note 2, corrected "sink drivers" to "source drivers".
2-18	**totem-pole output:** Two editorial changes in note 2.
2-19	**noise margin:** Added "maximum" before "voltage amplitude" and made other, editorial changes.
2-24	**hold time (t_h):** In note 1, inserted word "interval". In note 2, added comma after "negative value".
2-25	**setup time (t_{su}):** In note 1, inserted word "interval". In note 2, added comma after "negative value".
2-26	**skew (time), output ($t_{sk(o)}$):** Changed "two outputs" to "specified outputs"; deleted "switching in the same direction while", and deleted the figure reference and the note. These changes are in agreement with JESD65-A as it was recently amended.
2-26	**skew (time), output, high-to-low ($t_{sk(HL)}$)** and **skew (time), output, low-to-high ($t_{sk(LH)}$)**: Changed "The output skew time" to "The skew time", changed "with the outputs" to "between specified outputs of a single logic device", and added "while driving identical loads", the figure reference, and the note.
2-27	**Figure 2.3-1:** The applicability of the first four equations has been changed to agree with the modified definitions.
2-28	**quiescent voltage:** Changed "through" to "at".
2-31	**maximum output voltage swing (V_{OM}):** Inserted "waveform" before "clipping".
2-32	**maximum output current swing (I_{OM}):** Inserted "waveform" before "clipping".
2-32	**input impedance, common-mode (z_{ic}):** Changed "Generally the parallel sum" to "The parallel equivalent".

Annex A (informative) Differences between JESD99B and JESD99A (cont'd)

Page	Term and description of change
2-32	**input impedance, single-ended (z_{is}):** Hyphenated "ac-grounded".
2-32	**output impedance, single-ended (z_{os}):** Hyphenated "ac-grounded".
2-32	**output resistance (r_o):** Deleted "parallel equivalent".
2-34	**noise temperature (T_n):** Made minor editorial changes.
2-35	**buffer:** Made minor editorial changes to harmonize wording in JESD99A and JESD100B.
2-35	**bus driver:** Hyphenated "fan-out".
2-36	**analog-to-digital processor:** Made 2nd sentence a note.
2-37	**conversion code** (1) **(of an ADC):** Split definitions for ADC and DAC codes.
2-40	**full-scale range, nominal (of a linear ADC** or **DAC) (V_{FSRnom}** or **I_{FSRnom}):** Added "up" after "rounded".
2-40	**full-scale range, (practical) (of a linear ADC** or **DAC) (V_{FSR}** or **I_{FSR}) (V_{FSRpr}** or **I_{FSRpr}):** In note 2, corrected symbol "I_{FSRpr}".
2-44	**nonlinear ADC [DAC]:** Made minor editorial changes.
2-44	**offset point (of an adjustable ADC [DAC]):** Made minor editorial change.
2-47	**temperature coefficients of analog characteristics (α):** Made editorial change in the note.
2-48	**conversion rate (of an externally controlled ADC) (f_c):** Made editorial change in note 3.
2-49	**glitch (of a DAC):** Made minor editorial change.
2-52	**full-scale error (of a linear ADC [DAC]) (E_{FS}):** Made minor editorial changes.
2-57	**total error; absolute accuracy error (of a linear ADC) (E_T):** Added 2nd term "**absolute accuracy error**" and "or 'total error'" at the end of note 1.
2-57	**total error; absolute accuracy error (of a linear DAC) (E_T):** Added 2nd term "**absolute accuracy error**" and "or 'total error'" at the end of note 1.
2-61	**peristaltic charge-coupled device:** Added item. Was in note to BCCD.
2-64	**storage gate** and **transfer gate:** Editorially rearranged.
2-64	**total charge (in a bucket-brigade device):** Rearranged to move "bucket brigade" from definition to qualifier of the term.

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Standard Improvement Form **JEDEC JESD99C**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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