JEDEC STANDARD

Transient Voltage Suppressor Standard for Thyristor Surge Protective Device Rating Verification and Characteristic Testing

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ELECTRONIC INDUSTRIES ALLIANCE

JEDEC Solid State Technology Association

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TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE RATING VERIFICATION AND CHARACTERISTIC TESTING

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Foreword

This standard was prepared by JEDEC JC-22.5 Committee on Transient Voltage Suppressors. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages.

Major contributions to the content of this standard come from recent work by the ANSI/IEEE in PC62.37, 1996 Standard Test Specification For Thyristor Diode Surge-Protective Devices, and from the JC-10 Committee in-process work on revisions to Standard No. 77, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices, Section 7 - Transient Voltage Suppressors; Surge Protective Devices. Similar standards are presently being developed by the IEC.

This standard conforms with the work of other groups. However, work on this standard, and the others in-process has not progressed to the point where an exact and complete comparison of documents can be made.

TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE RATING VERIFICATION AND CHARACTERISTIC TESTING

(From JEDEC Board Ballot JCB-97-81, formulated under the cognizance of the JC-22.5 Committee on Transient Voltage Suppressors.)

1 Introduction

The Thyristor Surge Protective Device (TSPD) is a semiconductor device that is recently finding widespread application in the telecommunications industry. The intent of this standard is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangability. This publication is not intended to preclude or discourage other approaches that similarly represent good engineering practice, or that may be acceptable to, or have been accepted by, appropriate bodies. Parties who wish to bring other approaches to the attention of the formulating committee to be considered for inclusion in future revisions of this publication are encouraged to do so. It is the intention of the formulating committee to revise and update this publication from time to time as may be occasioned by changes in technology, industry practice, or government regulations, or for other appropriate reasons.

2 Scope

This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics.

3 Device definitions

3.1 Thyristor surge protective device (TSPD)

A thyristor, designed for transient voltage suppression in telecommunication, data line, and similar applications. They limit voltage transients by conducting surge currents. It returns to a blocking state when the current decays below a critical value.

NOTE — The device is also known as a thyristor surge suppressor (TSS).

3.1.1 Off state of a TSPD

The state of a TSPD, in a quadrant in which switching can occur, that corresponds to the high dynamic-resistance portion of the characteristic between the origin and the beginning of the breakdown region.

3.1 Thyristor surge protective device (TSPD) (cont'd)

3.1.2 Breakdown region of a TSPD

The portion of the characteristic that starts with the transition from the high dynamic resistance off state to a substantially lower dynamic resistance and extends to the switching point.

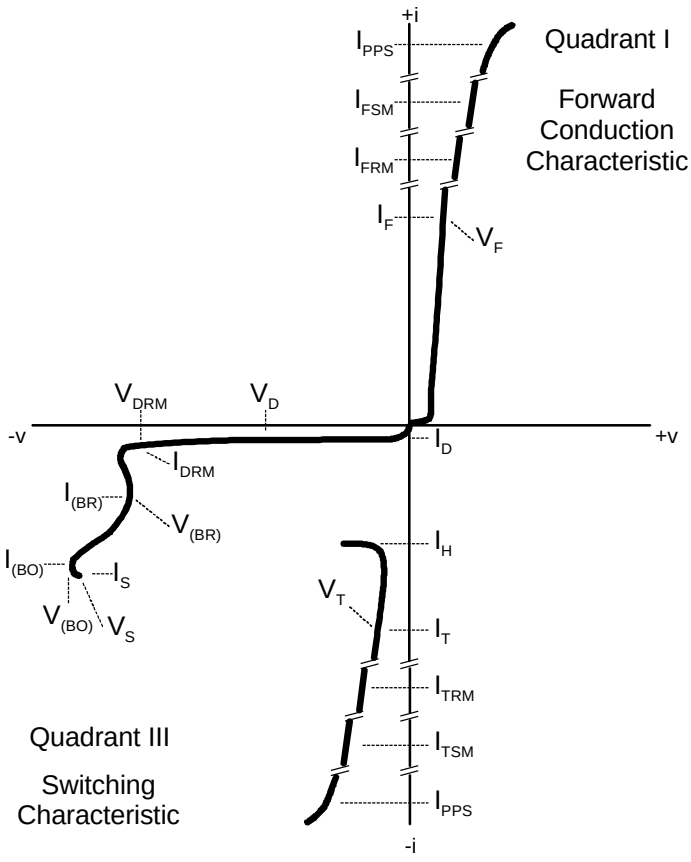


Figure 1 — Symbols and terms for a forward-conducting positive-breakdown-resistance TSPD

3.1.3 On state of a TSPD

The condition of the TSPD corresponding to the low-resistance low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

3.2 Classes of thyristor surge protective devices

3.2.1 Forward-conducting diode TSPD

A two-terminal internally triggered TSPD that switches only for negative cathode voltage and conducts large currents at positive cathode voltages comparable in magnitude to the on-state voltage (see figures 1 and 2).

NOTES

1 In conventional SCR thyristor terminology, where the voltage is applied to the anode, this device would be called a reverse-conducting diode thyristor.

2 When the TSPD cathode is positive, the device characteristics are similar to those of a forward-biased diode.

3 When the TSPD cathode is negative, the device characteristics are similar to those of a breakover-triggered SCR thyristor.

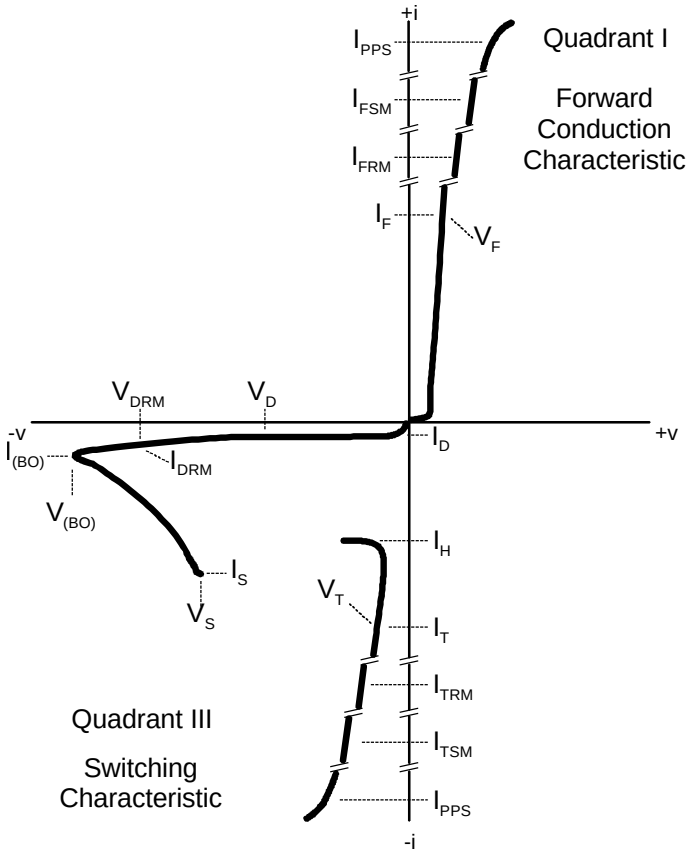


Figure 2 — Symbols and terms for a forward-conducting negative-breakdown-resistance TSPD

3.2 Classes of thyristor surge protective devices (cont'd)

3.2.2 Forward-conducting triode TSPD

A three-terminal TSPD that switches only for negative cathode voltage and conducts large currents at positive cathode voltages comparable in magnitude to the on-state voltage. Figure 3 shows the characteristic applicable to the switching quadrant of gated devices.

NOTES

1 In conventional SCR thyristor terminology, where the cathode is the common terminal, this device would be called a reverse-conducting triode thyristor.

2 Application of an appropriate fixed gate voltage allows switching to take place at voltages below the intrinsic breakover value.

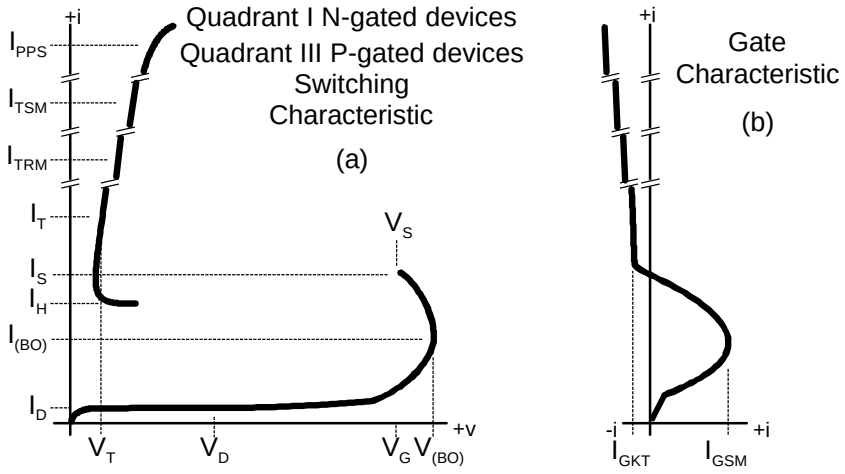


Figure 3 — Symbols and terms for a gated TSPD

3.2.3 Reverse-blocking diode TSPD

A two-terminal TSPD that exhibits a blocking state for positive cathode voltage. Figures 4 and 5 illustrate the device characteristic.

3.2 Classes of thyristor surge protective devices (cont'd)

3.2.4 Reverse-blocking triode TSPD

A three-terminal (gated) TSPD that exhibits a blocking state for positive cathode voltage. Figures 4 and 5 illustrate the device characteristic in quadrant three only.

3.2.5 Bidirectional TSPD

A TSPD having switching characteristics in the first and third quadrants. Figures 6 and 7 show the characteristic for this type device.

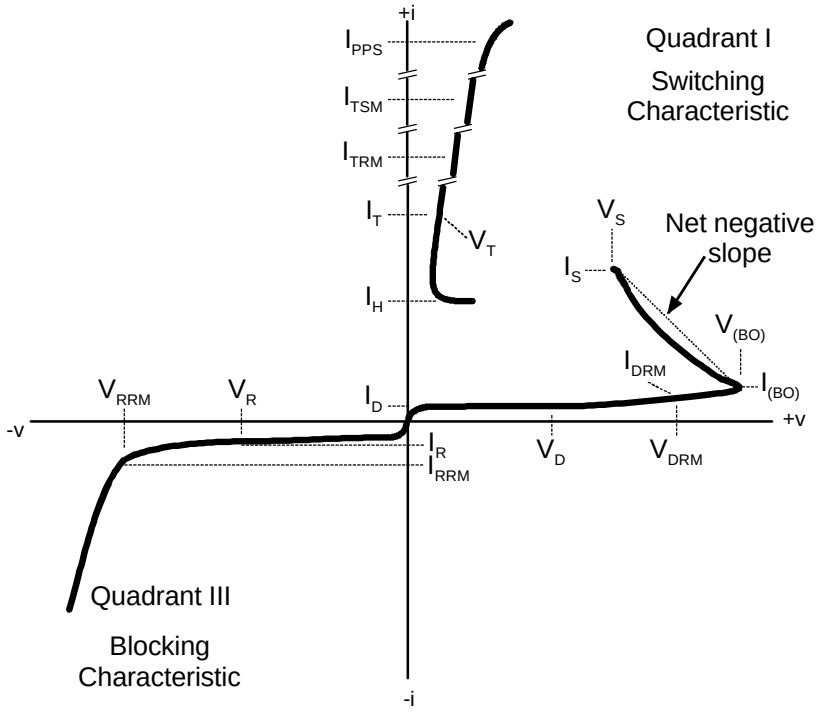


Figure 4 — Symbols and terms for a reverse-blocking negative-breakdown-resistance TSPD

3.2.6 Unidirectional TSPD

A TSPD that can switch in only one quadrant.

NOTE — There are two types: forward-conducting TSPDs and reverse-blocking TSPDs.

3.2.7 Negative-breakdown-resistance TSPD

A TSPD whose static characteristic has a negative-resistance slope between the breakover point ($V_{(BO)}$, $I_{(BO)}$) and a higher-current, lower-voltage point (V_S,I_S) at which switching occurs. Any of the device types described in 3.2.1 – 3.2.6 can have negative-breakdown resistance in the quadrants where switching occurs. Figures 2, 4, and 6 show devices with negative-breakdown resistance.

3.2 Classes of thyristor surge protective devices (cont'd)

3.2.8 Positive-breakdown-resistance TSPD

A TSPD whose static characteristic has a positive-resistance slope between the breakover point ($V_{(BR)}$, $I_{(BR)}$) and a higher-current, higher-voltage point (V_S, I_S) at which switching occurs. Any of the device types described in 3.2.1 – 3.2.6 can have positive-breakdown resistance in the quadrants where switching occurs. Figures 1, 3, 5, and 7 show devices with positive-breakdown resistance.

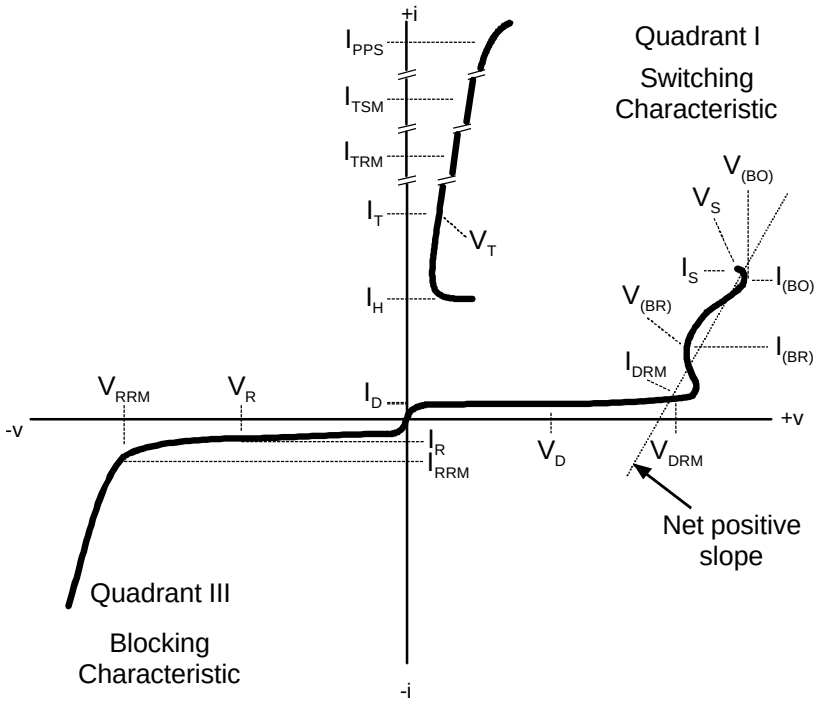


Figure 5 — Symbols and terms for a reverse-blocking positive-breakdown-resistance TSPD

3.3 Definitions of characteristic, rating, and parameter

The following definitions are offered to aid the reader in understanding the terms presented.

3.3.1 Characteristic

A characteristic is an inherent and measurable property of a device. It can be expressed as a value for stated or recognized conditions. A characteristic also may be a set of related values, usually shown in graphical form.

3.3.2 Rating

A rating is a value establishing either a limiting capability or limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may either be maxima or minima.

3.3 Definitions of characteristic, rating, and parameter (cont'd)

3.3.3 Parameter

A device descriptor that is measurable or quantifiable such as a device characteristic or rating.

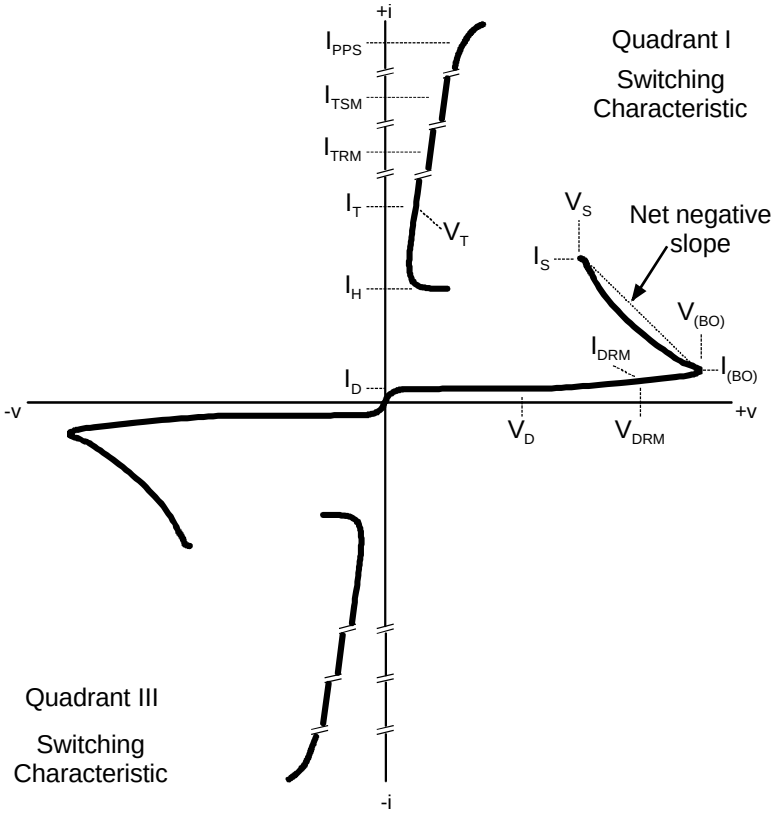


Figure 6 — Bidirectional negative-breakdown-resistance TSPD

3.4 Thyristor surge protective device parameters

The manufacturer establishes the values of device parameters according to statistical acceptance criteria. The specified tests are performed at nominal 25 °C ambient temperature unless otherwise stated. If the volt-ampere characteristics are asymmetrical, the characteristic values shall be specified for each (V,I) graph as illustrated in figures 1 – 7.

For the method of defining impulse waveforms, see figures 11 and 12 of this standard. For voltage waves with wavefront duration less than 30 µs, the virtual duration of the impulse wavefront is 1.67 times the time for the voltage to increase from 30% to 90% of its crest value. For voltage waves with wavefront duration of 30 µs or more, it is the time taken by the voltage to increase from actual zero to maximum crest value. For current waves, the virtual wavefront duration is 1.25 times the time for the current to increase from 10% to 90% of crest value.

The ac power frequency is the operating frequency of the ac power distribution system, which is often 50 or 60 Hz but can range up to 420 Hz.

3.4 Thyristor surge protective device parameters (cont'd)

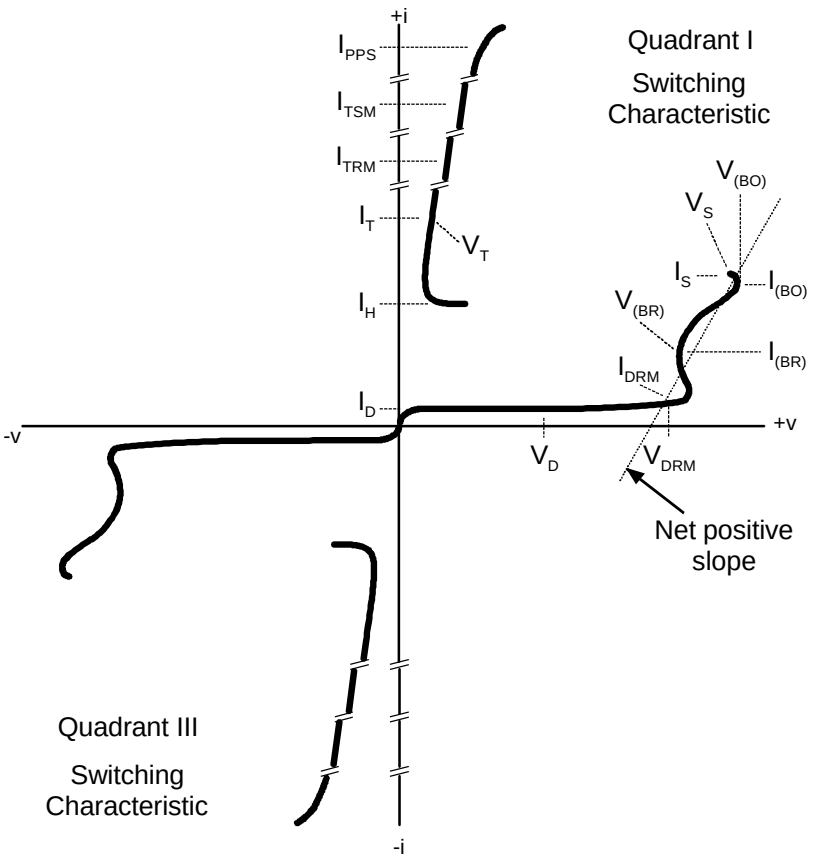


Figure 7 — Symbols and terms for a bidirectional positive-breakdown-resistance TSPD

3.4.1 Electrical parameters applicable to all device types

The parameters described in table 1 apply to all TSPDs (regardless of whether they are bidirectional, unidirectional, symmetrical, asymmetrical, reverse blocking, forward conducting, or any permutation or combination of the former) in their switching quadrant or quadrants.

3.4 Thyristor surge protective device parameters (cont'd)

3.4.1 Electrical parameters applicable to all device types (cont'd)

Table 1 — Electrical parameters applicable to all TSPDs

Term and description	Symbol	Reference
(1) Off-State Voltage. The principal voltage when the thyristor is in the off state.	V_D	Fig. 1 -7
(2) Off-State Current. The principal current when the thyristor is in the off state.	I_D	Fig. 1 -7
(3) Repetitive Peak Off-State Voltage. The highest instantaneous value of the off-state voltage, including all repetitive transient voltages but excluding all nonrepetitve transient voltages.	V_{DRM}	Fig. 1 and 2, 47
(4) Maximum Off-State Current. The maximum (peak) instantaneous value of the off-state current that results from the application of repetitive peak off-state voltage.	I_{DRM}	Fig. 1 and 2, 47
(5) Breakover Voltage. The maximum voltage in the breakdown region.	$V_{(BO)}$	Fig. 1 -7
(6) Breakover Current. The principal current at the thyristor breakover voltage.	$I_{(BO)}$	Fig. 1 -7
(7) On-State Voltage. The principal voltage when the thyristor is in the on state.	V_T	Fig. 1 -7
(8) On-State Current. The principal current when the thyristor is in the on state.	I_T	Fig. 1 -7
(9) Repetitive Peak On-State Current. Rated maximum (peak) value of on-state current of specified waveshape and frequency which may be applied continuously.	I_{TRM}	Fig. 1 -7
(10) Nonrepetitive Peak On-State Current. The maximum (peak) value of on-state surge current of specified waveform, frequency, and duration or number of cycles.	I_{TSM}	Fig. 1 -7
(11) Nonrepetitive Peak Pulse Current. Rated maximum value of peak impulse pulse current of specified amplitude and waveform.	I_{PPS}	Fig. 1 -7
(12) Holding Current. The minimum, principal, or thyristor current that will maintain the thyristor in the on state.	I_H	Fig. 1 -7
(13) Off-State Capacitance. The capacitance in the off state.	C_O	
(14) Critical Rate of Rise of Off-State Voltage. The maximum rate of rise of voltage (less than or equal to V_{DRM}) that will not cause switching from the off state to the on state.	dv/dt	Fig. 39 -40
(15) Critical Rate of Rise of On-State Current. Rated value of the rate of rise of current which the device can withstand without damage.	di/dt	Fig. 45

3.4 Thyristor surge protective device parameters (cont'd)

3.4.1 Electrical parameters applicable to all device types (cont'd)

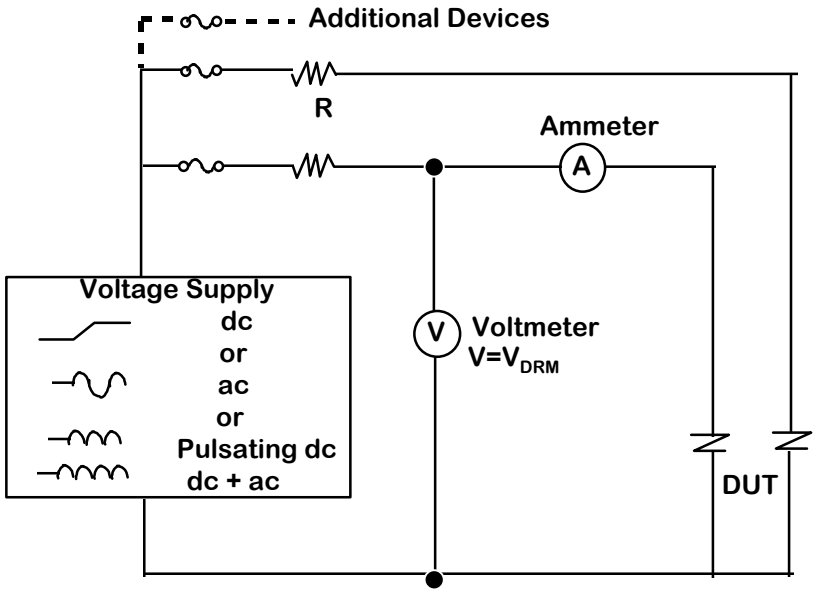


Figure 8 — Maximum repetitive off-state voltage (V_{DRM}) test circuit

3.4.2 Thermal parameters applicable to all device types

TSPD parameters often depend on temperature. Different temperatures may arise as a result of ambient conditions or because of power dissipation in the TSPD. Table 2 gives common parameters useful for thermal characterization of all TSPDs.

3.4 Thyristor surge protective device parameters (cont'd)

3.4.2 Thermal parameters applicable to all device types (cont'd)

Table 2 — TSPD thermal parameters

Term and description	Symbol	Unit
(1) Thermal Resistance. The effective temperature rise per unit power dissipation of a designated junction, above the temperature of a stated external reference point (lead,case, or ambient) under conditions of thermal equilibrium.	$R_{\theta JL}$ $R_{\theta JC}$ $R_{\theta JA}$	°C/W (K/W)
(2) Transient Thermal Impedance. The change in the difference between the virtual junction temperature and the temperature of a specified reference point or region (lead, case, or ambient) at the end of a time interval, divided by the step function change in power dissipation during the same time interval which causes the change of temperature difference. NOTE — It is the thermal impedance of the junction under conditions of changing time, and is generally given in the form of a curve as a function of the duration of an applied pulse.	$Z_{\theta JL(t)}$ $Z_{\theta JC(t)}$ $Z_{\theta JA(t)}$	°C/W (K/W)
(3) Temperature Coefficient of Breakdown Voltage. The ratio of the change in breakdown voltage, ($V_{(BR)}$) to changes in temperature expressed as either millivolts per °C or percent per °C with reference to the 25 °C value of breakdown voltage.	$\alpha_{V(BR)}$ $dV_{(BR)}/dT_J$	mV/°C or %/°C (mV/K or %/K)
(4) Variation of Holding Current with Temperature. The change in holding current, I_H, with changes in temperature. It is shown as a graph of I_H versus T_J.		
(5) Temperature Derating. Derating with temperature above a specified base temperature, expressed as a percentage per degree C, may be applied to surge or operating current parameters.		%/°C %/K

3.4 Thyristor surge protective device parameters (cont'd)

3.4.2 Thermal parameters applicable to all device types (cont'd)

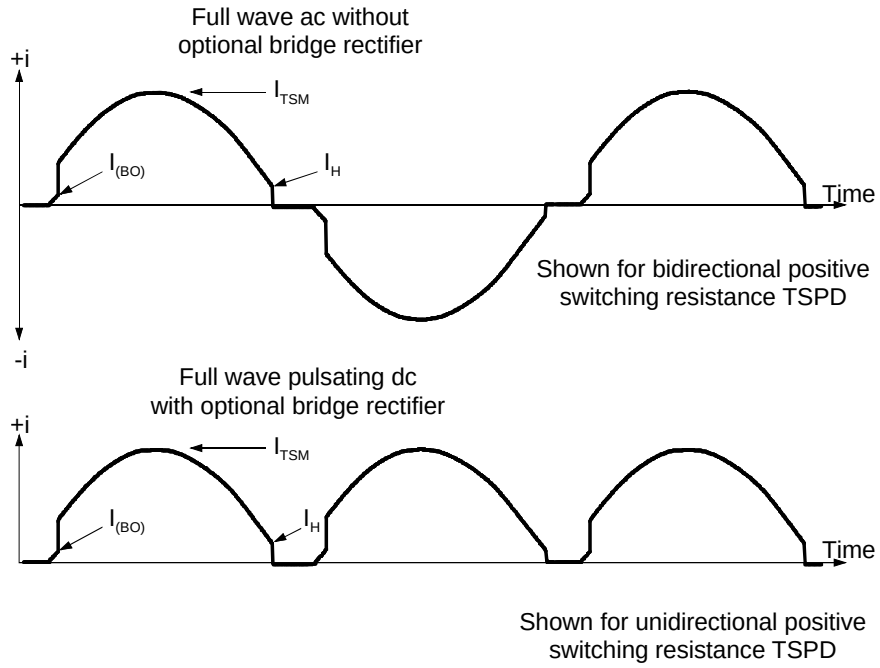


Figure 9 — Example of current wave, I_{TSM} test

3.4.3 Additional electrical parameters for positive-breakdown-resistance types

Table 3 gives parameters applicable to the switching quadrant or quadrants of positive-breakdown-resistance TSPDs.

NOTE — The switching voltage and current are useful only when the coordinate (V_S, I_S) is substantially different from ($V_{(BO)}$, $I_{(BO)}$) as in some negative-breakdown-resistance types. When (V_S, I_S) is coincident with ($V_{(BO)}$, $I_{(BO)}$), or not significantly different, the latter shall be used to describe the device characteristic.

Table 3 — Electrical parameters for positive-breakdown-resistance TSPDs

Term and parameter description	Symbol	Reference
(1) Breakdown Voltage. The voltage across the device in the breakdown region.	$V_{(BR)}$	Fig. 1, 5, and 7
(2) Breakdown Current. The anode, principal, or thyristor current at the breakdown voltage.	$I_{(BR)}$	Fig. 1, 5, and 7
(3) Switching Voltage. The instantaneous principal voltage at the highest current point in the breakdown region prior to switching to the on state.	V_S	Fig. 1 – 7
(4) Switching Current. The instantaneous principal current at which the thyristor begins to switch from the breakdown region to the on state.	I_S	Fig. 1 – 7

3.4 Thyristor surge protective device parameters (cont'd)

3.4.3 Additional electrical parameters for positive-breakdown-resistance types (cont'd)

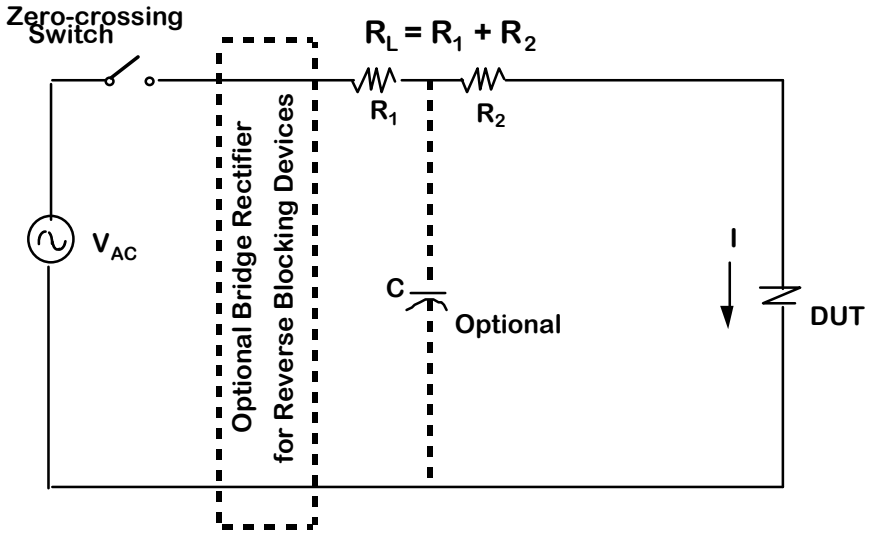


Figure 10 — Nonrepetitive peak on-state surge current (I_{TSM}) test

3.4.4 Additional parameters for negative-breakdown-resistance types

Table 4 gives electrical parameters applicable to the switching quadrant or quadrants of negative-breakdown-resistance TSPDs.

NOTE — These devices have a switching voltage much lower than their breakover voltage and a switching current much greater than their breakover current. They exhibit switchback in their volt-ampere characteristic which is observable on a curve tracer but is often difficult to measure. Specification of (V_S, I_S) is optional.

Table 4 — Electrical parameters for negative-breakdown-resistance TSPDs

Term and parameter description	Symbol	Reference
(1) Switching Voltage. The voltage at the high-current termination of the breakdown region prior to switching to the on state.	V_S	Fig. 1 - 7
(2) Switching Current. The current at the high-current termination of the breakdown region prior to switching to the on state.	I_S	Fig. 1 - 7
(3) Switching Resistance. The quotient of (a) the difference between the breakover voltage and the switching voltage and (b) the difference between the breakover current and the switching current. $R_S = (V_{(BO)} - V_S)/(I_{(BO)} - I_S)$	R_S	Fig. 2, 4, and 6

3.4 Thyristor surge protective device parameters (cont'd)

3.4.4 Additional parameters for negative-breakdown-resistance types (cont'd)

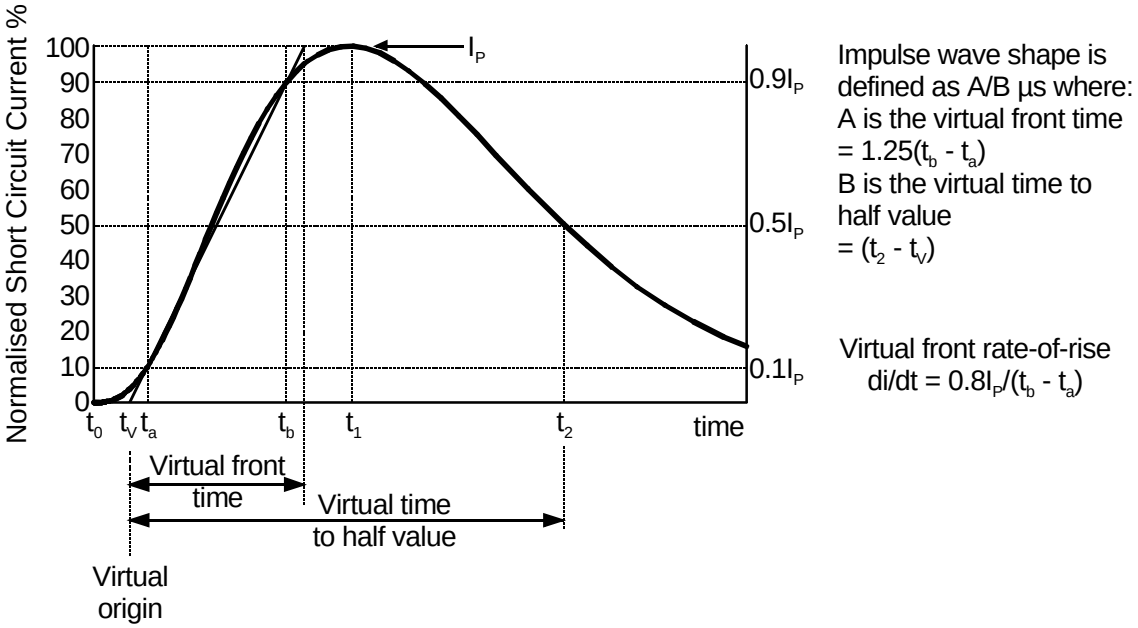


Figure 11 — Definition of double exponential impulse current waveshape

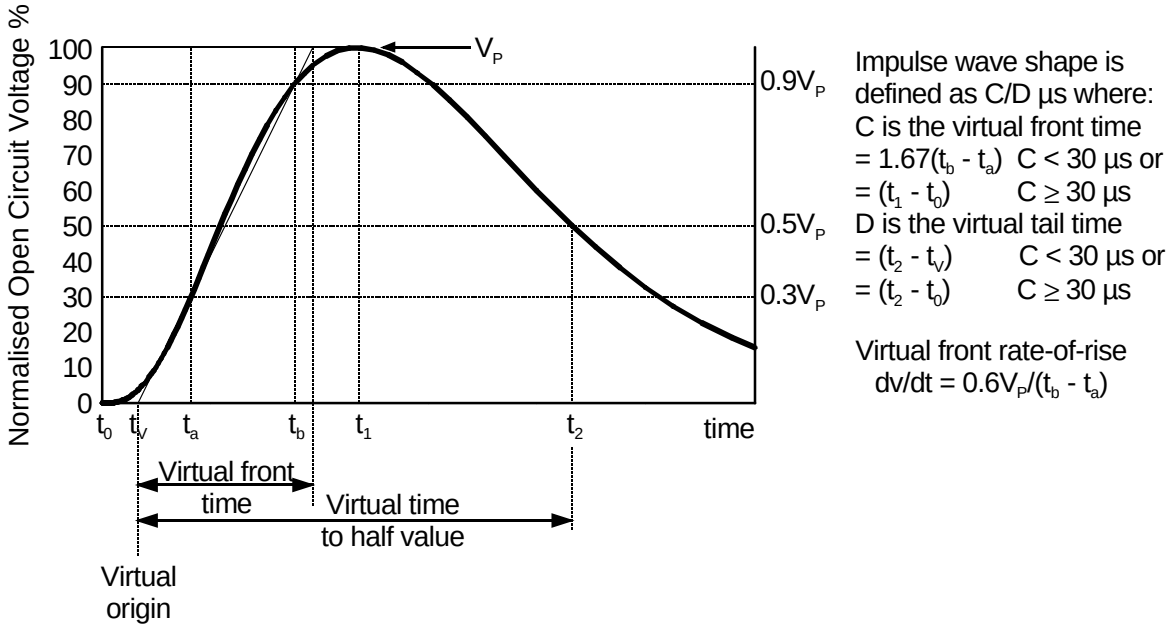


Figure 12 — Definition of double exponential impulse voltage waveshape

3.4 Thyristor surge protective device parameters (cont'd)

3.4.5 Additional parameters for reverse-blocking types

The definitions in table 5 apply in the quadrant where switching does not occur.

Table 5 — Reverse-blocking TSPD parameters

Term and parameter description	Symbol	Reference
(1) Reverse Voltage. The principal voltage when the thyristor is in the reverse-blocking state.	V_R	Fig. 4 and 5
(2) Repetitive Peak Reverse Voltage. The highest instantaneous value of the reverse voltage, including all repetitive transient voltages but excluding all nonrepetitive transient voltages.	V_{RRM}	Fig. 4 and 5
(3) Repetitive Peak Reverse Current. The maximum (peak) value of reverse current that results from the application of the repetitive peak reverse voltage, V_{RRM}.	I_{RRM}	Fig. 4 and 5

3.4.6 Additional parameters for forward-conducting types

The definitions in table 6 are for the operating quadrant with a forward-biased characteristic similar to a diode.

Table 6 — Parameters for forward-conducting TSPDs

Term and Parameter Description	Symbol	Reference
(1) Nonrepetitive Peak Forward Current. Rated maximum (peak) value of ac power frequency forward surge current of specified waveform and frequency that may be applied for a specified time or number of ac cycles.	I_{FSM}	Fig. 1 and 2
(2) Forward Voltage (of a forward-conducting TSPD). A positive cathode-to-anode thyristor voltage at a forward current. NOTE — This is the polarity that forward-biases the antiparallel diode.	V_F	Fig. 1 and 2
(3) Forward Current (of a forward-conducting TSPD). A principal current through the device resulting in a positive cathode-to-anode (thyristor) voltage. NOTE — This is the voltage polarity that forward-biases the antiparallel diode.	I_F	Fig. 1 and 2
(4) Repetitive Peak Forward Current. Rated maximum (peak) value of ac power frequency forward current of specified waveshape and frequency that may be applied continuously.	I_{FRM}	Fig. 1 and 2
(5) Peak Forward Recovery Voltage. The maximum (peak) valueof forward conduction voltage across the device upon the application of a specified voltage and current rate of rise following a zero or specified reverse-voltage condition.	V_{FRM}	Fig. 1 and 2

3.4 Thyristor surge protective device parameters (cont'd)

3.4.6 Additional parameters for forward-conducting types (cont'd)

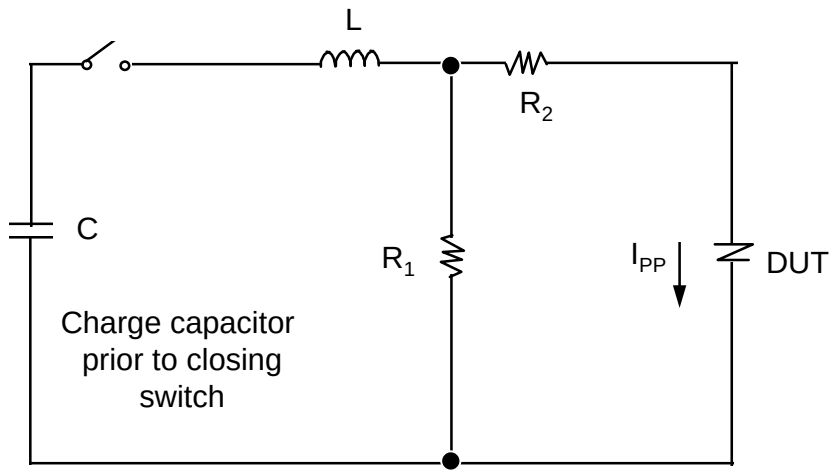


Figure 13 — Measurement of impulse $V_{(BO)}$, $I_{(BO)}$, and I_{PPS}: Example of a pulse forming network

3.4.7 Additional parameters for triode, gate accessible device types

These devices have a gate terminal that controls the switching region characteristics. The main terminals provide the TSPD function. Two gate types are possible, as the additional terminal is connected to either an intermediate p or n layer of the thyristor. The first is a p-gate device, which has the gate biased negatively with respect to the anode. The p-gate device provides negative transient voltage protection with respect to the anode. The second is an n-gate device, which has the gate biased positively with respect to the cathode. The n-gate device provides positive transient voltage protection with respect to the cathode. Table 7 gives the additional electrical parameters required to describe these devices.

3.4 Thyristor surge protective device parameters (cont'd)

3.4.7 Additional parameters for triode, gate accessible device types (cont'd)

Table 7 — Additional parameters for gated TSPDs

Term and parameter description	Symbol	Reference
(1) Gate-to-Adjacent Terminal Peak Off-State Voltage. The maximum (peak) gate voltage that may be applied such that a specified off-state current, I_D, is not exceeded.	V_{GDM}	Fig. 3
(2) Peak Off-State Gate Current. The maximum gate current that results from the application of the peak off-state gate voltage, V_{GDM}	I_{GDM}	Fig. 3
(3) Gate Reverse Current, Adjacent Terminal Open. The current through the gate terminal when a specified gate bias voltage V_G, is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is open-circuited.	I_{GAO} p-gate I_{GKO} n-gate	Fig. 3
(4) Gate Reverse Current, Main Terminals Short-Circuited. The current through the gate terminal when a specified gate bias voltage, V_G, is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is short-circuited to the third.	I_{GAS} p-gate I_{GKS} n-gate	Fig. 3
(5) Gate Reverse Current, On-State. The current through the gate terminal when a specified gate bias voltage V_G, is applied and a specified on-state current, I_T, is flowing.	I_{GAT} p-gate I_{GKT} n-gate	Fig. 3
(6) Gate Reverse Current, Forward-Conducting State. The current through the gate terminal when a specified gate bias voltage, V_G, is applied and a specified forward conduction current, I_F, is flowing.	I_{GAF} p-gate I_{GKF} n-gate	Fig. 3
(7) Gate-Switching Charge. The charge through the gate terminal, under impulse conditions, during the transition from the off state to the switching point, when a specified gate bias voltage, V_G, is applied.	Q_{GS}	Fig. 27 – 28
(8) Peak Gate-Switching Current. The maximum value of current through the gate terminal during the transition from the off state to switching point, when a specified gate bias voltage, V_G, is applied.	I_{GSM}	Fig. 3, 27, 28
(9) Gate-to-Adjacent Terminal Breakover Voltage. The gate to cathode voltage for a p-type device or gate to anode voltage for an n-gate device at the breakover point. This is equivalent to the voltage difference between the breakover voltage, $V_{(BO)}$, and the specified gate voltage, V_G.	$V_{GK(BO)}$ p-gate $V_{GA(BO)}$ n-gate	Fig. 27 – 28

3.4 Thyristor surge protective device parameters (cont'd)

3.4.7 Additional parameters for triode, gate accessible device types (cont'd)

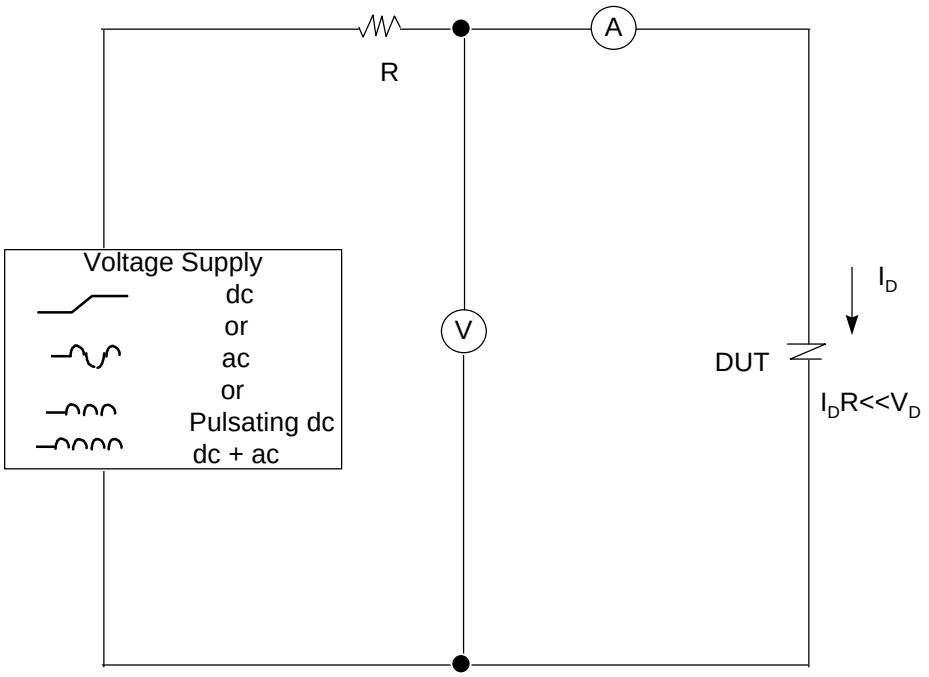


Figure 14 — Off-state current test circuit

3.4.8 Common telecommunications impulse waveshape definitions

Standards for a variety of impulse waveshapes exist. Table 8 and figures 11 and 12 show common definitions. In this table, the first number gives the virtual front time, and the second the duration. It may be desirable to test more than one waveshape because of the application, and thermal or dynamic parameters of the DUT. The introduction of external series resistance, as required by some standards and applications to attenuate the wave, could alter the parameters of the short-circuit current waveform.

Note that device impedance and switching will alter voltage waveform across it, and the current wave through it, from the open-circuit and short-circuited values.

Table 8 — Common impulse waveshape definitions

Open-circuit voltage waveshape (C/B µs)	Short-circuit current waveshape (A/B µs)
2/10	2/10
1.2/50	8/20
10/160	10/160
10/560	10/560
10/700	5/310
10/1000	10/1000

4 Rating verification tests

This section describes standard test methods for verifying the maximum ratings of TSPDs. Operating beyond the maximum rating can result in excessive off-state current, device damage, or higher than normal voltages across the protected circuit such as can arise from thermal coefficients, device impedances, and open-circuit failure.

NOTE— Accurate reproduction of the test conditions can require dangerous high voltages and currents. Proper safety practices, including good contact to the unit under test, shields, and interlocks, should be employed to reduce shock and burn hazards.

4.1 Maximum repetitive off-state voltage (V_{DRM})

4.1.1 Introduction (V_{DRM})

This test verifies that the TSPD can continuously block rated voltage at its maximum or minimum rated temperature without degradation of the device such as excessive off-state current. The TSPD must not turn on under the influence of typical operating voltages present in the protected circuit. It must not load the protected circuit with excessive off-state current.

4.1.2 Test Method (V_{DRM})

The device is connected across a voltage source and the resulting off-state current measured. The applied voltage shall be gradually and carefully increased to the specified V_{DRM} value to prevent voltage overshoot or dv/dt triggering of the device under test. The abrupt application of voltage can result in currents exceeding the specified I_{DRM} and damage to the device under test (DUT).

V_{DRM} must be less than the lowest breakdown or breakover voltage (whichever is applicable to the device type) at any temperature within the specified operating junction temperature range. Devices with a positive $V_{(BR)}$ or $V_{(BO)}$ temperature coefficient will have their lowest voltage at minimum operating junction temperature.

Figure 8 gives the simplified schematic. The resistor "R" is optional. It prevents possible damage to the device and the ammeter by surge current. It also prevents a failing device from shorting the power supply and removing the voltage to other devices using the same supply. The resistor shall be selected to have a voltage drop much lower than V_{DRM} when I_{DRM} flows through it. Device off-state current can be monitored by measuring the voltage drop across R when the voltmeter is removed.

Elevated temperatures provide the maximum stress on the device and are recommended for life testing. Power loss and off-state current depend on the junction temperature. A heatsink may be required to control the case and resulting junction temperature. The voltage shall remain applied as the device cools following completion of the test. This prevents thermal disturbances from annealing out possible polarization resulting from the test. The test duration shall be long enough to establish the desired confidence in device reliability.

4.1 Maximum repetitive off-state voltage (V_{DRM}) (cont'd)

4.1.2 Test Method (V_{DRM}) (cont'd)

(1) Test conditions to be specified (V_{DRM})

A dc test source provides the greatest stress on the device. Bidirectional devices require two dc tests, one for each polarity. Alternatively, an ac test, or combined ac and dc, appropriate for the device type (reverse-blocking, forward-conducting, etc.), may be specified.

NOTE — Choose item (a), (b), (c), or (d). Items (e) and (f) are mandatory. Item (g) applies only to gated devices.

(a) DC bias

dc voltage=V_{DRM} _____ V

(b) Full-wave ac bias

Peak voltage = V_{DRM} _____ V

Frequency (f) _____ Hz

(c) Full-wave pulsating dc

Peak voltage = V_{DRM} _____ V

Frequency (f) _____ Hz

(d) AC with dc component

Peak positive voltage _____ V

Peak negative voltage _____ V

Frequency (f) _____ Hz

(e) Junction temperature (T_J) _____ °C

(f) Test duration _____ hours

4.1 Maximum repetitive off-state voltage (V_{DRM}) (cont'd)

4.1.2 Test Method (V_{DRM}) (cont'd)

parameters applicable only to triode devices

(g) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX} _____ V
Gate source resistance R_G _____ Ω

Gate bias resistance R_{GX} _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurements (V_{DRM})

(a) Pretest

Room temperature off-state current must be less than the specified value at the beginning of the test. It is recommended that off-state current should be measured and recorded at the beginning and end of test to permit calculating its change.

(b) In process

The off-state current shall always be less than I_{DRM}.

(c) Post test

The device shall not fail any of its specified characteristics or exhibit parametric shifts outside of specified delta limits. Large changes in measured values are a possible indication of cumulative device degradation.

4.2 Nonrepetitive peak on-state surge current (I_{TSM})

4.2.1 Introduction (I_{TSM})

This test verifies the device's ability to survive a quasi-sinusoidal current wave with defined amplitude, frequency, and duration. The test simulates the conditions that occur when the device is protecting a telephone line, when an ac power line contacts or induces current into the line.

Figure 9 describes the surge waveform. The exact shape of the current wave depends on device and circuit parameters. Different types of devices (positive-breakdown-resistance, negative-breakdown-resistance, forward-conducting) result in somewhat different current waveshapes.

4.2 Nonrepetitive peak on-state surge current (I_{TSM}) (cont'd)

4.2.2 Test method for I_{TSM}

A zero-crossing switch (figure 10) connects the device under test, through a series resistance, to an ac voltage source providing a peak voltage greater than the device breakover voltage. A bridge rectifier is added to the circuit for testing reverse-blocking devices that are not rated for bidirectional surges. The optional capacitor simulates distributed capacitance on the transmission line and aids switching. Low values for R2, and large C, will increase di/dt stress if the leadlength is short, and can result in damage to the DUT. A heatsink may be required to maintain device case or lead temperature. Case or lead temperature, the heatsink, and conditions of device mounting shall be defined.

(1) Test conditions to be specified

(a) Source voltage (V_{ac}) _____ V_{rms}

(b) Short-circuit current _____ A_{peak}
or:
Load resistance (R_L) _____ Ω

(c) Case or lead temperature (T_C or T_L) _____ °C

(d) Frequency (Typically 50 or 60 Hz) _____ Hz

(e) Test duration

Number of pulses _____ pulses
or:
Time _____ seconds

(f) Number of test repetitions _____ trials

(g) Cooling time between test repetitions _____ seconds

(h) Describe mounting, leadlength, or board material and foil pattern

parameters applicable only to triode devices

(i) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX}__ _____ V
Gate source resistance R_G__ _____ Ω

Gate bias resistance R_{GX}__ _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

4.2 Nonrepetitive peak on-state surge current (I_{TSM}) (cont'd)

4.2.2 Test method for I_{TSM} (cont'd)

(2) Post test measurements

The device shall not fail any of its specified characteristics or exhibit parametric shifts outside specified limits. Large changes in measured values are a possible indication of cumulative device degradation.

4.3 Nonrepetitive peak impulse current (I_{PPS})

4.3.1 Introduction (I_{PPS})

This test verifies the device's ability to survive a double exponential current surge. These surges are typical of those resulting from the effects of lightning on transmission lines. Examples include telephone, current-loop control, and data transmission lines. The ratios "A/B" and "C/B" describe the surge waveshapes. "A" is the current waveshape virtual front time, "C" is the voltage waveshape virtual front time, and "B" is the impulse duration. Figures 11 and 12 show the impulse waveshape.

4.3.2 Test method for I_{PPS} testing

The device under test is connected to a surge generator (figure 13). The generator may be synthesized with active or passive components. These tests may be defined in terms of the voltage and current wave or the circuit. The open-circuit voltage wave and the short-circuit current wave can be significantly different for some test definitions.

Capacitor discharge pulse forming networks (PFNs) are best described by a schematic showing component values and initial conditions. These circuits generate the impulse using L/R and, or RC time constants. Figure 13 illustrates the design of a simple inductive PFN. The components required for network construction are often large because of high voltages and currents. This can result in waveform ringing and spikes that are the result of parasitic inductance and capacitance. Shunt-series connected RC snubbers may be added to filter out waveform aberrations or to adjust the value of dv/dt. These components shall be carefully selected to prevent damage to the device under test by the snubber discharge that takes place when the device under test switches.

TSPDs respond to the rate, amplitude, and duration of current flow through their terminals. These waveform parameters can be different from a generator's open-circuit voltage wave or short-circuit current wave. The device under test virtually short circuits the generator when it switches. Consequently, its main terminal current wave resembles the generator's short-circuit current wave. High voltages improve the semblance, causing the DUT to switch more quickly. High test voltages require larger resistor values. These improve current control and pulse fidelity. However, capacitor discharge currents and inductive current diversion effects can significantly alter the current wave through the DUT from that of the short-circuited generator.

The rate of voltage rise (dv/dt), before avalanche, results in capacitance charging displacement currents. These currents tend to increase turn-on speed, promote uniform conduction, and aid device robustness. The rate of current rise after the start of avalanche depends on dv/dt. Higher dv/dt can increase current rates, power loss, peak voltage, and stress. These are counterbalancing effects.

4.3 Nonrepetitive peak impulse current (I_{PPS}) (cont'd)

4.3.2 Test method for I_{PPS} testing (cont'd)

The pulse width of the test is usually short in comparison to the package thermal time constant. Case or lead temperature control does not require a heatsink, provided the duty cycle and average power of the impulse sequence are low.

Each polarity of bidirectional devices shall be separately tested.

(1) Test conditions to be specified

(a) Peak impulse short-circuit current (I_{PPS}) _____ A

(b) Peak impulse open-circuit voltage _____ V

(c) Virtual front time (short-circuit current wave, figure 11) _____ µs

(d) Duration (short-circuit current wave, figure 11) _____ µs

(e) Virtual front time (open-circuit voltage wave, figure 12) _____ µs

(f) Duration (open-circuit voltage wave, figure 12) _____ µs

NOTE — Items (b) through (f) can be specified by a circuit diagram and initial conditions.

(g) Case or lead temperature (T_C or T_L) _____ °C

(h) Number of pulses _____ trials

(i) Pulse repetition time _____ seconds

<u>parameters applicable only to triode devices</u>

(j) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX} _____ V
Gate source resistance R_G _____ Ω

Gate bias resistance R_{GX} _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

4.3 Nonrepetitive peak impulse current (I_{PPS}) (cont'd)

4.3.2 Test method for I_{PPS} testing (cont'd)

2) Post test measurements

No device parameters may shift outside their specified limits or ratings. Large changes in measured values are a possible indication of cumulative device degradation.

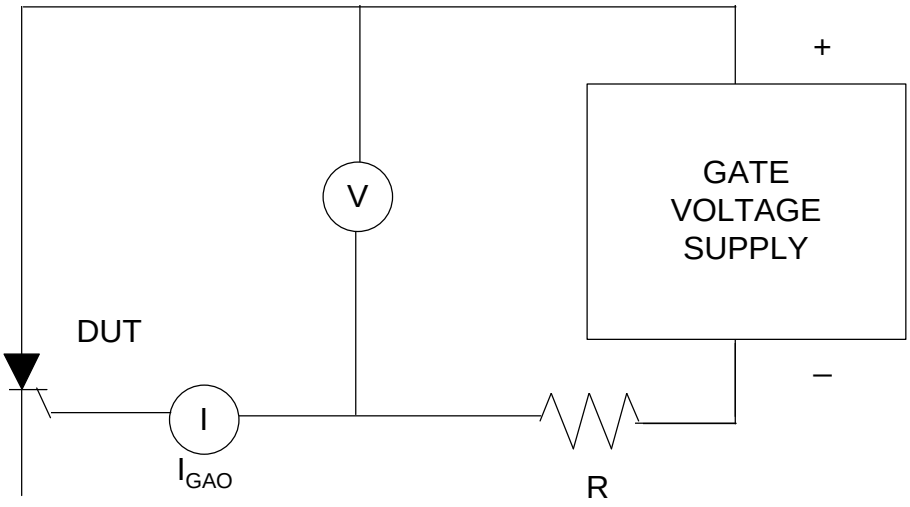


Figure 15 — P-gate reverse current, cathode terminal open test circuit

5 Characteristic tests

This section describes methods for measuring the electrical characteristics of TSPDs. Its objective is to aid correlation between manufacturers and users. It is the responsibility of the manufacturer and user to agree on the specified tests and perform correlation.

5.1 Off-state current (I_D) testing

Off-state current is tested by applying a voltage across the DUT ($V_D \leq V_{DRM}$) and measuring the resulting current. The applied voltage shall be gradually and carefully increased to the specified value to prevent voltage overshoot and dv/dt triggering of the device under test. It shall remain at the specified value until steady state conditions exist and the measurement is taken.

The off-state current is sensitive to temperature. High temperature measurements may require a heatsink to control the case and junction temperature and thus prevent thermal runaway. Alternatively, a pulsed test of short duration in comparison to the thermal time constant should be performed to prevent heating.

5.1.1 I_D test method

This test measures the off-state current flowing through a device in response to an applied off-state voltage.

Figure 14 shows the test circuit for diode devices. Triode devices are tested in similar fashion; however, the test circuit must add the gate bias when required. The resistor "R" is optional. It limits current flow and prevents possible damage to the device under test and the ammeter in the event of DUT turn-on. Its value shall be selected for negligible voltage drop at I_D.

Bidirectional devices require a test for each polarity.

(1) Test conditions to be specified

(a) Off-state voltage (V_D) _____ V

(b) Junction temperature (T_J) _____ °C

(c) Test duration (t_w) (use with pulsed tests) _____ ms

5.1 Off-state current (I_D) testing (cont'd)

5.1.1 I_D test method (cont'd)

parameters applicable only to triode devices

(d) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX} _____ V
Gate source resistance R_G _____ Ω

Gate bias resistance R_{GX} _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurement

Off-state current (I_D) _____ μA

5.1.2 Reverse gate current test, adjacent terminal open (triodes), I_{GAO}, I_{GKO}

This test measures the reverse gate to anode off-state current of a p-gate device with the cathode terminal open or the reverse gate to cathode off-state current of an n-gate device with the anode open. Figures 15 (p-gate types) and 16 (n-gate types) show test circuits for measurement of reverse gate current with the adjacent terminal open.

(1) Test conditions to be specified

(a) Gate bias voltage V_{GX} _____ V

(b) Junction temperature (T_J) _____ °C

(c) Test duration (t_w) (use with pulsed tests) _____ ms

(2) Test measurements

(a) P-gate reverse current (I_{GAO}) _____ μA

or:

(b) N-gate reverse current (I_{GKO}) _____ μA

5.1 Off-state current (I_D) testing (cont'd)

5.1.2 Reverse gate current test, adjacent terminal open (triodes), I_{GAO}, I_{GKO} (cont'd)

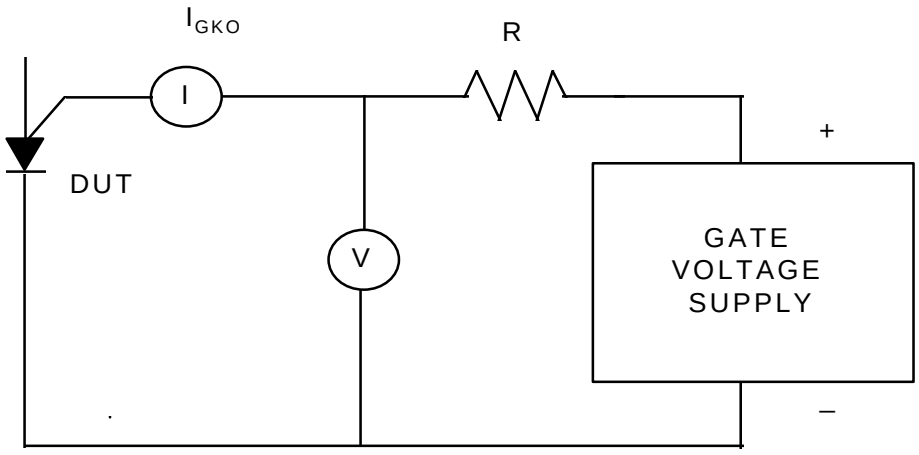


Figure 16 — N-gate reverse current, anode terminal open test circuit

5.1.3 Reverse gate current test, adjacent terminal shorted (triodes), I_{GAS}, I_{GKS}

This test measures the reverse gate to anode current of a p-gate device when the anode is short-circuited to the cathode or the reverse gate to cathode current of a n-gate device with the cathode shorted to the anode.

Figures 17 (p-gate types) and 18 (n-gate types) show test circuits for measurement of reverse gate current with the adjacent terminal short-circuited.

(1) Test conditions to be specified

(a) Gate bias voltage V_{GX}__ _____ V

(b) Junction temperature (T_J) _____ °C

(c) Test duration (t_w) (use with pulsed tests) _____ ms

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurements

(a) P-gate reverse current (I_{GAS}) _____ µA

or:

(b) N-gate reverse current (I_{GKS}) _____ µA

5.1 Off-state current (I_D) testing (cont'd)

5.1.3 Reverse gate current test, adjacent terminal shorted (triodes), I_{GAS},I_{GKS} (cont'd)

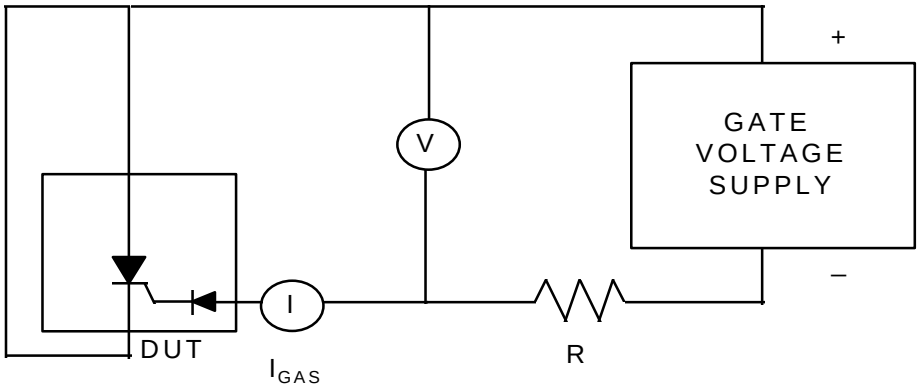


Figure 17 — P-gate reverse current, cathode terminal shorted test circuit

5.1.4 On-state reverse gate current test (triodes), I_{GAT}, I_{GKT}

This test measures the reverse gate current when the thyristor is turned on. On-state conduction increases the gate off-state current.

Figure 19 (p-gate types) and figure 20 (n-gate types) show test circuits for measurement of reverse gate current during on-state conduction.

(1) Test conditions to be specified

(a) Gate bias voltage V_{GX}__ _____ V

(b) On-state current (I_T) _____ A

(c) Junction temperature (T_J) _____ °C

(d) Test duration (t_w) (use with pulsed tests) _____ ms

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurements

(a) P-gate reverse current (I_{GAT}) _____ mA

or:

(b) N-gate reverse current (I_{GKT}) _____ mA

5.1 Off-state current (I_D) testing (cont'd)

5.1.4 On-state reverse gate current test (triodes), I_{GAT}, I_{GKT} (cont'd)

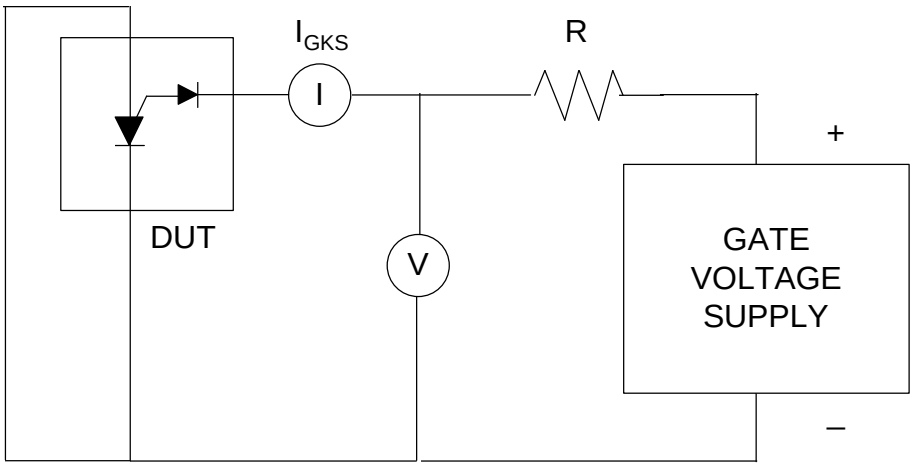


Figure 18 — N-gate reverse current, cathode terminal shorted test circuit

5.1.5 Forward-conducting state reverse gate current test (triodes), I_{GAF}, I_{GKF}

This test applies to forward conduction triode type devices only. It measures the reverse gate current when the surge protector diode is on. Diode conduction increases the gate off-state current.

Figure 21 (p-gate types) and figure 22 (n-gate types) show test circuits for measurement of reverse gate current when forward current flows.

(1) Test conditions to be specified

(a) Gate bias voltage V_{GX} _____ V

(b) Forward conduction current (I_F) _____ A

(c) Junction temperature (T_J) _____ °C

(d) Test duration (t_w) (use with pulsed tests) _____ ms

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurements

(a) P-gate reverse current (I_{GAF}) _____ µA

or:

(b) N-gate reverse current (I_{GKF}) _____ µA

5.1 Off-state current (I_D) testing (cont'd)

5.1.6 Peak off-state gate current test for triode devices (I_{GDM})

This test measures the gate off-state current when the thyristor portion of the TSPD blocks voltage. Figures 23 and 24 show the measurement circuit for p-gate and n-gate devices.

(1) Test conditions to be specified

(a) Maximum rated gate off-state voltage (V_{GDM}) _____ V

(b) Maximum rated anode to cathode off-state voltage _____ V

(c) Junction temperature (T_J) _____ °C

(d) Test duration (t_w) (use with pulsed tests) _____ ms

(2) Test measurements

(a) Maximum gate reverse current (I_{GDM}) _____ μA

(b) Anode (n-gate) or cathode (p-gate) off-state current (I_D) _____ μA

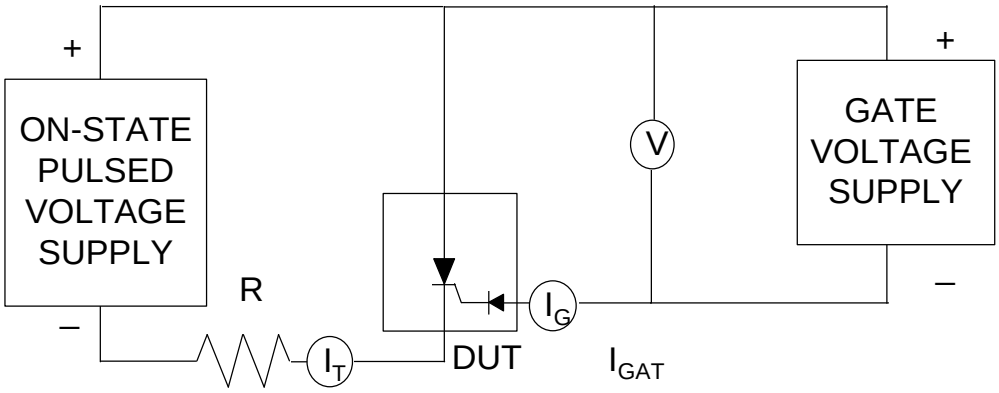


Figure 19 — P-gate reverse current, on-state test circuit

5.2 Breakover voltage $V_{(BO)}$ testing

These measurements evaluate a device's ability to limit voltage. Peak voltage is a complex function of stimulus waveshape, amplitude, duration, and device junction heating. Typical device behavior includes clamping and switching attributes. Current flow amplitudes and rates also influence device response. Gated types include characterizable current responses in the gate circuit, in addition to those associated with the principal current.

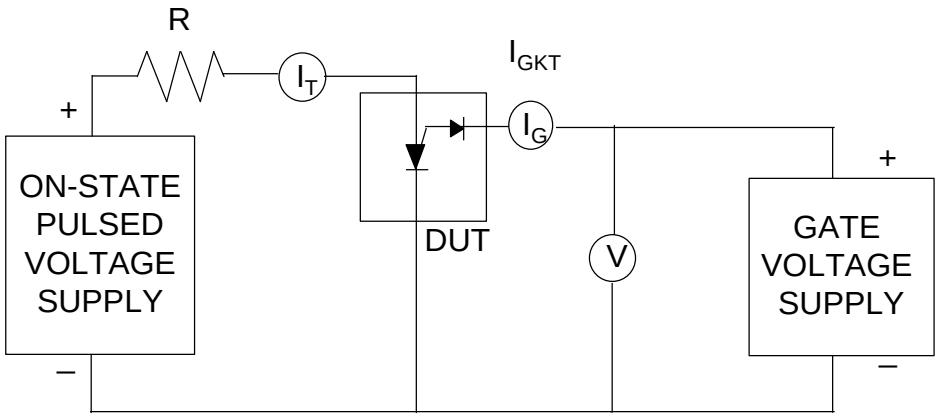


Figure 20 — N-gate reverse current, on-state test circuit

5.2.1 AC $V_{(BO)}$ test method (all device types)

This test simulates the conditions that occur when an ac power line contacts or induces current into a telephone line protected by the TSPD. It is similar to the I_{TSM} test described in 2.2. The peak voltage across the device under test is measured using an oscilloscope or peak detecting circuit. Figure 35 shows typical waveforms.

The current may be lower than for I_{TSM} verification. The selection of a lower current (particularly for positive resistance device types) can lengthen the time spent operating in the avalanche region, increase self-heating, and raise $V_{(BO)}$. The selection of a current amplitude sufficient to fully turn the DUT on, but low enough to prevent unnecessary heating, is desirable.

$V_{(BO)}$ is temperature dependent. A heatsink may be necessary to control the case or lead temperature. The heatsink or conditions of device mounting shall be defined.

5.2 Breakover voltage $V_{(BO)}$ testing (cont'd)

5.2.1 AC $V_{(BO)}$ test method (all device types) (cont'd)

A zero crossing-cycle counting switch connects the device under test, through a series resistance, to an ac voltage source (figure 25). This source shall provide a peak voltage greater than or equal to $V_{(BO)}+I_{(BO)}*R_L$ in order to breakover the DUT. Unidirectional TSPDs may require the inclusion of series rectification, as shown in Figure 10.

The optional capacitor simulates distributed capacitance on a transmission line and aids switching. Very low values for R2, and large C, will increase turn-on di/dt stress if the leadlength is short and the series inductance is low and can cause damage to the DUT as a result of the capacitor discharge.

A single half-cycle ac test minimizes self-heating, prevents thermal interactions, and improves the accuracy of measurement. Thermal effects may cause errors when devices are bidirectional and heat remains from the previous polarity tested, or when several tests must run with little cooling time between them. Sufficient cooling time shall be allowed to ensure correct initial temperature conditions.

(1) Test conditions to be specified

(a) Source voltage (V_{ac}) _____ V_{rms}

(b) Source frequency (f) _____ Hz

(c) Short-circuit current _____ A_{peak}

or:

(d) Load resistance (R_L) _____ Ω
or:
R_1 _____ Ω
and:
R_2 _____ Ω

(e) Optional capacitor (C) _____ μF

(f) Case or lead temperature (T_C or T_L) _____ °C

(g) Describe mounting, leadlength, or board material and foil pattern

(h) Test duration (t_w) _____ ms
or:
Number of pulses _____ pulses

5.2 Breakover voltage $V_{(BO)}$ testing (cont'd)

5.2.1 AC $V_{(BO)}$ test method (all device types) (cont'd)

parameters applicable only to triode devices

(i) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX} _____ V
Gate source resistance R_G _____ Ω

Gate bias resistance R_{GX} _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurement

Breakover voltage ($V_{(BO)}$) _____ V
or:
Gate-to-cathode breakover voltage ($V_{GK(BO)}$) _____ V
or:
Gate-to-anode breakover voltage ($V_{GK(BO)}$) _____ V

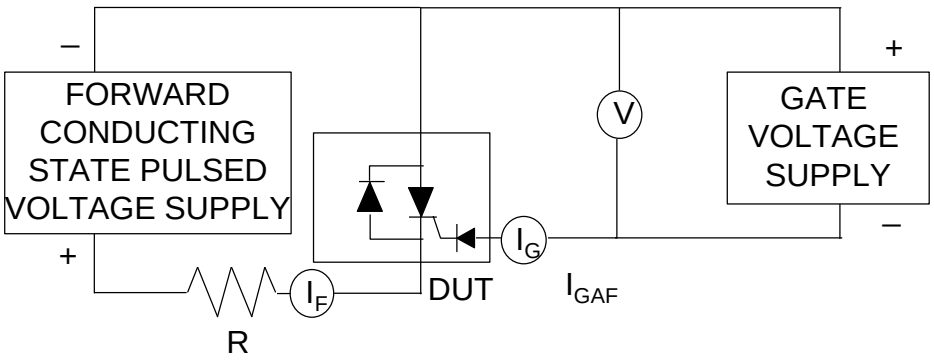


Figure 21 — P-gate reverse current, forward-conducting state test circuit

5.2 Breakover voltage $V_{(BO)}$ testing (cont'd)

5.2.2 Impulse $V_{(BO)}$ test method (all device types)

This test simulates the conditions when a device limits the voltage on a telephone line when a lightning strike occurs. It is similar to the I_{PPS} test described in 2.3. However, instead of checking device robustness, it measures the resulting peak voltage across the TSPD with an oscilloscope or peak detector (figure 26). Therefore, the impulse $V_{(BO)}$ specification may have shorter duration and lower amplitude than the I_{PPS} test. Lower energy pulses are desirable to reduce the chance of damaging a device with a test intended primarily for voltage measurement and to prevent self-heating from influencing following measurements. Sufficient cooling time between test repetitions to provide equilibrium temperature shall be used to prevent errors due to self-heating.

The device under test is connected to a surge generator (figure 13). The generator may be synthesized with active or passive components. These tests may be defined in terms of the voltage and current wave or the circuit. The open-circuit voltage wave and the short-circuit current wave can be significantly different for some test definitions.

Capacitor discharge pulse forming networks (PFNs) are best described by a schematic showing component values and initial conditions. These circuits generate the impulse using L/R and/or RC time constants. Figure 13 illustrates the design of a simple inductive PFN. The components required for network construction are often large because of high voltages and currents. This can result in waveform ringing and spikes that are the result of parasitic inductance and capacitance. Shunt-series connected RC snubbers may be added to filter out waveform aberrations or to adjust the value of dv/dt. These components shall be carefully selected to prevent damage to the device under test by the snubber discharge that takes place when the device under test switches (see 4.3.2 for additional information).

The PFN open-circuit voltage and its Thevenin driving resistance determine the peak short-circuit current. Snubbers can change the driving impedance seen by the unit under test and alter the current wave and the resulting breakover voltage. This is significant when the snubber is located close to the DUT, the snubber discharge current is appreciable in comparison to I_{PPS}, and the snubber discharge time constant is longer than or comparable to the device turn-on time.

Measurements using fast pulses are subject to errors resulting from inductance and rapidly changing currents. High frequency techniques (short connections and thick conductors) should be used. Differential preamplifier measurement techniques or single point grounding may be used to prevent errors due to ground loops and currents along probe leads. Shielding of the generator may be needed to prevent unwanted signal radiation and pickup. Twisting the probe leads together, reducing the area of loops formed by them, and placing the probes through magnetic cores help to prevent errors caused by magnetically induced currents flowing along the cable shields. Errors resulting from electric coupling and parasitic capacitance can be reduced by using Faraday shields and ground planes.

Measurements using slow pulses (< 10 V/ms) can cause significant heating of the TSPD. Device damage could be caused by prolonged operation of the device in the breakdown region. As the intent of this test is accurate voltage measurement instead of stress testing, this condition should be avoided.

Figures 27 and 28 show the test circuits for p-gate and n-gate devices.

5.2 Breakover voltage $V_{(BO)}$ testing (cont'd)

5.2.2 Impulse $V_{(BO)}$ test method (all device types) (cont'd)

(1) Test conditions to be specified

parameters for diode and triode device types

(a) Peak impulse short-circuit current _____ A

(b) Peak impulse open-circuit voltage _____ V

NOTE — Items (c) through (f) apply to tests with double exponential waves.

(c) Virtual front time (short-circuit current wave, figure 11) _____ µs

(d) Duration (short-circuit current wave, figure 11) _____ µs

(e) Virtual front time (open-circuit voltage wave, figure 12) _____ µs

(f) Duration (open-circuit voltage wave, figure 12) _____ µs

NOTE — If a double exponential impulse is not used, specify dv/dt and source resistance.

(g) dv/dt (open-circuit voltage wave) _____V/µs

(h) Generator source resistance (R_S) _____ Ω

NOTE — Items (b) to (f) can be specified by a circuit diagram showing initial conditions.

(i) Case or lead temperature (T_C or T_L) _____ °C

parameters applicable only to triode devices

(j) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX}__ _____ V
Gate source resistance R_G__ _____ Ω

Gate bias resistance R_{GX}__ _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

5.2 Breakover voltage $V_{(BO)}$ testing (cont'd)

5.2.2 Impulse $V_{(BO)}$ test method (all device types) (cont'd)

(2) Test measurements

Breakover voltage ($V_{(BO)}$)	_____ V
or:	
Gate-to-cathode breakover voltage ($V_{GK(BO)}$) p-gate triodes	_____ V
or:	
Gate-to-anode breakover voltage ($V_{GA(BO)}$) n-gate triodes	_____ V

5.3 Breakover current ($I_{(BO)}$) testing

This test measures the TSPD breakover current with an oscilloscope. It is the current through the TSPD at the breakover voltage. This current can be measured by adding a low value noninductive "sense" resistor (0.001 to 0.1 Ohm) in series with the TSPD, and computing the current corresponding to the observed voltage drop across the resistance. Alternatively, a variety of commercial current probes and transformers can be used to measure the current.

The recommended test conditions are identical to those used for the breakover voltage measurement. The breakover current has a strong and complex dependence on the virtual front time, junction temperature, and device type (positive or negative-breakdown-resistance). Slow rates of current rise prolong operation in the breakdown region causing high dissipation resulting in low values of measured $I_{(BO)}$ or device damage. This effect is most prominent in positive resistance types.

Fast rates of current rise increase measured $I_{(BO)}$ because of the finite reaction time of the TSPD.

Negative-breakdown-resistance TSPDs have low breakover currents, often on the order of a few microamperes at low values of dv/dt. This current will be negligible for most applications and need not be measured.

5.3.1 AC $I_{(BO)}$ test method (positive resistance types)

A single half-cycle ac pulse is recommended to reduce thermal errors. The device shall be allowed to cool to equilibrium temperature between each test.

This test uses the same circuit described in 3.2.1 for ac $V_{(BO)}$. Figure 35 shows the typical current waveform.

(1) Test conditions to be specified

(a) Source voltage (V_{ac})	_____ V_{RMS}
(b) Source frequency (f)	_____ Hz

5.3 Breakover current ($I_{(BO)}$) testing (cont'd)

5.3.1 AC $I_{(BO)}$ test method (positive resistance types) (cont'd)

(c) Short-circuit peak current (I_{sc}) _____ A

or:

(d) Load resistance (R_L) _____ Ω

or:

R_1 _____ Ω
and
R_2 _____ Ω

(e) Optional capacitor (C) _____ μF

(f) Case or lead temperature (T_C or T_L) _____ °C

(g) Describe mounting, leadlength, or board material and foil pattern

parameters applicable only to triode devices

(h) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX} _____ V
Gate source resistance R_G _____ Ω

Gate bias resistance R_{GX} _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurement

Breakover current ($I_{(BO)}$) _____ mA

5.3 Breakover current ($I_{(BO)}$) testing (cont'd)

5.3.1 AC $I_{(BO)}$ test method (positive resistance types) (cont'd)

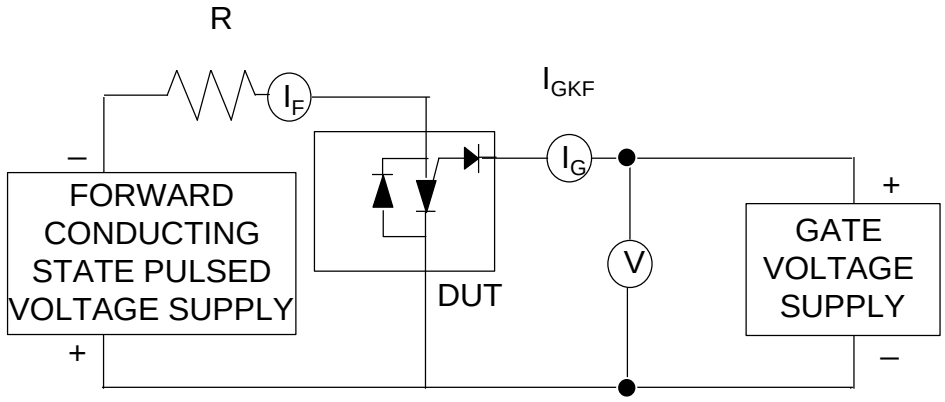


Figure 22 — N-gate reverse current, forward-conducting state test circuit

5.3.2 Impulse $I_{(BO)}$ test method (all device types)

The recommended test conditions are identical to those for Impulse $V_{(BO)}$. Figure 26 describes typical waveforms.

Figure 13 shows the test circuit. The information in 5.2.2 applies.

(1) Test conditions to be specified

(a) Peak impulse short-circuit current _____ A

(b) Peak impulse open-circuit voltage _____ V

NOTE — Items (c) through (f) apply for tests with double exponential waves

(c) Virtual front time (short-circuit current wave, figure 11) _____ µs

(d) Duration (short-circuit current wave, figure 11) _____ µs

(e) Virtual front time (open-circuit voltage wave, figure 12) _____ µs

5.3 Breakover current ($I_{(BO)}$) testing (cont'd)

5.3.2 Impulse $I_{(BO)}$ test method (all device types) (cont'd)

(f) Duration (open-circuit voltage wave, figure 12) _____ μs

NOTE — If a double exponential impulse is not used, specify dv/dt and source resistance.

(g) dv/dt (open-circuit voltage wave) _____ V/μs

(h) Generator source resistance (R_S) _____ Ω

NOTE — Items (b) to (f) can be specified by a circuit diagram showing initial conditions.

(i) Case or lead temperature (T_C or T_L) _____ °C

parameters applicable only to triode devices

(j) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX}___ _____ V
Gate source resistance R_G___ _____ Ω

Gate bias resistance R_{GX}___ _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurement

Breakover current ($I_{(BO)}$) _____ mA

5.4 Gate-switching current (I_{GSM}) and charge (Q_{GS}) testing

Gated device types couple some of the impulse current into the gate circuit. The gate circuit must be designed for these conditions.

5.4.1 Gate-switching current (I_{GSM}) test method, triode types

This test measures the peak gate current resulting from the device switching on. The conditions for this test are identical to the impulse breakover test. Figures 27 and 28 show test circuits measuring the current with an oscilloscope.

5.4 Gate-switching current (I_{GSM}) and charge (Q_{GS}) testing (cont'd)

5.4.1 Gate-switching current (I_{GSM}) test method, triode types (cont'd)

(1) Test conditions to be specified

(a) Peak impulse short-circuit current _____ A

NOTE — Items (b) to (f) can be specified by a circuit diagram showing initial conditions.

(b) Peak impulse open-circuit voltage _____ V

NOTE — Items (c) through (f) apply for tests with double exponential waves.

(c) Virtual front time (short-circuit current wave, figure 11) _____ µs

(d) Duration (short-circuit current wave, figure 11) _____ µs

(e) Virtual front time (open-circuit voltage wave, figure 12) _____ µs

(f) Duration (open-circuit voltage wave, figure 12) _____ µs

NOTE — When a linear ramp is used, specify dv/dt and source resistance for (g) and (h).

(g) dv/dt (open-circuit voltage wave) _____ V/µs

(h) Generator source resistance (R_S) _____ Ohms

(i) Case or lead temperature (T_C or T_L) _____ °C

(j) Gate bias voltage

V_{GA} (p-gate types) _____ V
or:
V_{GK} (n-gate types) _____ V
or:
Gate decoupling capacitor (C_G) _____ nF

(2) Test measurement

Peak gate-switching current (I_{GSM}) _____ A

5.4 Gate-switching current (I_{GSM}) and charge (Q_{GS}) testing (cont'd)

5.4.1 Gate-switching current (I_{GSM}) test method, triode types (cont'd)

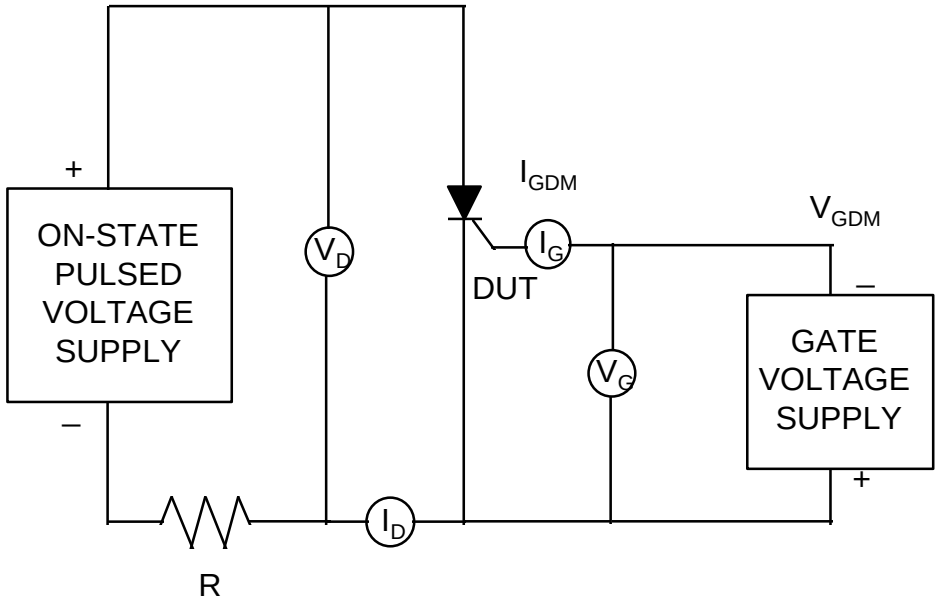


Figure 23 — P-gate-to-cathode terminal peak off-state voltage test, peak off-state p-gate current test circuit

5.4.2 Gate-switching charge (Q_{GS}) test method, triode types

This test measures the gate charge, resulting from voltage limiting, which will increase the magnitude of the gate voltage supply. The conditions for this test are identical to the impulse breakover test. Figures 27 and 28 show the test circuits.

(1) Test conditions to be specified

(a) Peak impulse short-circuit current _____ A

(b) Peak impulse open-circuit voltage _____ V

NOTE — Items (c) through (f) apply for tests with double exponential waves.

(c) Virtual front time (short-circuit current wave, figure 11) _____ µs

(d) Duration (short-circuit current wave, figure 11) _____ µs

(e) Virtual front time (open-circuit voltage wave, figure 12) _____ µs

5.4 Gate-switching current (I_{GSM}) and charge (Q_{GS}) testing (cont'd)

5.4.2 Gate-switching charge (Q_{GS}) test method, triode types (cont'd)

(f) Duration (open-circuit voltage wave, figure 12) _____ μs

NOTE — If a double exponential impulse is not used, specify dv/dt and source resistance

(g) dv/dt (open-circuit voltage wave) _____V/μs

(h) Generator source resistance (R_S) _____ Ω

(i) Case or lead temperature (T_C or T_L) _____ °C

(j) Gate bias voltage

V_{GA} (p-gate types) _____ V
or:
V_{GK} (n-gate types) _____ V

(2) Test measurement

Gate charge (Q_{GS}) _____ nC

5.5 Holding current (I_H) testing

This test measures the ability of the device to revert back to an off state, following a surge, when dc current is present on the protected transmission line. The device turns off when its principal current falls below the holding current value.

A pulse generator turns the device on. The breakover current wave is superimposed on a dc or slowly decaying current provided by a generator (Figures 29 and 30).

Large breakover pulses heat the device and reduce the measured value of I_H. Damage by a test intended only to verify or measure I_H can occur. Time delay before subsequent tests to allow cooling and reduce thermal errors may become necessary.

Correlation between tests with different current waves depends on junction temperature at turn-off time. This objective requires similar energy loss in the DUT. Turn-off will never occur if self heating by the current from the holding generator causes the device holding current to remain below the critical value.

5.5 Holding current (I_H) testing (cont'd)

The following conditions are suggested to improve the accuracy of I_H measurement:

(1) The turn-on pulse duration should be long enough for the TSPD conduction to stabilize.

(2) The turn-on current amplitude should be much greater than the holding current. Various turn-on current amplitudes should also be tested since incomplete turn-on can result in a lower measured value of I_H.

(3) The turn-on pulse should quickly and cleanly turn the device on. This avoids hot spots and tolerance in the measured I_H value.

(4) The test duration should be long enough to allow thermal disturbances created by the breakdown event to die out before turn-off, but not so long as to cause undesired on-state heating.

(5) The turn-off loadline should not intersect the device breakdown characteristic to prevent incomplete turn-off and device heating. Select the turn-off voltage below $V_{(BR)}$ or V_S.

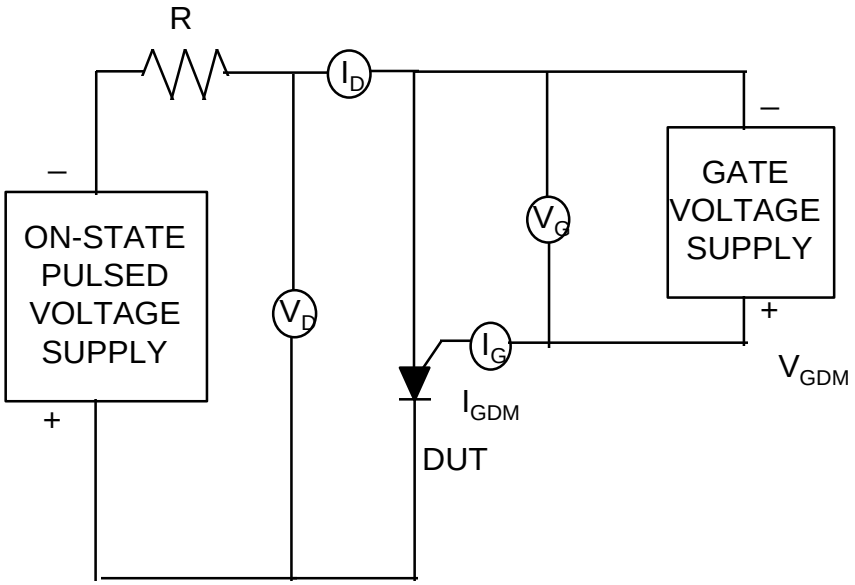


Figure 24 — N-gate-to-anode terminal peak off-state voltage test circuit, peak off-state n-gate current test circuit

5.5 Holding current (I_H) testing (cont'd)

5.5.1 I_H test circuit (impulse method)

The test apparatus may be synthesized with active or passive components. Figure 29 shows a simple passive circuit suitable for I_H verification. An example of a breakover generator is shown in figure 13. The holding current is supplied by a generator consisting of a non-inductive resistor in series with a dc power supply. These generators connect to the DUT through diodes D_1 and D_2.

Following breakover, the voltage across the DUT drops to a low value allowing both generators to supply current into the DUT. The exponentially decaying current from the breakover generator asymptotically approaches the dc current supplied by the holding generator. The holding current must be greater than this dc current for turn-off to occur. The holding current of failing units can be approximately measured by reducing V_H until turn-off occurs.

(1) I_H Test conditions to be specified

(a) Case or lead temperature (T_C or T_L) _____ °C

parameters of the breakover pulse

(b) Peak impulse short-circuit current _____ A

(c) Virtual front time (short-circuit current wave, figure 11) _____ µs

(d) Impulse duration (short-circuit current wave, figure 11) _____ µs

NOTE — Unless otherwise specified, use a 10/1000 µs or 10/700 µs waveform.

parameters of the holding generator

(e) Open-circuit voltage _____ V

(f) Load resistance _____ Ω

parameters applicable only to triode devices

(g) Gate bias voltage

V_{GA} (p-gate types) _____ V
or:
V_{GK} (n-gate types) _____ V

(2) Test measurement

Holding current (I_H) _____ mA

5.5 Holding current (I_H) testing (cont'd)

5.5.1 I_H test circuit (impulse method) (cont'd)

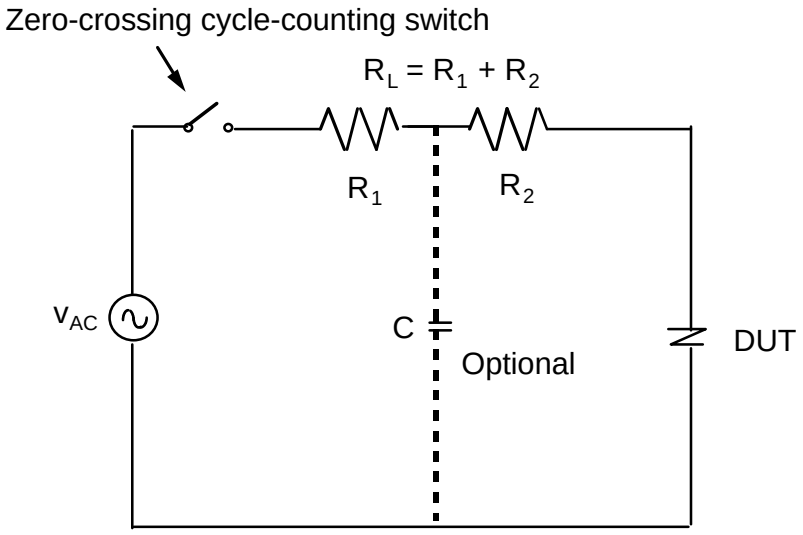


Figure 25 — AC $V_{(BO)}$ test circuit

5.5.2 I_H test circuit (ramp method)

This method is often employed by automatic test equipment. Figure 30 shows the block diagram of the test circuit. The high-voltage low-current breakover generator provides a short, fast rise pulse, turning the device on with negligible heating. The holding generator then linearly reduces the current through the device under test until the device turns off or a preset minimum level is achieved. The holding generator may be an ideal current source with zero slope load line, a variable voltage acting through a fixed series resistance, or a fixed voltage operating through a variable resistance. The diodes in series with each generator prevent them from loading one another. As the on-state current decreases the TSPD will switch off when the test circuit load line no longer intersects with the TSPD on-state characteristics.

The measured value of I_H can be influenced by the turn-off load-line intersection with the device characteristic. Figure 31 illustrates this behavior. In the case of a variable voltage acting through a fixed resistance, the slope of the load line is $-1/R_L$ and the load line undergoes parallel translations across the device characteristic. In the case of a fixed voltage with variable resistance, the loadline pivots about the holding generator open-circuit voltage. In the case of an ideal current source, the loadline is parallel to the voltage axis and undergoes parallel translations along the current axis. Slightly different minimum current intersections with the device characteristic and measured I_H values results from these method variations. Current source measurements tend to provide the lowest values for I_H.

5.5 Holding current (I_H) testing (cont'd)

5.5.2 I_H test circuit (ramp method) (cont'd)

Because holding current depends strongly on junction temperature at turn-off, correlation between different test methods requires equal junction temperatures. Test methods may minimize test heating or deliberately introduce self-heating for optimum correlation. Correlation exercises should be performed to determine the difference between test methods.

(1) I_H Test conditions to be specified

(a) Case or lead temperature (T_C or T_L) _____ °C

parameters of the holding generator

(b) Peak ramp current _____ A

(c) Ramp down rate _____ A/ms

(d) Turn-off load resistance (Specify if used.) _____ Ω

parameters applicable only to triode devices

(e) Gate bias voltage

V_{GA} (p-gate types) _____ V
or:
V_{GK} (n-gate types) _____ V

(2) Test measurement

Holding current (I_H) _____ mA

5.6 On-state voltage (V_T) testing

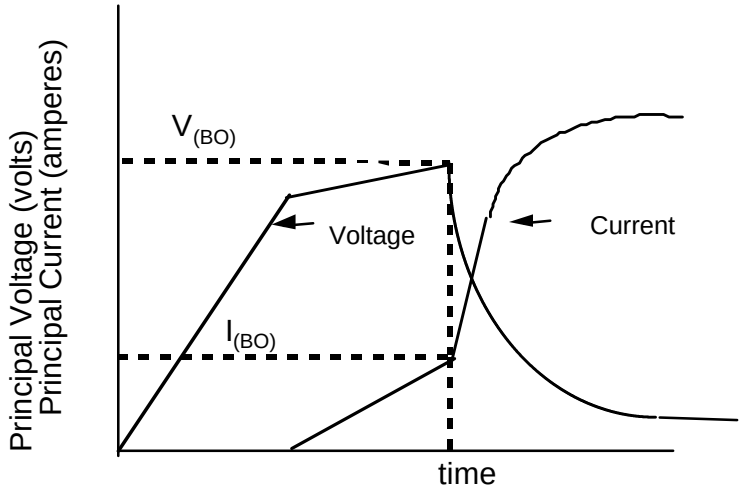
On-state power dissipation in a TSPD is proportional to on-state voltage. Knowledge of the on-state voltage is useful for estimating junction and case or lead temperature rise and heatsink requirements. The on-state voltage itself can have a dependence on temperature as well as current. Therefore, differing test methods have evolved.

The pulsed dc method is particularly useful for high-speed automated testing because it minimizes the effects of heating, reducing thermal interactions with subsequent tests.

The impulse method determines the on-state voltage with a double exponential current surge similar to that used in I_{PPS} testing.

5.6 On-state voltage (V_T) testing (cont'd)

The ac method turns the device on with a sinusoidal pulse similar to that occurring with contact or induction from a power line.



$_{(BO)}$, $I_{(BO)}$ test waveform

5.6.1 Pulsed dc on-state voltage (V_T) test method

This method uses either one high-voltage high-current power source or separate power sources to break the device over and supply the follow-on current.

In the former case, the single high-power source shall be capable of supplying the breakover current at the breakover voltage as well as the on-state current at the on-state voltage.

In the latter case, the breakover generator can be a low current high-voltage source and the follow-on generator can be a low-voltage high-current source. The breakover generator needs to supply sufficient current for a brief but yet long enough time to allow device latching and current delivery by the follow-on generator.

In both cases, the current pulse duration shall be long enough to establish near-equilibrium current and voltage conditions. This ensures complete turn-on of the device under test. The pulse shall be short enough to prevent excessive variation resulting from self-heating.

Figures 30 and 32 show the two test methods.

5.6 On-state voltage (V_T) testing (cont'd)

5.6.1 Pulsed dc on-state voltage (V_T) test method (cont'd)

(1) Test conditions to be specified

(a) On-state test current (I_T) _____ A

(b) Pulse width (t_w) _____ μs

(c) Case or lead temperature (T_C or T_L) _____ °C

(2) Test measurement

On-state voltage (V_T) _____ V

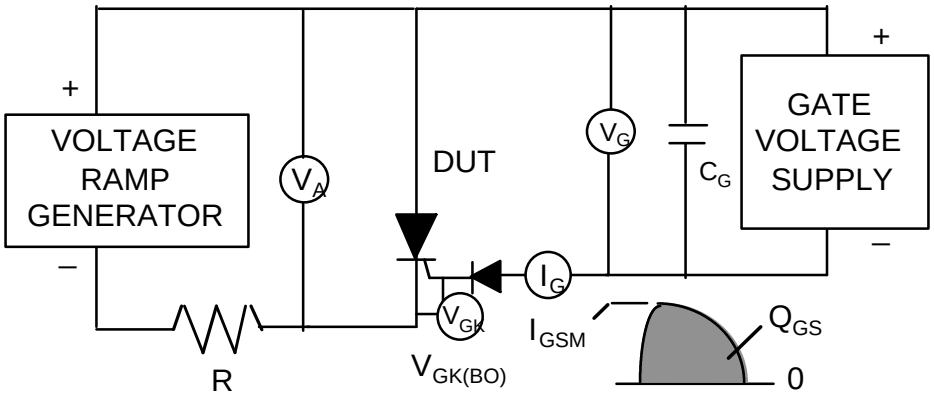


Figure 27 — P-gate switching Q, I, and gate to cathode breakover voltage test circuit

5.6.2 Impulse on-state voltage (V_T) test method

This test is similar to the pulsed dc on-state voltage test. It may be implemented using one or two power sources (figures 32 and 34).

The current wave has a double exponential waveform. Its heating effects are not negligible. Because no equilibrium current or junction temperature exists, V_T shall be measured at a defined current level as shown in Figure 33.

Figure 33 shows measurement waveforms.

5.6 On-state voltage (V_T) testing (cont'd)

5.6.2 Impulse on-state voltage (V_T) test method (cont'd)

(1) Test conditions to be specified

(a) Current waveform (10/1000 µs wave is recommended) _____ µs

(b) Short-circuit current peak amplitude _____ A

(c) On-state test current (I_T) _____ A

(d) Case or lead temperature (T_C or T_L) _____ °C

(2) Test measurement

Instantaneous on-state voltage (V_T) _____ V

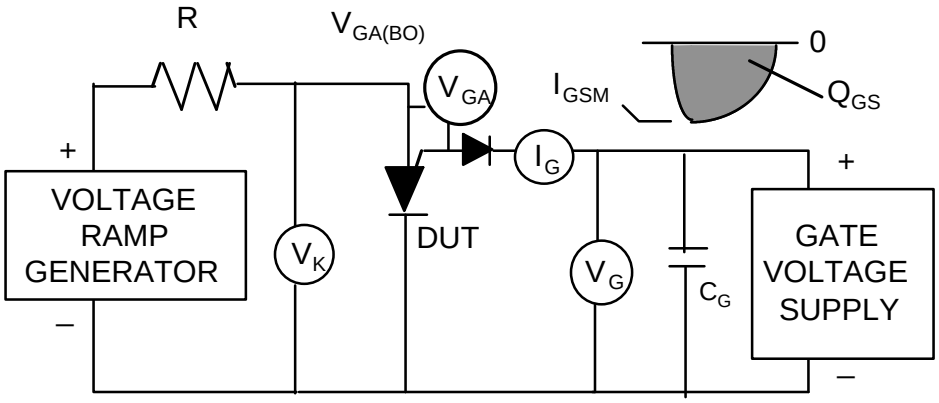


Figure 28 — N-gate switching Q, I, and gate-to-anode breakover voltage test

5.6.3 AC on-state voltage (V_T) test method

This method measures on-state voltage while operating the device with a sinusoidal power source. Junction heating will not be negligible. Positive resistance device types, operated at low currents, can experience appreciable avalanche mode heating resulting from power being dissipated while the device current rises to the breakover value. Consequently, measurements of this type need to specify the test conditions influencing breakover. The peak source voltage shall be greater than $V_{(BO)} + I_{(BO)}*R_L$.

5.6 On-state voltage (V_T) testing (cont'd)

5.6.3 AC on-state voltage (V_T) test method (cont'd)

The test circuit is identical to that used for ac $V_{(BO)}$ (figure 25). A zero-crossing switch applies a half cycle of power through a resistance to the device under test. The on-state voltage is measured at the peak of the sinusoidal current wave (figure 35).

(1) AC on-state voltage test conditions to be specified

(a) AC rms open-circuit voltage _____ V_{rms}

(b) Peak on-state test current _____ A_{peak}

(c) AC frequency (typically 50 or 60 Hz) _____ Hz

(d) Case or lead temperature (T_C or T_L) _____ °C

(2) AC on-state voltage test measurement

Instantaneous on-state voltage (V_T) _____ V

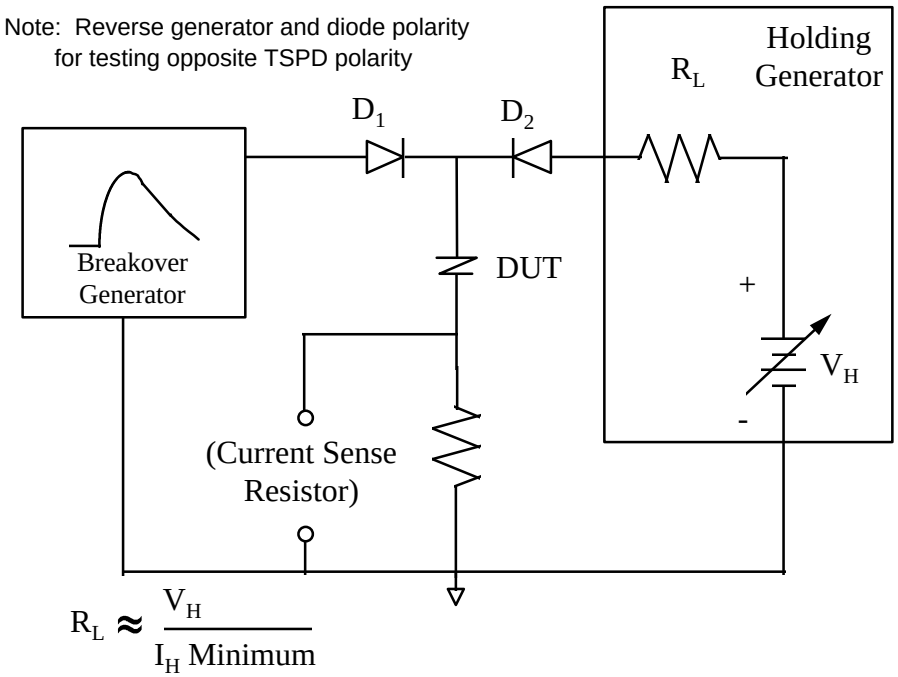


Figure 29 — Impulse method test circuit for I_H verification

5.7 Off-state capacitance (C_O) testing

This test applies to all TSPDs. The off-state capacitance of a TSPD is sensitive to temperature, dc voltage, and ac bias voltage. Devices with junctions exposed to light will be sensitive to light level.

Since the capacitance of a TSPD is voltage dependent, the amplitude of ac bias voltage (V_d) will affect the measured capacitance value. At zero dc voltage bias, forward-conducting TSPDs will have diode conduction occur if the ac bias exceeds 200 mV rms. Diode conduction gives high loss values and the measuring equipment's interpretation of the capacitance value can be in error.

TSPDs have multiple junctions. The series connected capacitances of these appear as part of the device capacitance. Applying increasing values of applied dc voltage charges that polarity's blocking junction. If the dc voltage bias is then decreased, the resulting discharge current causes the opposite polarities blocking junction to be charged, creating an internal voltage bias in addition to the externally applied bias. Adequate time needs to be allowed for this charge to disappear and stabilize the capacitance value. The shortest stabilization time occurs when measurements are taken progressively from the lowest to highest magnitude of dc voltage bias.

The capacitance value can be directly measured with commercially available equipment. These are usually multifunctional impedance bridges and network analyzers (measuring L, C, R, and phase angle). Most of the ac bias voltage, V_d, occurs at the equipment's high (Hi) measurement terminal. The low (Lo) measurement terminal provides the ac return path for the capacitance being measured.

When a TSPD has more than two terminals, there will be capacitance to the extra terminals. To remove the error caused by these additional capacitances, connect the other terminals to the equipment’s guard terminal. Normally the guard terminal is the equipment's earth plane.

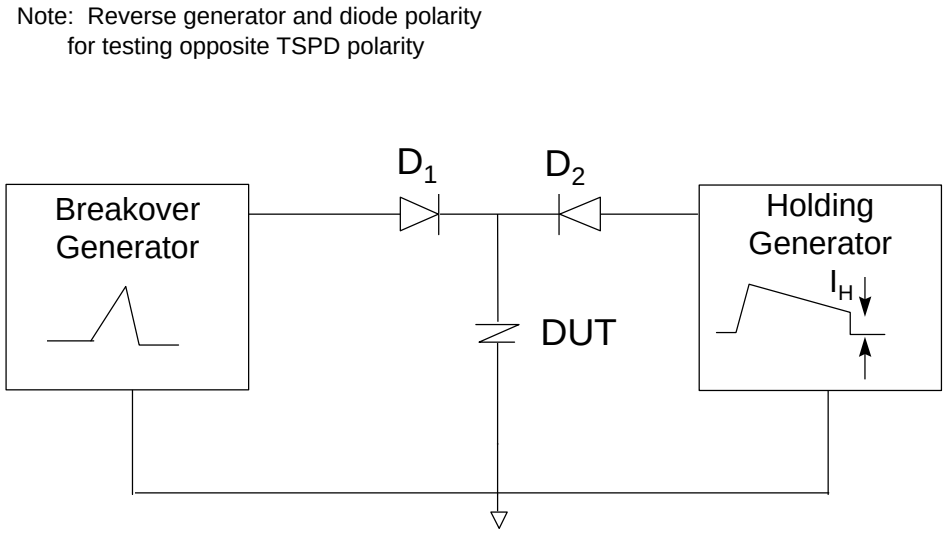


Figure 30 — Test circuit for ramp down method of I_H measurement

5.7 Off-state capacitance (C_O) testing (cont'd)

5.7.1 Two terminal TSPD capacitance (C_O) test method

Specified off-state dc voltage (V_D), ac frequency (f), and ac voltage (V_d) are applied to the DUT, and the resulting capacitance is measured.

The test circuit is shown in figure 36. Initially the equipment should be set for 0 V dc bias and the specified ac bias voltage. Any necessary equipment nulling and calibrating should then be done. After connecting the device, the specified dc bias voltage level shall be applied.

When the measurement equipment cannot provide adequate levels of dc bias voltage, the circuit shown in figure 37 may be used to apply the specified dc bias. To remove the capacitance of the bias components (C_1, C_2, R_1, R_2, variable dc voltage dc power supply) from the measurement, the bias circuit is connected to the equipment guard terminal (see Figure 37). The values of dc blocking capacitor, C_1 and C_2, shall be much larger than the device capacitance, so as not to reduce the measured capacitance value. Generally a capacitance value of 100 X C_O will be adequate. The value of the charging resistors, $R_1$and R_2, are set by the allowable dc voltage drop caused by the maximum expected off-state current, I_D, of the TSPD. Generally, a resistance value of 100 X (V_D/I_D) will be adequate. Low values of charging resistance can cause measurement equipment error due to excessive loading.

It may be desirable to prevent the possibility of the dc blocking capacitors rapidly discharging into the equipment's measurement terminals. Any protective network, such as a back-to-back avalanche diode pair, should be returned to the guard terminal to null out the capacitance of the protection network.

(1) Test conditions to be specified

(a) Off-state dc voltage bias (V_D) _____ V

(b) AC voltage and frequency

AC voltage (V_d) _____ V_{rms}

AC frequency (f) _____ kHz

(c) Case or lead temperature (T_C or T_L) _____ °C

(2) Test measurement

Off-state capacitance (C_O) _____ pF

5.7 Off-state capacitance (C_O) testing (cont'd)

5.7.1 Two terminal TSPD capacitance (C_O) test method (cont'd)

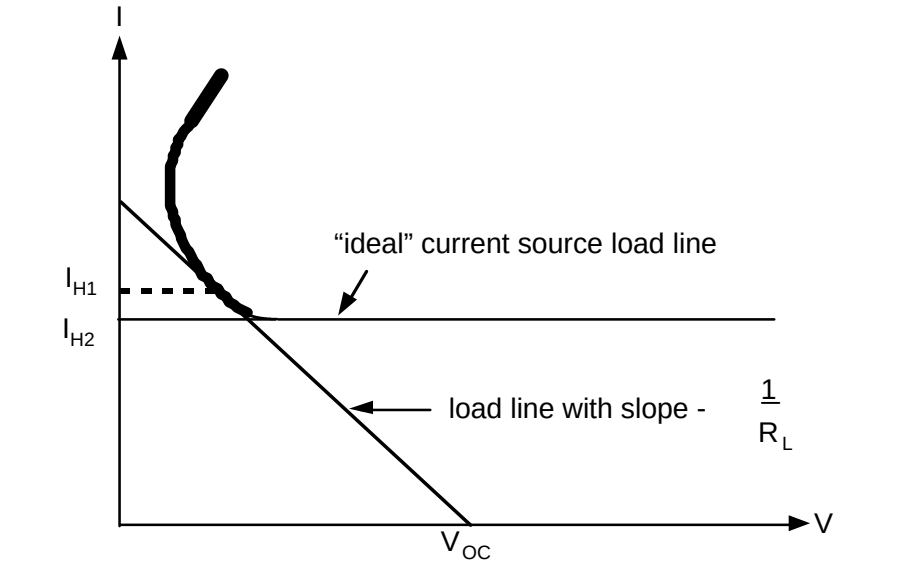


Figure 31 — I_H versus turn-off load line

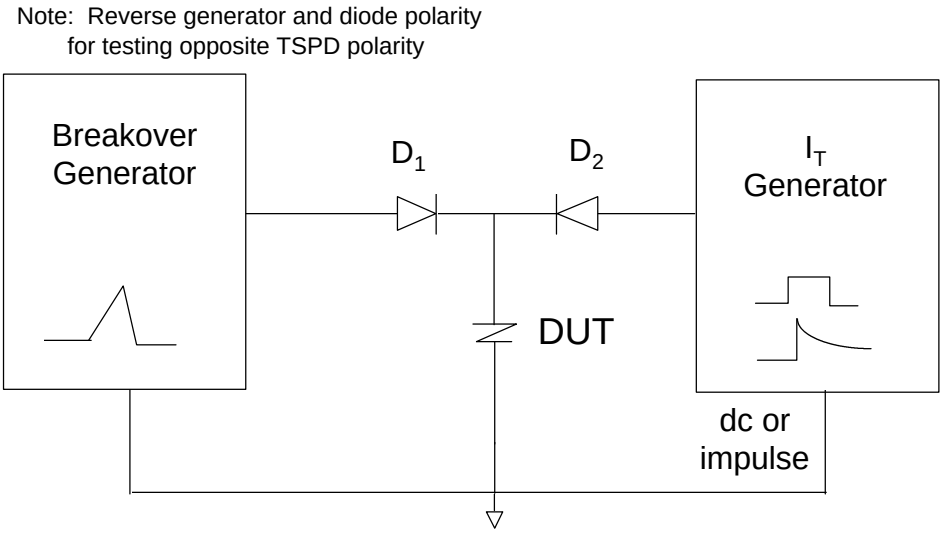


Figure 32 — Pulsed on-state voltage test

5.7 Off-state capacitance (C_O) testing (cont'd)

5.7.2 DC voltage-biased multi-terminal TSPD capacitance (C_O) test method

Specified dc voltages (V_{D1} to V_{DN}), ac frequency (f), and ac voltage (V_d), are applied to DUT, and the resulting capacitance is measured.

Figure 38 shows the test circuit. This is a general test circuit capable of measuring N terminal TSPDs. Each non-measurement terminal is returned to the guard terminal through an ac coupling capacitor, C_N. Any required dc voltage bias, V_{DN}, is applied from a voltage supply through the feed resistor, R_N. Unless there are specific requirements, the capacitance and resistance values can be made the same as those in the measurement terminal circuit (C_1=C_2, R_1=R_2). Initially the dc bias on the terminals should be set to 0 V dc and the specified ac bias applied from the measurement equipment. Any necessary equipment nulling and calibrating should then be done. After connecting the DUT, the specified dc bias voltage shall be applied to the DUT terminals. In some cases, it may be necessary to bias both the measurement terminals using voltage supplies V_{D1} and V_{D2}.

(1) Test conditions to be specified

(a) Off-state dc voltage bias (V_D)

use only as many terminals as are applicable

Terminal 1 _____ V

Terminal 2 _____ V

Terminal 3 _____ V

Terminal 4 _____ V

(b) AC bias

AC voltage (V_d) _____ V_{RMS}

AC frequency (f) _____ kHz

(c) Case or lead temperature (T_C or T_L) _____ °C

(2) Test measurements

Off-state capacitance (C_O) _____ pF

5.7 Off-state capacitance (C_O) testing (cont'd)

5.7.2 DC voltage-biased multi-terminal TSPD capacitance (C_O) test method (cont'd)

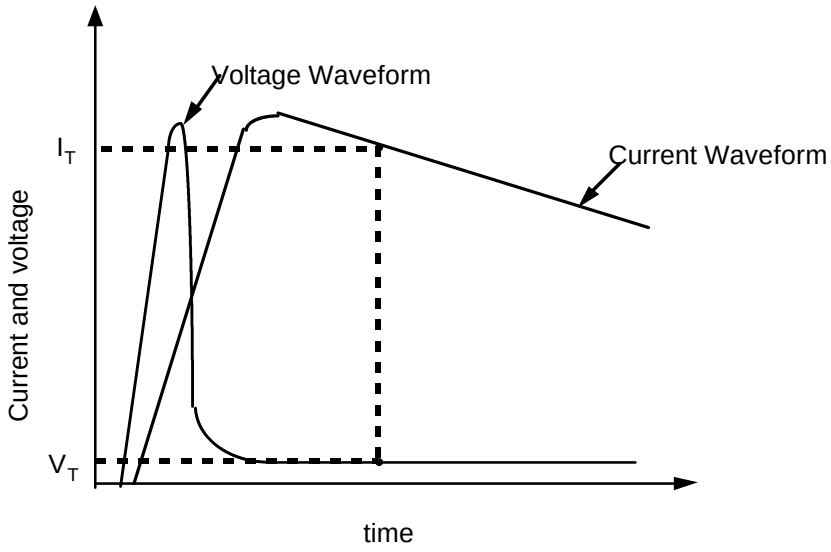


Figure 33 — Impulse on-state voltage measurement

5.8 Critical rate of rise of off-state voltage (dv/dt) test

5.8.1 Description (dv/dt)

A TSPD must not turn on because of typical voltage rates present within a circuit. Such rates cause self-capacitance charging currents that will trigger the thyristor on when their amplitude exceeds a critical value. This test determines whetherthe device will maintain a blocking state under the influence of voltages with peak amplitudes below the device breakover voltage and rates below the specified critical dv/dt value.

5.8 Critical rate of rise of off-state voltage (dv/dt) test (cont'd)

5.8.1 Description (dv/dt) (cont'd)

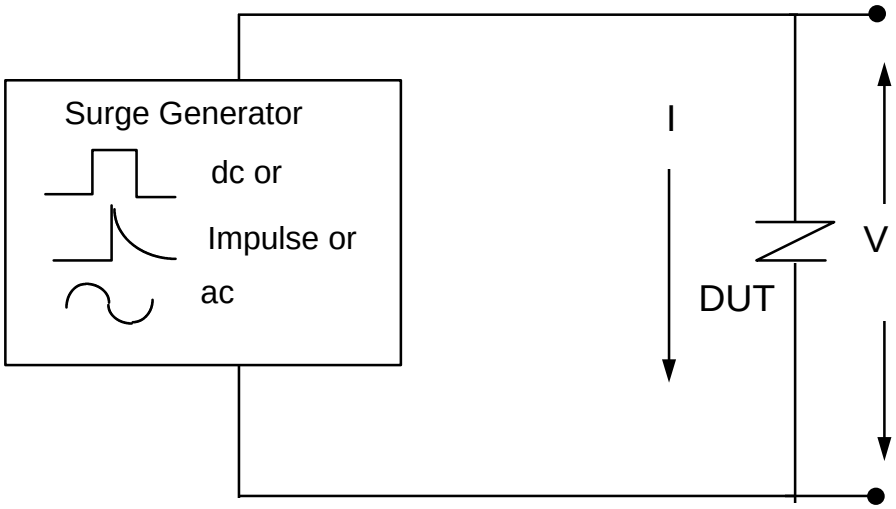


Figure 34 — Single power source on-state voltage test

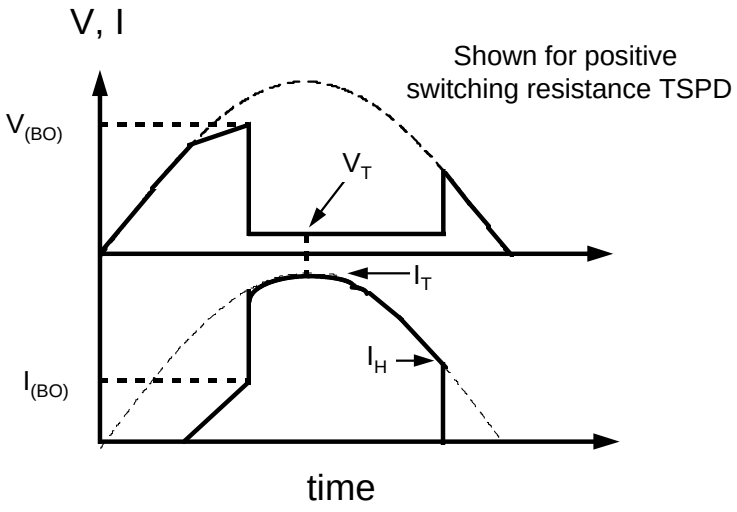


Figure 35 — AC on-state voltage measurement

5.8 Critical rate of rise of off-state voltage (dv/dt) test (cont'd)

5.8.1 Description (dv/dt) (cont'd)

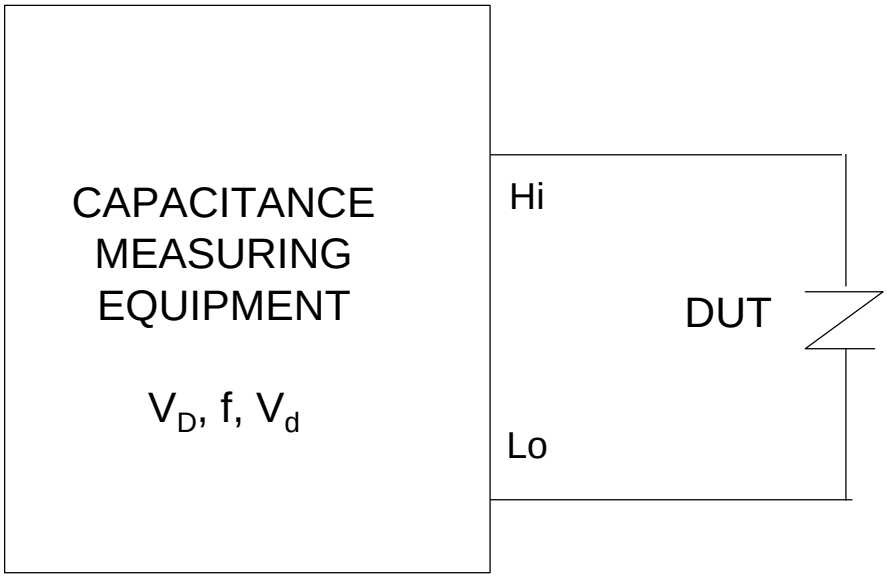


Figure 36 — Capacitance measurement circuit

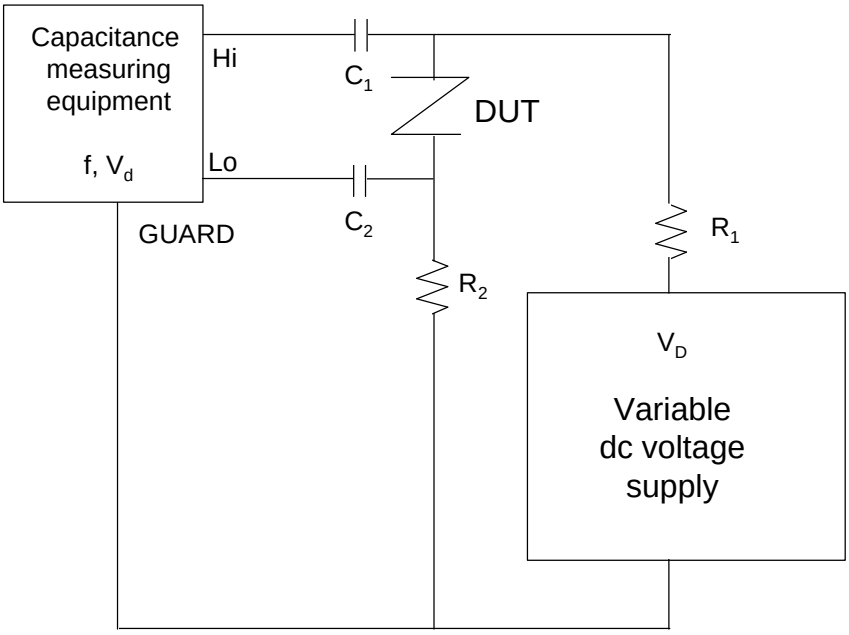


Figure 37 — Capacitance measurement with external dc voltage bias

5.8 Critical rate of rise of off-state voltage (dv/dt) test (cont'd)

5.8.1 Description (dv/dt) (cont'd)

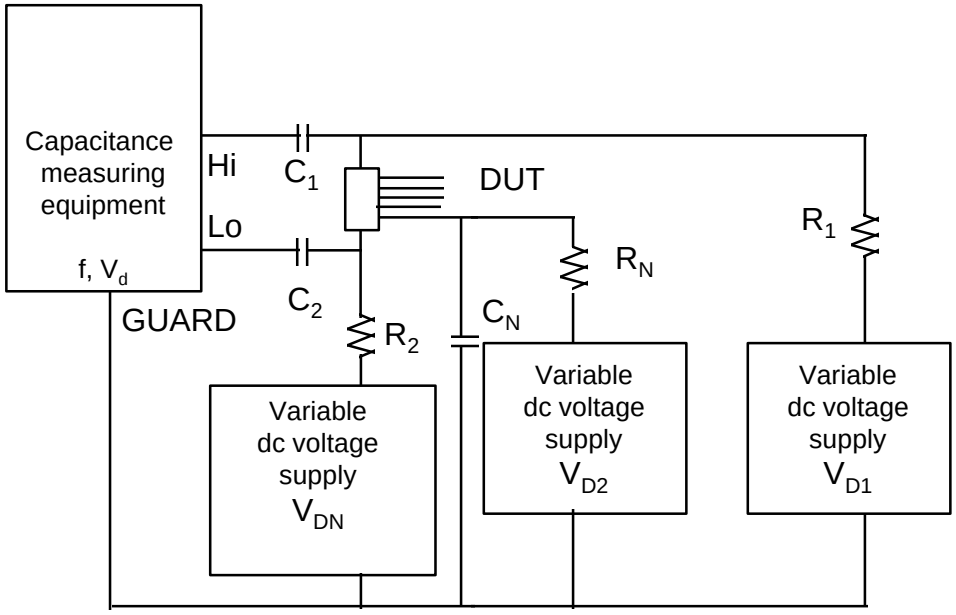


Figure 38 — Multi-terminal device capacitance measurement circuit

5.8.2 Test method (dv/dt)

The test applies a specified rate of voltage rise, beginning at zero volts and ending below the breakover voltage, across the principal device terminals at the specified rate and peak voltage. The defined values are for the principal voltage instead of the open-circuit voltage used with other tests. The test applies only to switching quadrants. Pulse duration shall be 50 microseconds minimum. Gate termination values shall be specified for gated devices. The applied voltage may be an exponential waveshape or a linear ramp. When the wave is exponential, the voltage rises to 63.2 percent of the peak in a time constant (see figure 39). The rate of rise is $(0.632*V_{PK})/\tau$. The rate of rise for a linear wave is $(0.8*V_{PK})/(t_2-t_1)$. At time t_2, the voltage is 90 percent of the peak. The voltage is 10 percent of the peak at t_1. Figure 40 illustrates the linear test waveform. Figures 41 and 42 show simplified test circuits. An RC charging circuit forms the basis of the exponential test method. The linear test method uses a constant current source to charge a capacitor and cause a linear rate of rise. R_1 and C shall be selected so that voltage-dependent device capacitance and wiring effects do not cause excessive wave distortion. R_2 prevents damage to the device under test if turn-on occurs. Switch S_2 initializes the capacitor voltage to 0 V at the start of the test. S_1 must switch quickly to prevent distortion of the early portion of the voltage wave. Elevated temperatures increase the chance of device turn-on. Measurement of dv/dt requires incrementing the applied rate of voltage rise until the device under test turns on. The device passes if it does not switch at the specified rate of rise.

5.8 Critical rate of rise of off-state voltage (dv/dt) test (cont'd)

5.8.2 Test method (dv/dt) (cont'd)

(1) Test conditions to be specified

(a) Peak main terminal voltage _____ V

(b) Case or lead temperature (T_C or T_L) _____ °C

(c) Waveshape (exponential or linear) _____

(d) Reference levels:

Exponential waveform: (recommended 0 to 63%) _____ %

Linear waveform: (recommended 10% to 90%) _____ %

parameters applicable only to triode devices

(e) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX} _____ V
Gate source resistance R_G _____ Ω

Gate bias resistance R_{GX} _____ Ω
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Test measurement

dv/dt _____ V/μs

5.9 Critical rate of rise of on-state current (di/dt)

5.9.1 Description (di/dt)

Impulses with fast rates of current rise (di/dt), such as those associated with close lightning strikes, can damage TSPDs although transient amplitudes and durations are within device ratings. This limitation results from switching speed, power dissipation, and the amount of time required for conduction to spread over the entire available chip area. If the rate of current inrush exceeds device capability, damage will result from localized heating. This test verifies the ability of the TSPD to survive a defined number of pulses at specified di/dt.

5.9 Critical rate of rise of on-state current (di/dt) (cont'd)

5.9.2 Test method (di/dt)

The DUT is connected in series with a surge generator that supplies the specified rates of current and voltage rise at defined peak current (figures 43, 44, and 45). The series CR_1L circuit shown in figure 44 may be used to generate the pulse when a commercial surge generator is not available. The damping factor determines the pulse waveshape. Components to suppress current wave undershoot and ringing (D_1 and S_2) may be used. The rate of current rise is proportional to the initial voltage on the capacitor and inversely proportional to the inductance.

Device types that are sensitive to dv/dt have their turn-on influenced by dv/dt induced Miller effect currents (see 3.8). R_2 (or the RC snubber if used in place of R_2) terminates the series CR_1L circuit to determine the voltage rate of rise. Pulse dv/dt is proportional to the voltage on the capacitor and the value of R_2 and is inversely proportional to the inductance. The initial voltage on the capacitor and the value of R_2 (or RC snubber if used in place of R_2) shall provide an open-circuit voltage greater than the TSPD breakover voltage.

The suggested value of peak current is the same as that for the I_{PPS} test. The surge duration should not be longer than that used for I_{PPS} testing. These surges shall be applied at a sufficiently low duty factor to prevent case heating. Low temperatures often cause the greatest stress because of reduced DUT switching speed.

This test is similar to the I_{PPS} test. However, it applies to the current through the DUT and the voltage across it, instead of the short-circuit current and open-circuit voltage of the generator. The test applies to each quadrant of operation where switching occurs. Gate termination conditions shall be specified for gated device types.

(1) Test conditions to be specified

(a) Rate of current rise (di/dt, 10 to 90% of the principal current) _____ A/μs

(b) Peak current _____ A

(c) Rate of voltage rise (dv/dt, 10 to 90% of the principal voltage) _____ V/μs

(d) Case or lead temperature (T_C or T_L) _____ °C

(e) Number of pulses _____ trials

5.9 Critical rate of rise of on-state current (di/dt) (cont'd)

5.9.2 Test method (di/dt) (cont'd)

parameters applicable only to triode devices

(f) Gate bias conditions (indicate the terminals the bias circuit will be applied across, e.g., gate to cathode (GK), gate to MT1 (GMT1), etc.)

Gate source voltage V_{GX}___ _____ V
Gate source resistance R_G___ _____ Ω

Gate bias resistance R_{GX}___ _____ Ω
or:
Gate decoupling capacitor (C_G) _____ nF
or:
Gate open-circuited

NOTE — Subscript "X" represents K, MT1, etc.

(2) Post test measurements

The device shall not fail any of its specified characteristics or exhibit shifts outside specified limits.

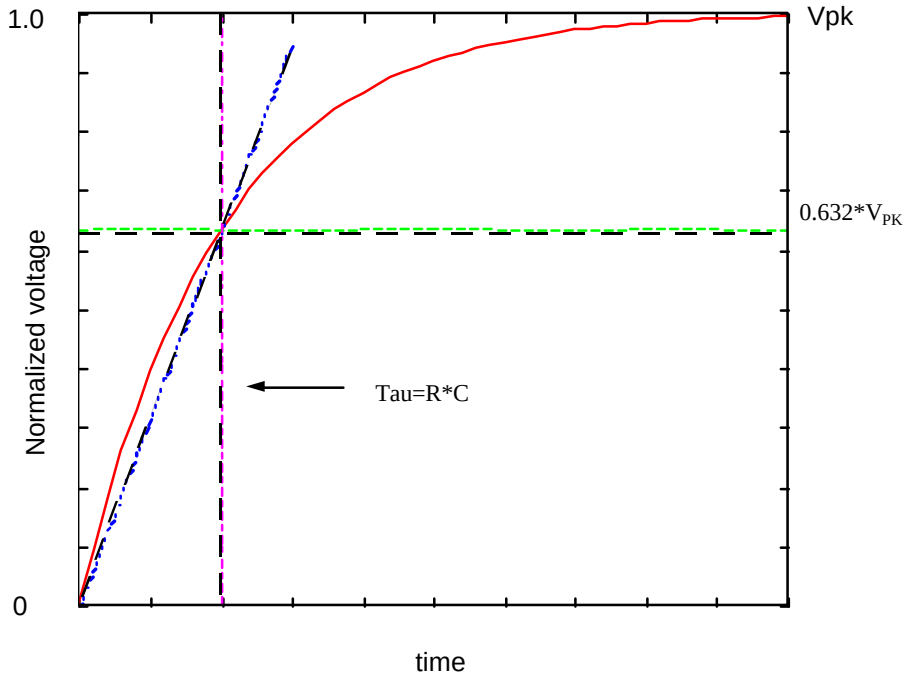


Figure 39 — dv/dt test voltage waveform (exponential waveform)

5.9 Critical rate of rise of on-state current (di/dt) (cont'd)

5.9.2 Test method (di/dt) (cont'd)

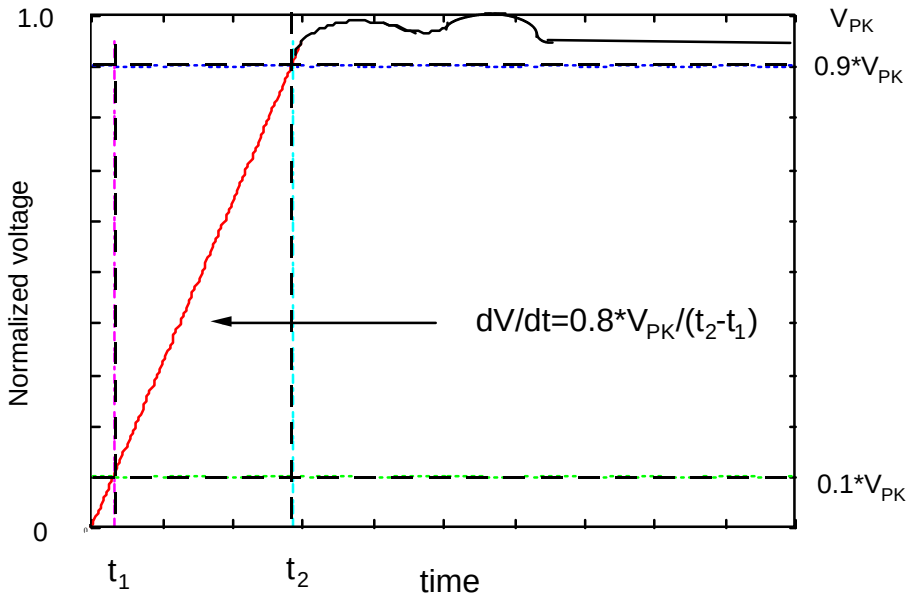


Figure 40 — dv/dt test voltage waveform (linear waveform)

5.10 Peak forward recovery voltage (V_{FRM}) test

5.10.1 Description (V_{FRM})

This test applies only to forward-conducting device types in their forward-conducting quadrants of operation. An overshoot voltage occurs when a current with high di/dt flows into the diode portion of a TSPD. This voltage results from carrier transit time, and the lenght of time to set up carrier gradients and conductivity modulate the diode. It can momentarily be much higher than the static on-state forward voltage. Excessive overshoot voltage can cause damage to protected circuits.

5.10 Peak forward recovery voltage (V_{FRM}) test (cont'd)

5.10.1 Description (V_{FRM}) (cont'd)

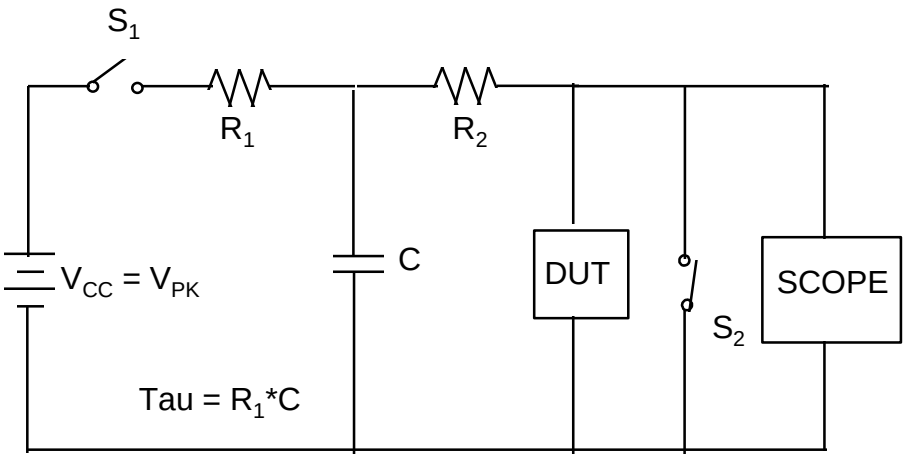


Figure 41 — Simplified exponential dv/dt test circuit

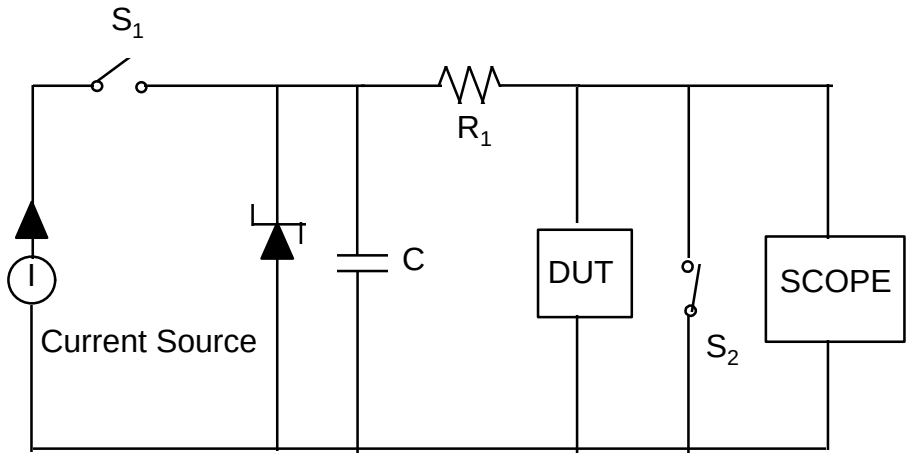


Figure 42 — Simplified linear dv/dt test circuit

5.10 Peak forward recovery voltage (V_{FRM}) test (cont'd)

5.10.2 Test method (V_{FRM})

The device is connected to a surge generator providing the specified peak current and di/dt. The open-circuit voltage shall be sufficient to provide correct values of V_{FRM}. A minimum of 5 times the expected V_{FRM} is recommended. The pulse duration shall be sufficiently short to prevent damage to the DUT. If the waveform generator provides a standard impulse, such as described in 1.4.8, its characteristics shall be described. Measurements of the current through and the voltage across the device under test are made. Figure 46 shows example test waveforms. The test circuit is like that shown in figures 43 or 44 for di/dt. The TSPD is connected in the polarity causing the device to operate in a forward-conducting quadrant.

(1) Test conditions to be specified

(a) Rate of current rise (di/dt, 10% to 90% of the principal current) _____ A/µs

(b) Peak current _____ A

(c) Case or lead temperature (T_C or T_L) _____ °C

additional parameters applicable to tests using standard impulse waveforms

(d) Virtual front time (short-circuit current wave, figure 11) _____ µs

(e) Duration (short-circuit current wave, figure 11) _____ µs

(f) Virtual front time (open-circuit voltage wave, figure 12) _____ µs

(g) Duration (open-circuit voltage wave, figure 12) _____ µs

(2) Post test measurement

Peak forward recovery voltage (V_{FRM}) _____ V

5.10 Peak forward recovery voltage (V_{FRM}) test (cont'd)

5.10.2 Test method (V_{FRM}) (cont'd)

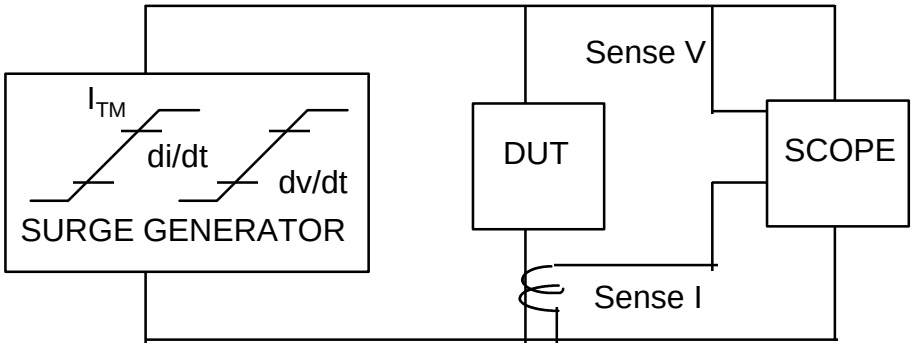


Figure 43 — di/dt test circuit

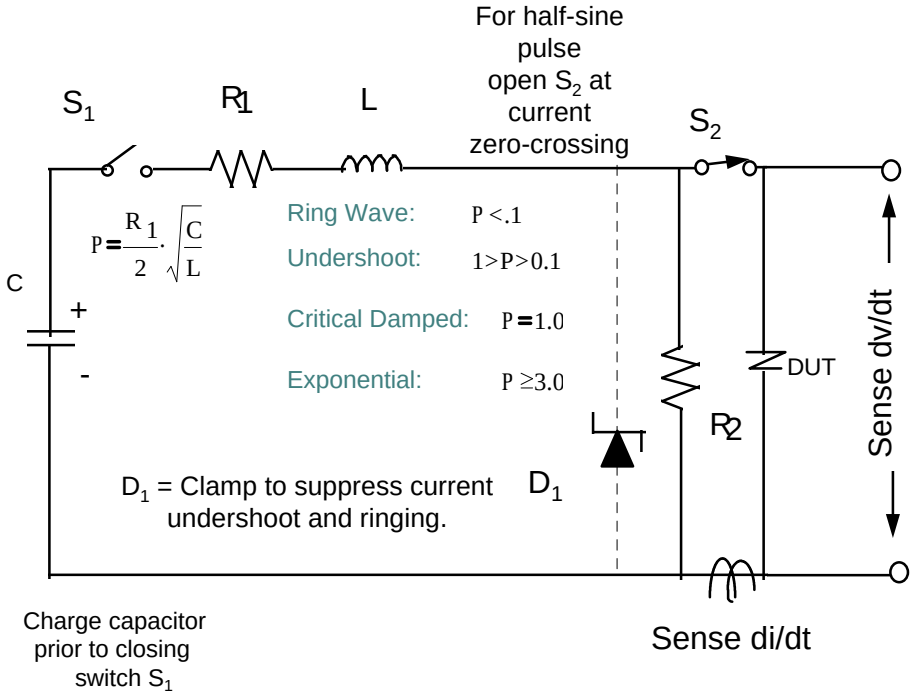


Figure 44 — Surge generator for di/dt test

5.10 Peak forward recovery voltage (V_{FRM}) test (cont'd)

5.10.2 Test method (V_{FRM}) (cont'd)

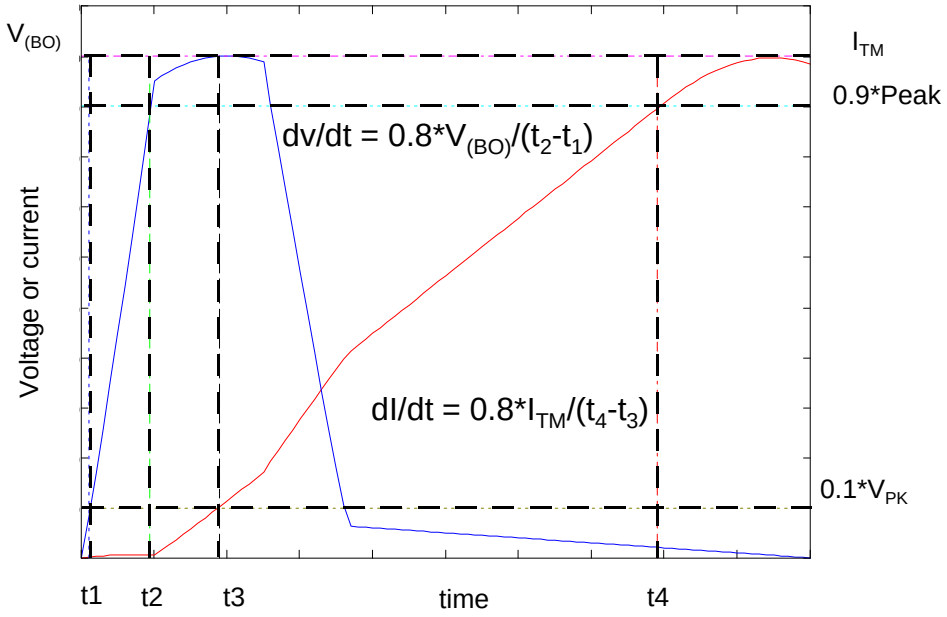


Figure 45 — di/dt test waveforms

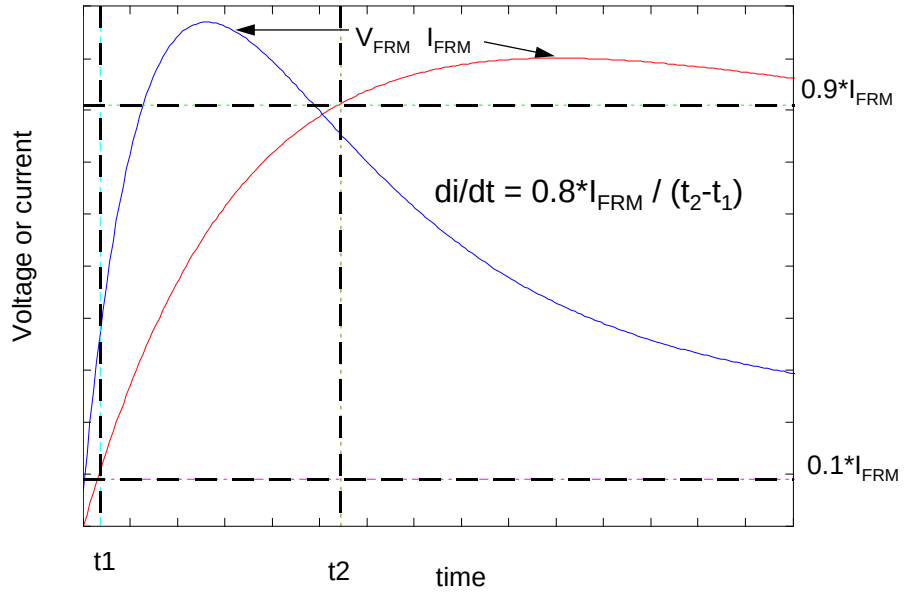
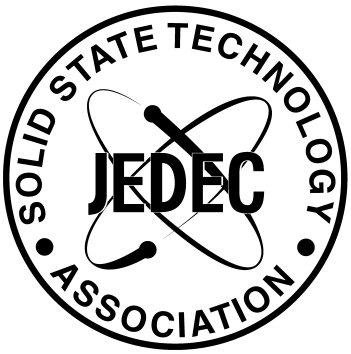


Figure 46 — Peak forward recovery voltage (V_{FRM}) waveforms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