JEDEC STANDARD

Definition of the SSTUB32868 Registered Buffer with Parity for 2R x4 DDR2 RDIMM Applications

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DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2R x4 DDR2 RDIMM APPLICATIONS

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DEFINITION OF THE SSTUB32868 1.8-V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-07-17, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications.

The purpose is to provide a standard for the SSTUB32868 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUB32868 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 28-bit 1:2 configurable registered buffer is designed for 1.7 V to 1.9 V V_{DD} operation.

All inputs are compatible with the JEDEC standard for SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset ($\overline{\text{RESET}}$) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for un-terminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error ($\overline{\text{QERR}}$) output.

The SSTUB32868 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and un-driven (floating) data, clock, and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are forced low except $\overline{\text{QERR}}$. The LVCMOS $\overline{\text{RESET}}$ and C inputs always must be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be ensured between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

2.1 Description (cont'd)

As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design of the SSTUB32868 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ must be held high, DODT0 and DODT1, DCKE0, and DCKE1 must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{\text{RESET}}$.

The SSTUB32868 includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. The corresponding $\overline{\text{QERR}}$ output signal for the data inputs is generated two clock cycles after the data, to which the $\overline{\text{QERR}}$ signal applies, is registered.

The SSTUB32868 accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1-D5, D7, D9-D12, D17-D28 when C = 0; or D1-D12, D17-D20, D22, D24-D28 when C = 1) and indicates whether a parity error has occurred on the open-drain $\overline{\text{QERR}}$ pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state.

If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low. If two or more consecutive parity errors occur, the $\overline{\text{QERR}}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{\text{RESET}}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power (LPM) and the $\overline{\text{QERR}}$ output is driven low, then it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) are not included in the parity check computation.

The parity error output $\overline{\text{QERR}}$ will be reset to high by $\overline{\text{RESET}}$ transitioning low and will not be decoded until after $\overline{\text{RESET}}$ goes high and $\overline{\text{DCS0}}$ and/or $\overline{\text{DCS1}}$ are asserted low. CSGEN does not affect $\overline{\text{QERR}}$ operation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hard-wired to a valid low or high level to configure the register in the desired mode.

The device also supports low-power active operation by monitoring both system chip select ($\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, $\overline{\text{DCS0}}$, and $\overline{\text{DCS1}}$ inputs are high. If CSGEN, $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ input is low, the Qn outputs will function normally. Also, if both $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ inputs are high, the device will gate the $\overline{\text{QERR}}$ output from changing states. If either $\overline{\text{DCS0}}$ or $\overline{\text{DCS1}}$ is low, the $\overline{\text{QERR}}$ output will function normally. The RESET input has priority over the $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ control and when driven low will force the Qn outputs low, and the $\overline{\text{QERR}}$ output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ would be the same as for the other D data inputs. To control the low-power mode with $\overline{\text{DCS0}}$ and $\overline{\text{DCS1}}$ only, then the CSGEN input should be pulled up to V_{DD} through a pull-up resistor.

The two V_{REF} pins (A1 and V1) are connected together internally by approximately 150 Ω. However, it is necessary to connect only one of the two V_{REF} pins to the external V_{REF} power supply. An unused V_{REF} pin should be terminated with a V_{REF} coupling capacitor.

2.2 176-ball TFBGA (MO-246)

Package options include 176-ball TFBGA (MO-246 version B).

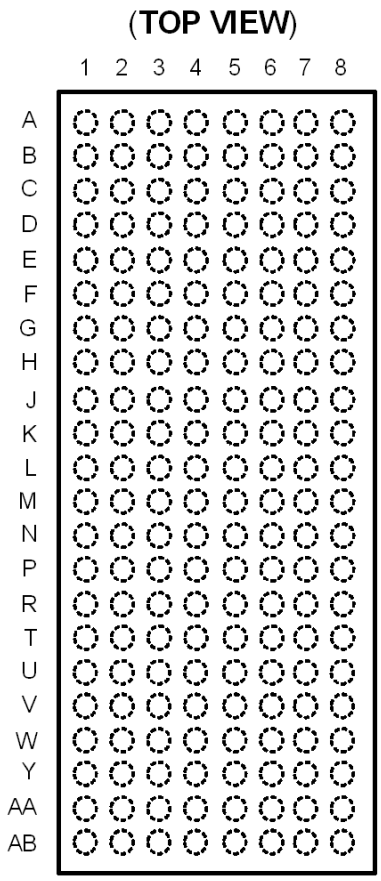


Figure 1 — Pinout Configuration

NOTE 1 8 x 22 array, 6.0 x 15.0 mm body size, 0.65 mm pitch. Diagram is for reference only. See MO-246 for detailed package specification.

2.3 Pinout Top View for 176-ball TFBGA

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A QCKE0A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B (QCKE1B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B (QCKE0B)
J	$\overline{DCS1}$	$\overline{QCS1A}$	GND	GND	GND	GND	Q10B	Q9B
K	$\overline{DCS0}$	$\overline{QCS0A}$	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B ($\overline{QCS0B}$)	Q13B ($\overline{QCS1B}$)
M	$\overline{CK}$	$\overline{RESET}$	$\overline{QERR}$	V_{DD}	V_{DD}	V_{DD}	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (Q0DT1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	VDD	Q28A	Q28B

Figure 2 — 1:2 Register A (C=0)

NOTE "NC" denotes no internal connection.

2.3 Pinout Top View for 176-ball TFBGA (cont'd)

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B
J	D13 (DODT1)	Q13A (QODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 (DODT0)	Q14A (QODT0A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	$\overline{CK}$	$\overline{RESET}$	$\overline{QERR}$	V_{DD}	V_{DD}	V_{DD}	Q15B ($\overline{QCS0B}$)	Q16B ($\overline{QCS1B}$)
N	D15 ($\overline{DCS0}$)	Q15A ($\overline{QCS0A}$)	GND	GND	GND	GND	Q17B	Q18B
P	D16 ($\overline{DCS1}$)	Q16A ($\overline{QCS1A}$)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	VDD	Q28A	Q28B

Figure 3 — 1:2 Register B (C=1)

NOTE "NC" denotes no internal connection.

2.4 Terminal Functions

Table 1 — Terminal Functions

Terminal Name	Description	Electrical Characteristics
GND	Ground	Ground input
V_{DD}	Power supply voltage	1.8 V nominal
V_{REF}	Input reference voltage	0.9 V nominal
CK	Positive main clock input	Differential input
$\overline{CK}$	Negative main clock input	Differential input
C	Configuration control inputs - Register A or Register B	LVCMOS inputs
$\overline{RESET}$	Asynchronous reset input – resets registers and disables V_{REF} data and clock differential-input receivers	LVCMOS input
CSGEN	Chip select gate enable – When high, D1-D28† inputs will be latched only when at least one chip select input is low during the rising edge of the clock. When low, the D1-D28† inputs will be latched and re-driven on every rising edge of the clock.	LVCMOS input
D1–D28	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$	SSTL_18 input
$\overline{DCS0}$, $\overline{DCS1}$	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to re-drive all D inputs (CSGEN high) only when at least one chip select input is low. If CSGEN, $\overline{DCS0}$, and $\overline{DCS1}$ inputs are high, D1–D28 inputs will be disabled [1].	SSTL_18 input
DODT0, DODT1	The outputs of this register bit will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	SSTL_18 input
DCKE0, DCKE1	The outputs of this register bit will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	SSTL_18 input
PAR_IN	Parity input - arrives one clock cycle after the corresponding data input.	SSTL_18 input
Q1–Q28[2]	Data outputs that are suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8 V CMOS outputs
$\overline{QCS0}$, $\overline{QCS1}$	Data output that will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8 V CMOS output
QODT0, QODT1	Data output that will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8 V CMOS output
QCKE0, QCKE1	Data output that will not be suspended by the $\overline{DC0}$ and $\overline{DCS1}$ control.	1.8 V CMOS output
$\overline{QERR}$	Output error bit - generated one clock cycle after the corresponding data output	Open-drain output
NC	No internal connection	

NOTE 1 Data inputs = D1-D5, D7, D9-D12, D17-D28 when C=0
Data inputs = D1-D12, D17-D20, D22, D24-D28 when C=1
NOTE 2 Data outputs = Q1-Q5, Q7, Q9-Q12, Q17-Q28 when C=0
Data outputs = Q1-Q12, Q17-Q20, Q22, Q24-Q28 when C=1

2.5 Function Table

Table 2 — Function Table (Each Flip Flop)

Inputs							Outputs			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGEN	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

2.5 Function Table (cont'd)

Table 3 — Parity and Standby Function Table

Inputs							Output
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CK	$\overline{\text{CK}}$	Σ of inputs = H (D1-D28)	PAR_IN[1]	$\overline{\text{QERR}}$[2]
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{\text{QERR}}_0$[3]
H	X	X	L or H	L or H	X	X	$\overline{\text{QERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	H

NOTE 1 PAR_IN arrives one clock cycle after the data to which it applies

NOTE 2 This transition assumes $\overline{\text{QERR}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{QERR}}$ is low, it stays latched low for two clock cycles or until $\overline{\text{RESET}}$ is driven low

NOTE 3 If $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, and CSGEN are driven high, the device is placed in low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{\text{QERR}}$ output is driven low, it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low.

2.6 Logic Diagram

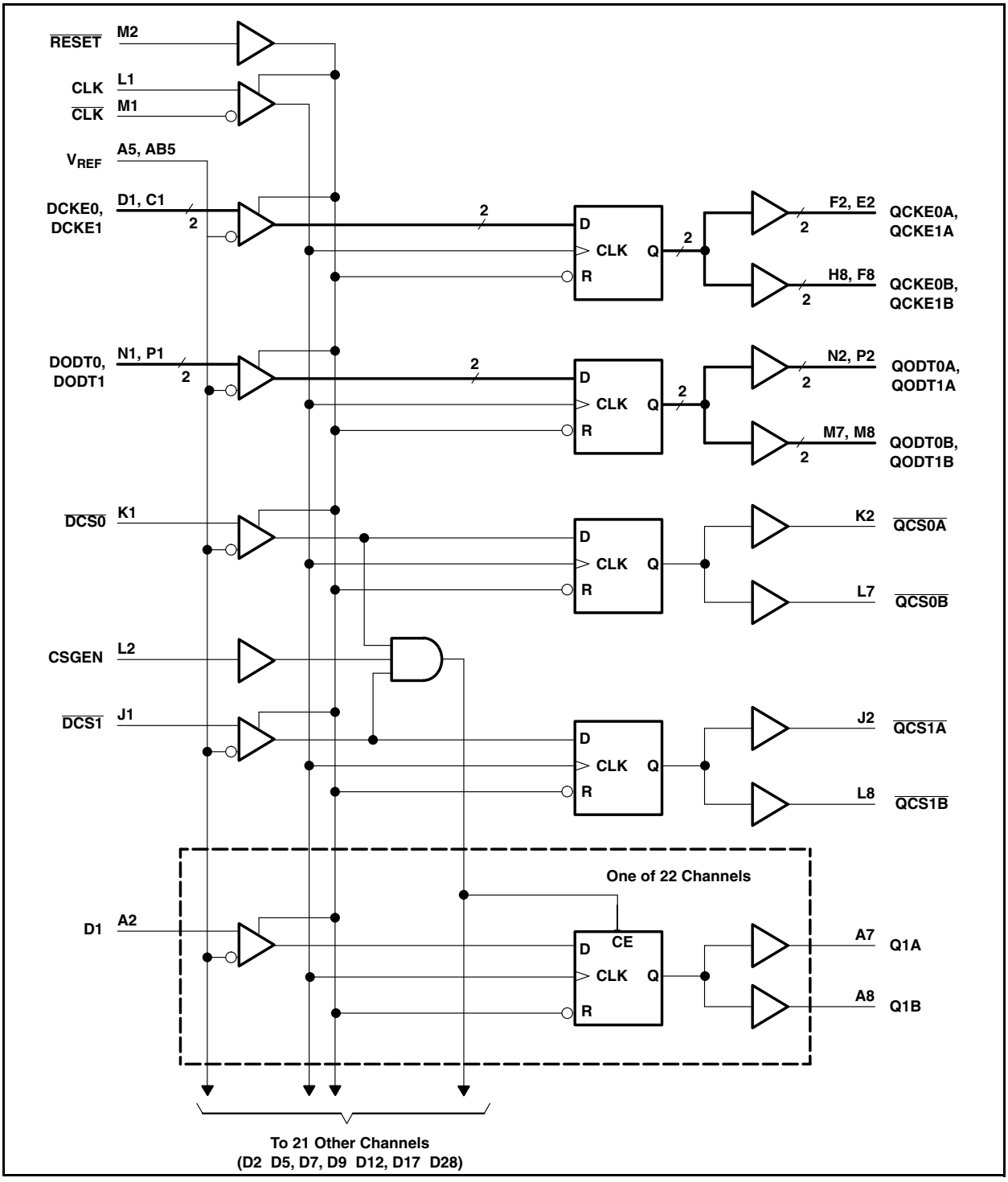


Figure 4 — Logic Diagram Register-A Configuration with C=0 (Positive Logic)

2.6 Logic Diagram (cont'd)

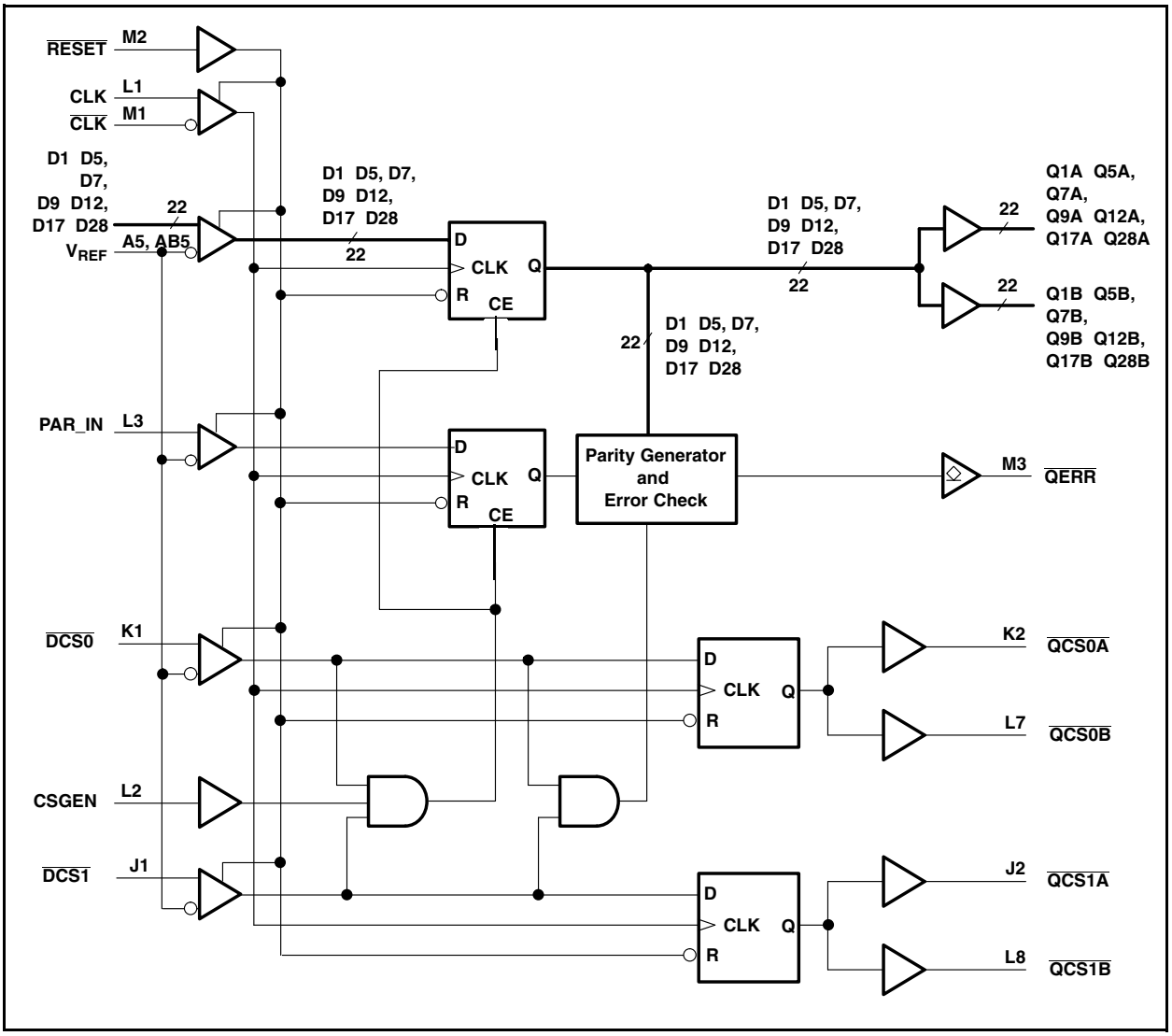


Figure 5 — Parity Logic Diagram for Register-A Configuration (Positive Logic); C=0

2.6 Logic Diagram (cont'd)

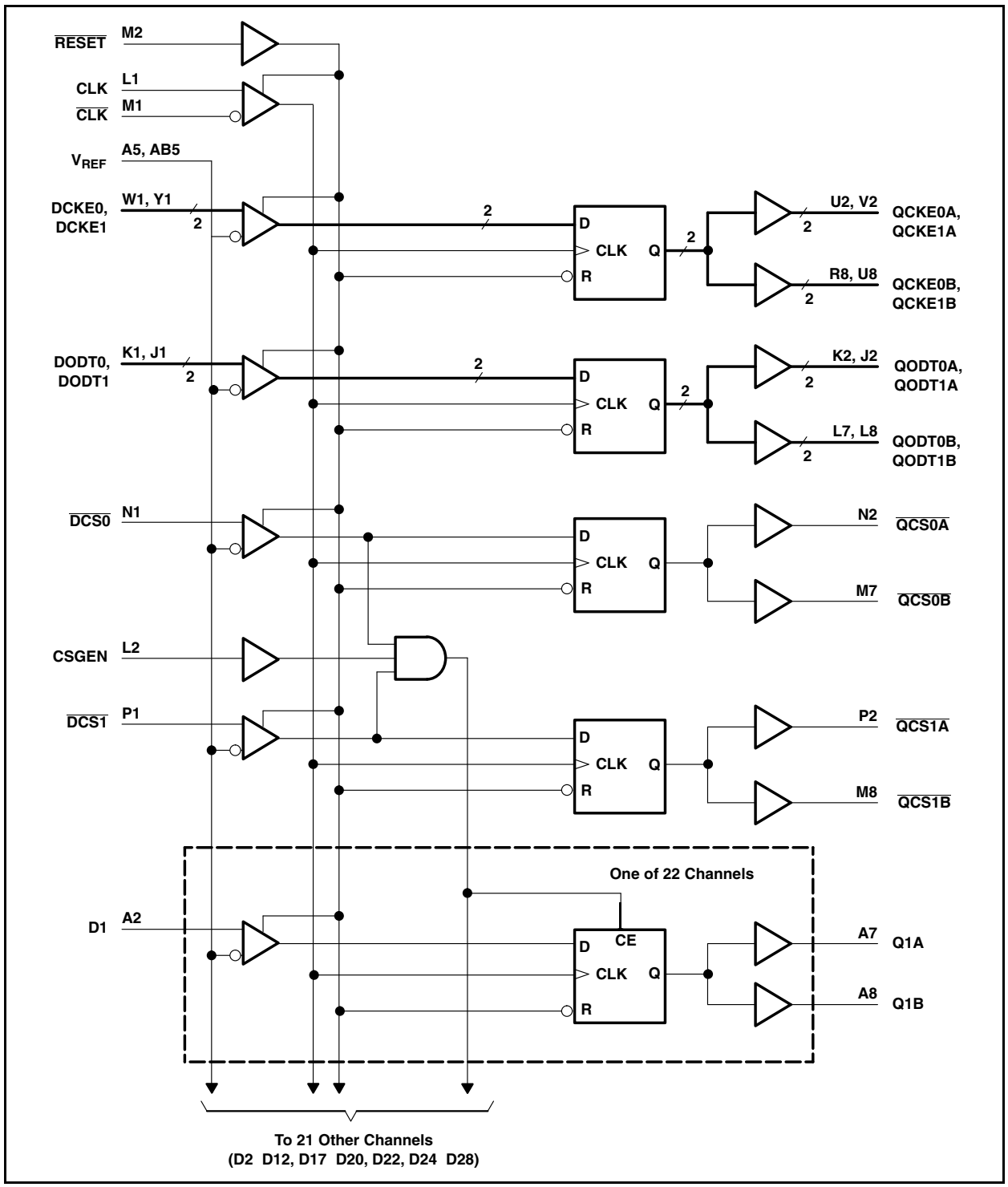


Figure 6 — Logic Diagram Register-B Configuration with C=1 (Positive Logic)

2.6 Logic Diagram (cont'd)

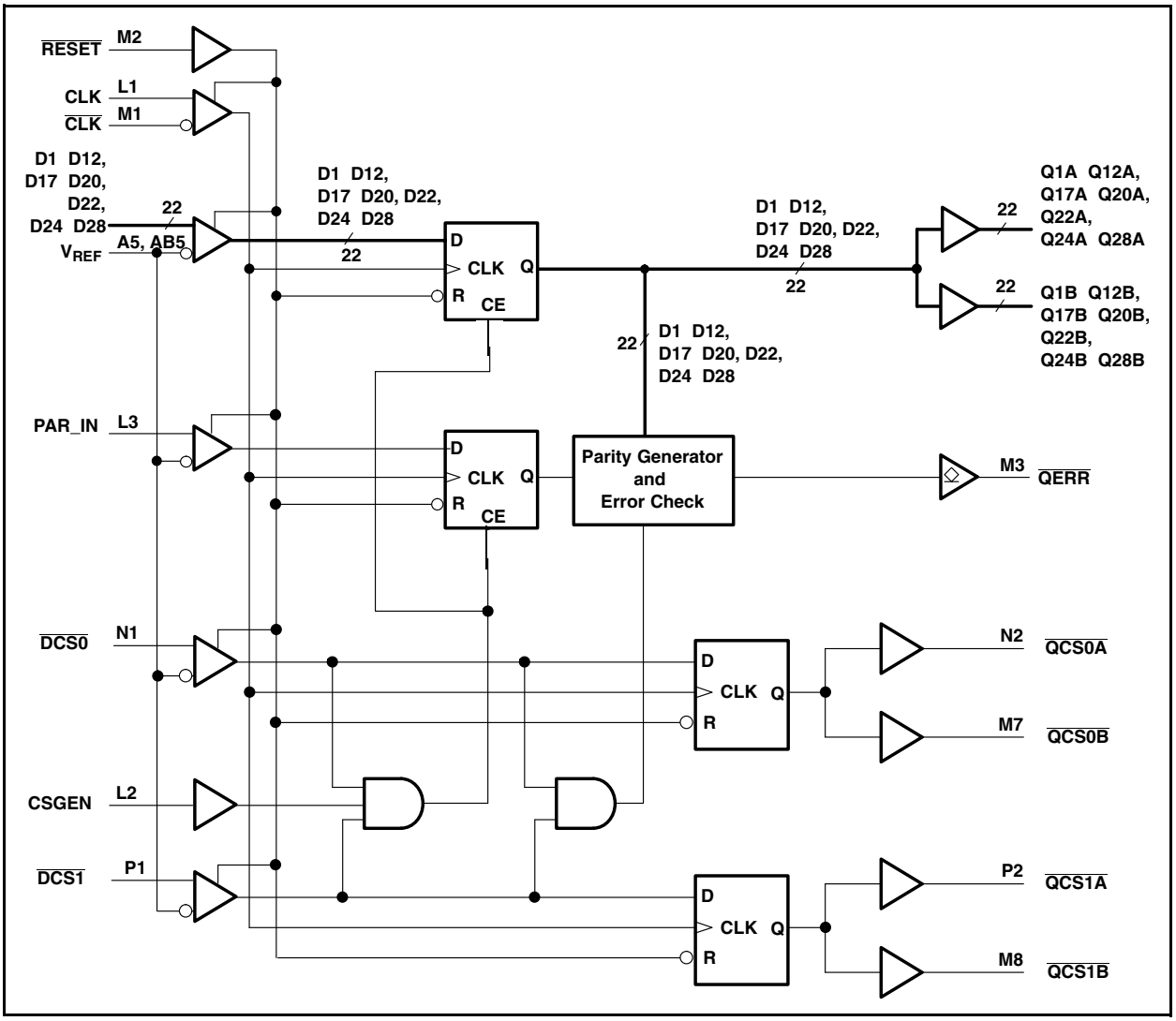


Figure 7 — Parity Logic Diagram for Register-B Configuration (Positive Logic); C=1

2.7 Register Timing

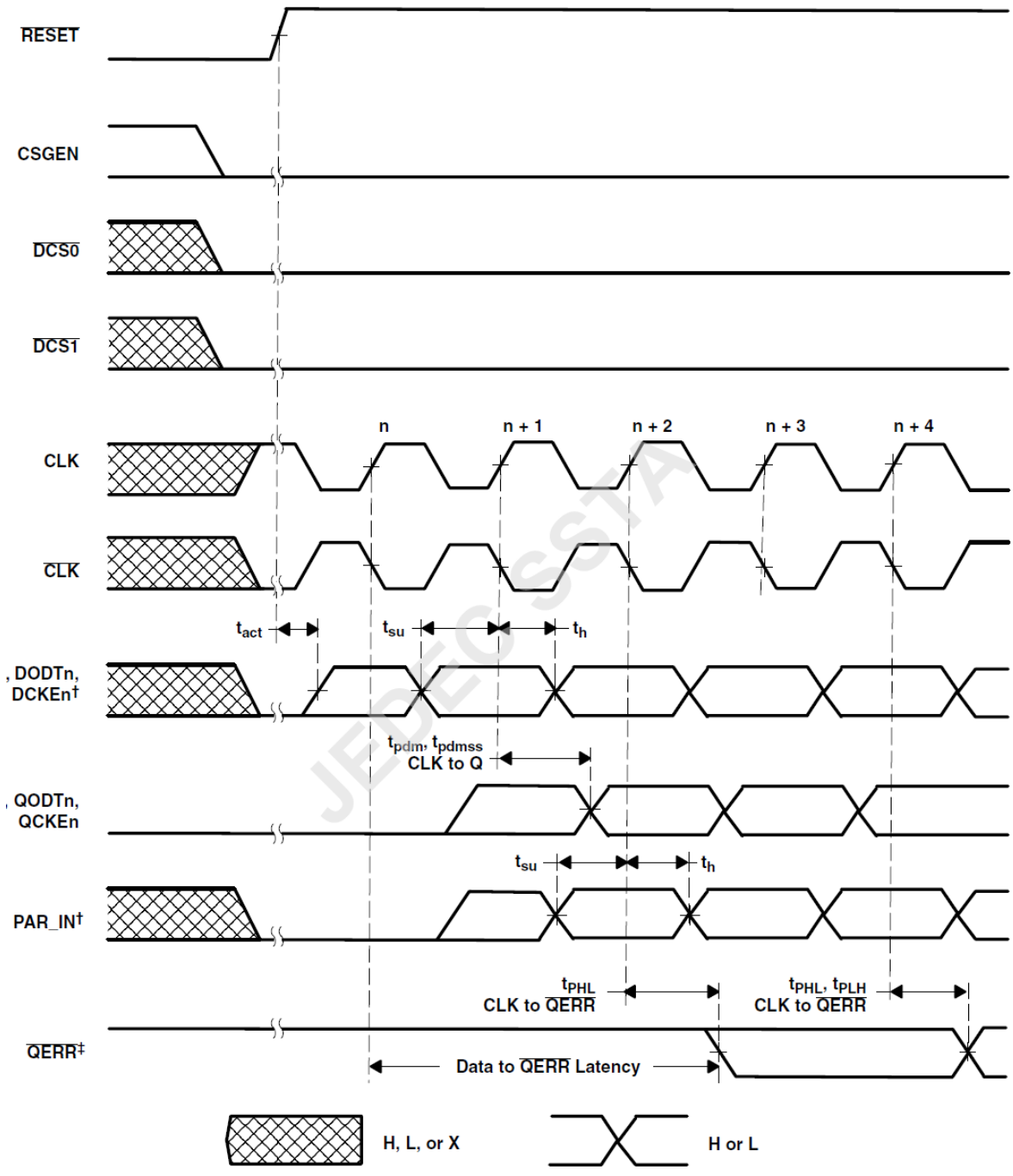


Figure 8 — Timing Diagram During Start-up ($\overline{\text{RESET}}$ Switches from L to H)

NOTE † After $\overline{\text{RESET}}$ is switched from low to high, if $\overline{\text{DCS}}$0 or $\overline{\text{DCS}}$1 are held Low than all data and PAR_IN input signals must be held Low for a minimum time of t_{ACT} max to avoid false error. If $\overline{\text{DCS}}$0 or $\overline{\text{DCS}}$1 are held high than all data and PAR_IN inputs signals must be held at valid logic levels for a minimum time of t_{ACT} max, to avoid false error.

NOTE ‡ If the data is clocked in on the n clock pulse, and PAR_IN is clocked in at n+1, the $\overline{\text{QERR}}$ output signal will be produced on the n+2 clock pulse and it will be valid on the n+3 clock pulse.

2.7 Register Timing (cont'd)

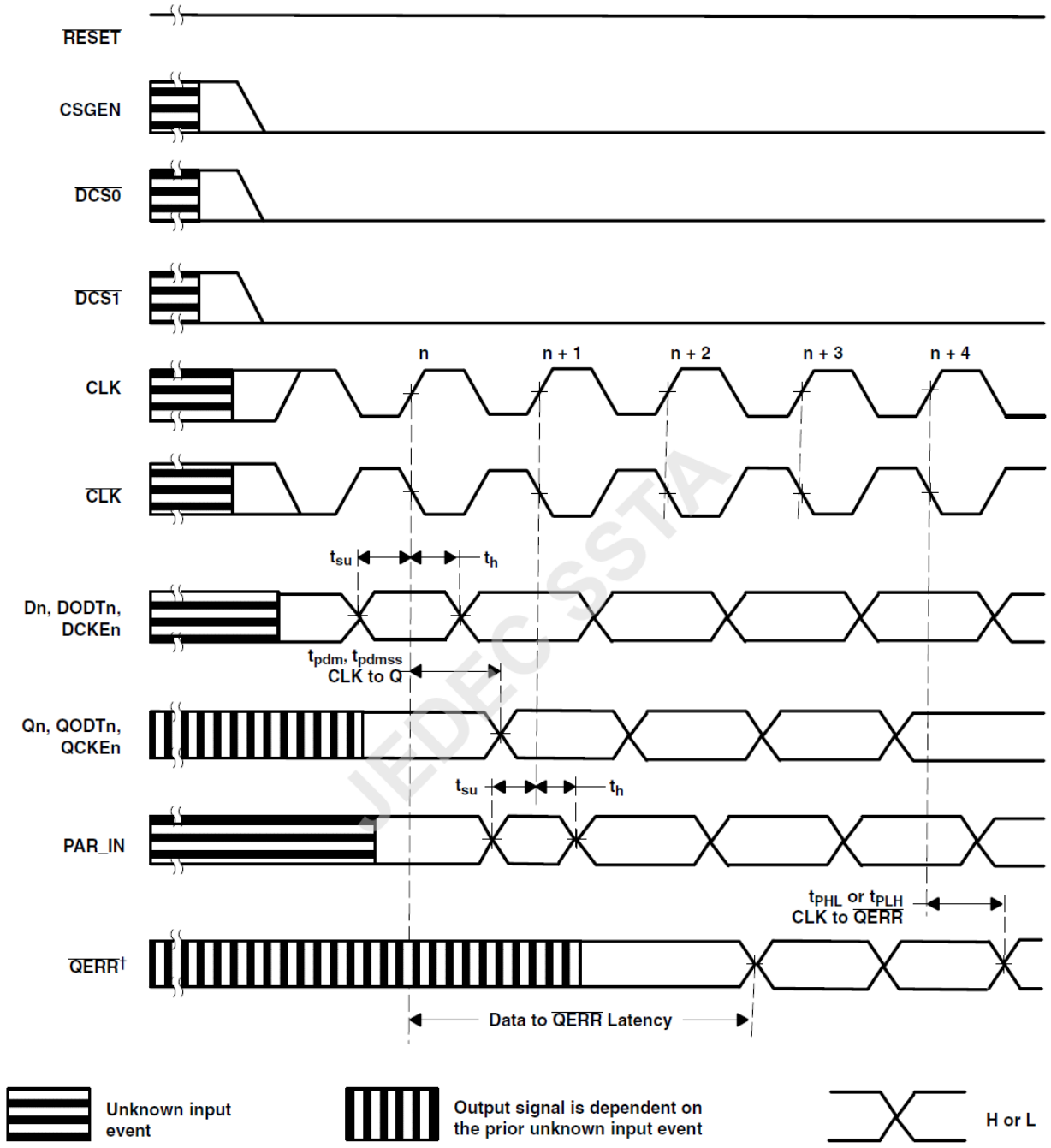


Figure 9 — Timing Diagram During Normal Operation ($\overline{\text{RESET}}$ = H)

NOTE † If the data is clocked in on the n clock pulse, and PAR_IN is clocked in at n+1, the $\overline{\text{QERR}}$ output signal will be generated on the n + 2 clock pulse and it will be valid on the n + 3 clock pulse. If an error occurs and the $\overline{\text{QERR}}$ output is driven low, it stays low for a minimum of two clock cycles or until $\overline{\text{RESET}}$ is driven low.

2.7 Register Timing (cont'd)

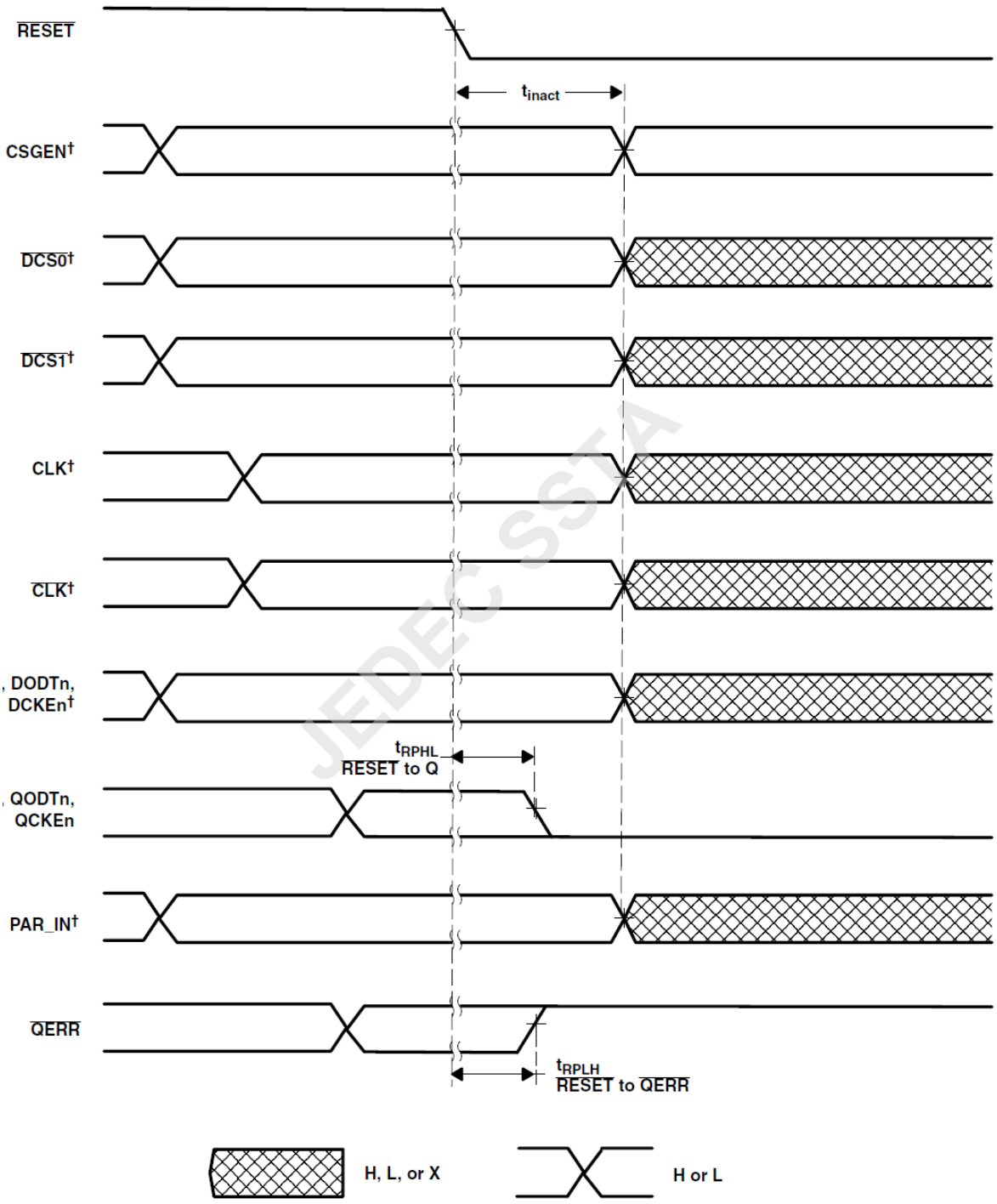


Figure 10 — Timing Diagram During Shutdown ($\overline{\text{RESET}}$ Switches from H to L)

NOTE † After $\overline{\text{RESET}}$ is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.

2.7 Register Timing (cont'd)

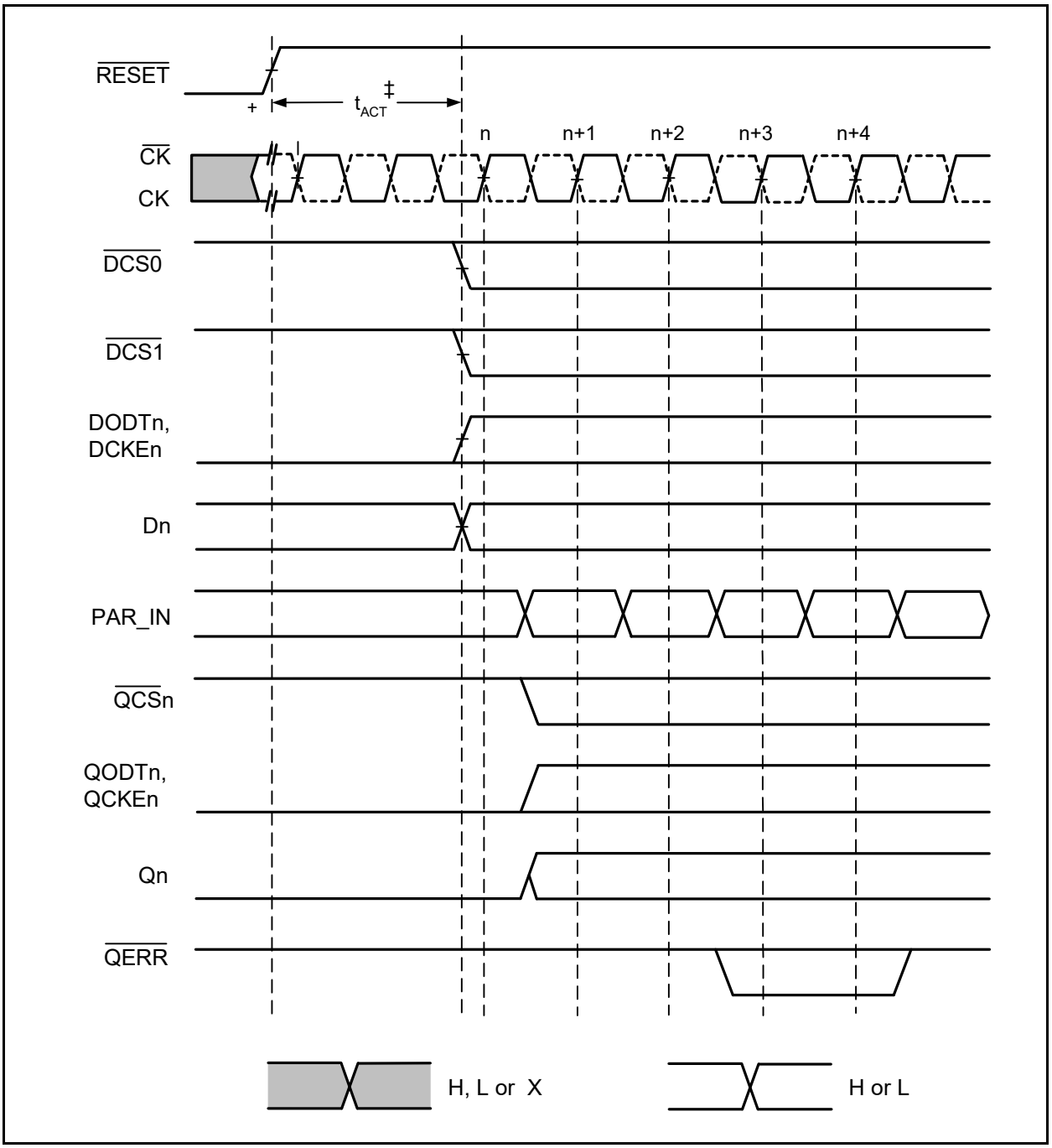


Figure 11 — Timing Diagram During Start-up when Data Inputs are LOW or HIGH (RESET Switches from L to H)

NOTE ‡ After RESET is switched from low to high, DCS0 and DSC1 must be held HIGH, DODT0, DODT1, DCKE0 and DCKE1 must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of t_{ACT} max.

2.7 Register Timing (cont'd

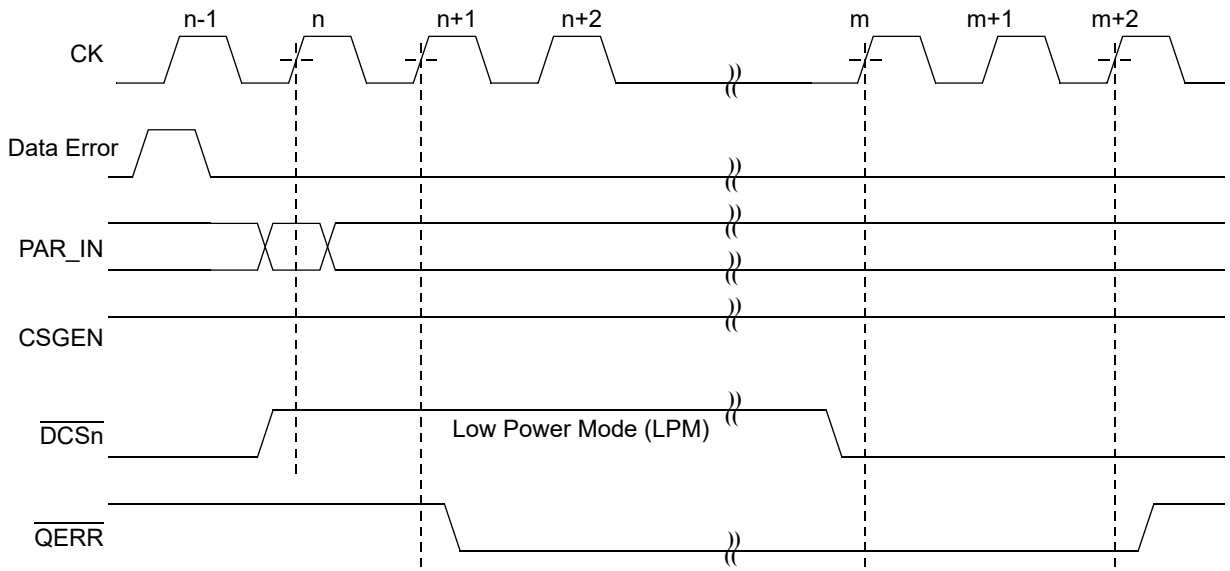


Figure 12 — Data Error Occurs at (n-1), LPM Occurs at (n)

2.8 Absolute Maximum Ratings

Table 4 — Absolute Maximum Ratings Over Operating Free-air Temperature Range (see NOTE 1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	+2.5	V
V_I	Receiver input voltage	(See Notes 2 and 3)	–0.5	+2.5	V
V_O	Driver output voltage	(See Notes 2 and 3)	–0.5	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$		±50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$		±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$		±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin			±100	mA
T_{stg}	Storage temperature		–65	+150	°C

NOTE 1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 2.5 V maximum.

2.9 Recommended Operating Conditions

Table 5 — Recommended Operating Conditions (see NOTE)

Symbol	Parameter		Min	Nom	Max	Unit
V_{DD}	Supply voltage		1.7	-	1.9	V
V_{REF}	Reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	Termination voltage		$V_{REF} - 40$ mV	V_{REF}	$V_{REF} + 40$ mV	V
V_I	Input voltage		0	-	V_{DD}	V
V_{IH}	AC HIGH-level input voltage	Data, DCKEn, DODTn, $\overline{DCSn}$, and PAR_IN inputs	$V_{REF} + 250$ mV	-	-	V
V_{IL}	AC LOW-level input voltage		-	-	$V_{REF} - 250$ mV	V
V_{IH}	DC HIGH-level input voltage		$V_{REF} + 125$ mV	-	-	V
V_{IL}	DC LOW-level input voltage		-	-	$V_{REF} - 125$ mV	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, CSGEN, and C	$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.35 \times V_{DD}$	V
V_{ICR}	Common-mode input voltage range	CK, $\overline{CK}$	0.675	-	1.125	V
V_{ID}	Differential input voltage		600	-	-	mV
I_{OH}	HIGH-level output current		-	-	-6	mA
I_{OL}	LOW-level output current		-	-	6	mA
I_{ERROL}	$\overline{QERR}$ LOW-level output current		25	-	-	mA
T_{amb}	Operating ambient temperature in free-air		0	-	+70	°C
NOTE	The $\overline{RESET}$, CSGEN, and C inputs of the device must be held at valid levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.					

2.10 DC Specifications

Table 6 — Electrical Characteristics over Recommended Operating Free-air Temperature Range

Symbol	Parameter	Test Conditions		V_{DD}	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = –6 mA		1.7 V	1.2	-	-	V
V_{OL}	Output LOW voltage	I_{OL} = 6 mA		1.7 V	-	-	0.5	V
V_{ERROL}	$\overline{QERR}$ Output LOW voltage	I_{ERROL} = 25 mA		1.7 V	-	-	0.5	V
I_I	Input current, all inputs	$V_I = V_{DD}$ or GND		1.9 V	-	-	±5	µA
I_{DD}	Static standby current	$\overline{RESET}$ = GND	$I_O = 0$	1.9 V	-	-	200	µA
	Static operating current	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$		1.9 V	-	-	80	mA
I_{DDD}	Dynamic operating current — clock only	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50%duty cycle.	$I_O = 0$	1.8 V	-	NOTE 1	-	µA/ MHz
	Dynamic operating current — per each data input, 1:1 mode	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.			-	NOTE 1	-	µA/ MHz
	Dynamic operating current — per each data input, 1:2 mode	$\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.			-	NOTE 1	-	µA/ MHz
C_i	Input capacitance, D_n, CSGEN, PAR_IN inputs	$V_I = V_{REF}$ ± 250 mV		1.8 V	2.5	-	4	pF
	Input capacitance, $\overline{DCS_n}$‡	$V_I = V_{REF}$ ± 250 mV			2.5	-	4	pF
	Input capacitance, CK and $\overline{CK}$ inputs‡	V_{ICR} = 0.9 V; $V_{I(PP)}$ = 600 mV			2	-	3	pF
	Input capacitance, $\overline{RESET}$ input	$V_I = V_{DD}$ or GND			NOTE 1	-	NOTE 1	pF

NOTE 1 The vendor must supply this value for full device description.

2.11 Timing Requirements

Table 7 — Timing Requirements Over Recommended Operating Free-air Temperature Range (See Figure 6)

Symbol	Parameter		Min	Max	Unit
f_{clock}	Clock frequency		-	410	MHz
t_W	Pulse duration, CK, $\overline{CK}$ HIGH or LOW		1	-	ns
t_{ACT}	Differential inputs active time (See Notes 1 and 2)		-	10	ns
t_{INACT}	Differential inputs inactive time (See Notes 1 and 3)		-	15	ns
t_{SU}	Setup time	$\overline{DCS0}$ before CK↑, $\overline{CK}$↓, $\overline{DCS1}$ and CSGEN high $\overline{DCS1}$ before CK↑, $\overline{CK}$↓, $\overline{DCS0}$ and CSGEN high	0.6	-	ns
	Setup time	$\overline{DCS0}$ before CK↑, $\overline{CK}$↓, $\overline{DCS1}$ low and CSGEN high or low $\overline{DCS1}$ before CK↑, $\overline{CK}$↓, $\overline{DCS0}$ low and CSGEN high or low	0.5	-	ns
	Setup time	DODTn, DCKEn, PAR_IN and data before CK↑, $\overline{CK}$↓	0.5	-	ns
t_H	Hold time	$\overline{DCSn}$, DODTn, DCKEn and data after CK↑, $\overline{CK}$↓	0.4	-	ns
	Hold time	PAR_IN after CK↑, $\overline{CK}$↓	0.4	-	ns
NOTE 1	This parameter is not necessarily production tested.				
NOTE 2	V_{REF} must be held at a valid input voltage level and data inputs must be held at valid logic levels for a minimum time of t_{ACT} (max) after $\overline{RESET}$ is taken high.				
NOTE 3	V_{REF}, Data and clock inputs must be held at valid voltage levels (not floating) a minimum time of t_{INACT} (max) after $\overline{RESET}$ is taken low.				

2.12 AC Specifications

Table 8 — Switching Characteristics over Recommended Operating Free-air Temperature Range (Unless Otherwise Noted) (see Clause 3.1)

Symbol	Parameter	Measurement Conditions	Min	Max	Unit
f_{MAX}	Maximum input clock frequency		410	-	MHz
t_{pdm}	Propagation delay, single bit switching	From CK↑ and $\overline{CK}$↓ to Qn (see Note 1)	1.1	1.5	ns
t_{PLH}	Low-to-high propagation delay	From CK↑ and $\overline{CK}$↓ to $\overline{QERR}$	1.2	3	ns
t_{PHL}	High-to-low propagation delay		1	2.4	ns
t_{pdmss}	Propagation delay, simultaneous switching	From CK↑ and $\overline{CK}$↓ to Qn (see Note 1)	-	1.6	ns
t_{RPHL}	High-to-low propagation delay	From $\overline{RESET}$↓ to Qn↓	-	3	ns
t_{RPLH}	Low-to-high propagation delay	From $\overline{RESET}$↓ to $\overline{QERR}$↑	-	3	ns
NOTE 1	Includes 350 ps of test-load transmission line delay.				

2.13 Output Buffer Characteristics

Table 9 — Output Edge Rates Over Recommended Operating Free-air Temperature Range (see Clause 3.2)

Symbol	Parameter	Measurement Conditions	Min	Max	Unit
dV/dt_r	rising edge slew rate	From 20% to 80%	1	4	V/ns
dV/dt_f	falling edge slew rate	From 80% to 20%	1	4	V/ns
dV/dt_Δ[1]	absolute difference between dV/dt_r and dV/dt_f	From 20% or 80% to 80% or 20%	-	1	V/ns
NOTE 1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).					

2.14 Output Buffer Overshoot/Undershoot

This register is - among other applications - intended for use in the JEDEC reference designs as defined in JESD21-C, DDR2 Registered DIMM Design Standard. It is designed and characterized to produce overshoots/undershoots less than indicated in the table below, to comply with DDR2 SDRAM overshoot/ undershoot requirements under worst case DRAM loading conditions (Min or Max), over DIMM operating conditions, and within the recommend operating conditions of the register listed in Table 5,

Table 10 — Output Overshoot/undershoot Over Recommended Operating Free-air Temperature Range

DIMM Design Specification	Reference Design	Speed Bin	Overshoot (above V_{DD}) Max[1]	Undershoot (below GND) Min[1]
e.g., DDR2 Registered DIMM Design Specification Rev 2.0	e.g. F0	e.g. PC2-4200	e.g. 0.5 V	e.g. -0.5 V
...	...	...	...	...
...	...	...	...	...
NOTE 1 This value is verified by design and characterization, and may not be subject to production test				

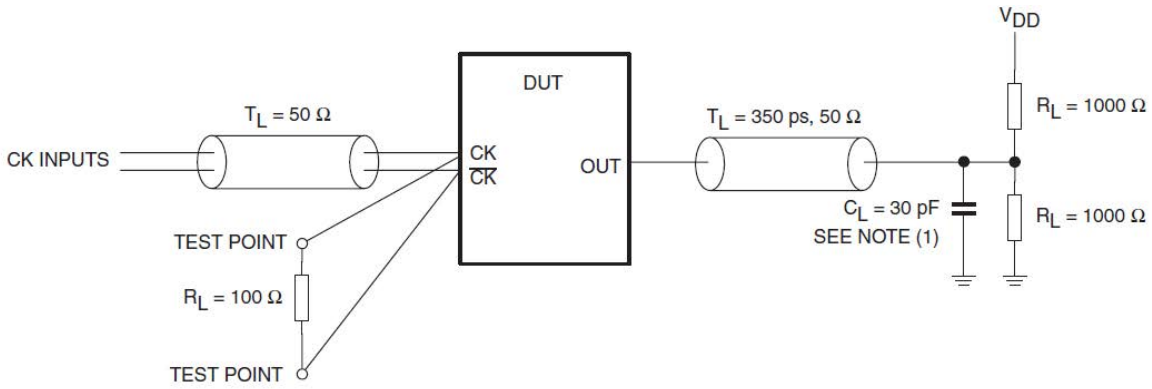
Register vendors are expected to supply the data in this table for the intended applications in their respective data sheets or in other suitable form.

3 Test Circuits and Switching Waveforms

3.1 Parameter Measurement Information for Data Output Load Circuit (V_{DD} = 1.8 V ± 0.1 V)

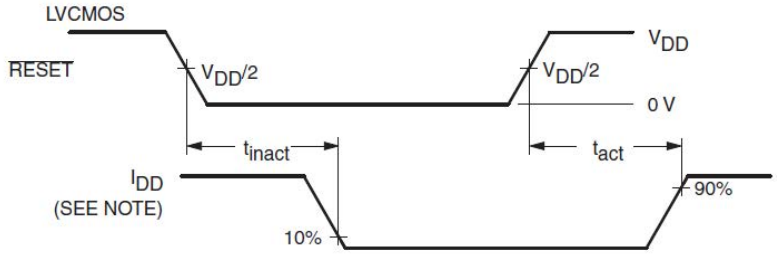
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



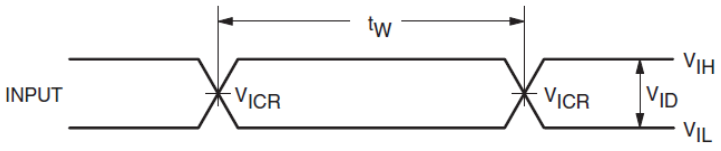
NOTE 1 C_L includes probe and jig capacitance.

Figure 13 — Load Circuit, Data Output Measurements



NOTE 1 I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

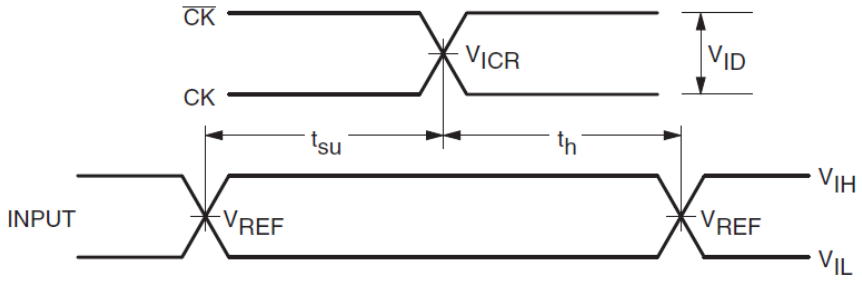
Figure 14 — Voltage and Current Waveforms; Inputs Active and Inactive Times



NOTE 1 V_{ID} = 600 mV
NOTE 2 $V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
NOTE 3 $V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

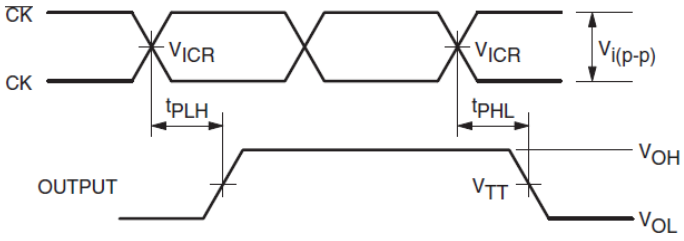
Figure 15 — Voltage Waveforms; Pulse Duration

3.1 Parameter Measurement Information (cont'd)



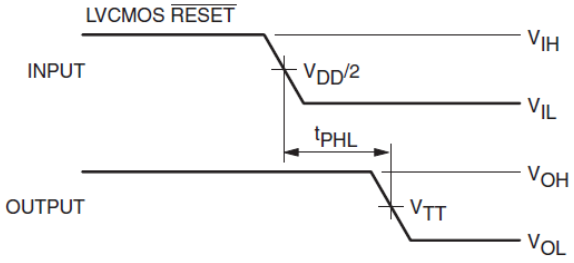
NOTE 1 V_{ID} = 600 mV
NOTE 2 $V_{REF} = V_{DD}/2$
NOTE 3 $V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
NOTE 4 $V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 16 — Voltage Waveforms; Set-up and Hold Times



NOTE 1 t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 17 — Voltage Waveforms; Propagation Delay Times

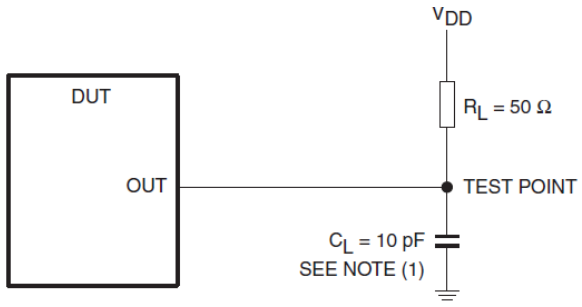


NOTE 1 t_{PLH} and t_{PHL} are the same as t_{PD}.
NOTE 2 $V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
NOTE 3 $V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 18 — Voltage Waveforms; Propagation Delay Times

3.2 Data Output Slew-rate Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



NOTE 1 C_L includes probe and jig capacitance.

Figure 19 — Load Circuit, HIGH-to-LOW Slew Measurement

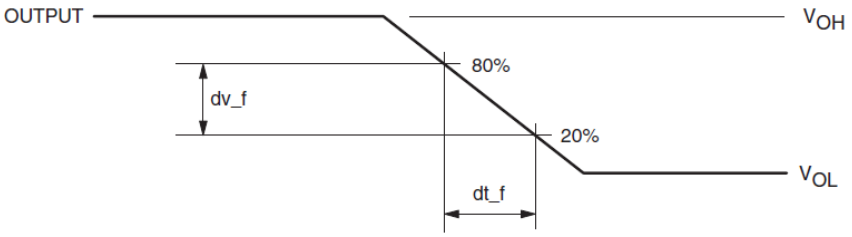
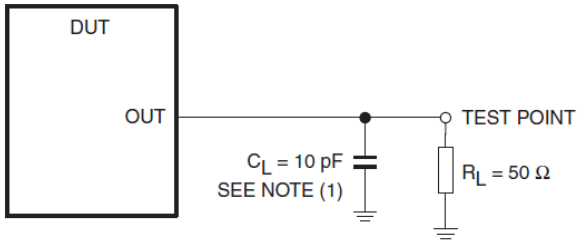


Figure 20 — Voltage Waveforms, HIGH-to-LOW Slew Rate Measurement



NOTE 1 C_L includes probe and jig capacitance.

Figure 21 — Load Circuit, LOW-to-HIGH Slew Measurement

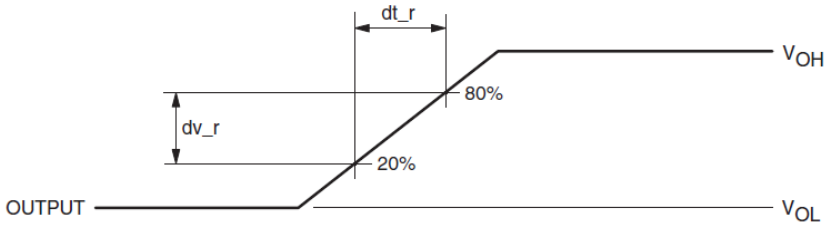
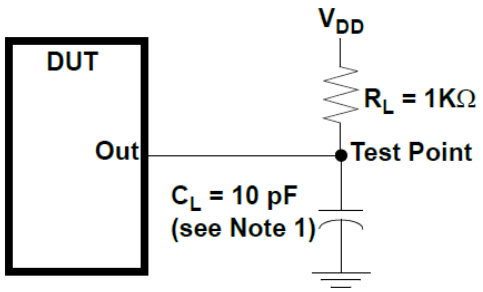


Figure 22 — Voltage Waveforms, LOW-to-HIGH Slew Rate Measurement

3.3 Error Output Load Circuit and Voltage Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



NOTE 1 C_L includes probe and jig capacitance.

Figure 23 — Load Circuit, Error Output Measurements

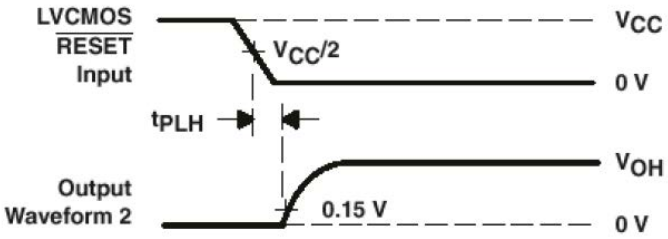


Figure 24 — Voltage Waveforms, Open-drain Output LOW-to-HIGH Transition Time with Respect to Reset Input

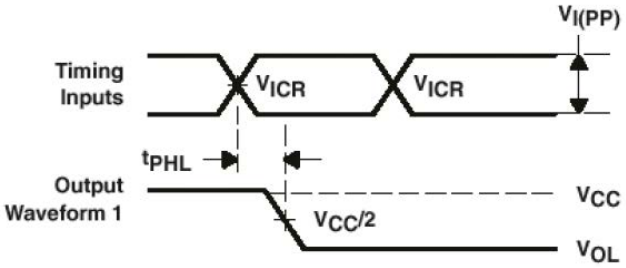


Figure 25 — Voltage Waveforms, Open-drain Output HIGH-to-LOW Transition Time with Respect to Clock Inputs

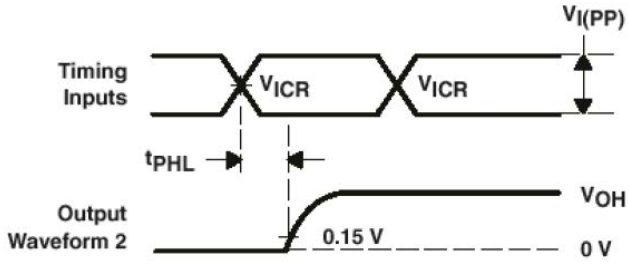


Figure 26 — Voltage Waveforms, Open-drain Output LOW-to-HIGH Transition Time with Respect to Clock Inputs

4 Reference to Other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*
- JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices*
- JESD8-7, *1.8V +/- 0.15V (Normal Range), and 1.2 - 1.95V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits*
- JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18)*
- JESD21-C, *Configuration for Solid State Memories*
- JESD82-7, *Definition of the SSTU32864 1.8 V Configurable Registered Buffer for DDR2 RDIMM Applications*

5 Annex A - (Informative) Differences between JESD82-26.01 and JESD82-26

- Terminology update on Table 1, changed “Master clock” to “Main clock”
- Reformatted the cover page to JEDEC standard
- Updated the JEDEC logo on front and back pages
- Removed the EIA logo from front page
- Moved table notes to inside of tables
- Added the JEDEC Standard Improvement Form
- Added Table of Contents, List of Tables, and List of Figures

Standard Improvement Form **JEDEC Standard JESD82-26.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause num- _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

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