JEDEC STANDARD

Definition of the SSTVN16859 2.5-2.6 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for PC1600, PC2100, PC2700, and PC3200 DDR DIMM Applications

JESD82-13A.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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STANDARD FOR DEFINITION OF THE SSTVN16859 2.5–2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS

Contents

Contents (cont'd)

Tables

Figures

STANDARD FOR DEFINITION OF THE SSTVN16859 2.5–2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS

(From JEDEC Board Ballot JCB-04-74 and JCB-05-11, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTVN16859 13-bit to 26-bit SSTL_2 registered buffer for PC1600, PC2100, PC2700, and PC3200 DDR DIMM applications. The SSTVN16859 is a speed upgrade of the SSTV16859 (JESD82-4) for use in PC3200 DDR DIMMs. It is fully backward compatible with SSTV16859 for all speed grades.

The purpose is to provide a standard for the SSTVN16859 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTVN16859 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 13-bit to 26-bit registered buffer is designed for 2.3 V to 2.7 V V_{DD} (PC1600, PC2100, PC2700) and 2.5 V to 2.7 V V_{DD} (PC3200) operation.

All inputs are compatible with the JEDEC standard for SSTL_2, except the LVCMOS reset ($\overline{\text{RESET}}$) input. All outputs are SSTL_2, Class II compatible.

The SSTVN16859 operates from a differential clock (CK and $\overline{\text{CK}}$). Data are registered at the crossing of CK going high, and $\overline{\text{CK}}$ going low.

The device supports low-power standby operation. When $\overline{\text{RESET}}$ is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{\text{RESET}}$ is low all registers are reset, and all outputs are forced low. The LVCMOS $\overline{\text{RESET}}$ input must always be held at a valid logic high or low level.

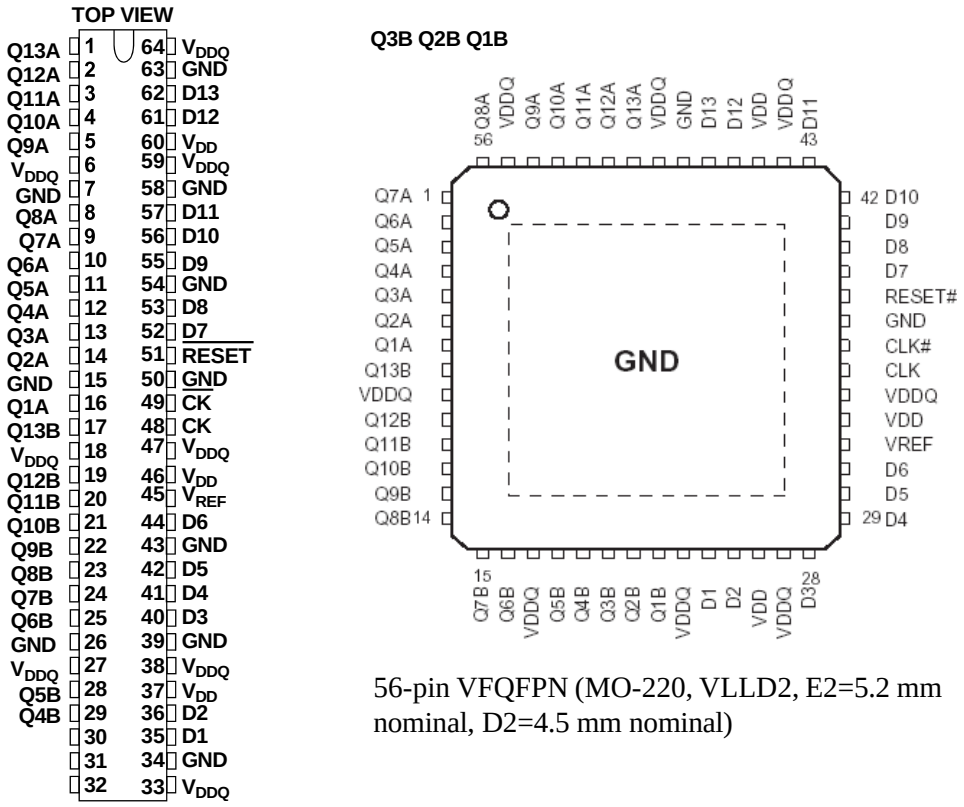
To ensure defined outputs from the register before a stable clock has been supplied, $\overline{\text{RESET}}$ must be held in the low state during power up.

In the DDR DIMM application, $\overline{\text{RESET}}$ is specified to be completely asynchronous with respect to CK and $\overline{\text{CK}}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers, thus ensuring no glitches on the output. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of $\overline{\text{RESET}}$ until the input receivers are fully enabled, the design must ensure that the outputs will remain low.

2.1 Description (cont'd)

Package options include plastic thin shrink small-outline package (MO-153) and 56-pin Very Fine Pitch Quad Flat No-Lead Package (MO-220).

2.2 Pinout Figures



56-pin VFQFPN (MO-220, VLLD2, E2=5.2 mm nominal, D2=4.5 mm nominal)

Figure 1 — 64-pin TSSOP and 56-pin VFQFPN Packages and Pinouts

2.3 Terminal Functions

Table 1 — Terminal Functions

Terminal Name	Description		Electrical Characteristics
Q1–Q13	Data output	PC1600, PC2100, PC2700	SSTL_2, Class II output
		PC3200	SSTL_2, Class II output
GND	Ground		Ground input
V_{DDQ}	Output-stage drain power voltage	PC1600, PC2100, PC2700	2.5-V nominal
		PC3200	2.6-V nominal
V_{DD}	Logic power voltage	PC1600, PC2100, PC2700	2.5-V nominal
		PC3200	2.6-V nominal
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables data and clock differential-input receivers		LVCMOS input
V_{REF}	Input reference voltage	PC1600, PC2100, PC2700	1.25-V nominal
		PC3200	1.30-V nominal
CK	Positive main clock input		Differential input
$\overline{\text{CK}}$	Negative main clock input		Differential input
D1–D13	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{\text{CK}}$		SSTL_2 input

2.4 Function Table

Table 2 — Function Table (each Flip Flop)

Inputs				Q Outputs
$\overline{\text{RESET}}$	**CK**	**$\overline{\text{CK}}$**	**D**	
H	↑	↓	L	L
H	↑	↓	H	H
H	L or H	L or H	X	Q_0
L	X or Floating	X or Floating	X or Floating	L

2.5 Logic Diagram

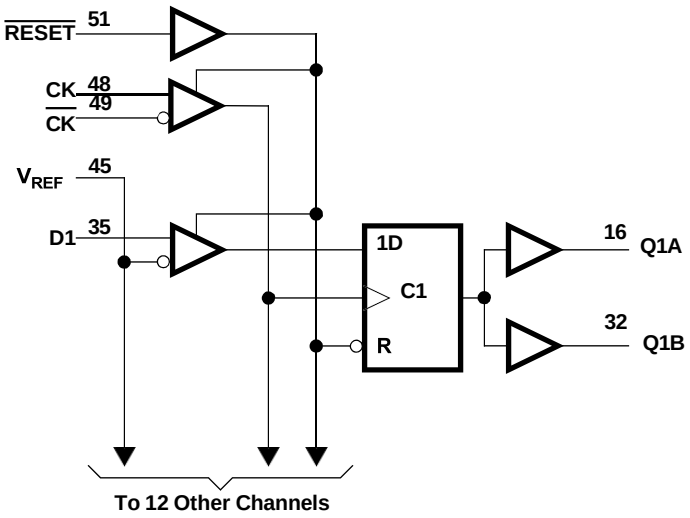


Figure 2 — Logic Diagram (Positive Logic)

2.6 Absolute Maximum Ratings

Table 3 — Absolute Maximum Ratings over Operating Free-Air Temperature Range (See NOTE 1)

Parameter	Range
Supply voltage range, V_{DD} or V_{DDQ}	-0.5 V to 3.6 V
Input voltage range, V_I (See NOTES 2 and 3)	-0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (See NOTES 2 and 3)	-0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	± 50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ})	± 50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ})	± 50 mA
Continuous current through each V_{DD}, V_{DDQ}, or GND	± 100 mA
Storage temperature range, T_{STG}	65 °C to 150 °C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 3.6 V maximum.

2.7 Recommended Operating Conditions

Table 4 — Recommended Operating Conditions (see NOTE)

Symbol	Description		Min	Nom	Max	Unit
V_{DD}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	PC1600-2700	2.3		2.7	V
		PC3200	2.5		2.7	V
V_{REF}	Reference voltage ($V_{REF} = V_{DDQ} / 2$)	PC1600-2700	1.15	1.25	1.35	V
		PC3200	1.25	1.30	1.35	
V_{TT}	Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0		V_{DD}	V
V_{IH}	AC high-level input voltage	Data inputs	V_{REF} + 310 mV			V
V_{IL}	AC low-level input voltage	Data inputs			V_{REF} – 310 mV	V
V_{IH}	DC high-level input voltage	Data inputs	V_{REF} + 150 mV			V
V_{IL}	DC low-level input voltage	Data inputs			V_{REF} – 150 mV	V
V_{IH}	High-level input voltage	$\overline{\text{RESET}}$	1.7			V
V_{IL}	Low-level input voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common-mode input range	CK, $\overline{\text{CK}}$	0.97		1.53	V
V_{ID}	Differential input voltage	CK, $\overline{\text{CK}}$	360			mV
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	
T_A	Operating free-air temperature		0		70	°C

NOTE The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

2.8 DC Specifications

Table 5 — Electrical Characteristics over Recommended Operating Free-Air Temperature Range for PC1600, PC2100, and PC2700

PARAMETER		TEST CONDITIONS		V_{DD}	MIN	TYP	MAX	UNIT
V_{IK}		I_I = –18 mA		2.3 V			–1.2	V
V_{OH}		I_{OH} = –100 μA		2.3 to 2.7 V	V_{DD} – 0.2			V
		I_{OH} = –16 mA		2.3 V	1.95			
V_{OL}		I_{OL} = 100 μA		2.3 to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.3 V			0.35	
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			±5	μA
I_{DD}	Static standby	$\overline{RESET}$= GND	I_O = 0	2.7 V			0.01	mA
	Static operating	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					†	
I_{DDD}	Dynamic operating – clock only	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and CK switching 50% duty cycle	I_O = 0	2.7 V		†		μA/ clock MHz
	Dynamic operating – per each data input	$\overline{RESET} = V_{DD}$, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and CK switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.				†		μA/ clock MHz/ data input
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV		2.5 V	2.5		3.5	pF
	CK and $\overline{CK}$	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV			2.5		3.5	
	$\overline{RESET}$	$V_I = V_{DD}$ or GND			†		†	

† The vendor must supply this value for full device description.

2.8 DC Specifications (cont'd)

Table 6 — Electrical Characteristics over Recommended Operating Free-Air Temperature Range for PC3200

PARAMETER		TEST CONDITIONS		V_{DD}	MIN	TYP	MAX	UNIT
V_{IK}		I_I = –18 mA		2.5 V			–1.2	V
V_{OH}		I_{OH} = –100 µA		2.5 to 2.7 V	V_{DD} – 0.2			V
		I_{OH} = –16 mA		2.5 V	1.95			
V_{OL}		I_{OL} = 100 µA		2.5 to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.5 V			0.35	
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			±5	µA
I_{DD}	Static standby	$\overline{RESET}$ = GND	I_O = 0	2.7 V			0.01	mA
	Static operating	$\overline{RESET}$ = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$					†	
I_{DDD}	Dynamic operating – clock only	$\overline{RESET}$ = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle	I_O = 0	2.7 V		†		µA/ clock MHz
	Dynamic operating – per each data input	$\overline{RESET}$ = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CK and $\overline{CK}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.				†		µA/ clock MHz/ data input
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV		2.6 V	2.5		3.5	pF
	CK and $\overline{CK}$	V_{ICR} = 1.30 V, $V_{I(PP)}$ = 360 mV			2.5		3.5	
	$\overline{RESET}$	$V_I = V_{DD}$ or GND			†		†	

† The vendor must supply this value for full device description.

2.9 Timing Requirements

Table 7 — Timing Requirements over Recommended Operating Free-Air Temperature Range

Symbol	Description		PC1600, PC2100, PC2700		PC3200		UNIT
			V_{DD} = 2.5 V ± 0.2 V		V_{DD} = 2.6 V ± 0.1 V		
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			200		220	MHz
t_w	Pulse duration, CK, $\overline{CK}$ high or low		2.5		2.5		ns
t_{act}†	Differential inputs active time (see NOTE 1)			22		22	ns
t_{inact}†	Differential inputs inactive time (see NOTE 2)			22		22	ns
t_{su}	Setup time, fast slew rate (See NOTES 3 and 5)	Data before CK ↑, CK ↓	0.65		0.65		ns
	Setup time, slow slew rate (See NOTES 4 and 5)		0.75		0.75		ns
t_h	Hold time, fast slew rate (See NOTES 3 and 5)	Data after CK ↑, CK ↓	0.75		0.75		ns
	Hold time, slow slew rate (See NOTES 4 and 5)		0.9		0.9		ns

† This parameter is not necessarily production tested.

NOTE 1 Data inputs must be low a minimum time of t_{act} max, after $\overline{RESET}$ is taken high

NOTE 2 Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max, after $\overline{RESET}$ is taken low.

NOTE 3 For data signal input slew rate $\geq$ 1 V/ns.

NOTE 4 For data signal input slew rate $\geq$ 0.5 V/ns and < 1 V/ns

NOTE 5 CK, $\overline{CK}$ signals input slew rates are $\geq$ 1 V/ns.

2.10 AC Specifications

Table 8 — Switching Characteristics over Recommended Operating Free-Air Temperature Range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	PC1600, PC2100, PC2700 V_{DD} = 2.5 V ± 0.2 V		UNIT
			MIN	MAX	
f_{max}			200		MHz
t_{pd}	CK and $\overline{CK}$	Q	1.1	2.6	ns
t_{pdss} (see NOTE 6)	CK and $\overline{CK}$	Q		2.9	ns
t_{PHL}	$\overline{RESET}$	Q		5	ns
t_{PDM}	CK - $\overline{CK}$	Q	see NOTE 7		ns

NOTE 6 The Simultaneous Switching specification is guaranteed by Characterization.
NOTE 7 Measured with reference load, see Figure 4. t_{PDM} is vendor specific. It is not required for compliant devices that this parameter is specified.

Table 9 — Switching Characteristics over Recommended Operating Free-Air Temperature Range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		PC3200 V_{DD} = 2.6 V ± 0.1 V		UNIT
				MIN	MAX	
f_{max}				220		MHz
t_{pd}	CK and $\overline{CK}$	Q	64-pin TSSOP	1.1	2.2	ns
			56-pin VFQFPN	1.1	1.8	ns
t_{pdss} (see NOTE 8)	CK and $\overline{CK}$	Q	64-pin TSSOP		2.5	ns
			56-pin VFQFPN		2.0	ns
t_{PHL}	$\overline{RESET}$	Q			5	ns
t_{PDM}	CK - $\overline{CK}$	Q		see NOTE 9		ns

NOTE 8 The Simultaneous Switching specification is guaranteed by Characterization.
NOTE 9 Measured with reference load, see Figure 4. t_{PDM} is vendor specific. It is not required for compliant devices that this parameter is specified.

3 Output Buffer Characteristics

3.1 Voltage vs. Current (V/I)

Table 10 describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these curves is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR DIMM application.

Table 10 — Output Buffer Voltage vs. Current (V/I) Characteristics

Voltage (V)	Pull-down		Pull-up	
	I(mA)	I(mA)	I(mA)	I(mA)
	MIN	MAX	MIN	MAX
0	0	0	0	-0
0.1	5	18	-5	-18
0.2	10	30	-10	-30
0.3	15	44	-15	-44
0.4	19	55	-19	-55
0.5	23	67	-23	-67
0.6	27	78	-27	-78
0.7	30	90	-30	-90
0.8	34	101	-34	-98
0.9	36	112	-36	-106
1.0	38	121	-38	-113
1.1	40	131	-40	-119
1.2	42	140	-42	-125
1.3	43	150	-43	-130
1.4	44	159	-44	-134
1.5	44	167	-44	-137
1.6	45	176	-45	-140
1.7	45	184	-45	-143
1.8	45	192	-45	-146
1.9	45	199	-45	-149
2.0	45	206	-45	-152
2.1	46	212	-46	-154
2.2	46	218	-46	-156
2.3	46	222	-46	-157
2.4	46	226	-46	-159
2.5	46	229	-46	-160
2.6	46	233	-46	-161
2.7	46	234	-46	-162

3.2 Slew Rate

Table 11 describes output-buffer slew-rate characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these rates is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR DIMM application. This information does not necessarily have to appear in the device datasheet.

Obtain rise and fall time measurements by using the same procedure for obtaining "[Ramp]" data according to the current EIA IBIS specification. In particular it is very important to note that the following slew rates are specified at the output of the die, **without** package parasitics in the power, ground or output paths. The measurement points are at 20% and 80%. The slew-rate test load shall be a 50 Ω resistor to GND for Rise, and a 50 Ω resistor to V_{DDQ} for Fall. The dV/dt ratio is reduced to V/ns.

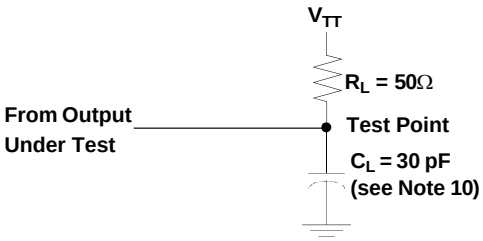
Table 11 — Output-buffer Slew Rate Characteristics

dV/dt	Min	Max
Rise	1.1 V/ns	13.9 V/ns
Fall	1.1 V/ns	14.5 V/ns

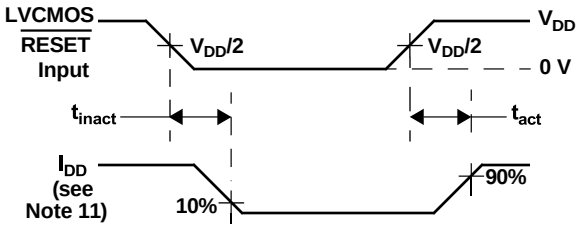
3.3 Simultaneous Switching

The vendor must supply, as requested, simultaneous switching information for full device description. In particular, slow corner propagation-delay increase due to simultaneous switching conditions is necessary for post-register timing analysis. This information does not necessarily have to appear in the device datasheet.

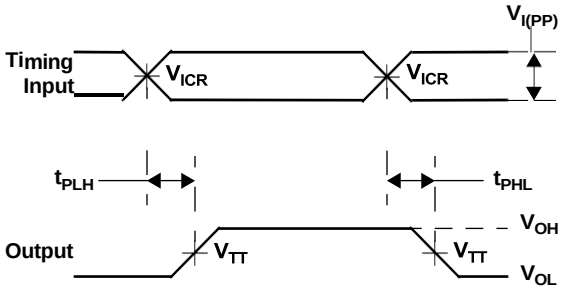
4 Test Circuit and Switching Waveforms



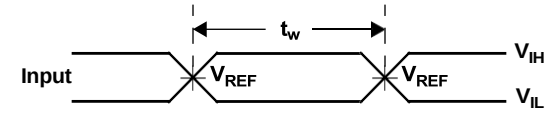
LOAD CIRCUIT



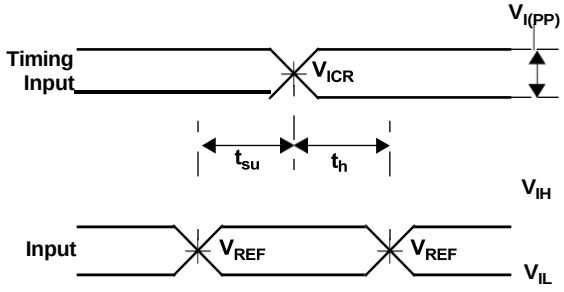
VOLTAGE AND CURRENT WAVEFORMS
INPUTS ACTIVE AND INACTIVE TIMES



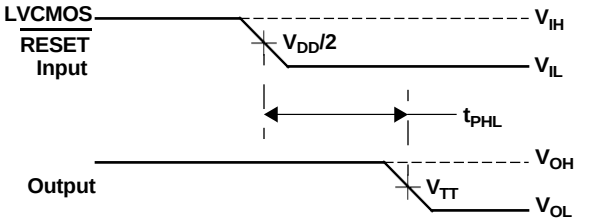
VOLTAGE WAVEFORMS – PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS – PULSE DURATION



VOLTAGE WAVEFORMS – SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS – PROPAGATION DELAY TIMES

NOTE 10 C_L includes probe and jig capacitance

NOTE 11 I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

NOTE 12 All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

NOTE 13 The outputs are measured one at a time with one transition per measurement.

NOTE 14 $V_{TT} = V_{REF} = V_{DDQ}/2$

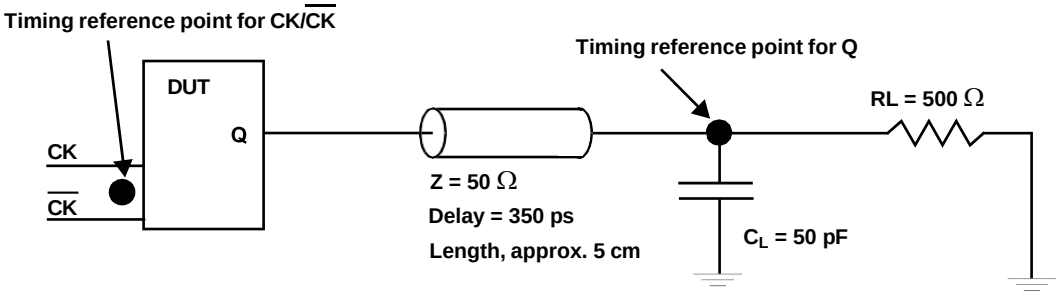
NOTE 15 $V_{IH} = V_{REF}$ + 310 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

NOTE 16 $V_{IL} = V_{REF}$ – 310 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

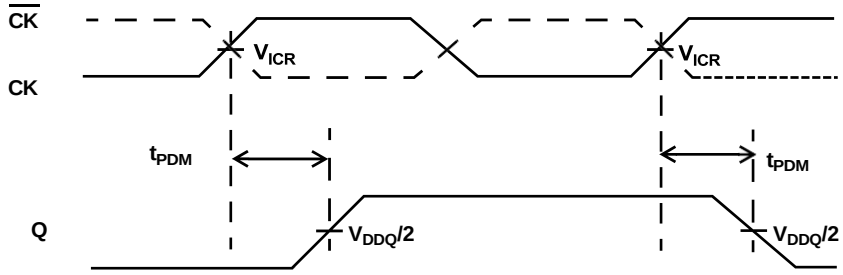
NOTE 17 t_{PLH} and t_{PHL} are the same as t_{pd}

Figure 3 — Parameter Measurement Information

5 Reference Load for Registered DIMMs



DIMM specific reference load circuit



NOTE The transmission line should be designed to have an impedance equal to 50 Ω and a delay (in matched impedance environment) equal to 350 ps. The actual length may vary with PCB parameters.

Figure 4 — Measurement Setup for t_{PDM}

6 Reference to other Applicable JEDEC Standards and Publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*

JEP104-A, *Reference Guide to Letter Symbols for Semiconductor Devices*

JESD8-5, *2.5 V ± 0.2 V (Normal Range) and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits.*

JESD8-9, *Stub Series Terminated Logic for 2.5 V (SSTL_2)*

JESD21-C, *Configuration for Solid State Memories*

Annex A — (Informative) Differences between JESD82-13A and JESD82-13

This table briefly describes most of the changes made to entries that appear in this standard, JESD82-13A, compared to its predecessor, JESD82-13 (November 2004). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Page	Description
9	In Table 9, changed the t_{pd} added the MIN and MAX values.

Annex B — (Informative) Differences between JESD82-13A.01 and JESD82-13A

Editorial revisions as follows:

1. Terminology update: Replaced “master” with “main” in Table 1 definitions for CK and $\overline{CK}$.
2. Updated JEDEC logos in title and back pages
3. Added Table of Contents and List of Tables and Figures
4. Reformatted all tables to the JEDEC standard layout
5. Initial caps on all headings and table/figure captions

Standard Improvement Form **JEDEC** **JESD82-13A.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

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