JEDEC STANDARD

Instrumentation Chip Data Sheet for FBDIMM Diagnostic Senselines

JESD82-22.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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INSTRUMENTATION CHIP DATA SHEET FOR FBDIMM DIAGNOSTIC SENSELINES

(From JEDEC Board Ballot JCB-06-53, formulated under the cognizance of the JC-40.1 Subcommittee on CMOS/BiCMOS Digital Logic.)

1 Scope

This device is a one-chip spectrum analyzer that operates in the frequency range from 1 to 2 GHz.

It requires no external components except some filtering of the voltage supply (one inductor, one bypass capacitor).

The frequency of the VCO is adjusted by an internal DAC. No PLL loop is used to lock the VCO to a reference frequency. A counter is used to determine the VCO frequency.

The device has a serial I2C data interface.

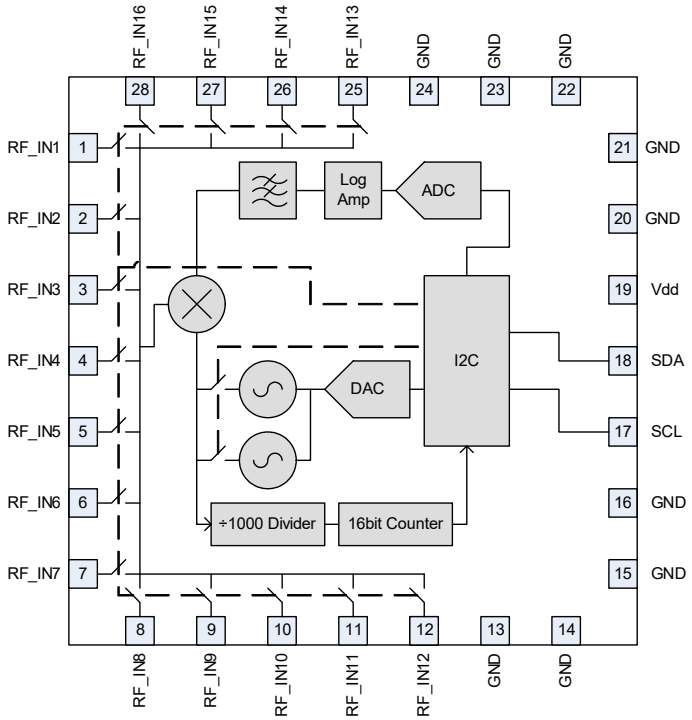
The device is available in a 28 pin TQFN package and is specified over the extended industrial (-40 ^{o}C to +85 ^{o}C) temperature range.

2 Features

- Input Frequency Range 1 – 2 GHz
- Integrated Frequency Counter
- 50 dB Dynamic Range
- 3.3 V power supply
- Low Power
- Low Cost
- Small 28 pin TQFN Packages
- Integrated I2C serial interface

2.1 Temperature Range / Package

Functional Diagram / Pin Configuration



2.2 DC Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltage		2.97	3.3	3.63	V

2.3 AC Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I2C Clock Frequency			400		kHz
Local Oscillator No. 1 Range		1000		1600	MHz
Local Oscillator No. 2 Range		1600		2000	MHz
Local Oscillators Step Size			4		MHz
Detected Power Range		-80		-30	dBm
Input Frequency Range		1000		2000	MHz
IF Detection Bandwidth			10		MHz
Input to Input Isolation	@ 2 GHz	20	30		dB
Local Oscillator Drift over time			500		kHz/sec
Local Oscillator Frequency Change due to Changes on the Supply Voltage	200mV voltage step on supply		5		MHz/V
Local Oscillator Drift over temperature			0.1		MHz/deg
Power Reading Response Time	measured from time of programming the DAC		100		µs
Receiver Gain Flatness	within f +/- 10MHz		+/- 0.5		dB
Receiver Selectivity	at Δf > 20MHz	5			dB
Receiver Selectivity	at Δf > 40MHz	10			dB
Receiver Selectivity	at Δf > 100MHz	25			dB

2.4 I^2C Electrical Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I2C Digital Input - SCL, SDA					
Clock Speed			400		KHz
Input Logic Level High		0.7 x Vcc			V
Input Logic Level Low				0.3 x Vcc	V
Input Hysteresis		0.05 x Vcc			V
Input Leakage Current	Digital Inputs 0 or Vcc		±0.1	±1	µA
Input Capacitance			6	10	pF
Output Logic Level Low				0.6	V
I2C Digital Output - SDA					
Output Logic Level Low	Isink = 3mA			0.4	V
Three-State Leakage Current	Digital Inputs 0 or Vcc	-10		+10	µA
Three-State Output Capacitance			6	10	pF

3 Digital Interface Description

Basic Function

The device features an I2C Bus compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). The device is a transmit/receive target-only device, relying upon a controller to generate a clock signal. The controller initiates data transfer on the bus and generates SCL to permit that transfer. A controller communicates to the device by transmitting the proper address followed by command and/or data words. Each transmit sequence is framed by a START (S) and STOP condition (P). Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse. The device contains drives that re open-drain, requiring a pullup resistor (500 or greater) to generate a logic high voltage.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see START and STOP Conditions). SDA and SCL idle high when the I2C bus is not busy.

Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high.

Repeated Start Conditions

A repeated Start (Sr) condition is a Start condition that occurs when another Start conditions has occurred earlier but no Stop condition occurred in the meantime. A repeated Start may indicate a change of data direction on the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. ACK is always generated by the receiving device.

Write Data Format

In write mode (R/W = 0), data that follows the address byte controls the device.

Read Data Format

In read mode (R/W = 1), the device writes data to the bus.

I2C Addresses

The four MSBs of the chip address are hard-coded (b4 to b7) whereas the three LSBs will be sensed by the Chip as the DC that has been applied to PINs 1 (A0), 2 (A1), and 3 (A2). Therefore, on a single I2C bus, up to eight spectrum analyzers can be used.

3 Digital Interface Description (cont'd)

Table 1 - Device Address

V(RF_IN1)	V(RF_IN2)	V(RF_IN3)	Device Address (A_6...A_0)
GND	GND	GND	0101 000
Vcc	GND	GND	0101 001
GND	Vcc	GND	0101 010
Vcc	Vcc	GND	0101 011
GND	GND	Vcc	0101 100
Vcc	GND	Vcc	0101 101
GND	Vcc	Vcc	0101 110
Vcc	Vcc	Vcc	0101 111

Table 2 - Command Byte Definitions

SERIAL DATA INPUT							Function
D6	D5	D4	D3	D2	D1	D0	
0	0	0	MUX3	MUX2	MUX1	MUX0	Four bit data for selecting one out of 16 RF inputs (multiplexer)
0	0	1	X	DAC9	DAC8	DAC7	Control word to load the DAC data including the three MSBs. The remaining 7 bits are transmitted in the following byte
0	1	0	X	X	X	X	Control word to start uploading the ADC data to the controller (1 Byte)
0	1	1	X	X	X	X	Control word to start uploading the Counter Registers to the controller (1 Byte)

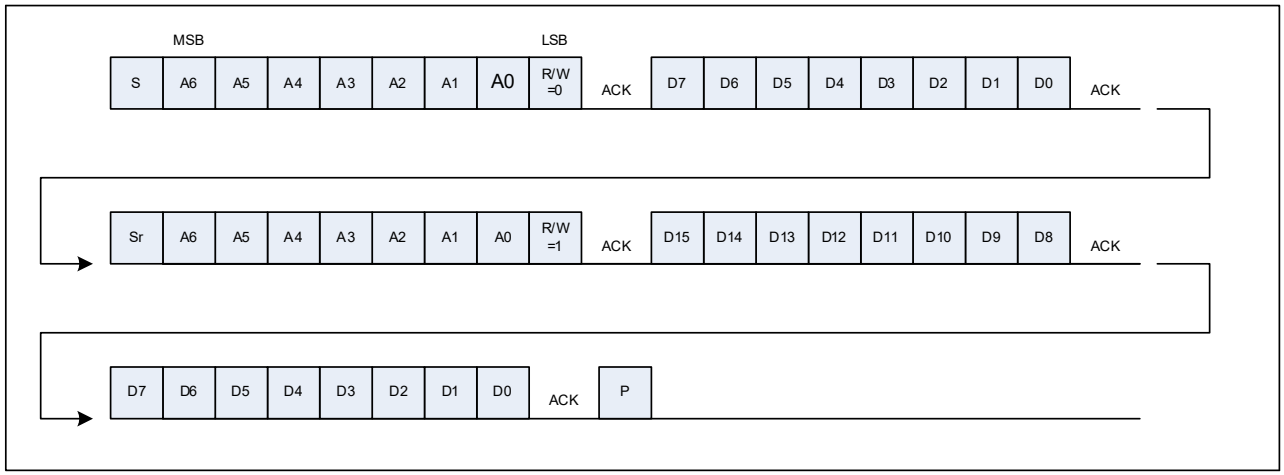


Figure 1 — Data SequencePin DescriptionPin Description

4 Pin Description

Table 3 - Pin Description

PIN	NAME	FUNCTION
1	RF_IN1	RF Input, also A0 bit of chip address
2	RF_IN2	RF Input, also A1 bit of chip address
3	RF_IN3	RF Input, also A2 bit of chip address
4, 5, 6, 7, 8, 9, 10, 11, 12, 25, 26, 27, 28	RF_Inx	RF Input
13, 14, 15, 16, 20, 21, 22, 23, 24	GND	Ground PIN
17	SCL	Serial Port Clock
18	SDA	Serial Port Data
19	Vdd	Supply Voltage

4.1 Detailed Description

The device is a one-chip spectrum analyzer. It is designed to find test signals within a spectrum of interferers and determine the power of these test signals. It uses a mixer to mix the receive signal to an IF of 10 MHz and use a logarithmic amplifier to determine the power of this signal. The local oscillator that is used for the mixing is a free-running VCO that is controlled by a DAC. The DAC can be stepped through its output voltage range to sweep the VCO over a frequency range that goes from 1000 to 2000 MHz. Due to the fact, that no image rejection is implemented, the receiver receives signals within a bandwidth that is double the cut-off frequency of the low pass filter. This is due to the simple architecture and has to be taken into account in case blocking signals exist at the RF inputs that are not separated from the wanted receive signals by more than this bandwidth. Due to the fact that the VCO is free-running and not locked to a PLL, its frequency is not stable and will change over time with temperature and also due to switching inside the chip or with changes on the supply voltage. However, the changes will be limited to a number corresponding to a few codes of the DAC, so that by scanning the adjacent DAC codes, the signal can be found easily.

One possible application is the assessment of the quality of interconnects in digital computer hardware, if this hardware is able to transmit a test signal that contains at least one harmonic that falls into the frequency range of this spectrum analyzer. By coupling a part of this signal from different locations within the signal path and determining the power of these signals, the quality of the interconnect can be determined either based on the absolute power reading or relative to results from previous measurements.

4.1 Detailed Description (cont'd)

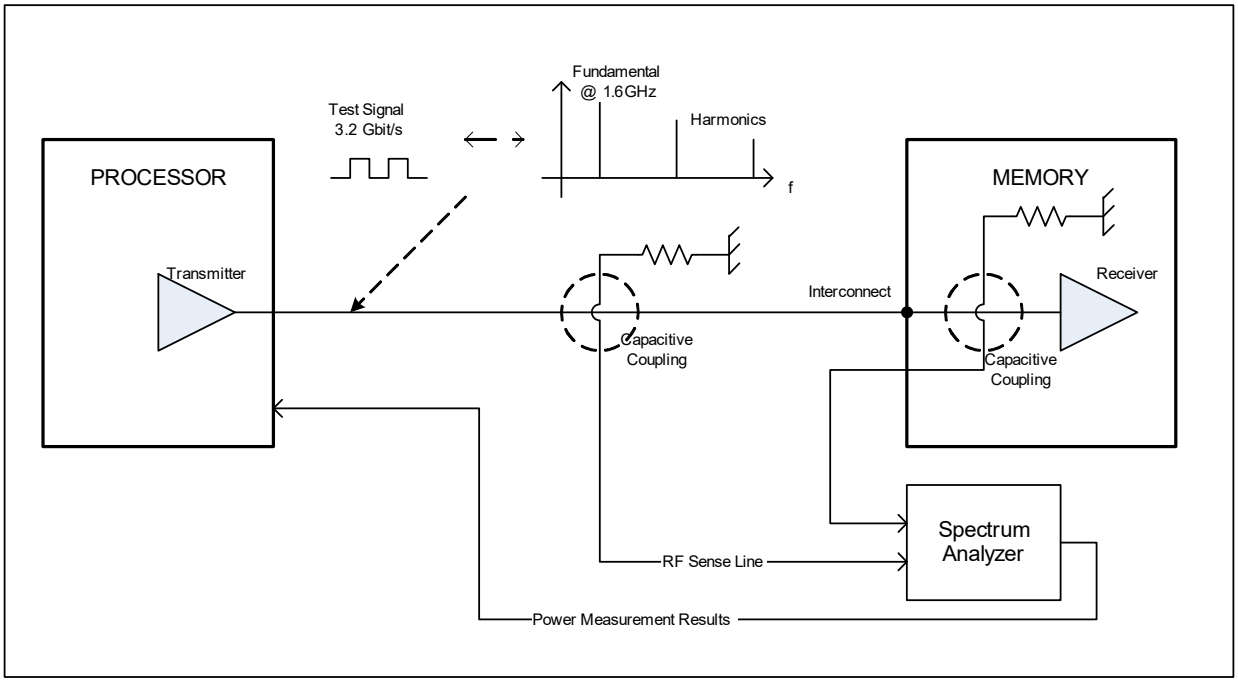


Figure 2 — Basic Principle

By adding the capacitive taps to the signal path, the original point-to-point structure is transferred into a point-to-multipoint architecture with one transmit node and N+1 receive nodes (Figure 3).

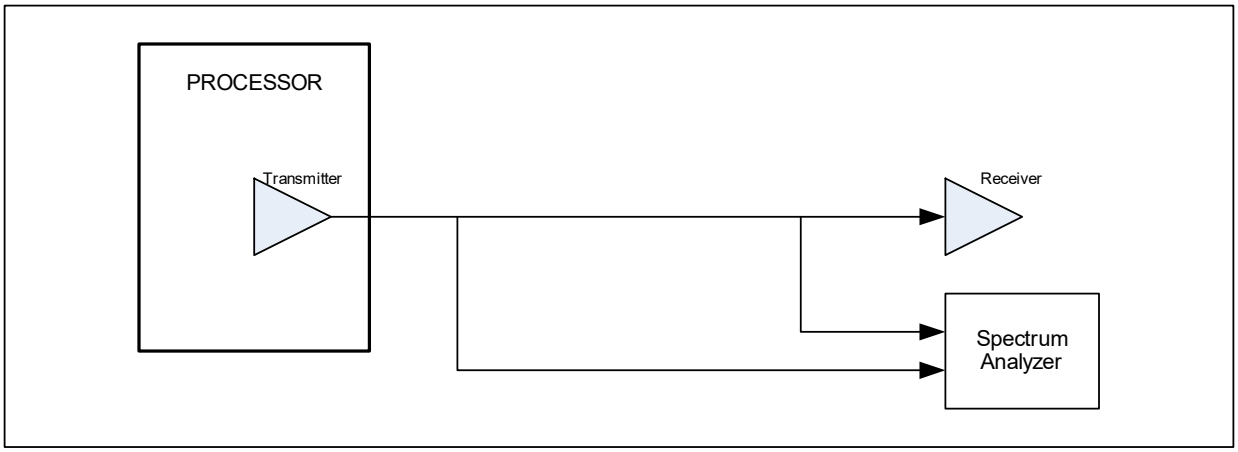


Figure 3 — Point-to-Multipoint Architecture

4.1 Detailed Description (cont'd)

In case of differential signal lines, a special layout is necessary in order to prevent the signals from both lines to cancel out on the sense lines (Figure 4).

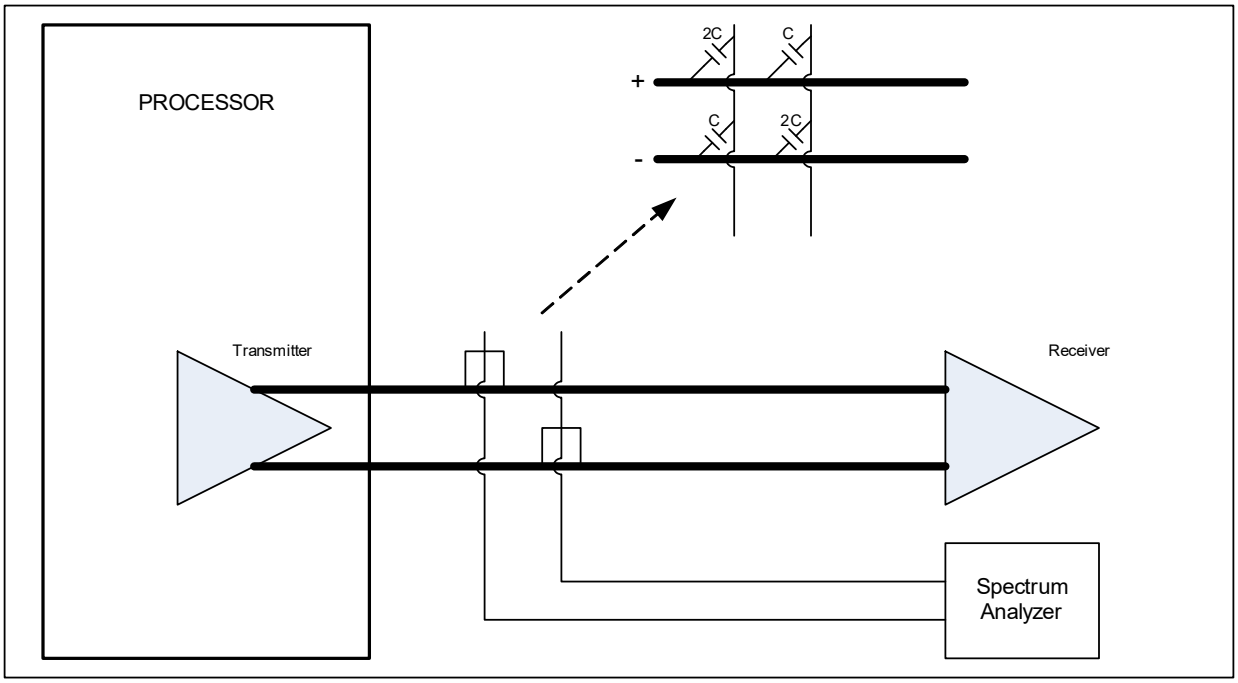


Figure 4 — Additional Capacitors

4.2 Basic Scanning Algorithm

Since there is no reference frequency available to the spectrum analyzer, the frequency of the oscillator is not exactly known. Therefore, at the beginning of a measurement, the whole DAC range is used to sweep the oscillator from its minimum to its maximum frequency. As long as the test signal frequency lies within this range, at least one DAC code can be found that yields the maximum power reading. In case of only the test signal is present and no interferers, there will be only one detectable maximum. In case of interferers, this algorithm will result in more than one DAC code with a power reading considerably higher than the noise level. In this case, a software algorithm can be used to switch off the test signal so that the power reading for this signal will change whereas the power reading for interferers will not change. This DAC setting can then be held constant in order to measure the power of the test signal on all available sense line inputs. As long as the oscillator frequency remains within a window as defined by the receive bandwidth of the spectrum analyzer, there is no need for re-calibration.

4.3 Detect Interconnect Problems

In case of interconnect problems i.e., broken connections or connections that have become resistive, the signal level on the data lines will change. This change can be detected with the spectrum analyzer. In case of memory modules, the level of the test signal on the motherboard as well as on the memory module can be compared and in case of memory errors it can be easily distinguished between interconnect faults and memory hardware errors.

4.3 Detect Interconnect Problems (cont'd)

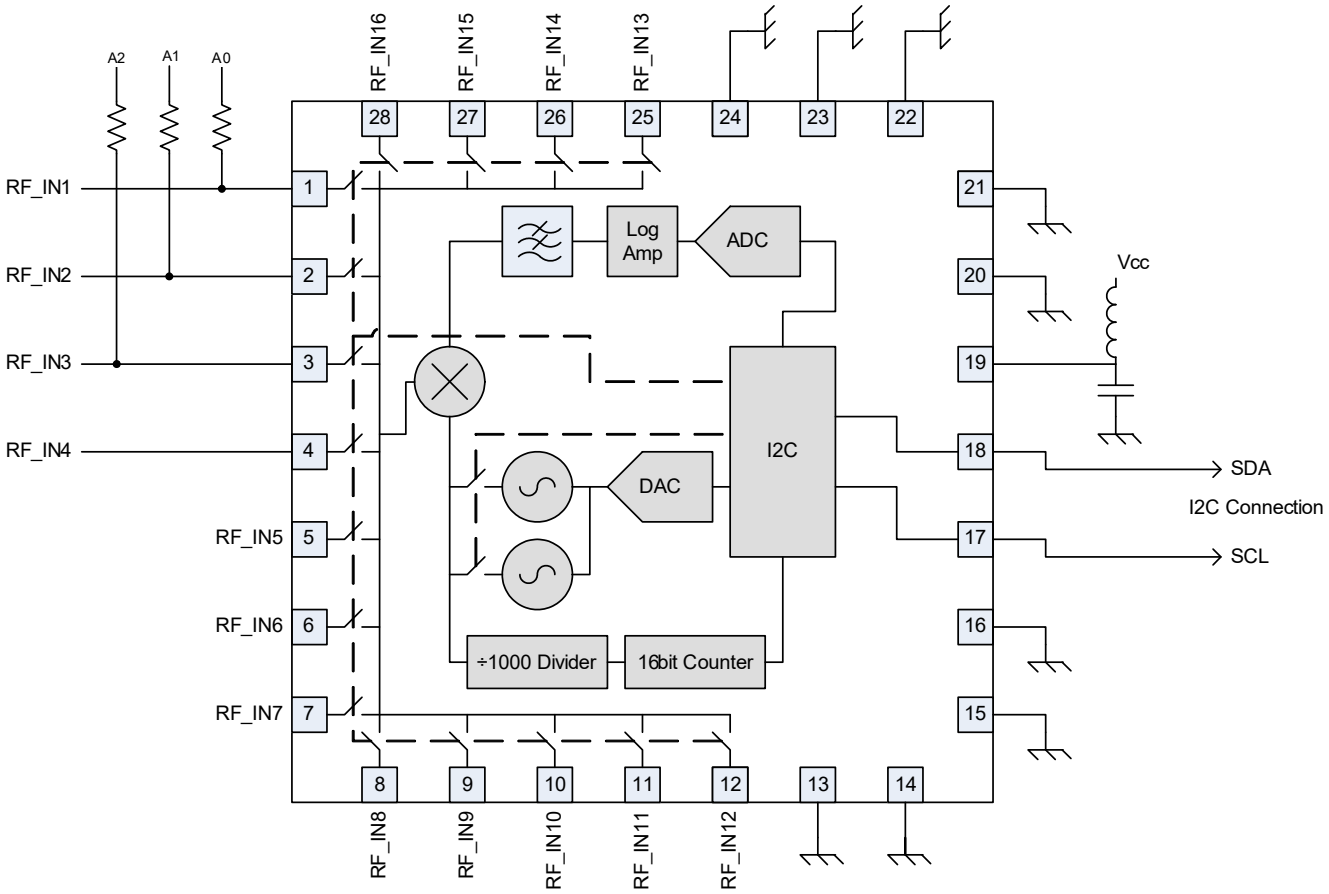
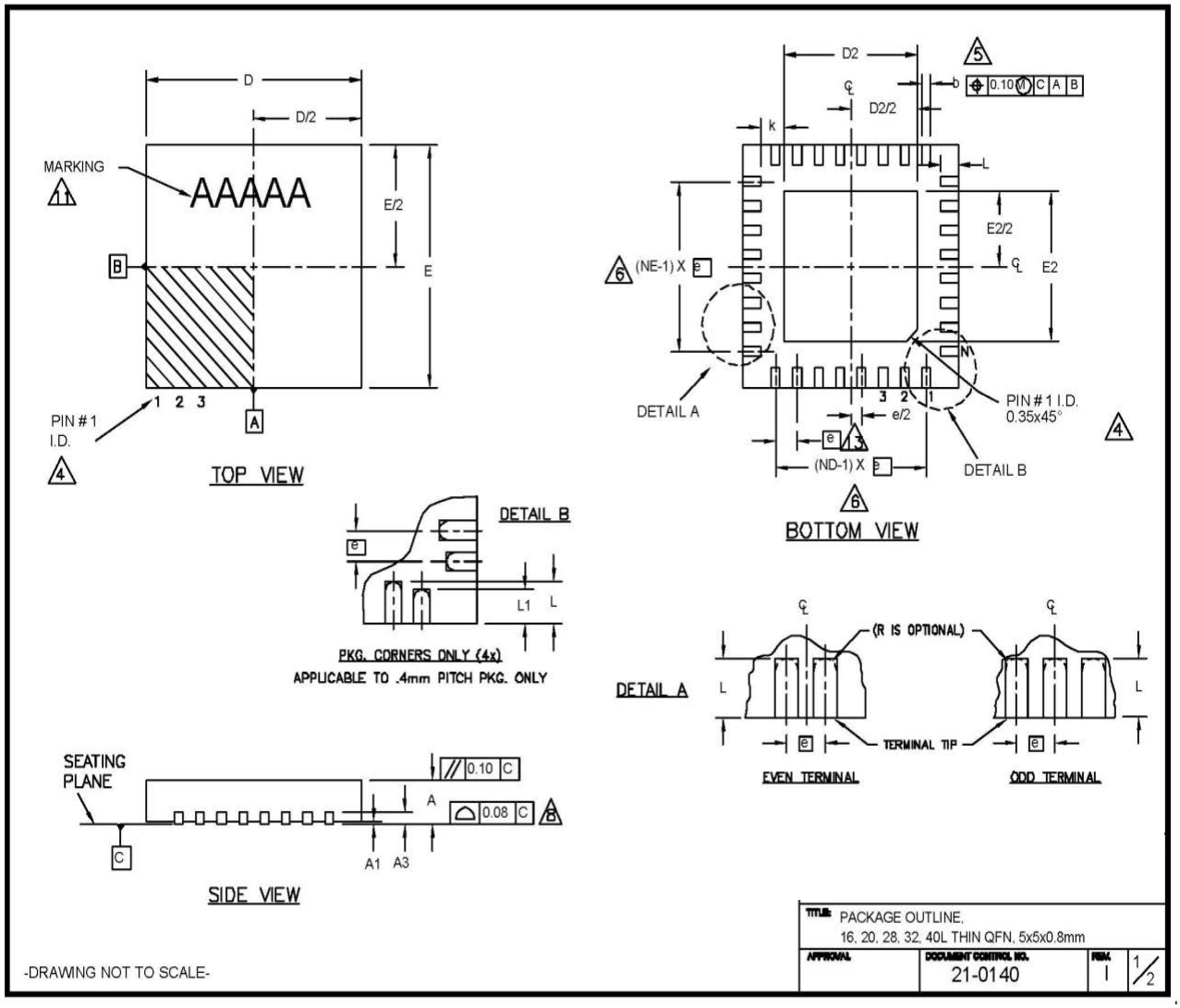


Figure 5 — Typical Application Circuit

4.3 Detect Interconnect Problems (cont'd)



4.3 Detect Interconnect Problems (cont'd)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L exceptions	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
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13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

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Annex A — (Informative) Differences between JESD82-22.01 and JESD82-22

Editorial changes as follows:

1. Terminology updates in Clause 3
   - Basic Function paragraph: changed “master” to “controller”
   - Start and Stop conditions paragraph: changed “master” to “controller”
   - Table 2: changed “master” to “controller”
   - Basic Function paragraph: changed “slave” to “target”
2. Updated JEDEC logos and Standard Improvement Form
3. All section headings, table titles, and figure titles changed to Initial Caps

Standard Improvement Form **JEDEC Standard JESD82-22.01**

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The referenced clause number has proven to be:

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