JEDEC STANDARD

Definition of the SSTUB32865 28-bit 1:2 Registered Buffer with Parity for DDR2 RDIMM Applications

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DEFINITION OF THE SSTUB32865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS

(From JEDEC Board Ballot JCB-07-14, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications. The SSTUB32865 is identical in functionality to the SSTU32865 but specifies tighter timing characteristics and a higher application frequency of up to 410 MHz.

The purpose is to provide a standard for the SSTUB32865 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation SSTUB32865 refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device Standard

2.1 Description

This 28-bit 1:2 registered buffer with parity is designed for 1.7 V to 1.9 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTUB32865 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going high, and $\overline{CK}$ going low.

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is low, the differential input receivers are disabled, and un-driven (floating) data, clock and reference voltage (V_{REF}) inputs are allowed. In addition, when $\overline{RESET}$ is low all registers are reset, and all outputs except $\overline{PTYERR}$ are forced low. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the low state during power up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

2.1 Description (cont'd)

As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the SSTUB32865 must ensure that the outputs will remain low, thus ensuring no glitches on the output. If the data inputs are not held low, then $\overline{DCS0}$ and $\overline{DCS1}$ must be held high, DODT0 and DODT1, DCKE0, and DCKE1 must be held low, and all other inputs must remain stable (either low or high) for a minimum of t_{ACT} (max) after the rising edge of $\overline{RESET}$.

The device monitors both $\overline{DCS0}$ and $\overline{DCS1}$ inputs and will gate the Qn outputs from changing states when both $\overline{DCS0}$ and $\overline{DCS1}$ are high. If either $\overline{DCS0}$ or $\overline{DCS1}$ input is low, the Qn outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS0}$ and $\overline{DCS1}$ control and will force the Qn outputs low and the $\overline{PTYERR}$ output high. If the DCS-control functionality is not desired, then the CSGateEN input can be hardwired to ground, in which case, the setup-time requirement for DCS would be the same as for the other D data inputs.

The SSTUB32865 includes a parity checking function. The SSTUB32865 accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs (with either $\overline{DCS0}$ or $\overline{DCS1}$ active) and indicates whether a parity error has occurred on its open-drain $\overline{PTYERR}$ pin (active LOW). If an error occurs and the $\overline{PTYERR}$ output is driven low, it stays latched low for a minimum of two clock cycles or until $\overline{RESET}$ is driven low. If two or more consecutive parity errors occur, the $\overline{PTYERR}$ output is driven low and latched low for a clock duration equal to the parity error duration or until $\overline{RESET}$ is driven low. If a parity error occurs on the clock cycle before the device enters the low-power mode (LPM) and the $\overline{PTYERR}$ output is driven low, then it stays latched low for the LPM duration plus two clock cycles or until $\overline{RESET}$ is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, $\overline{DCS0}$ and $\overline{DCS1}$) are not included in the parity check computation.

The parity error output $\overline{PTYERR}$ will be reset to high by $\overline{RESET}$ transitioning low and will not be decoded until after $\overline{RESET}$ goes high and $\overline{DCS0}$ and/or $\overline{DCS1}$ are asserted low. CSGateEN does not affect $\overline{PTYERR}$ operation.

2.2 160-ball TFBGA (MO-246A)

Package options include 160-ball Thin Profile Fine Pitch BGA (TFBGA) (12 × 18 array, 9.0 × 13.0 mm body size, 0.65 mm pitch, MO-246, Issue A).

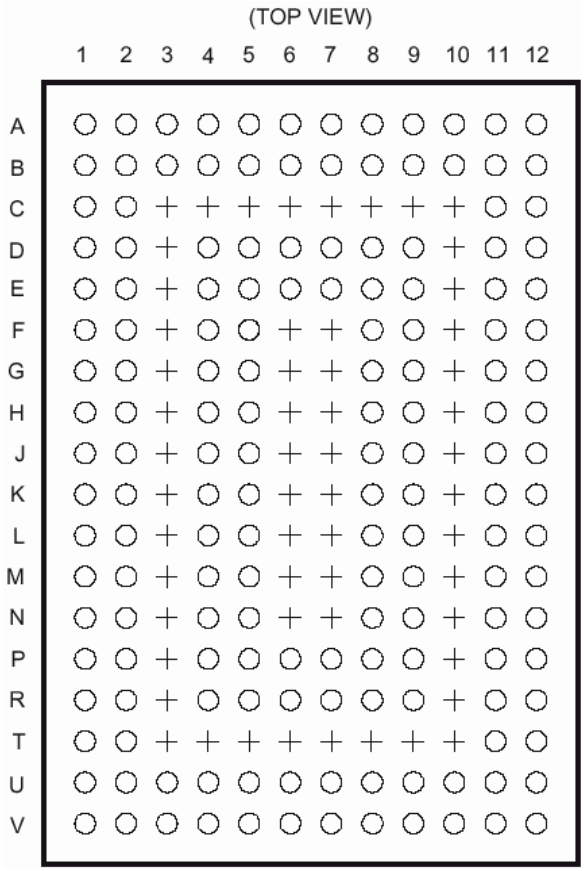


Figure 1 — Pinout Configuration

2.3 Pinout Top View for 160-ball TFBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGate EN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CK	$\overline{\text{DCS0}}$		GND	GND			VDDR	VDDR		$\overline{\text{QCS0B}}$	$\overline{\text{QCS0A}}$
K	$\overline{\text{CK}}$	$\overline{\text{DCS1}}$		VDDL	VDDL			GND	GND		$\overline{\text{QCS1B}}$	$\overline{\text{QCS1A}}$
L	$\overline{\text{RESET}}$	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14A
U	DCKE0	DCKE1	MCL	$\overline{\text{PTYERR}}$	MCH	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

An empty cell indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die). MCL denotes a pin that Must be Connected LOW. MCH denotes a pin that Must be Connected HIGH.

Figure 2 — Pinout Top View for 160-ball TFBGA (12 × 18 Grid)

2.4 Terminal Functions

Table 1 — Terminal Functions

Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0, DCKE1, DODT0, DODT1	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D0 ... D21	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	$\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes and parity checking, and as such at least one will be low when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN high) when at least one Chip Select input is LOW.
Re-driven outputs	Q0A...Q21A, Q0B ... Q21B, $\overline{\text{QCS}}$0-1A,B, QCKE0-1A,B, QODT0-1A,B	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN	SSTL_18	Parity input for the D0 ... D21 inputs; arrives one clock cycle after the corresponding data input.
Parity error output	$\overline{\text{PTYERR}}$	Open drain	When LOW, this output indicates that a parity error was identified associated with a valid address and/or command input. $\overline{\text{PTYERR}}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program inputs	CSGateEN	1.8 V LVCMOS	Chip Select Gate Enable. When HIGH, the D0..D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0...D21 inputs will be latched and re-driven on every rising edge of the clock.
Clock inputs	CK, $\overline{\text{CK}}$	SSTL_18	Differential system clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	MCL, MCH		Must be connected to a logic LOW or HIGH.
	$\overline{\text{RESET}}$	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{\text{RESET}}$ also resets the $\overline{\text{PTYERR}}$ signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.

2.5 Function Table

Table 2 — Function Table (each Flip Flop)

Inputs							Outputs			
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CSGate EN	CK	$\overline{\text{CK}}$	Dn, DODTn, DCKEn	Qn	$\overline{\text{QCS0}}$	$\overline{\text{QCS1}}$	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

2.5 Function Table (cont'd)

Table 3 — Parity and Standby Function Table

Inputs							Output
$\overline{\text{RESET}}$	$\overline{\text{DCS0}}$	$\overline{\text{DCS1}}$	CK	$\overline{\text{CK}}$	Σ of inputs = H (D0-D21)	PARIN[1]	$\overline{\text{PTYERR}}$[2]
H	L	H	↑	↓	Even	L	H
H	L	H	↑	↓	Odd	L	L
H	L	H	↑	↓	Even	H	L
H	L	H	↑	↓	Odd	H	H
H	H	L	↑	↓	Even	L	H
H	H	L	↑	↓	Odd	L	L
H	H	L	↑	↓	Even	H	L
H	H	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$\overline{\text{PTYERR}}_0$[3]
H	X	X	L or H	L or H	X	X	$\overline{\text{PTYERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

NOTE 1 PARIN arrives one clock cycle after the data to which it applies. All D inputs must be driven to a known state for parity to be calculated correctly.

NOTE 2 This transition assumes $\overline{\text{PTYERR}}$ is high at the crossing of CK going high and $\overline{\text{CK}}$ going low. If $\overline{\text{PTYERR}}$ is low, it stays latched low for two clock cycles or until $\overline{\text{RESET}}$ is driven low. CSGateEN is "don't care" for $\overline{\text{PTYERR}}$.

NOTE 3 If $\overline{\text{DCS0}}$, $\overline{\text{DCS1}}$, and CSGEN are driven high, the device is placed in low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the $\overline{\text{PTYERR}}$ output is driven low, it stays latched low for the LPM duration plus two clock cycles or until $\overline{\text{RESET}}$ is driven low.

2.6 Logic Diagram

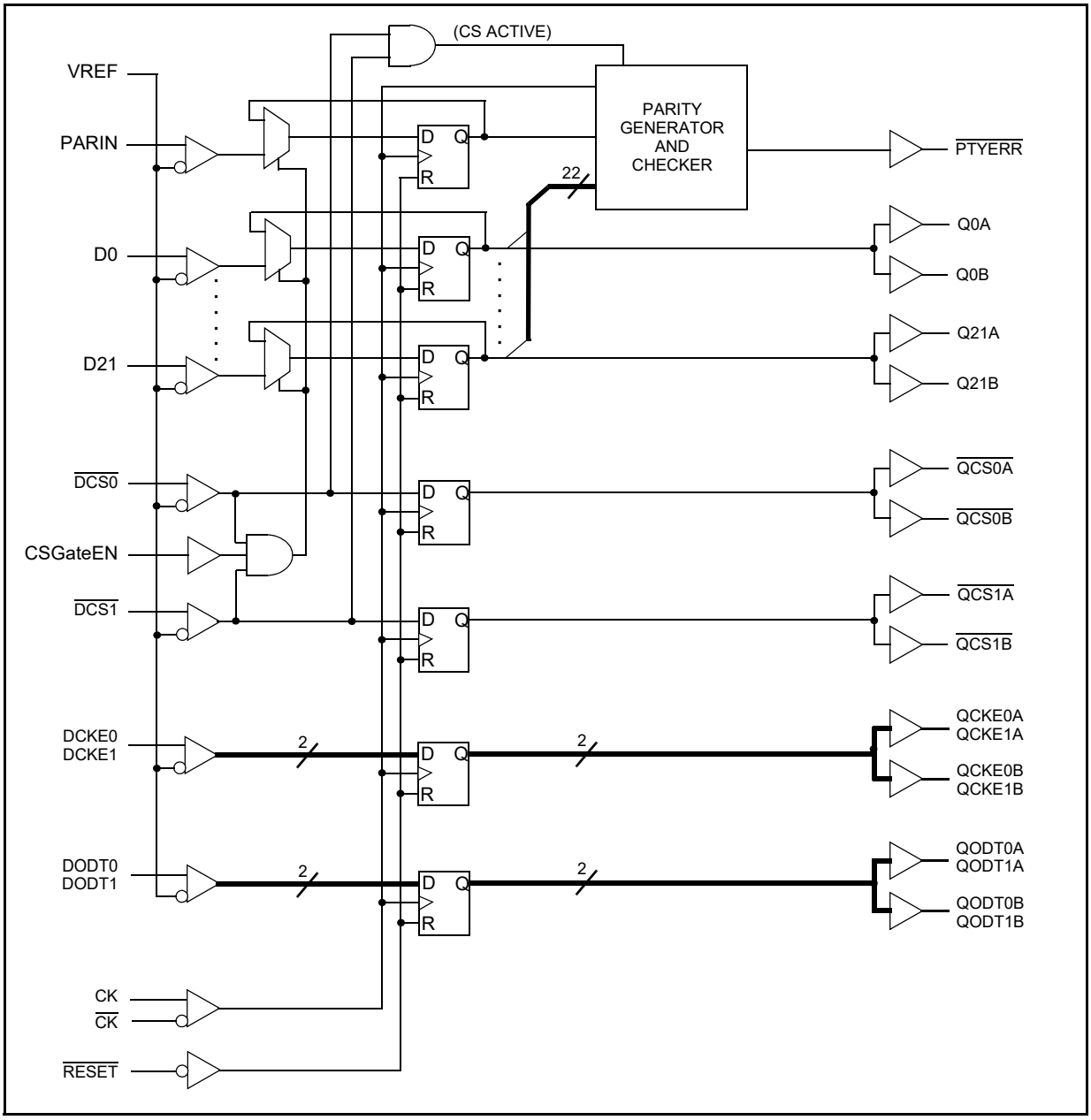


Figure 3 — Logic Diagram (Positive Logic)

2.7 Register Timing

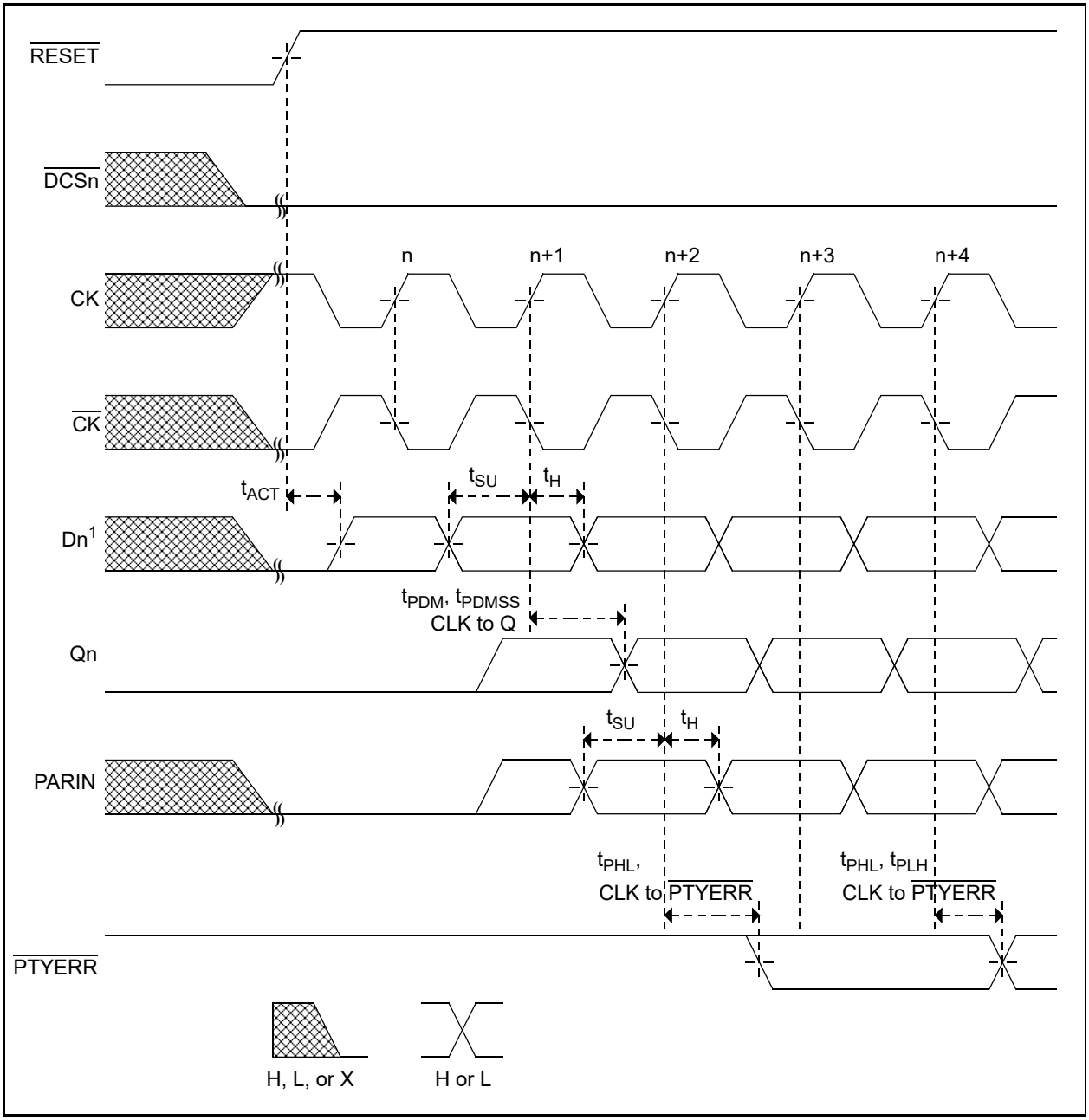


Figure 4 — $\overline{\text{RESET}}$ Switches from L to H

NOTE 1 After $\overline{\text{RESET}}$ is switched from LOW to HIGH, if $\overline{\text{DCS}}$0 or $\overline{\text{DCS}}$1 are held Low than all data and PAR_IN input signals must be held Low for a minimum time t_{ACT} (max.) to avoid false error. If $\overline{\text{DCS}}$0 or $\overline{\text{DCS}}$1 are held High than all data and PAR_IN input signals must be held at valid logic levels for a minimum time of t_{ACT} (max.) to avoid false error.

2.7 Register Timing (cont'd)

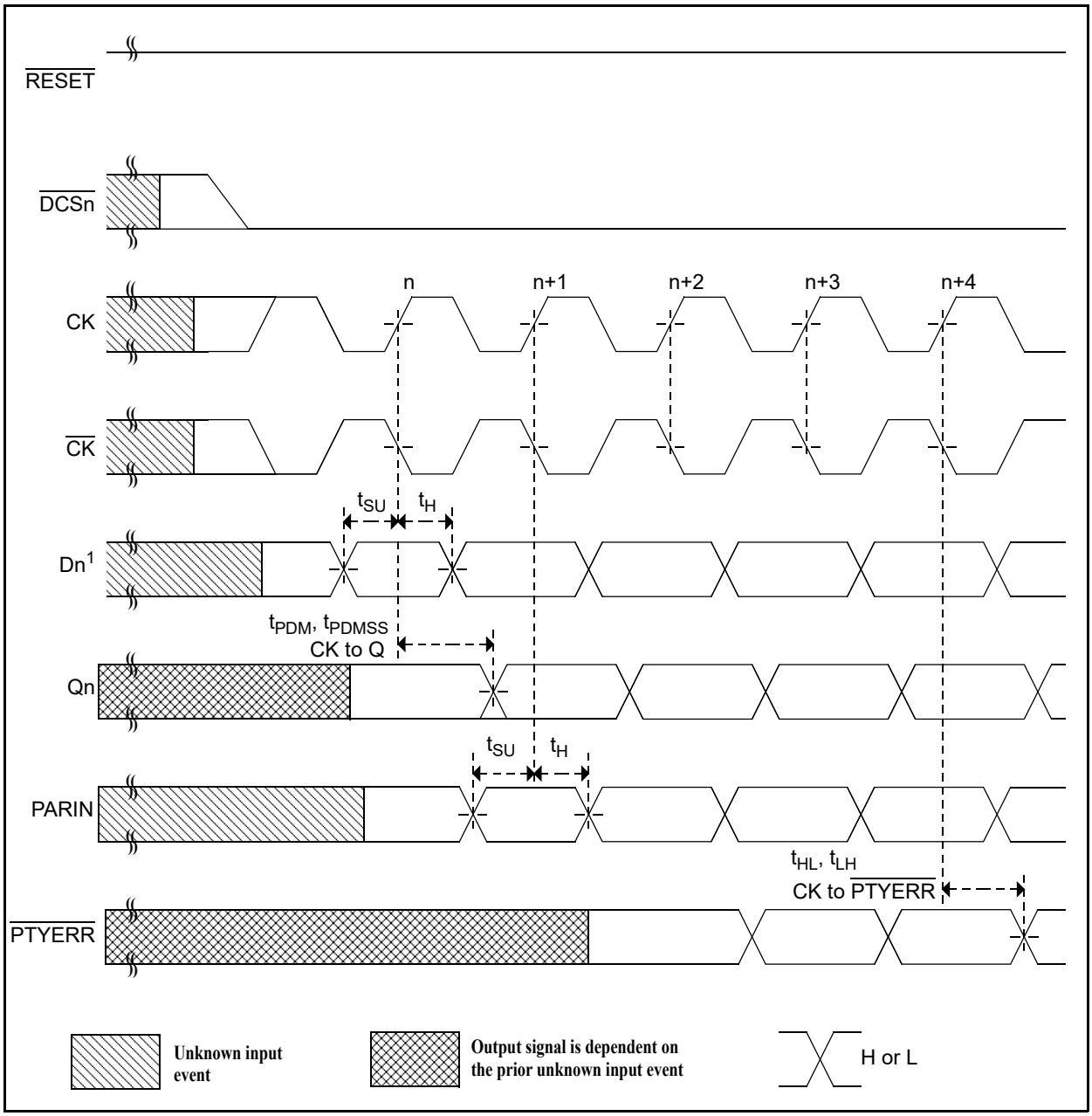


Figure 5 — $\overline{\text{RESET}}$ being Held High

2.7 Register Timing (cont'd)

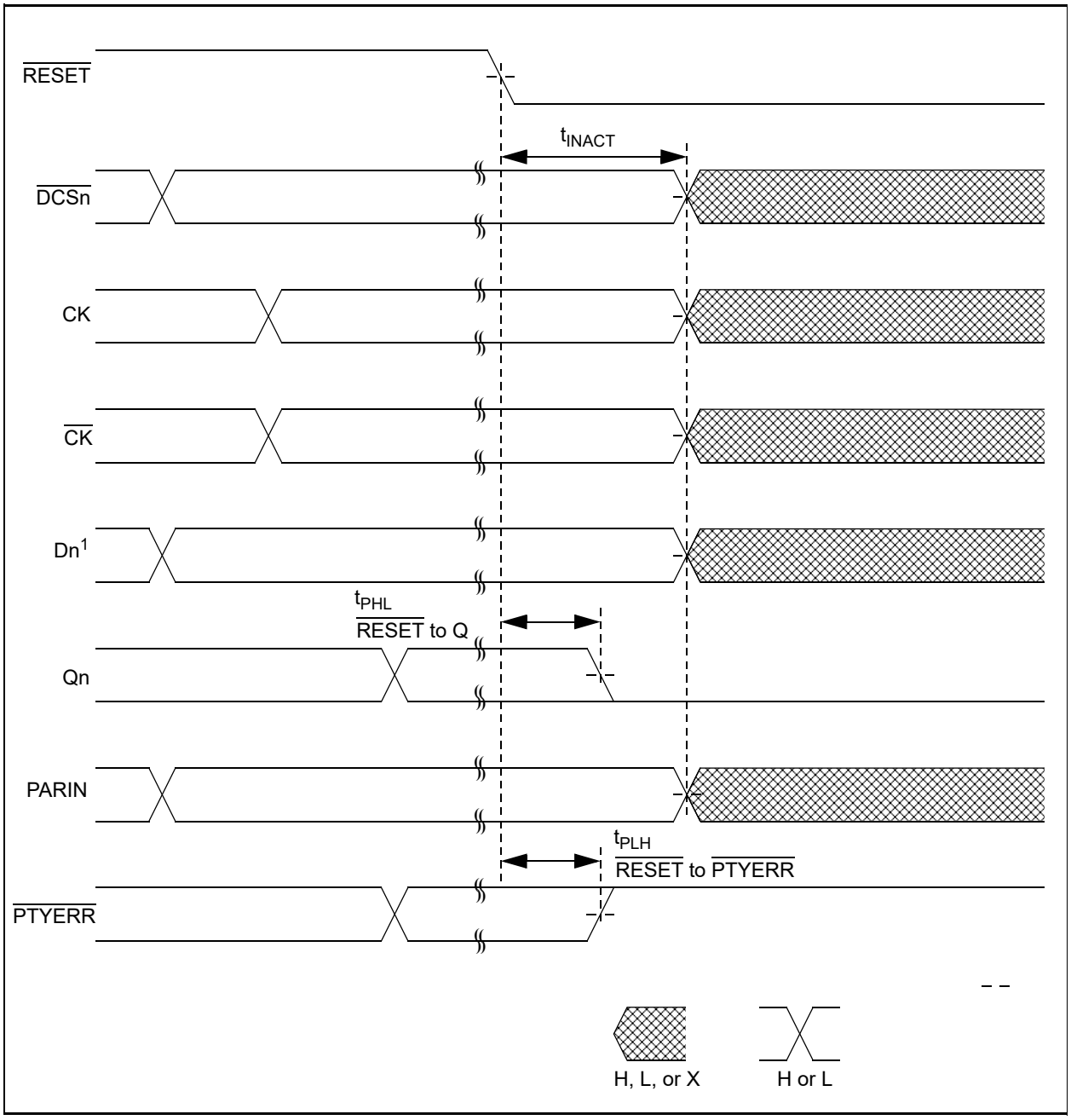


Figure 6 — $\overline{\text{RESET}}$ Switches from H to L

NOTE 1 After $\overline{\text{RESET}}$ is switched from HIGH to LOW, all data and clock input signals must be set and held at valid logic levels (not floating) for a minimum time of t_{INACT} (max.).

2.7 Register Timing (cont'd)

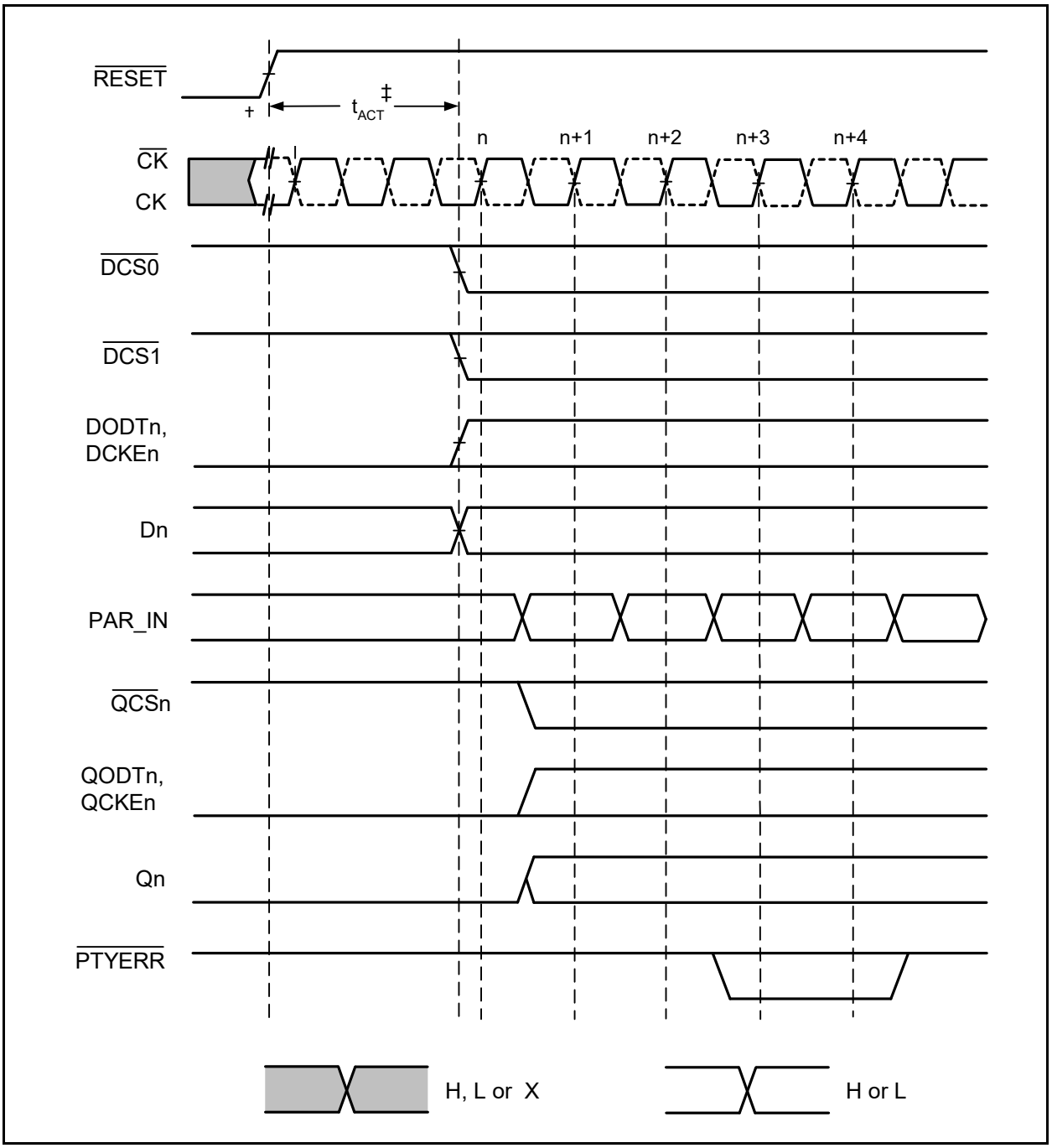


Figure 7 — Timing Diagram during Start-up when Data Inputs are Low Or High (Reset Switches from L to H)

‡ After $\overline{\text{RESET}}$ is switched from low to high, $\overline{\text{DCS0}}$ and $\overline{\text{DSC1}}$ must be held HIGH, DODT0, DODT1, DCKE0 and DCKE1 must be held LOW, and all other inputs must remain stable either LOW or HIGH (not floating) for a minimum time of t_{ACT} max.

2.7 Register Timing (cont'd)

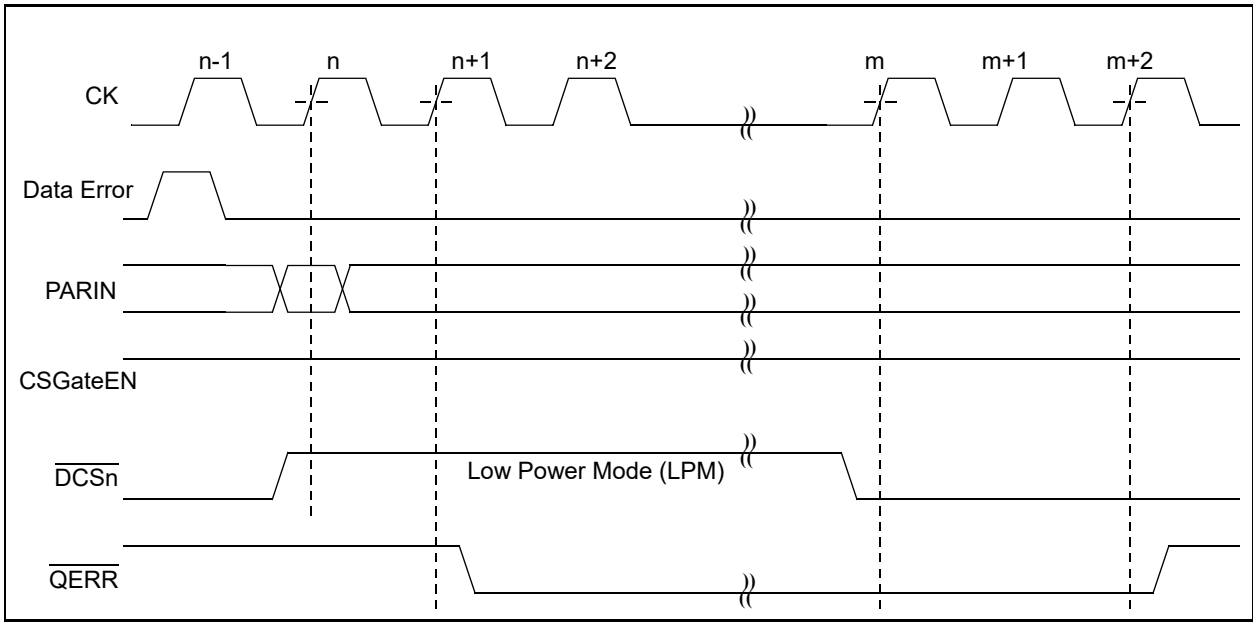


Figure 8 — Data Error Occurs at (n-1), LPM Occurs at (n)

2.8 Parity Logic Diagram

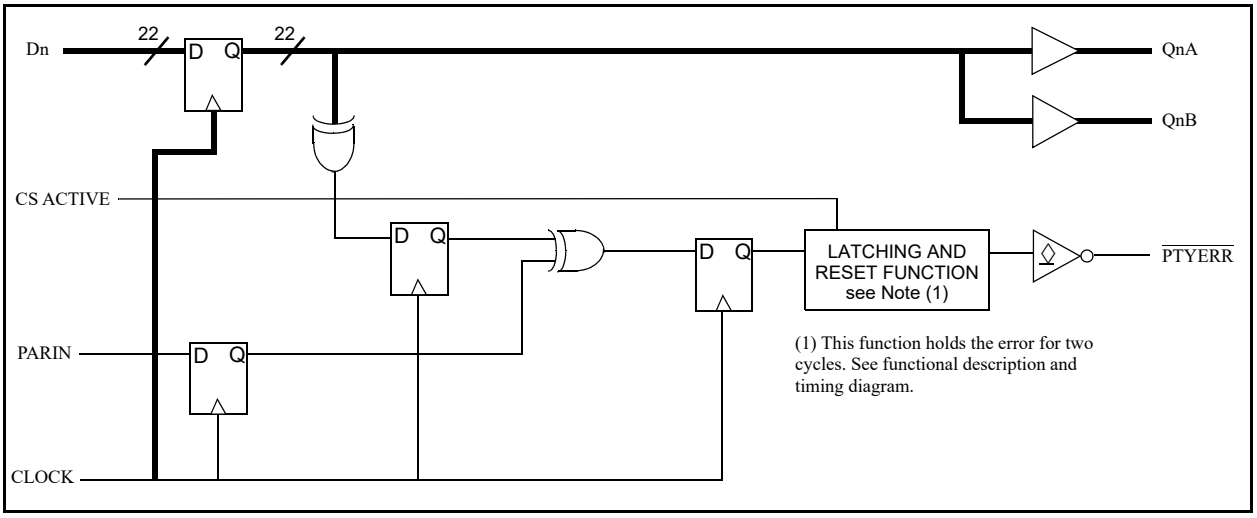


Figure 9 — Parity Logic Diagram

2.9 Absolute Maximum Ratings

Table 4 — Absolute Maximum Ratings over Operating Free-air Temperature Range[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		–0.5	+2.5	V
V_I	Receiver input voltage	Note 2	–0.5	+2.5	V
V_O	Driver output voltage	Note 2	–0.5	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$ or $V_I > V_{DD}$	-	–50	mA
I_{OK}	Output clamp current	$V_O < 0$ or $V_O > V_{DD}$	-	±50	mA
I_O	Continuous output current	$0 < V_O < V_{DD}$	-	±50	mA
I_{CCC}	Continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	Storage temperature		–65	+150	°C

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2.10 Recommended Operating Conditions

Table 5 — Recommended Operating Conditions[1]

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{DD}	Supply voltage		1.7	-	1.9	V
V_{REF}	Reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_{TT}	Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0	-	V_{DD}	V
V_{IH}	AC HIGH-level input voltage	Data inputs	V_{REF} + 250 mV	-	-	V
V_{IL}	AC LOW-level input voltage	Data inputs	-	-	V_{REF} – 250 mV	V
V_{IH}	DC HIGH-level input voltage	Data inputs	V_{REF} + 125 mV	-	-	V
V_{IL}	DC LOW-level input voltage	Data inputs	-	-	V_{REF} – 125 mV	V
V_{IH}	HIGH-level input voltage	$\overline{\text{RESET}}$, CSGateEN	$0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.35 \times V_{DD}$	V
V_{ICR}	Common-mode input voltage range	CK, $\overline{\text{CK}}$	0.675	-	1.125	V
V_{ID}	Differential input voltage	CK, $\overline{\text{CK}}$	600	-	-	mV
I_{OH}	HIGH-level output current		-	-	–6	mA
I_{OL}	LOW-level output current		-	-	6	mA
I_{ERROL}	$\overline{\text{PTYERR}}$ LOW-level output current		25	-	-	mA
T_{amb}	Operating ambient temperature in free-air		0	-	+70	°C

NOTE 1 The $\overline{\text{RESET}}$ input of the device must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is LOW.

2.11 DC Specifications

Table 6 — Electrical Characteristics over Recommended Operating Free-air Temperature Range

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH voltage	I_{OH} = -6 mA; V_{DD} = 1.7 V	1.2	-	-	V
V_{OL}	Output LOW voltage	I_{OL} = 6 mA; V_{DD} = 1.7 V	-	-	0.5	V
V_{ERROL}	$\overline{\text{PTYERR}}$ output LOW voltage	I_{ERROL} = 25 mA; V_{DD} = 1.7 V	-	-	0.5	V
I_I	Input current	All inputs, $V_I = V_{DD}$ or GND; V_{DD} = 1.9 V	-	-	±5	µA
I_{DD}	Static standby current	$\overline{\text{RESET}}$ = GND; V_{DD} = 1.9 V	-	-	200	µA
	Static operating current	$\overline{\text{RESET}} = V_{DD}$; V_{DD} = 1.9 V; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	80	mA
I_{DDD}	Dynamic operating current — clock only	$\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50% duty cycle. I_O = 0; V_{DD} = 1.8 V	-	Note 1	-	µA/ MHz
	Dynamic operating current — per each data input	$\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle. I_O = 0; V_{DD} = 1.8 V	-	Note 1	-	µA/ MHz
C_i	Input capacitance, Data inputs	$V_I = V_{REF}$ ± 250 mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
	Input capacitance, CK and $\overline{\text{CK}}$	V_{ICR} = 0.9 V; V_{ID} = 600 mV; V_{DD} = 1.8 V	2	-	3	pF
	Input capacitance, $\overline{\text{RESET}}$	$V_I = V_{DD}$ or GND; V_{DD} = 1.8 V	Note 1	-	Note 1	pF
NOTE 1 The vendor must supply this value for full device description.						

2.12 Timing Requirements

Table 7 — Timing Requirements over Recommended Operating Free-air Temperature Range (see Figure 6)

Symbol	Parameter		Min	Max	Unit
f_{clock}	Clock frequency		-	410	MHz
t_W	Pulse duration, CK, $\overline{CK}$ HIGH or LOW		1	-	ns
t_{ACT}	Differential inputs active time (See Notes 1 and 2)		-	10	ns
t_{INACT}	Differential inputs inactive time (See Notes 1 and 3)		-	15	ns
t_{SU}	Setup time	$\overline{DCS0}$ before CK↑, $\overline{CK}$↓, $\overline{DCS1}$ and CSGateEN high $\overline{DCS1}$ before CK↑, $\overline{CK}$↓, $\overline{DCS0}$ and CSGateEN high	0.6	-	ns
	Setup time	$\overline{DCS0}$ before CK↑, $\overline{CK}$↓, $\overline{DCS1}$ low and CSGateEN high or low $\overline{DCS1}$ before CK↑, $\overline{CK}$↓, $\overline{DCS0}$ low and CSGateEN high or low	0.5	-	ns
	Setup time	DODTn, DCKEn and data before CK↑, $\overline{CK}$↓	0.5	-	ns
	Setup time	PARIN before CK↑, $\overline{CK}$↓	0.5	-	ns
t_H	Hold time	$\overline{DCSn}$, DODTn, DCKEn and data after CK↑, $\overline{CK}$↓	0.4	-	ns
	Hold time	PARIN after CK↑, $\overline{CK}$↓	0.4	-	ns

NOTE 1 This parameter is not necessarily production tested.

NOTE 2 V_{REF} must be held at a valid input voltage level and data inputs must be held at valid logic levels for a minimum time of t_{ACT} (max) after $\overline{RESET}$ is taken high.

NOTE 3 V_{REF}, data, and clock inputs must be held at valid voltage levels (not floating) a minimum time of t_{INACT} (max) after $\overline{RESET}$ is taken low.

2.13 AC Specifications

Table 8 — Switching Characteristics over Recommended Operating Free-air Temperature Range (Unless Otherwise Noted) (see section 3.1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MAX}	Maximum input clock frequency		410	-	MHz
t_{PDM}	Propagation delay	Clock to output (see Note 1)	1.10	1.50	ns
t_{LH}	LOW-to-HIGH delay	CK and $\overline{CK}$ to $\overline{PTYERR}$	1.2	3	ns
t_{HL}	HIGH-to-LOW delay	CK and $\overline{CK}$ to $\overline{PTYERR}$	1	3	ns
t_{PLH}	LOW-to-HIGH propagation delay	from $\overline{RESET}$ to $\overline{PTYERR}$	-	3	ns
t_{PDMSS}	Propagation delay, simultaneous switching	Clock to output (See Notes 1 and 2)	-	1.60	ns
t_{PHL}	Propagation delay	Reset to output	-	3	ns
NOTE 1 Includes 350 ps of test-load transmission line delay. NOTE 2 This parameter is not necessarily production tested.					

2.14 Output Buffer Characteristics

Table 9 — Output Edge Rates over Recommended Operating Free-air Temperature Range (see section 3.2)

Symbol	Parameter	Conditions	Min	Max	Unit
dV/dt_r	rising edge slew rate		1	4	V/ns
dV/dt_f	falling edge slew rate		1	4	V/ns
dV/dt_Δ[1]	absolute difference between dV/dt_r and dV/dt_f		-	1	V/ns
NOTE 1 Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate).					

2.15 Output Buffer Overshoot/undershoot

This register is, among other applications, intended for use in the JEDEC reference designs as defined in JESD21-C, DDR2 Registered DIMM Design Specification. It is designed and characterized to produce overshoots/undershoots less than indicated in the table below, to comply with DDR2 SDRAM overshoot/undershoot requirements under worst case DRAM loading conditions (Min or Max), over DIMM operating conditions, and within the recommend operating conditions of the register listed in Table 5.

Table 10 — Output Overshoot/undershoot over Recommended Operating Free-air Temperature Range

DIMM Design Specification	Reference Design	Speed Bin	Overshoot (above V_{DD}) Max[1]	Undershoot (below GND) Min[1]
e.g., DDR2 Registered DIMM Design Specification Rev 2.0	e.g., F0	e.g., PC2-4200	e.g., 0.5 V	e.g., -0.5 V
...	...	...	...	...
...	...	...	...	...
NOTE 1 This value is verified by design and characterization, and may not be subject to production test.				

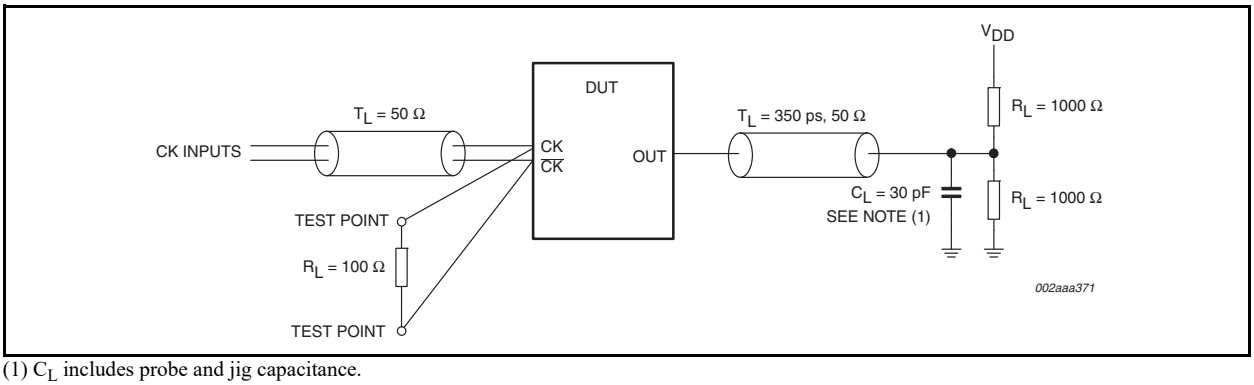
Register vendors are expected to supply the data in this table for the intended applications in their respective data sheets or in other suitable form.

3 Test Circuits and Switching Waveforms

3.1 Parameter Measurement Information (V_{DD} = 1.7 V to 1.9 V)

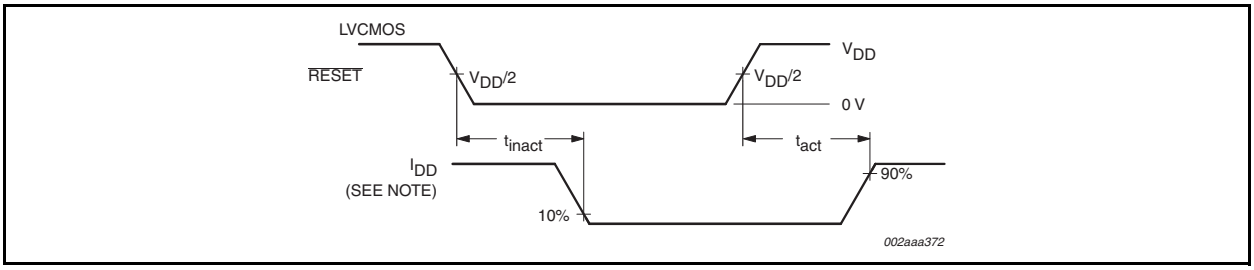
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



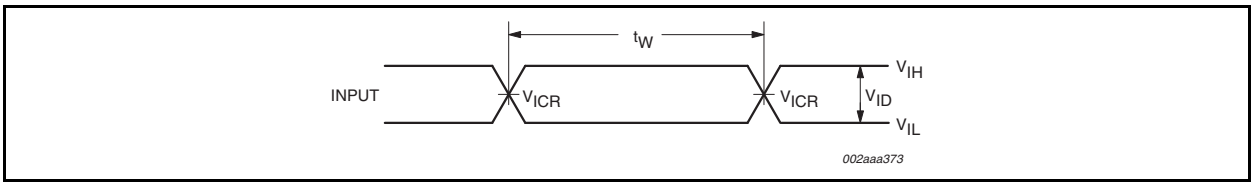
(1) C_L includes probe and jig capacitance.

Figure 10 — Load Circuit



I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Figure 11 — Voltage and Current Waveforms; Inputs Active and Inactive Times



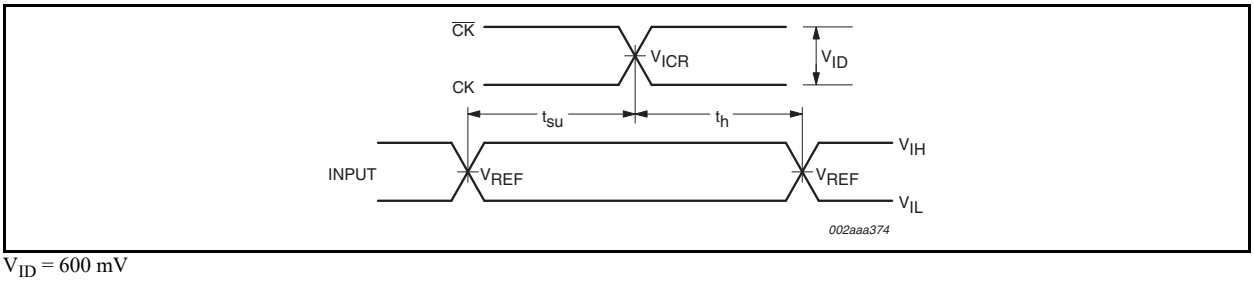
V_{ID} = 600 mV

$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{REF}$ − 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

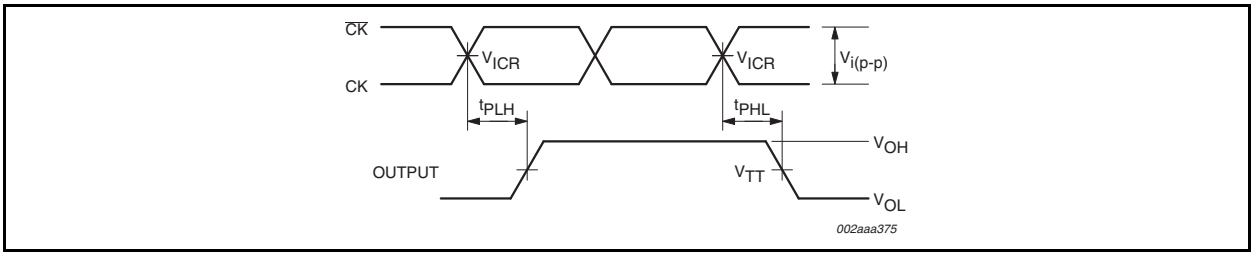
Figure 12 — Voltage Waveforms; Pulse Duration

3.1 Parameter Measurement Information (cont'd)



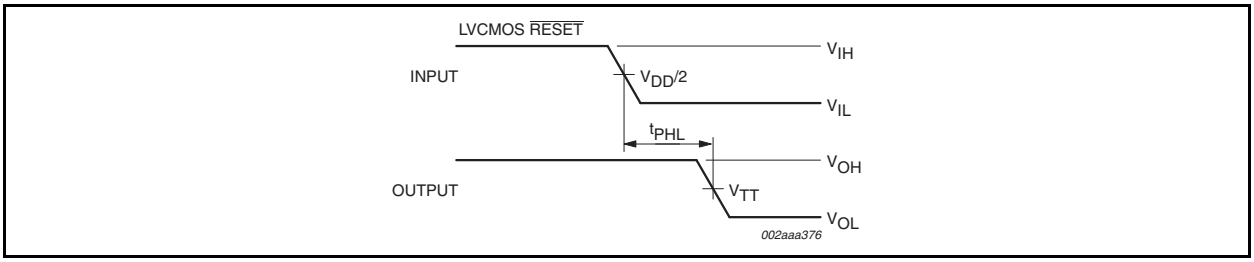
V_{ID} = 600 mV
$V_{REF} = V_{DD}/2$
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 13 — Voltage Waveforms; Set-up and Hold Times



t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 14 — Voltage Waveforms; Propagation Delay Times

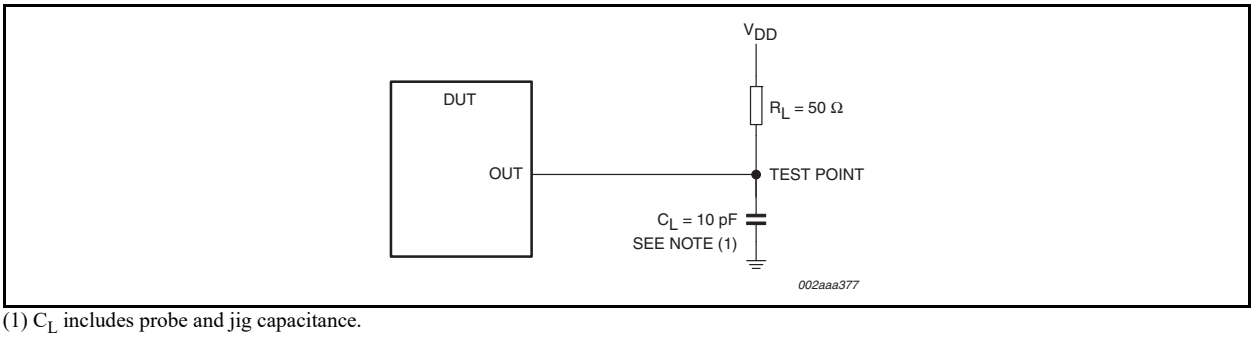


t_{PLH} and t_{PHL} are the same as t_{PD}.
$V_{IH} = V_{REF}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ – 250 mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs.

Figure 15 — Voltage Waveforms; Propagation Delay Times

3.2 Output Slew Rate Measurement Information (V_{DD} = 1.7 V to 1.9 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 16 — Load Circuit, HIGH-to-LOW Slew Measurement

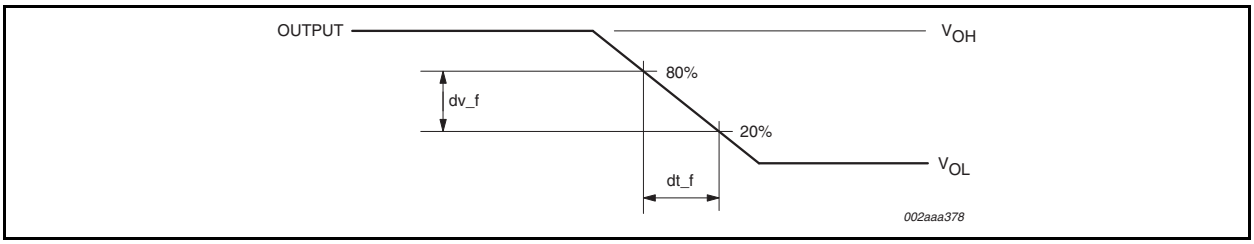
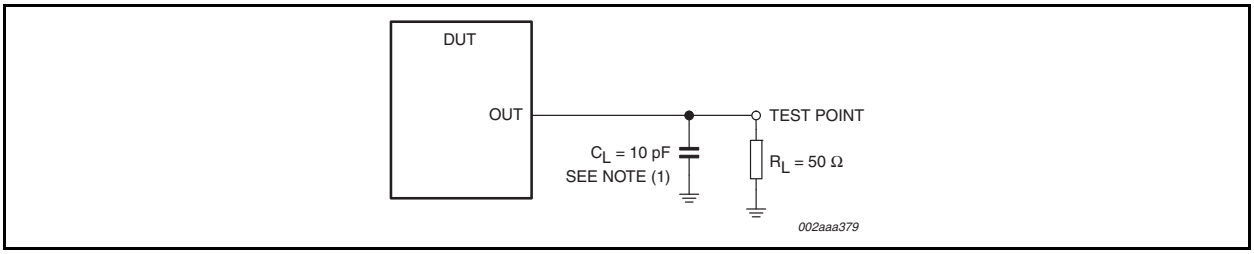


Figure 17 — Voltage Waveforms, HIGH-to-LOW Slew Rate Measurement



(1) C_L includes probe and jig capacitance.

Figure 18 — Load Circuit, LOW-to-HIGH Slew Measurement

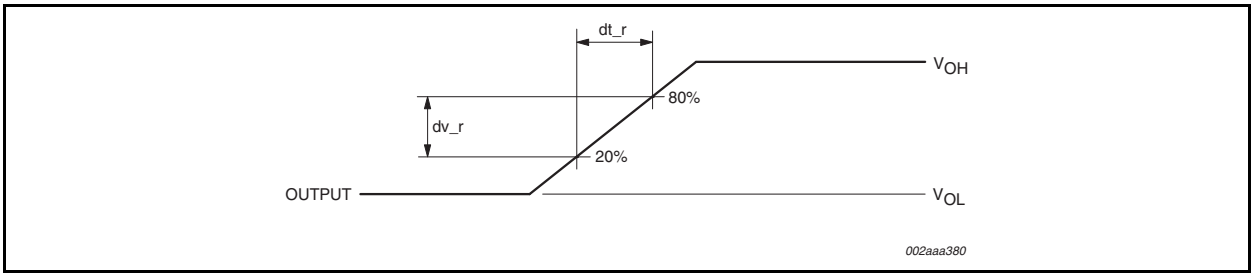
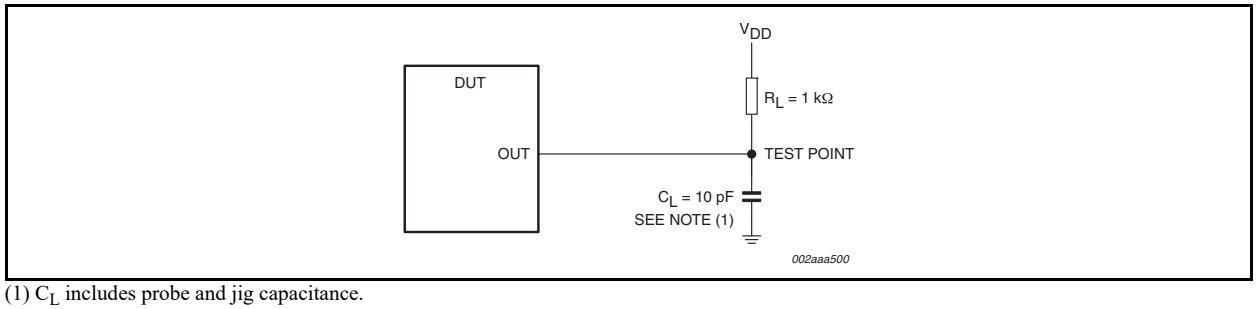


Figure 19 — Voltage Waveforms, LOW-to-HIGH Slew Rate Measurement

3.3 Error Output Load Circuit and Voltage Measurement Information (V_{DD} = 1.7 V to 1.9 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 20 — Load Circuit, Error Output Measurements

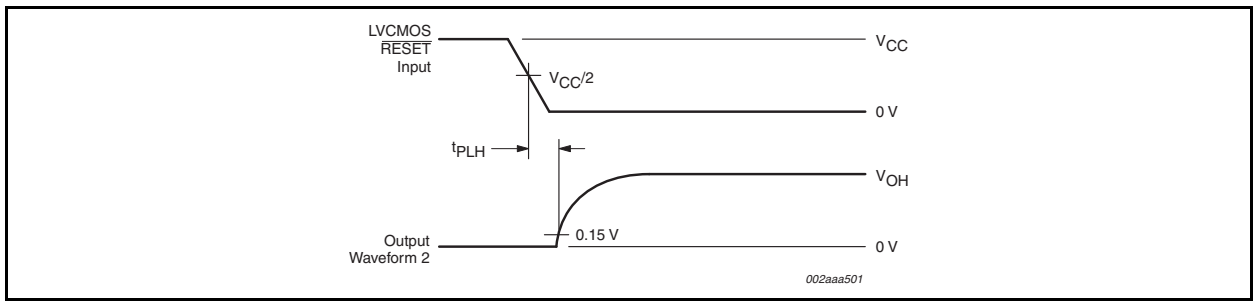


Figure 21 — Voltage Waveforms, Open-drain Output LOW-to-HIGH Transition Time with Respect to RESET Input

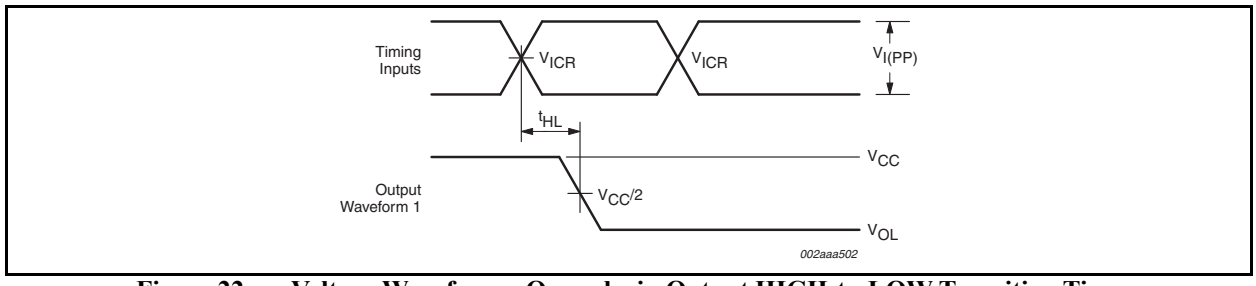


Figure 22 — Voltage Waveforms, Open-drain Output HIGH-to-LOW Transition Time with Respect to Clock Inputs

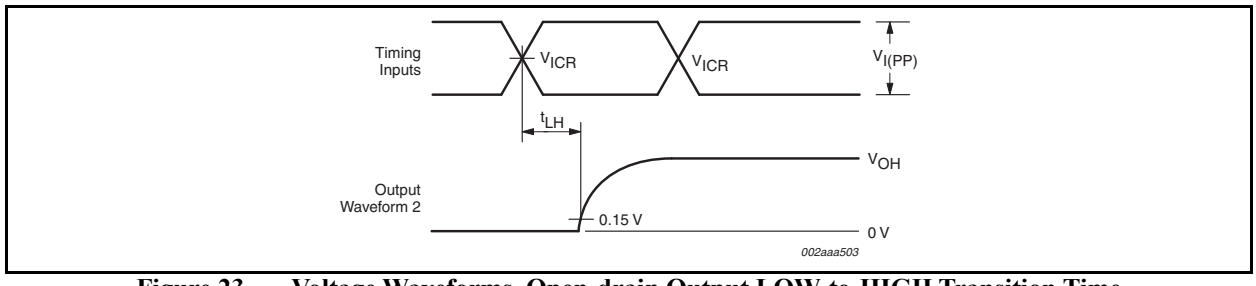


Figure 23 — Voltage Waveforms, Open-drain Output LOW-to-HIGH Transition Time with Respect to Clock Inputs

4 Reference to other Applicable JEDEC Standards and Publications

- JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*
- JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*
- JESD8-7, *1.8 V +/- 0.15 V (Normal Range), and 1.2 - 1.95 V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits.*
- JESD8-15, *Stub Series Terminated Logic for 1.8 V (SSTL_18).*
- JESD21-C, *Configuration for Solid State Memories.*
- JESD82-7A, *Definition of the SSTU32864 1.8 V Configurable Registered Buffer for DDR2 RDIMM Applications*
- JESD82-9A, *Definition of the SSTU32865 1.8 V Registered Buffer with Parity for DDR2 RDIMM Applications*

5 Annex A — (Informative) Difference between JESD82-24.01 and JESD82-24

Editorial revisions as follows:

- Table 1: Removed the word “master” from the description for Clock Inputs
- Updated the JEDEC logos to the latest version
- Changed Table captions, Figure captions, and headings to Initial Caps
- Formatted all tables to the JEDEC standard layout

Standard Improvement Form **JEDEC No. JESD82-24.01**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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