JEDEC STANDARD

DDR5 Data Buffer Definition (DDR5DB01) - Rev 1.1

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DDR5 DATA BUFFER DEFINITION (DDR5DB01)

(From JEDEC Board Ballot JCB-21-41, formulated under the cognizance of the JC-40.4 Subcommittee on Registered and Fully Buffered Memory Support Logic.)

1 Scope

This standard defines standard specifications for features and functionality, DC & AC interface parameters and test loading for definition of the DDR5 data buffer for driving DQ and DQS nets on DDR5 LRDIMM applications.

The purpose is to provide a standard for the DDR5DB01 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation DDR5DB01 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

This document uses DDR5DB01, Data Buffer, DB or Buffer interchangeably throughout for the DDR5DB01 device naming.

2 Mechanical Outline

The DDR5DB01 Package is a 55 - ball Fine-Pitch BGA (FBGA) with 0.5mm ball pitch, 15 x 5 grid with 20 balls depopulated, 7.8 mm x 2.73 mm as defined in MO-276 Issue N, Variation 1007.80x2.73-5030-55Y[1]. The device pinout options support the register link inputs in the center columns to support signal routing matching from alternate sides of the DIMM to the DDR5RCD01. Corresponding host side data/strobe balls are placed in a way to match the corresponding pin location on the connector if the device is mounted on the backside of an LRDIMM module. Each V_{DD} and V_{SS} is located close to an associated no ball position to allow low-cost via technology combined with the small 0.50 mm ball pitch.

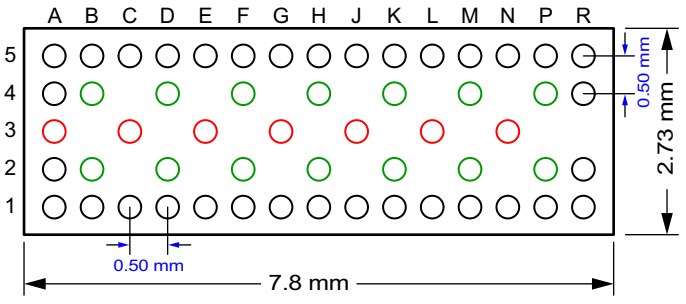


Figure 1 — 55 Ball Configuration 15 x 5 (TOP VIEW)

Ball pitch: 0.50 mm x 0.50 mm, Size (ø 0.3 mm), SMD Pad SRO (ø 0.275 mm). X-ray view from topside.

1. This variation defines a maximum package thickness of 1.00 mm. The DDR5DB01 must comply with a minimum thickness of 0.80 mm.

2.1 Pinout 15 x 5

Table 1 specifies the pinout for the DDR5DB01. The device has (mostly) symmetric pinout with host interface at the south side and DRAM interface at the north side.

Table 1 — Ball Assignment -55 ball FBGA, 15 x 5 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
5	MDQ7	MDQ5	MDQ6	MDQ4	MDQS1_t	MDQS1_c	BCOM0	BCOM1	BCOM2	MDQS0_c	MDQS0_t	MDQ3	MDQ1	MDQ2	MDQ0
4	BRST_n	VSS		VSS		VSS		VSS		VSS		VSS		VSS	LB TXDQ
3	VDD		VDD		VDD		VDD		VDD		VDD		VDD		
2	ZQCAL	VSS		VSS		VSS		VSS		VSS		VSS		VSS	LB TXDQS
1	DQ7	DQ5	DQ6	DQ4	DQS1_t	DQS1_c	BCK_c	BCK_t	BCS_n	DQS0_c	DQS0_t	DQ3	DQ1	DQ2	DQ0

2.2 Terminal Functions for 55-Ball Data Buffer Package Configuration

Table 2 — Terminal Functions for 55-Ball Package Configuration

Signal Group	Signal Name	Type	Description
Data buffer control inputs	BCS_n	POD V_{REF} based[1]	Chip Select Input
	BRST_n	CMOS	Level Triggered Reset, when BCOM is ‘000’ or ‘111’resets device to default values, otherwise used for BCOM Strap mode defined in “BCOM Training Mode (BCOMTM) - Data Buffer Interface” on page 51.
	BCOM[2:0]	POD V_{REF} based[1]	Register communication bus for data buffer programming and control access
Clock inputs	BCK_t, BCK_c	POD differential	Differential clock input pair
Host Interface	DQ[3:0] DQ[7:4]	POD V_{REF} based bidirectional	Host side data lower nibble Host side data upper nibble
	DQS0_t DQS0_c DQS1_t DQS1_c	POD differential bidirectional	Host side data strobe for lower nibble Host side data strobe complement for lower nibble Host side data strobe for upper nibble Host side data strobe complement for upper nibble
DRAM Interface	MDQ[3:0] MDQ[7:4]	POD V_{REF} based bidirectional	DRAM side data lower nibble DRAM side data upper nibble
	MDQS0_t MDQS0_c MDQS1_t MDQS1_c	POD differential bidirectional	DRAM side data strobe for lower nibble DRAM side data strobe complement for lower nibble DRAM side data strobe for upper nibble DRAM side data strobe complement for upper nibble
Loopback	LBTXDQ LBTXDQS	POD	Loopback DQ Transmit Loopback DQS Transmit

Table 2 — Terminal Functions for 55-Ball Package Configuration

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration

1. These receivers use the internal BVref as the switching point reference

3 Device Description and Features

3.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.1 V, V_{DD} operation. The device has a dual 4-bit host bus interface that is connected to a memory controller and a dual 4-bit DRAM interface that is connected to two x4 DRAMs. It also has an input-only control bus interface that is connected to a DDR5 Register.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are V_{DD} terminated drivers optimized to drive single or dual terminated traces in DDR5 LRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR5DB01 for driving out the DQ outputs on the opposite side of the device.

The clock inputs BCK_t and BCK_c are used to sample the control inputs BCS_n and BCOM[2:0]. The BCOM[2:0] inputs are used to write device internal control registers. The buffer control word (RW) mechanism is described in more detail in Section 9 BCK_t, BCK_c, BCS_n and BCOM[2:0] signals are terminated to VDDQ on the DDR5 LRDIMM.

The DDR5DB01 also supports dedicated pins for ZQ calibration.

3.2 Power-on Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. After the voltage ramp, stable power is held for a minimum of t_{RINIT1} in the Power-on RESET state. During this time, a static value of BCOM[2] = BCOM[1] = BCOM[0] = HIGH or LOW shall be applied to ensure Normal Operation RESET. In addition to t_{RINIT1}, t_{Strap_Hold} also applies (see Table 155 on page 163). In the Power-on RESET state all Strobe and Data input receivers are disabled and can be left floating. In the Power-on RESET state, all control registers are restored to their default states (which is “0”, except when explicitly defined otherwise). All Strobe and Data outputs must float. In the Power-on RESET state the data buffer is in low-power state and host interface and DRAM interface ODT terminations are disabled.

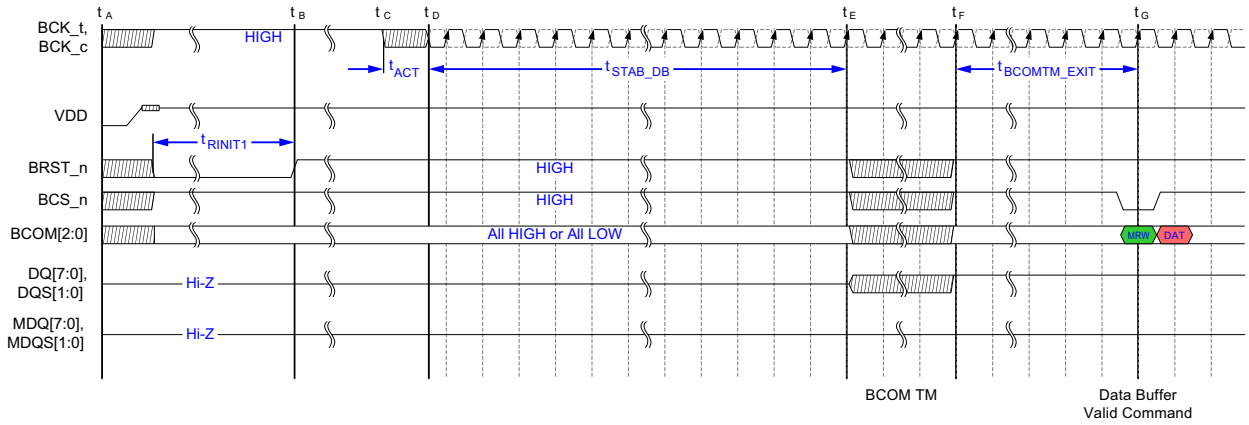


Figure 2 — Data Buffer Initialization Sequence

3.2.1 Clock Stabilization Time t_{STAB_DB}

During PLL stabilization time t_{STABDB} the data buffer is not fully operational. To ensure correct operation, some rules apply to the inputs of the buffer:

- BCS_n must remain HIGH.

These rules apply to any instance where stabilization time t_{STAB_DB} is required:

- Exit from Reset state
- Exit from clock stop power down
- Changing clocking related registers

Since the data buffer has not reached a stable state the termination on the host interface will be undefined before the end of the stabilization time.

After reset and after the stabilization time (t_{STAB_DBDATA}) the DB must meet the input setup- and hold specification, as well as accept and transfer input signals to the corresponding outputs.

BCOM VREF and Command Timing settings are set through a Static mode defined in the BCOM Training section.

3.2.2 Reset Initialization with Stable Power

The timing diagram in Figure 3 depicts the initialization sequence with stable power and clock. For this sequence, the BCK continues toggling with stable phase and frequency. The data buffer remains in the RESET state for a minimum of t_{RINIT1}. During this time, a static value of BCOM[2] = BCOM[1] = BCOM[0] = HIGH or LOW shall be applied to ensure Normal Operation RESET. In addition to t_{RINIT1}, t_{Strap_Setup} and t_{Strap_Hold} also apply (see Table 155 on page 163). In the RESET state, all non-sticky control registers are restored to their default states.

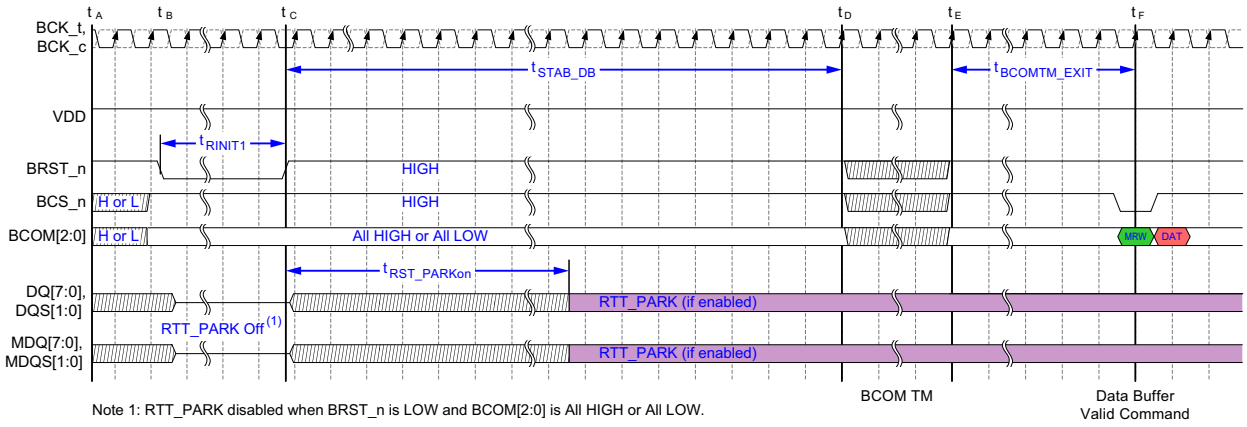


Figure 3 — Data Buffer Reset with Stable Power and Clock

Figure 4 depicts the initialization sequence with stable power and stopped clock. For this sequence, the BCK clock is allowed to stop (i.e., BCK_t = BCK_c = HIGH). The data buffer remains in the RESET state for a minimum of t_{RINIT1}. During this time, a static value of BCOM[2] = BCOM[1] = BCOM[0] = HIGH or LOW shall be applied to ensure Normal Operation RESET. In addition to t_{RINIT1}, t_{Strap_Hold} also applies (see Table 155 on page 163). In the RESET state, all non-sticky control registers are restored to their default states.

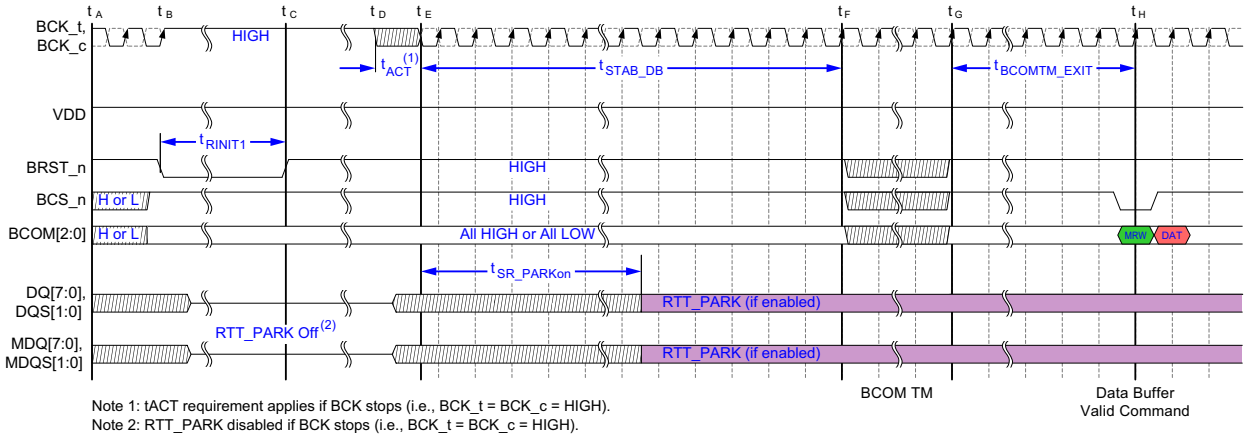


Figure 4 — Data Buffer Reset with Stable Power and Stopped Clock

3.3 Transparent Mode

Transparent mode is enabled in the DDR5DB01 by setting RW82[0] to 1. While in transparent mode, the DB does not interpret BCS_n and BCOM commands as defined in Table 12, “Data Buffer Control Bus Command Truth Table”. For BCS_n input value of “1” and BCOM[2:0] input values of “111” it directs the data flow from host interface to DRAM interface, and it enables or disables the on-die termination at the host interface based on the setting in RW82[1]. For BCS_n input value of “1” and BCOM[2:0] input values of “000”, the Data Buffer directs the data flow from DRAM interface to host interface and it enables or disables the on-die termination at the DRAM interface based on the setting in RW82[1]. Any other input values of BCS_n and BCOM[2:0] are invalid.

The Data Buffer does not support high-speed changes in direction of data flow. The host will wait for 32 clock cycles of settling time after the direction in data flow is reversed in transparent mode.

In transparent mode the Data Buffer statically enables the input receivers of the interface that is receiving signals and is permanently enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the DB. Propagation delays for all the signals within each DQ/DQSMDQ/MDQS nibble must be matched closely enough to meet parameter D_{TPM_DQ} in Table 156. All the clock frequencies available in test mode and nor-mal operation mode in the Data Buffer will be supported in transparent mode. DQSs are treated as differential. This means if a DQSx_t and the corresponding DQSx_c are both HIGH or both LOW, the associated MDQSx_t and MDQSx_c will be invalid. MDQSs are treated as differential as well.

In transparent mode, the strength of the DRAM interface termination is controlled by the MDQ RTT Buffer Control Word and the strength of the Host Interface termination is controlled by the RTT_PARK Buffer Control Word.

To exit transparent mode in the DDR5DB01 device, it is necessary to apply power cycle or Normal Operation RESET (as defined in Table 27, “BCOM Strap for Data Buffer Training States,” on page 52).

Table 3 — DB Termination Control in Transparent Mode

BCS_n, BCOM[2:0]	TPM Termination Control RW82[1]	Host Interface Termination	DRAM Interface Termination
= “1111”	0	ON	OFF
	1	OFF	OFF
= “1000”	0	OFF	ON
	1	OFF	OFF

3.4 DQ Pass-Through Mode

For initialization and training applications, DDR5DB01 supports DQ pass through mode.

DQ pass-through mode is enabled in the DDR5DB01 by setting RW82[2] to 1. While in the DQ pass-through mode, the DDR5DB01 only supports MRW BCOM commands and any commands other than MRW are not allowed.

When DQ pass-through mode is enabled, if the direction select control word bit RW82[3] is set to 0 (default value), then DQ pass-through mode is enabled in the Write direction from host interface DQ/DQS to DRAM interface MDQ/MDQS. The DDR5DB01 directs the data flow from host interface to DRAM interface, and it enables or disables the on-die termination at the host interface based on the setting in RW82[1].

When DQ pass-through mode is enabled, if the direction select control word bit RW82[3] is set to 1, then DQ pass-through mode is enabled in the read direction from DRAM interface MDQ/MDQS to host interface DQ/DQS. The DDR5DB01 directs the data flow from DRAM interface to host interface, and it enables or disables the on-die termination at the DRAM interface based on the setting in RW82[1].

In the DQ pass-through mode, the strength of the DRAM interface termination is controlled by the MDQ RTT Buffer Control Word and the strength of the Host Interface termination is controlled by the RTT_PARK Control Word. In the DQ pass-through mode, the Data Buffer statically enables the input receivers of the interface that is receiving signals and enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the DB. Propagation delays for all the signals within each DQ/DQS-MDQ/MDQS nibble must be matched closely enough to meet parameter D_{TPM_DQ} in Table 156. All the clock frequencies available in test mode and normal operation mode will be supported. DQSs are treated as differential. This means if a DQSx_t and the corresponding DQSx_c are both HIGH or both LOW, the associated MDQSx_t and MDQSx_c will

be invalid. MDQSs are treated as differential as well.

Table 4 — DB Termination Control in DQ Pass-Through Mode[1]

DQ pass through mode	Termination Control RW82[1]	Host Interface Termination	DRAM interface Termination
Enabled for write direction	0 (default)	ON	-
	1	OFF	-
Enabled for read direction	0 (default)	-	ON
	1	-	OFF

1. The DB termination control during DQ pass-through mode is irrelevant to the {BCS_n, BCOM} patterns.

After the DQ pass-through mode is enabled or disabled, the controller will wait for 32 clock cycles of data path settling time.

The DDR5DB01 exits the DQ pass-through mode when RW82[2] is set to 0.

3.5 Loopback Mode

With loopback circuit the DDR5DB01 can feed a received signal or data back out to an external receiver for debugging, testing, and/or training purposes. Loopback is necessary in order for the host memory controller or test instrument to immediately read back data that was written to the Data Buffer without having to issue multiple DRAM WRITE/READ commands. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis.

For example, at BER=10^{-16}:

1. There is not enough memory depth in the DRAM to store all the 10^{16} data.
2. The amount of time to perform multiple WRITE/READ commands to and from the array is prohibitively long.
3. Since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the host or memory controller must also manage Refreshes during testing to ensure data retention.
4. Limited pattern depth means limited Intersymbol Interference (ISI). Loopback is a necessity for characterizing the receiver without the limitations and complexities of other traditional methods.

3.5.1 Loopback Output Definition

The Loopback circuitry requires two output pins (one single ended Loopback data, LBTXDQ, and one single ended Loopback strobe, LBTXDQS). The Loopback circuitry also consists of multiplexers to select the DQ and Phase for Loopback. Pin assignment location for Loopback pins are defined as R4 for LBTXDQ and R2 for LBTXDQS.

It is the Host's responsibility to put the device into a normal operating mode prior to sending BCOM commands.

The default RTT state for Loopback when RW8D[0] = 0 is RZQ/5 (48 Ω), designated by RW8E[2:0] = 101. In this state, both the LBTXDQS and LBTXDQ outputs are disabled. If the Loopback pins of several Data Buffer devices are connected together and some devices need disabled termination, there is RTT_OFF option available by setting RW8E[2:0] = 000.

Enabling the Loopback Output value via RW8D[0] = 1 will result in the LBTXDQS and LBTXDQ pins to transition from the RTT_Loopback state to a DB Drive State.

The LBTXDQS output will transition with the differential input crossing point of DQS_t/DQS_c, plus latency.

The LBTXDQ output will transition with the receiver data state of the DQ pin selected by RW8D[4:2].

Table 5 — Loopback Output Definition

Condition	LBTXDQS	LBTXDQ	NOTE
Loopback Disabled	RTT_Loopback	RTT_Loopback	
Loopback Enabled	Selected Phase	Selected Phase and Selected DQ	

3.5.2 Loopback Phase

Due to the high data rates of the DDR5 Data Buffer, Loopback is implemented with 2-way interleaved outputs. With a 2-way implementation, the DQS and selected DQ will be sampled and output every 1 CK or 2 UI. To be able to sample all bits with a 2-way interleave implementation, the Loopback Phase Select programmed in RW8D[5] allows selection of the DQS/DQ phase to be output. In 2-way mode, Phase A and Phase B are valid options.

Figure 5 shows an example of a Loopback implementation for 2-way interleave Data Buffer. This example requires a divided clock to produce DQS_0 (PHASE A) and DQS_180 (PHASE B). The output of the DQ slicer runs at 1/2 the speed as received data. In a 2-way interleave design, the data is received at full speed, but internally the data is latched only at half speed.

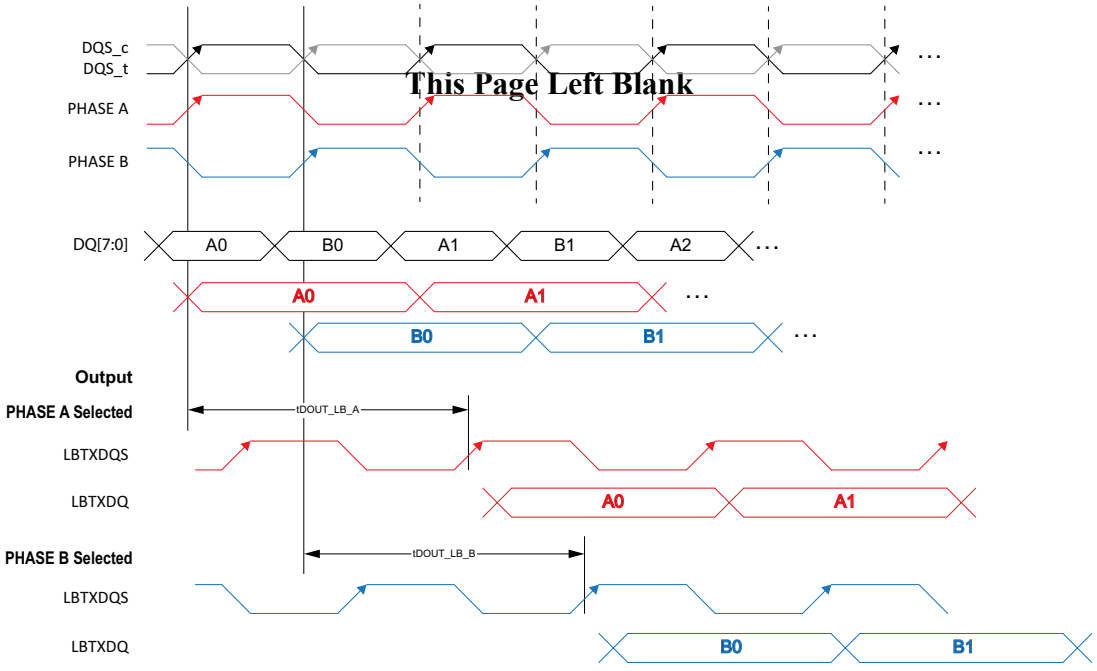


Figure 5 — Data Buffer Internal Phase Selection

3.5.3 Loopback Output Mode

Loopback Output Mode selects whether to output LBTXDQS and LBTXDQ in DQS Qualified Output Mode or WE Qualified Output Mode, based on RW8D[1]. In the default DQS Qualified Output Mode (RW8D[1] = 0), the selected DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase. In WE Qualified Output Mode (RW8D[1] = 1), the selected DQ state will be output on LBTXDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

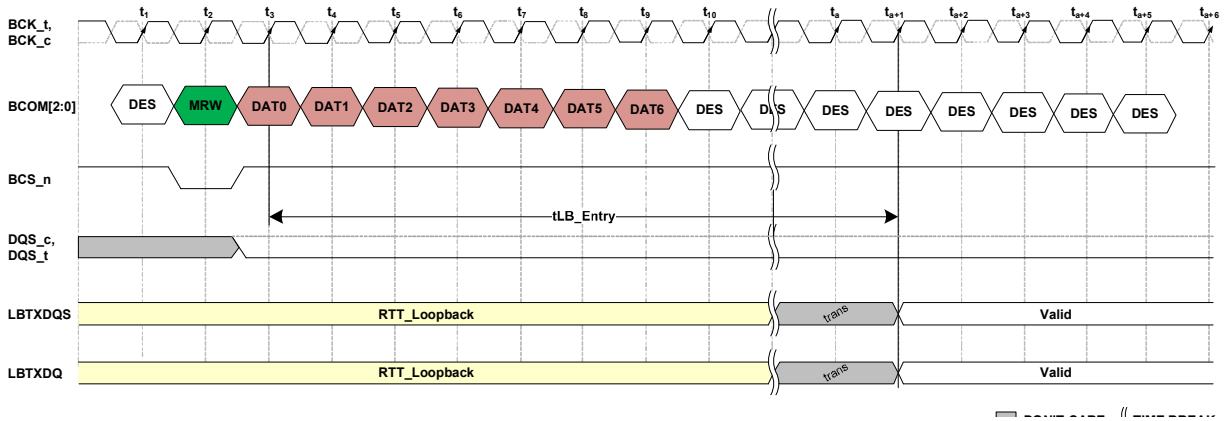


Figure 6 — Loopback Mode Entry for Output Modes Qualified by DQS or Qualified by WE

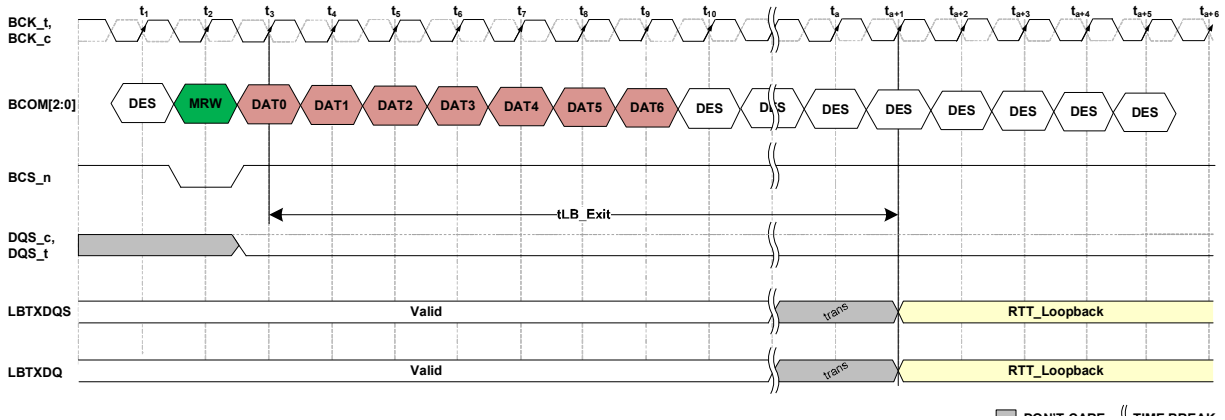


Figure 7 — Loopback Mode Exit for Output Modes Qualified by DQS or Qualified by WE

3.5.3.1 Loopback DQS Qualified Output Mode (Default)

In DQS Qualified Output Mode (RW8D[1] = 0), the selected DQ state is captured with every DQS_t/DQS_c toggle for the selected Loopback Phase and output on LBTXDQ. The LBTXDQS output will be delayed by tDOUT_LB_* from the selected DQS_t/DQS_c Loopback Phase. Since no Write commands are required in DQS Qualified Output Mode, MR settings pertaining to preamble, postamble, CWL are ignored by the Loopback function.

Additional requirements for DQS Qualified Output Mode:

- DQS must be driven differentially LOW (DQS_t LOW, DQS_c HIGH) prior to entry into DQS Qualified Output Mode.
- DQS_t/DQS_c must be continuously driven during Loopback operation. (Hi-Z state not allowed.)
- Only DSEL or MRW commands can be applied at BCOM[2:0]/BCS_n command pins during DQS Qualified Output Mode.

No DFE Reset is assumed after first rising edge of DQS_t. DRAM WR/RD operations are not supported after entering DQS Qualified Output Mode.

3.5.3.2 Loopback DQS Qualified Output Mode Timing Diagrams

Loopback DQS Qualified Output Mode entry and output example timing diagrams are shown below. The timing diagrams in Figure 8 and Figure 9 assume there have been other previous bursts of Loopback data.

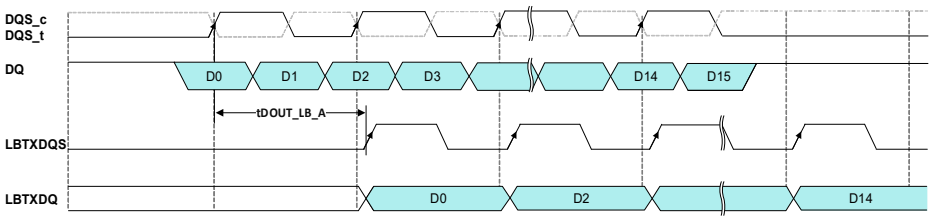


Figure 8 — Phase A is selected - DQS Qualified Output Mode

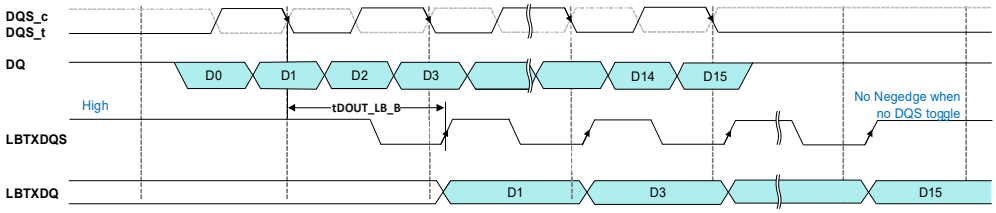


Figure 9 — Phase B is selected - DQS Qualified Output Mode

3.5.3.3 Loopback WE Qualified Output Mode

In WE Qualified Output Mode (RW8D[1] = 1), Loopback data is only generated during the write burst, so it is effectively masked for the DQS toggles during the preamble or postamble. Normal Write operation for the Command, DQS and DQ is assumed. MR settings pertaining to preamble, postamble, CWL apply, as they do for any Write command.

Implementation of 2-way interleave Loopback introduces complexity in Write Burst Mode when the DQS toggle is not continuous.

If the DQS toggle is continuously generated by Write commands spaced BL/2, Loopback will align the LBTXDQS/

LBTXDQ output with the selected phase for all write bursts. If the DQS toggle is not continuous due to gaps in Write commands spaced greater than BL/2, LBTXDQS/LBTXDQ may not align with the selected phase after the first write burst unless the “gap” is at least 16 CK (Write, BL/2 + 16CK, Write).

Table 6 — Loopback Output Phase

Write to Write Separation	Phase	NOTE
X = BL/2	Selected	
BL/2 < X < BL/2 + 16	Determined via analysis of specific conditions	1
X >= BL/2 + 16	Selected	

Note 1: Specific conditions include selected phase, data rate, preamble, postamble and write burst gap duration.

In the case where continuous bursts are not issued in Loopback WE Qualified Output Mode, selection of Phase B may result in the last tHW_LBTXDQS width of a burst that does not comply with spec.

Additional requirements for WE Qualified Output Mode:

Write Leveling training is required prior to Write Burst Loopback operation.

All Write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data sent to DRAM, and the Loopback pins may not output the captured input data as expected.

3.5.3.4 Loopback WE Qualified Output Mode Timing Diagrams

Loopback WE Qualified Output Mode timing diagram examples are shown below. The timing diagrams in Figure 10 through Figure 25 assume there have been other previous bursts of Loopback data and the Loopback settings in RW8D have not been modified.

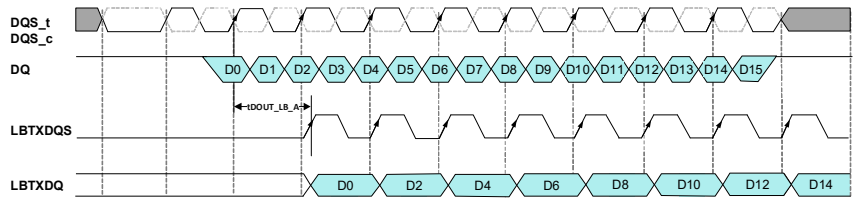


Figure 10 — Phase A: 2tCK or 3tCK Preamble – WE Qualified

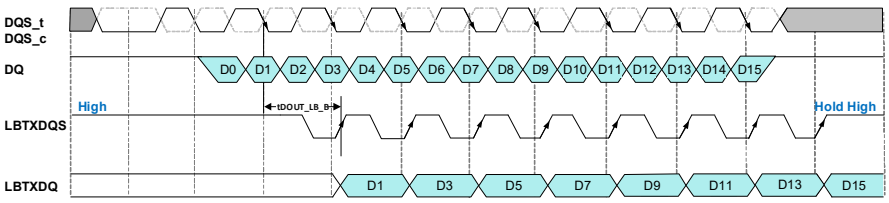


Figure 11 — Phase B: 2tCK or 3tCK Preamble – WE Qualified

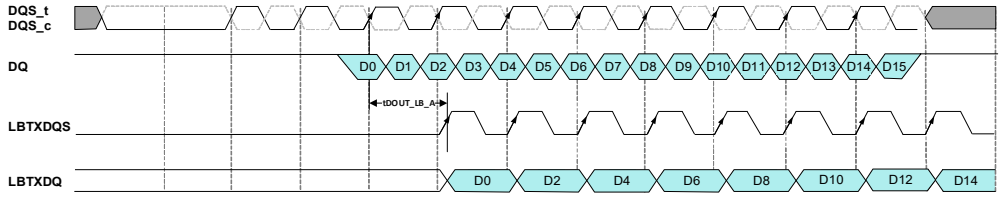


Figure 12 — Phase A: 4tCK Preamble - WE Qualified

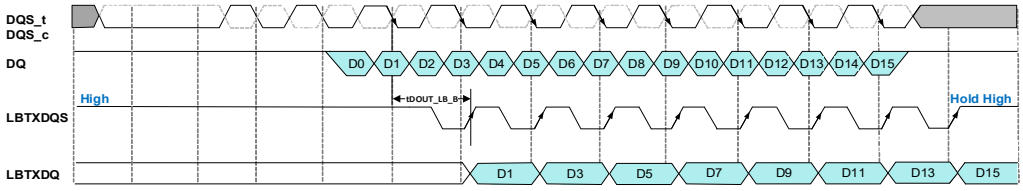


Figure 13 — Phase B: 4tCK Preamble - WE Qualified

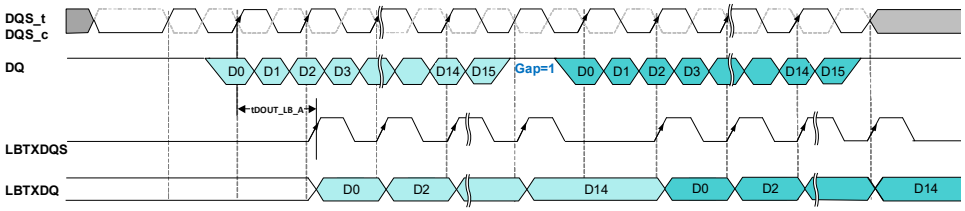


Figure 14 — Phase A: 2tCK or 3tCK Preamble and 1tCK Gap - WE Qualified

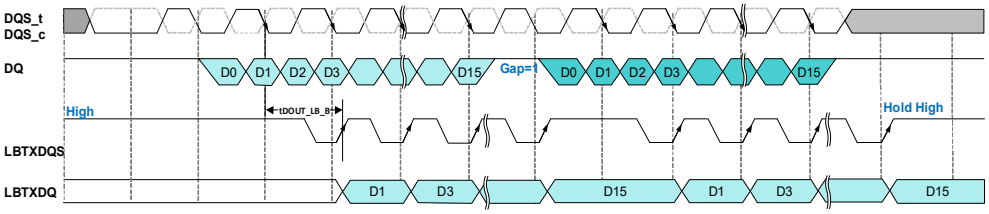


Figure 15 — Phase B: 2tCK or 3tCK Preamble and 1tCK Gap - WE Qualified

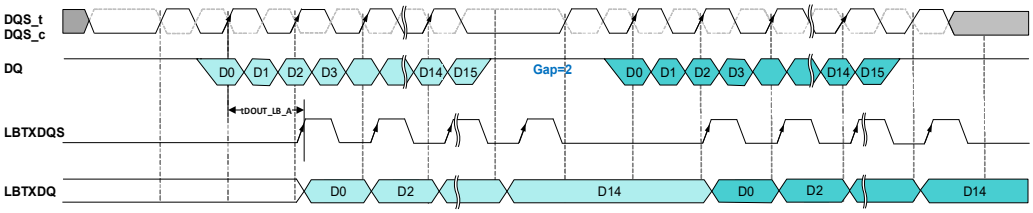


Figure 16 — Phase A: 2tCK or 3tCK Preamble and 2tCK Gap - WE Qualified

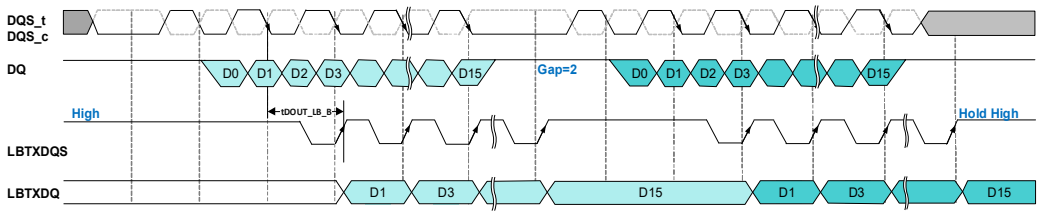


Figure 17 — Phase B: 2tCK or 3tCK Preamble and 2tCK Gap - WE Qualified

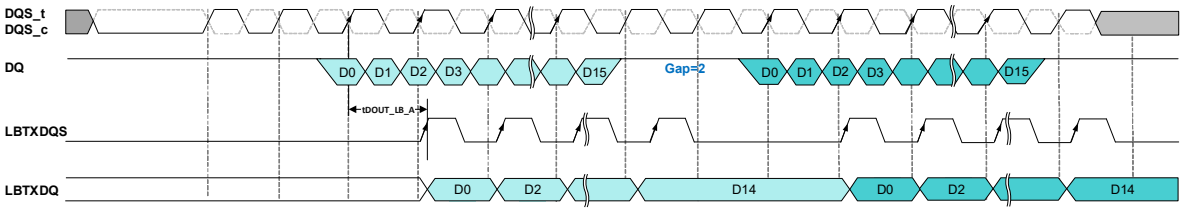


Figure 18 — Phase A: 4tCK Preamble and 2tCK Gap - WE Qualified

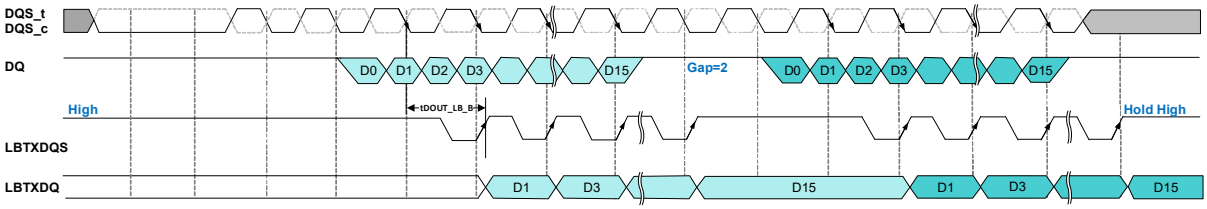


Figure 19 — Phase B: 4tCK Preamble and 2tCK Gap - WE Qualified

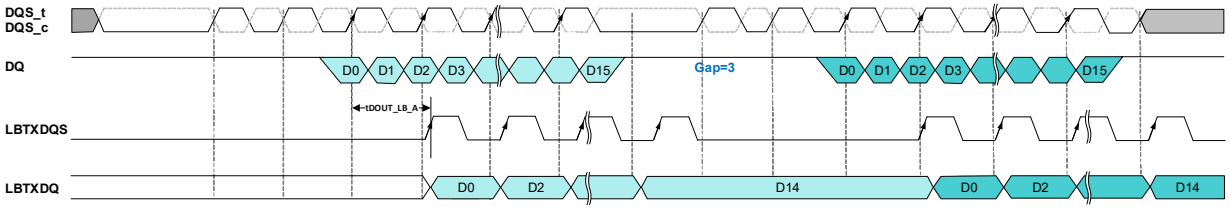


Figure 20 — Phase A: 4tCK Preamble and 3tCK Gap - WE Qualified

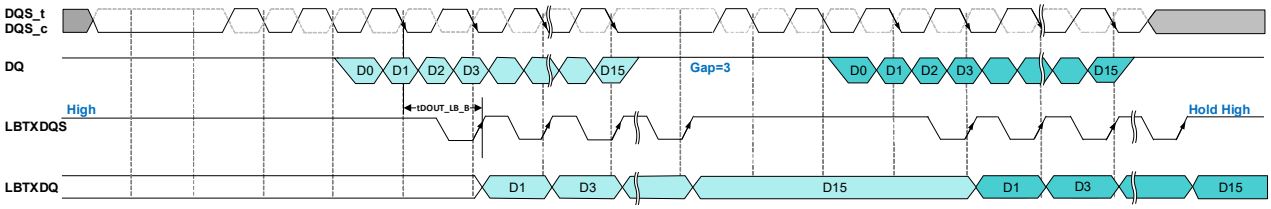


Figure 21 — Phase B: 4tCK Preamble and 3tCK Gap - WE Qualified

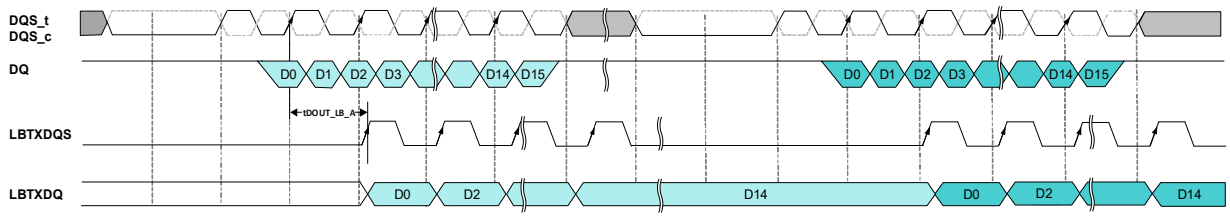


Figure 22 — Phase A: 2tCK or 3tCK Preamble without any Overlap - WE Qualified

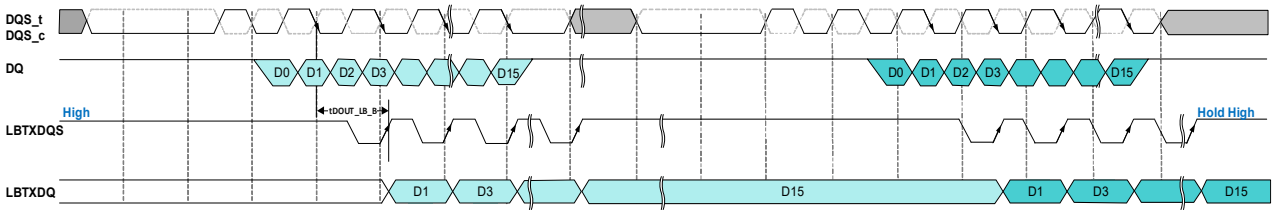


Figure 23 — Phase B: 2tCK or 3tCK Preamble without any Overlap - WE Qualified

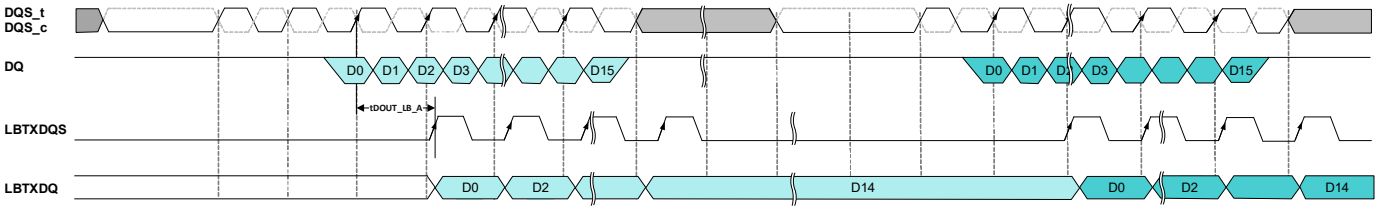


Figure 24 — Phase A: 4tCK Preamble without any Overlap - WE Qualified

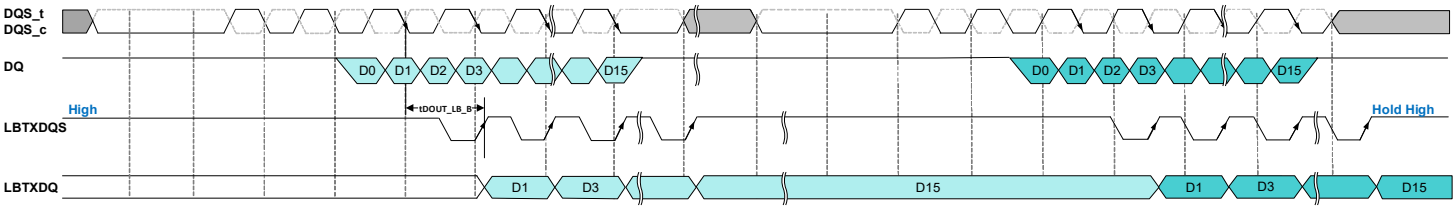


Figure 25 — Phase B: 4tCK Preamble without any Overlap - WE Qualified

3.5.4 Loopback Timing and Levels

The LBTXDQS output will be delayed from the selected DQS_t/DQS_c Loopback Phase. The timing parameter, tDOUT_LB_A/tDOUT_LB_B, is shown in Table 156, “Output timing requirements,” on page 167.

Loopback strobe LBTXDQS to Loopback data LBTXDQ relationship is illustrated in Figure 26.

- tHW_LBTXDQS describes the single-ended LBTXDQS strobe HIGH pulse width
- tLW_LBTXDQS describes the single-ended LBTXDQS strobe LOW pulse width
- tSK_LBTX describes the latest valid transition of LBTXDQ measured at both rising and falling edges of LBTXDQS
- tLBTXDQ_H describes the earliest invalid transition of LBTXDQ measured at both rising and falling edges of LBTXDQS
- tLBTXDQ_VW describes the data valid window per device per UI and is derived from (tLBTXDQ_H-tSK_LBTX) of each UI on a given Data Buffer

Table 156 on page 167 document the values for these timing parameters.

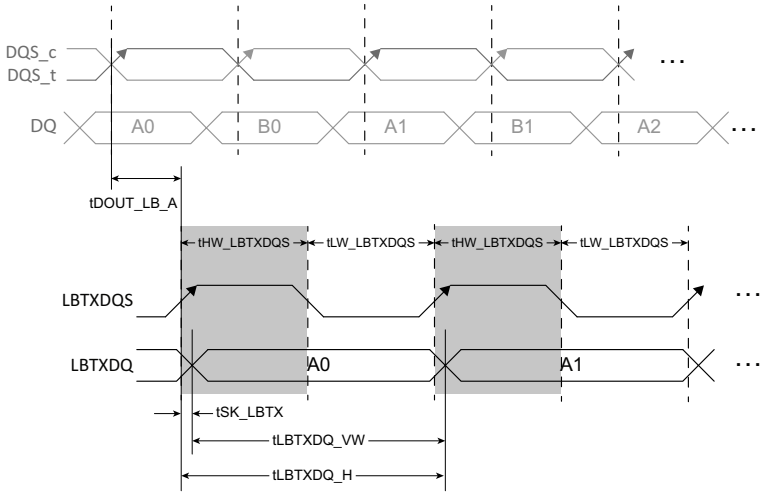


Figure 26 — Loopback Output Timing Parameters

ODT for Loopback is described in Section 14.2, “LBTXDQ/LBTXDQS On Die Termination DC Electrical Characteristics,” on page 181. Output driver electrical characteristics for Loopback is described in Section 15.2, “Output Driver DC Electrical Characteristics for LBTXDQS, LBTXDQ,” on page 198.

3.6 ZQ Calibration

The DDR5DB01 performs I/O circuit calibration when it receives a ZQ calibration in the MPC command. In order to use ZQ calibration command, a 240 Ω +/– 1% resistor must be connected between the ZQCAL pin and V_{SS}.

Proper host interface RTT_NOM, RTT_WR, RTT_PARK DQ/DQS drive strength, DRAM interface RTT and MDQ/MDQS drive strength not guaranteed until a ZQ calibration has been performed. The host sends ZQCal Start and ZQCal Latch calibration commands through the DDR5RCD01 and forwards to DRAM and Data Buffer.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the Data Buffer's calibration procedure, and ZQCal Latch captures the result and loads it into the Data Buffer's drivers. A ZQCal Start command may be issued anytime the DB is in a state in which it can receive valid commands.

There are two timing parameters associated with ZQ Calibration. t_{ZQCAL} is the time from when the ZQCal Start MPC command is sent to when the host can send the ZQCal Latch MPC command. t_{ZQLAT} is the time from when the ZQCal Latch MPC command is sent by the host to when the DQ bus can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after t_{ZQCAL} has expired and all DQ bus operations have completed. The DQ Bus must maintain a Deselect state during t_{ZQLAT} to allow ODT calibration settings to be updated.

After a ZQCal Start and until t_{ZQCAL} finishes, neither another ZQCal Start nor a ZQCAL Latch is allowed.

No other commands that cause data transfers on the host interface DQ/DQS outputs or the DRAM interface MDQ/MDQS outputs are allowed during ZQCal Latch.

The DDR5DB01 may or may not perform any calibration for its own I/O circuits on receipt of ZQCal Start.

3.7 Continuous Burst Mode

A continuous burst mode is configured with MRW to RW90[0] = 1. There are two usage models, one for DRAM interface test and the other for Host interface test.

For MDQ/MDQS test on the DRAM interface, the test sequence is as below:

1. Configure LFSR0 in PG[8]RWE3 and LFSR1 in PG[8]RWE4
2. Set RW90[0] to 1
3. Enable MWD training mode in RW83
4. Send one WR command

Then the DB will start the pattern output on MDQ/MDQS and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or receiving an MRW RW90[0] = 0 command to disable the continuous burst mode. After the WR command in Step 4 only MRW commands are allowed.

For DQ/DQS test on the Host interface, the test sequence is as below:

1. Configure LFSR0 in PG[8]RWE3 and LFSR1 in PG[8]RWE4
2. Set RW90[0] to 1
3. Enable HIR training mode in RW83
4. Send one DB-space Short MRR command

Then the DB will start the pattern output on DQ/DQS and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or receiving an MRW RW90[0] = 0 command to disable the continuous burst mode. After the DB-space MRR command in step 4 only MRW commands are allowed.

Using the continuous burst mode restarts the Data Pattern/LFSR. Additionally, the DB will not store the current seed value when it has exited the continuous burst mode, therefore any subsequent pattern reads will restart the seed to the programmed values of PG[8]RWE3 in PG[8]RWE4.

Once the MRW RW90[0] = 0 is registered by the DB, it will stop all pattern traffic by tCont_Exit. Since there is no min time for tCont_Exit, the DB may stop the pattern prior to tCont_Exit, potentially truncating any current burst pattern. After tCont_Exit_Delay has expired, any other valid command is then legal. All training patterns (modes) are supported in the continuous burst mode.

The DB will not store the current LFSR state when it exits continuous burst mode and it may clear the pattern values stored in PG[8]RW[E4:E3]. The host is required to program the seed/pattern again for subsequent runs.

3.8 Dynamic ODT Control on the Host interface

In certain application cases and to further enhance signal integrity on the Host interface data bus, it is desirable that the termination strength of the DB can be changed without issuing an MRW command. This requirement is supported by the “Dynamic ODT” feature as described as follows.

3.8.1 ODT Functional Description

There are four RTT values are available for DQ: RTT_NOM_RD, RTT_NOM_WR, RTT_PARK and RTT_WR. DQS only has one RTT value which is DQS_RTT_PARK.

- The value for DQ *RTT_NOM_RD* is preselected via RW88[5:3]
- The value for DQ *RTT_NOM_WR* is preselected via RW88[2:0]
- The value for DQ *RTT_WR* is preselected via RW87[5:3]
- The value for DQ *RTT_PARK* is preselected via RW87[2:0]
- The value for DQS *DQS_RTT_PARK* is preselected via RW86[2:0]
- RTT_NOM_RD & RTT_NOM_WR on/off timings are controlled via the respective NT Read and Write command and latencies.
- DQS_RTT_PARK is held static and is based on the value programmed in the RW listed above.

The combination of allowable CAS Latency settings and ODTLon offsets are shown in Table 7. Refer to the DDR5 SDRAM device specification for allowable combinations of ODTLon and ODLoff offset values.

Table 7 — Allowable CL and ODTLon Offset Combinations

		ODTLon_WR_Offset, ODTLon_WR_NT_Offset, ODTLon_RD_NT Offset Setting					
		-4	-3	-2	-1	0	1
CAS Latency (CL)	22	Invalid	Invalid	Valid	Valid	Valid	Valid
	24	Invalid	Valid	Valid	Valid	Valid	Valid
	26	Valid	Valid	Valid	Valid	Valid	Valid
	>26	Valid	Valid	Valid	Valid	Valid	Valid

Table 8 — Latencies and Timing Parameters Relevant for Dynamic ODT when CRC is Disabled

Symbol	Parameter	Conditions	DDR5 speed bins 3200 to 4800	Unit	Note
tODTLon_WR_DB	ODT Latency On from target WRITE command to RTT Enable	**From:** Registering BCOM bus target write command **To:** Change RTT strength from Previous State to RTT_WR	tODTLon_WR_DB = DB_WL(R) - tPDM_WR + ODTLon_WR_offset	ns	1,4
tODTLon_WR_NT_DB	ODT Latency On from NT WRITE command to RTT Enable	**From:** Registering BCOM bus NT write command **To:** Change RTT strength from Previous State to RTT_NOM_WR	tODTLon_WR_NT_DB = DB_WL(R0) - tPDM_WR + ODTLon_WR_NT_offset	ns	1,4
tODTLoff_WR_DB	ODT Latency Off from target WRITE command to RTT Disable	**From:** Registering BCOM bus target write command **To:** Change RTT strength from RTT_WR to RTT_PARK/RTT_NOM_RD/ RTT_NOM_WR/Hi-Z	tODTLoff_WR _DB = DB_WL(R) + BL/2 – tPDM_WR + ODTLoff_WR_offset	ns	1,4
tODTLoff_WR_NT_DB	ODT Latency Off from NT WRITE command to RTT Disable	**From:** Registering BCOM bus NT write command **To:** Change RTT strength from RTT_NOM_WR to RTT_PARK/ RTT_NOM_RD/RTT_WR/Hi-Z	tODTLoff_WR_NT _DB = DB_WL(R0) + BL/2 – tPDM_WR + ODTLoff_WR_NT_offset	ns	1,4
tODTLoff_RD_DB	Data Termination Disable	**From:** Registering BCOM bus target read command **To:** Disables the termination upon driving data	Data Termination Disable = DB_RL(R) + tPDM_RD – 1 tCK	ns	2
tODTLon_RD_DB	Data Termination Enable	**From:** Registering BCOM bus target read command **To**: Re-enables the termination after driving data	Data Termination Enable = DB_RL(R) + BL/2 + tPDM_RD	ns	2
tODTLoff_RD_DQS_DB	Strobe Termination Disable	**From:** Registering BCOM bus target read command **To:** Disables the termination upon driving strobe	Strobe Termination Disable = DB_RL(R) – tRPRE + tPDM_RD – 1 tCK – Read DQS OFFSET	ns	2
tODTLon_RD_DQS_DB	Strobe Termination Enable	**From:** Registering BCOM bus target read command **To:** Re-enables the termination after driving strobe	Strobe Termination Enable = DB_RL(R) + BL/2 + tRPST - 0.5 tCK + tPDM_RD – Read DQS OFFSET	ns	2
tODTLon_RD_NT_DB	ODT Latency On from NT READ command to RTT Enable	**From:** Registering BCOM bus NT read command **To:** Change RTT strength from Previous State to RTT_NOM_RD	tODTLon_RD_NT_DB = DB_RL(R0) + tPDM_RD + ODTLon_RD_NT_offset	ns	1,4
tODTLoff_RD_NT_DB	ODT Latency Off from NT READ command to RTT Disable	**From:** Registering BCOM bus NT read command **To:** Change RTT strength from RTT_NOM_RD to RTT_PARK/ RTT_NOM_WR/RTT_WR/Hi-Z	tODTLoff_RD_NT_DB = DB_RL(R0) + BL/2 + tPDM_RD + ODTLoff_RD_NT_offset	ns	1,4
tADC	RTT change skew	**From:** Transitioning from one RTT State to the next RTT State **To**: RTT valid	tADC(min) = 0.2 tADC(max) = 0.8	tCK (avg)	3

Note(s):

1. All "_offset" parameters refer to the ODT Configuration Control Words in address space Page [B].
2. For simplicity, Reads are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset control word to control it. To indicate this, it was named Data (or Strobe) Termination Disable and Enable.
3. When transitioning from a value of RTT equal to RA, to a value of RTT equal to RB, the RTT termination resistance during the transition must be constrained from the minimum of (RA, RB) to the maximum of (RA, RB).
4. ODT ON to Off pulse duration must be longer than the Data Burst Length (BL/2).

3.8.2 ODT tADC Clarifications

tADC is defined as the time it takes for the Data Buffer to transition from one RTT state to the next RTT state. In case of the read, it is the time from the RTT state to the Data Buffer Drive state. Unless the RTT is specifically disabled, no High-Z state shall be allowed during tADC. During Data Buffer Drive state, the Data Buffer RON shall keep the DQ signal HIGH prior to the first DQ transition. The DFE should assume that 4UI prior to D0 the signal is HIGH.

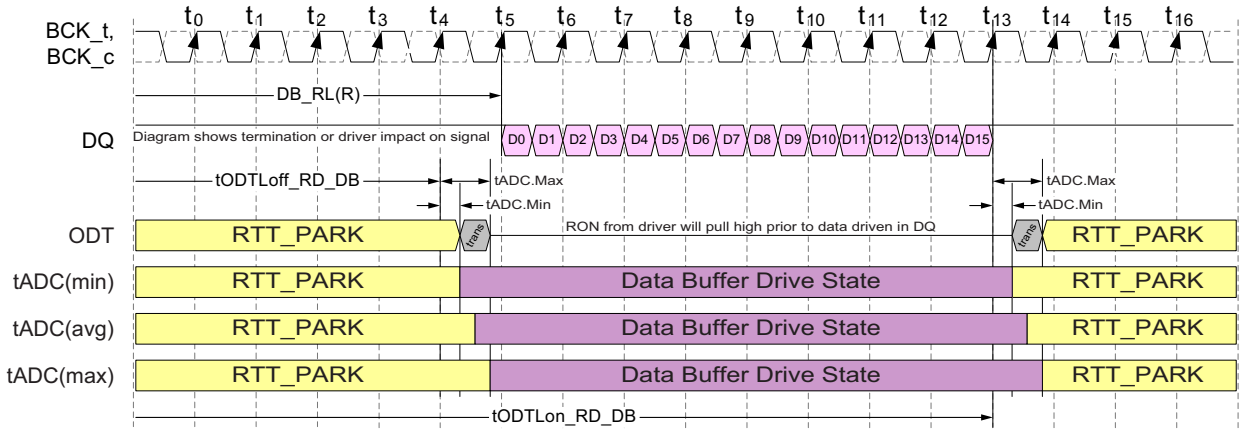


Figure 27 — Example of tADC

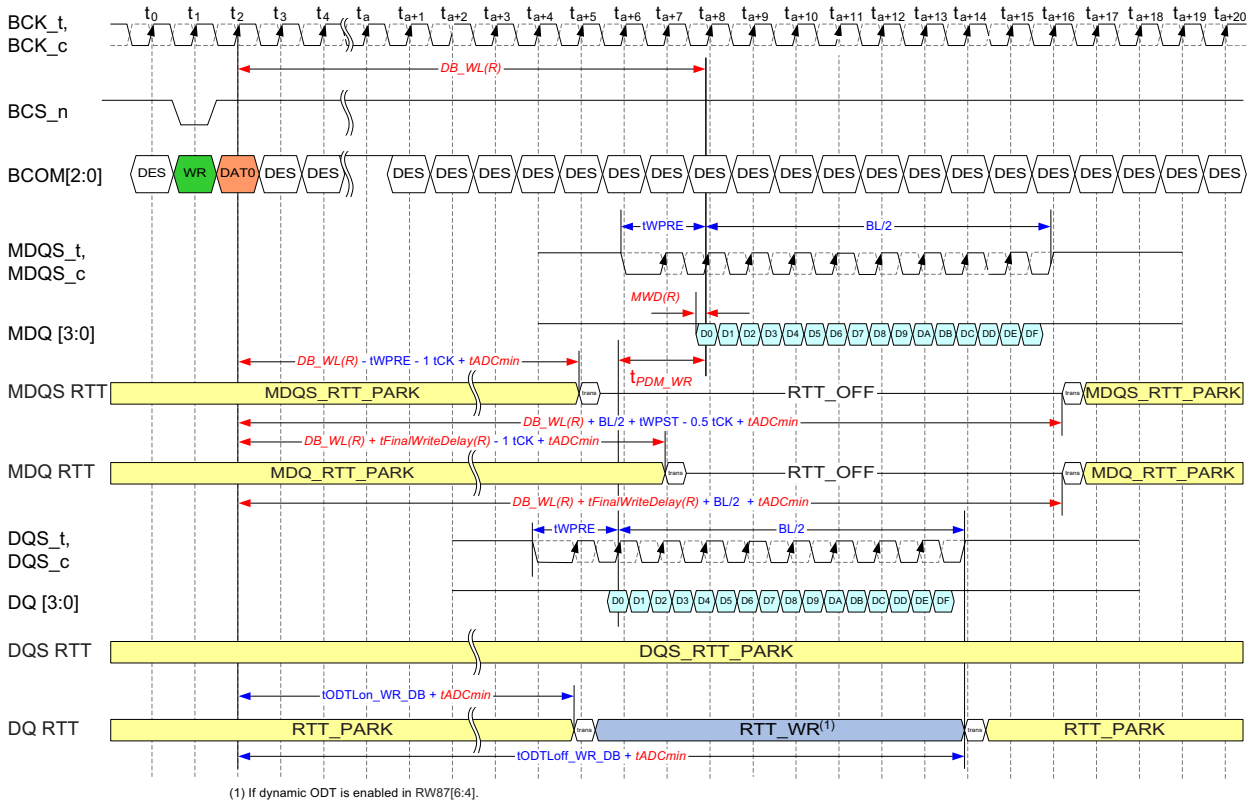
3.8.3 ODT Timing Diagrams

The following pages provide examples of ODT utilization timing diagrams. Examples of Write-to-Write, Read-to-Write, and Read-to-Read are provided for clarification only. Implementations may vary, including termination on other DIMMS.

It is the controller's responsibility to manage command spacing and the programmable aspect of tODLon/off times to ensure that preambles and postambles are included in the RTT ON time.

When there is a 1-t_{CK} ODT control gap for any ODT operation, the said gap's RTT value will be the same or smaller (stronger termination) than RTT_PARK.

All timings noted in the figures below are just used as reference.



Note: tFinalWriteDelay(R) = tMdqWriteBaselineDelay(R) + tDram_DqsDelay_Change(R)[1]

Figure 28 — Example of Burst Write Operation ODT Latencies

1. Devices are also allowed to apply the per-bit MDQ Write delay settings (PG[1:0]RW[F1:EE]) in the MDQ_RTT_PARK timings.

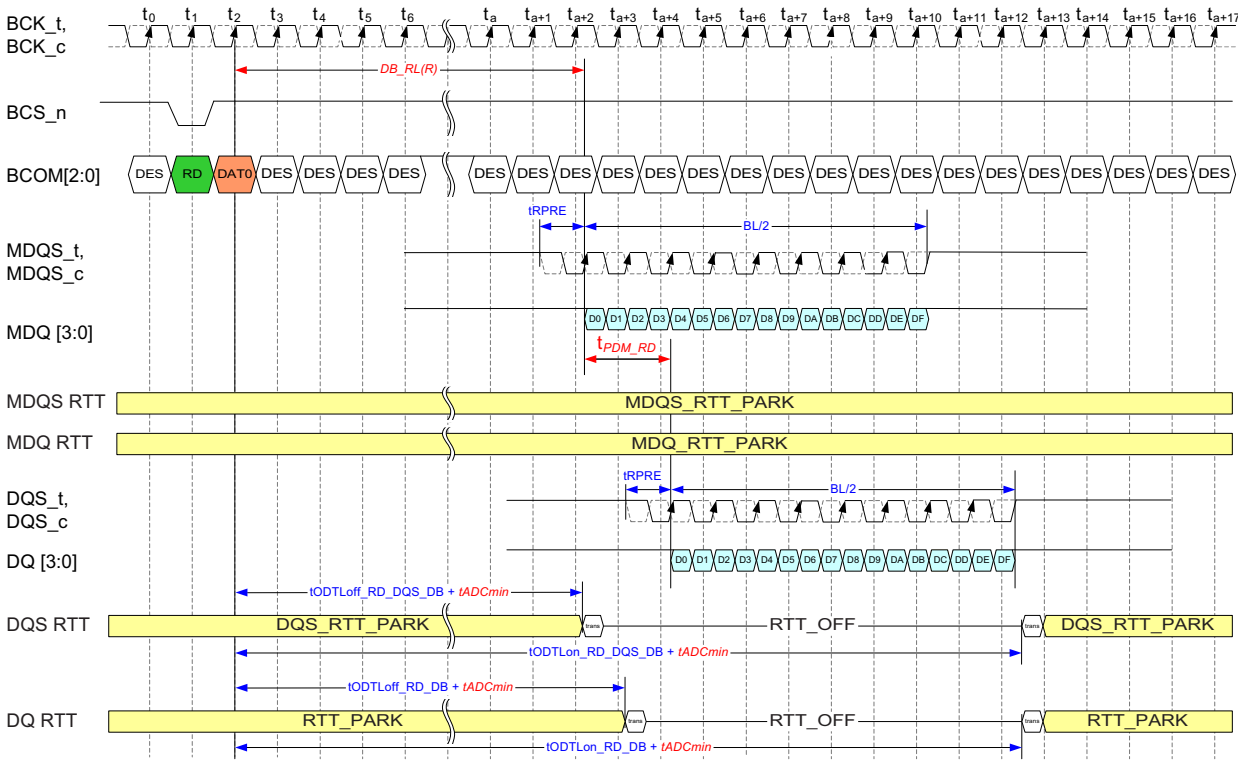


Figure 29 — Example of Burst Read Operation ODT Latencies

3.9 DRAM Periodic Update Support

To track the DRAM tDQS2DQ drift per rank, a tracking mechanism is required to periodically monitor this drift and update the respective MDQ-MDQS write delay settings in the DB as required to compensate for the drift.

For the host to support this for LRDIMM, significant amounts of additional logic and MRW traffic overhead would be needed relative to the RDIMM case. An alternative is to have the Data Buffer assist the host in managing each DRAM's tMDQS2MDQ drift by providing most of the tracking functionality.

3.9.1 DRAM tDQS2DQ Tracking Modes

- DRAM tDQS2DQ tracking initialization mode
- DRAM tDQS2DQ tracking mode.

Prior to performing DRAM tDQS2DQ tracking, the DB requires the Host to issue an MPC to start a DQS interval oscillator measurement for each DRAM rank. The DB supports two ranks of DRAM tDQS2DQ tracking per nibble.

- The *DRAM tDQS2DQ tracking initialization mode* is used to calculate the initial DQS clock tree delay value for each DRAM nibble and rank in PG[A]RW[EF:E0]. The DB stores these values for later use during the DRAM tDQS2DQ tracking mode. DRAM tDQS2DQ tracking initialization on the DB only needs to be done by the host once after MDQ-MDQS Write Delay Training completes, since any delay adjustment due to drift is with respect to the trained values.

- The *DRAM tDQS2DQ tracking mode* is used to calculate the current DQS clock tree delay value for each DRAM nibble and rank stored in PG[A]RW[FF:F0]. These are used to calculate the timing drift relative to their respective initial delay values, and then to update their respective MDQ-MDQS write delay values for drift compensation. DRAM tDQS2DQ tracking is performed periodically by the host as a function of system conditions. All operations, commands, and features are supported when tracking mode is enabled in RWB0[0] excepting during calculation window tTrkCalcCur.

3.9.2 Operational Requirements

The following describes the operational requirements associated with the DRAM tDQS2DQ tracking feature:

- The DB initially enters the DRAM tDQS2DQ tracking initialization mode as a result of power-on initialization. When a DRAM-space MRR read to MR47 is received, the DB will trigger a calculation update for the tracking initialization mode. It is the host's responsibility to issue the MPC command to start the DRAM DQS oscillator and to issue a DRAM-space MRR read to MR46 prior to issuing a DRAM-space MRR read to MR47.
- The DB supports DB-space MRW operations to any register address while in either tracking mode except during a DQS clock tree delay calculation period. The host must make sure that these MRW operations do not interfere with any tracking-related settings or processes.
- The DB supports snooping of the DRAM-space MRW to the DRAM’s DQS interval oscillator control register to obtain the DRAM's run-time count value needed for DQS clock tree calculations. The host must configure the DRAM to perform automatic stop based on its run-time count. The snooped value is loaded into the DB’s DQS Interval Timer Run Time MR45 register PG[8]RWE7.
- The read data format of the DRAM-space MRR is assumed to be the same as defined for the DB-space MRR.
- The DB supports DB-space MRR operations to any register address while in either tracking mode except during a DQS clock tree delay calculation period.
  - The initial and current DRAM DQS OSC Counter values captured by the DB from each DRAM nibble and rank are readable by the host via DB-space MRR.
  - The initial and current DRAM DQS clock tree delay values calculated by the DB for each DRAM nibble and rank are readable by the host via DB-space MRR.
- The host must read DRAM OSC Counter LSB MR46 and MSB MR47 registers sequentially as an {LSB, MSB} pair from the same rank. Upon issuing a DRAM-space read to MR47, the host must block all transactions to all ranks for the duration of tTrkCalcInit if in tracking initialization mode, or for the duration of tTrk CalcCur if in tracking mode, to allow the DB to complete the calculation and update of the DRAM MDQ-MDQS write delay adjustment.
- Host-side read timing for rank-x is defined in the standard way as DB_RL(Rx) + tPDM_RD after the DAT0 cycle of the DRAM-space MRR command sequence. Data is returned using DB-space MRR read format.

3.9.3 DRAM tDQS2DQ Tracking Initialization Mode

To initialize the reference values for subsequent DRAM tDQS2DQ tracking in the DB, the host performs DRAM tDQS2DQ tracking initialization only once per rank after MDQS Write Delay Training completes. After power cycle reset the DB defaults to DRAM tDQS2DQ tracking initialization mode, or the mode can be set via a DB-space MRW to set RWB0[0] = 0. To perform the initialization the host must first issue an MPC to start an initial DQS interval oscillator measurement for each DRAM rank (not shown).

The host will issue two sequential DRAM-space MRR commands to MR46 and MR47 to read the initial values of a DRAM DQS OSC Counter LSB and MSB register pair from the same rank.

When the host issues the first DRAM-space MRR to the DRAM DQS OSC Counter LSB register MR46, the DB captures the read data from each DRAM nibble using the read timing for the specified rank and stores the captured value for the lower nibble in PG[A]RWE0 for rank-0 or PG[A]RWE2 for rank-1, and it stores the captured value for the upper nibble in PG[A]RWE4 for rank-0 or PG[A]RWE6 for rank-1. The DB will return a predefined value in

RWB1 to the Host.

When the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register MR47, the DB captures the read data from each DRAM nibble using the read timing for the specified rank and stores the captured value for the lower nibble in PG[A]RWE1 for rank-0 or PG[A]RWE3 for rank-1, and it stores the captured value for the upper nibble in PG[A]RWE5 for rank-0 or PG[A]RWE7 for rank-1.The DB will return a predefined value in RWB1 to the Host.

As shown in Figure 30, the host must meet the t_{MRROD1} timing parameter between MRR operations to DRAM-space MR46 and MR47. In general, MRR operations to DRAM-space MR46 and MR47 must also be considered as DB space MRR operations from the timing point of view since the DB returns the contents of RWB1 to the Host.

Once the DQS OSC Counter LSB and MSB values from each DRAM nibble for a particular rank are captured and stored, the DB will then calculate the initial DQS clock tree delay for each nibble of the specified rank. The calculation starts when the capture has completed for the DRAM nibble with the latest read timing.

Once the calculation has completed, the DB then stores the calculated value for the lower nibble in PG[A]RWE8 and PG[A]RWE9 for rank-0 or PG[A]RWEA and PG[A]RWEB for rank-1, and it stores the calculated value for the upper nibble in PG[A]RWEC and PG[A]RWED for rank-0 or PG[A]RWEE and PG[A]RWEF for rank-1. The calculate and store operations complete within tTrkCalcInit.

From the time when the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register MR47 to the end of the tTrkCalcInit period, only DES and NOP commands are legal. Once the period has completed for the specified rank, the DB will remain in the tracking initialization mode as shown in Figure 30. The host can then execute DRAM tDQS2DQ tracking initialization functions at a later time to perform the tDQS2DQ tracking initialization process to the other rank.

At the end of DRAM tDQS2DQ Tracking Initialization, both Initial DRAM DQS Clock Tree Delay and Current DRAM DQS Clock Tree Delay share the same value. This results in tDRAM_DqsDelay_Change being equal to 0 which means no change to the MDQ-to-MDQS Write Delay.

As depicted in Figure 32, the tDQS2DQ Tracking Initialization Mode calculations described in the above paragraphs can also be triggered by direct MRW operations to the MSB counter values in PG[A]RW[E1, E3, E5, E7]. In the case of direct MRW access, the tracking mode selection bit RWB0[0] is ignored and the host is required to meet applicable timing parameters in Table 155.

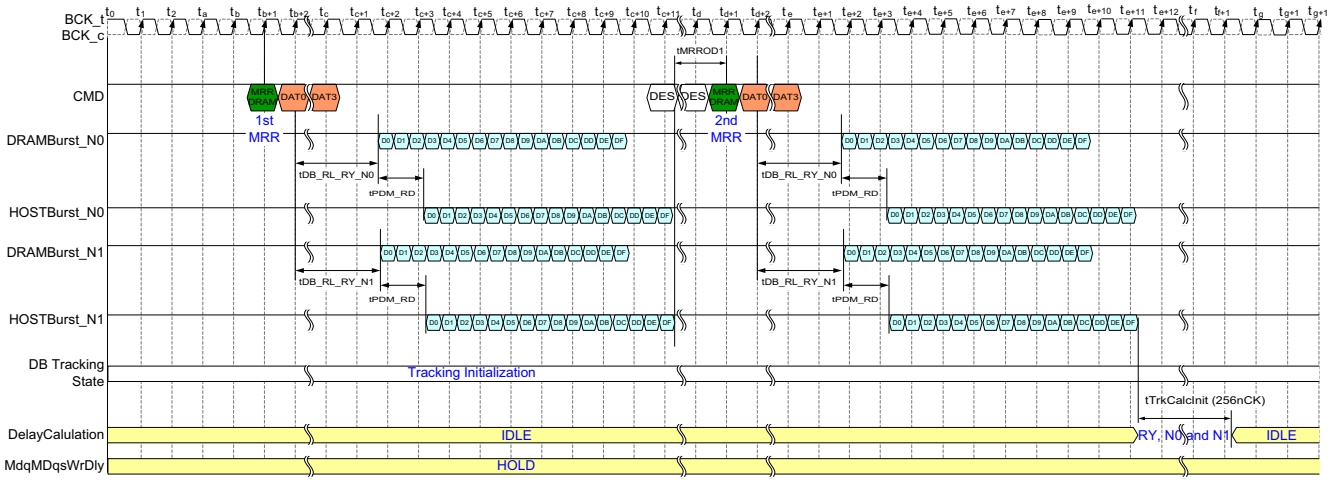


Figure 30 — DRAM tDQ2DQ Tracking Initialization Mode Flow

3.9.4 DRAM tDQS2DQ Tracking Mode

DRAM tDQS2DQ tracking is performed periodically by the host as a function of system conditions. After the DRAM tDQS2DQ tracking initialization has completed, the host must set the DB in DRAM tDQS2DQ tracking mode via a DB-space MRW to set RWB[0] = 1. To perform the tracking the host shall issue an MPC to start a DQS interval oscillator measurement for each DRAM rank (not shown). After starting the DRAM DQS interval oscillator the host will issue two sequential DRAM-space MRR commands to MR46 and MR47 to read the current values of a DRAM DQS OSC Counter LSB and MSB register pair from the same rank. The read process is the same as described in the Initialization mode except that different DB registers are used for value storage.

When the host issues the first DRAM-space MRR to the DRAM DQS OSC Counter LSB register MR46, the DB stores the captured value for the lower nibble in PG[A]RWF0 for rank-0 or PG[A]RWF2 for rank-1, and it stores the captured value for the upper nibble in PG[A]RWF4 for rank-0 or PG[A]RWF6 for rank-1. The DB will return a predefined value in RWB1.

As shown in Figure 31 the host must meet the t_{MRROD1} timing parameter between MRR operations to DRAM-space MR46 and MR47. In general, MRR operations to DRAM-space MR46 and MR47 must also be considered as DB-space MRR operations from the timing point of view since the DB returns the contents of RWB1 to the Host.

When the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register MR47, the DB stores the captured value for the lower nibble in PG[A]RWF1 for rank-0 or PG[A]RWF3 for rank-1, and it stores the captured value for the upper nibble in PG[A]RWF5 for rank-0 or PG[A]RWF7 for rank-1.The DB will return a predefined value in RWB1.

Once the DQS OSC Counter LSB and MSB values from each DRAM nibble for a particular rank are captured and stored, the DB will then calculate the current DQS clock tree delay for each nibble of the specified rank. The calculation starts when the capture has completed for the DRAM nibble with the latest read timing.

Once the calculation has completed, the DB then stores the calculated value for the lower nibble in PG[A]RWF8 and PG[A]RWF9 for rank-0 or PG[A]RWFA and PG[A]RWFB for rank-1, and it stores the calculated value for the upper nibble in PG[A]RWFC and PG[A]RWFD for rank-0 or PG[A]RWFE and PG[A]RWFF for rank-1. The DB will update the applied MDQ-MDQS write delay value for each nibble of the rank based on its MDQ write baseline delay and its stored initial and current DQS clock tree delay values. The calculate, store and update operations must complete within tTrkCalcCur. From the time when the host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register MR47 to the end of the tTrkCalcCur period, only DES and NOP commands are legal.

Once the tTrkCalcCur period has completed for the specified rank, the DB will remain in tracking mode as shown in Figure 31.

As shown in Figure 33, the tDQS2DQ Tracking Mode calculations described in the above paragraphs can also be triggered by direct MRW operations to the MSB counter values in PG[A]RW[F1, F3, F5, F7]. In the case of direct MRW access, the tracking mode selection bit RWB0[0] is ignored and the host is required to meet applicable timing parameters in Table 155.

3.9.5 MDQ-MDQS Adjustment Calculations

The DB is only required to support calculation for one rank at a given time, in each x4 nibble. The MDQ-MDQS write delay adjustment calculation for each nibble, Ny, of a specified rank, Rx, is as follows.

The initial count from the DRAM tDQS2DQ tracking initialization step provides the initial DRAM DQS clock tree delay in units of tCK/128:

tDram_DqsDelay_Initial(Rx, Ny) = Dram_RunTimeCount * tCK / (2 * Dram_DQSOscCount_Initial(Rx, Ny)).

For each DRAM tDQS2DQ tracking step, the current count provides the drifted DRAM DQS clock tree delay in units of tCK/128:

tDram_DqsDelay_Current(Rx, Ny) = Dram_RunTimeCount * tCK / (2 * Dram_DQSOscCount_Current(Rx, Ny))

The change in the DRAM DQS clock tree delay is calculated in units of tCK/64:

tDram_DqsDelay_Change(Rx, Ny) = tDram_DqsDelay_Current(Rx, Ny) - tDram_DqsDelay_Initial(Rx, Ny).

The DB then updates the applied MDQ-MDQS write delay values as:

tMdqMdqsWriteDelay(Rx, Ny) = tMdqWriteBaselineDelay(Rx, Ny) + tDram_DqsDelay_Change(Rx, Ny)

Each MDQ write baseline delay register is not updated from its trained value. Instead, its value is offset by its respective tDram_DqsDelay_Change value before being applied to the delay circuitry.

As an example, if the current DQS clock tree delay is larger than the initial DQS clock tree delay, the DQS clock tree delay has increased by tDram_DqsDelay_Change, so the applied MDQ-MDQS write delay needs to be increased by this amount.

For the Final Write Delay including all offset contributors such as tDRAM_DQSDelay_Change from Page PG[A] and PG[1:0]RW[EE:F1] (per-bit Write Delays), the DDR5DB01 device is only required to support the -0.5 * tCK(minimum) to + 3.5 * tCK(maximum) delay range defined for the Write Delay baseline control words in PG[1:0]RW[E6:E7].

In cases where control words in PG[1:0]RW[E6:E7], PG[1:0]RW[EE:F1], and Page PG[A] are programmed with settings that would cause any Final Write Delay value to be outside the delay range supported by the device, the DB will saturate the effective Final Write Delay values at the maximum or minimum (as applicable) of the delay range it supports.

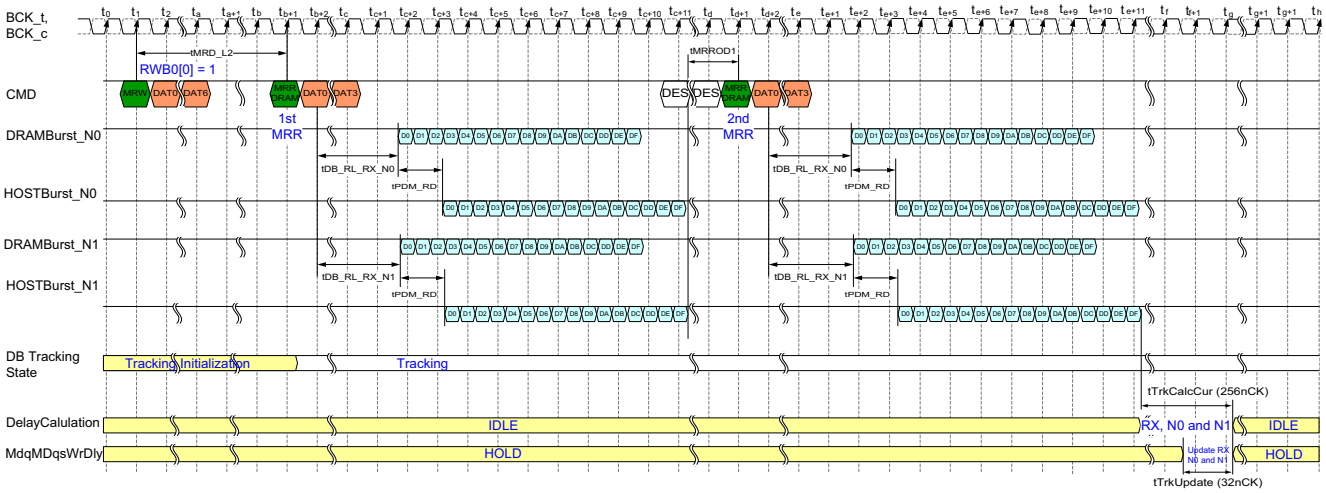
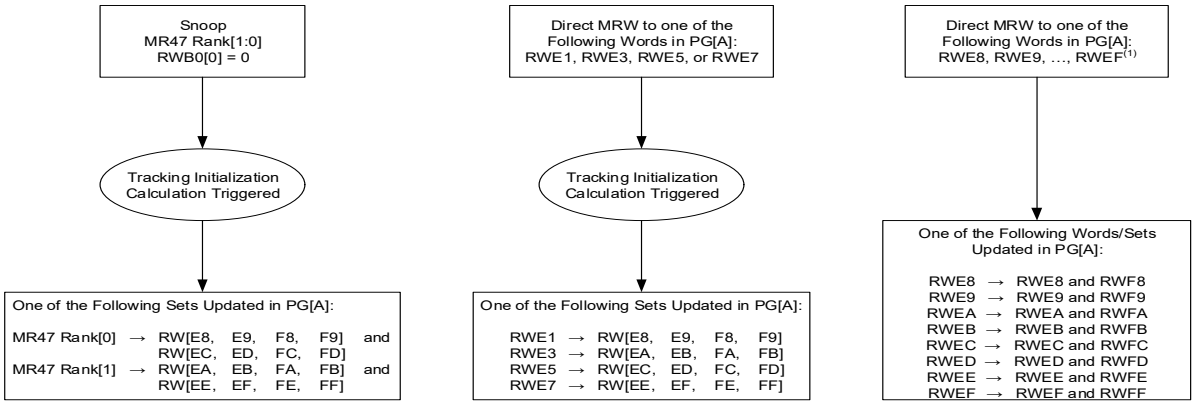


Figure 31 — DRAM tDQS2DQ Tracking Mode Flow

3.9.6 DRAM interval Oscillator Snoop Value

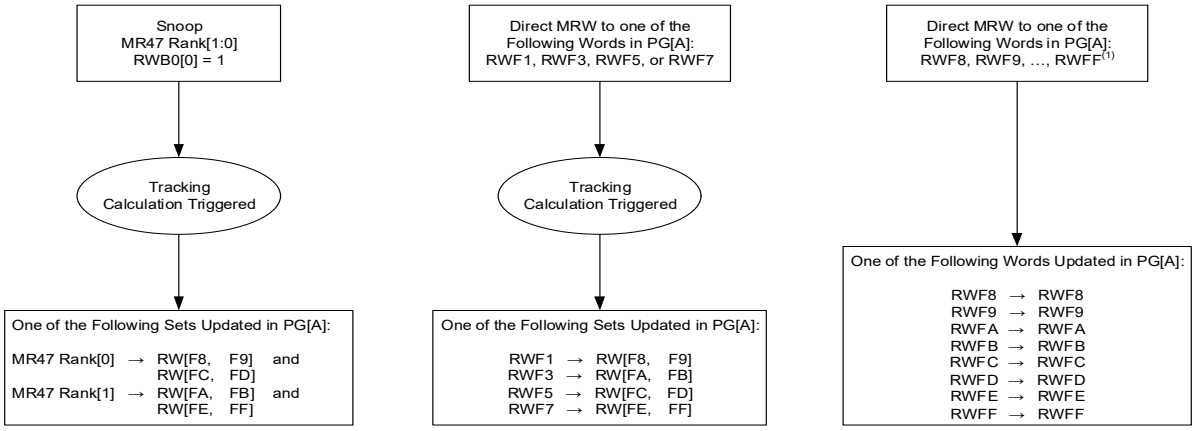
The DB configures PG[8]RWE7 with the snooped value from a DRAM-space MRW to the DRAM's interval oscillator control register MR45. The DB uses the snooped interval timer stop value, referred to as the run-time count value, for DRAM DQS clock tree delay calculations. The host must make sure that the DRAM's run-time count value is configured as necessary. It must also make sure that the DRAM's interval oscillator is configured for automatic stop based on its run-time count value.

Although PG[8]RWE7 can be written directly by the host, the intent is that it will not be written directly by the host after it has been configured with the snooped value. Writing to this register directly is intended for debug purposes.



Note 1: Direct MRW operations to initial DRAM DQS clock tree delay LSB/MSB registers must be performed sequentially as pairs, LSB followed by MSB, with only DES commands in between.

Figure 32 — tDQS2DQ Tracking Initialization Sequences



Note 1: Direct MRW operations to current DRAM DQS clock tree delay LSB/MSB registers must be performed sequentially as pairs, LSB followed by MSB, with only DES commands in between.

Figure 33 — tDQS2DQ Tracking Sequences

4 Power Down operation

DDR5 does not have a separate CKE signal going to the DIMM or the DBs. Power Down Entry, including self refresh, is signaled via a command sequence on the BCOM interface. A BCS_n active pulse will take the Data Buffer out of the power down state. A NOP command is placed on the BCOM bus along with BCS_n pulse so that no commands are executed by the DB devices. The DDR5DB01 can be put in power down mode with or without non-target ODT control.

4.1 Power Savings Modes

The DDR5DB01 device supports the following power saving mechanisms:

- PDE Power Down Mode.
- PDE Power Down with ODT control. In this mode ranks can be in power down mode but will still require ODT commands for termination, therefore the RCD and Data buffer will remain in normal operating mode.
- Self Refresh Modes. With and without Clock Stop.

4.1.1 PDE Power Down Mode

The DB device enters power down mode when it receives a PDE command sequence on the BCOM interface. Due to the external V_{DD} termination, all BCOM[2:0] and BCS_n inputs of the Data Buffer remain HIGH during PDE power down mode just as in Deselect operation. The DB may reduce power internally as it is able.

The PDE command is sent to the Data Buffers on the BCOM bus only when the last rank has entered PDE mode. The PDX command is sent to the Data Buffers on the BCOM bus when the first rank receives the PDX command. Therefore, the Data Buffers are in power down mode only when ALL ranks on the sub channel are in power down mode. Also, because of this, a two-cycle PDE command on the BCOM[2:0] bus can be followed immediately by a PDX command.

4.1.2 PDE Power Down Mode with ODT Control Enabled

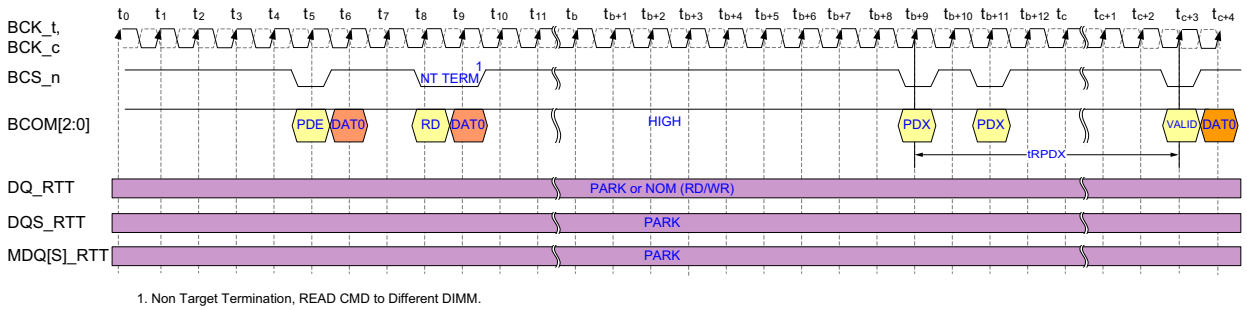
Power Down with ODT Control Enabled when the DB receives a PDE Command DAT0 BCOM[1:0] = ‘10’. In PDE Power Down Mode with ODT control, the Data Buffers may still receive non-target termination commands.

While in PDE with ODT control, RD, WR, and MRR commands may be sent to the Data Buffer. It is the responsibility of the host controller to not send commands which are “Not Allowed”, as defined in Table 9. The non-target termination commands must be sent to the Data Buffers when they are in PDE with ODT control.

Table 9 — ODT Control during Power Down Mode[1]

Mode	NOP/PDX command	RD w/ non-target term	WR w/ non-target term	MRR w/ non-target term	All Others
PDE w/o ODT control	Allowed. Exits PDE mode	Not Allowed	Not Allowed	Not Allowed	Not Allowed
PDE w/ODT control	Allowed. Exits PDE Mode	Allowed	Allowed	Allowed	Not Allowed

1. This table applies to the commands sent from the RCD to the Data Buffer when the Data Buffer is in PDE state with ODT Control.



1. Non Target Termination, READ CMD to Different DIMM.

Figure 34 — Power Down with ODT Control Enabled Mode Entry and Exit

4.1.3 PDE Power Down Mode without ODT Control Disabled

Power Down with ODT Control Enabled when the DB receives a PDE Command DAT0 BCOM[1:0] = '11'. In PDE Power Down Mode without ODT control, the Data Buffers does not process any commands excepting for Power Down Exit.

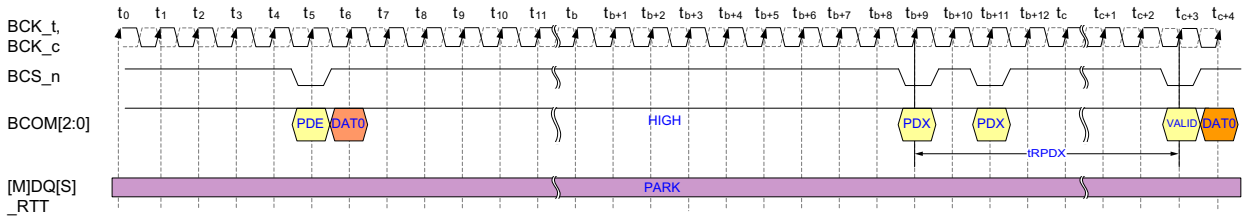


Figure 35 — Power Down with ODT Control Disabled Mode Entry and Exit

4.2 Self Refresh Modes

After the SRE command is received by the Data Buffer (i.e., PDE Command DAT0 BCOM[1] = 0), the DB input clock may stop as BCK_t = BCK_c = HIGH. When the BCK clock is running, the BCS_n signal must remain HIGH in order for the DB to stay in Self Refresh state. A BCS_n active (LOW) pulse instructs the Data Buffer to get out from SRE state.

4.2.1 Self Refresh Mode with Clock Stop Entry

Self Refresh Mode is a very low power state in which the input clocks can stop and the DB on-die terminations, including RTT_PARK, are disabled. Self-refresh entry is signaled when the RCD sends SRE command on the BCOM[2:0] control bus (i.e., PDE Command DAT0 BCOM[1] = 0). See Figure 36, "Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by PDE Command with SRE Indication," on page 30 through Figure 39, "Self Refresh Entry Exit with Clock Stop but without Frequency Change – Termination Disabled by Clock Stop Detection Circuit," on page 31.

The DDR5DB01 uses a clock-stop detection circuit to disable the command bus BCK_t/BCK_c, BCOM[2:0], and BCS_n receivers. When the clock stops, BCK_t and BCK_c will be driven or pulled up HIGH, respectively, by the Host or by the discrete termination resistors on the module. Similarly, BCS_n, and BCOM[2:0] signals will be pulled HIGH by the Host or the termination resistors. Note that the BCS_n is NOT driven LOW when in self refresh.

The DDR5DB01 will disable DQ/DQS and MDQ/MDQS on-die terminations during Self Refresh with Clock Stop. The DB may disable on die terminations using the PDE command with SRE indication as shown in Figure 36 on page 30 and Figure 38 on page 31. The DB may also rely on the clock-stop detection circuit for this purpose as shown in Figure 37 and Figure 39 on page 31. Either method is acceptable.

4.2.2 Exit from Self Refresh Mode with Clock Stop

To exit the Clock Stop condition, the Host starts the BCK clocks with stable frequency and phase while keeping BCOM[2:0] and BCS_n signals HIGH.

On die terminations in the DB can get re-enabled either by the first NOP command following exit from Clock-Stop condition as depicted in Figure 36 and Figure 38 or by the exit from Clock-Stop condition directly as shown in Figure 37 and Figure 39.

If the BCOM[2:0] and BCS_n bus timings have not been trained for the current frequency of operation, after a wait of t_{STAB_DB} from when the BCK clocks are toggling with stable phase and frequency, the host is allowed to apply the "BCOMTM Entry" strap command (see Table 27 on page 52) to train the BCOM[2:0] and BCS_n signal timings.

The BCS_n signal is allowed to pulse LOW for one cycle (with valid timings) after a wait of t_{STAB_DB} from when the BCK clocks are toggling with stable phase and frequency. This BCS_n LOW pulse instructs the DDR5DB01 to exit from Self Refresh mode.

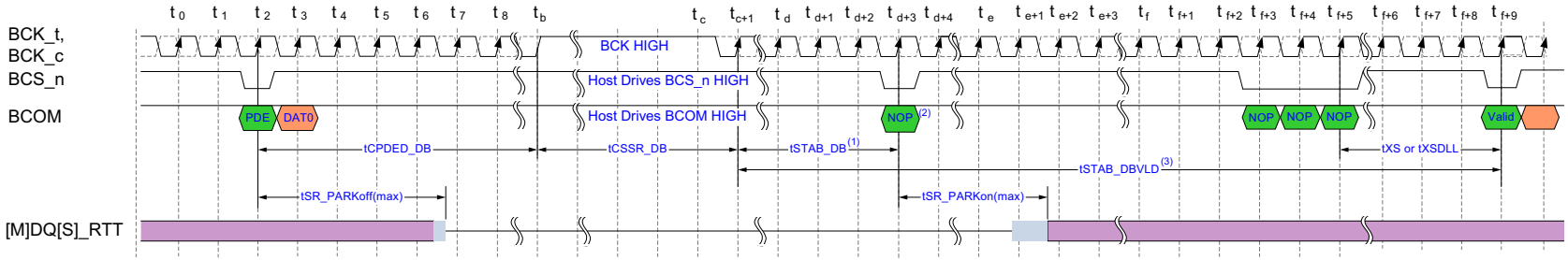
4.2.3 Self Refresh Mode without Clock Stop Entry

As seen in Figure 40 on page 32, Self Refresh without Clock Stop is similar to Self Refresh with Clock Stop mode except that the Host will not stop the BCK clock in this mode.

The DDR5DB01 device may disable on die terminations during Self Refresh without Clock Stop using the PDE command with SRE indication as a trigger as shown in Figure 40 on page 32. The DB is also allowed to keep on-die terminations (RTT_PARK) enabled as shown in Figure 41. Either method is acceptable.

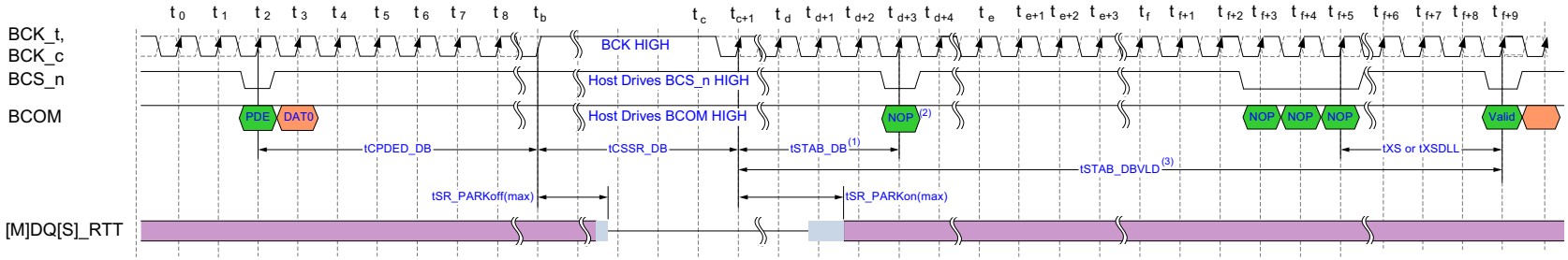
4.2.4 Self Refresh Mode without Clock Stop Exit

Exiting this mode is similar to Self Refresh with Clock Stop, except that the host will not wait t_{STAB_DB} upon exit, as the clock circuitry in the Data Buffer stays locked.



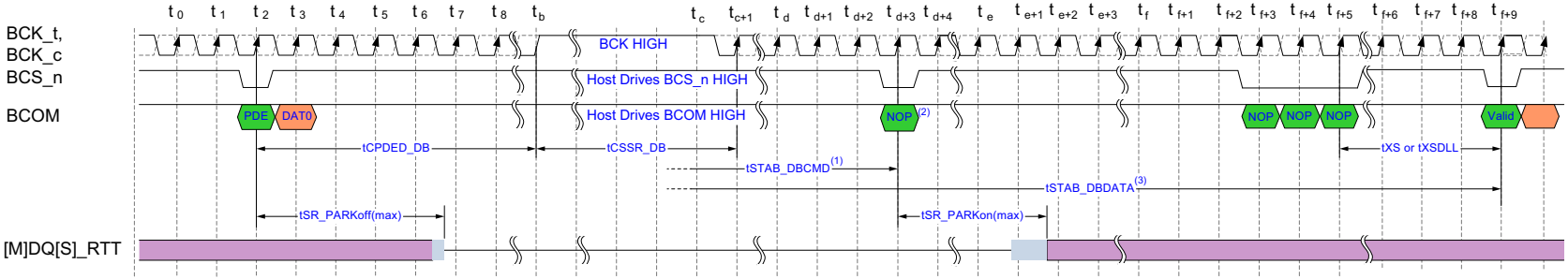
1. In LRDIMM, tSTAB01 + tSTAB_DB must be met from start of RCD DCK to the first DCA command that gets forwarded to the LRDIMM BCOM bus interface but does not use the DQ data path (e.g., SRX, NOP).
2. Instead of NOP, the host may issue “BCOMTM Entry” strap command after meeting tSTAB_DB.
3. In LRDIMM, tSTAB01 + tSTAB_DBVLD must be met from start of RCD DCK to the first DCA command that gets forwarded to the LRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

Figure 36 — Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by PDE Command with SRE Indication



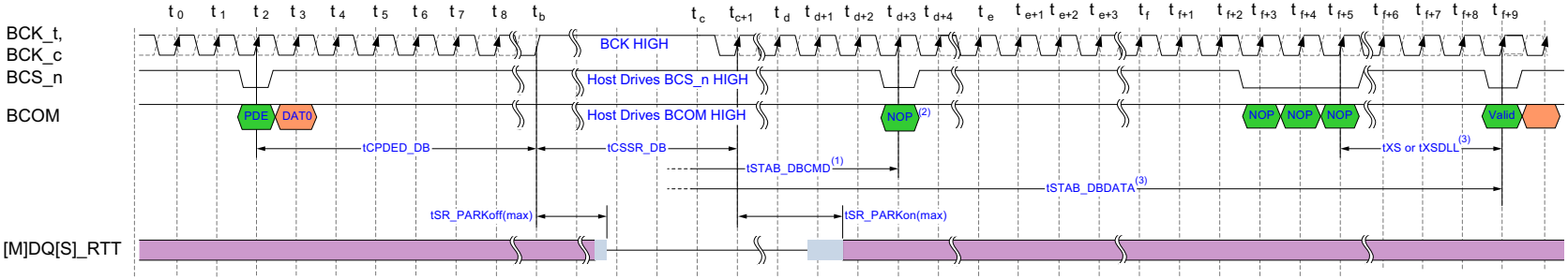
1. In LRDIMM, tSTAB01 + tSTAB_DB must be met from start of RCD DCK to the first DCA command that gets forwarded to the LRDIMM BCOM bus interface but does not use the DQ data path (e.g., SRX, NOP).
2. Instead of NOP, the host may issue “BCOMTM Entry” strap command after meeting tSTAB_DB.
3. In LRDIMM, tSTAB01 + tSTAB_DBVLD must be met from start of RCD DCK to the first DCA command that gets forwarded to the LRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

Figure 37 — Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by Clock Stop Detection Circuit



1. In LRDIMM, tSTAB_DBCMD must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does **not** use the DQ data path (e.g., SRX, NOP, etc.).
2. Instead of NOP, the host may issue "BCOMTM Entry" strap command after meeting tSTAB_DB.
3. In LRDIMM, tSTAB_DBDATA must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

Figure 38 — Self Refresh Entry Exit with Clock Stop but without Frequency Change – Termination Disabled by PDE Command with SRE Indication



1. In LRDIMM, tSTAB_DBCMD must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does **not** use the DQ data path (e.g., SRX, NOP, etc.).
2. Instead of NOP, the host may issue "BCOMTM Entry" strap command after meeting tSTAB_DB.
3. In LRDIMM, tSTAB_DBDATA must be met from start of RCD DCK to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

Figure 39 — Self Refresh Entry Exit with Clock Stop but without Frequency Change – Termination Disabled by Clock Stop Detection Circuit

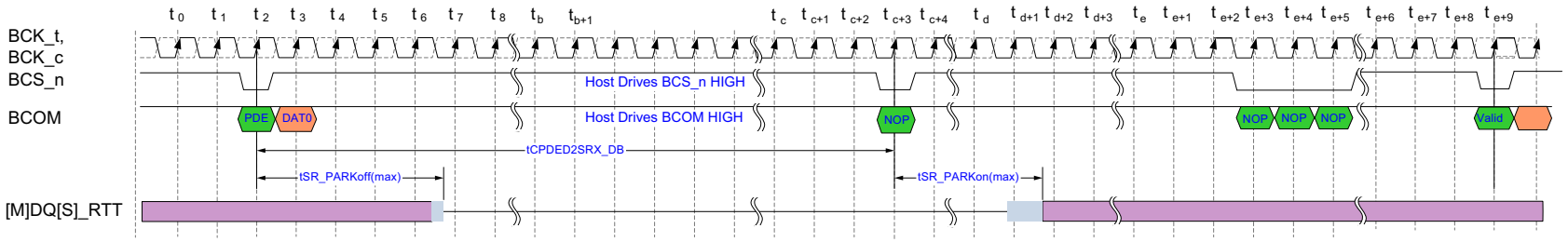


Figure 40 — Self Refresh Entry and Exit without Clock Stop – Termination Disabled by PDE Command with SRE Indication

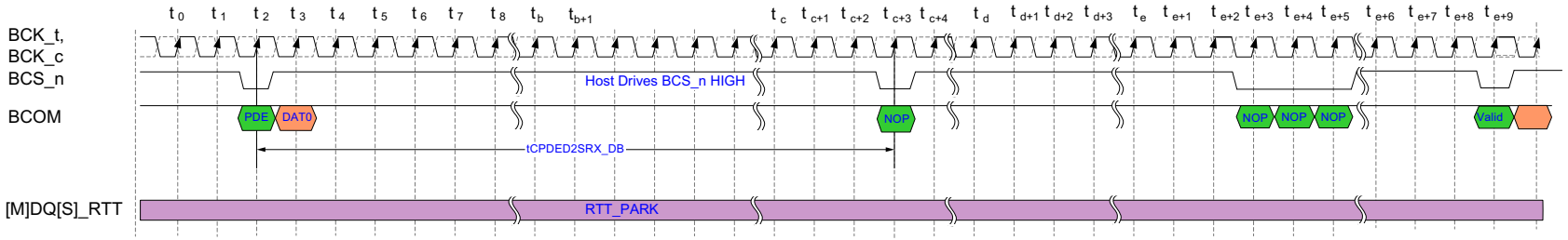


Figure 41 — Self Refresh Entry and Exit without Clock Stop – RTT_PARK Remains Enabled

5 Data Buffer Control Bus

This section describes the signals used in the DDR5 LRDIMM control bus that connects the DDR5 Register with each of the ten DDR5 Data Buffer (DB).

5.1 Control Bus Signals

Table 10 — List of Signals for Data Buffer Control Signals

Name	Description	Signal Count per channel
BCS_n	BCOM Chip Select	1
BCOM[2:0]	Data buffer command signals	3
BRST_n	BCOM Reset	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
	Total	7

5.1.1 Control Bus Signal Termination

BCK_t, BCK_c, BCS_n and BCOM[2:0] signals are terminated to VDDQ on the DDR5 LRDIMM as shown in figure.

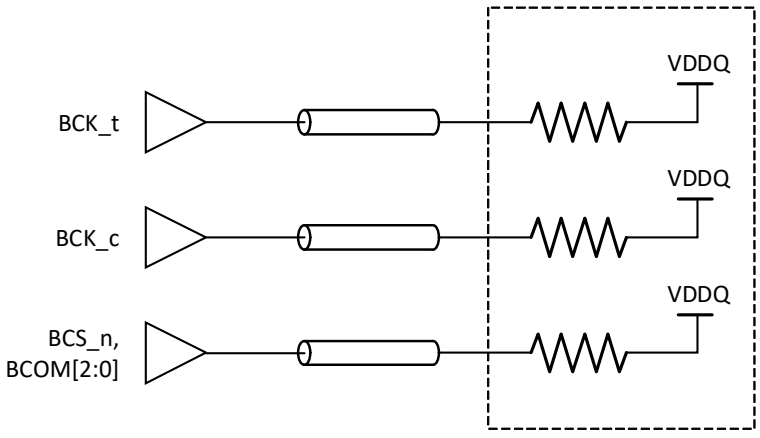


Figure 42 — Control Bus Termination

5.1.2 Control Bus Timing

The output BCOM signals are driven one clock later than the QnxCA outputs as shown in Figure 44. Like the QnxCA outputs, they are delayed by the RCD Command Latency Adder Control Word RW11.

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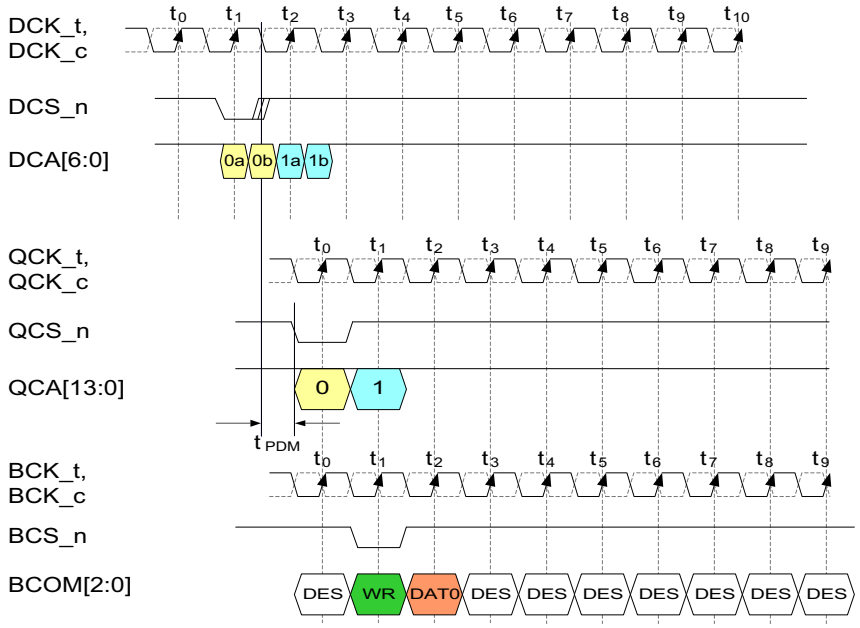

Figure 43 — Example BCOM 1N WR Command

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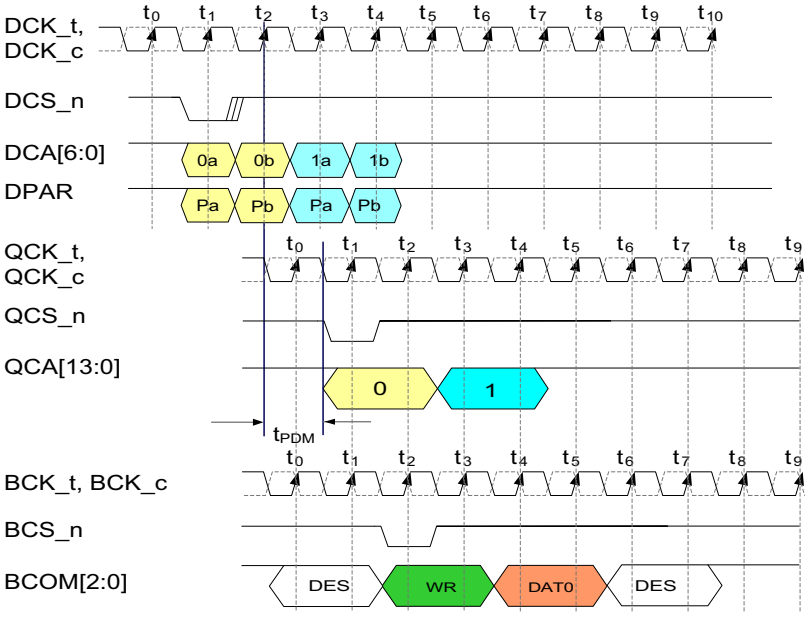
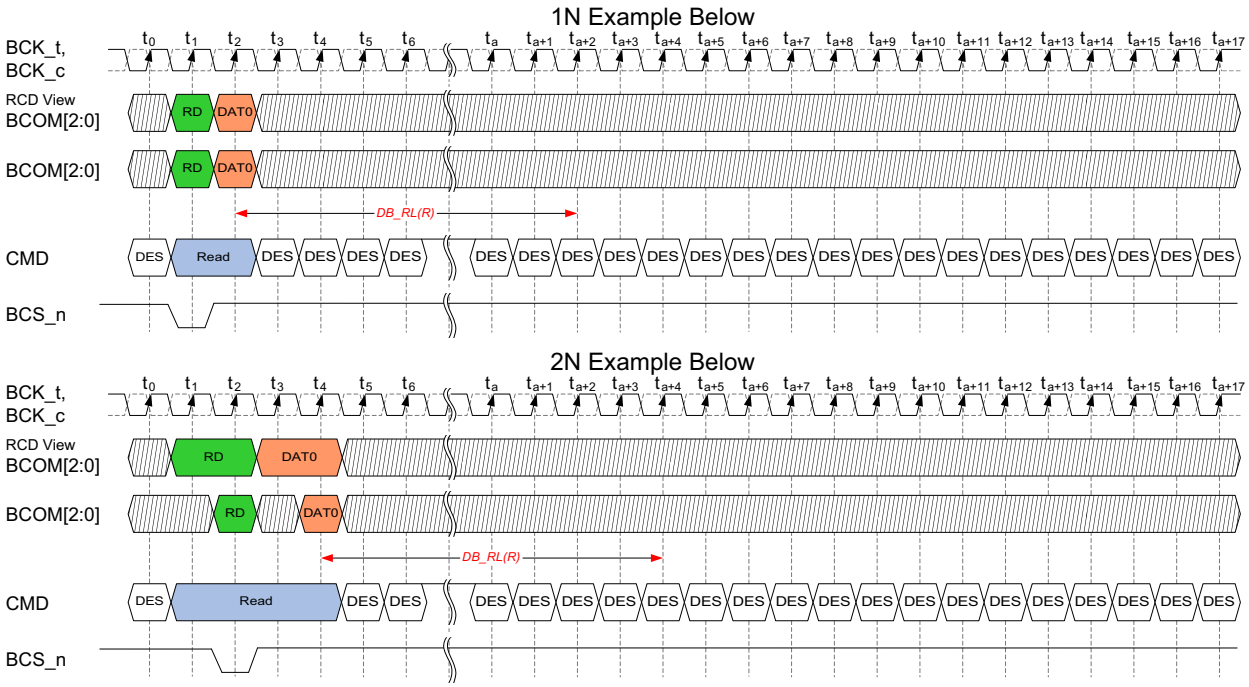


Figure 44 — Example BCOM 2N WR Command

A BCOM command can start on any clock. Figure 41 below shows the differences between standard 1N mode with a 2-cycle Read BCOM command, and what it looks like when operated in 2N mode. While in 2N mode, the host will never send two consecutive Chip Selects.



NOTE: 1. The RCD View BCOM[2:0] is shown for clarification, while BCOM[2:0] is what the Data Buffer should expect.

Figure 45 — Example of 1N vs 2N Mode - For reference only

In Figure 41, the 2N mode example shows SDR1 mode operation for “RCD view BCOM[2:0].” This is only for illustration purposes. From the point of view of the DDR5DB01 device, SDR1 and SDR2 modes are not different because the timing point of reference is determined only by the BCS_n pulse.

BCOM[2:0] are encoded such that DDR5 command bits can be used directly from the first UI of the command sequence on the RCD host interface. The mapping is as follows:

Table 11 — BCOM bus mapping

DDR5RCD CA bit	BCOM bit
CA4	BCOM0
CA3	BCOM1
CA1	BCOM2

5.2 Control Bus Commands

5.2.1 Data Buffer Control Bus Command Truth Table

Table 12 — Data Buffer Control Bus Command Truth Table

Command	Description	BCS_n	BCOM[2:0] Encoding
MRW	Mode Register Write	L	000
MRR	Mode Register Read	L	001
WR	Write	L	010
RD	Read	L	011
RFU	Reserved for Future Use	L	100
PDE	Power Down Entry	L	101
MPC	Multi-purpose CMD	L	110
NOP / PDX	Power Down exit if in power down mode.	L	111
DES	BCOM De-select	H	xxx

5.3 Command Sequences

Some commands require more than one clock cycle in order to send additional information needed by the Data Buffer in the execution of the command. This succession of command and its corresponding data transfers is called a command sequence. The command sequence for Read or Write commands requires one additional cycle to transfer the rank number corresponding to the write or read command, the sequence for MRW requires seven clock cycles in addition to the basic command, the sequence for the MRR command uses four additional clock cycles. The MPC requires three additional cycles and the PDE command requires only one additional clock cycle. The RCD will drive BCOM DES on the BUS between commands.

5.3.1 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the Data Buffer. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 16, preamble = 1 nCK, and postamble = 0.5 nCK, but an equivalent timing relationship exists for burst length = 18, 32, or 36, preamble = 2 nCK, 3 nCK or 4 nCK, and postamble = 1.5 nCK. Users should reference DRAM specification for DRAM supported pre-amble and post-amble settings.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between second cycle of RD command and the first rising edge of MDQS at the Data Buffer inputs and for the latency between second cycle of WR command and the first rising edge of MDQS at the Data Buffer outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

BCOML = 1 nCK

$DB\_WL(R)^1 = CWL + DWL(R) - BCOML$

$DB\_RL(R)^2 = CL + MRE(R) - BCOML$

1. This equation assumes that the Data Buffer MDQ-MDQS Write Delay Control Words in PG[1:0]RW[E7:E6] are at their default power-on setting.

Fractional cycle delay equations for DWL and MRE for Ranks 0 to 1 are listed below.

where xxx[R].l and xxx[R].u are the equations for the lower and upper nibbles respectively

DWL[0].l = (PG[0]RWE1[3:0] * 64 + PG[0]RWE8[5:0]) * tCK/64

DWL[0].u = (PG[0]RWE1[7:4] * 64 + PG[0]RWE9[5:0]) * tCK/64

DWL[1].l = (PG[1]RWE1[3:0] * 64 + PG[1]RWE8[5:0]) * tCK/64

DWL[1].u = (PG[1]RWE1[7:4] * 64 + PG[1]RWE9[5:0]) * tCK/64

MRE[0].l = (PG[0]RWE0[3:0] * 64 + PG[0]RWE2[5:0]) * tCK/64

MRE[0].u = (PG[0]RWE0[7:4] * 64 + PG[0]RWE3[5:0]) * tCK/64

MRE[1].l = (PG[1]RWE0[3:0] * 64 + PG[1]RWE2[5:0]) * tCK/64

MRE[1].u = (PG[1]RWE0[7:4] * 64 + PG[1]RWE3[5:0]) * tCK/64

Table 13 — Data Buffer PG[1:0] Rank Training Control Word Decoding

Register Control Word	Meaning
RWE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word
RWE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word
RWE2	Lower nibble DRAM interface receive enable training control
RWE3	Upper nibble DRAM interface receive enable training control
RWE8	Lower nibble DRAM interface write leveling control
RWE9	Upper nibble DRAM interface write leveling control

2. This equation assumes that the Data Buffer MDQS Read Delay Control Words in PG[1:0]RW[E5:E4] are at their default power-on setting.

The Data Buffer delays tPDM_RD and tPDM_WR are defined as the delay between first effective rising edge of MDQS and the first effective rising edge of DQS for a RD command and as the delay between first effective rising edge of DQS and the first effective rising edge of MDQS for a WR command respectively. By default these delays are constant per Data Buffer for all ranks and nibbles, however the DB may need to adjust tPDM for non-default register settings in order to maintain the data path fall through time in the device.

Timing parameters that are integer multiples of tCK are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of tCK are shown in *red italic* letters.

For simplicity, the timing diagrams only show one of the possible host interface termination modes and RTT_PARK is never shown even though it is always supported.

5.3.2 WR/RD Burst Length Processing

Table 14 — WR/RD Burst Length Processing

DRAM MR0 Snooped BL Type PG8RWE0[1:0]	DRAM MR50 Snooped WR/RD CRC Enabled PG8RWE8[1:0]	WR/RD Sequence DAT0 BCOM[0]	DB Burst Length Processing (BL)	DB Burst Length Processing Details
00 = BL16 Fixed	Disabled	X	16	
	Enabled	X	18	
01 = BC8 OTF	Disabled	0 = BC8	8	
		1 = BL16	16	
	Enabled	X	18	
10 = BL32 Fixed	Disabled	X	32	The dummy WR/RD command that is 8tCK after the primary WR/RD command is ignored[1]
	Enabled	X	36	The dummy WR/RD command that is 9tCK after the primary WR/RD command is ignored.[1]
11 = BL32 OTF	Disabled	0 = BL32	32	The dummy WR/RD command that is 8tCK after the primary WR/RD command is ignored.[1]
		1 = BL16	16	
	Enabled	0 = BL32	36	The dummy WR/RD command that is 9tCK after the primary WR/RD command is ignored.[1]
		1 = BL16	18	

1. The dummy WR/RD command is assumed to be to the same rank and of the same burst length type as the primary WR/RD command.

5.3.3 Control Word Burst Length Processing

Table 15 — Control Word Burst Length Processing

DRAM MR0 Snooped BL Type PG8RWE0[1:0]	DRAM MR50 Snooped Read CRC Enable (PG8RWE8[0])	Control Register Command Sequence	DB Burst Length Processing (BL)	DB Burst Length Processing Details
XX	Disabled	DRAM-Space MRR	16	
	Enabled		18	
XX	Disabled	DB-Space MRR to a Control Register	16	
	Enabled		18	The last two bits of the BL18 burst are Don't Care X
XX	Disabled	DB-Space MRR to the Read Training Pattern	16	
	Enabled		Illegal	The DB assumes that the host will ensure that read CRC is disabled since it is necessary for the LFSR pattern to be kept continuous. Read CRC is unnecessary since the known LFSR pattern intrinsically allows for error checking.

Table 16 — PBA Control Word Burst Length Processing

DRAM MR0 Snooped BL Type (PG8RWE0[1:0])	DRAM MR50 Snooped Write CRC Enable (PG8RWE8[1])	Control Register Command Sequence	DB Burst Length Processing (BL)	DB Burst Length Processing Details
XX	Disabled	PBA Enumerate ID Programming MRW	16	Used to capture the Enumerate ID.
	Enabled		Illegal	The DB assumes that the host will ensure that write CRC is disabled.

5.3.4 MRW Commands

The RCD generates MRW commands to the data buffers for each MR command. Table 17 shows the sequence for MRW commands.

Table 17 — Multi-cycle Sequence for MRW Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MRW	MRW Command BCOM[2:0] = 000
2	1	DAT0	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[2:1] = RFU
3	1	DAT1	BCOM[1:0] = MRA[7:6] BCOM[2] = RFU
4	1	DAT2	BCOM[2:0] = MRA[5:3]
5	1	DAT3	BCOM[2:0] = MRA[2:0]
6	1	DAT4	BCOM[1:0] = OP[7:6] BCOM[2] = RFU
7	1	DAT5	BCOM[2:0] = OP[5:3]
8	1	DAT6	BCOM[2:0] = OP[2:0]
9		Next Cmd	Next Command

The sequence for an MRS Write command is shown in Figure 46 below. The timing diagrams show how the MR Write command is followed by seven data transfer cycles. Since the command sequence uses eight cycles, it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the MRW command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRW command also imposes a limitation on how close consecutive MRW commands can be issued to the Data Buffer.

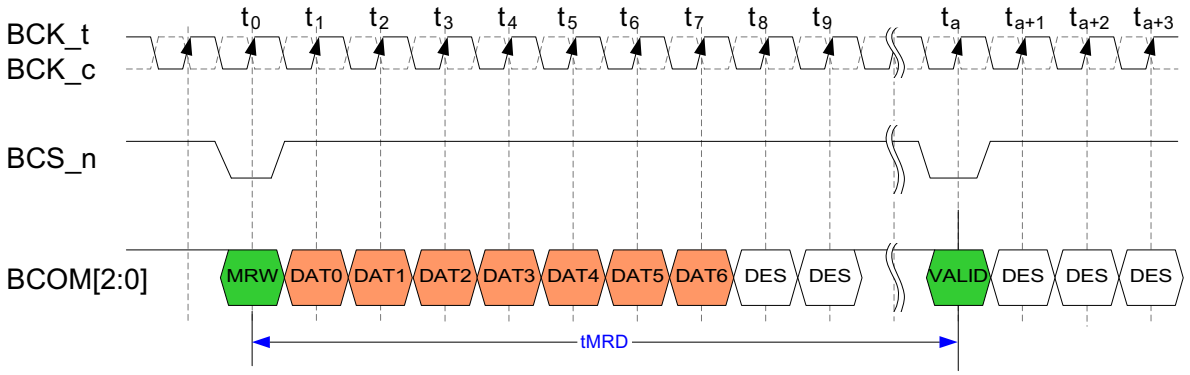


Figure 46 — MRW command sequence

5.3.5 MRR Commands

5.3.5.1 Multi-cycle Sequence for MRR Commands

Table 18 shows the sequence for MRR commands.

Table 18 — Multi-cycle Sequence for MRR Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MRR	Mode Register Read Command BCOM[2:0] = 001
2	1	DAT0	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU Note: Burst length is fixed BL16
3	1	DAT1	BCOM[1:0] = MRA[7:6] BCOM[2] = RFU
4	1	DAT2	BCOM[2:0] = MRA[5:3]
5	1	DAT3	BCOM[2:0] = MRA[2:0]
6		Next Cmd	Next Command

If BCS_n is active for 2 clock cycles, it indicates a non-target read termination. The Data Buffer will terminate with RTT_NOM_RD and will not transfer/send data through/from the buffer. In this case, the DB will use Rank 0 or Rank 1 timing automatically depending on the settings in RW80[4] (see Table 67 on page 102).

MRR commands read data from the MR locations in either the DRAM or the data buffer. MR locations in the RCD must be read by first transferring their contents to a DRAM register then reading that DRAM register. If the CW bit is a 0, the read will come from the DRAMs, and the data buffer will treat this command like a read command. The case CW = 1 MRA7 = 0 is not defined. Data Buffer will treat it as invalid address and Read zeros. If the CW =1 and MRA7 = 1, then read will come from the Data Buffer's MR location. The Data Buffer will send the same data on all DQs for the second 8 UI and drive HIGH or LOW on the first 8 UI as shown in Table 18.

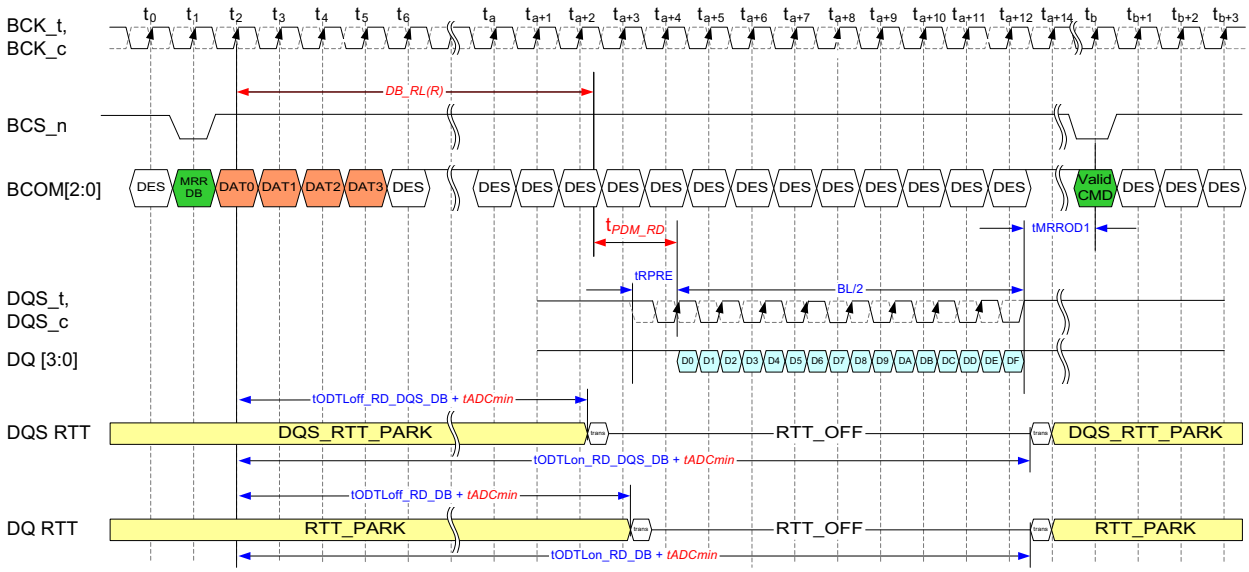


Figure 47 — MRR Command Sequence to Data Buffer address space

5.3.5.2 Short MRR Command for SDR Training.

Table 19 — Short MRR Command for SDR Training[1]

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MRR	Mode Register Read Command BCOM[2:0] = 001
2	1	DAT0	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU Note: Burst length is fixed BL16
6		Next Cmd	Next Command

1. Provides a shorter MRR command for SDR mode Host interface Data Buffer DQ training to maintain a continuous read from Data Buffer

Table 20 — MRR Read Format for Data Buffer Return

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12	UI 13	UI 14	UI 15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

Table 21 — MRR Read Format for Data Buffer Return with Read CRC Enabled

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12	UI 13	UI 14	UI 15	UI 16	UI 17
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x

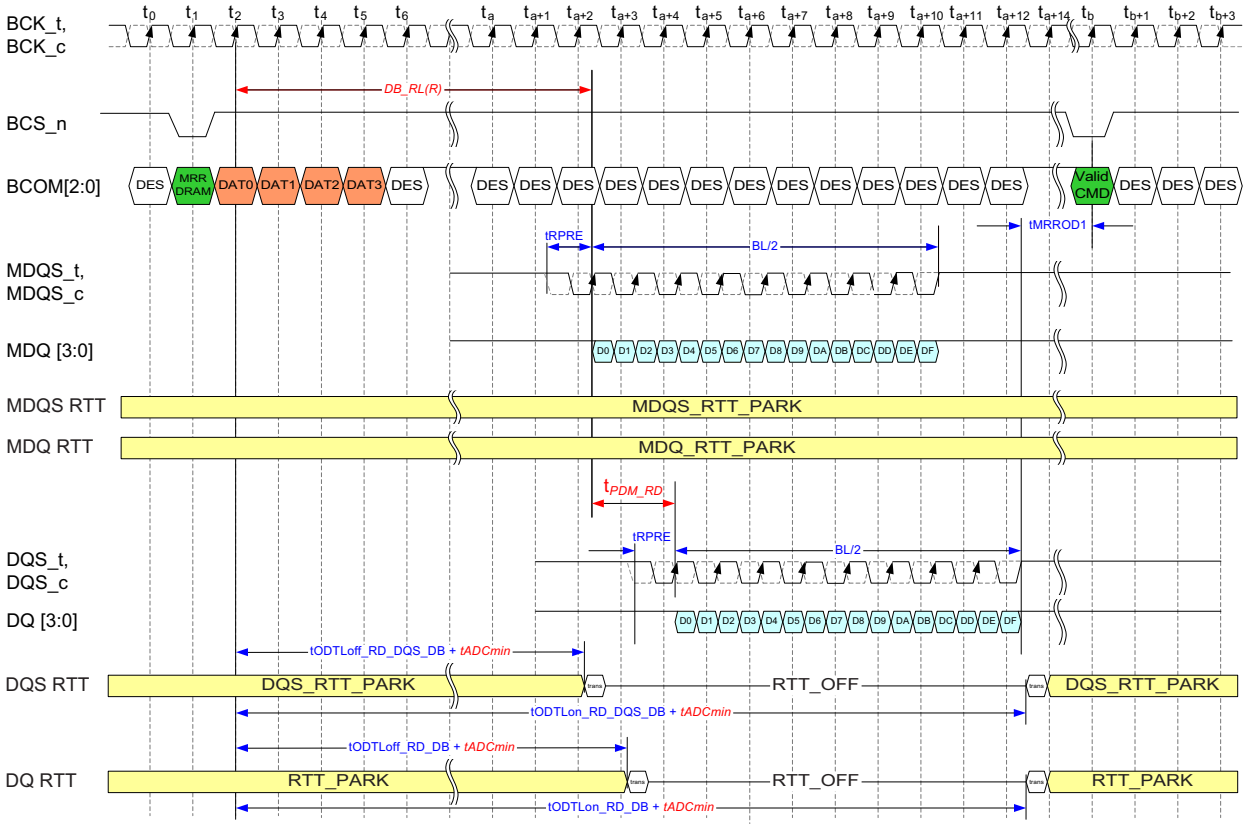


Figure 48 — MRR Command Sequence to DRAM Address Space

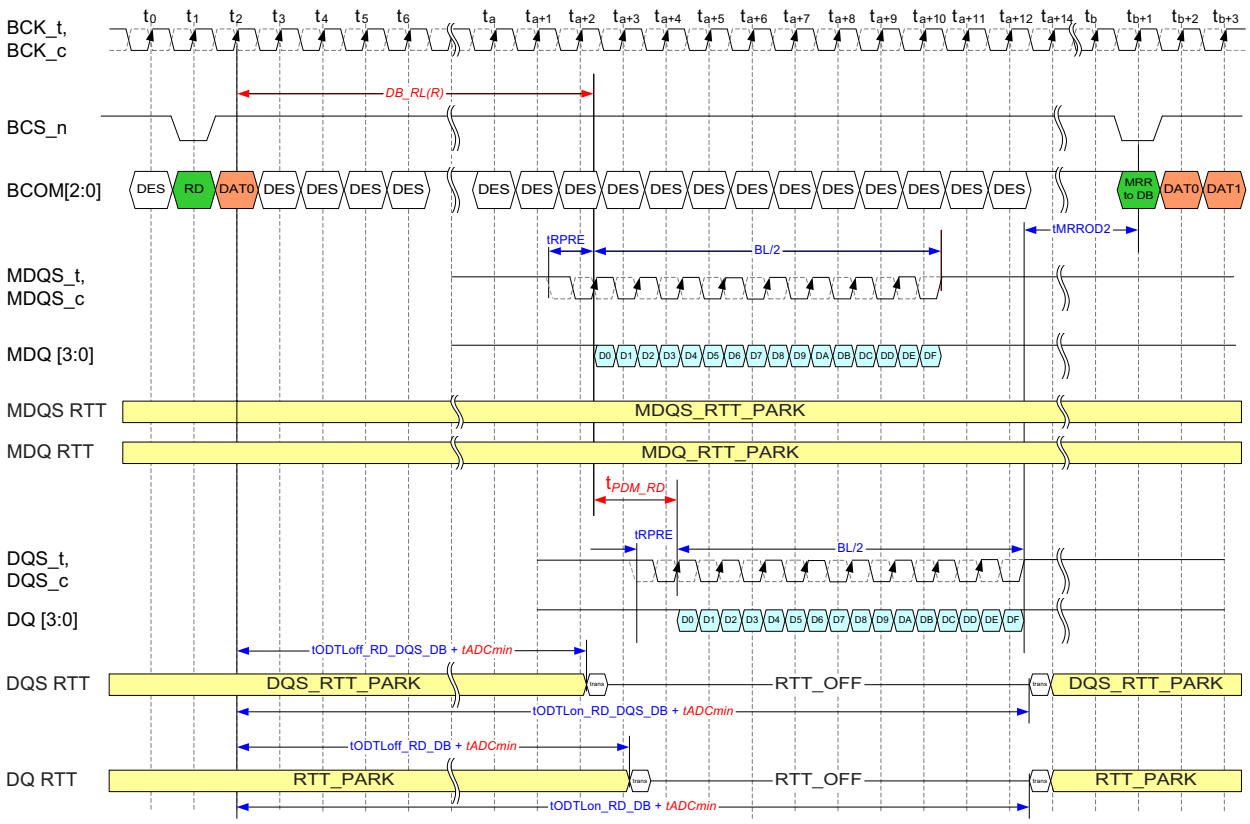
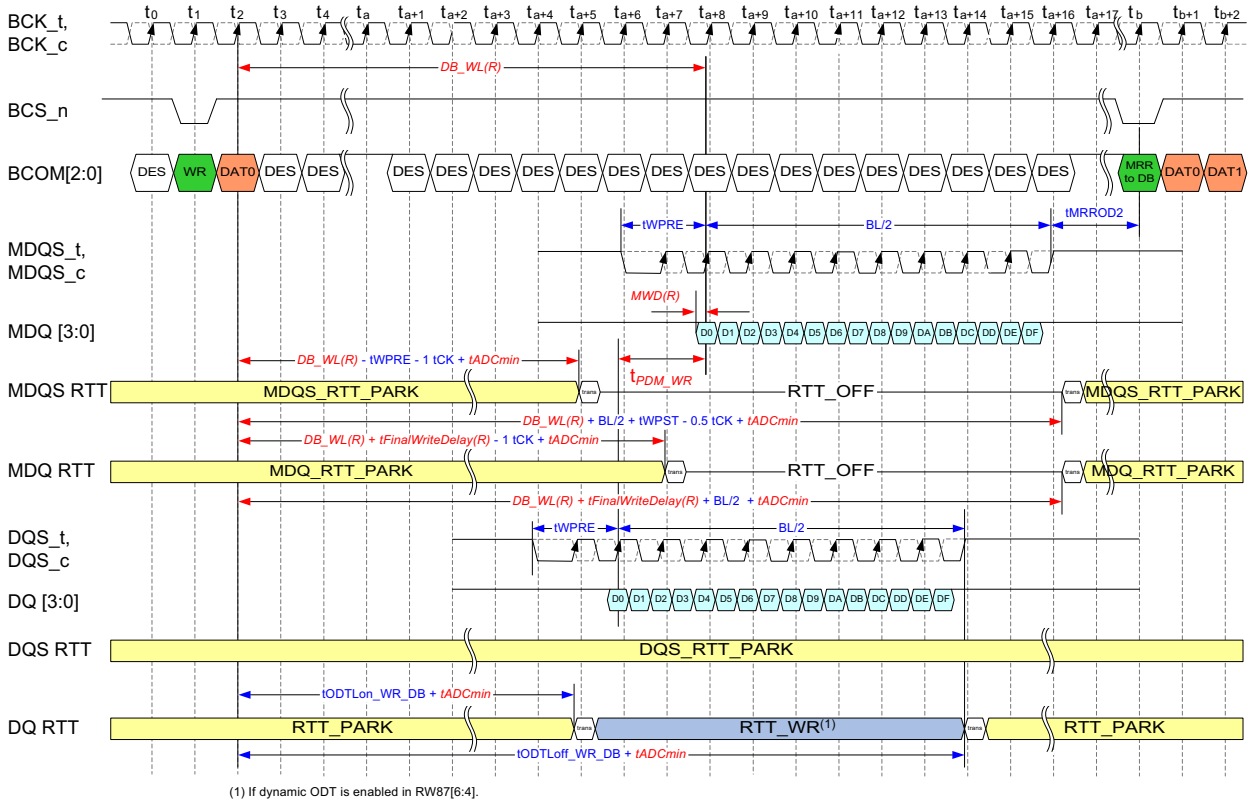


Figure 49 — RD to MRR Command Sequence to Data Buffer Address Space



Note: tFinalWriteDelay(R) = tMdqWriteBaselineDelay(R) + tDram_DqsDelay_Change(R)[1]

Figure 50 — WR to MRR Command Sequence to Data Buffer Address Space

1. Devices are also allowed to apply the per-bit MDQ Write delay settings (PG[1:0]RW[F1:EE]) in the MDQ_RTT_PARK timings.

5.3.6 WR Commands

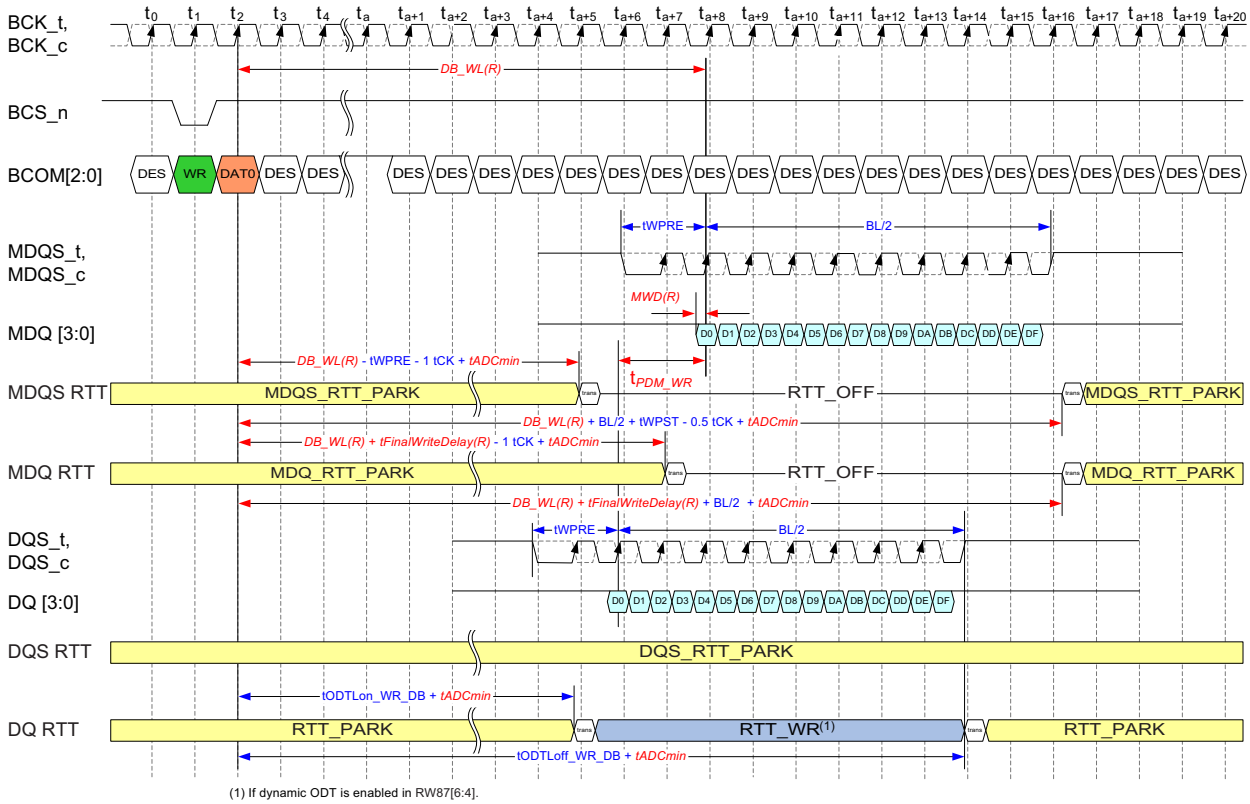
Table 22 shows the sequence for write (WR8, WR16) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 2 that needs to be accessed and the burst length information for the data transfer. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the Data Buffer PG8RWE8, the burst length will be 18UI, or be 36 UI, see Table 14, “WR/RD Burst Length Processing”.

Table 22 — Multi-cycle Sequence for WR Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	WR	Write command BCOM[2:0] = 010
2	1	DAT0	Rank ID & BL BCOM[0] = BL. 0 = BC8 or BL32, 1 = BL16 BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU
3		Next Cmd	Next Command

If BCS_n is active for 2 clock cycles, it indicates a non-target write termination. The Data Buffer will terminate with RTT_NOM_WR and will not transfer data through the buffer. In this case, the RCD will send Rank0 and DB will use Rank 0 or Rank 1 timing automatically depending on the settings in RW80[4] (see Table 67 on page 102).

Figure 51 shows the timing sequence for a Write command.



Note: tFinalWriteDelay(R) = tMdqWriteBaselineDelay(R) + tDram_DqsDelay_Change(R)[1]

Figure 51 — WRITE Timing

Enable and disable timings for MDQ_RTT_PARK include the MDQ Write Baseline as well as the Write delay adjustment from DRAM tDQS2DQ periodic updates (i.e., tDram_DqsDelay_Change). Devices are also allowed to apply the per-bit MDQ Write delay settings (PG[1:0]RW[F1:EE]) in the MDQ_RTT_PARK timings.

5.3.7 RD Commands

Table 23 shows the sequence for read (RD8, RD16) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 2 that needs to be accessed and the burst length information for the data transfer. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[0] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the Data Buffer if the BL field in the PG8RWE0 snoop register is set for fixed burst length of 8 or 16 or 32. If CRC is enabled in the DRAM and in the Data Buffer PG8RWE8, the burst length will be 18UI or be 36 UI, see Table 14, “WR/RD Burst Length Processing”.

1. Devices are also allowed to apply the per-bit MDQ Write delay settings (PG[1:0]RW[F1:EE]) in the MDQ_RTT_PARK timings.

Table 23 — Multi-cycle Sequence for RD Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	RD	Read command BCOM[2:0] = 011
2	1	DAT0	Rank ID & BL BCOM[0] = BL. 0 = BC8 or BL32, 1 = BL16 BCOM[1] = RANK_ID; 0 = Rank 0, 1 = Rank 1 BCOM[2] = RFU
3		Next Cmd	Next Command

If BCS_n is active for 2 clock cycles, it indicates a non-target read termination. The Data Buffer will terminate with RTT_NOM_RD and will not transfer data through the buffer. In this case, the RCD will send Rank0 and DB will use Rank 0 or Rank 1 timing automatically depending on the settings in RW80[4] (see Table 67 on page 102).

Figure 52 shows the timing sequence for a Read command.

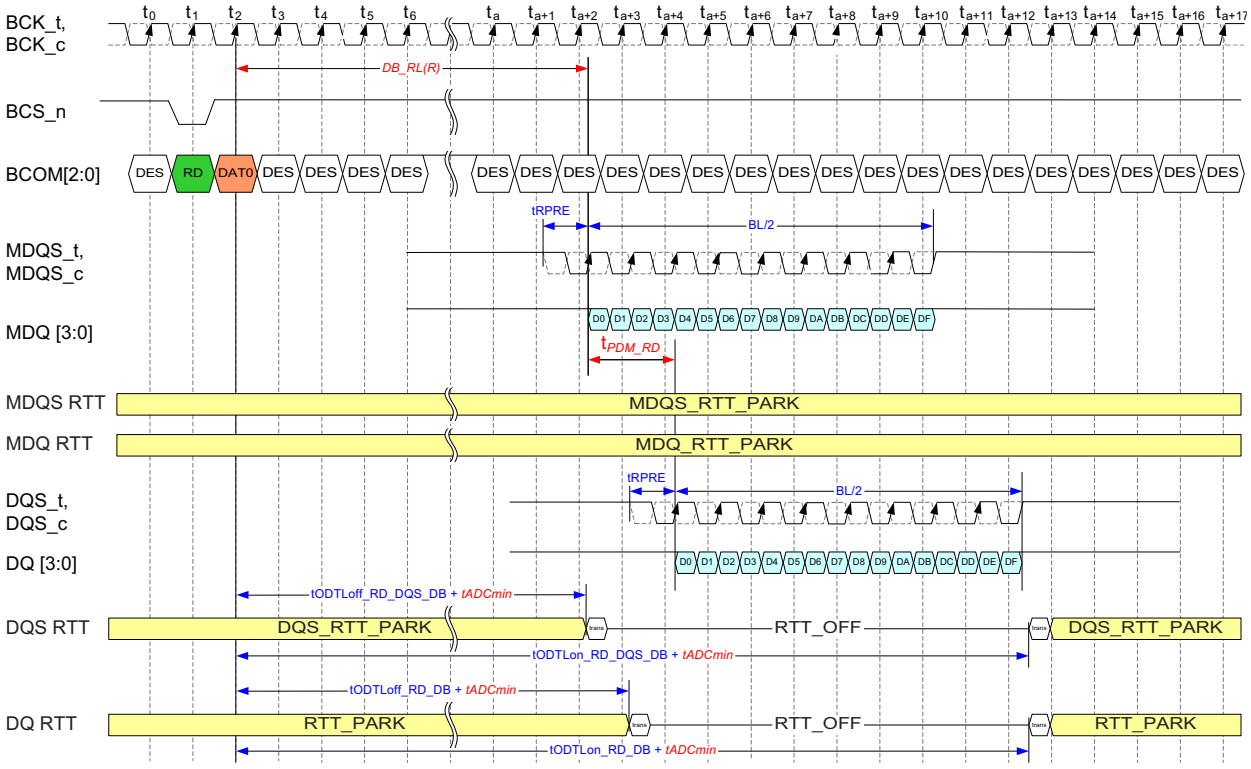


Figure 52 — READ Timing

5.3.8 PDE Commands

The Power Down Entry command is only sent on the BCOM bus when all ranks are being put into or are already in power down. Table 24 shows the sequence for PDE commands.

Table 24 — Multi-cycle Sequence for PDE Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	PDE[1]	Power-Down Entry Command BCOM[2:0] = 101
2	1	DAT0	PDE Modes and ODT BCOM [0] = ODT; 0 = Enabled, 1 = Disabled BCOM [1] = PDE MODE; 0 = Self-Refresh, 1 = PDE BCOM [2] = RFU
3		Next Cmd	Next Command

1. Since the PDE command is a 1UI command on the DRAM bus and a 2UI command on the BCOM bus, the host controller must ensure there is enough spacing between the PDE command any next command that would be sent on the BCOM bus.

5.3.9 MPC Command

Table 25 shows the sequence for MPC commands.

Table 25 — Multi-cycle Sequence for MPC Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	MPC	Multi-purpose Command BCOM[2:0] = 110
2	1	DAT0	BCOM[1:0] = OP[7:6] BCOM[2]= RFU
3	1	DAT1	BCOM[2:0] = OP[5:3]
4	1	DAT2	BCOM[2:0] = OP[2:0]
5		Next Cmd	Next Command

5.3.10 NOP / Power Down Exit

Table 26 shows the sequence for NOP / PDX commands.

Table 26 — Multi-cycle Sequence for NOP/PDX Commands

Time (clock cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	NOP/PDX	NOP / PDX Command BCOM[2:0] = 111
2		Next Cmd	Next Command

When in power down, an active BCS_n signal will return the Data Buffer to the active state. The BCOM command will indicate NOP so that no other command is executed.

6 BCOM Training Mode (BCOMTM) - Data Buffer Interface

BCOMTM is a method to facilitate the feedback of a logical combination of the sampled BCOM[2:0] and BCS_n signals. In this mode, the BCK is running and the BCK samples the BCOM and BCS_n signals every rising edge of BCK. A feedback equation that includes all the BCOM and BCS_n signals results in an output value that is sent on the DQ signal back to the host memory controller. The RCD timings for BCS_n and BCOM[2:0] signals can then be optimized for proper alignment to the BCK signal. When the Data Buffer is in this mode, no functional commands are executed. The functional command interface is restored only after exiting BCOMTM. The Data Buffer can exit BCOM TM in three ways, which requires a reset with BCOM[2:0] straps all HIGH, with straps all LOW, or with straps set for the BCOM TM exit (010), see Table 27.

6.1 Entry and Exit for BCOM Training Mode

BCOMTM is enabled by a static value of BCOM[2] = LOW, BCOM[1] = LOW, and BCOM[0] = HIGH on the BCOM signals when BRST_n de-asserts. The Data Buffer captures encoding on BCOM signal pins.

BCOMTM Exit by a static value of BCOM[2] = LOW, BCOM[1] = HIGH, and BCOM[0] = LOW on the BCOM signals when BRST_n de-asserts. The Data Buffer captures encoding on BCOM signal pins.

6.2 Data Buffer Training States

When the Data Buffer powers up the command bus may need to be trained prior to normal operation. In order to set BCOM VREF and enable BCOM Training Mode, the following training states will be supported by the DDR5DB01:

BCOMTM, set 1N BCOM CMD Timing, and set BCOM VREF as shown in Table 27.

Table 27 — BCOM Strap for Data Buffer Training States

BCS_n Static value[1]	BCOM[2:0] Static Value	Description	tStrap_Delay[2]
H	000	Normal operation - RESET[3]	tSTAB_DB (Max)
H	001	BCOMTM ENTRY[4]	tBCOMTM_Entry (Max)
H	010	BCOMTM EXIT[5]	tBCOMTM_Exit (Max)
H	011	Set 1N BCOM CMD Timing[6]	tBCOM_1N (Max)
H	100	Set BCOM BVref to 75% VDD[7,8]	tBCOM_Vref (Max)
H	101	Increase voltage of BCOM BVref by 1%[7,8]	tBCOM_Vref (Max)
H	110	Decrease voltage of BCOM BVref by 1%[7,8]	tBCOM_Vref (Max)
H	111	Normal operation - RESET[3]	tSTAB_DB (Max)

1. The host is required to drive BCS_n HIGH and the DB ignores BCS_n when decoding Strap command.
2. Minimum waiting times the host must guarantee from Strap command being captured to the next valid command, shown in Figure 53 and defined in Table 155, “Input Timing requirements”.
3. Normal Reset - default reset - all non-sticky control registers are restored to their default states (which is “0”, except when explicitly defined otherwise).
4. BRST_n sequence only sets BCOMTM enable within buffer. Retain any previous control word values, internal register and any previous Vref values
5. BRST_n sequence only clears BCOMTM enable within buffer. Retain any previous control word values, internal register and any previous Vref values
6. BRST_n sequence only sets BCOM CMD timing. Retain any previous control word values. When Host applies “Set 1N BCOM CMD Timing,” RW80[0] and RW80[7] will be updated to 1N mode.
7. BRST_n sequence only sets BCOM BVref within buffer. Retain any previous control word values.
8. The Data Buffer will update the BVref control word PG[2]RWFA setting so that it reflects the voltage value resulting from executing this Strap command.

When BRST_n de-asserts the Data Buffer captures encoding on BCOM signal pins.

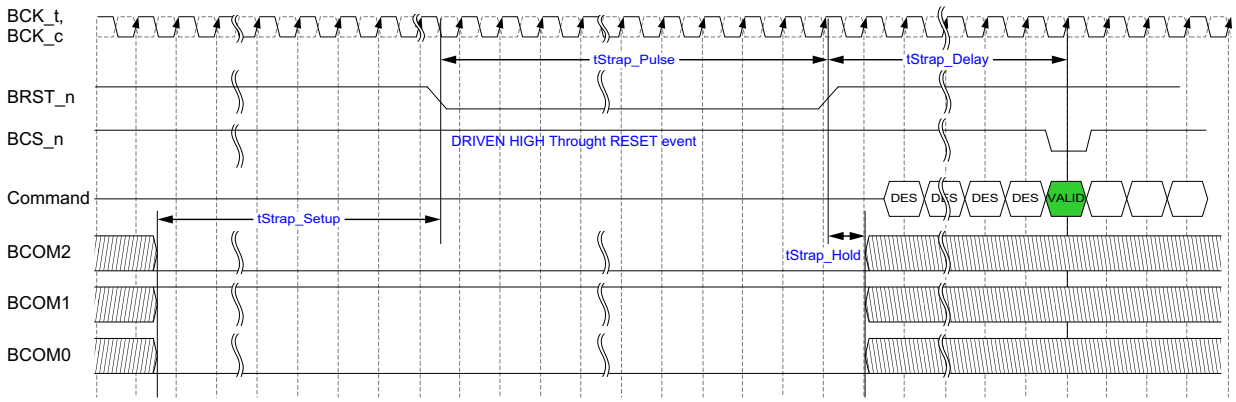


Figure 53 — Strap Example

6.3 BCOM Training Mode (BCOMTM) Operation

In BCOMTM the BCOM values are sampled on every rising BCK edge. In BCOMTM the BCS_n signal is also sampled on every rising BCK edge as an input signal and does not qualify the BCOM signals. Once the BCOM and BCS_n signals are sampled, the values are XOR'd to produce an XOR Sample. This XOR Sample is logically combined with other XOR Samples in the sequence to produce an output value that is driven on all the DQs, as a static value.

During BCOM Training Mode the module-level BCOM termination is enabled as for functional operation. The BCOM VREF is set according to the value programmed through the BRST_n static BCOM settings. The timing requirements for the BCOM bus, BCK_t, BCK_c, and BCS_n are the same as for functional operation.

The delay from when the BCOM and BCS_n signals are sampled and when the output of the logical combination of XOR Samples is driven on the DQ signals is specified as t_{BCOMTM_Valid}, as shown in the following figure. The XOR Samples should alternate between a 0 and 1 in order to produce a training pattern with consistent feedback to the host. The pattern is generated by the host and leverages the BCOM Pass Through mode in the RCD. The BCOM training pattern will assert BCS_n LOW one or more times for each BCOM/BCS_n or BCK output delay setting change.

On the Host interface, while in BCOM training mode, the DB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination (DQ_RTT_PARK, DQ_RTT_NOM_WR, DQ_RTT_NOM_RD, DQ_RTT_WR). Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS_RTT_PARK continuously on DQS if enabled.

As shown in Figure 54, the Data Buffer device is required to disable the DQ outputs within tBCOMTM_Exit after executing a BCOMTM Exit strap command. Since there is no minimum value defined for tBCOMTM_Exit, the DQ outputs can be disabled any time between the BCOMTM_Exit command and tBCOMTM_Exit (Max).

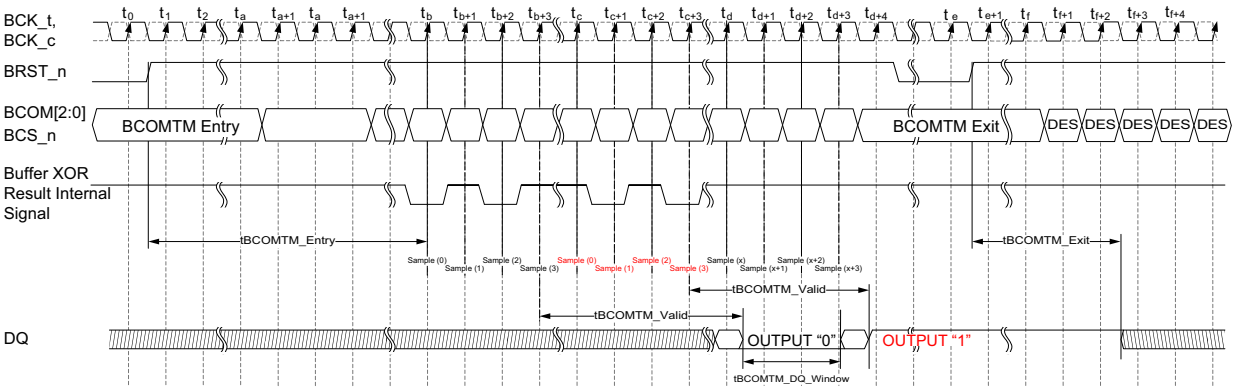


Figure 54 — Timing Diagram for BCOMTM

6.4 BCOM Training Feedback Equations

The BCOMTM Output is computed based on the BCS_n assertion and the values of the BCOM inputs. The following Table 28 clarifies the output computation.

Table 28 — XOR Sample

BCK	BCOMTM XOR Sample
Rising Edge	XOR (BCOM[2:0], BCS_n)
Falling Edge	No Sample

In BCOMTM, the BCOM and BCS_n values are sampled on all BCK rising edges and XOR'd. Each group of 4 consecutive XOR samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The XOR samples evaluation to determine the output is as follows:

Table 29 — Sample Evaluation for Intermediate Output[0]

Output[0]	XOR Sample[0]	XOR Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 30 — Sample Evaluation for Intermediate Output[1]

Output[1]	XOR Sample[2]	XOR Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 31 — Sample Evaluation for final BCOMTM Output

BCOMTM Output[1]	Output[0]	Output[1]
0	0	0
1	0	1
1	1	0
1	1	1

1. When there is no change on the BCOMTM Output from previous evaluation, DQ shall continue to drive same value continuously with no switching on the bus.

7 Per X Addressability Modes

7.1 Per DRAM Addressability (PDA) Mode

The DDR5DB01 will need to support DQ pass through mode, details in Chapter 3.4, “DQ Pass Through Mode”.

7.2 Per Buffer Addressability (PBA) Mode

It is necessary for the data buffer to support a feature similar to per-DRAM addressability for buffer control word access transactions. This feature will be used to allow the host controller to configure each data buffer independently from each other. This is a requirement, for example, to allow independent DFE register settings per buffer.

DDR5 introduces a BCOM interface-only method for Per Buffer Addressability, by having a unique PBA Enumerate ID in each Data Buffer and the ability to set a PBA Select ID in all Data Buffers.

The unique PBA Enumerate ID requires the use of the DQ signals and a PBA Enumerate Programming Mode in the Data Buffer to program.

Once the PBA Enumerate ID has been programmed, subsequent commands do not use the DQ signals (Legacy PBA mode) to designate which Data Buffer is selected for the command. The PBA Enumerate ID is a 4-bit field which is different in each Data Buffer. The PBA Select ID is also a 4-bit field which is set dynamically via MRW commands and it set to the same value in all Data Buffers.

When the PBA Select ID is the same as the PBA Enumerate ID or when the PBA Select ID is set to the “All Buffers” code of 1111B, the Buffer will apply the MRW command.

During RESET procedure, the receive FIFO must be initialized with all ones in order to ensure that the PBA enumerate flow does not program an enumerate ID when the strobes are not officially toggling. This is specifically for the case where the DIMM is connected in a test environment where the strobes of some devices are not connected. Those buffers will retain the default ID of 15.

7.3 PBA Enumerated ID Programming

PBA Enumerate Programming Mode is enabled by setting the PBA Enumerate Mode bit to a 1. While in this mode only MRWs to the PBA Enumerate ID Control Word or the PBA Enumerate Enable Control word (to disable the mode) are permitted. There are two sequences that may be used to perform PBA Enumerated ID Programming. Sequence A involves providing a single burst of 16 strobe edges sent in association with the PBA Enumerate ID MRW command. Sequence B involves a continuous toggling of the DQS_t and DQS_c.

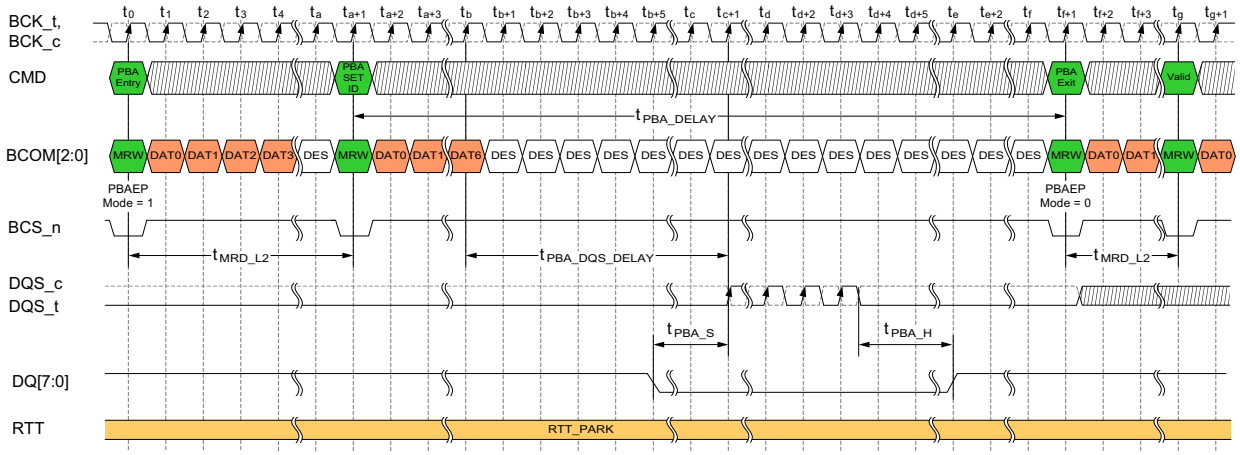
In PBA Enumerate Programming Mode, the default (or previously programmed) RTT_PARK value will be applied on the DQ signals.

In PBA Enumerate Programming Mode, only PBA Set ID MRW commands and Exit PBA Enumerate Programming Mode MRW commands are allowed.

To remove the DB from PBA Enumerate Programming Mode, send an Exit PBA Enumerate Programming MRW command. The Exit PBA Enumerate Programming Mode MRW command is never qualified by the DQ settings and is applied to all DBs.

During the PBA Enumerate ID Programming mode, the host is only allowed to execute one Enumerate Command in each DB device (i.e., MRW to PBA Enumerate ID with the corresponding DQ0 or DQ4 bit LOW). Once the PBA Enumerate ID is programmed in a DB, any change for the PBA Enumerate ID requires the host to perform a new PBA Enumerate ID Programming sequence.

7.3.1 Sequence A - Single Burst of 16 Strobe Edges



Note 1: The PBA Set ID MRW command cycle time is defined as tPBA_DELAY. This time is longer than the normal MRD_L2 and must be met in order to provide the DB time to latch the asserted DQ and complete the write operation to the PBA Enumerate ID control word prior to the next PBA Set ID command.

Figure 55 — PBAEP Mode Entry, Programming of PBA Enumerate ID, and PBAEP Mode Exit

Prior to enabling PBA Enumerate Programming Mode, the host must drive DQS_t and DQS_c differentially LOW, other than when the burst of 16 strobe edges is sent in association with the PBA Enumerate ID MRW command. The host must send preamble and postamble DQS_t/DQS_c toggles during the qualification of the PBA command.

Once PBA Enumerate Programming Mode is enabled in the Data Buffer, the host memory controller shall wait tMRD_L2 to the time the first PBA Enumerate ID MRW command is issued.

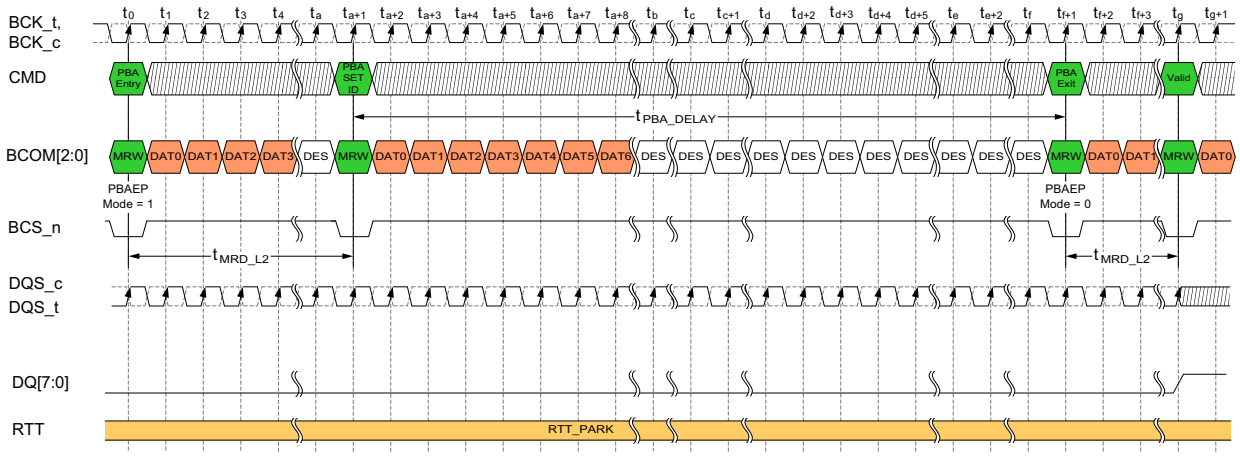
When a PBA Enumerate ID command is sent, only the buffer which samples its DQ0 bit LOW or its DQ4 bit LOW will enumerate itself with the ID. Data Buffers which sample both the DQ0 bit HIGH AND DQ4 HIGH will retain their previous enumeration ID.

A complete BL16 set of strobe edges (8 rising edges and 8 falling edges) must be sent by the host within the tPBA_DQS_DELAY min/max range from the MRW command. The DB is allowed to use any one of the strobe edges or set of edges—for example, the last 4 strobe edges—to capture the DQ value during the valid Low duration of the target DQ. Valid Low time is defined as the time between tPBA_S and tPBA_H. If the DB captures a 0 on DQ0 or DQ4 at any strobe edge in the strobe sequence, the PBA Enumerate ID command shall be executed by the DB. Since the write timings for the DQ bus have not been trained, the host must ensure a minimum of 16 strobe edges occurs after a period of tPBA_DQS_DELAY(min) after the associated MRW command. The BC8 control word setting in the DB is ignored while in PBA Enumerate Programming mode. The DQS assumes preamble/postamble requirements.

An example of PBA Enumerate Sequence A is as follows:

1. All buffers default to ID=15.
2. The host sends an MRW to the Select ID Control Word with a 15 to select all devices (if not already set that way).
3. The host begins driving DQS_t and DQS_c differentially LOW.
4. The host sends an MRW to the Enumerate Enable Control Word to enable PBA Enumerating Programming mode.
5. The host sends an MRW to the Enumerate ID Control Word with an ID of 0000, driving a 0 onto the DQ signals of the buffer that it desires to enumerate with an ID of 0. The strobes are toggled as described above. The host drives 1s on all other DQ signals. The host sends the BL16 strobe sequence on ALL strobes.
6. The host repeats the above step with IDs of 0001 through 0100 to enumerate the remaining 4 buffers, driving their DQ signals LOW on the appropriate command.
7. The host sends an MRW to the Enumerate Enable Control Word to Disable PBA mode.
8. All buffers are uniquely enumerated.

7.3.2 Sequence B - Continuous DQS Toggle



Note 1: The PBA Set ID MRW command cycle time is defined as tPBA_DELAY. This time is longer than the normal MRD_L2 and must be met in order to provide the DB time to latch the asserted DQ and complete the write operation to the PBA Enumerate ID control word prior to the next PBA Set ID command.

Figure 56 — PBA Enumerate Programming Mode w/Continuous DQS Toggle Timing Diagram

Prior to enabling PBA Enumerate Programming Mode, the host drives the proper DQs low and begins toggling DQS_t/DQS_c. As shown in Figure 56, the host continues to drive these signals in this manner through the sequence of PBA Enumerate Programming Mode Enable MRW, wait tMRD_L2, PBA Set ID MRW, wait tPBA_DELAY, Exit PBA Enumerate Programming Mode MRW and, finally, wait until tMRD_L2 is satisfied. At this point, the host may stop driving DQ and DQS_t/DQS_c or change the DQ value to enumerate the next buffer and begin the sequence again.

During this sequence, in the period from the PBA Set ID MRW command cycle to the end of tPBA_DELAY, the buffer will sample the DQ value. Only the buffer which samples its DQ0 bit LOW or its DQ4 bit LOW will enumerate itself with the ID. Data Buffers which sample both the DQ0 bit HIGH AND DQ4 HIGH will retain their previous enumeration ID.

An example of PBA Enumerate Sequence B is as follows:

1. All buffers default to ID=15.
2. The host sends an MRW to the Select ID Control Word with a 15 to select all devices (if not already set that way).
3. The host begins toggling DQS_t and DQS_c.
4. The hosts drives a 0 onto the DQ signals of the buffer that it desires to enumerate with an ID of 0. The host drives 1s on all other DQ signals.
5. The host sends an MRW to the Enumerate Enable Control Word to enable PBA Enumerating Programming mode.
6. The host sends an MRW to the Enumerate ID Control Word with an ID of 0000.
7. The host sends an MRW to the Enumerate Enable Control Word to Disable PBA mode.
8. The host repeats steps 4-7 with IDs of 0001 through 0100 to enumerate the remaining 4 buffers, driving their DQ signals LOW on the appropriate command.
9. The host stops driving DQ and DQS_t/DQS_c.
10. All buffers are uniquely enumerated.

7.3.3 PBA Enumerate Cases

For the “don’t enumerate” case where the DB ignores the PBA Enumerate ID MRW command in the PBA Enumerate Programming Mode, the DQS_t/DQS_c and DQ signals may be high (driven or due to RTT_PARK termination) prior to sending the MRW command to enter PBA Enumerate Programming Mode. After entering PBA Enumerate Programming Mode, the DQS and DQ signals must remain high (driven or due to RTT_PARK termination) until exiting PBA Enumerate Programming Mode. Holding the signals high will ensure that this Data Buffer is never set to a PBA Enumerate ID other than the default setting of 0xFh (15). Refer to Table 32 below for a complete list of notes and cases.

Table 32 — PBA Enumerate Results

DQS[1:0]_t/DQS[1:0]_c	DQ0/DQ4	PBA Enumerate Result	Notes
Toggling	Low - “0”	Enumerate	1
Toggling	High - “1”	Don’t Enumerate	
High/High	Low - “0”	Unknown	2
High/High	High - “1”	Don’t Enumerate	3
High/Low, Low/High	Valid	Don’t Enumerate	

Note 1: The DB will enumerate if either DQ0 or DQ4 is sampled low.
Note 2: DQS_t/DQS_c are differential signals and small amounts of noise could appear as “toggling”, resulting in “Unknown” PBA Enumerate Results.
Note 3: The expected usage case where the DQS signals are High is to have the DQs held High as well.

7.4 PBA Select ID Operation

Once the PBA Enumerate ID's have been programmed in all the Data Buffers, the execution of future MRW. commands depend on the value of the PBA Select ID. If the PBA Select ID is set to 1111B, all Data Buffers will execute the command. For all other values of the select ID, only a buffer enumerated to the same ID as the select ID will respond to the MRW command. An MRW to the PBA Buffer Select ID Control Word will always be executed in all buffers regardless of the current Select ID.

As an example, the following sequence could be used to program unique MR fields per device:

1. Send MRW with 'PBA Select ID' opcode, with encoding 0000 included in the opcode.
2. Send MRW's for field settings specific to Device 0000. This can be any number of MRW's.
3. Send MRW with 'PBA Select ID' opcode, with encoding 0001 included in the opcode.
4. Send MRW's for field settings specific to Device 0001. This can be any number of MRW's.
5. Repeat for any number of devices.
6. Send MRW with 'PBA Select ID' opcode, with encoding 1111 included in the opcode to enable all Data Buffers to execute all MRW commands.

The following timing diagram shows an example sequencing of the programming of the PBA Select ID and MRW command.

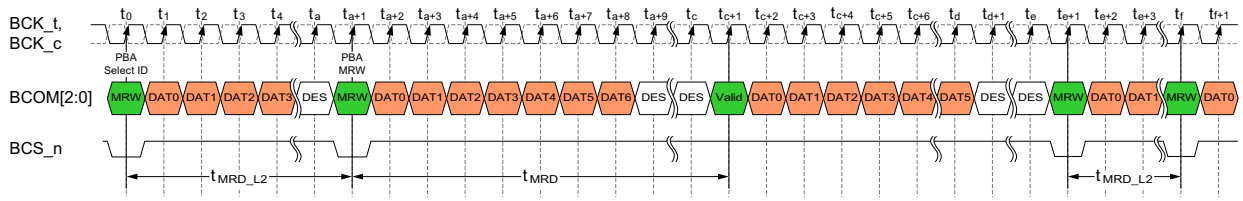


Figure 57 — PBA Access after ID has been programmed

7.5 Dual Frequency Support

The DDR5 data buffer supports operation at a second, i.e. lower than nominal, frequency as a means to save RCD/DB and DRAM power when the memory bandwidth demand allows. To enable fast frequency switching without the need for retraining every time the frequency is changed, the DDR5DB01 can be trained at two, or more, different frequencies at boot up time. When only two frequencies need to be supported, the DDR5DB01 can retain register settings associated with each of the two frequencies. The two sets of DB registers are listed in Table 33. The DB hardware will take care of updating any other frequency-dependent internal settings in each frequency context as needed. In cases where more than two frequencies of operation are necessary, DB training information will need to be stored in memory space available to the host controller for this purpose since the DDR5DB01 device only contains two sets of frequency context registers.

Table 33 — Control Words Duplicated for Frequency Context Support

Register	Description
RW86	DQS RTT Park Termination Control Word
RW87	Host Interface DQ RTT Termination Control Word
RW88	Host Interface DQ RTT NOM Termination Control Word
RW8A	Host Interface DQ Driver Control Word
RW8B	DRAM Interface MDQ Driver Control Word
RW8C	MDQS and MDQ Park Termination Control Word
RW8F	Host Interface Read DQS Offset Timing Control Word
RWA0	DFE Control Word Control Word
RW B0[0]	DRAM t_{DQS2DQ} tracking mode selection
PG[1:0]RWE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable
PG[1:0]RWE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling
PG[1:0]RWE2	Lower Nibble DRAM Interface Receive Enable training control
PG[1:0]RWE3	Upper Nibble DRAM Interface Receive Enable training control
PG[1:0]RWE4	Lower Nibble MDQS Read delay control
PG[1:0]RWE5	Upper Nibble MDQS Read delay control
PG[1:0]RWE6	Lower Nibble MDQ Write Baseline delay control
PG[1:0]RWE7	Upper Nibble MDQ Write Baseline delay control
PG[1:0]RWE8	Lower Nibble DRAM Interface Write Leveling control
PG[1:0]RWE9	Upper Nibble DRAM Interface Write Leveling control
PG[1:0]RW[ED:EA]	MDQ0/4, MDQ1/5, MDQ2/6, MDQ3/7 - Read Delay control
PG[1:0]RW[F1:EE]	MDQ0/4, MDQ1/5, MDQ2/6, MDQ3/7 - Write Delay control
PG[2]RW[E7:E0]	Host DQ Vref
PG[2]RW[F1:F0]	DRAM MDQ Vref
PG[2] RWFA	BCOM Vref
PG[5:4]RW[E0, E8, F0, F8]	DQ[7:0] Receiver DFE Gain Offset
PG[5:4]RW[E1, E9, F1, F9]	DQ[7:0] Receiver DFE Tap 1 Coefficients
PG[5:4]RW[E2, EA, F2, FA]	DQ[7:0] Receiver DFE Tap 2 Coefficients
PG[5:4]RW[E3, EB, F3, FB]	DQ[7:0] Receiver DFE Tap 3 Coefficient
PG[5:4]RW[E4, EC, F4, FC]	DQ[7:0] Receiver DFE Tap 4 Coefficients
PG[A]RW[EF:E8]	Initial DRAM DQS Clock Tree Delay
PG[A]RW[FF:F8]	Current DRAM DQS Clock Tree Delay .

Switching between the two frequency contexts is achieved by writing to control word RW84. RW84[6] = 0 selects the default Frequency Context 1 while RW84[6] = 1 selects Frequency Context 2. Changing the setting in RW84[6] by itself only affects which copy of frequency dependent registers responds to MRW writes and MRR reads. However, when RW84[6] is different from the value it had in the previous Exit from Clock Stop event, the new settings any updates in RW84[3:0], RW85, and the dual-context registers listed in Table 33 will not be applied internally in the DB until after the DB and DRAMs have entered and exited Self Refresh with Clock Stop mode. The DB will use the value of RW84[6] at the time of Exit from Self Refresh with Clock Stop to determine which context to switch to. A context switch only occurs when the value of RW84[6] is different from the value it had in the previous Exit from Self Refresh with Clock Stop event.

7.5.1 Input Clock Frequency Change

Once the DDR5DB01 is initialized, the DDR5DB01 requires the clock to be stable during almost all states of normal operation. This means that, once the clock frequency has been set and is in the stable state, the clock period must not deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only by going through Self Refresh with Clock Stop power down mode. The sequence must allow the host controller to update the frequency dependent registers in the background during normal operation. The sequence of steps for an input frequency change to an LRDIMM is outlined below.

1. Set RW05[6] in RCD space to choose a frequency context different from the current one. At the same time update the Frequency Information settings for the next operating speed in RW05[3:0]. These updates will only be applied internally after the RCD exits from Self Refresh with Clock Stop.
2. Set RW84[6] in DB space to choose a frequency context different from the current one. At the same time, update the Frequency Information settings for the next operating speed in RW84[3:0]. These updates will only be applied internally after the DB exits from Self Refresh with Clock Stop.
3. Write Fine Granularity Frequency information in RCD space for the next operating speed in RW06. The new setting will only be applied internally after the RCD exits from Self Refresh with Clock Stop.
4. Write Fine Granularity Frequency information in DB space for the next operating speed in RW85. The new setting will only be applied internally after the DB exits from Self Refresh with Clock Stop.
5. Set new values for the frequency specific registers listed in Table 33—as well as the RCD frequency specific settings—in the background as needed during normal operation. These changes will only be applied internally after the DB and RCD exit from Self Refresh with Clock Stop mode.
6. Go through Entry and Exit from Self Refresh with Clock Stop. The DB and the RCD will apply the new settings upon Exit from Self Refresh with Clock Stop.

With the exception of Self Refresh Entry, normal DRAM traffic and operations are supported intermingled with Steps 3, 4, and 5 of the transition sequence defined above.

8 Strobe and Data Training Support Features

The DDR5DB01 does not contain self-sufficient training state machines for calibrating its timing control settings. It will instead depend on the host controller to get the timing control registers programmed with the appropriate settings that will allow the DB to work in the DDR5 LRDIMM environment. To enable the host controller in performing the training procedure in an efficient and reliable manner, the data buffer provides various Strobe and Data training support features. The following sections describe such training support features in the DDR5DB01. The Data Path training modes in Table 34, “Summary of Training Support Features and Functions” and the DFE training are performed with a Fixed BL16.

Table 34 below provides a summary description of the various Strobe and Data training support functions and features in the DDR5DB01 for the Data Bus Training.

Table 34 — Summary of Training Support Features and Functions

Interface	Training Step	Symbol	Direction	Features
DRAM Interface	MDQS Receive Enable	MRE	DRAM to DB	Receiver enable sampling of MDQS pins Output sample driven out on host interface DQ pins
	MDQS Read Delay	MRD[1]	DRAM to DB	Phase adjustment for MDQS input delay using Read Training pattern from DRAM. Data Comparator output sample driven out on host interface DQ pins
	DRAM Write Leveling	DWL	DB to DRAM	Transmits MDQS according to write commands generated from host. Receives DQ feedback from DRAM and sends to host.
	MDQ Write Delay	MWD[1]	DB to DRAM	Phase adjustment for MDQ output delay using the Data Buffer *Training Pattern Generator* for writes to the DRAM and read comparison. Data Comparator output sample driven out on host interface DQ pins
Host Interface	Host Write Leveling	HWL	Host to DB	The Data Buffer samples the internal WL Pulse with the host transmitted strobe pattern and sends the sampled value back to the host on the DQ signals.
	Host Interface Read	HIR[1]	DB to Host	The Data Buffer generates the Training Pattern in response to MRR’s and returns to host while DRAM interface is disabled.
	Host Pre-Amble	HPA	DB to Host	The Data Buffer drives host-side strobes differentially LOW other than when driving strobes in response to the MRR to access the Training Pattern. In this mode, only a single toggle is supported in the preamble (similar to 1tCK preamble setting.)

1. CRC modes must be disabled.

The DDR5DB01 provides separate timing control registers for the lower and upper nibbles. However, there is only one Buffer Training Mode Control Word so both nibbles are always in the same training mode. Table 35 below provides an overview of the buffer control words (RW) that are involved in the timing control and timing training features of the DDR5DB01.

Table 35 — Summary of Strobe and Data Timing and Training Control Words

Page	RWxx	Description	Scope
Direct	RW83	[M]DQS, [M]DQ Training Modes	Select Training mode
	RW94	Internal Receive Enable Offset Coarse Status	Read only Status
	RW95	Internal Receive Enable Offset Fine Lower Nibble Status	Read only Status
	RW96	Internal Receive Enable Offset Fine Upper Nibble Status	Read only Status
	RW97	Buffer Training Configuration Control Word	
	RW98	Buffer Training Status Word	
PG[1:0]	RWE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable	Control per rank/per nibble
	RWE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling	
	RWE2	Lower nibble DRAM interface receive enable training control	MRE phase and cycle control per rank
	RWE3	Upper nibble DRAM interface receive enable training control	
	RWE4	Lower nibble MDQS Read delay control	Input control per rank
	RWE5	Upper nibble MDQS Read delay control	
	RWE6	Lower nibble MDQ Write Baseline delay control	Output control per rank
	RWE7	Upper Nibble MDQ Write Baseline Delay	
	RWE8	Lower nibble DRAM interface write leveling control	Write leveling phase and cycle control per rank
	RWE9	Upper nibble DRAM interface write leveling control	
	RWEA	MDQ0/4-Read delay control	Input control per rank/per bit
	RWEB	MDQ1/5-Read delay control	
	RWEC	MDQ2/6-Read delay control	
	RWED	MDQ3/7-Read delay control	
	RWEE	MDQ0/4-MDQS Write delay control	Output control per rank/per bit
	RWEF	MDQ1/5-MDQS Write delay control	
	RWF0	MDQ2/6-MDQS Write delay control	
	RWF1	MDQ3/7-MDQS Write delay control	

8.1 MRE: DRAM Interface MDQS Receive Enable Training Mode

The problem is how to find the optimal settings that will allow the data buffer to work reliably in the LRDIMM environment. To help the host controller solve this problem, the data buffer provides a DRAM interface receive enable phase training mode. In this training mode, the data buffer uses a group of programmable delay elements and sampling circuits to capture the MDQSx_t/MDQSx_c signals received from the DRAMs. This is accomplished by the rising edge of the DB Receive Enable signal sampling the MDQSx_t/MDQSx_c signals and sending this sampled value to the host via the DQ signals per nibble.

This training mode has been defined so that it can be performed before any training has taken place between the host controller and the DDR5DB01.

The DB will support Per-Rank, Upper and Lower Nibble - Receive Enable cycle adjustment = -4, -3, -2, -1, 0, 1, 2, 3, 4 (signed magnitude) as defined in PG[1:0]RW[E0].

The DB will support Per-Rank, Upper and Lower Nibble - Receive Enable phase adjustment (6 bits, 1/64th tCK granularity) as defined in PG[1:0]RW[E3:E2].

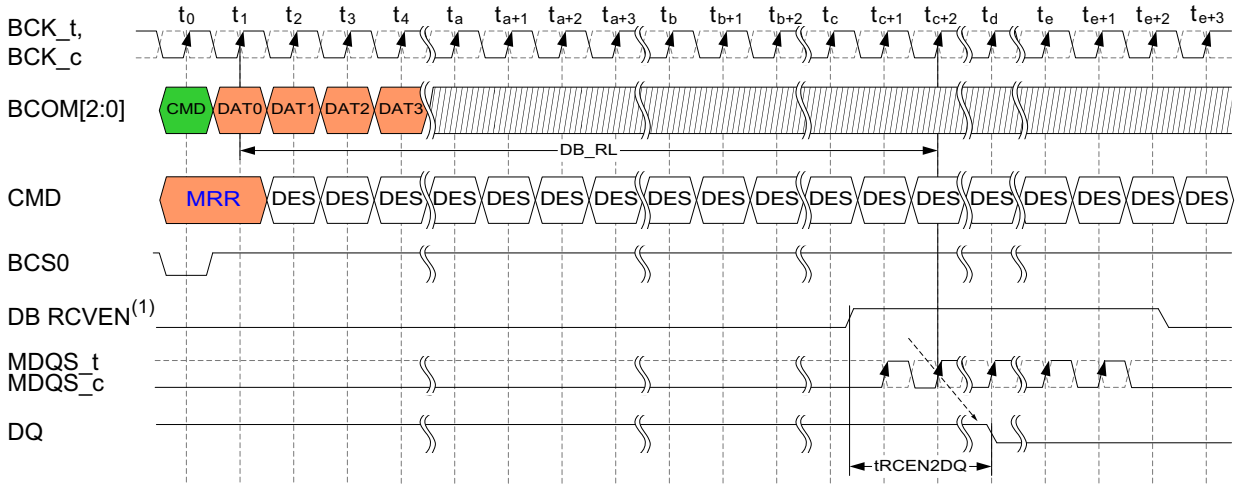
The DB will also include read-only register for the internal Receive Enable offset that is applied by the DB after exiting the MRE training mode as defined in RW[96:94].

The DRAM interface receive enable timing selection is controlled in steps of 1/64 * t_{CK} by PG[1:0]RW[E3:E2]. The host controller has the ability of setting the values for this parameter by means of MRW Write commands. When the Receive Enable training control bits PG[1:0]RW[E3, E2, E0] are all set to zero delay (default settings), the rising edge of the input-referred receive enable is aligned to a rising edge BCK that corresponds to a read latency of DB_RL. In this training mode, the output of each MDQSx_t/MDQSx_c sampling circuit is driven onto the four host interface DQ pins corresponding to each nibble. In this training mode, the DQS_t/DQS_c inputs and outputs at the host interface are disabled.

To perform receive enable phase training, the host will first enable the MDQS Receive Enable Training mode in RW83. After that, if the DRAMs have already been initialized, the host will send a sequence of MRR commands to the DRAMs to access the Read Training Pattern. This may be any number of consecutive or non-consecutive DRAM MRR commands. The DRAM will be in Preamble Training Mode, causing the MDQSx_t/MDQSx_c inputs of the data buffer to be differentially LOW other than when the DRAM responds with a read burst due to the MRR command. The DRAM will generate a train of pulses in the MDQSx_t/MDQSx_c inputs of the data buffer according to the number of MRR commands sent by the host. The data buffer will use the RANK_ID field in the MRR Command sequences received through the BCOM[2:0] interface to select which receive enable timing control register will be used during training. The DB will use PG[0]RW[E3:E2] for Rank 0, and PG[1]RW[E3:E2] for Rank 1. Using the output of the sampling circuits available on the DQ pins, the host controller will be able to decide if it needs to increase or decrease the receive enable phase control settings in the data buffer by means of MRW commands. The objective is to find the end of the DRAM read preamble, i.e. first effective rising edge of MDQS_t. At this time, the output of the sampling circuits will change from LOW to HIGH. With this method, the host controller will be able to align the rising edge of the internal receive enable to the first effective rising edge of the incoming MDQSx_t/MDQSx_c signals. The host will use combinations of cycle and phase settings to determine the first effective rising strobe edge of the read burst. The host may send any number of back-to-back DRAM MRR commands to accomplish this step. The DB will sample only during the rising edge of the Receive Enable signal and will hold this sample on the DQ signals to the host until the next Receive Enable rising edge. For back-to-back DRAM-space MRRs, there is only one read enable rising edge at the beginning of the contiguous burst. The DB will apply an internal offset adjustment after training to account for correct centering within the programmed preamble timing. The final offset will take effect once the host exits the MRE training mode. The host must program the correct preamble timing prior to execution of the training sequence.

The following diagram shows an example of the DB Receive Enable signal sampling the MDQSx_t/MDQSx_c signal. The DRAM has the preamble training mode enabled.

On the Host interface, while in MRE training mode, the DB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination (DQ_RTT_PARK, DQ_RTT_NOM_WR, DQ_RTT_NOM_RD, DQ_RTT_WR). Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS_RTT_PARK continuously on DQS if enabled.



1. DB RCVEN is High when the DB input receivers are enabled for sampling the MDQS_t/MDQS_c strobe signals from DRAM device.

Figure 58 — MRE Timing Diagram

The data buffer provides only a single Read FIFO fall-through time for both ranks and for correct operation this delay cannot change. Any potential adjustments to this data buffer Read FIFO fall-through time have to be performed prior to this training step. The host is responsible for establishing and maintaining its own unique read enable timing for each rank.

The DRAM interface receive enable timing established in this training step is also used by the DB for the driver enable for the DQ/DQS outputs for Read commands (by adding an offset that corresponds to the Read FIFO flow-through time).

To exit this training mode, the host controller can resume normal operation or enable other training modes with an MRW to RW83.

8.2 MRD: MDQS Read Delay Training Mode

For the DRAM-to-DB read training, the MDQS delay adjustments are performed in the data buffer so that it can correctly sample the data driven by the DRAM. The data buffer provides data pattern control words that are programmed with the expected read data pattern from the DRAM and the results of the comparison are provided on the data buffer host interface.

To perform DRAM-to-DB read training, the host will first enable the MDQS read delay (MRD) training mode in the Training Mode Control Word RW83.

The delay of the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) during read transactions is selected by buffer control word PG[1:0]RW[E5:E4] for upper and lower nibble respectively. The nominal setting for PG[1:0]RW[E5:E4] is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including Host Interface Read Training, when non-default settings are written into PG[1:0]RW[E5:E4].

While in MRD training mode, the DB treats any DRAM-space MRR as a short MRR. A sequence of short MRR may be used by the host to generate back-to-back BL16 read transfers from the DRAM to the DB.

In this training mode, the data buffer uses a data pattern comparator to determine if the read data from the DRAMs matches an expected result. The expected data pattern values are stored in Read Pattern 0 and Read Pattern 1 the control words PG[8]RWE3 and PG[8]RWE4, or the expected data pattern is generated by LFSR pattern generators. There is only one data comparator per data buffer, with a selected per-MDQ comparison results. The output of the data comparator is driven onto the host connector interface on DQ pins.

- If the data pattern is matched, the DQ pins drive HIGH until the next comparison takes place or until the training mode is disabled.
- If the data pattern is not matched, the DQ pins drive LOW until the next comparison takes place or until the training mode is disabled. RW97[3] selects whether all four DQ bits within a nibble are driven LOW see Table 38 for functional description.

The control words PG[8]RWE2 through PG[8]RWE6 are used to configure these pattern generators. When the LFSR pattern generators are enabled, the host may send a long sequence of MRR commands for continuous comparison to the read training pattern. The DQ feedback to the host must indicate a match '1' or a mis-compare '0' after each read burst of each Read command has completed. See Table 38. The comparison can also be configured to look at specific UI's within the read burst. RW97 is used to configure the UI filtering for the comparison.

When using a Serial pattern, PG[8]RWE3 will contain the expected first 8 UI for all MDQ signals. PG[8]RWE4 will contain the expected last 8 UI for all MDQ signal. The Serial pattern can also be inverted per MDQ lane, PG[8]RWE5 indicates which DQ signals are inverted. These settings should match the DRAM configuration for the Read Training Pattern. The DB shall support snooping of the DRAM MR settings for the Read Training Pattern configuration.

In addition to driving the DQ pins, status for the pattern comparison is also provided in the Buffer Training Status word RW98. The status provided in RW98 can be modified by the Buffer Training Configuration control word RW97, to provide status of a mis-compare with or without UI filtering applied. The status in RW98 is always per DQ lane.

On the Host interface, while in MRD training mode, the DB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination (DQ_RTT_PARK, DQ_RTT_NOM_WR, DQ_RTT_NOM_RD, DQ_RTT_WR). Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS_RTT_PARK continuously on DQS if enabled. CRC modes must be disabled.

The DDR5DB01 is required to support fine adjustment of the phase of individual bit lanes relative to the baseline MDQS. For this purpose, the host controller can utilize the per lane MDQS-MDQ read delay control words PG[0]RWEA controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, PG[0]RWEB controls the phase bits MDQ1 and MDQ5 for Rank 0, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3/64 t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQS delay in PG [1:0] RW[E5:E4] for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQS delay in PG [1:0] RW[E5:E4] for the entire nibble.

To exit this training mode, the host controller can resume normal operation or enable other training modes with an MRW to RW83.

8.2.1 UI filtering and Sticky Status Summary Table

Table 36 — UI filtering and Sticky Status Summary Table

Long-RD Pattern Sticky Status	Status Format	UI Filtering	DQ Output (HIGH = No error, LOW= Error
Disabled	Per Transaction	Disabled (default)	For each BL16 RD/MRR command, an error during the burst on any UI of any bit lane of a nibble will set all DQ bits of the nibble LOW. When set LOW, this level is held until the next BL16 RD/MRR command or until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
		Enabled	For each BL16 RD/MRR command, an error during the burst on the selected UI of any bit lane of the burst will set all DQ bits of the nibble LOW. When set LOW, this level is held until the next BL16 RD/MRR command or until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
	Per Bit Lane (default)	Disabled (default)	For each BL16 RD/MRR command, an error on any UI of bit lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the next BL16 RD/MRR command or until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
		Enabled	For each BL16 RD/MRR command, an error on the selected UI of bit Lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the next BL16 RD/MRR command or until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
Enabled[1] (default)	Per Transaction	Disabled (default)	For each BL16 RD/MRR command, an error during the burst on any UI of any bit lane of a nibble will set all DQ bits of the nibble LOW. When set LOW, this level is held until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
		Enabled	For each BL16 RD/MRR command, an error during the burst on the selected UI of any bit lane of a nibble will set all DQ bits of the nibble LOW. When set LOW, this level is held until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
	Per Bit Lane (default)	Disabled (default)	For each BL16 RD/MRR command, an error on any UI of bit lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.
		Enabled	For each BL16 RD/MRR command, an error on the selected UI of bit Lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the Clear Feedback Status bit in RW97[0] is asserted or DB reset.

1. After exiting the training mode (i.e., MRD or MWD), the feedback status will be removed from the DQ pins to support Read/Write normal operation. The DDR5DB01 hardware may clear the sticky status, but the host is required to set the Clear Feedback Status bit in RW97[0] to guarantee that the sticky status will not be carried over into a new (MRD or MWD) training mode entry.

8.3 MWD: DB-to-DRAM Write Delay Training Mode

For the DB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The host-to-DB data path has not been trained at this time so the data that is written to the DRAM comes from a pattern generator that is configured with DB MRW commands through the DDR5 register via the BCOM bus. Since the DB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to DB read training has already been finished.

The host will ensure that MWD training is only performed with delay values in PG[A] cleared to zero.

To perform DB-to-DRAM write training, the host will first enable the MDQ-MDQS write delay (MWD) training mode in the Training Mode Control Word (RW83). The DB will use the pattern generation capability for MWD training. The configuration state for the patterns is the same for the read comparison pattern and the write pattern. Therefore, there is no need to duplicate these configuration registers. The logic to generate the patterns must enable independent state transitions for write pattern versus read comparison pattern, due to the timing difference for when these patterns are used.

When the LFSR pattern is enabled, the current state for each LFSR can be read from WRITE LFSR registers RW[9F:9E] and READ LFSR registers RW[9D:9C]. MWD mode must first be exited to read these registers. While the DB is in the MWD training mode, the host sends write commands to an arbitrary DRAM location. The host must not drive DQ during MWD training since the DB will be continuously driving training result status. The data for these Write commands come from the DB write pattern generators.

To check whether the writes were successful, the host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the read comparison pattern. The feedback on the DQ pins to the host will indicate a mis-compare in the same way as defined for the MRD training mode. All configuration settings for per-bit sticky error status or per transaction error events are the same as for the MRD training mode. The UI filtering and Training Status word are also the same. The phase relationship between the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words PG[1:0]RWE6 and PG[1:0]RWE7 for lower and upper nibble respectively. The DDR5DB01 uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively. The DDR5DB01 also uses this rank information to exercise the appropriate MDQ-MDQS settings.

Due to the unmatched receiver in the DRAM, the range of the MDQ signal timings must account for the unmatched range. DDR5 DB accounts for this by extending the MDQ to MDQS_t phase delay range to be defined as - tCK/2 to (3+31/64) tCK in 1/64 increments.

On the Host interface, while in MWD training mode, the DB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination (DQ_RTT_PARK, DQ_RTT_NOM_WR, DQ_RTT_NOM_RD, DQ_RTT_WR). Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS_RTT_PARK continuously on DQS if enabled. CRC modes must be disabled.

For DDR5 data rates, fine adjustment of the phase of individual MDQ bit lanes relative to MDQS are required. For this purpose, the host controller can utilize the per lane MDQ-MDQS write delay control words through PG[1:0]RWEE controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively, PG[1:0]RWEF controls the phase bits MDQ1 and MDQ5, and so on. Since all bits within are nibble a generally aligned by routing, only a small range of +/- [3/64]t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in PG[1:0]RW[E7:E6] for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in PG[1:0]RW[E7:E6] for the entire nibble.

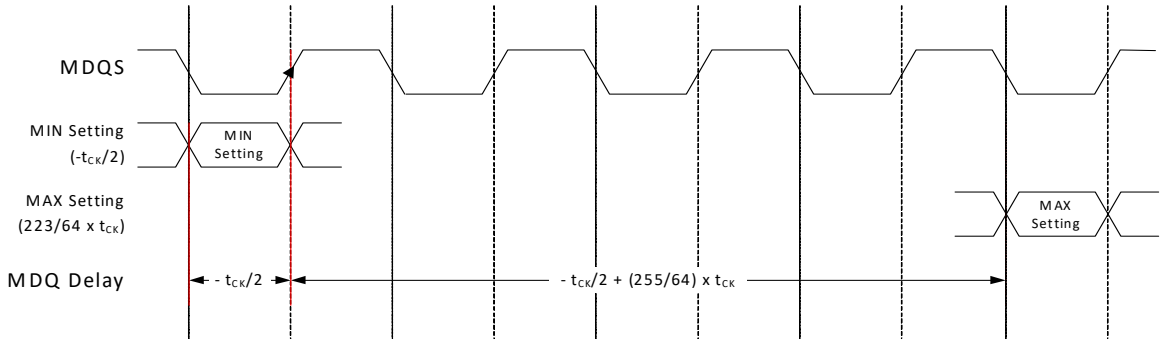


Figure 59 — MDQ Write Baseline Delay

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with an MRW to RW83.

8.4 DWL: DRAM Write Leveling Training Mode

The DDR5DB01 supports both DRAM write leveling (WL) training modes: external WL training and internal WL training with the same DRAM-interface write leveling (DWL) training mode. DWL training mode is selected via RW83.

For each nibble, the Data Buffer must have an adjustable delay setting per rank to align the first effective rising edge of its differential MDQS with the timing at the DRAM receiver. This adjustable delay in the data buffer is programmed using PG[1:0]RWE1 and PG[1:0]RW[E9:E8] control words.

When the Data Buffer enters DWL training mode it drives both MDQS differentially LOW (MDQSy_t = LOW MDQSy_c = HIGH) at all times except when it is generating a training pattern. When a target WRITE command is received, the Data Buffer generates the training pattern which is the preamble and the first functional MDQS pulse, see Figure 60. The pre-amble format is snooped by the Data Buffer and stored in PG[8]RWE1. The minimum tCCD (Command to Command Delay time) between write commands is 8tCK.

The rising edge of the first functional MDQS pulse occurs DB_WL(Rx, Ny) after the DAT0 cycle of a WRITE command sequence, where Rx represents rank x and Ny represents nibble y. Rank x is the rank being trained and is selected by the Rank_ID field in the DAT0 cycle of the write command sequence.

In DWL for each nibble, the Data Buffer forwards the DRAM's WL response asynchronously from its respective MDQ input pins to their corresponding DQ output pins so that the host can read the response.

On the Host interface, while in DWL training mode, the Data Buffer continuously enables its DQ drivers, and disable its DQ receivers and DQ termination (DQ_RTT_PARK, DQ_RTT_NOM_WR, DQ_RTT_NOM_RD, DQ_RTT_WR). Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS_RTT_PARK continuously on DQS if enabled.

On the DRAM Interface, while in DWL training mode, the Data Buffer disables its MDQ drivers, and it continuously enables is MDQ receivers. It continuously applies MDQ_RTT_PARK if enabled. The DB operates its MDQS drivers as described above. It may disable its MDQS receivers. It disables MDQS_RTT_PARK.

The Data Buffer must continue to process MRWs normally in DWL mode to allow the host to adjust its related delay registers. The host will only send target write commands to the DB, and non-target write commands are illegal.

Figure 60 shows the sequence of events for Data Buffer DWL training. The DRAM requires MDQS to be driven differentially LOW before it enters WL training mode. Therefore, the Data Buffer must be placed in DWL training mode prior to placing the DRAM in either of the WL training modes. Upon entering DWL mode the DB will begin driving MDQS differentially LOW, and it will apply all of its other IO states mentioned previously. When the Data Buffer receives a WRITE command, it generates the pre-amble and the first function MDQS pulse. When the rising edge of the first functional MDQS pulse samples the DRAM's internal WL pulse, the DRAM returns the sampled result after tWLO on all of its DQ outputs. Once the DB receives the sample result it propagates this information to its respective DQ outputs tTPM_DQD later.

The Data Buffer's output mismatch uncertainty between its DQ while in DWL training mode is DTPM_DQ. Therefore, the host must expect an accumulative mismatch uncertainty of DRAM and Data Buffer.

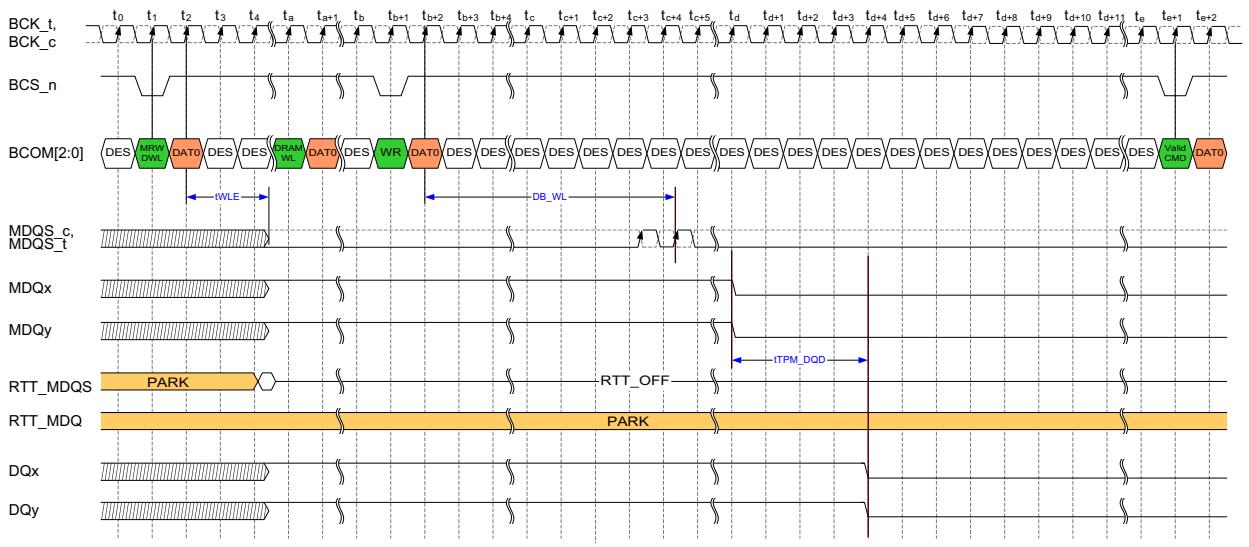


Figure 60 — DWL

8.5 HWL: Host Interface Write Leveling Training Mode

The Data Buffer supports a host-interface write leveling (HWL) training mode that is similar to the DRAM's external WL training mode. For each nibble y, prior to placing the DB in HWL training mode the host is required drive DQS differentially LOW (DQSy_t = LOW, DQSy_c = HIGH).

Once the host places the Data Buffer in HWL training mode, the host is required to drive DQS differentially LOW except when it generates a training pattern. For each write command, the host generates only the preamble and the first functional pulse on DQS. The preamble pattern depends on the selected preamble mode.

When the Data Buffer is in HWL training mode, for each target write command the Data Buffer always generates a one-cycle wide pulse on each of its per-nibble internal WL pulse signals. The rising edge of each WL pulse is aligned with the internal WL timing point that is DB_WL(Rx, Ny) - tPDM_WR after the DAT0 cycle of the write command, where Rx represents rank x and Ny represents nibble y. Rank x is the rank being trained and is selected by the Rank_ID field in the DAT0 cycle of the write command sequence. At all other times, each per-nibble WL pulse signal is LOW.

For nibble-y, the WL pulse signal is sampled by each rising edge of its respective DQS, including any rising edges within the preamble. The DQS burst can arrive any time after the write command. Figure 61 shows the case where the rising edge of the DQS preamble samples the LOW level prior to the WL pulse, and the rising edge of the first functional DQS pulse samples the HIGH level of the WL pulse. The DB asynchronously outputs each sample on the nibble's four DQ outputs after t_{TPM_DQD}. The DB's output mismatch uncertainty between its per-nibble DQ outputs is D_{TPM_DQ}.

While in HWL training mode, the Data Buffer continuously enables its DQ drivers, and it may disable its DQ receivers. It disables DQ termination (DQ_RTT_PARK, DQ_RTT_NOM_WR, DQ_RTT_NOM_RD, DQ_RTT_WR). The Data Buffer disables its DQS drivers, and it must continuously enable its DQS receivers. It applies DQS_RTT_PARK continuously on DQS if enabled. The Data Buffer disables its MDQ drivers and receivers, and applies MDQ_RTT_PARK if enabled. The Data Buffer disables its MDQS drivers and receivers and applies MDQS_RTT_PARK if enabled.

While in HWL training mode, the Data Buffer must continue to process DB-space MRWs normally.

While in HWL training mode, the host will only send targeted Write commands to the DB.

When HWL training has been completed, the host must continue to drive DQS differentially LOW until the DB has completed HWL mode exit.

HWL training mode is selected via RW83.

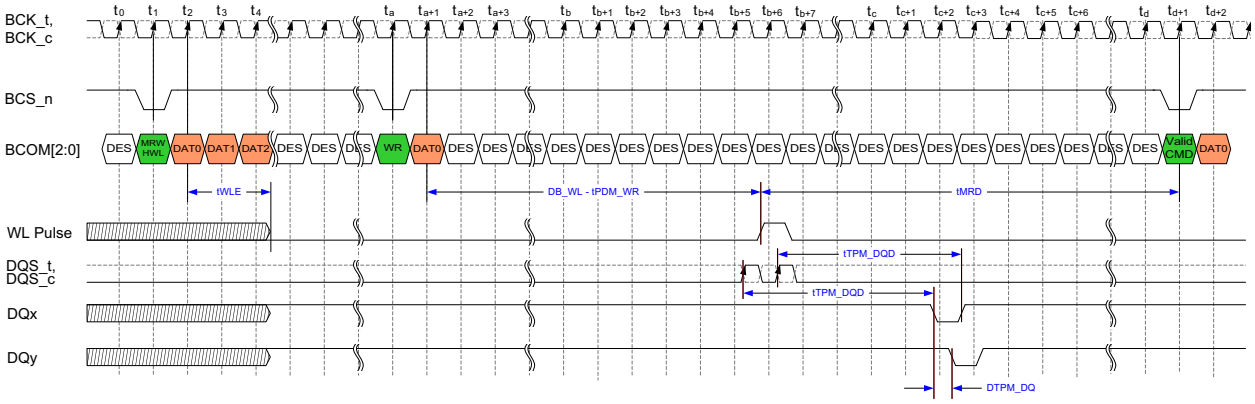


Figure 61 — Host Write Leveling (HWL)

8.6 HIR: Host Interface Read Training Mode

The host performs host-interface read (HIR) training that includes host read enable alignment and host read eye sample alignment. This is done in two phases, initial host read training and final host read training. For initial host read training, the host will use HIR training mode. While in HIR training mode, the DB treats any DB-space MRR as a short MRR and when any DB-space MRR is received it generates a BL16 read burst to the host using its internal read training pattern generator. The read burst timing is determined by the rank ID field in the DAT0 cycle of the DB-space MRR sequence. The host-side read burst for rank-x and nibble-y occurs DB_RL(Rx, Ny) + tPDM_RD after the DAT0 cycle of the DB-space MRR sequence. The MDQS/MDQ receivers remain disabled during the DB-space MRR and ODT will operate normally at RTT_PARK.

For final host training, if the host is using 1N command timing it can keep the DB in its normal operating mode and send DRAM-space MRRs to the DRAM's read training pattern register. For each DRAM-space MRR, the DB performs a normal read from the DRAM.

If the host is using SDR (2N) command timing, it must first place the DB in HIR training mode. While in HIR training mode, the DB treats any DRAM-space MRR as a short MRR and when any DRAM-space MRR is received it performs a normal BL16 read that transfers the read burst from the DRAM to the host. The read burst timing is determined by the rank ID in the DAT0 cycle of the DRAM-space MRR sequence. The host-side read burst for rank-x and nibble-y occurs DB_RL(Rx, Ny) + tPDM_RD after the DAT0 cycle of the DRAM-space MRR sequence. The MDQS/MDQ receivers and ODT operate normally for the reception of the read burst from the DRAM.

When HIR training is performed in SDR (2N) command timing mode, since the DB treats any MRR as a short-MRR in HIR training mode it naturally supports a minimum MRR spacing of 8tCK. Table 37 provides a summary

command processing while in HIR training mode.

Table 37 — HIR Training Mode Command Processing Summary

Command Timing Mode	A DB-space MRR is treated as ...	A DRAM-space MRR is treated as ...	A RD is treated as ...
1N	A 1N short MRR that causes a read from the DB's read training pattern generator and advances the generator's LFSRs	A 1N short MRR that is processed as a normal read from the DRAM	A 1N RD that is processed as a normal read from the DRAM
2N	A 2N short MRR that causes a read from the DB's read training pattern generator and advances the generator's LFSRs	A 2N short MRR that is processed as a normal read from the DRAM	A 2N RD that is processed as a normal read from the DRAM.

In HIR training mode, when the host applies a 2tCK BCS_n assertion during any MRR the DB will not execute the MRR, but it will automatically use rank-0 timing to apply RTT_NOM_RD on DQ if enabled during the burst.

8.7 HPA: Host Preamble Training Mode

Host preamble training supports read leveling of the host receiver timings. This mode is intended to be used during HIR training mode that supports MRR or Read transactions. Host preamble training changes the read strobe behavior such that the strobes are always driven by the Data Buffer, and only toggle during a 1tCK preamble plus the actual burst of the read data. There is no toggle during post-amble time. This mode enables the host to detect the timing of when the first data and associated strobe is returned after a read command.

The Data Buffer enters and exits Host Preamble Training Mode via MRW to RW83.

8.7.1 Host Preamble Training Mode Operation

Once the Data Buffer is placed in Host Preamble Training Mode, the only data transactions supported are MRR or Read commands. All non-data commands, such as MRW, are still supported in this mode. Once Host Preamble Training is enabled, the device will drive DQS_t LOW and DQS_c HIGH within tSDOn and remain at these levels until an MRR or Read command is issued.

During Host Preamble Training Mode, the DQS preamble provided during normal operation will not be driven by the Data Buffer. Once the MRR or Read command is issued, the Data Buffer will drive a 1tCK preamble plus the actual DQS_t/DQS_c strobe burst for the read data. In response to DB-Space MRR command when HIR training mode is enabled, the DB device must drive the DQ pattern as per the Read Training Pattern configuration. In response to Read command or DRAM-Space MRR command when HIR training mode is either enabled or disabled, the DB device must drive the DQ pattern received from the DRAM. The MRR or Read commands may be sequenced to enable back-to-back bursts on the DQ bus. While in HPA mode, the host will not send non-target read and MRR commands, because DQS will be driven LOW during idle times.

Host Preamble Training Mode is exited within tSDOff after setting RW83.

The following figure shows the timing for the strobe driven differential LOW after Host Preamble Training Mode is enabled, and also shows the strobe timings including a 1tCK Preamble, after an MRR command to access the read training pattern:

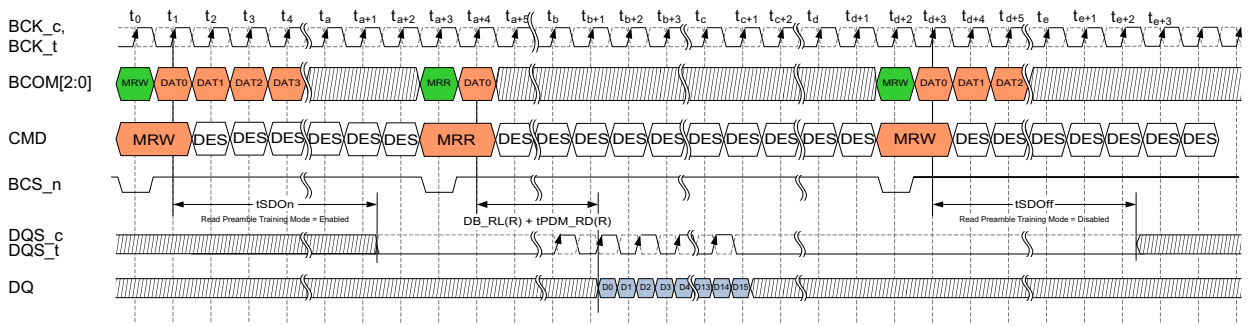


Figure 62 — Timing diagram for Host Preamble Training Mode entry, read training pattern access and Host Preamble Training Mode Exit

8.8 Data Buffer Training Pattern Generator

The Data Buffer includes two training pattern generators to support the HIR, MRD, and MWD training modes. One pattern generator is used for reads and one pattern generator is used for writes. The read training pattern generator is enabled when the Data Buffer is in HIR, MRD, or MWD training mode. The write training pattern generator is only enabled when the Data Buffer is in MWD training mode. While in HIR training mode, the DB will handle DB-space MRRs as a short-MRR. When the Data Buffer receives any DB-space MRR it generates a BL16 read burst with the full BL16 data pattern sourced from its read pattern generator. Only a BL16 read burst type is supported. When in MRD or MWD training modes, the read training pattern generator is used to compare to the read data being returned from the DRAM. The write training pattern generator is used to send the write pattern to the DRAM when in MWD training mode.

8.8.1 Pattern Control

The read and write training pattern generators support two primary generation format modes. A Serial format and LFSR format. The LFSR format has two secondary pattern options: the LFSR pattern or a high-frequency clock pattern. The format and pattern option are selected via the PG[8]RWE2 register as summarized in Table 38.

When a DRAM-space Mode Register Write (MRW) to MR25 occurs, the op-codes are snooped by the Data Buffer and MR25[2:0] are copied into the DB-space register PG[8]RWE2. This register is reset to its default values during power-up initialization, Reset initialization with Stable Power, and DB reset. In addition to configuring the read training pattern format for HIR training mode, this register also configures the pattern format for the pattern checker used for MRD training mode and the read phase of MWD training mode, and the pattern generator used for the write

phase of MWD.

Table 38 — Read Training Mode Settings

Data Buffer RW	Operating Mode	Bit Description	Snoop Value from DRAM MRW
PG[8]RWE2[0]	Read Training Pattern Format	0 = Serial (default), 1 = LFSR	MR25[0]
PG[8]RWE2[1]	LFSR0 Pattern Option	0 = LFSR (default), 1 = Clock	MR25[1]
PG[8]RWE2[2]	LFSR1 Pattern Option	0 = LFSR (default), 1 = Clock	MR25[2]
PG[8]RWE2[7:3]	Reserved	Reserved	NA
PG[8]RWE3[7:0]	Read Pattern_0[1]	Serial Data_0: UI[7:0] LFSR Seed_0: UI[7:0] Default: 0x5A	MR26[7:0]
PG[8]RWE4[7:0]	Read Pattern_1[2]	Serial Data_1: UI[15:8] LFSR Seed_1: UI[7:0] Default: 0x3C	MR27[7:0]
PG[8]RWE5[7:0]	Read Pattern Invert[3]	0= DQ[x] is not inverted 1= DQ[x] is inverted Default: 0x00	MR28[3:0][4]
PG[8]RWE6[7:0]	Read LFSR Assignment[3]	[x] = 0, DQ[x] is sourced from LFSR0 [x] = 1, DQ[x] is sourced from LFSR1 Default: 0xEE	MR30[3:0][4]
RW9C[7:0]	READ LFSR0 State Monitor (Read Only)	The current state of READ LFSR0	N/A
RW9D[7:0]	READ LFSR1 State Monitor (Read Only)	The current state of READ LFSR1	N/A
RW9E[7:0]	WRITE LFSR0 State Monitor (Read Only)	The current state of WRITE LFSR0	N/A
RW9F[7:0]	WRITE LFSR1 State Monitor (Read Only)	The current state of WRITE LFSR1	N/A

1. The WRITE LFSR0 and READ LFSR0 are initialized with the same seed value of Read Pattern_0.
2. The WRITE LFSR1 and READ LFSR1 are initialized with the same seed value of Read Pattern_1
3. Upper/lower nibble can be written with different code only by direct MRW, and DRAMs need to be configured in PDA mode to support this case.
4. This value gets copied to 7:4 and 3:0

There are two 8-bit pattern generation LFSRs provided for LFSR pattern generation, LFSR0 and LFSR1. Associated with each LFSR is a clock pattern generator, this can be implemented as a single, shared clock-pattern generator.

For LFSR format and the LFSR pattern selected for a particular LFSR, when a DB-space MRR occurs the LFSR changes state. For LFSR format and the clock pattern option selected for a particular LFSR, when a DB-space MRR occurs the LFSR holds its state and the clock pattern generator generates the clock pattern.

Two registers are provided to allow the host to specify the 16-bit fixed pattern for serial format, or the two 8-bit seed values for LFSR format. The PG[8]RWE3 register provides UI[7:0] of the 16-bit fixed pattern for serial format, or

UI[7:0] of LFSR0's 8-bit seed value for LFSR format. This register defaults to 0x5A, and can be written to any value by the host. The PG[8]RWE4 register provides UI[15:8] of the 16-bit fixed pattern for serial format, or UI[7:0] of LFSR1's 8-bit seed value for LFSR format. This register defaults to 0x3C and can be written to any value by the host.

These two registers are reset to their default values under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- BRST_n assertion, when BCOM is '000' or '111'
- Self Refresh with and without Clock Stop
- Power-down entry

In addition to configuring PG[8]RWE[4:3] for HIR training mode, these registers can also be configured as the pattern/seed for the pattern checker used for MRD training mode, the read phase of MWD training mode, and the pattern generator used for the write phase of MWD.

When a DRAM-space MRW to MR26 occurs, it is snooped by the DB and PG[8]RWE3 is loaded with MR26[7:0].

When a DRAM-space MRW to MR27 occurs, it is snooped by the DB and PG[8]RWE4 is loaded with MR27[7:0].

The PG[8]RWE5 register is provided to allow the host to select per-DQ pattern inversion that is applied for either serial format or LFSR format. If PG[8]RWE5[x] = 0 the pattern applied to DQ[x] is not inverted, otherwise if PG[8]RWE5[x] = 1 then the pattern applied to DQ[x] is inverted. This register defaults to 0x00, and it is reset to its default value under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- BRST_n assertion, when BCOM is '000' or '111'
- Self Refresh with and without Clock Stop
- Power-down entry

In addition to configuring the per-DQ pattern inversion for HIR training mode, this register also configures the per-DQ pattern inversion for the pattern checker used for MRD training mode and the read phase of MWD training mode, and the pattern generator used for the write phase of MWD.

When a DRAM-space MRW to MR28 occurs, it is snooped by the DB. Since each DRAM is an x4 device, only MR28[3:0] is valid. All DRAM are programmed with the same value. So, when MR28 is snooped, PG[8]RWE5 is loaded with {MR28[3:0], MR28[3:0]}.

8.8.2 LFSR Functionality and Control

Figure 63 shows an example LFSR topology with its associated clock pattern generator. Each LFSR is an 8-bit Galois LFSR with polynomial $x^8 + x^6 + x^5 + x^4 + 1$. The numbered shifter stages of each LFSR are mapped 1:1 with the bit numbers of its respective pattern/seed register. The output of each LFSR can be assigned to any number of DQ outputs. The PG[8]RWE6 register allows the host to select the per-DQ assignment between the two LFSRs. This register defaults to 0xEE, and it is reset to its default value under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- BRST_n assertion when BCOM is '000' or '111'
- Self Refresh with and without Clock Stop
- Power-down entry

In addition to configuring the per-DQ pattern assignment for HIR training mode, this register also configures the per-DQ assignment for the pattern checker used for MRD training mode, the read phase of MWD training mode, and the

pattern generator used for the write phase of MWD.

When a DRAM-space MRW to MR30 occurs, it is snooped by the DB. Since each DRAM is a x4 device, only MR30[3:0] is valid. All DRAM are programmed with the same value. So, when MR30 is snooped, PG[8]RWE6[7:0] is loaded with {MR30[3:0], MR30[3:0]}.

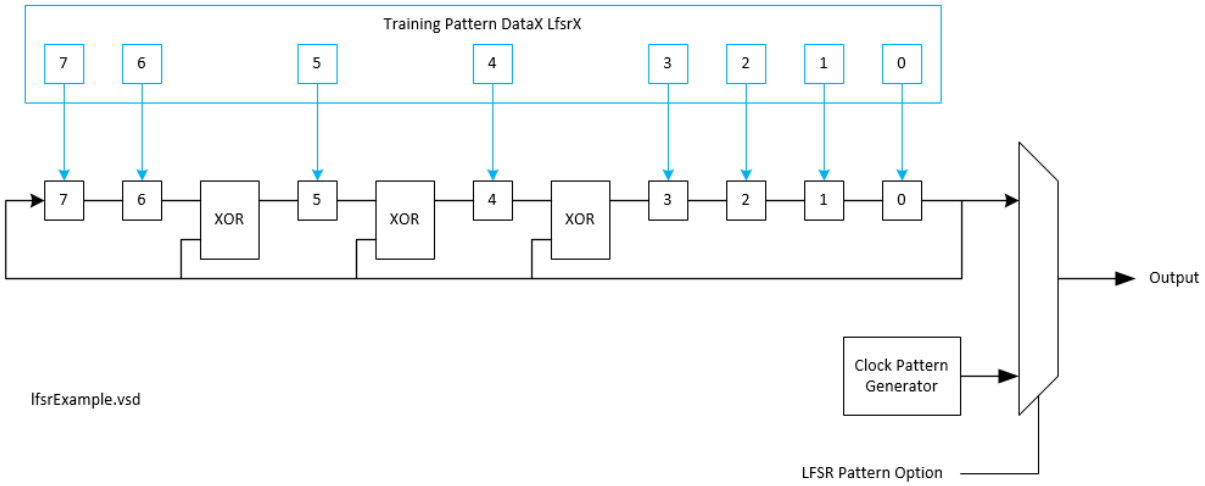


Figure 63 — Example LFSR Topology

Each LFSR is enabled for pattern generation (i.e. next-state computation) only when LFSR format is selected and its LFSR pattern option is selected. Each LFSR is seeded to a new state whenever its respective pattern/seed register PG[8]RW[E4:E3] is written via a DB-space MRW. It is also seeded with the default value of its respective pattern/seed register whenever the reset condition for its respective pattern/seed register occurs (i.e. during power-up initialization, reset initialization with stable power, DB reset, Self-Refresh, and power-down entry).

Each LFSR operates at the UI rate and produces a new output value each UI. Each LFSR only changes state when generating a data burst for a DB-space MRR. During idle times, each LFSR retains its state from the end of the data burst of the previous DB-space MRR. Since the data burst for each DB-space MRR is 16-bits, each LFSR will complete its full sequence after 16 consecutive DB-space MRRs. When an LFSR is seeded with 0x00 the LFSR will produce a constant zero pattern.

The state of LFSR0 will not change when a DB-space MRR occurs if its respective clock pattern option is selected. Instead, the clock-pattern generator changes state. The clock pattern is sent only to the DQ signals whose corresponding assignment bit is set to zero. The first UI of the clock pattern will have a value of zero, the second UI will have a value of one, and this toggle pattern will continue for each subsequent UI of the burst.

The state of LFSR1 will not change when a DB-space MRR occurs if its respective clock pattern option is selected. Instead, the clock-pattern generator changes state. The clock pattern is sent only to the DQ signals whose corresponding assignment bit is set to one. The first UI of the clock pattern will have a value of zero, the second UI will have a value of one, and this toggle pattern will continue for subsequent UI of the burst.

An LFSR changes state for each DB-space MRR received only when LFSR format is selected and its respective LFSR pattern option is selected. The assignment settings have no impact on whether an LFSR state changes for each DB-space MRR received.

In addition to pattern generation during HIR training mode, LFSR0 and LFSR1 are used for pattern checking during MRD training mode and the read phase of MWD training mode.

The state of LFSR0 can be monitored via a DB-space MRRs to read-only register RW9E and RW9C, and the state of LFSR1 can be monitored via a DB-space MRRs to read-only register RW9F and RW9D. HIR training mode must be exited prior to reading these registers. HIR training mode exit and re-entry does not change the state of LFSR0 and LFSR1.

In addition to providing monitoring of LFSR0 and LFSR1 for HIR training mode, these registers also provide monitoring of LFSR0 and LFSR1 when used for the pattern checking during MRD training mode and the read phase of MWD training mode.

8.8.3 Pattern Generation Examples

The following examples cover various read training pattern generator use cases. Table 39 shows an example of serial format usage, Figure 41 shows an example of LFSR format usage and Figure 47 shows an example of LFSR format with 0x00 seed and clock usage.

8.8.3.1 Serial Format Example

Table 39 — Serial Format Example Settings

Data Buffer RW	Operating Mode	Setting
PG[8]RWE2[0]	Read Training Pattern Format	0
PG[8]RWE2[1]	LFSR0 Pattern Option	0
PG[8]RWE2[2]	LFSR1 Pattern Option	0
PG[8]RWE3[7:0]	Read Pattern_0	0x1C
PG[8]RWE4[7:0]	Read Pattern_1	0x59
PG[8]RWE5[7:0]	Read Pattern Invert	0x55

Table 40 — Base Pattern

Base Pattern															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

Table 41 — Serial Format Pattern Example

DQ	Invert	UI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
1	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
2	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
3	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
4	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
5	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
6	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
7	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

8.8.3.2 LFSR Format with LFSR Pattern Example

Table 42 — LFSR Format with LRSR Pattern Example Settings

Data Buffer RW	Operating Mode	Setting
PG[8]RWE2[0]	Read Training Pattern Format	1
PG[8]RWE2[1]	LFSR0 Pattern Option	0
PG[8]RWE2[2]	LFSR1 Pattern Option	0
PG[8]RWE3[7:0]	Read Pattern_0	0x5A
PG[8]RWE4[7:0]	Read Pattern_1	0x3C
PG[8]RWE5[7:0]	Read Pattern Invert	0xF0
PG[8]RWE6[7:0]	Read LFSR Assignment	0xFE

Table 43 — Seed Pattern

Seed Pattern															
LFSR1								LFSR0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0	0	1	0	1	1	0	1	0

Table 44 — LFSR Format with LFSR Pattern Example

DQ	Invert	LFSR	UI															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1	0
1	0	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
2	0	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
3	0	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	0	0
4	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
5	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
6	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1
7	1	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1	1

8.8.3.3 LFSR Format with Clock Pattern Example

Table 45 — LFSR Format with Clock Pattern Example Settings

Data Buffer RW	Operating Mode	Setting
PG[8]RWE2[0]	Read Training Pattern Format	1
PG[8]RWE2[1]	LFSR0 Pattern Option	0
PG[8]RWE2[2]	LFSR1 Pattern Option	1
PG[8]RWE3[7:0]	Read Pattern_0	0x00 (Constant Zero)
PG[8]RWE4[7:0]	Read Pattern_1	0x3C (Don’t care)
PG[8]RWE5[7:0]	Read Pattern Invert	0xDB
PG[8]RWE6[7:0]	Read LFSR Assignment	0x04

Table 46 — Seed Pattern

Seed Pattern															
LFSR1								LFSR0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0

Table 47 — LFSR Format with Clock Pattern Example

DQ	Invert	LFSR	UI															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
3	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.8.4 Timing

Figure 64 shows an example of two back-to-back DB-space MRRs. The DB-space MRRs are short MRRs that are separated by tMRR = 8tCK.

While in HIR mode, when a DB receives any DB-space MRR with a 1tCK BCS_n assertion (target) it generates a BL16 read burst with the full BL16 data pattern sourced from its read pattern generator. The read burst timing is determined by the rank ID field in the DAT0 cycle of the DB-space MRR sequence. The read latency for rank-x and nibble-y is DB_RL(Rx, Ny) + tPDM_RD after the DAT0 cycle of the DB-space MRR sequence.

While in HIR mode, if any DB-space MRR is received with a 2tCK BCS_n assertion (non-target), the DB will not execute the MRR, but it will apply RTT_NOM_RD if enabled with rank-0 timing.

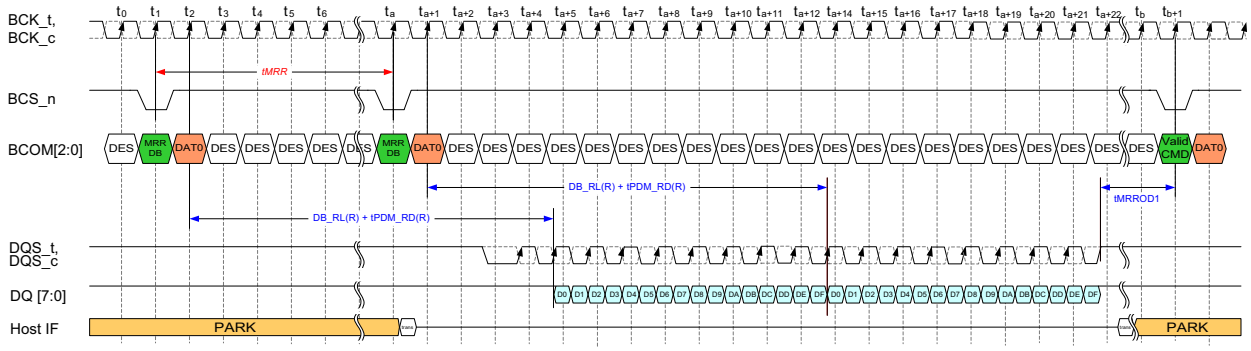


Figure 64 — Back-to-Back DB-Space MRRs - 2tCK Pre, 0.5tCK Post, 3200Mbps

8.9 MDQ Read Error Counter

The Data Buffer supports an error counter per bit that provides per UI to support error counting during MRD training and read phase of MWD training. The error counters are enabled when MRD mode or MWD mode is entered. All error counters can be reset through PG[7]RWF0.

Each Error counter registers is restored to the default value under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- Normal Reset during normal operation. BRST_n assertion and BCOM[2:0]= 000 or BCOM[2:0]= 111
- Self Refresh with and without Clock Stop
- Power-down entry
- Reset event through PG[7]RWF0

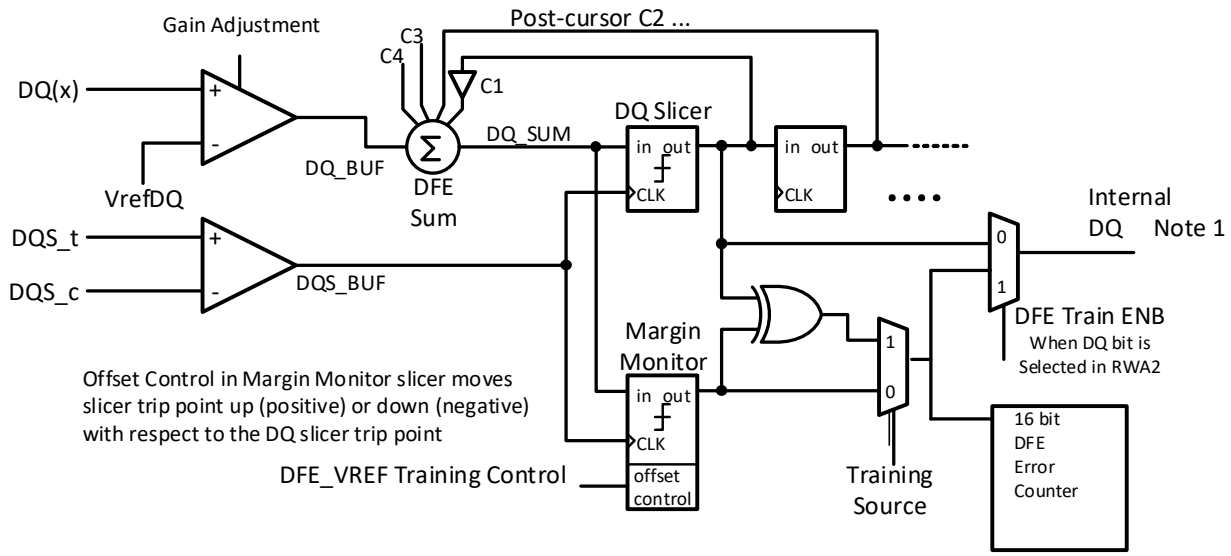
However, it is not reset as a result of MRD/MWD mode entry and exit.

When enabled, each error counter counts bit errors for its respective bit lane during each read burst that is a result of a DRAM-space MRR or RD during MRD training mode or normal read command during MWD training mode. Each error counter holds its value during idle periods. If an error counter reaches its maximum error counter at any time, it will hold its maximum value until reset.

Each error counter is 16 bits wide. Its current error count value can be read at any time via DB-space MRRs to its lower- and upper-byte registers that contain the lower and upper bytes, respectively, of tis 16-bit value (MRD/MWD mode would first need to be exited). The error count value registers are PG[7]RW[EF:E0].

9 Decision Feedback Equalization (DFE)

The DDR5DB01 device will support a 4 Tap decision feedback equalization (DFE) on its host-interface receivers. The host can enable 1, 2, 3 or 4 taps in a consecutive order always starting with Tap 1 as shown in Table 48. The DFE Tap Coefficients and Gain adjustments are set by control words PG[5:4]RWE0- RWFF. These DFE control words allow programming of each parameter on a DQ I/O-specific basis, and they are intended to be trained by the host. The DDR5DB01 device does not support adaptive DFE. In order to allow Data Buffer hardware to correctly preset DFE post-cursor bit values before the start of Write data bursts, all DQ pins must be at or above VDD(min) during DQS preamble and inter-amble.



NOTE 1: This signal propagates through the Data Buffer device and supports regular DDR5DB01 features such as DRAM Data Writes

Figure 65 — DFE Training Circuitry Per Pin

9.1 DFE Tap Configurations

Table 48 — DFE Tap Configurations

RWA0 OP4	RWA0 OP5	RWA0 OP6	RWA0 OP7	Tap 1	Tap 2	Tap 3	Tap 4
0	x	x	x	Disabled	Disabled[1]	Disabled[1]	Disabled[1]
1	0	x	x	Enabled	Disabled	Disabled[2]	Disabled[2]
1	1	0	x	Enabled	Enabled	Disabled	Disabled[3]
1	1	1	0	Enabled	Enabled	Enabled	Disabled
1	1	1	1	Enabled	Enabled	Enabled	Enabled

1. DDR5DB01 hardware disabled by RWA0[4]= 0, RWA0[5], RWA0[6], RWA0[7] are don't care and ignored by Data Buffer.
2. DDR5DB01 hardware disabled by RWA0[5] = 0, RWA0[6], RWA0[7] are don't care and ignored by Data Buffer.
3. DDR5DB01 Hardware disabled by RWA0[6] = 0, RWA0[7] is a don't care and ignored by Data Buffer.

9.2 DFE Gain and Tap Range

Table 49 — DFE Gain and Tap Total Control Word Range

DFE Parameter	Min	Max	Unites
Gain	-6	6	dB
Tap1	- 150	45	mV
Tap 2	- 60	45	mV
Tap 3	- 45	45	mV
Tap 4	- 45	45	mV

Table 50 — DFE Gain and Tap Coefficient Step Parameters

DFE Parameter	DDR5-3200 - 4800			Unit
	Min	Typ	Max	
DFE Gain Bias Step Size[1,2]	1.7	2	2.3	dB
DFE Gain Bias Tolerance (INL)[1,2]	- 0.5	-	0.5	dB
DFE Gain Bias Step Size Tolerance (DNL)[1,2]	- 0.3	-	0.3	dB
DFE Gain Bias Step Time[1]	-	-	300	ns
DFE Tap Bias Step Size[1,2]	1	3	5	mV
DFE Tap Bias Tolerance (INL) (-150 mV to 0 mV)[1,2]	Min (V_ideal x 115%, V_ideal - 3 * LSB)[3,4]	-	Max (V_ideal x 85%, V_ideal + 3 * LSB)[3,4]	mV
DFE Tap Bias Tolerance (INL) (0 mV to 45 mV)[1,2]	V_ideal - 3 * LSB[3,4]	-	V_ideal + 3 * LSB[3,4]	mV
DFE Tap Bias Step Size Tolerance (DNL)[2]	- 66.67	-	66.67	% of Step Size
DFE Tap Bias Step Time	-	-	64	tCK

1. Host Vref fixed at 0.75 x V_{DD}, typical Voltage-Temperature condition (i.e., V_{DD} = 1.1 V, 25 °C), and default gain setting.
2. These parameters are neither subject to silicon validation nor production testing.
3. V_ideal refers to the ideal DFE Tap value based on the setting.
4. LSB = 3 mV.

9.3 Training Accelerator for Decision Feedback Equalization (DFE)

The Data Buffer will support the ability to accelerate DFE training sweeps of critical DFE training parameters for each DQ bit that is enabled for DFE training. This functionality is provided by the DFE training accelerator (DFETA). Figure 66 shows a top-level block diagram for the DFETA and Figure 67 shows the DFETA Flow. There is a single DFETA mode that is global to all DQ pins.

To perform DFE training acceleration, the host first makes sure that the monitor path is selected in RWA1, to directly drive its internal DQ path, and that DQ[x] has DFE training mode enabled.

The host then configures and enables the DFETA for a specific training task, and the DFETA sweeps parameters in parallel for all DQ bits that have DFE training mode enabled. Selected DQs in RWA2 for DFE Training Mode enabled will have their inner/outer loop parameter swept as part of the DFETA mode while non-selected DQs will remain static to their programmed settings.

When enabled, the DFETA has the ability to override VrefDQ, DFE Tap coefficients, and DFE_Vref. VrefDQ, DFE Tap coefficient biases, and DFE_Vref become DFETA loop parameters. DQ's that are not enabled for training in RWA2 shall maintain their per-pin values in PG[6:4] and PG2. This processing flow implements inner and outer loop

levels as shown in Figure 67. The loop parameter values applied by the DFETA depend on how the host has configured its inner and outer loop parameter selection and control.

When the DFETA is first enabled, the selected inner and outer loop parameter values are no longer determined by their respective functional registers. Instead, their values are determined by global inner and outer loop “sweep” registers. For example, if the Tap-1 coefficient bias is selected as the outer loop parameter, the actual Tap-1 coefficient bias value is determined by the global outer-loop sweep register instead of the functional Tap-1 coefficient bias register.

For each DFETA iteration, the host performs a series of Writes to the DRAM followed by a complimentary series of reads from the DRAM, and the host performs the necessary pattern comparison.

At the end of each series of writes, the DFETA modifies the selected inner and outer loop sweep registers as per the flow shown in Figure 67.

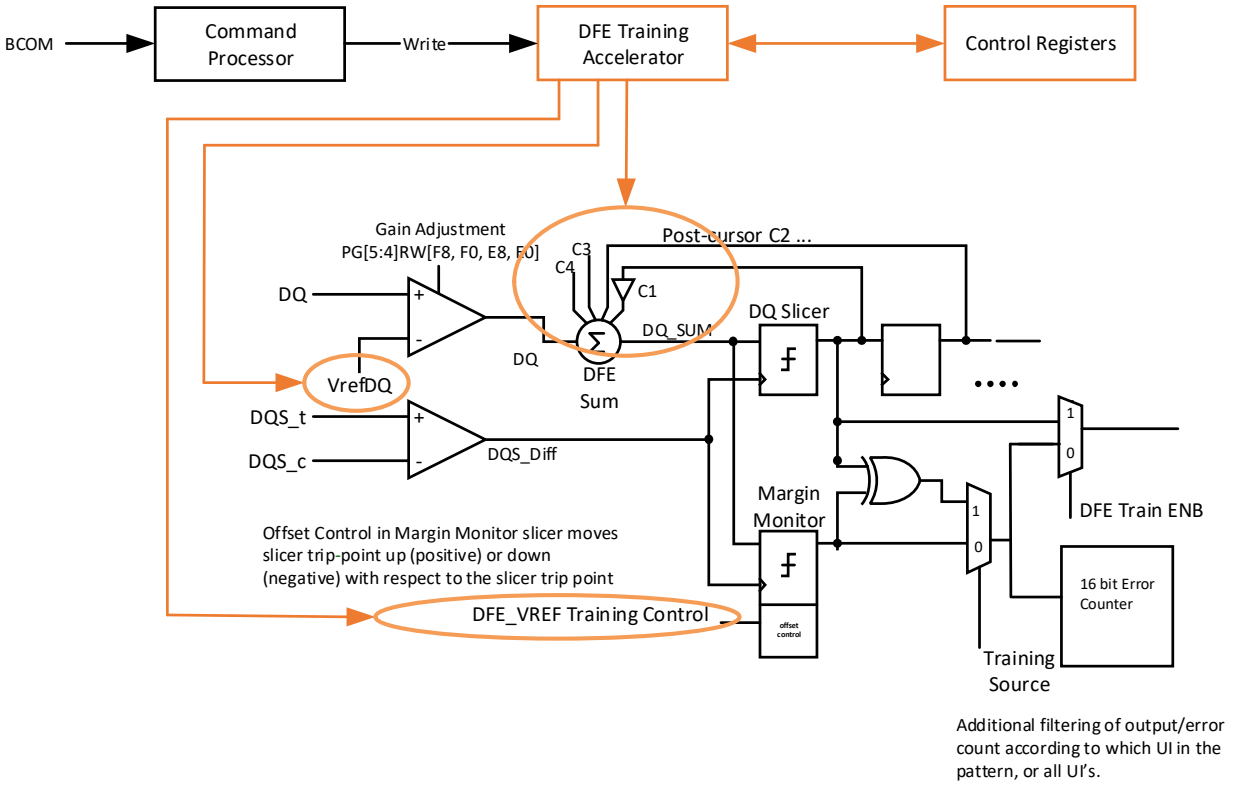


Figure 66 — DFE Training Accelerator

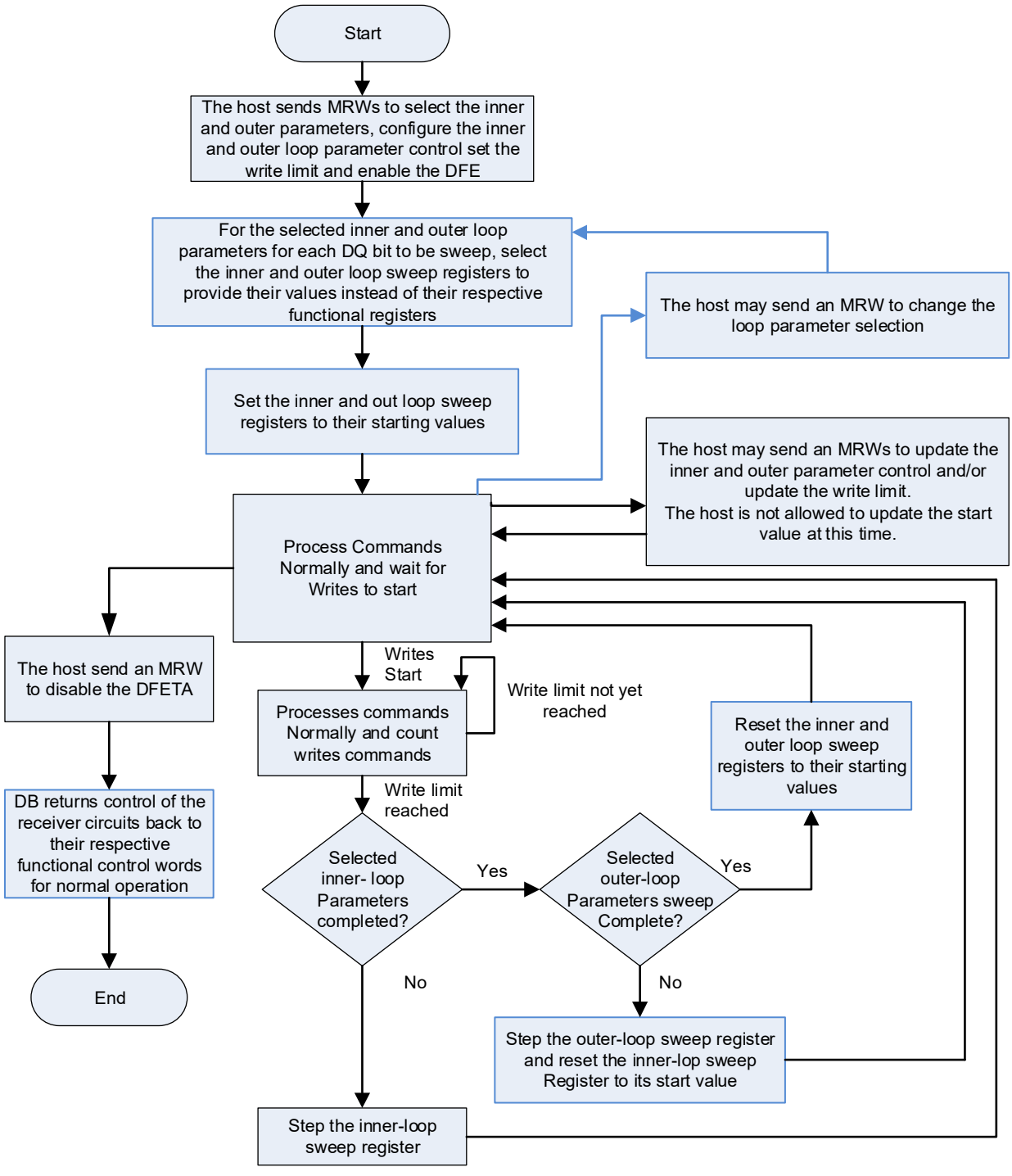


Figure 67 — DFE Training Accelerator Flow

NOTE When host reads current loop parameter value DB shall provide the value for upcoming or next write command.

The DFETA partitions the loop parameters into inner and outer loop parameter sets. These are shown in Table 51. The host selects one parameter out of each set for a particular training scenario. When the NULL parameter is selected for a particular loop level, each pass of the loop does not modify a loop parameter.

Table 51 — Loop Parameter Partitioning

Inter-Loop Parameters	Outer-Loop Parameters
VrefDQ	DFE Tap-1 Coefficient
DFE_Vref	DFE Tap-2 Coefficient
NULL	DFE Tap-3 Coefficient
	DFE Tap-4 Coefficient
	NULL

In addition to selecting the inner and outer loop parameters, the host must also configure the inner and output loop controls, each consisting of starting value, step size and number of increments. This is summarized in Table 52. It is the host's responsibility to make sure that loop parameter ranges are not exceeded depending on the starting value, step size and number of increments specified.

The Tap-x coefficient biases (in the outer loop) and DFE_Vref registers (in the inner loop) are defined as signed-magnitude numbers, whereas the inner loop and outer-loop start values are is defined as a two's complement number to simplify the logic in the accelerator state machine for incrementing from negative to positive values. The Data Buffer must convert the inner/outer-loop sweep register value from two's complement to signed-magnitude for the corresponding parameter.

Table 52 — DFETA Loop Control

Loop Level	Loop Control	Register
Inner	Start Value	PG[9]RW[E2:E1] Inner Loop Start Value
	Step Size	PG[9]RWE7[3:0] Inner Loop Step Size
	Number of increments	PG[9]RWE[9:8] Inner Loop Number of Increments
Outer	Start Value	PG[9]RW[E3] Outer Loop Start Value
	Step Size	PG[9]RWE7[7:4] Outer Loop Step Size
	Number of increments	PG[9]RWEA Outer Loop Number of Increments

Example use cases and respective configurations are shown in Table 53.

Table 53 — DFETA Example Use Cases and Configurations

Use Case	Inner-Loop Parameter	Outer-Loop Parameter
Pulse Response measurement	DFE_Vref	NULL with the number of outer loop increments set to one
Eye height margin measurement	DFE_Vref	Tap-x Coefficient Bias
2D eye measurements	DFE_Vref	NULL with the number of outer loop increments set to the number of host increments

As shown in Figure 67, after the host configures and enables the DFETA, the DFETA enters a waits state and waits for writes to start. While in the wait state, the DB processes commands normally.

Once writes start, the DFETA moves to the write state and begins counting write commands. The number of writes in the series of writes can vary depending on the training scenario. A series of writes can be composed of non-contiguous or back-to-back write commands. The DFETA provides a programmable 16-bit write-limit counter to detect the end of each series of writes. The write-limit is configured using PG[9]RW[EF:EE]. The write limit counter is re-initialized for the next full count period each time the wait state is entered. It is the responsibility of the host to make sure that the number of writes sent matches the write limit. The write-limit counter state can be read via MRRs to read-only registers, PG[9]RW[F1:F0].

While in the write state, the DB processes writes normally until the write limit is reached. The DB processes other commands normally as well. If an MRR or a Read command occurs, the DFETA will maintain its state. If a DB space MRW command occurs, it is the host's responsibility to make sure that it does not alter any registers that will perturb

the current DFETA iteration. If an MPC command occurs, the DFETA will maintain its state.

While in the wait state, the host may send an MRW to change the loop parameter selection.

For example, if the Tap-1 coefficient bias is currently the selected outer-loop parameter, the actual tTap-1 coefficient bias value is determined by the outer-loop sweep register instead of the functional Tap-1 coefficient bias register.

If the Tap-2 coefficient bias is then selected as the outer-loop parameter, the actual Tap-2 coefficient bias value is then determined by the outer-loop sweep register, and the actual Tap-1 coefficient bias value returns to being determined by its functional Tap-1 coefficient bias register. Since the wait state allows for normal command processing, the host can send MRWs to change the settings of any of the functional VrefDQ, DFE tap coefficient bias, and DFE_Vref registers while in the wait state.

While in the wait state, the host may send MRWs to update the inner and outer loop parameter control and/or update the write limit.

When the write limit is reached, the host must stop write traffic and must wait $t_{DFETA\_LoopUpdateWait}$ for the DFETA to update its inner and outer loop parameters for the next iteration as shown in Figure 67.

When the DFETA is disabled, the selected inner and outer loop parameters are returned to being determined by their respective functional registers.

The timing parameters associated with the DFETA are shown in Table 155.

10 Control Words

The DDR5DB01 device features a set of 8-bit control words, which allow the optimization of the device properties for different raw card designs. DDR5RCD and DDR5DB01 control word writes appear as MRW commands but with the CW bit HIGH. DRAMs will ignore MRW commands with the CW bit set HIGH. The different control words and settings are described below. Any change to these control words require some time for the device to settle, these times are defined in Table 155, “Input Timing requirements”. The chip select input, BCS_n, must be kept HIGH during that time.

The DDR5DB01 must support control word access for any of the DDR5DB01 specified frequency ranges.

The control word space is divided as follows:

10.1 Register Word Decoding

The MRW command sequence is initiated in the data buffer when the BCOM control bus code received at the DDR5 DB is equal to 000b (BCOM[2:0]=000). The RW address and the settings are transmitted over the MRA bits included in the MRW command sequence in the six clock cycles immediately following the cycle when the 000b BCOM command is captured. The reset default state of all control word bits unless otherwise specified is ‘0’. Every time the device is reset, its default state is restored. Stopping the clocks (BCK_t = BCK_c = HIGH) to put the device in low-power mode will not alter the control word settings.

Data Buffer Control Word attributes can be:

- Reserved[1]
- Read Only
- Write Only
- RD/WR
- Sticky - Cleared by power cycle not Reset

The DDR5 Mode Register space is divided as follows:

Table 54 — Control Word Addressing

CW bit	MRA7	Description
0	x	DRAM MR space.
1	0	RCD CW space. 128 registers decoded via MRA[6:0]
1	1	Data Buffer CW space. 128 registers decoded via MRA[6:0]

Within the DB control word space, 96 registers are accessed directly, while 32 registers are addressed through an 8-bit paging system, providing 8192 registers. RWDF is the page register while addresses E0-FF are used to access the registers within each page. Pages 00-7F are for JEDEC use while pages 80-FF are vendor specific.

1. Reserved control bits may not be physically implemented and they shall be written to zero to ensure forward compatibility.

Table 55 — Control Word spaces

MRA[7:0]	Location	Page Pointer RW[1]	Page value	Definition	Size (bytes)	Description
00h to 5Fh	RCD	RW5F	X	JEDEC	96	96 directly addressed registers
60h to 7Fh	RCD	RW5F	00h-7Fh	JEDEC	4096	32 paged registers
60h to 7Fh	RCD	RW5F	80h-FFh	Vendor	4096	32 paged registers
80h to DFh	Data Buffer	RWDF	X	JEDEC	96	96 directly addressed registers
E0h to FFh	Data Buffer	RWDF	00h-7Fh	JEDEC	4096	32 paged registers
E0h to FFh	Data Buffer	RWDF	80h-FFh	Vendor	4096	32 paged registers

1. RW5F is the Page Pointer located in the DDR5RCD and RWDF is the Page Pointer located in the DDR5DB01.

All registers are 8-bits wide. If enabled in RCD, all MRW accesses are sent across the BCOM bus to the data buffers, allowing the data buffers to snoop values sent to the DRAM or RCD.

10.2 Reading Control Words from Data Buffer

MRR commands read data from the MR locations in either the DRAM or the data buffer. MR locations in the RCD must be read by first transferring their contents to a DRAM register and then reading that DRAM register using the MRR command. If the CW bit of the MRR command is 0, the MR read data will come from the DRAM and the data buffer will treat the command like a regular Read command. If the CW bit is 1, the MR read data will come from the data buffer and all undefined or reserved bits in the selected MR location will be driven as '0' by the DDR5DB01.

The data buffer will always drive valid data and strobe pattern sequences on its Host interface in response to an MRR command. Depending on the value of the MRR CW bit, the data may come from DRAMs or from internal registers. When the MRR command has CW = 1 and MRA7 = 0, the data buffer treats the target location as Reserved and returns all-zero bit values regardless of the address code in MRA[6:0].

10.3 Direct Control Word Decoding

Table 56 — Direct Control Word Decoding

	Register Control Word	MRA [7:0] HEX[1]	Meaning
Modes	RW80[2]	0x80	Features
	RW81	0x81	Buffer Configuration Modes
	RW82	0x82	BCS_n BCOM Training
	RW83	0x83	[M]DQS, [M]DQ Training Modes
Timing and Voltage	RW84[2]	0x84	LRDIMM Operating Speed
	RW85[2]	0x85	Fine Granularity DIMM Operating Speed
	RW86[2]	0x86	DQS PARK
	RW87[2]	0x87	Host Interface DQ RTT WR & Park Termination
	RW88[2]	0x88	Host Interface DQ RTT NOM Termination
	RW89	0x89	Reserved
	RW8A[2]	0x8A	Host Interface DQ Driver
	RW8B[2]	0x8B	DRAM Interface MDQ Driver and Termination
	RW8C[2]	0x8C	MDQS and MDQ PARK
	RW8D	0x8D	Loopback Control
	RW8E	0x8E	Loopback RTT and Ron
	RW8F[2]	0x8F	Host Interface Read DQS Offset Timing
Data Training	RW90	0x90	Continuous Burst Mode Control
	RW91	0x91	Reserved
	RW92[2]	0x92	PBA Enumerate ID Control Word
	RW93[2]	0x93	PBA Buffer Select ID Control Word
	RW94	0x94	Internal Receive Enable Offset Coarse Status
	RW95	0x95	Internal Receive Enable Offset Fine Lower Nibble Status
	RW96	0x96	Internal Receive Enable Offset Fine Upper Nibble Status
	RW97	0x97	Buffer Training Configuration Control Word
	RW98	0x98	Buffer Training Status Word
	RW99	0x99	Reserved
	RW9A	0x9A	Reserved
	RW9B	0x9B	Reserved
	RW9C	0x9C	LFSR0 State Monitor for Reads
	RW9D	0x9D	LFSR1 State Monitor for Reads
	RW9E	0x9E	LFSR0 State Monitor for Writes
	RW9F	0x9F	LFSR1 State Monitor for Writes
DFE	RWA0[2]	0xA0	DFE Global Control
	RWA1	0xA1	DQ[7:0] DFE Training Mode
	RWA2	0xA2	DQn DFE pin selection
Periodic	RWB0	0xB0	DRAM tDQS2DQ Tracking
	RWB1	0xB1	DRAM tDQS2DQ Tracking Return Value
Reserved	RWB3	0xB3	Reserved
	...	...	Reserved
	...	...	Reserved
	...	...	Reserved
	RWDE	0xDE	Reserved
CW Page	RWDF	0xDF	CW DB Page

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

10.4 Paged Control Word Decoding

10.4.1 Page [1:0] Rank Training Control Word Decoding

Table 57 — Page [1:0] Rank Training Control Word Decoding [1]

Page	Register Control Word	MRA [7:0] HEX[2]	Meaning
[1:0]	RWE0[3]	0xE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word
	RWE1[3]	0xE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word
	RWE2[3]	0xE2	Lower nibble DRAM interface receive enable training control
	RWE3[3]	0xE3	Upper nibble DRAM interface receive enable training control
	RWE4[3]	0xE4	Lower nibble MDQS read delay control
	RWE5[3]	0xE5	Upper nibble MDQS read delay control
	RWE6[3]	0xE6	Lower nibble MDQ Write Baseline Delay control
	RWE7[3]	0xE7	Upper nibble MDQ Write Baseline Delay control
	RWE8[3]	0xE8	Lower nibble DRAM interface write leveling control
	RWE9[3]	0xE9	Upper nibble DRAM interface write leveling control
	RWEA[3]	0xEA	MDQ0/4-Read delay control
	RWEB[3]	0xEB	MDQ1/5-Read delay control
	RWEC[3]	0xEC	MDQ2/6-Read delay control
	RWED[3]	0xED	MDQ3/7-Read delay control
	RWEE[3]	0xEE	MDQ0/4-MDQS write delay control
	RWEF[3]	0xEF	MDQ1/5-MDQS write delay control
	RWF0[3]	0xF0	MDQ2/6-MDQS write delay control
	RWF1[3]	0xF1	MDQ3/7-MDQS write delay control
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

1. The Data Path Training modes are performed with Fixed BL16.
2. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
3. Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

10.4.2 Page 2 Vref Paged Control Word Decoding

Table 58 — Page 2 Vref Paged Control Word Decoding

Page	Register Control Word	MRA [7:0] HEX[1]	Meaning
[0x02]	RWE0[2]	0xE0	DQ0 VrefDQ
	RWE1[2]	0xE1	DQ1 VrefDQ
	RWE2[2]	0xE2	DQ2 VrefDQ
	RWE3[2]	0xE3	DQ3 VrefDQ
	RWE4[2]	0xE4	DQ4 VrefDQ
	RWE5[2]	0xE5	DQ5 VrefDQ
	RWE6[2]	0xE6	DQ6 VrefDQ
	RWE7[2]	0xE7	DQ7 VrefDQ
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0[2]	0xF0	Lower Nibble VrefMDQ
	RWF1[2]	0xF1	Upper Nibble VrefMDQ
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	BVref
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

10.4.3 Page 4 DQ[3:0]DFE Control Word Decoding

Table 59 — Page 4 DQ[3:0]DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x04	RWE0[2]	0xE0	DQ0 Rx DFE Gain Coefficients
	RWE1[2]	0xE1	DQ0 Rx DFE Tap 1 Coefficients
	RWE2[2]	0xE2	DQ0 Rx DFE Tap 2 Coefficients
	RWE3[2]	0xE3	DQ0 Rx DFE Tap 3 Coefficients
	RWE4[2]	0xE4	DQ0 Rx DFE Tap 4 Coefficients
	RWE5	0xE5	RFU
	RWE6	0xE6	RFU
	RWE7	0xE7	RFU
	RWE8[2]	0xE8	DQ1 Rx DFE Gain Coefficients
	RWE9[2]	0xE9	DQ1 Rx DFE Tap 1 Coefficients
	RWEA[2]	0xEA	DQ1 Rx DFE Tap 2 Coefficients
	RWEB[2]	0xEB	DQ1 Rx DFE Tap 3 Coefficients
	RWEC[2]	0xEC	DQ1 Rx DFE Tap 4 Coefficients
	RWED	0xED	RFU
	RWEE	0xEE	RFU
	RWEF	0xEF	RFU
	RWF0[2]	0xF0	DQ2 Rx DFE Gain Coefficients
	RWF1[2]	0xF1	DQ2 Rx DFE Tap 1 Coefficients
	RWF2[2]	0xF2	DQ2 Rx DFE Tap 2 Coefficients
	RWF3[2]	0xF3	DQ2 Rx DFE Tap 3 Coefficients
	RWF4[2]	0xF4	DQ2 Rx DFE Tap 4 Coefficients
	RWF5	0xF5	RFU
	RWF6	0xF6	RFU
	RWF7	0xF7	RFU
	RWF8[2]	0xF8	DQ3 Rx DFE Gain Coefficients
	RWF9[2]	0xF9	DQ3 Rx DFE Tap 1 Coefficients
	RWFA[2]	0xFA	DQ3 Rx DFE Tap 2 Coefficients
	RWFB[2]	0xFB	DQ3 Rx DFE Tap 3 Coefficients
	RWFC[2]	0xFC	DQ3 Rx DFE Tap 4 Coefficients
	RWFD	0xFD	RFU
	RWFE	0xFE	RFU
	RWFF	0xFF	RFU

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

10.4.4 Page 5 DQ[7:4] DFE Paged Control Word Decoding

Table 60 — Page 5 DQ[7:4]DFE Paged Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x05	RWE0[2]	0xE0	DQ4 Rx DFE Gain Coefficients
	RWE1[2]	0xE1	DQ4 Rx DFE Tap 1 Coefficients
	RWE2[2]	0xE2	DQ4 Rx DFE Tap 2 Coefficients
	RWE3[2]	0xE3	DQ4 Rx DFE Tap 3 Coefficients
	RWE4[2]	0xE4	DQ4 Rx DFE Tap 4 Coefficients
	RWE5	0xE5	RFU
	RWE6	0xE6	RFU
	RWE7	0xE7	RFU
	RWE8[2]	0xE8	DQ5 Rx DFE Gain Coefficients
	RWE9[2]	0xE9	DQ5 Rx DFE Tap 1 Coefficients
	RWEA[2]	0xEA	DQ5 Rx DFE Tap 2 Coefficients
	RWEB[2]	0xEB	DQ5 Rx DFE Tap 3 Coefficients
	RWEC[2]	0xEC	DQ5 Rx DFE Tap 4 Coefficients
	RWED	0xED	RFU
	RWEE	0xEE	RFU
	RWEF	0xEF	RFU
	RWF0[2]	0xF0	DQ6 Rx DFE Gain Coefficients
	RWF1[2]	0xF1	DQ6 Rx DFE Tap 1 Coefficients
	RWF2[2]	0xF2	DQ6 Rx DFE Tap 2 Coefficients
	RWF3[2]	0xF3	DQ6 Rx DFE Tap 3 Coefficients
	RWF4[2]	0xF4	DQ6 Rx DFE Tap 4 Coefficients
	RWF5	0xF5	RFU
	RWF6	0xF6	RFU
	RWF7	0xF7	RFU
	RWF8[2]	0xF8	DQ7 Rx DFE Gain Coefficients
	RWF9[2]	0xF9	DQ7 Rx DFE Tap 1 Coefficients
	RWFA[2]	0xFA	DQ7 Rx DFE Tap 2 Coefficients
	RWFB[2]	0xFB	DQ7 Rx DFE Tap 3 Coefficients
	RWFC[2]	0xFC	DQ7 Rx DFE Tap 4 Coefficients
	RWFD	0xFD	RFU
	RWFE	0xFE	RFU
	RWFF	0xFF	RFU

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

10.4.5 Page 6 DFE_Vref and Error Counter DFE Paged Control Word Decoding

Table 61 — Page 6 DFE_Vref and Error Counter DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x06	RWE0	0xE0	DQ0 Rx DFE Error Counter Lower 8 Bits
	RWE1	0xE1	DQ0 Rx DFE Error Counter Upper 8 Bits
	RWE2	0xE2	DQ0 DFE_Vref[2]
	RWE3	0xE3	Sign bit DQ0 DFE_Vref
	RWE4	0xE4	DQ1 Rx DFE Error Counter Lower 8 Bits
	RWE5	0xE5	DQ1 Rx DFE Error Counter Upper 8 Bits
	RWE6	0xE6	DQ1 DFE_Vref[2]
	RWE7	0xE7	Sign bit DQ1 DFE_Vref
	RWE8	0xE8	DQ2 Rx DFE Error Counter Lower 8 Bits
	RWE9	0xE9	DQ2 Rx DFE Error Counter Upper 8 Bits
	RWEA	0xEA	DQ2 DFE_Vref[2]
	RWEB	0xEB	Sign bit DQ2 DFE_Vref
	RWEC	0xEC	DQ3 Rx DFE Error Counter Lower 8 Bits
	RWED	0xED	DQ3 Rx DFE Error Counter Upper 8 Bits
	RWEE	0xEE	DQ3 DFE_Vref[2]
	RWEF	0xEF	Sign bit DQ3 DFE_Vref
	RWF0	0xF0	DQ4 Rx DFE Error Counter Lower 8 Bits
	RWF1	0xF1	DQ4 Rx DFE Error Counter Upper 8 Bits
	RWF2	0xF2	DQ4 DFE_Vref[2]
	RWF3	0xF3	Sign bit DQ4 DFE_Vref
	RWF4	0xF4	DQ5 Rx DFE Error Counter Lower 8 Bits
	RWF5	0xF5	DQ5 Rx DFE Error Counter Upper 8 Bits
	RWF6	0xF6	DQ5 DFE_Vref[2]
	RWF7	0xF7	Sign bit DQ5_ DFE_Vref
	RWF8	0xF8	DQ6 Rx DFE Error Counter Lower 8 Bits
	RWF9	0xF9	DQ6 Rx DFE Error Counter Upper 8 Bits
	RWFA	0xFA	DQ6 DFE_Vref[2]
	RWFB	0xFB	Sign bit DQ6 DFE_Vref
	RWFC	0xFC	DQ7 Rx DFE Error Counter Lower 8 Bits
	RWFD	0xFD	DQ7 Rx DFE Error Counter Upper 8 Bits
	RWFE	0xFE	DQ7 DFE_Vref[2]
	RWFF	0xFF	Sign bit DQ7 DFE_Vref

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. Each DQ I/O has its own Margin Monitor with DFE_Vref control.

10.4.6 Page 7 MDQ Error Counters Paged Control Word Decoding

Table 62 — Page 7 MDQ Error Counters Paged Control Word Decoding[1]

Page	Register Control Word	MR [7:0] HEX[2]	Meaning
0x07	RWE0	0xE0	MDQ0 Rx Error Counter Lower 8 Bits
	RWE1	0xE1	MDQ0 Rx Error Counter Upper 8 Bits
	RWE2	0xE2	MDQ1 Rx Error Counter Lower 8 Bits
	RWE3	0xE3	MDQ1 Rx Error Counter Upper 8 Bits
	RWE4	0xE4	MDQ2 Rx Error Counter Lower 8 Bits
	RWE5	0xE5	MDQ2 Rx Error Counter Upper 8 Bits
	RWE6	0xE6	MDQ3 Rx Error Counter Lower 8 Bits
	RWE7	0xE7	MDQ3 Rx Error Counter Upper 8 Bits
	RWE8	0xE8	MDQ4 Rx Error Counter Lower 8 Bits
	RWE9	0xE9	MDQ4 Rx Error Counter Upper 8 Bits
	RWEA	0xEA	MDQ5 Rx Error Counter Lower 8 Bits
	RWEB	0xEB	MDQ5 Rx Error Counter Upper 8 Bits
	RWEC	0xEC	MDQ6 Rx Error Counter Lower 8 Bits
	RWED	0xED	MDQ6 Rx Error Counter Upper 8 Bits
	RWEE	0xEE	MDQ7 Rx Error Counter Lower 8 Bits
	RWEF	0xEF	MDQ7 Rx Error Counter Upper 8 Bits
	RWF0	0xF0	Error Counter Reset
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

1. Read-only register for MDQ Error Counters
2. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

10.4.7 Page 8 MR Snooped Settings Paged Control Word Decoding

Upon receiving a DRAM MR command, the DDR5 RCD snoops relevant bits that are needed by the DB for its operation and sends them to the DB via an MRS Write command over the BCOM bus. The data buffer stores these bit settings in DB-space RWs. The stored snooped MR settings can be read by means of MRR commands. The MRW command can be used to program these settings directly and override the results of any prior MR snooping.

Table 63 — Page 8 MR Snooped Setting Paged Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x08	RWE0	0xE0	BL and CL
	RWE1	0xE1	Read and write pre-amble and post-amble settings
	RWE2	0xE2	Read training pattern mode settings
	RWE3	0xE3	Read training pattern Data0/LFSR0 setting
	RWE4	0xE4	Read training pattern Data1/LFSR1 setting
	RWE5	0xE5	Read training pattern invert DQL
	RWE6	0xE6	Read LFSR assignment MR30
	RWE7	0xE7	DQS Interval Timer Run Time MR45
	RWE8	0xE8	Read and Write CRC enable MR50[1:0]
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	Reserved
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

10.4.8 Page 9 DFE Training Accelerator Paged Control Word Decoding

Table 64 — Page 9 DFE Training Accelerator Paged Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x09	RWE0	0xE0	DFETA Training Mode
	RWE1	0xE1	DFETA Inner Loop Start Value [7:0]
	RWE2	0xE2	DFETA Inner Loop Start Value, Bit [8]
	RWE3	0xE3	DFETA Outer Loop Start Value
	RWE4	0xE4	DFETA Inner Loop Current Value, Bit [7:0]
	RWE5	0xE5	DFETA Inner Loop Current Value, Bit [8]
	RWE6	0xE6	DFETA Outer Loop Current Value
	RWE7	0xE7	DFETA Inner and Outer Loop Step Size
	RWE8	0xE8	DFETA Inner Loop Number of Increments, Bit [7:0]
	RWE9	0xE9	DFETA Inner Loop Number of Increments, Bit [8]
	RWEA	0xEA	DFETA Outer Loop Number of Increments
	RWEB	0xEB	DFETA Inner Loop Current Increment, Bit [7:0]
	RWEC	0xEC	DFETA Inner Loop Current Increment, Bit [8]
	RWED	0xED	DFETA Outer Loop Current Increment
	RWEE	0xEE	DFETA Write Limit Value - Lower Byte
	RWEF	0xEF	DFETA Write Limit Value - Upper Byte
	RWF0	0xF0	DFETA Write Limit Counter Value Status - Lower Byte
	RWF1	0xF1	DFETA Write Limit Counter Value Status - Upper Byte
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

10.4.9 Page A Periodic Update Paged Control Word Decoding

Table 65 — Page A Periodic Update Paged Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x0A	RWE0	0xE0	Lower-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter LSB
	RWE1	0xE1	Lower-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter MSB
	RWE2	0xE2	Lower-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter LSB
	RWE3	0xE3	Lower-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter MSB
	RWE4	0xE4	Upper-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter LSB
	RWE5	0xE5	Upper-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter MSB
	RWE6	0xE6	Upper-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter LSB
	RWE7	0xE7	Upper-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter MSB
	RWE8	0xE8	Lower-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay LSB
	RWE9	0xE9	Lower-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay MSB
	RWEA	0xEA	Lower-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay LSB
	RWEB	0xEB	Lower-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay MSB
	RWEC	0xEC	Upper-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay LSB
	RWED	0xED	Upper-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay MSB
	RWEE	0xEE	Upper-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay LSB
	RWEF	0xEF	Upper-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay MSB
	RWF0	0xF0	Lower-Nibble, Rank-0 Current DRAM DQS Oscillator Counter LSB
	RWF1	0xF1	Lower-Nibble, Rank-0 Current DRAM DQS Oscillator Counter MSB
	RWF2	0xF2	Lower-Nibble, Rank-1 Current DRAM DQS Oscillator Counter LSB
	RWF3	0xF3	Lower-Nibble, Rank-1 Current DRAM DQS Oscillator Counter MSB
	RWF4	0xF4	Upper-Nibble, Rank-0 Current DRAM DQS Oscillator Counter LSB
	RWF5	0xF5	Upper-Nibble, Rank-0 Current DRAM DQS Oscillator Counter MSB
	RWF6	0xF6	Upper-Nibble, Rank-1 Current DRAM DQS Oscillator Counter LSB
	RWF7	0xF7	Upper-Nibble, Rank-1 Current DRAM DQS Oscillator Counter MSB
	RWF8	0xF8	Lower-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay LSB
	RWF9	0xF9	Lower-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay MSB
	RWFA	0xFA	Lower-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay LSB
	RWFB	0xFB	Lower-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay MSB
	RWFC	0xFC	Upper-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay LSB
	RWFD	0xFD	Upper-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay MSB
	RWFE	0xFE	Upper-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay LSB
	RWFF	0xFF	Upper-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay MSB

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.

10.4.10 Page B Dynamic ODT Control Word Decoding

Table 66 — Page B Dynamic ODT Control Word Decoding

Page	Register Control Word	MR [7:0] HEX[1]	Meaning
0x0B	RWE0[2]	0xE0	Rank0 ODTLon_WR_offset
	RWE1[2]	0xE1	Rank1 ODTLon_WR_offset
	RWE2[2]	0xE2	Rank0 ODTLoff_WR_offset
	RWE3[2]	0xE3	Rank1 ODTLoff_WR_offset
	RWE4[2]	0xE4	Rank0 ODTLon_WR_NT_offset
	RWE5[2]	0xE5	Rank0 ODTLoff_WR_NT_offset
	RWE6[2]	0xE6	Rank0 ODTLon_RD_NT_offset
	RWE7[2]	0xE7	Rank0 ODTLoff_RD_NT_offset
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	Reserved
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

1. MRA7 must be 0 for RCD accesses and must be 1 for Data Buffer (DB) Control Words accesses.
2. Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

10.5 Sticky Bits

10.5.1 Direct-

1. RW80[7]: BCOM 2N/1N mode selection for Context switching
2. RW80[2:0]: 1N/2N, Low Nibble/Upper Nibble disable
3. RW80[5:4]: R1/R0 disable
4. RW84[3:0]: DIMM Operating Speed
5. RW84[6]: Freq Context
6. RW85[4:0]: Fine Granularity DIMM Operating Speed
7. RW86[2:0]: DQS RTT Park Termination
8. RW87[5:0]: Host Interface DQ RTT Termination
9. RW88[5:0]: Host Interface DQ RTT NOM Termination
10. RW8A[6:0]: Host Interface DQ Driver
11. RW8B[6:0]: DRAM Interface MDQ Driver
12. RW8C[5:0]: DRAM Interface MDQ Driver
13. RW8F[2:0]: Host Interface DQS0 Pre-launch
14. RW8F[6:4]: Host Interface DQS1 Pre-launch
15. RW92[3:0]: PBA Enumerate ID
16. RW93[3:0]: PBA Buffer Select ID
17. RWA0[7:0]: DFE Feature ENB/DFE_Vref ENB/ERROR Counter ENB/Broadcast ENB/tap1/2/3/4 ENB
18. RWB0[0]: DRAM tDQS2DQ Tracking
19. RWB1[7:0]: DRAM tDQS2DQ Tracking Return Value

10.5.2 Paged-

1. PG[1:0]RW[F1:E0]OP[7:0]: Additional Cycles of DRAM Interface Write Leveling/DRAM interface receive enable/MDQS read delay control/MDQ Write Baseline Delay/DRAM interface write leveling/per pin RD-delay/ per pin WR-delay
2. PG[2]RW[E7:E0]OP[7:0]: Host Interface Internal per pin VrefDQ
3. PG[2]RW[F1:F0]OP[7:0]: DRAM Interface Internal per nibble VrefMDQ
4. PG[5:4]RW[E1,E9,F1,F9]OP[7:0]: tap1
5. PG[5:4]RW[E2,EA,F2,FA]OP[7:0]: tap2
6. PG[5:4]RW[E3,EB,F3,FB]OP[7:0]: tap3
7. PG[5:4]RW[E4,EC,F4,FC]OP[7:0]: tap4
8. PG[5:4]RW[E0,E8,F0,F8]OP[7:0]: gain offset
9. PG[8]RWE7 DQS Interval Timer Runtime MR45
10. PG[A]RW[FF-E0]: Periodic Update
11. PG[B]RW[E7:E0]OP[7:0]: Dynamic ODT Control Offsets

10.6 Mode Control Words

10.6.1 RW80 - Features Control Word

Table 67 — RW80: Features Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	BCOM Command Rate (Read Only)	2N (Default)
x	x	x	x	x	x	x	1		1N
x	x	x	x	x	x	0	x	Low Nibble I/O buffer Disable[2]	Enable
x	x	x	x	x	x	1	x		Disable[3,4]
x	x	x	x	x	0	x	x	Upper Nibble I/O buffer Disable[5]	Enable
x	x	x	x	x	1	x	x		Disable[3]
x	x	x	x	0	x	x	x	Lockout Protection Enable[6]	No effect[7]
x	x	x	x	1	x	x	x		Protection enabled[8]
x	x	x	0	x	x	x	x	Rank0 Present[9]	Package Rank 0 Enabled
x	x	x	1	x	x	x	x		Package Rank 0 Disabled[10]
x	x	0	x	x	x	x	x	Rank 1 Present[9]	Package Rank 1 Enabled
x	x	1	x	x	x	x	x		Package Rank 1 Disabled
x	0	x	x	x	x	x	x	Power Down Mode[11]	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	BCOM 2N/1N mode selection in self refresh Exit[12]	2N
1	x	x	x	x	x	x	x		1N

1. RW80[7], RW80[5:4] and RW80[2:0] will be sticky, cleared by power cycle not reset.
2. When this bit is set [M]DQS0_t, [M]DQS0_c, [M]DQ[3:0] are disabled.
3. Disable does not affect buffer control words, or the BCOM programming of buffer control words
4. Per Buffer and Per DRAM Enumeration must be completed before disabling either nibble's I/O buffers
5. When this bit is set [M]DQS1_t, [M]DQS1_c, [M]DQ[7:4] are disabled.
6. This feature is intended to protect the Data Buffer against lockout state that is unrecoverable with BRST_n Reset and is caused by invalid BCOM commands associated with incorrect input signal voltage levels or timing.
7. This control bit is type "Write-1 Only" and cannot be written to 0 by the user. It only gets cleared to zero by BRST_n Reset or by internal Power-On Reset.
8. When OP[3] = 1, the Data Buffer prevents Writes to vendor specific CW pages (i.e., Pages 80 to FFh) triggered by commands received at the BCOM interface of the Data Buffer including MRW commands.
9. This control word contains the number of package rank used on an LRDIMM. The host controller will write RW80[5:4] to indicate which package ranks are used on the LRDIMM so that the DDR5DB01 can power down unnecessary logic for unused package ranks.
10. When RW80[4] is set to "1", physical Rank 0 is not present. In this case, for non-target WR/RD, the non-target ODT output timing should be based on Rank 1 instead of Rank 0 training result.
11. This bit will disable vendor specific circuitry if any, for power reduction during PDE mode.
12. When written by MRW command, the setting in RW80[7] is not applied directly by the DB. Instead, during each Exit from Self Refresh with Clock Stop, the DB uses the setting in RW80[7] to select the BCOM 2N/1N mode and to update the status in RW80[0] accordingly. Conversely, when the DB executes a "Set 1N BCOM CMD Timing" BCOM Strap command, the DB hardware sets RW80[7] to '1' and it directly applies BCOM 1N mode and updates the status in RW80[0] to '1'.

10.6.2 RW81 Buffer Configuration Mode Control Word

This control word contains data buffer mode information that does not come from snooping of DRAM MRW commands.

Table 68 — RW81: Buffer Configuration Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	PBA Enumerate Programming Mode[1]	PBA Enumerate Mode Disabled
x	x	x	x	x	x	x	1		PBA Enumerate Mode Enabled
x	x	x	x	x	x	0	x	VrefDQ broadcast	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	VrefMDQ broadcast	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Assigns IDs to specific Data Buffer on the DIMM.

10.6.3 RW82 - Transparent and DQ Pass Through Control Word

Table 69 — RW82: Transparent and DQ Pass Through Support Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Transparent Mode Enable	Transparent mode disabled
x	x	x	x	x	x	x	1		Transparent mode enabled[1]
x	x	x	x	x	x	0	x	Termination disable for TPM and DQ PTM	Termination enabled
x	x	x	x	x	x	1	x		Termination disabled
x	x	x	x	x	0	x	x	DQ Pass Through Mode	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	DQ pass through mode direction select	Write direction (default)
x	x	x	x	1	x	x	x		Read direction
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. A waiting time t_{TM_Entry} applies when Transparent Mode is enabled in RW82[0].

10.6.4 RW83 - [M]DQS, [M]DQ Training Modes Control Word

Table 70 — RW83: [M]DQS, [M]DQ Training Modes Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Normal operation	Exit any of the training mode
x	x	x	x	0	0	0	1	MRE	DRAM Interface Receive Enable Training
x	x	x	x	0	0	1	0	MRD	MDQS Read Delay Training
x	x	x	x	0	0	1	1	DWL	DRAM Write Leveling
x	x	x	x	0	1	0	0	MWD	MDQ Write Delay Training
x	x	x	x	0	1	0	1	HWL	Host Interface Write Leveling
x	x	x	x	0	1	1	0	HIR	Host Interface Read Training
x	x	x	x	0	1	1	1	Reserved	Reserved
x	x	x	x	1	0	0	0	Reserved	Reserved
x	x	x	0	x	x	x	x	HPA[1]	Host Preamble Training Mode disabled
x	x	x	1	x	x	x	x		Host Preamble Training Mode enabled
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. When HPA is enabled the DB ignores non-target read/MRR events

10.7 Timing and Voltage Control Words

10.7.1 RW84 - LRDIMM Operating Speed

Table 71 — RW84: LRDIMM Operating Speed[1,2]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Operating Speed	DDR5-3200 (2800 MT/s < f ≤ 3200 MT/s)
x	x	x	x	0	0	0	1		DDR5-3600 (3200 MT/s < f ≤ 3600 MT/s)
x	x	x	x	0	0	1	0		DDR5-4000 (3600 MT/s < f ≤ 4000 MT/s)
x	x	x	x	0	0	1	1		DDR5-4400 (4000 MT/s < f ≤ 4400 MT/s)
x	x	x	x	0	1	0	0		DDR5-4800 (4400 MT/s < f ≤ 4800 MT/s)
x	x	x	x	0	1	0	1		Reserved
x	x	x	x	0	1	1	0		Reserved
x	x	x	x	0	1	1	1		Reserved
x	x	x	x	1	0	0	0		Reserved
x	x	x	x	1	0	0	1		Reserved
x	x	x	x	1	0	1	0		Reserved
x	x	x	x	1	0	1	1		Reserved
x	x	x	x	1	1	0	0		Reserved
x	x	x	x	1	1	0	1		Reserved
x	x	x	x	1	1	1	0		DDR5-2100 (1980 MT/s ≤ f ≤ 2100 MT/s)[3]
x	x	x	x	1	1	1	1		Test Frequency Range (560 MT/s < f < 1980 MT/s)[4]
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Context for operation training	Default; Context 1 operation
x	1	x	x	x	x	x	x		Context 2 operation[5]
0	x	x	x	x	x	x	x	Buffer V_{DD} Operating Voltage[6]	1.1 V
1	x	x	x	x	x	x	x		Reserved

1. The encoding value is used to inform the data buffer the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a data buffer can run.
2. RW84[6] and RW84[3:0] will be sticky, cleared by power cycle not reset.
3. This setting may or may not support fractional delay settings, Fine Granularity DIMM Operating Speed Control, Per-Bit Read Delay, and will require a longer clock stabilization time.
4. Intended for Transparent mode only. RW84[3:0] shall be set to '1111' in order to guarantee PLL Lock when BCK is running in the Test frequency range (i.e., 280 MHz < f_{TEST} < 990 MHz).
5. The control words listed in Table 33 are duplicated by the DDR5DB01 for the 2nd frequency context.
6. RW84[7] will be used to inform DDR5DB01 under what operating voltage V_{DD} will be used. The Data Buffer can use the information to optimize functionality and performance at low-voltage conditions.

10.7.2 RW85 - Fine Granularity DIMM Operating Speed Control Word

Table 72 — RW85: Fine Granularity DIMM Operating Speed Control Word[1,2]

Setting								Definition	Encoding[3]
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Fine Granularity Operating Speed in terms of f_{bin}, where f_{bin} is the top speed for the speed range selected in RW84 OP[3:0]	(f_{bin} - 20 MT/s) < f ≤ f_{bin}
x	x	x	0	0	0	0	1		(f_{bin} - 40 MT/s) < f ≤ (f_{bin} - 20 MT/s)
x	x	x	0	0	0	1	0		(f_{bin} - 60 MT/s) < f ≤ (f_{bin} - 40 MT/s)
x	x	x	0	0	0	1	1		(f_{bin} - 80 MT/s) < f ≤ (f_{bin} - 60 MT/s)
x	x	x	0	0	1	0	0		(f_{bin} - 100 MT/s) < f ≤ (f_{bin} - 80 MT/s)
x	x	x	0	0	1	0	1		(f_{bin} - 120 MT/s) < f ≤ (f_{bin} - 100 MT/s)
x	x	x	0	0	1	1	0		(f_{bin} - 140 MT/s) < f ≤ (f_{bin} - 120 MT/s)
x	x	x	0	0	1	1	1		(f_{bin} - 160 MT/s) < f ≤ (f_{bin} - 140 MT/s)
x	x	x	0	1	0	0	0		(f_{bin} - 180 MT/s) < f ≤ (f_{bin} - 160 MT/s)
x	x	x	0	1	0	0	1		(f_{bin} - 200 MT/s) < f ≤ (f_{bin} - 180 MT/s)
x	x	x	0	1	0	1	0		(f_{bin} - 220 MT/s) < f ≤ (f_{bin} - 200 MT/s)
x	x	x	0	1	0	1	1		(f_{bin} - 240 MT/s) < f ≤ (f_{bin} - 220 MT/s)
x	x	x	0	1	1	0	0		(f_{bin} - 260 MT/s) < f ≤ (f_{bin} - 240 MT/s)
x	x	x	0	1	1	0	1		(f_{bin} - 280 MT/s) < f ≤ (f_{bin} - 260 MT/s)
x	x	x	0	1	1	1	0		(f_{bin} - 300 MT/s) < f ≤ (f_{bin} - 280 MT/s)
x	x	x	0	1	1	1	1		(f_{bin} - 320 MT/s) < f ≤ (f_{bin} - 300 MT/s)
x	x	x	1	0	0	0	0		(f_{bin} - 340 MT/s) < f ≤ (f_{bin} - 320 MT/s)
x	x	x	1	0	0	0	1		(f_{bin} - 360 MT/s) < f ≤ (f_{bin} - 340 MT/s)
x	x	x	1	0	0	1	0		(f_{bin} - 380 MT/s) < f ≤ (f_{bin} - 360 MT/s)
x	x	x	1	0	0	1	1		(f_{bin} - 400 MT/s) < f ≤ (f_{bin} - 380 MT/s)
x	x	x	1	0	1	0	0		Reserved
x	x	x	...						Reserved
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This control word defines the frequency of the BCK_t - BCK_c input reference clock during normal operation (i.e., when not in test frequency range) in units of 20 MT/s (i.e., 10 MHz).
2. RW85[4:0] will be sticky, cleared by power cycle not reset.
3. The frequency ranges shown in this column are for the base frequency of the input clock and they do not include SSC modulation effects. In some cases, due to SSC modulation, the actual frequency of the input clock can straddle two adjacent frequency ranges.

10.7.3 RW86 - DQS RTT Park Termination Control Word

Table 73 — RW86: DQS RTT Park Termination Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DQS_RTT_PARK	RTT_OFF (Default)
x	x	x	x	x	0	0	1		RZQ/1 (240 Ω)
x	x	x	x	x	0	1	0		RZQ/2 (120 Ω)
x	x	x	x	x	0	1	1		RZQ/3 (80 Ω)
x	x	x	x	x	1	0	0		RZQ/4 (60 Ω)
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω)
x	x	x	x	x	1	1	0		RZQ/6 (40 Ω)
x	x	x	x	x	1	1	1		RZQ/7 (34 Ω)
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW86[2:0] will be sticky, cleared by power cycle not reset

10.7.4 RW87 - Host Interface DQ RTT WR & Park Termination Control Word

Table 74 — RW87: Host Interface DQ RTT Termination Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DQ RTT_PARK	RTT_OFF Default
x	x	x	x	x	0	0	1		RZQ/1 (240 Ω)
x	x	x	x	x	0	1	0		RZQ/2 (120 Ω)
x	x	x	x	x	0	1	1		RZQ/3 (80 Ω)
x	x	x	x	x	1	0	0		RZQ/4 (60 Ω)
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω)
x	x	x	x	x	1	1	0		RZQ/6(40 Ω)
x	x	x	x	x	1	1	1		RZQ/7(34 Ω)
x	x	0	0	0	x	x	x	DQ RTT_WR	RTT_OFF Default
x	x	0	0	1	x	x	x		RZQ/1 (240 Ω)
x	x	0	1	0	x	x	x		RZQ/2 (120 Ω)
x	x	0	1	1	x	x	x		RZQ/3 (80 Ω)
x	x	1	0	0	x	x	x		RZQ/4 (60 Ω)
x	x	1	0	1	x	x	x		RZQ/5 (48 Ω)
x	x	1	1	0	x	x	x		RZQ/6 (40 Ω)
x	x	1	1	1	x	x	x		RZQ/7 (34 Ω)
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW87[5:0] will be sticky, cleared by power cycle not reset

10.7.5 RW88 - Host Interface DQ RTT NOM Termination Control Word

Table 75 — RW88: Host Interface DQ RTT NOM Termination Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DQ RTT_NOM_WR	RTT_OFF
x	x	x	x	x	0	0	1		RZQ/1 (240 Ω)
x	x	x	x	x	0	1	0		RZQ/2 (120 Ω)
x	x	x	x	x	0	1	1		RZQ/3 (80 Ω)
x	x	x	x	x	1	0	0		RZQ/4 (60 Ω) (default)
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω)
x	x	x	x	x	1	1	0		RZQ/6 (40 Ω)
x	x	x	x	x	1	1	1		RZQ/7 (34 Ω)
x	x	0	0	0	x	x	x	DQ RTT_NOM_RD	RTT_OFF
x	x	0	0	1	x	x	x		RZQ/1 (240 Ω)
x	x	0	1	0	x	x	x		RZQ/2 (120 Ω)
x	x	0	1	1	x	x	x		RZQ/3 (80 Ω)
x	x	1	0	0	x	x	x		RZQ/4 (60 Ω) (default)
x	x	1	0	1	x	x	x		RZQ/5 (48 Ω)
x	x	1	1	0	x	x	x		RZQ/6 (40 Ω)
x	x	1	1	1	x	x	x		RZQ/7 (34 Ω)
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW88[5:0] will be sticky, cleared by power cycle not reset

10.7.6 RW8A - Host Interface DQ Driver Control Word

Table 76 — RW8A: Host Interface DQ Driver Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Host Interface DQ/DQS Output Disable	Normal Operation -Default
x	x	x	x	x	x	x	1		Outputs Disabled
x	x	x	x	0	0	0	x	Host Interface DQ/DQS Output Driver Pull up Impedance control	RZQ/7 (34 Ω)
x	x	x	x	0	0	1	x		Reserved
x	x	x	x	0	1	0	x		RZQ/5 (48 Ω)
x	x	x	x	0	1	1	x		Reserved
x	x	x	x	1	0	0	x		Reserved
x	x	x	x	1	0	1	x		Reserved
x	x	x	x	1	1	0	x		Reserved
x	x	x	x	1	1	1	x		Reserved
x	0	0	0	x	x	x	x	Host Interface DQ/DQS Output Driver Pull Down Impedance control	RZQ/7 (34 Ω)
x	0	0	1	x	x	x	x		Reserved
x	0	1	0	x	x	x	x		RZQ/5 (48 Ω)
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW8A[6:0] will be sticky, cleared by power cycle not reset

10.7.7 RW8B - DRAM Interface MDQ Driver Control Word

Table 77 — RW8B: DRAM Interface MDQ Driver Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DRAM Interface MDQ/MDQS Output Disable	Normal Operation -Default
x	x	x	x	x	x	x	1		Outputs Disabled
x	x	x	x	0	0	0	x	DRAM Interface MDQ/MDQS Output Driver Pull up Impedance control	RZQ / 7 (34 Ω)
x	x	x	x	0	0	1	x		RZQ / 6 (40 Ω)
x	x	x	x	0	1	0	x		RZQ / 5 (48 Ω)
x	x	x	x	0	1	1	x		Reserved
x	x	x	x	1	0	0	x		Reserved
x	x	x	x	1	0	1	x		Reserved
x	x	x	x	1	1	0	x		Reserved
x	x	x	x	1	1	1	x		Reserved
x	0	0	0	x	x	x	x	DRAM Interface MDQ/MDQS Output Driver Pull Down Impedance control	RZQ / 7 (34 Ω)
x	0	0	1	x	x	x	x		RZQ / 6 (40 Ω)
x	0	1	0	x	x	x	x		RZQ / 5 (48 Ω)
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW8B[6:0] will be sticky, cleared by power cycle not reset

10.7.8 RW8C - MDQS and MDQ Park Termination Control Word

Table 78 — RW8C: MDQS and MDQ Park Termination Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	MDQS_RTT_PARK	RTT_OFF (Default)
x	x	x	x	x	0	0	1		RZQ/1 (240 Ω)
x	x	x	x	x	0	1	0		RZQ/2 (120 Ω)
x	x	x	x	x	0	1	1		RZQ/3 (80 Ω)
x	x	x	x	x	1	0	0		RZQ/4 (60 Ω)
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω)
x	x	x	x	x	1	1	0		RZQ/6 (40 Ω)
x	x	x	x	x	1	1	1		RZQ/7 (34 Ω)
x	x	0	0	0	x	x	x	MDQ_RTT_PARK	RTT_OFF (Default)
x	x	0	0	1	x	x	x		RZQ/1 (240 Ω)
x	x	0	1	0	x	x	x		RZQ/2 (120 Ω)
x	x	0	1	1	x	x	x		RZQ/3 (80 Ω)
x	x	1	0	0	x	x	x		RZQ/4 (60 Ω)
x	x	1	0	1	x	x	x		RZQ/5 (48 Ω)
x	x	1	1	0	x	x	x		RZQ/6 (40 Ω)
x	x	1	1	1	x	x	x		RZQ/7 (34 Ω)
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW8C[5:0] will be sticky, cleared by power cycle not reset

10.7.9 RW8D - Loopback Control Word

Table 79 — RW8D: Loopback Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Loopback Enabled	Loopback mode disabled (default)
x	x	x	x	x	x	x	1		Loopback mode Enabled
x	x	x	x	x	x	0	x	Loopback Output Mode[1]	DQS qualified output (default)[2]
x	x	x	x	x	x	1	x		WE qualified output[3]
x	x	x	0	0	0	x	x	DQ Loopback selection	DQ0 selected (default)
x	x	x	0	0	1	x	x		DQ1
x	x	x	0	1	0	x	x		DQ2
x	x	x	0	1	1	x	x		DQ3
x	x	x	1	0	0	x	x		DQ4
x	x	x	1	0	1	x	x		DQ5
x	x	x	1	1	0	x	x		DQ6
x	x	x	1	1	1	x	x		DQ7
x	x	0	x	x	x	x	x	Loopback Phase Select[4]	Phase A selected (default)
x	x	1	x	x	x	x	x		Phase B selected
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This bit configures the DB loopback output to either send data out every time the DQS toggles, or to only send it out when qualified with the write enable, so that only burst data is sent out via the loopback.
2. Since this mode does not support normal WR and RD commands, only DQ_RTT_PARK termination, if enabled, is available in DQ pins. DQS_RTT_PARK termination, if enabled, is available for DQS pins.
3. All termination features from normal operation available in DQ pins. DQS_RTT_PARK termination, if enabled, is available for DQS pins
4. DDR5DB01 supports 2-way interface only for loopback test. Phase A refers to UI D0, D2, D4, etc. Phase B refers to UI D1, D3, D5, etc.

10.7.10 RW8E- Loopback RTT and Ron Control Word

Table 80 — RW8E: Loopback RTT and Ron Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	RTT_Loopback	RTT_OFF
x	x	x	x	x	0	0	1		Reserved
x	x	x	x	x	0	1	0		Reserved
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω) Default
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved)
x	x	0	0	0	x	x	x	Loopback Driver Strength Settings	RZQ/7 (34 Ω) Default
x	x	0	0	1	x	x	x		RZQ/6 (40 Ω)
x	x	0	1	0	x	x	x		RZQ/5 (48 Ω)
x	x	0	1	1	x	x	x		Reserved
x	x	1	0	0	x	x	x		Reserved
x	x	1	0	1	x	x	x		Reserved
x	x	1	1	0	x	x	x		Reserved
x	x	1	1	1	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

10.7.11 RW8F - Host Interface Read DQS Offset Timing Control Word

Table 81 — RW8F: Host Interface Read DQS Offset Timing Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Host Interface DQS0 Pre-launch	0 tCK (DQS match DQ delay)
x	x	x	x	x	0	0	1		1 tCK
x	x	x	x	x	0	1	0		2 tCK
x	x	x	x	x	0	1	1		3 tCK
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		Reserved
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Host Interface DQS1 Pre-launch	0 tCK (DQS match DQ delay)
x	0	0	1	x	x	x	x		1 tCK
x	0	1	0	x	x	x	x		2 tCK
x	0	1	1	x	x	x	x		3 tCK
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW8F[6:4] and RW8F[2:0] will be sticky, cleared by power cycle not reset.

10.8 DQ Training Configuration

10.8.1 RW90 - Continuous Burst Mode Control Word

Table 82 — RW90: Continuous Burst Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Continuous Burst Mode Enable[1]	Mode disabled (default)
x	x	x	x	x	x	x	1		Mode enabled
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This feature is not intended to be used when the DRAM pattern generator is also enabled.

10.8.2 RW92 - PBA Enumerate ID Control Word

Table 83 — RW92: PBA Enumerate ID Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	PBA Set ID[2]	ID = 0
x	x	x	x	0	0	0	1		ID = 1
x	x	x	x	0	0	1	0		ID = 2
x	x	x	x	0	0	1	1		ID = 3
x	x	x	x	0	1	0	0		ID = 4
x	x	x	x	0	1	0	1		ID = 5
x	x	x	x	0	1	1	0		ID = 6
x	x	x	x	0	1	1	1		ID = 7
x	x	x	x	1	0	0	0		ID = 8
x	x	x	x	1	0	0	1		ID = 9
x	x	x	x	1	0	1	0		ID = 10
x	x	x	x	1	0	1	1		ID = 11
x	x	x	x	1	1	0	0		ID = 12
x	x	x	x	1	1	0	1		ID = 13
x	x	x	x	1	1	1	0		ID = 14
x	x	x	x	1	1	1	1		ID = 15 (default)
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW92[3:0] will be sticky, cleared by power cycle not reset
2. Only are written when PBA Enumerated Programing mode is enabled RW81[0] = 1.

10.8.3 RW93 - PBA Buffer Select ID Control Word

Table 84 — RW93: PBA Buffer Select ID Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	PBA Select ID[2]	ID = 0
x	x	x	x	0	0	0	1		ID = 1
x	x	x	x	0	0	1	0		ID = 2
x	x	x	x	0	0	1	1		ID = 3
x	x	x	x	0	1	0	0		ID = 4
x	x	x	x	0	1	0	1		ID = 5
x	x	x	x	0	1	1	0		ID = 6
x	x	x	x	0	1	1	1		ID = 7
x	x	x	x	1	0	0	0		ID = 8
x	x	x	x	1	0	0	1		ID = 9
x	x	x	x	1	0	1	0		ID = 10
x	x	x	x	1	0	1	1		ID = 11
x	x	x	x	1	1	0	0		ID = 12
x	x	x	x	1	1	0	1		ID = 13
x	x	x	x	1	1	1	0		ID = 14
x	x	x	x	1	1	1	1		ID = 15 Selects All Buffers (Default)
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RW93[3:0] will be sticky, cleared by power cycle not reset
2. Selects the data buffer or all data buffer to accept MRW command

10.8.4 RW[96:94] - Read-only register for the Internal Receive Enable Offset

Table 85 — RW[96:94]: Read-only register for the Internal Receive Enable Offset[1]

RW	Description	Encoding
RW94[3:0]	Internal Receive Enable Offset Coarse Status	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay
RW94[7:4]		Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay
RW95[5:0]	Internal Receive Enable Offset Fine Lower Nibble Status	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * tCK
RW96[5:0]	Internal Receive Enable Offset Fine Upper Nibble Status	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * tCK

1. RW[96:94]: are Read-only register for the Internal Receive Enable Offset

10.8.5 RW 97 - Buffer Training Configuration Control Word

Table 86 — RW97: Buffer Training Configuration Control Word

Settings (DA[7:0]								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Clear feedback status bit[1]	Default
x	x	x	x	x	x	x	1		Clear feedback status (all DQ feedback returns to HIGH)
x	x	x	x	x	x	0	x	Per UI Filtering	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	Long Read pattern sticky status feedback mode[2]	Enabled
x	x	x	x	x	1	x	x		Disabled
x	x	x	x	0	x	x	x	per-bit vs. per-transaction	Per-bit (default)
x	x	x	x	1	x	x	x		Per-transaction (per-nibble)
0	0	0	0	x	x	x	x	Select 1 of 16 UIs for Per UI Filtering	UI-0
0	0	0	1	x	x	x	x		UI-1
0	0	1	0	x	x	x	x		UI-2
0	0	1	1	x	x	x	x		UI-3
0	1	0	0	x	x	x	x		UI-4
0	1	0	1	x	x	x	x		UI-5
0	1	1	0	x	x	x	x		UI-6
0	1	1	1	x	x	x	x		UI-7
1	0	0	0	x	x	x	x		UI-8
1	0	0	1	x	x	x	x		UI-9
1	0	1	0	x	x	x	x		UI-10
1	0	1	1	x	x	x	x		UI-11
1	1	0	0	x	x	x	x		UI-12
1	1	0	1	x	x	x	x		UI-13
1	1	1	0	x	x	x	x		UI-14
1	1	1	1	x	x	x	x		UI-15

1. Set to 1 to clear feedback status (all DQ feedback returns to HIGH). This bit automatically returns to 0.
2. When Enabled, the host DQ feedback will hold any mis-compare output (i.e. continue driving LOW) until host sets the Clear Feedback Status bit in RW97[0]. After exiting the training mode (i.e., MRD or MWD), the feedback status will be removed from the DQ pins to support Read/Write normal operation. The DDR5DB01 hardware may clear the sticky status, but the host is required to set the Clear Feedback Status bit in RW97[0] to guarantee that the sticky status will not be carried over into a new (MRD or MWD) training mode entry. When Disabled, the host DQ feedback will change with each RD burst, depending on the comparison result. If only a single RD occurs and there is a mis-compare, the DQ feedback will still hold a LOW value until the next RD, or when the host sets the “Clear Feedback Status” bit.

10.8.6 RW98 - Buffer Training Status Word

This control word contains status information that indicates the result of certain training modes.

The state of each bit in the Buffer Training Status Word must be preserved when the DDR5DB01 enters or exits any training mode. This is needed because in most cases the data buffer needs to be taken out of training mode before the host controller can access the Buffer Training Status Word by means of MRR commands. The DDR5DB01 hardware should only update the state of the Buffer Training Status Word when a new result is generated by the corresponding training logic.

Table 87 — RW98: Buffer Training Status Word[1, 2]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ 0 status	DQ status based on previous Read comparison
x	x	x	x	x	x	x	1		
x	x	x	x	x	x	0	x	DQ 1 status	
x	x	x	x	x	x	1	x		
x	x	x	x	x	0	x	x	DQ 2 status	
x	x	x	x	x	1	x	x		
x	x	x	x	0	x	x	x	DQ 3 status	
x	x	x	x	1	x	x	x		
x	x	x	0	x	x	x	x	DQ 4 status	
x	x	x	1	x	x	x	x		
x	x	0	x	x	x	x	x	DQ 5 status	
x	x	1	x	x	x	x	x		
x	0	x	x	x	x	x	x	DQ 6 status	
x	1	x	x	x	x	x	x		
0	x	x	x	x	x	x	x	DQ 7 status	
1	x	x	x	x	x	x	x		

1. The Training Status should always report per-DQ results per MRR or Read command (i.e. update the status register even if Long Read pattern sticky status is enabled) and should represent the results for the UI filtering setting in RW97.
2. RW98 gets cleared with RESET strap command (BRST_n assertion pulse with BCOM[2:0] driven All HIGH or All LOW) and power cycle or when the Clear Feedback Status bit in RW97[0] is set to 1.

10.8.7 RW[9F:9C] Read and Write LFSR State Monitors

Table 88 — RW[9F:99] Read and Write LFSR State Monitors

RW	Description	Encoding
RW9C[7:0]	READ LFSR0 State Monitor (Read Only)	The current state of READ LFSR0
RW9D[7:0]	READ LFSR1 State Monitor (Read Only)	The current state of READ LFSR1
RW9E[7:0]	WRITE LFSR0 State Monitor (Read Only)	The current state of WRITE LFSR0
RW9F[7:0]	WRITE LFSR1 State Monitor (Read Only)	The current state of WRITE LFSR1

10.9 DFE Control Words

10.9.1 RWA0 DFE Control Word.

Table 89 — RWA0: DFE Control Word Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Feature Enable [2]	DFE and gain features Disabled (Default)
x	x	x	x	x	x	x	1		DFE and gain features Enabled
x	x	x	x	x	x	0	x	DFE_Vref Enable[3]	DFE_Vref Circuitry Disabled
x	x	x	x	x	x	1	x		DFE_Vref Circuitry Enabled
x	x	x	x	x	0	x	x	ERROR Counter Enable	All ERROR Counters Disable
x	x	x	x	x	1	x	x		All ERROR Counters Enabled
x	x	x	x	0	x	x	x	RW Control Word Writes Broadcasted[4]	RW Write to select DQn
x	x	x	x	1	x	x	x		RW Writes Broadcast to DQ[7:0]
x	x	x	0	x	x	x	x	Tap 1 Enable Bit for all DQ[7:0]	(Default) Tap 1 disabled
x	x	x	1	x	x	x	x		Tap 1 enabled
x	x	0	x	x	x	x	x	Tap 2 Enable Bit for all DQ[7:0]	(Default) Tap 2 disabled
x	x	1	x	x	x	x	x		Tap 2 enabled
x	0	x	x	x	x	x	x	Tap 3 Enable Bit for all DQ[7:0]	(Default) Tap 3 disabled
x	1	x	x	x	x	x	x		Tap 3 enabled
0	x	x	x	x	x	x	x	Tap 4 Enable Bit for all DQ[7:0]	(Default) Tap 4 disabled
1	x	x	x	x	x	x	x		Tap 4 enabled

1. RWA0[7:0] will be sticky, cleared by power cycle not reset
2. This control bit enables DFE circuitry in the Data Buffer
3. To save power the host can disable the DFE_Vref Circuitry when not in use.
4. When this bit is enabled, DFE RW Control Word Writes are broadcasted to all DQ pins which are selected for DFE training in RWA2.

10.9.2 RWA1 - DQ[7:0] DFE Training Mode Control Word

Table 90 — RWA1 - DQ[7:0] DFE Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Global DFE Training Mode Enable [,1]	DFE Training Mode disabled
x	x	x	x	x	x	x	1		DFE Training Mode enabled[2,3,]
x	x	x	x	x	0	0	x	Training Source	Monitor
x	x	x	x	x	0	1	x		Monitor XOR Slicer Output
x	x	x	x	x	1	0	x		Reserved
x	x	x	x	x	1	1	x		Reserved
x	x	x	x	0	x	x	x	DFE Error Counter Reset	Normal Operation
x	x	x	x	1	x	x	x		Resets upper and lower Error counters
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RWA2[7:0] determines the target receiver for DFE training.
2. DFE circuits are configured into training mode for selected pin RWA2.
3. Vref generator circuits are configured so that a DFE training reference voltage (DFE_Vref) is controlled by PG[6]RW[E2, E3, E6, E7, EA, EB, EE, EF, F2, F3, F6, F7, FA, FB, FE, FF].

10.9.3 RWA2 - DQn DFE pin selection Control Word

Table 91 — RWA2 - DQn DFE pin selection Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQn DFE pin selection [1]	DQ0 - Not Selected
x	x	x	x	x	x	x	1		DQ0 - Selected
x	x	x	x	x	x	0	x		DQ1 - Not Selected
x	x	x	x	x	x	1	x		DQ1 - Selected
x	x	x	x	x	0	x	x		DQ2 - Not Selected
x	x	x	x	x	1	x	x		DQ2 - Selected
x	x	x	x	0	x	x	x		DQ3 - Not Selected
x	x	x	x	1	x	x	x		DQ3 - Selected
x	x	x	0	x	x	x	x		DQ4 - Not Selected
x	x	x	1	x	x	x	x		DQ4 - Selected
x	x	0	x	x	x	x	x		DQ5 - Not Selected
x	x	1	x	x	x	x	x		DQ5 - Selected
x	0	x	x	x	x	x	x		DQ6 - Not Selected
x	1	x	x	x	x	x	x		DQ6 - Selected
0	x	x	x	x	x	x	x		DQ7 - Not Selected
1	x	x	x	x	x	x	x		DQ7 - Selected

1. RWA2[7:0] determines the target receivers for DFE training.

10.10 Periodic Update Control Words

10.10.1 RWB0: DRAM tDQS2DQ Tracking Control Word

Table 92 — RWB0: DRAM tDQS2DQ Tracking Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Tracking mode	DRAM tDQS2DQ tracking initialization mode enabled (default)
x	x	x	x	x	x	x	1		DRAM tDQS2DQ tracking mode enabled[1]
x	x	x	x	x	x	0	x	Clear all Tracking RWs in Page A[2]	Normal operation
x	x	x	x	x	x	1	x		All periodic control words are reset to zero. [3]
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RWB0[0] will be sticky, cleared by power cycle not reset.
2. RWB0[1] will only reset the PG[A] current context registers
3. This applies to PG[A]RW[FF:E0] control words. When this bit is set, all periodic control words are reset to zero. This bit is self-clearing in the next cycle.

10.10.2 RWB1: DRAM tDQS2DQ Tracking Return Value Control Word

Table 93 — RWB1: DRAM tDQS2DQ Tracking Return Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	x	DRAM tDQS2DQ Tracking Return Value[1,2]	Whenever there is a DRAM MRR to MR46 or MR47 the DB will return the value from this register. This register defaults to 8'h00.

1. The host will program this register prior to DRAM tDQS2DQ tracking initialization mode or DRAM tDQS2DQ tracking mode or any access to DRAM MR46 or MR47.
2. RWB1 will be sticky, cleared by power cycle not reset

10.11 Paging Control Words

10.11.1 RWDF - CW Page Control Word

Table 94 — RWDF- CW Page Control Word

Page Control Register[1,]							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0

1. Power on Default is OP[7:0] = 0.

10.12 Paged [M]DQS/[M]DQ Training Support Control Words

10.12.1 PG [1:0] RWE0 - Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for all Ranks

The lower 4 bits of this control word is for the additional cycles of trained receive enable timing on the lower nibble (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble (MDQS1_t/MDQS1_c).

Table 95 — PG [1:0] RWE0: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for all Ranks[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay[2]	0 nCK receive enable timing latency adder.
x	x	x	x	0	0	0	1		+1 nCK receive enable timing latency adder
x	x	x	x	0	0	1	0		+2 nCK receive enable timing latency adder
x	x	x	x	0	0	1	1		+3 nCK receive enable timing latency adder
x	x	x	x	0	1	0	0		+4 nCK receive enable timing latency adder
x	x	x	x	0	1	0	1		Reserved
x	x	x	x	...					Reserved
x	x	x	x	1	0	0	0		Reserved
x	x	x	x	1	0	0	1		-1 nCK receive enable timing latency adder
x	x	x	x	1	0	1	0		-2 nCK receive enable timing latency adder
x	x	x	x	1	0	1	1		-3 nCK receive enable timing latency adder
x	x	x	x	1	1	0	0		-4 nCK receive enable timing latency adder
x	x	x	x	1	1	0	1		Reserved
x	x	x	x	...					Reserved
x	x	x	x	1	1	1	1		Reserved
0	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay[2]	0 nCK receive enable timing latency adder.
0	0	0	1	x	x	x	x		+1 nCK receive enable timing latency adder
0	0	1	0	x	x	x	x		+2 nCK receive enable timing latency adder
0	0	1	1	x	x	x	x		+3 nCK receive enable timing latency adder
0	1	0	0	x	x	x	x		+4 nCK receive enable timing latency adder
0	1	0	1	x	x	x	x		Reserved
...				x	x	x	x		Reserved
1	0	0	0	x	x	x	x		Reserved
1	0	0	1	x	x	x	x		-1 nCK receive enable timing latency adder
1	0	1	0	x	x	x	x		-2 nCK receive enable timing latency adder
1	0	1	1	x	x	x	x		-3 nCK receive enable timing latency adder
1	1	0	0	x	x	x	x		-4 nCK receive enable timing latency adder
1	1	0	1	x	x	x	x		Reserved
...				x	x	x	x		Reserved
1	1	1	1	x	x	x	x		Reserved

1. PG[1:0]RWE0 will be sticky, cleared by power cycle not reset.
2. The baseline delay includes the snooped values for CL.

10.12.2 PG [1:0] RWE1 - Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word

The lower 4 bits of this control word is for the additional cycles of trained write leveling timing on the lower nibble of Rank [1:0] (MDQS0_t/MDQS0_c) and upper 4 bits of this control word is for the upper nibble of Rank [1:0] (MDQS1_t/MDQS1_c).

Table 96 — PG [1:0] RWE1: Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Write Leveling Delay[2]	0 nCK write leveling timing latency adder.
x	x	x	x	0	0	0	1		+1 nCK write leveling timing latency adder
x	x	x	x	0	0	1	0		+2 nCK write leveling timing latency adder
x	x	x	x	0	0	1	1		+3 nCK write leveling timing latency adder
x	x	x	x	0	1	0	0		+4 nCK write leveling timing latency adder
x	x	x	x	0	1	0	1		Reserved
x	x	x	x	...					Reserved
x	x	x	x	1	0	0	0		Reserved
x	x	x	x	1	0	0	1		-1 nCK write leveling timing latency adder
x	x	x	x	1	0	1	0		-2 nCK write leveling timing latency adder
x	x	x	x	1	0	1	1		-3 nCK write leveling timing latency adder
x	x	x	x	1	1	0	0		-4 nCK write leveling timing latency adder
x	x	x	x	1	1	0	1		Reserved
x	x	x	x	...					Reserved
x	x	x	x	1	1	1	1		Reserved
0	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Write Leveling Delay[2]	0 nCK write leveling timing latency adder.
0	0	0	1	x	x	x	x		+1 nCK write leveling timing latency adder
0	0	1	0	x	x	x	x		+2 nCK write leveling timing latency adder
0	0	1	1	x	x	x	x		+3 nCK write leveling timing latency adder
0	1	0	0	x	x	x	x		+4 nCK write leveling timing latency adder
0	1	0	1	x	x	x	x		Reserved
...				x	x	x	x		Reserved
1	0	0	0	x	x	x	x		Reserved
1	0	0	1	x	x	x	x		-1 nCK write leveling timing latency adder
1	0	1	0	x	x	x	x		-2 nCK write leveling timing latency adder
1	0	1	1	x	x	x	x		-3 nCK write leveling timing latency adder
1	1	0	0	x	x	x	x		-4 nCK write leveling timing latency adder
1	1	0	1	x	x	x	x		Reserved
...				x	x	x	x		Reserved
1	1	1	1	x	x	x	x		Reserved

1. PG[1:0]RWE1 will be sticky, cleared by power cycle not reset.
2. The baseline delay includes the snooped values for CWL.

10.12.3 PG [1:0] RWE2 - Lower/Upper Nibble DRAM Interface Receive Enable Training Control Word (per rank)

There are two 8-bit control words for the trained receive enable timing on the lower nibble of the DRAM interface (MDQS0_t/MDQS0_c) and two 8-bit control words for the upper nibble (MDQS1_t/MDQS1_c).

Table 97 — PG [1:0] RWE2: Lower Nibble DRAM Interface Receive Enable Training Control Word (per rank)[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS receive enable timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS receive enable timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS receive enable timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS receive enable timing by (3/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS receive enable timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS receive enable timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS receive enable timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS receive enable timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

1. PG[1:0]RWE2 will be sticky, cleared by power cycle not reset.

10.12.4 PG [1:0] RWE3 - Upper Nibble DRAM Interface Receive Enable Training Control Word (per rank)

Table 98 — PG [1:0] RWE3: Upper Nibble DRAM Interface Receive Enable Training Control Word (per rank)[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS receive enable timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS receive enable timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS receive enable timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS receive enable timing by (3/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS receive enable timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS receive enable timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS receive enable timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS receive enable timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

1. PG[1:0]RWE3 will be sticky, cleared by power cycle not reset.

10.12.5 PG [1:0] RWE4 - Lower Nibble MDQS Read Delay Control Word

Table 99 — PG [1:0] RWE4: Lower Nibble MDQS Read Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Lower Nibble MDQS Delay Control During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQS by $t_{CK}/4$ (Default)
x	x	x	0	0	0	0	1		Delay MDQS by $t_{CK}/4$ + (1/64) * t_{CK}
x	x	x	0	0	0	1	0		Delay MDQS by $t_{CK}/4$ + (2/64) * t_{CK}
x	x	x	0	0	0	1	1		Delay MDQS by $t_{CK}/4$ + (3/64) * t_{CK}
x	x	x	0	0	1	0	0		Delay MDQS by $t_{CK}/4$ + (4/64) * t_{CK}
x	x	x	0	0	1	0	1		Delay MDQS by $t_{CK}/4$ + (5/64) * t_{CK}
x	x	x	0	0	1	1	0		Delay MDQS by $t_{CK}/4$ + (6/64) * t_{CK}
x	x	x	0	0	1	1	1		Delay MDQS by $t_{CK}/4$ + (7/64) * t_{CK}
x	x	x	0	1	0	0	0		Delay MDQS by $t_{CK}/4$ + (8/64) * t_{CK}
x	x	x	0	1	0	0	1		Delay MDQS by $t_{CK}/4$ + (9/64) * t_{CK}
x	x	x	0	1	0	1	0		Delay MDQS by $t_{CK}/4$ + (10/64) * t_{CK}
x	x	x	0	1	0	1	1		Delay MDQS by $t_{CK}/4$ + (11/64) * t_{CK}
x	x	x	0	1	1	0	0		Delay MDQS by $t_{CK}/4$ + (12/64) * t_{CK}
x	x	x	0	1	1	0	1		Delay MDQS by $t_{CK}/4$ + (13/64) * t_{CK}
x	x	x	0	1	1	1	0		Delay MDQS by $t_{CK}/4$ + (14/64) * t_{CK}
x	x	x	0	1	1	1	1		Delay MDQS by $t_{CK}/4$ + (15/64) * t_{CK}
x	x	x	1	0	0	0	0		Delay MDQS by $t_{CK}/4$ (same as default)
x	x	x	1	0	0	0	1		Delay MDQS by $t_{CK}/4$ - (1/64) * t_{CK}
x	x	x	1	0	0	1	0		Delay MDQS by $t_{CK}/4$ - (2/64) * t_{CK}
x	x	x	1	0	0	1	1		Delay MDQS by $t_{CK}/4$ - (3/64) * t_{CK}
x	x	x	1	0	1	0	0		Delay MDQS by $t_{CK}/4$ - (4/64) * t_{CK}
x	x	x	1	0	1	0	1		Delay MDQS by $t_{CK}/4$ - (5/64) * t_{CK}
x	x	x	1	0	1	1	0		Delay MDQS by $t_{CK}/4$ - (6/64) * t_{CK}
x	x	x	1	0	1	1	1		Delay MDQS by $t_{CK}/4$ - (7/64) * t_{CK}
x	x	x	1	1	0	0	0		Delay MDQS by $t_{CK}/4$ - (8/64) * t_{CK}
x	x	x	1	1	0	0	1		Delay MDQS by $t_{CK}/4$ - (9/64) * t_{CK}
x	x	x	1	1	0	1	0		Delay MDQS by $t_{CK}/4$ - (10/64) * t_{CK}
x	x	x	1	1	0	1	1		Delay MDQS by $t_{CK}/4$ - (11/64) * t_{CK}
x	x	x	1	1	1	0	0		Delay MDQS by $t_{CK}/4$ - (12/64) * t_{CK}
x	x	x	1	1	1	0	1		Delay MDQS by $t_{CK}/4$ - (13/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay MDQS by $t_{CK}/4$ - (14/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay MDQS by $t_{CK}/4$ - (15/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWE4 will be sticky, cleared by power cycle not reset.
2. By default, the delay of MDQS signals received by the DDR5DB01 during read commands is tCK/4. The PG [1:0] RWE4 control bits can be used by the host to adjust this lower nibble delay to a more optimal position.

10.12.6 PG [1:0] RWE5 - Upper Nibble MDQS Read Delay Control Word

Table 100 — PG [1:0] RWE5: Upper Nibble MDQS Read Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Upper Nibble MDQS Delay Control During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQS by $t_{CK}/4$ (Default)
x	x	x	0	0	0	0	1		Delay MDQS by $t_{CK}/4$ + (1/64) * t_{CK}
x	x	x	0	0	0	1	0		Delay MDQS by $t_{CK}/4$ + (2/64) * t_{CK}
x	x	x	0	0	0	1	1		Delay MDQS by $t_{CK}/4$ + (3/64) * t_{CK}
x	x	x	0	0	1	0	0		Delay MDQS by $t_{CK}/4$ + (4/64) * t_{CK}
x	x	x	0	0	1	0	1		Delay MDQS by $t_{CK}/4$ + (5/64) * t_{CK}
x	x	x	0	0	1	1	0		Delay MDQS by $t_{CK}/4$ + (6/64) * t_{CK}
x	x	x	0	0	1	1	1		Delay MDQS by $t_{CK}/4$ + (7/64) * t_{CK}
x	x	x	0	1	0	0	0		Delay MDQS by $t_{CK}/4$ + (8/64) * t_{CK}
x	x	x	0	1	0	0	1		Delay MDQS by $t_{CK}/4$ + (9/64) * t_{CK}
x	x	x	0	1	0	1	0		Delay MDQS by $t_{CK}/4$ + (10/64) * t_{CK}
x	x	x	0	1	0	1	1		Delay MDQS by $t_{CK}/4$ + (11/64) * t_{CK}
x	x	x	0	1	1	0	0		Delay MDQS by $t_{CK}/4$ + (12/64) * t_{CK}
x	x	x	0	1	1	0	1		Delay MDQS by $t_{CK}/4$ + (13/64) * t_{CK}
x	x	x	0	1	1	1	0		Delay MDQS by $t_{CK}/4$ + (14/64) * t_{CK}
x	x	x	0	1	1	1	1		Delay MDQS by $t_{CK}/4$ + (15/64) * t_{CK}
x	x	x	1	0	0	0	0		Delay MDQS by $t_{CK}/4$ (same as default)
x	x	x	1	0	0	0	1		Delay MDQS by $t_{CK}/4$ - (1/64) * t_{CK}
x	x	x	1	0	0	1	0		Delay MDQS by $t_{CK}/4$ - (2/64) * t_{CK}
x	x	x	1	0	0	1	1		Delay MDQS by $t_{CK}/4$ - (3/64) * t_{CK}
x	x	x	1	0	1	0	0		Delay MDQS by $t_{CK}/4$ - (4/64) * t_{CK}
x	x	x	1	0	1	0	1		Delay MDQS by $t_{CK}/4$ - (5/64) * t_{CK}
x	x	x	1	0	1	1	0		Delay MDQS by $t_{CK}/4$ - (6/64) * t_{CK}
x	x	x	1	0	1	1	1		Delay MDQS by $t_{CK}/4$ - (7/64) * t_{CK}
x	x	x	1	1	0	0	0		Delay MDQS by $t_{CK}/4$ - (8/64) * t_{CK}
x	x	x	1	1	0	0	1		Delay MDQS by $t_{CK}/4$ - (9/64) * t_{CK}
x	x	x	1	1	0	1	0		Delay MDQS by $t_{CK}/4$ - (10/64) * t_{CK}
x	x	x	1	1	0	1	1		Delay MDQS by $t_{CK}/4$ - (11/64) * t_{CK}
x	x	x	1	1	1	0	0		Delay MDQS by $t_{CK}/4$ - (12/64) * t_{CK}
x	x	x	1	1	1	0	1		Delay MDQS by $t_{CK}/4$ - (13/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay MDQS by $t_{CK}/4$ - (14/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay MDQS by $t_{CK}/4$ - (15/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWE5 will be sticky, cleared by power cycle not reset.
2. By default, the delay of MDQS signals received by the DDR5DB01 during read commands is tCK/4. The PG [1:0] RWE5 control bits can be used by the host to adjust this upper nibble delay to a more optimal position.

10.12.7 PG [1:0] RWE6 - Lower Nibble MDQ Write Baseline Delay Control Word

Table 101 — PG [1:0] RWE6: Lower Nibble MDQ Write Baseline Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Phase Control for Lower Nibble MDQ with respect to MDQS_t During Write Transactions in Steps of (1/64) * t_{CK}[2,3]	MDQ phase delay = - t_{CK}/2
0	0	0	0	0	0	0	1		MDQ phase delay = - t_{CK}/2 + (1/64) * t_{CK}
0	0	0	0	0	0	1	0		MDQ phase delay = - t_{CK}/2 + (2/64) * t_{CK}
0	0	0	0	0	0	1	1		MDQ phase delay = - t_{CK}/2 + (3/64) * t_{CK}
0	0	0	0	0	1	0	0		MDQ phase delay = - t_{CK}/2 + (4/64) * t_{CK}
0	0	0	0	0	1	0	1		MDQ phase delay = - t_{CK}/2 + (5/64) * t_{CK}
0	0	0	0	0	1	1	0		MDQ phase delay = - t_{CK}/2 + (6/64) * t_{CK}
0	0	0	0	0	1	1	1		MDQ phase delay = - t_{CK}/2 + (7/64) * t_{CK}
0	0	0	0	1	0	0	0		MDQ phase delay = - t_{CK}/2 + (8/64) * t_{CK}
0	0	0	0	1	0	0	1		MDQ phase delay = - t_{CK}/2 + (9/64) * t_{CK}
0	0	0	0	1	0	1	0		MDQ phase delay = - t_{CK}/2 + (10/64) * t_{CK}
0	0	0	0	1	0	1	1		MDQ phase delay = - t_{CK}/2 + (11/64) * t_{CK}
0	0	0	0	1	1	0	0		MDQ phase delay = - t_{CK}/2 + (12/64) * t_{CK}
0	0	0	0	1	1	0	1		MDQ phase delay = - t_{CK}/2 + (13/64) * t_{CK}
0	0	0	0	1	1	1	0		MDQ phase delay = - t_{CK}/2 + (14/64) * t_{CK}
0	0	0	0	1	1	1	1		MDQ phase delay = - t_{CK}/2 + (15/64) * t_{CK}
0	0	0	1	0	0	0	0		MDQ phase delay = - t_{CK}/2 + (16/64) Default
...									...
...									...
...									...
1	1	1	1	0	0	0	1		MDQ phase delay = - t_{CK}/2 + (241/64) * t_{CK}
1	1	1	1	0	0	1	0		MDQ phase delay = - t_{CK}/2 + (242/64) * t_{CK}
1	1	1	1	0	0	1	1		MDQ phase delay = - t_{CK}/2 + (243/64) * t_{CK}
1	1	1	1	0	1	0	0		MDQ phase delay = - t_{CK}/2 + (244/64) * t_{CK}
1	1	1	1	0	1	0	1		MDQ phase delay = - t_{CK}/2 + (245/64) * t_{CK}
1	1	1	1	0	1	1	0		MDQ phase delay = - t_{CK}/2 + (246/64) * t_{CK}
1	1	1	1	0	1	1	1		MDQ phase delay = - t_{CK}/2 + (247/64) * t_{CK}
1	1	1	1	1	0	0	0		MDQ phase delay = - t_{CK}/2 + (248/64) * t_{CK}
1	1	1	1	1	0	0	1		MDQ phase delay = - t_{CK}/2 + (249/64) * t_{CK}
1	1	1	1	1	0	1	0		MDQ phase delay = - t_{CK}/2 + (250/64) * t_{CK}
1	1	1	1	1	0	1	1		MDQ phase delay = - t_{CK}/2 + (251/64) * t_{CK}
1	1	1	1	1	1	0	0		MDQ phase delay = - t_{CK}/2 + (252/64) * t_{CK}
1	1	1	1	1	1	0	1		MDQ phase delay = - t_{CK}/2 + (253/64) * t_{CK}
1	1	1	1	1	1	1	0		MDQ phase delay = - t_{CK}/2 + (254/64) * t_{CK}
1	1	1	1	1	1	1	1		MDQ phase delay = - t_{CK}/2 + (255/64) * t_{CK}

1. PG[1:0]RWE6 will be sticky, cleared by power cycle not reset.
2. By default, the phase between the MDQ and MDQS signals driven by the DDR5DB01 during write commands is t_{CK}/4, meaning MDQ is "tCK/4" earlier than MDQS. The PG [1:0] RWE6 control bits can be used by the host to adjust the phase relationship between lower nibble MDQ and MDQS to a more optimal position.
3. MDQ needs to be delayed instead of MDQS since the MDQS phase is fixed after write leveling.

10.12.8 PG [1:0] RWE7 - Upper Nibble MDQ Write Baseline Delay Control Word

Table 102 — PG [1:0] RWE7: Upper Nibble MDQ Write Baseline Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Phase Control for Upper Nibble MDQ with respect to MDQS_t During Write Transactions in Steps of (1/64) * t_{CK}[2,3]	MDQ phase delay = - t_{CK}/2
0	0	0	0	0	0	0	1		MDQ phase delay = - t_{CK}/2 + (1/64) * t_{CK}
0	0	0	0	0	0	1	0		MDQ phase delay = - t_{CK}/2 + (2/64) * t_{CK}
0	0	0	0	0	0	1	1		MDQ phase delay = - t_{CK}/2 + (3/64) * t_{CK}
0	0	0	0	0	1	0	0		MDQ phase delay = - t_{CK}/2 + (4/64) * t_{CK}
0	0	0	0	0	1	0	1		MDQ phase delay = - t_{CK}/2 + (5/64) * t_{CK}
0	0	0	0	0	1	1	0		MDQ phase delay = - t_{CK}/2 + (6/64) * t_{CK}
0	0	0	0	0	1	1	1		MDQ phase delay = - t_{CK}/2 + (7/64) * t_{CK}
0	0	0	0	1	0	0	0		MDQ phase delay = - t_{CK}/2 + (8/64) * t_{CK}
0	0	0	0	1	0	0	1		MDQ phase delay = - t_{CK}/2 + (9/64) * t_{CK}
0	0	0	0	1	0	1	0		MDQ phase delay = - t_{CK}/2 + (10/64) * t_{CK}
0	0	0	0	1	0	1	1		MDQ phase delay = - t_{CK}/2 + (11/64) * t_{CK}
0	0	0	0	1	1	0	0		MDQ phase delay = - t_{CK}/2 + (12/64) * t_{CK}
0	0	0	0	1	1	0	1		MDQ phase delay = - t_{CK}/2 + (13/64) * t_{CK}
0	0	0	0	1	1	1	0		MDQ phase delay = - t_{CK}/2 + (14/64) * t_{CK}
0	0	0	0	1	1	1	1		MDQ phase delay = - t_{CK}/2 + (15/64) * t_{CK}
0	0	0	1	0	0	0	0		MDQ phase delay = - t_{CK}/2 + (16/64) Default
...									...
...									...
...									...
1	1	1	1	0	0	0	1		MDQ phase delay = - t_{CK}/2 + (241/64) * t_{CK}
1	1	1	1	0	0	1	0		MDQ phase delay = - t_{CK}/2 + (242/64) * t_{CK}
1	1	1	1	0	0	1	1		MDQ phase delay = - t_{CK}/2 + (243/64) * t_{CK}
1	1	1	1	0	1	0	0		MDQ phase delay = - t_{CK}/2 + (244/64) * t_{CK}
1	1	1	1	0	1	0	1		MDQ phase delay = - t_{CK}/2 + (245/64) * t_{CK}
1	1	1	1	0	1	1	0		MDQ phase delay = - t_{CK}/2 + (246/64) * t_{CK}
1	1	1	1	0	1	1	1		MDQ phase delay = - t_{CK}/2 + (247/64) * t_{CK}
1	1	1	1	1	0	0	0		MDQ phase delay = - t_{CK}/2 + (248/64) * t_{CK}
1	1	1	1	1	0	0	1		MDQ phase delay = - t_{CK}/2 + (249/64) * t_{CK}
1	1	1	1	1	0	1	0		MDQ phase delay = - t_{CK}/2 + (250/64) * t_{CK}
1	1	1	1	1	0	1	1		MDQ phase delay = - t_{CK}/2 + (251/64) * t_{CK}
1	1	1	1	1	1	0	0		MDQ phase delay = - t_{CK}/2 + (252/64) * t_{CK}
1	1	1	1	1	1	0	1		MDQ phase delay = - t_{CK}/2 + (253/64) * t_{CK}
1	1	1	1	1	1	1	0		MDQ phase delay = - t_{CK}/2 + (254/64) * t_{CK}
1	1	1	1	1	1	1	1		MDQ phase delay = - t_{CK}/2 + (255/64) * t_{CK}

1. PG[1:0]RWE7 will be sticky, cleared by power cycle not reset.
2. By default, the phase between the MDQ and MDQS signals driven by the DDR5DB01 during write commands is t_{CK}/4, meaning MDQ is "tCK/4" earlier than MDQS. The PG [1:0] RWE7 control bits can be used by the host to adjust the phase relationship between upper nibble MDQ and MDQS to a more optimal position.
3. MDQ needs to be delayed instead of MDQS since the MDQS phase is fixed after write leveling.

10.12.9 PG [1:0] RWE8 - Lower/Upper Nibble DRAM Interface Write Leveling Control Word (per rank)

There are two 8-bit control words for the trained write leveling timing on the lower nibble of the DRAM interface (MDQS0_t/MDQS0_c) and two 8-bit control words for the upper nibble (MDQS1_t/MDQS1_c).

Table 103 — PG [1:0] RWE8: Lower Nibble DRAM Interface Write Leveling Control Word (per rank)[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Write Leveling Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS write leveling timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS write leveling timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS write leveling timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS write leveling timing by (3/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS write leveling timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS write leveling timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS write leveling timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS write leveling timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

1. PG[1:0]RWE8 will be sticky, cleared by power cycle not reset.

10.12.10 PG [1:0] RWE9 - Upper Nibble DRAM Interface Write Leveling Control Word (per rank)

Table 104 — PG [1:0] RWE9: Upper Nibble DRAM Interface Write Leveling Control Word (per rank)[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Write Leveling Timing Phase Control in Steps of (1/64) * t_{CK}	Delay MDQS write leveling timing by (0/64) * t_{CK}
x	x	0	0	0	0	0	1		Delay MDQS write leveling timing by (1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay MDQS write leveling timing by (2/64) * t_{CK}
x	x	0	0	0	0	1	1		Delay MDQS write leveling timing by (3/64) * t_{CK}
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS write leveling timing by (60/64) * t_{CK}
x	x	1	1	1	1	0	1		Delay MDQS write leveling timing by (61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay MDQS write leveling timing by (62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay MDQS write leveling timing by (63/64) * t_{CK}
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

1. PG[1:0]RWE9 will be sticky, cleared by power cycle not reset.

10.12.11 PG [1:0] RWEA- MDQ0/4 Read Delay Control Word

The control word location PG[1:0]RWEA is used to store per lane precise delay adjustment for MDQ0 and MDQ4 relative to the whole nibble delays in PG [1:0]RW[E5:E4].

Table 105 — PG [1:0] RWEA: MDQ0/4 Read Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ0 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ0 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ0 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ0 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ0 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ0 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ0 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ0 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ0 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ4 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ4 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ4 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWEA will be sticky, cleared by power cycle not reset.
2. The delay of the lower nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E4]. The PG [1:0] RWEA[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ0 lane relative to the lower nibble baseline delay for a more optimal position.
3. The delay of the upper nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E5]. The PG [1:0] RWEA[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ4 lane relative to the upper nibble baseline delay for a more optimal position.

10.12.12 PG [1:0] RWEB- MDQ1/5 Read Delay Control Word

The control word location PG[1:0]RWEB is used to store per lane precise delay adjustment for MDQ1 and MDQ5 relative to the whole nibble delays in PG[1:0]RW[E5:E4].

Table 106 — PG [1:0] RWEB: MDQ1/5 Read Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ1 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ1 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ1 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ1 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ1 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ1 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ1 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ1 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ1 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ5 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ5 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ5with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ5with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWEB will be sticky, cleared by power cycle not reset.
2. The delay of the lower nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E4]. The PG [1:0] RWEB[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ1 lane relative to the lower nibble baseline delay for a more optimal position.
3. The delay of the upper nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E5]. The PG [1:0] RWEB[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ5 lane relative to the upper nibble baseline delay for a more optimal position.

10.12.13 PG [1:0] RWEC- MDQ2/6 Read Delay Control Word

The control word location PG[1:0]RWEC is used to store per lane precise delay adjustment for MDQ2 and MDQ6 relative to the whole nibble delays in PG[1:0]RW[E5:E4].

Table 107 — PG [1:0] RWEC: MDQ2/6 Read Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ2 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ2 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ2 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ2 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ2 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ2 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ2 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ2 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ2 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ6 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ6 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ6with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ6 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWEC will be sticky, cleared by power cycle not reset.
2. The delay of the lower nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E4]. The PG [1:0] RWEC[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ2 lane relative to the lower nibble baseline delay for a more optimal position.
3. The delay of the upper nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E5]. The PG [1:0] RWEC[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ6 lane relative to the upper nibble baseline delay for a more optimal position.

10.12.14 PG [1:0] RWED - MDQ3/7 Read Delay Control Word

The control word location PG[1:0]RWED is used to store per lane precise delay adjustment for MDQ3 and MDQ7 relative to the whole nibble delays in PG[1:0]RW[E5:E4].

Table 108 — PG [1:0] RWED: MDQ3/7 Read Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ3 and Lower Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ3 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ3 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ3 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ3 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ3 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ3 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ3 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ3 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ7 and Upper Nibble Baseline MDQS Delay During Read Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ7 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ7 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWED will be sticky, cleared by power cycle not reset.
2. The delay of the lower nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E4]. The PG[1:0]RWED[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ3 lane relative to the lower nibble baseline delay for a more optimal position.
3. The delay of the upper nibble MDQS_t/MDQS_c signals received by the DDR5DB01 during read commands is set by PG [1:0] RW[E5]. The PG[1:0]RWED[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ7 lane relative to the upper nibble baseline delay for a more optimal position.

10.12.15 PG[1:0] RWEE - MDQ0/4 Write Delay Control Word

The control word location PG[1:0]RWEE is used to store per lane precise delay adjustment for MDQ0 and MDQ4 relative to the whole nibble delays in PG[1:0]RW[E7:E6].

Table 109 — PG [1:0] RWEE: MDQ0/4 Write Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ0 and Lower Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ0 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ0 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ0 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ0 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ0 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ0 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ0 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ0 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ4 and Upper Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ4 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ4 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWEE will be sticky, cleared by power cycle not reset.
2. The phase between the lower nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG [1:0] RWE6. The PG[1:0] RWEE[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ0 lane relative to the lower nibble baseline for a more optimal position.
3. The phase between the upper nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG [1:0] RWE7. The PG[1:0] RWEE[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ4 lane relative to the upper nibble baseline for a more optimal position.

10.12.16 PG[1:0] RWEF- MDQ1/5 Write Delay Control Word

The control word location PG[1:0]RWEF is used to store per lane precise delay adjustment for MDQ1 and MDQ5 relative to the whole nibble delays in PG[1:0]RW[E7:E6].

Table 110 — PG[1:0] RWEF: MDQ1/5 Write Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ1 and Lower Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ1 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ1 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ1 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ1 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ1 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ1 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ1 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ1 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ5 and Upper Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ5 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ5 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWEF will be sticky, cleared by power cycle not reset.
2. The phase between the lower nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG[1:0] RWE6. The PG[1:0] RWEF[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ1 lane relative to the lower nibble baseline for a more optimal position.
3. The phase between the upper nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG[1:0] RWE7. The PG[1:0] RWEF[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ5 lane relative to the upper nibble baseline for a more optimal position.

10.12.17 PG[1:0] RWF0- MDQ2/6 Write Delay Control Word

The control word location PG[1:0] RWF0 is used to store per lane precise delay adjustment for MDQ2 and MDQ6 relative to the whole nibble delays in PG [1:0] RW[E7:E6].

Table 111 — PG[1:0] RWF0:MDQ2/6 Write Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ2 and Lower Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ2 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ2 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ2 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ2 with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ2 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ2 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ2 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ2 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ6 and Upper Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ6 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ6 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWF0 will be sticky, cleared by power cycle not reset.
2. The phase between the lower nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG [1:0] RWE6. The PG[1:0] RWF0[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ2 lane relative to the lower nibble baseline for a more optimal position.
3. The phase between the upper nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG [1:0] RWE7. The PG[1:0] RWF0[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ6 lane relative to the upper nibble baseline for a more optimal position.

10.12.18 PG[1:0] RWF1 - MDQ3/7 Write Delay Control Word

The control word location PG[1:0]RWF1 is used to store per lane precise delay adjustment for MDQ3 and MDQ7 relative to the whole nibble delays in PG[1:0]RW[E7:E6].

Table 112 — PG [1:0] RWF1- MDQ3/7 Write Delay Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ3 and Lower Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[2]	Delay MDQ3 with respect to baseline by +0/64 * t_{CK} (Default)
x	x	x	x	x	0	0	1		Delay MDQ3 with respect to baseline by +1/64 * t_{CK}
x	x	x	x	x	0	1	0		Delay MDQ3 with respect to baseline by +2/64 * t_{CK}
x	x	x	x	x	0	1	1		Delay MDQ3with respect to baseline by +3/64 * t_{CK}
x	x	x	x	x	1	0	0		Delay MDQ3 with respect to baseline by -0/64 * t_{CK} (same as default)
x	x	x	x	x	1	0	1		Delay MDQ3 with respect to baseline by -1/64 * t_{CK}
x	x	x	x	x	1	1	0		Delay MDQ3 with respect to baseline by -2/64 * t_{CK}
x	x	x	x	x	1	1	1		Delay MDQ3 with respect to baseline by -3/64 * t_{CK}
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ7 and Upper Nibble Baseline MDQ Delay During Write Transactions in Steps of (1/64) * t_{CK}[3]	Delay MDQ7 with respect to baseline by +0/64 * t_{CK} (Default)
x	0	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by +1/64 * t_{CK}
x	0	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by +2/64 * t_{CK}
x	0	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by +3/64 * t_{CK}
x	1	0	0	x	x	x	x		Delay MDQ7 with respect to baseline by -0/64 * t_{CK} (same as default)
x	1	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by -1/64 * t_{CK}
x	1	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by -2/64 * t_{CK}
x	1	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by -3/64 * t_{CK}
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[1:0]RWF1 will be sticky, cleared by power cycle not reset.
2. The phase between the lower nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG[1:0] RWE6. The PG[1:0] RWF1[3:0] control bits can be used by the host to adjust the phase relationship for the MDQ3 lane relative to the lower nibble baseline for a more optimal position.
3. The phase between the upper nibble MDQ and MDQS signals driven by the DDR5DB01 during write commands is set by PG[1:0] RWE7. The PG[1:0] RWF1[7:4] control bits can be used by the host to adjust the phase relationship for the MDQ7 lane relative to the upper nibble baseline for a more optimal position.

10.13 Paged Vref Control Words

10.13.1 PG[2]RW[E7:E0] - Host Interface Internal VrefDQ Control Word

Table 113 — PG[2]RW[E7:E0]: Host Interface Internal VrefDQ Control Word[1,2]

Setting								Definition	Encoding VrefDQ as % of V_{DD}[3]
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	0	0	0	0	0	0	0	Host Interface Internal VrefDQ Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	1	0		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x	...								...
x	0	1	0	1	1	0	1		75% (Default)
x	...								...
x	1	1	1	0	1	0	1		39.0%
x	1	1	1	0	1	1	0		38.5%
x	1	1	1	0	1	1	1		38.0%
x	1	1	1	1	0	0	0		37.5%
x	1	1	1	1	0	0	1		37.0%
x	1	1	1	1	0	1	0		36.5%
x	1	1	1	1	0	1	1		36.0%
x	1	1	1	1	1	0	0		35.5%
x	1	1	1	1	1	0	1		35.0%
x	1	1	1	1	1	1	0		Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		

1. PG[2]RW[E7:E0] will be sticky, cleared by power cycle not reset
2. Table 58 illustrates the assignment of each control word in the PG[2]RW[E7:E0] group to the corresponding input pin it controls.
3. These are target VrefDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.

10.13.2 PG[2]RW[F1:F0] - DRAM Interface Internal VrefMDQ Control Word

Table 114 — PG[2]RW[F1:F0]: DRAM Interface Internal VrefMDQ Control Word[1,2]

Setting								Definition	Encoding VrefMDQ as % of V_{DD}[3]
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	0	0	0	0	0	0	0	DRAM Interface Internal VrefMDQ Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	1	0		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x	...								...
x	0	1	0	1	1	0	1		75% (Default)
x	...								...
x	1	1	1	0	1	0	1		39.0%
x	1	1	1	0	1	1	0		38.5%
x	1	1	1	0	1	1	1		38.0%
x	1	1	1	1	0	0	0		37.5%
x	1	1	1	1	0	0	1		37.0%
x	1	1	1	1	0	1	0		36.5%
x	1	1	1	1	0	1	1		36.0%
x	1	1	1	1	1	0	0		35.5%
x	1	1	1	1	1	0	1		35.0%
x	1	1	1	1	1	1	0		Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		

1. PG[2]RW[F1:F0] will be sticky, cleared by power cycle not reset
2. Table 58 illustrates the assignment of each control word in the PG[2]RW[F1:F0] group to the corresponding input pin it controls.
3. These are target VrefMDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.

Note: Table 114 applies to Upper and Lower nibble on DRAM interface.

10.13.3 PG[2]RWFA - Internal BVref Control Word

Table 115 — PG[2]RWFA: Internal BVref Control Word

Setting								Definition	Encoding BVref as % of V_{DD}[1]
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Internal BVref Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	1	0		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x				...					...
x	0	1	0	1	1	0	1		75% (Default)
x				...					...
x	1	1	1	0	1	0	1		39.0%
x	1	1	1	0	1	1	0		38.5%
x	1	1	1	0	1	1	1		38.0%
x	1	1	1	1	0	0	0		37.5%
x	1	1	1	1	0	0	1		37.0%
x	1	1	1	1	0	1	0		36.5%
x	1	1	1	1	0	1	1		36.0%
x	1	1	1	1	1	0	0		35.5%
x	1	1	1	1	1	0	1		35.0%
x	1	1	1	1	1	1	0		Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		

1. These are target BVref values. Acceptable actual values are determined based on tolerances defined in electrical section.

10.14 Paged DFE Control Words

10.14.1 PG[5:4]RW[E0,E8,F0,F8] - DQ[7:0] Receiver DFE Gain Offset

Table 116 — PG[5:4]RW[E0,E8,F0,F8] DQ[7:0] Receiver DFE Gain Offset Adjustment[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Flat-band (DC) gain adjustment [2,3,4,5,6]	Gain Adjustment = 0 dB (default)
x	x	x	x	x	0	0	1		Gain Adjustment = +6 dB
x	x	x	x	x	0	1	0		Gain Adjustment = +4 dB
x	x	x	x	x	0	1	1		Gain Adjustment = +2 dB
x	x	x	x	x	1	0	0		Gain Adjustment = 0 dB (same as default)
x	x	x	x	x	1	0	1		Gain Adjustment = -2 dB
x	x	x	x	x	1	1	0		Gain Adjustment = -4 dB
x	x	x	x	x	1	1	1		Gain Adjustment = -6 dB
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x		Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x		Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x		Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x		Reserved
1	x	x	x	x	x	x	x		Reserved

1. Table 59 and Table 60 illustrate the assignment of each control word in the PG[5:4]RW[E0,E8,F0,F8] group to the corresponding input pin it controls.
2. Flat-band (DC) gain adjustment (up to the Nyquist rate) adjustment control from I/O die pad to latching element in DQn.
3. The Gain Adjustment is applied to the baseline (default) inherent gain implemented in the receiver.
4. Gain Adjustment values shown are verified by design and the measurement from device pins is defined in a separate specification.
5. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 50, “DFE Gain and Tap Coefficient Step Parameters,” on page 83.
6. PG[5:4]RW[E0,E8,F0,F8] will be sticky, cleared by power cycle not reset.

10.14.2 PG[5:4]RW[E1,E9,F1,F9] - DQ[7:0] Receiver DFE Tap 1 Coefficients

Table 117 — PG[5:4]RW[E1,E9,F1,F9]: DQ [7:0] Receiver DFE Tap 1 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Tap 1 DFE Coefficient [2,3,4]	(Default) Tap 1 DFE bias = 0 mV
x	x	0	0	0	0	0	1		Tap 1 DFE bias +1 Tap Step
x	x	0	0	0	0	1	0		Tap 1 DFE bias +2 Tap Steps
x	x	0	0	0	0	1	1		Tap 1 DFE bias +3 Tap Step
x	x	0	0	0	1	0	0		Tap 1 DFE bias +4 Tap Steps
x	x	0	0	0	1	0	1		Tap 1 DFE bias +5 Tap Steps
x	x	0	0	0	1	1	0		Tap 1 DFE bias +6 Tap Steps
x	x	0	0	0	1	1	1		Tap 1 DFE bias +7 Tap Steps
x	x	0	0	1	0	0	0		Tap 1 DFE bias +8 Tap Steps
x	x	0	0	1	0	0	1		Tap 1 DFE bias +9 Tap Steps
x	x	0	0	1	0	1	0		Tap 1 DFE bias +10 Tap Steps
x	x	0	0	1	0	1	1		Tap 1 DFE bias +11 Tap Steps
x	x	0	0	1	1	0	0		Tap 1 DFE bias +12 Tap Steps
x	x	0	0	1	1	0	1		Tap 1 DFE bias +13 Tap Steps
x	x	0	0	1	1	1	0		Tap 1 DFE bias +14 Tap Steps
x	x	0	0	1	1	1	1		Tap 1 DFE bias +15 Tap Steps
x	x	0	1	0	0	0	0		Tap 1 DFE bias +16 Tap Steps
x	x	0	1	0	0	0	1		Tap 1 DFE bias +17 Tap Steps
x	x	0	1	0	0	1	0		Tap 1 DFE bias +18 Tap Steps
x	x	0	1	0	0	1	1		Tap 1 DFE bias +19 Tap Steps
x	x	0	1	0	1	0	0		Tap 1 DFE bias +20 Tap Steps
x	x	0	1	0	1	0	1		Tap 1 DFE bias +21 Tap Steps
x	x	0	1	0	1	1	0		Tap 1 DFE bias +22 Tap Steps
x	x	0	1	0	1	1	1		Tap 1 DFE bias +23 Tap Steps
x	x	0	1	1	0	0	0		Tap 1 DFE bias +24 Tap Steps
x	x	0	1	1	0	0	1		Tap 1 DFE bias +25 Tap Steps
x	x	0	1	1	0	1	0		Tap 1 DFE bias +26 Tap Steps
x	x	0	1	1	0	1	1		Tap 1 DFE bias +27 Tap Steps
x	x	0	1	1	1	0	0		Tap 1 DFE bias +28 Tap Steps
x	x	0	1	1	1	0	1		Tap 1 DFE bias +29 Tap Steps
x	x	0	1	1	1	1	0		Tap 1 DFE bias +30 Tap Steps
x	x	0	1	1	1	1	1		Tap 1 DFE bias +31 Tap Steps
x	x	1	0	0	0	0	0		Tap 1 DFE bias +32 Tap Steps
x	x	1	0	0	0	0	1		Tap 1 DFE bias +33 Tap Steps
x	x	1	0	0	0	1	0		Tap 1 DFE bias +34 Tap Steps
x	x	1	0	0	0	1	1		Tap 1 DFE bias +35 Tap Steps
x	x	1	0	0	1	0	0		Tap 1 DFE bias +36 Tap Steps
x	x	1	0	0	1	0	1		Tap 1 DFE bias +37 Tap Steps
x	x	1	0	0	1	1	0		Tap 1 DFE bias +38 Tap Steps
x	x	1	0	0	1	1	1		Tap 1 DFE bias +39 Tap Steps
x	x	1	0	1	0	0	0		Tap 1 DFE bias +40 Tap Steps
x	x	1	0	1	0	0	1		Tap 1 DFE bias +41 Tap Steps
x	x	1	0	1	0	1	0		Tap 1 DFE bias +42 Tap Steps
x	x	1	0	1	0	1	1		Tap 1 DFE bias +43 Tap Steps
x	x	1	0	1	1	0	0		Tap 1 DFE bias +44 Tap Steps
x	x	1	0	1	1	0	1		Tap 1 DFE bias +45 Tap Steps
x	x	1	0	1	1	1	0		Tap 1 DFE bias +46 Tap Steps
x	x	1	0	1	1	1	1		Tap 1 DFE bias +47 Tap Steps
x	x	1	1	0	0	0	0		Tap 1 DFE bias +48 Tap Steps
x	x	1	1	0	0	0	1		Tap 1 DFE bias +49 Tap Steps
x	x	1	1	0	0	1	0		Tap 1 DFE bias +50 Tap Steps
x	x	1	1	0	0	1	1		Reserved
x	x	1	1	0	1	0	0		Reserved
x	x	1	1	0	1	0	1		Reserved
x	x	1	1	0	1	1	0		Reserved

Table 117 — PG[5:4]RW[E1,E9,F1,F9]: DQ [7:0] Receiver DFE Tap 1 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	1	1	0	1	1	1	Tap 1 DFE Coefficient [1,2,3]	Reserved
x	x	1	1	1	0	0	0		Reserved
x	x	1	1	1	0	0	1		Reserved
x	x	1	1	1	0	1	0		Reserved
x	x	1	1	1	0	1	1		Reserved
x	x	1	1	1	1	0	0		Reserved
x	x	1	1	1	1	0	1		Reserved
x	x	1	1	1	1	1	0		Reserved
x	x	1	1	1	1	1	1		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 1 Coefficient Sign Bit	(Default) Positive Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

1. Table 59 and Table 60 illustrate the assignment of each control word in the PG[5:4]RW[E1,E9,F1,F9] group to the corresponding input pin it controls.
2. Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 50, “DFE Gain and Tap Coefficient Step Parameters,” on page 83.
4. PG[5:4]RW[E1,E9,F1,F9] will be sticky, cleared by power cycle not reset.

10.14.3 PG[5:4]RW[E2,EA,F2,FA] - DQ[7:0] Receiver DFE Tap 2 Coefficients

Table 118 — PG[5:4]RW[E2,EA,F2,FA]: DQ[7:0] Receiver DFE Tap 2 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Tap 2 DFE Coefficient[2,3,4]	(Default) Tap 2 DFE bias = 0 mV
x	x	0	0	0	0	0	1		Tap 2 DFE bias+1 Tap Step
x	x	0	0	0	0	1	0		Tap 2 DFE bias +2 Tap Steps
x	x	0	0	0	0	1	1		Tap 2 DFE bias +3 Tap Steps
x	x	0	0	0	1	0	0		Tap 2 DFE bias +4 Tap Steps
x	x	0	0	0	1	0	1		Tap 2 DFE bias +5 Tap Steps
x	x	0	0	0	1	1	0		Tap 2 DFE bias +6 Tap Steps
x	x	0	0	0	1	1	1		Tap 2 DFE bias +7 Tap Steps
x	x	0	0	1	0	0	0		Tap 2 DFE bias +8 Tap Steps
x	x	0	0	1	0	0	1		Tap 2 DFE bias +9 Tap Steps
x	x	0	0	1	0	1	0		Tap 2 DFE bias +10 Tap Steps
x	x	0	0	1	0	1	1		Tap 2 DFE bias +11 Tap Steps
x	x	0	0	1	1	0	0		Tap 2 DFE bias +12 Tap Steps
x	x	0	0	1	1	0	1		Tap 2 DFE bias +13 Tap Steps
x	x	0	0	1	1	1	0		Tap 2 DFE bias +14 Tap Steps
x	x	0	0	1	1	1	1		Tap 2 DFE bias +15 Tap Steps
x	x	0	1	0	0	0	0		Tap 2 DFE bias +16 Tap Steps
x	x	0	1	0	0	0	1		Tap 2 DFE bias +17 Tap Steps
x	x	0	1	0	0	1	0		Tap 2 DFE bias +18 Tap Steps
x	x	0	1	0	0	1	1		Tap 2 DFE bias +19 Tap Steps
x	x	0	1	0	1	0	0		Tap 2 DFE bias +20 Tap Steps
x	x	0	1	0	1	0	1		Reserved
x	x	0	1	0	1	1	0		Reserved
x	x	0	1	0	1	1	1		Reserved
x	x	0	1	1	0	0	0		Reserved
x	x	0	1	1	0	0	1		Reserved
x	x	0	1	1	0	1	0		Reserved
x	x	0	1	1	0	1	1		Reserved
x	x	0	1	1	1	0	0		Reserved
x	x	0	1	1	1	0	1		Reserved
x	x	0	1	1	1	1	0		Reserved
x	x	0	0	1	1	1	1		Reserved
x	x	1	0	0	0	0	1		Reserved
x	x	1	0	0	0	0	0		Reserved
x	x	1	0	0	0	1	1		Reserved
x	x	1	0	0	0	1	0		Reserved
x	x	1	0	0	1	0	1		Reserved
x	x	1	0	0	1	0	0		Reserved
x	x	1	0	0	1	1	1		Reserved
x	x	1	0	0	1	1	0		Reserved
x	x	1	0	1	0	0	1		Reserved
x	x	1	0	1	0	0	0		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 2 Coefficient Sign Bit	(Default) Positive Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 2 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 2 post-cursor)

1. Table 59 and Table 60 illustrate the assignment of each control word in the PG[5:4]RW[E2,EA,F2,FA] group to the corresponding input pin it controls.
2. Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 50, “DFE Gain and Tap Coefficient Step Parameters,” on page 83.
4. PG[5:4]RW[E2,EA,F2,FA] will be sticky, cleared by power cycle not reset.

10.14.4 PG[5:4]RW[E3,EB,F3,FB] - DDQ[7:0] Receiver DFE Tap 3 Coefficient

Table 119 — PG[5:4]RW[E3,EB,F3,FB]: DQ [7:0] Receiver DFE Tap 3 Coefficient[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 3 DFE Coefficient [2,3,4]	(Default) Tap 3 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 3 DFE bias +1 Tap Step
x	x	x	0	0	0	1	0		Tap 3 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 3 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 3DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 3 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 3 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 3 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 3 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 3 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 3 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 3DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 3 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 3DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 3 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 3 DFE bias +15 Tap Steps
x	x	x	1	0	0	0	0		Reserved
x	x	x	1	0	0	0	1		Reserved
x	x	x	1	0	0	1	0		Reserved
x	x	x	1	0	0	1	1		Reserved
x	x	x	1	0	1	0	0		Reserved
x	x	x	1	0	1	0	1		Reserved
x	x	x	1	0	1	1	0		Reserved
x	x	x	1	0	1	1	1		Reserved
x	x	x	1	1	0	0	0		Reserved
x	x	x	1	1	0	0	1		Reserved
x	x	x	1	1	0	1	0		Reserved
x	x	x	1	1	0	1	1		Reserved
x	x	x	1	1	1	0	0		Reserved
x	x	x	1	1	1	0	1		Reserved
x	x	x	1	1	1	1	0		Reserved
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 3 Coefficient Sign Bit	(Default) Positive Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 3 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 3 post-cursor)

1. Table 59 and Table 60 illustrate the assignment of each control word in the PG[5:4]RW[E3,EB,F3,FB] group to the corresponding input pin it controls.
2. Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 50, “DFE Gain and Tap Coefficient Step Parameters,” on page 83.
4. PG[5:4]RW[E3,EB,F3,FB] will be sticky, cleared by power cycle not reset.

10.14.5 PG[5:4]RW[E4,EC,F4,FC] - DQ[7:0] Receiver DFE Tap 4 Coefficients

Table 120 — PG[5:4]RW[E4,EC,F4,FC]: DQ[7:0] Receiver DFE Tap 4 Coefficients[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 4 DFE Coefficient[2,3,4]	(Default) Tap 4 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 4 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 4 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 4 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 4 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 4 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 4 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 4 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 4 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 4 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 4 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 4 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 4 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 4 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 4 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 4 DFE bias +15 Tap Steps
x	x	x	1	0	0	0	0		Reserved
x	x	x	1	0	0	0	1		Reserved
x	x	x	1	0	0	1	0		Reserved
x	x	x	1	0	0	1	1		Reserved
x	x	x	1	0	1	0	0		Reserved
x	x	x	1	0	1	0	1		Reserved
x	x	x	1	0	1	1	0		Reserved
x	x	x	1	0	1	1	1		Reserved
x	x	x	1	1	0	0	0		Reserved
x	x	x	1	1	0	0	1		Reserved
x	x	x	1	1	0	1	0		Reserved
x	x	x	1	1	0	1	1		Reserved
x	x	x	1	1	1	0	0		Reserved
x	x	x	1	1	1	0	1		Reserved
x	x	x	1	1	1	1	0		Reserved
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 4 Coefficient Sign Bit	(Default) Positive Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 4 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 4 post-cursor)

1. Table 59 and Table 60 illustrate the assignment of each control word in the PG[5:4]RW[E4,EC,F4,FC] group to the corresponding input pin it controls.
2. Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.
3. Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 50, “DFE Gain and Tap Coefficient Step Parameters,” on page 83.
4. PG[5:4]RW[E4,EC,F4,FC] will be sticky, cleared by power cycle not reset.

10.14.6 PG[6]RW[E0, E4, E8, EC, F0, F4, F8, FC] - DFE Error Counter Lower 8 Bits

Table 121 — PG[6]RW[E0, E4, E8, EC, F0, F4, F8, FC] - DFE Error Counter Lower 8 Bit

DFE Error Counter Lower 8 Bit Register[1,2]							
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

1. Power on Default is OP[7:0] = 0.
2. Read Only Register.

10.14.7 PG[6]RW[E1, E5, E9, ED, F1, F5, F9, FD] - DFE Error Counter Upper 8 Bits

Table 122 — PG[6]RW[E1, E5, E9, ED, F1, F5, F9, FD]- DFE Error Counter Upper 8 Bit

DFE Error Counter Upper 8 Bit Register[1,2]							
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP1**	**OP0**
EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC 9	EC 8

1. Power on Default is OP[7:0] = 0.
2. Read Only Register.

10.14.8 PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE] - DFE_Vref

Table 123 — PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE]: DFE_Vref[1]

PG[6]RW[E2, E6 .. FE]						DFE Training VREF in mV[2,3,4]							
						PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]= 1 (NEG Range)				PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]= 0 (POS Range)			
OP7	**OP6**	**OP5**	**OP4**	**OP3**	**OP2**	**OP[1:0] = 00**	**OP[1:0] = 01**	**OP[1:0] = 10**	**OP[1:0] = 11**	**OP[1:0] = 00**	**OP[1:0] = 01**	**OP[1:0] = 10**	**OP[1:0] = 11**
0	0	0	0	0	0	0.0	- 2.5	- 5.0	- 7.5	0.0	+ 2.5	+ 5.0	+ 7.5
0	0	0	0	0	1	- 10.0	- 12.5	- 15.0	- 17.5	+ 10.0	+ 12.5	+ 15.0	+ 17.5
0	0	0	0	1	0	- 20.0	- 22.5	- 25.0	- 27.5	+ 20.0	+ 22.5	+ 25.0	+ 27.5
0	0	0	0	1	1	- 30.0	- 32.5	- 35.0	- 37.5	+ 30.0	+ 32.5	+ 35.0	+ 37.5
0	0	0	1	0	0	- 40.0	- 42.5	- 45.0	- 47.5	+ 40.0	+ 42.5	+ 45.0	+ 47.5
0	0	0	1	0	1	- 50.0	- 52.5	- 55.0	- 57.5	+ 50.0	+ 52.5	+ 55.0	+ 57.5
0	0	0	1	1	0	- 60.0	- 62.5	- 65.0	- 67.5	+ 60.0	+ 62.5	+ 65.0	+ 67.5
0	0	0	1	1	1	- 70.0	- 72.5	- 75.0	- 77.5	+ 70.0	+ 72.5	+ 75.0	+ 77.5
0	0	1	0	0	0	- 80.0	- 82.5	- 85.0	- 87.5	+ 80.0	+ 82.5	+ 85.0	+ 87.5
0	0	1	0	0	1	- 90.0	- 92.5	- 95.0	- 97.5	+ 90.0	+ 92.5	+ 95.0	+ 97.5
0	0	1	0	1	0	- 100.0	- 102.5	- 105.0	- 107.5	+ 100.0	+ 102.5	+ 105.0	+ 107.5
0	0	1	0	1	1	- 110.0	- 112.5	- 115.0	- 117.5	+ 110.0	+ 112.5	+ 115.0	+ 117.5
0	0	1	1	0	0	- 120.0	- 122.5	- 125.0	- 127.5	+ 120.0	+ 122.5	+ 125.0	+ 127.5
0	0	1	1	0	1	- 130.0	- 132.5	- 135.0	- 137.5	+ 130.0	+ 132.5	+ 135.0	+ 137.5
0	0	1	1	1	0	- 140.0	- 142.5	- 145.0	- 147.5	+ 140.0	+ 142.5	+ 145.0	+ 147.5
0	0	1	1	1	1	- 150.0	- 152.5	- 155.0	- 157.5	+ 150.0	+ 152.5	+ 155.0	+ 157.5
0	1	0	0	0	0	- 160.0	- 162.5	- 165.0	- 167.5	+ 160.0	+ 162.5	+ 165.0	+ 167.5
0	1	0	0	0	1	- 170.0	- 172.5	- 175.0	- 177.5	+ 170.0	+ 172.5	+ 175.0	+ 177.5
0	1	0	0	1	0	- 180.0	- 182.5	- 185.0	- 187.5	+ 180.0	+ 182.5	+ 185.0	+ 187.5
0	1	0	0	1	1	- 190.0	- 192.5	- 195.0	- 197.5	+ 190.0	+ 192.5	+ 195.0	+ 197.5
0	1	0	1	0	0	- 200.0	- 202.5	- 205.0	- 207.5	+ 200.0	+ 202.5	+ 205.0	+ 207.5
0	1	0	1	0	1	- 210.0	- 212.5	- 215.0	- 217.5	+ 210.0	+ 212.5	+ 215.0	+ 217.5
0	1	0	1	1	0	- 220.0	- 222.5	- 225.0	- 227.5	+ 220.0	+ 222.5	+ 225.0	+ 227.5
0	1	0	1	1	1	- 230.0	- 232.5	- 235.0	- 237.5	+ 230.0	+ 232.5	+ 235.0	+ 237.5
0	1	1	0	0	0	- 240.0	- 242.5	- 245.0	- 247.5	+ 240.0	+ 242.5	+ 245.0	+ 247.5
0	1	1	0	0	1	- 250.0	- 252.5	- 255.0	- 257.5	+ 250.0	+ 252.5	+ 255.0	+ 257.5
0	1	1	0	1	0	- 260.0	- 262.5	- 265.0	- 267.5	+ 260.0	+ 262.5	+ 265.0	+ 267.5
0	1	1	0	1	1	- 270.0	- 272.5	- 275.0	- 277.5	+ 270.0	+ 272.5	+ 275.0	+ 277.5
0	1	1	1	0	0	- 280.0	- 282.5	- 285.0	- 287.5	+ 280.0	+ 282.5	+ 285.0	+ 287.5
0	1	1	1	0	1	- 290.0	- 292.5	- 295.0	- 297.5	+ 290.0	+ 292.5	+ 295.0	+ 297.5
0	1	1	1	1	0	- 300.0	- 302.5	- 305.0	- 307.5	+ 300.0	+ 302.5	+ 305.0	+ 307.5

Table 123 — PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE]: DFE_Vref[1]

PG[6]RW[E2, E6 .. FE]						DFE Training VREF in mV[2,3,4]							
						PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]= 1 (NEG Range)				PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]= 0 (POS Range)			
OP7	OP6	OP5	OP4	OP3	OP2	OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11	OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11
0	1	1	1	1	1	- 310.0	- 312.5	- 315.0	- 317.5	+ 310.0	+ 312.5	+ 315.0	+ 317.5
1	0	0	0	0	0	- 320.0	- 322.5	- 325.0	- 327.5	+ 320.0	+ 322.5	+ 325.0	+ 327.5
1	0	0	0	0	1	- 330.0	- 332.5	- 335.0	- 337.5	+ 330.0	+ 332.5	+ 335.0	+ 337.5
1	0	0	0	1	0	- 340.0	- 342.5	- 345.0	- 347.5	+ 340.0	+ 342.5	+ 345.0	+ 347.5
1	0	0	0	1	1	- 350.0	- 352.5	- 355.0	- 357.5	+ 350.0	+ 352.5	+ 355.0	+ 357.5
1	0	0	1	0	0	- 360.0	- 362.5	- 365.0	- 367.5	+ 360.0	+ 362.5	+ 365.0	+ 367.5
1	0	0	1	0	1	- 370.0	- 372.5	- 375.0	- 377.5	+ 370.0	+ 372.5	+ 375.0	+ 377.5
1	0	0	1	1	0	- 380.0	- 382.5	- 385.0	- 387.5	+ 380.0	+ 382.5	+ 385.0	+ 387.5
1	0	0	1	1	1	- 390.0	- 392.5	- 395.0	- 397.5	+ 390.0	+ 392.5	+ 395.0	+ 397.5
1	0	1	0	0	0	- 400.0	- 402.5	- 405.0	- 407.5	+ 400.0	+ 402.5	+ 405.0	+ 407.5
1	0	1	0	0	1	- 410.0	- 412.5	- 415.0	- 417.5	+ 410.0	+ 412.5	+ 415.0	+ 417.5
1	0	1	0	1	0	- 420.0	- 422.5	- 425.0	- 427.5	+ 420.0	+ 422.5	+ 425.0	+ 427.5
1	0	1	0	1	1	- 430.0	- 432.5	- 435.0	- 437.5	+ 430.0	+ 432.5	+ 435.0	+ 437.5
1	0	1	1	0	0	- 440.0	- 442.5	- 445.0	- 447.5	+ 440.0	+ 442.5	+ 445.0	+ 447.5
1	0	1	1	0	1	- 450.0	- 452.5	- 455.0	- 457.5	+ 450.0	+ 452.5	+ 455.0	+ 457.5
1	0	1	1	1	0	- 460.0	- 462.5	- 465.0	- 467.5	+ 460.0	+ 462.5	+ 465.0	+ 467.5
1	0	1	1	1	1	- 470.0	- 472.5	- 475.0	- 477.5	+ 470.0	+ 472.5	+ 475.0	+ 477.5
1	1	0	0	0	0	- 480.0	- 482.5	- 485.0	- 487.5	+ 480.0	+ 482.5	+ 485.0	+ 487.5
1	1	0	0	0	1	- 490.0	- 492.5	- 495.0	- 497.5	+ 490.0	+ 492.5	+ 495.0	+ 497.5
1	1	0	0	1	0	- 500.0	Reserved	Reserved	Reserved	+ 500.0	Reserved	Reserved	Reserved
1	1	0	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

1. Table 61 illustrates the assignment of each control word in the PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE] group to the corresponding input pin it controls.
2. These are target DFE_Vref values. Acceptable actual values are determined based on tolerances defined in electrical section.
3. The target DFE_Vref values shown in this table are input referred.
4. Even though each input receiver has a dedicated DFE_Vref control word, only one DFE_Vref monitor is allowed to be enabled at the same time in each sub-channel.

10.14.9 PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF] - Sign Bit Dn DFE_Vref Control Word

Table 124 — PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF] - Sign Bit Dn DFE_Vref Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Dn Sign DFE_Vref	Positive
x	x	x	x	x	x	x	1		Negative
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Table 61 illustrates the assignment of each control word in the PG[6][E3, E7, EB, EF, F3, F7, FB, FF] group to the corresponding input pin it controls.

10.14.10 PG[7]RW[EF:E0]- MDQ Error Counters Control Words

Table 125 — PG[7]RW[EF:E0]:MDQ Error Counters Control Words[1,2,3]

RW	Description	Encoding
PG7RW[E0,E2,E4,E6,E8,EA,EC, EE]	MDQ Read Error Counter Lower 8 Bits (Read Only)	Least Significant byte (bits[7:0] of the 16-bit MDQ Read Error Counter value
PG7RW[E1,E3,E5,E7,E9,EB,ED,EF]	MDQ Read Error Counter Upper 8 Bits (Read Only)	Most Significant byte (bits[15:8] of the 16-bit MDQ Read Error Counter value

1. The MDQ read error counters are Enabled only with RW83 MRD or MWD are set.
2. The counters maintain their state independent of MRD/MWD entry/exit.
3. Table 62 illustrates the assignment of each control word in the PG[7]RW[EF:E0] group to the corresponding input pin it controls.

10.14.11 PG[7]RWF0 - MDQ Error Counters Reset Control Word

Table 126 — PG[7]RWF0 - MDQ Error counters Reset Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	MDQ Error counters Reset	All per-bit MDQ read error counters operate normally.
x	x	x	x	x	x	x	1		All per-bit MDQ read error counters are reset to zero. This bit is self-clearing in the next cycle
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

10.15 Paged Snooped Control Words

10.15.1 PG[8]RW[E8:E0] - Snooped Control Words

Table 127 — PG[8]RW[E8:E0]- Snooped Control Word

Control Word	MR	CW Bits	Function	Default Setting	
				Required[1]	Recommended[2]
PG[8]E0	MR0	[1:0]	Burst Length	-	00_B
		[6:2]	CAS Latency (RL)	-	00010_B
		[7]	RFU	-	0_B
PG[8]E1	MR8	[2:0]	Read Preamble Settings	-	000_B
		[4:3]	Write Preamble Settings	-	01_B
		[5]	RFU	-	0_B
		[6]	Read Postamble	-	0_B
		[7]	Write Postamble	-	0_B
PG[8]E2	MR25	[0]	Read Training Pattern Format	0_B	-
		[1]	LFSR0 Pattern Option	0_B	-
		[2]	LFSR1 Pattern Option	0_B	-
		[3]	Not used for DB	0_B	-
		[7:4]	RFU	0000_B	-
PG[8]E3	MR26	[7:0]	Read Pattern Data0 / LFSR0	$0101\ 1010_B$	-
PG[8]E4	MR27	[7:0]	Read Pattern Data1 / LFSR1	$0011\ 1100_B$	-
PG[8]E5	MR28	[7:0]	Read Pattern Invert DQ[7:0]	$0000\ 0000_B$	-
PG[8]E6	MR30	[7:0]	Read LFSR Assignments DQ[7:0]	$1110\ 1110_B$	-
PG[8]E7	MR45	[7:0]	DQS Interval Timer Run Time	-	$0000\ 0000_B$
PG[8]E8	MR50	[0]	Read CRC Enable	-	0_B
		[1]	Write CRC Enable	-	0_B
		[5:2]	Not used for DB	-	0000_B
		[7:6]	RFU	-	00_B

1. All of the DDR5DB01 devices are required to implement the default settings defined in this column.
2. The default settings recommended in this column are intended to match the MR default settings of the DRAM device. The DDR5DB01 devices may or may not implement the default settings shown in this column.

10.16 Paged DFE Training Accelerator Control Words

10.16.1 PG[9]RWE0 - DFETA Training Mode Control Word

Table 128 — PG[9]RWE0 DFETA Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Training Accelerator	Stop DFE Training Accelerator (default)
x	x	x	x	x	x	x	1		Start DFE Training Accelerator
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	0	0	x	x	Select Inner Loop Parameter	Select Inner Loop Parameter - NULL[1]
x	x	x	x	0	1	x	x		Select Inner Loop Parameter - DFE_Vref
x	x	x	x	1	0	x	x		Select Inner Loop Parameter - VrefDQ
x	x	x	x	1	1	x	x		Reserved
x	0	0	0	x	x	x	x	Select Outer Loop Parameter	Select Outer Loop Parameter - NULL
x	0	0	1	x	x	x	x		Select Outer Loop Parameter - Tap 1
x	0	1	0	x	x	x	x		Select Outer Loop Parameter - Tap 2
x	0	1	1	x	x	x	x		Select Outer Loop Parameter - Tap 3
x	1	0	0	x	x	x	x		Select Outer Loop Parameter - Tap 4
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. NULL parameter choice means no change. NULL parameter loop can have multiple iterations.

10.16.2 PG[9]RWE1 - DFETA Inner Loop Start Value Bit [7:0]Control Word

DFETA Inner Loop Start Value is a 9-bit field the Lower bits 7:0 are in PG[9]RWE1 and the upper bit located in PG[9]RWE2.

Table 129 — PG[9]RWE1 - DFETA Inner Loop Start Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Start Value[1]	Inner Loop Start Value = 0x00
0	0	0	0	0	0	0	1		Inner Loop Start Value = 0x01
0	0	0	0	0	0	1	0		Inner Loop Start Value = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Start Value = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Start Value = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Start Value = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Start Value = 0xFF

1. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

10.16.3 PG[9]RWE2 - DFETA Inner Loop Start Value Bit [8]Control Word

Table 130 — PG[9]RWE2 - DFETA Inner Loop Start Value Bit [8]Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Start Value[1]	Inner Loop Start Value = 0x0
x	x	x	x	x	x	x	1		Inner Loop Start Value = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

10.16.4 PG[9]RWE3- DFETA Outer Loop Start Value Control Word

Table 131 — PG[9]RWE3: DFETA Outer Loop Start Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Start Value[1,2]	Outer Loop Start Value = 0x00
x	0	0	0	0	0	0	1		Outer Loop Start Value = 0x01
x	0	0	0	0	0	1	0		Outer Loop Start Value = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Start Value = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Start Value = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Start Value = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Start Value = 0x7F
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Depending on the Outer Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Outer Loop Parameter.
2. Even though the tap setting parameter registers are defined as signed magnitude fields, this start value is a two's complement encoding. The DB must convert this value to a signed magnitude format prior to updating the tap setting when Tap1, Tap2, Tap3, or Tap4 is chosen for the Outer Loop Parameter.

10.16.5 PG[9]RWE4- DFETA Inner Loop Current Value Bit [7:0] Control Word

Table 132 — PG[9]RWE4: DFETA Inner Loop Current Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Current Value. (Read Only)	Inner Loop Current Value = 0x00
0	0	0	0	0	0	0	1		Inner Loop Current Value = 0x01
0	0	0	0	0	0	1	0		Inner Loop Current Value = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Current Value = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Current Value = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Current Value = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Current Value = 0xFF

10.16.6 PG[9]RWE5- DFETA Inner Loop Current Value Bit [8]Control Word

Table 133 — PG[9]RWE5 - DFETA Inner Loop Current Value Bit [8]Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Current Value[1] (Read Only)	Inner Loop Current Value = 0x0
x	x	x	x	x	x	x	1		Inner Loop Current Value = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

10.16.7 PG[9]RWE6 - DFETA Outer Loop Current Value Control Word

Table 134 — RW[9]RWE6: DFETA Outer Loop Current Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Current Value. (Read Only)	Outer Loop Current Value = 0x00
x	0	0	0	0	0	0	1		Outer Loop Current Value = 0x01
x	0	0	0	0	0	1	0		Outer Loop Current Value = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Current Value = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Current Value = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Current Value = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Current Value = 0x7F
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

10.16.8 PG[9]RWE7 - DFETA Inner and Outer Loop Step Size Control Word

Table 135 — PG[9]RWE7: DFETA Inner and Outer Loop Step Size Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Inner Loop Step Size[1]	Inner Loop Step Size = 1
x	x	x	x	0	0	0	1		Inner Loop Step Size = 2
x	x	x	x	0	0	1	0		Inner Loop Step Size = 3
x	x	x	x	0	0	1	1		Inner Loop Step Size = 4
x	x	x	x	0	1	0	0		Inner Loop Step Size = 5
x	x	x	x	0	1	0	1		Inner Loop Step Size = 6
x	x	x	x	0	1	1	0		Inner Loop Step Size = 7
x	x	x	x	0	1	1	1		Inner Loop Step Size = 8
x	x	x	x	1	0	0	0		Inner Loop Step Size = 9
x	x	x	x	1	0	0	1		Inner Loop Step Size = 10
x	x	x	x	1	0	1	0		Inner Loop Step Size = 11
x	x	x	x	1	0	1	1		Inner Loop Step Size = 12
x	x	x	x	1	1	0	0		Inner Loop Step Size = 13
x	x	x	x	1	1	0	1		Inner Loop Step Size = 14
x	x	x	x	1	1	1	0		Inner Loop Step Size = 15
x	x	x	x	1	1	1	1		Inner Loop Step Size = 16
0	0	0	0	x	x	x	x	Outer Loop Step Size[1]	Outer Loop Step Size = 1
0	0	0	1	x	x	x	x		Outer Loop Step Size = 2
0	0	1	0	x	x	x	x		Outer Loop Step Size = 3
0	0	1	1	x	x	x	x		Outer Loop Step Size = 4
0	1	0	0	x	x	x	x		Outer Loop Step Size = 5
0	1	0	1	x	x	x	x		Outer Loop Step Size = 6
0	1	1	0	x	x	x	x		Outer Loop Step Size = 7
0	1	1	1	x	x	x	x		Outer Loop Step Size = 8
1	0	0	0	x	x	x	x		Outer Loop Step Size = 9
1	0	0	1	x	x	x	x		Outer Loop Step Size = 10
1	0	1	0	x	x	x	x		Outer Loop Step Size = 11
1	0	1	1	x	x	x	x		Outer Loop Step Size = 12
1	1	0	0	x	x	x	x		Outer Loop Step Size = 13
1	1	0	1	x	x	x	x		Outer Loop Step Size = 14
1	1	1	0	x	x	x	x		Outer Loop Step Size = 15
1	1	1	1	x	x	x	x		Outer Loop Step Size = 16

1. The step size is always positive, and thus the increment is always from lowest to highest value in the sweep. Note that the actual field setting indicates the Step Size – 1. The DB must account for this in the increment logic.

10.16.9 PG[9]RWE8 - DFETA Inter Loop Number of Increments Bit [7:0]Control Word

Table 136 — PG[9]RWE8: DFETA Inter Loop Number of Increments Bit [7:0] Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Number of Increments[1]	Inner Loop Number of Increments = 0x00
0	0	0	0	0	0	0	1		Inner Loop Number of Increments = 0x01
0	0	0	0	0	0	1	0		Inner Loop Number of Increments = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Number of Increments = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Number of Increments = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Number of Increments = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Number of Increments = 0xFF

1. Depending on the Inner Loop Parameter Selection and the Inner Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.

10.16.10 PG[9]RWE9 - DFETA Inter Loop Number of Increments Bit [8]Control Word

Table 137 — PG[9]RWE9 - DFETA Inner Loop Start Value Bit [8]Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Number of Increments[1]	Inner Loop Number of Increments = 0x0
x	x	x	x	x	x	x	1		Inner Loop Number of Increments = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

10.16.11 PG[9]RWEA - DFETA Outer Loop Number of Increments Control Word

Table 138 — PG[9]RWEA: DFETA Outer Loop Number of Increments Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Number of Increments[1]	Outer Loop Number of Increments = 0x00
x	0	0	0	0	0	0	1		Outer Loop Number of Increments = 0x01
x	0	0	0	0	0	1	0		Outer Loop Number of Increments = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Number of Increments = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Number of Increments = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Number of Increments = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Number of Increments = 0x7F
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Depending on the Outer Loop Parameter Selection and the Outer Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Outer Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.

10.16.12 PG[9]RWEB - DFETA Inner Loop Current Increment Bit [7:0] Status Control Word

Table 139 — PG[9]RWEB: DFETA Inner Loop Current Increment Bit [7:0] Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Current Increment (Read Only)	Inner Loop Current Increment = 0x00
0	0	0	0	0	0	0	1		Inner Loop Current Increment = 0x01
0	0	0	0	0	0	1	0		Inner Loop Current Increment = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Current Increment = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Current Increment = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Current Increment = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Current Increment = 0xFF

10.16.13 PG[9]RWEC - DFETA Inner Loop Current Increment Bit [8] Status Control Word

Table 140 — PG[9]RWEC - DFETA Inner Loop Current Increment Bit [8] Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Current Increment (Read Only)[1]	Inner Loop Current Increment = 0x0
x	x	x	x	x	x	x	1		Inner Loop Current Increment = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

10.16.14 PG[9]RWED - DFETA Outer Loop Current Increment Status Control Word

Table 141 — PG[9]RWED: DFETA Outer Loop Current Increment Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Outer Loop Current Increment (Read Only)	Outer Loop Current Increment = 0x00
x	0	0	0	0	0	0	1		Outer Loop Current Increment = 0x01
x	0	0	0	0	0	1	0		Outer Loop Current Increment = 0x02
x	...								...
x	1	1	1	1	1	0	0		Outer Loop Current Increment = 0x7C
x	1	1	1	1	1	0	1		Outer Loop Current Increment = 0x7D
x	1	1	1	1	1	1	0		Outer Loop Current Increment = 0x7E
x	1	1	1	1	1	1	1		Outer Loop Current Increment = 0x7F
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

10.16.15 PG[9]RW[F1:EE] - DFETA Write Limit and Counter Control Words

Table 142 — PG[9]RW[F1:EE]- DFETA Write Limit and Counter Control Words

Control Word	Definition	Encoding
RWEE[7:0]	Write Limit Value - Lower Byte	The write limit value is computed as RW_WriteLimitUpperByte[7:0] * 256 + RW_WriteLimitLowerByte[7:0] + 1
RWEF[7:0]	Write Limit Value - Upper Byte	The write limit value is computed as RW_WriteLimitUpperByte[7:0] * 256 + RW_WriteLimitLowerByte[7:0] + 1
RWF0[7:0]	Write Limit Counter Value Status - Lower Byte (Read Only)	The current value of the write limit counter's lower byte.
RWF1[7:0]	Write Limit Counter Value Status - Upper Byte (Read Only)	The current value of the write limit counter's upper byte.

10.17 Paged Periodic Update Registers

10.17.1 PG[A]RW[E7:E0] - Initial DRAM DQS Oscillator Counter Value

Table 143 — PG[A]RW[E7:E0] -Initial DRAM DQS Oscillator Counter Value[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	initial DRAM DQS oscillator counter value[2]	If DRAM tDQS2DQ tracking initialization mode is enabled, this register is written with the read data that is captured from the DRAM as a result of a DRAM-space MRR. Otherwise, it is unaltered. This register can also be written by a DB-space MRW operation and read by a DB-space MRR operation. This register defaults to 8'h00.

1. Table 65 illustrates the assignment of each control word in the PG[A]RW[E7:E0] group to the corresponding rank and nibble it controls.
2. PG[A]RW[E7:E0] will be sticky, cleared by power cycle, or RWB0[1], not reset.

10.17.2 PG[A]RW[EF:E8] - Initial DRAM DQS Clock Tree Delay Value

Table 144 — PG[A]RW[EF:E8] - Initial DRAM DQS Clock Tree Delay Value[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	Initial DRAM DQS clock tree delay value[2]	If DRAM tDQS2DQ tracking initialization mode is enabled, this register is written by the DB hardware with the calculated DQS clock tree delay value for the DRAM. Otherwise, it is unaltered. This register can be read by a DB-space MRR operation. This register defaults to 8'h00.

1. Table 65 illustrates the assignment of each control word in the PG[A]RW[EF:E8] group to the corresponding rank and nibble it controls.
2. PG[A]RW[EF:E8] will be sticky, cleared by power cycle or RWB0[1], not reset.

10.17.3 PG[A]RW[F7:F0] - Current DRAM DQS Oscillator Counter

Table 145 — PG[A]RW[F7:F0] - Current DRAM DQS Oscillator Counter[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	The current DRAM DQS oscillator counter value[2]	This register is written with the read data that is captured from the DRAM as a result of a DRAM-space MRR to its DQS OSC Counter register in either of the tDQS2DQ tracking modes. Otherwise, it is unaltered. This register can also be written by a DB-space MRW operation and read by a DB-space MRR operation. This register defaults to 8'h00.

1. Table 65 illustrates the assignment of each control word in the PG[A]RW[F7:F0] group to the corresponding rank and nibble it controls.
2. PG[A]RW[F7:F0] will be sticky, cleared by power cycle or RWB0[1], not reset.

10.17.4 PG[A]RW[FF:F8] - Current DRAM DQS Clock Tree Delay Value

Table 146 — PG[A]RW[FF:F8] - Current DRAM DQS Clock Tree Delay Value[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	The current DRAM DQS Clock Tree Delay.[2]	This register is written by the DB hardware with the calculated DQS clock tree delay LSB value for the lower nibble ,rank-0 DRAM in either of the tDQS2DQ tracking modes. Otherwise, it is unaltered. This register can be read by a DB-space MRR operation. This register defaults to 8'h00

1. Table 65 illustrates the assignment of each control word in the PG[A]RW[FF:F8] group to the corresponding rank and nibble it controls.
2. PG[A]RW[FF:F8] will be sticky, cleared by power cycle or RWB0[1], not reset.

10.17.5 PG[B]E0: Rank0 ODTLon_WR_offset Control Word

Table 147 — PG[B]E0: Rank0 ODTLon_WR_offset Control Word[1]

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	x	x	x	0	0	0	ODTLon_WR_N0_R0_offset (the offset for the lower nibble of Rank0)	Reserved
x	x	x	x	x	0	0	1		-4 Clocks
x	x	x	x	x	0	1	0		-3 Clocks
x	x	x	x	x	0	1	1		-2 Clocks
x	x	x	x	x	1	0	0		-1 Clocks (default)
x	x	x	x	x	1	0	1		0 Clocks
x	x	x	x	x	1	1	0		+1 Clocks
x	x	x	x	x	1	1	1		+2 Clocks
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLon_WR_N1_R0_offset (the offset for the upper nibble of Rank0)	Reserved
x	0	0	1	x	x	x	x		-4 Clocks
x	0	1	0	x	x	x	x		-3 Clocks
x	0	1	1	x	x	x	x		-2 Clocks
x	1	0	0	x	x	x	x		-1 Clocks (default)
x	1	0	1	x	x	x	x		0 Clocks
x	1	1	0	x	x	x	x		+1 Clocks
x	1	1	1	x	x	x	x		+2 Clocks
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE0 will be sticky, cleared by power cycle not reset.

10.17.6 PG[B]E1: Rank1 ODTLon_WR_offset Control Word

Table 148 — PG[B]E1: Rank1 ODTLon_WR_offset Control Word[1]

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	x	x	x	0	0	0	ODTLon_WR_N0_R1_offset (the offset for the lower nibble of Rank1)	Reserved
x	x	x	x	x	0	0	1		-4 Clocks
x	x	x	x	x	0	1	0		-3 Clocks
x	x	x	x	x	0	1	1		-2 Clocks
x	x	x	x	x	1	0	0		-1 Clocks (default)
x	x	x	x	x	1	0	1		0 Clocks
x	x	x	x	x	1	1	0		+1 Clocks
x	x	x	x	x	1	1	1		+2 Clocks
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLon_WR_N1_R1_offset (the offset for the upper nibble of Rank1)	Reserved
x	0	0	1	x	x	x	x		-4 Clocks
x	0	1	0	x	x	x	x		-3 Clocks
x	0	1	1	x	x	x	x		-2 Clocks
x	1	0	0	x	x	x	x		-1 Clocks (default)
x	1	0	1	x	x	x	x		0 Clocks
x	1	1	0	x	x	x	x		+1 Clocks
x	1	1	1	x	x	x	x		+2 Clocks
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE1 will be sticky, cleared by power cycle not reset.

10.17.7 PG[B]E2: Rank0 ODTLoff_WR_offset Control Word

Table 149 — PG[B]E2: Rank0 ODTLoff_WR_offset Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	ODTLoff_WR_N0_R0_offset (the offset for the lower nibble of Rank0)	Reserved
x	x	x	x	x	0	0	1		+4 Clocks
x	x	x	x	x	0	1	0		+3 Clocks
x	x	x	x	x	0	1	1		+2 Clocks
x	x	x	x	x	1	0	0		+1 Clocks
x	x	x	x	x	1	0	1		0 Clocks (default)
x	x	x	x	x	1	1	0		-1 Clocks
x	x	x	x	x	1	1	1		-2 Clocks
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLoff_WR_N1_R0_offset (the offset for the upper nibble of Rank0)	Reserved
x	0	0	1	x	x	x	x		+4 Clocks
x	0	1	0	x	x	x	x		+3 Clocks
x	0	1	1	x	x	x	x		+2 Clocks
x	1	0	0	x	x	x	x		+1 Clocks
x	1	0	1	x	x	x	x		0 Clocks (default)
x	1	1	0	x	x	x	x		-1 Clocks
x	1	1	1	x	x	x	x		-2 Clocks
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE2 will be sticky, cleared by power cycle not reset.

10.17.8 PG[B]E3: Rank1 ODTLoff_WR_offset Control Word

Table 150 — PG[B]E3: Rank1 ODTLoff_WR_offset Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	ODTLoff_WR_N0_R1_offset (the offset for the lower nibble of Rank1)	Reserved
x	x	x	x	x	0	0	1		+4 Clocks
x	x	x	x	x	0	1	0		+3 Clocks
x	x	x	x	x	0	1	1		+2 Clocks
x	x	x	x	x	1	0	0		+1 Clocks
x	x	x	x	x	1	0	1		0 Clocks (default)
x	x	x	x	x	1	1	0		-1 Clocks
x	x	x	x	x	1	1	1		-2 Clocks
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLoff_WR_N1_R1_offset (the offset for the upper nibble of Rank1)	Reserved
x	0	0	1	x	x	x	x		+4 Clocks
x	0	1	0	x	x	x	x		+3 Clocks
x	0	1	1	x	x	x	x		+2 Clocks
x	1	0	0	x	x	x	x		+1 Clocks
x	1	0	1	x	x	x	x		0 Clocks (default)
x	1	1	0	x	x	x	x		-1 Clocks
x	1	1	1	x	x	x	x		-2 Clocks
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE3 will be sticky, cleared by power cycle not reset.

10.17.9 PG[B]E4: Rank0 ODTLon_WR_NT_offset Control Word

Table 151 — PG[B]E4: Rank0 ODTLon_WR_NT_offset Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	ODTLon_WR_NT_N0_offset (the offset for the lower nibble, NT write commands are to Rank0 only)	Reserved
x	x	x	x	x	0	0	1		-4 Clocks
x	x	x	x	x	0	1	0		-3 Clocks
x	x	x	x	x	0	1	1		-2 Clocks
x	x	x	x	x	1	0	0		-1 Clocks (default)
x	x	x	x	x	1	0	1		0 Clocks
x	x	x	x	x	1	1	0		+1 Clocks
x	x	x	x	x	1	1	1		+2 Clocks
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLon_WR_NT_N1_offset (the offset for the upper nibble, NT write commands are to Rank0 only)	Reserved
x	0	0	1	x	x	x	x		-4 Clocks
x	0	1	0	x	x	x	x		-3 Clocks
x	0	1	1	x	x	x	x		-2 Clocks
x	1	0	0	x	x	x	x		-1 Clocks (default)
x	1	0	1	x	x	x	x		0 Clocks
x	1	1	0	x	x	x	x		+1 Clocks
x	1	1	1	x	x	x	x		+2 Clocks
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE4 will be sticky, cleared by power cycle not reset.

10.17.10 PG[B]E5: Rank0 ODTLoff_WR_NT_offset Control Word

Table 152 — PG[B]E5: Rank0 ODTLoff_WR_NT_offset Control Word[1]

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	ODTLoff_WR_NT_N0_offset (the offset for the lower nibble, NT write commands are to Rank0 only)	Reserved
x	x	x	x	x	0	0	1		+4 Clocks
x	x	x	x	x	0	1	0		+3 Clocks
x	x	x	x	x	0	1	1		+2 Clocks
x	x	x	x	x	1	0	0		+1 Clocks
x	x	x	x	x	1	0	1		0 Clocks (default)
x	x	x	x	x	1	1	0		-1 Clocks
x	x	x	x	x	1	1	1		-2 Clocks
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLoff_WR_NT_N1_offset (the offset for the upper nibble, NT write commands are to Rank0 only)	Reserved
x	0	0	1	x	x	x	x		+4 Clocks
x	0	1	0	x	x	x	x		+3 Clocks
x	0	1	1	x	x	x	x		+2 Clocks
x	1	0	0	x	x	x	x		+1 Clocks
x	1	0	1	x	x	x	x		0 Clocks (default)
x	1	1	0	x	x	x	x		-1 Clocks
x	1	1	1	x	x	x	x		-2 Clocks
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE5 will be sticky, cleared by power cycle not reset.

10.17.11 PG[B]E6: Rank0 ODTLon_RD_NT_offset Control Word

Table 153 — PG[B]E6: Rank0 ODTLon_RD_NT_offset Control Word[1]

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	x	x	x	0	0	0	ODTLon_RD_NT_N0_offset (the offset for the lower nibble, NT read commands are to Rank0 only)	Reserved
x	x	x	x	x	0	0	1		Reserved
x	x	x	x	x	0	1	0		-3 Clocks
x	x	x	x	x	0	1	1		-2 Clocks
x	x	x	x	x	1	0	0		-1 Clocks (default)
x	x	x	x	x	1	0	1		0 Clocks
x	x	x	x	x	1	1	0		+1 Clocks
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLon_RD_NT_N1_offset (the offset for the upper nibble, NT read commands are to Rank0 only)	Reserved
x	0	0	1	x	x	x	x		Reserved
x	0	1	0	x	x	x	x		-3 Clocks
x	0	1	1	x	x	x	x		-2 Clocks
x	1	0	0	x	x	x	x		-1 Clocks (default)
x	1	0	1	x	x	x	x		0 Clocks
x	1	1	0	x	x	x	x		+1 Clocks
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE6 will be sticky, cleared by power cycle not reset.

10.17.12 PG[B]E7: Rank0 ODTLoff_RD_NT_offset Control Word

Table 154 — PG[B]E7: Rank0 ODTLoff_RD_NT_offset Control Word[1]

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	x	x	x	0	0	0	ODTLoff_RD_NT_N0_offset (the offset for the lower nibble, NT read commands are to Rank0 only)	Reserved
x	x	x	x	x	0	0	1		Reserved
x	x	x	x	x	0	1	0		+3 Clocks
x	x	x	x	x	0	1	1		+2 Clocks
x	x	x	x	x	1	0	0		+1 Clocks
x	x	x	x	x	1	0	1		0 Clocks (default)
x	x	x	x	x	1	1	0		-1 Clocks
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	ODTLoff_RD_NT_N1_offset (the offset for the upper nibble, NT read commands are to Rank0 only)	Reserved
x	0	0	1	x	x	x	x		Reserved
x	0	1	0	x	x	x	x		+3 Clocks
x	0	1	1	x	x	x	x		+2 Clocks
x	1	0	0	x	x	x	x		+1 Clocks
x	1	0	1	x	x	x	x		0 Clocks (default)
x	1	1	0	x	x	x	x		-1 Clocks
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. PG[B]RWE7 will be sticky, cleared by power cycle not reset.

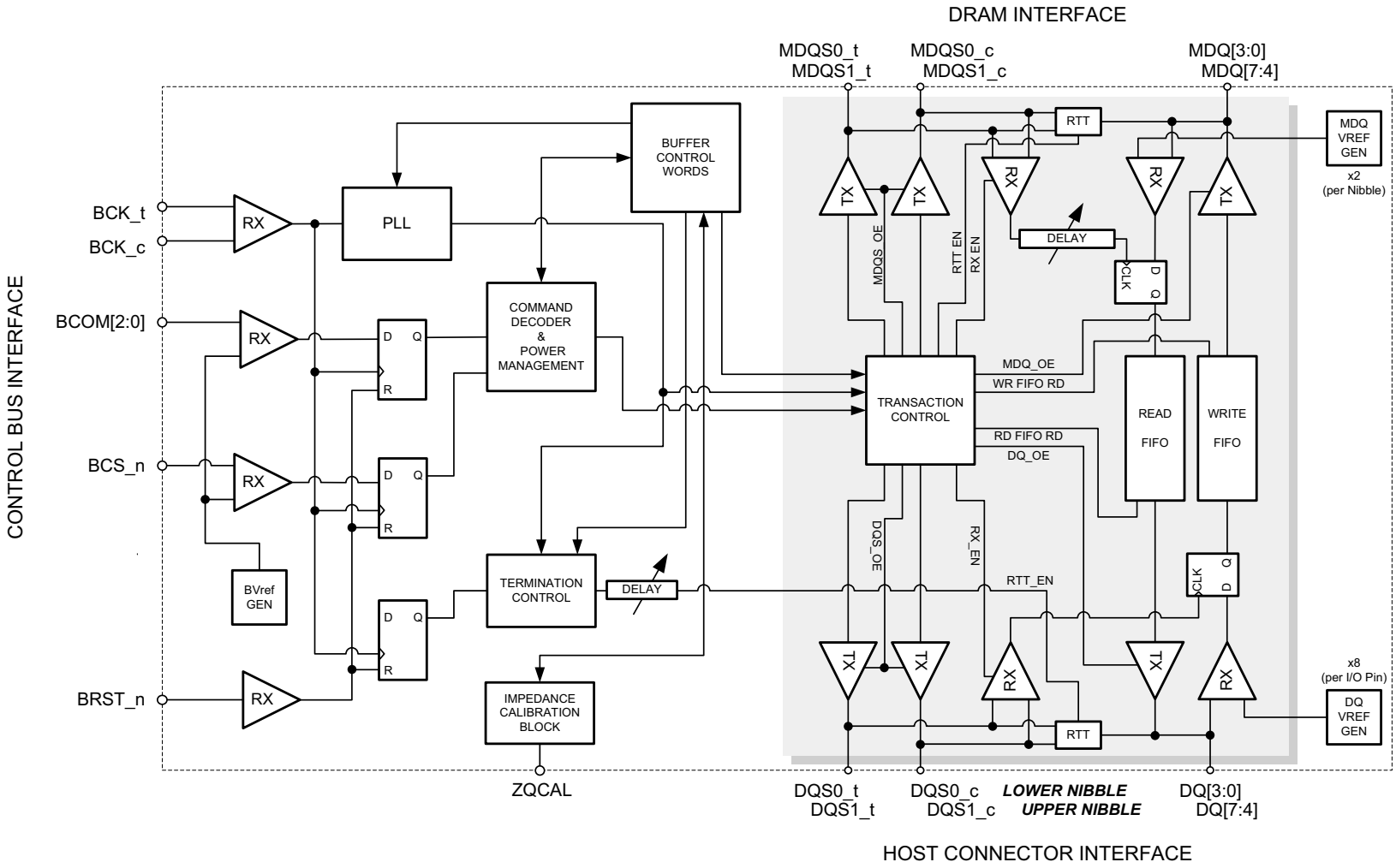


Figure 68 — Logic Diagram

11 Timing Requirements

Table 155 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5 -3200/ 3600/4000		DDR5-4400		DDR5-4800		
			Min	Max	Min	Max	Min	Max	Unit
f_{CLOCK}	Input clock frequency[1]	Application frequency[2]	1400	2030	1400	2233	1400	2436	MHz
f_{TEST}	Input clock frequency	Test frequency	280	990	280	990	280	990	MHz
t_{MRD}	Control word to control word delay	Number of clock cycles between two control word accesses or one control word access and the following DRAM command.	8	-	8	-	8	-	t_{CK}
t_{MRD_L}	Control word to control word delay	Number of clock cycles between an access to RW86, RW87, RW88, RW8A, RW8B, RW8C, RW8E, RW90, RWA0[7:2], PG[2]RW[FA, F1,F0,E7:E0][3], RWDF[4], PG[5:4]RW[FC:E0] (i.e., any receiver DFE tap coefficient value) and the next control word access or DRAM command.	16	-	16	-	16	-	t_{CK}
t_{MRD_L2}	Control word to control word delay	Number of clock cycles between an access to RW80, RW81, RW82, RW83, RW84[5], RW85[5], RW8D, RW97, RWA1[2:1], RWB0[1:0], PG[1:0]RW[F1:E0], RW8F, PG8RWE0, PG8RWE1, PG[9]RW[EF:EE, EA:E7, E3:E0], PG[A]RW[EF:E8, FF:F8], tODTL adjuster registers PGBRW[E7:E0], and the next control word access or DRAM command. Number of clock cycles between all PBA related control words (RW81, RW92, RW93).	32	-	32	-	32	-	t_{CK}
t_{MRD_L3}	Control word to DRAM Command delay for DFE Gain Adjustment in 1N and 2N modes	Waiting time between an access to RWA1[3, 0], PG[5:4]RW[F8, F0, E8, E0] RWA2[7:0] and the next DRAM command[6].	300	-	300	-	300	-	ns
t_{MRD_L4}	Control word to DRAM Command delay for DFE Vref Settling Time in 1N and 2N modes for $16 \le n < 32$, where n = number of steps[7]	Waiting time between an access to RWA0[1:0], PG[6]RW[FF, FE, FB, FA, F7, F6, F3, F2, EF, EE, EB, EA, E7, E6, E3, E2] and the next DRAM command[6].	300	-	300	-	300	-	ns
t_{ErrCnt_Rst}	Control word to control word delay for Error Counter Reset	Waiting time between Write access to RWA1[3] or PG[7]RWF0[0] and the next control word access.	32	-	32	-	32	-	t_{CK}
t_{TM_Entry}	Transparent Mode Entry Time	Delay from MRW that sets RW82[0] = 1 to Transparent Mode features enabled in DB.	-	250	-	250	-	250	ns
t_{MRR}	Mode Register Read Pattern to Mode Register Read Pattern Command Spacing	Back-to-back MRRs to Data Buffer or Back-to-Back MRRs to DRAM	8	-	8	-	8	-	t_{CK}
t_{MRROD1}	Delay from MRR data post-amble to next valid command	MRR from Data Buffer address space to any next valid command or MRR from DRAM address space to any next valid command	8	-	8	-	8	-	t_{CK}
t_{MRROD2}	Delay from WR or RD data post-amble to MRR to Data Buffer address space	DRAM WR or RD data to MRR to Data Buffer address space during normal operation or training modes	8	-	8	-	8	-	t_{CK}

Table 155 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5 -3200/ 3600/4000		DDR5-4400		DDR5-4800		
			Min	Max	Min	Max	Min	Max	Unit
t_{MRD2N}	Control word to control word delay in 2N mode	Number of clock cycles between two control word accesses or one control word access and the following DRAM command.	16	-	16	-	16	-	t_{CK}
t_{MRD2N_L}	Control word to control word delay in 2N mode	Number of clock cycles between an access to RW86, RW87, RW88, RW8A, RW8B, RW8C, RW8E, RWA0[7:2], RW90[0], PG[2]RW[FA, F1,F0,E7:E0][3], RWDF[4], PG[5:4]RW[FC:E0] (i.e., any receiver DFE tap coefficient value) and the next control word access or DRAM command.	24	-	24	-	24	-	t_{CK}
t_{MRD2N_L2}	Control word to control word delay in 2N mode	Number of clock cycles between an access to RW80, RW81, RW82, RW83, RW84, RW8F, RW85, RW8D, RW97, RWA1[2:1], RWB0[1:0], PG[1:0]RW[F1:E0], PG8RWE0, PG8RWE1, PG9RW[EF: EE, EA:E7, E3:E0], PG[A]RW[EF:E8, FF:F8],PGBRW[E7:E0] and the next control word access or DRAM command. Number of clock cycles between all PBA related control words (RW81, RW92, RW93).	50	-	50	-	50	-	t_{CK}
t_{MRR2N}	Mode Register Read Pattern to Mode Register Read Pattern Command Spacing in 2N mode	Back-to-back MRRs to Data Buffer or Back-to-Back MRRs to DRAM	16	-	16	-	16	-	t_{CK}
$t_{MRR2NOD1}$	Delay from MRR data post-amble to next valid command in 2N mode	MRR from Data Buffer address space to any next valid command or MRR from DRAM address space to any next valid command	16	-	16	-	16	-	t_{CK}
$t_{MRR2NOD2}$	Delay from WR or RD data post-amble to MRR to Data Buffer address space in 2N mode	DRAM WR or RD data to MRR to Data Buffer address space	16	-	16	-	16	-	t_{CK}
t_{Strap_Setup}	BCOM Strap Setup time from BCOM[2:0] stable to BRST_n HIGH-to-LOW transition	Before BRST_n HIGH-to-LOW transition[8]	32	-	32	-	32	-	t_{CK}
t_{Strap_Hold}	BCOM Strap Hold time from BRST_n LOW-to-HIGH transition to BCOM[2:0] changes	After BRST_n LOW-to-HIGH transition[9]	32	-	32	-	32	-	t_{CK}
t_{Strap_Pulse}	Minimum BRST_n assertion time for BCOM Strap command		64	-	64	-	64	-	t_{CK}
t_{BCOMTM_Entry}	Registration of BCOMTM entry from BRST_n LOW-to-HIGH transition to start of training samples time.	After BRST_n LOW-to-HIGH transition[9]	-	64	-	64	-	64	t_{CK}
t_{BCOMTM_Exit}	Registration of BCOMTM exit from BRST_n LOW-to-HIGH transition to end of training mode.	After BRST_n LOW-to-HIGH transition[9]	-	64	-	64	-	64	t_{CK}
t_{BCOM_1N}	Time for the Data Buffer to change CMD timing from BRST_n LOW-to-HIGH transition.	After BRST_n LOW-to-HIGH transition[9]	-	64	-	64	-	64	t_{CK}
t_{BCOM_Vref}	Time for the BVref to settle from BRST_n LOW-to-HIGH transition.	After BRST_n LOW-to-HIGH transition[9]	-	500	-	500	-	500	ns
t_{PBA_Delay}	Minimum delay from PBA SET ID to PBA SET ID or from PBA SET ID to PBA Exit		tPDA_DQS_Delay_max + BL/2 + 19ns						ns

Table 155 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5 -3200/ 3600/4000		DDR5-4400		DDR5-4800		
			Min	Max	Min	Max	Min	Max	Unit
$t_{PBA\_D-QS\_Delay}$	Delay to rising strobe edge used for sampling DQ during PBA operation[10]		5	18	5	18	5	18	ns
t_{PBA_S}	DQ Setup Time during PBA Enumerate Programming mode		3	-	3	-	3	-	t_{CK}
t_{PBA_H}	DQ Hold Time during PBA Enumerate Programming mode		3	-	3	-	3	-	t_{CK}
t_{WLE}	The time from the MRWDAT0 cycle to the Data Buffer being in DWL and HWL training modes.		-	32	-	32	-	32	t_{CK}
t_{DFETA_Entry}	Time from enabling DFETA to when the first Write command can occur		32	-	32	-	32	-	t_{CK}
$t_{DFE-TA\_LoopU-dateWait}$	Minimum time from the last Write for a particular iteration to the first Write of the next iteration		Min: (DB_WL - tPDM_WR + BL/2 + 64[11,12]) / Max: (-)						t_{CK}
t_{DFETA_Exit}	Time from disabling DFETA to when the next valid command can occur		32	-	32	-	32	-	t_{CK}
t_{RPDX}	Minimum time between PDX and the next valid command other than NOP[13]		Min: max(16 nCK, 10 ns) / Max: (-)						t_{CK}
t_{XS}	DRAM Exit Self Refresh to next valid command not requiring DLL		See DDR5 DRAM Specification						
t_{RINIT1}	Minimum BRST_n LOW time after completion of voltage ramp		200	-	200	-	200	-	µs
	Minimum BRST_n LOW time with stable power		1	-	1	-	1	-	µs
t_{ACT}	Delay from BCK Clock Stop condition to Valid BCK Clock that has reached steady phase and frequency	DB Power-up Initialization (Figure 2), Reset with Stable Power and Stopped Clock (Figure 4), Self Refresh with Clock Stop (Figure 36, Figure 37)	-	10	-	10	-	10	ns
t_{CPDED_DB}	Minimum time of valid BCK clock after received PDE command for Self Refresh		Min: max(16 nCK, 10 ns) / Max: (-)						ns
t_{CSSR_DB}	Minimum time of stopped BCK clock		Min: max(32 nCK, 20 ns) / Max: (-)						ns
$t_{CPDED2SRX\_DB}$	Minimum time between PDE for Self Refresh and BCS_n LOW pulse signaling Self Refresh Exit if BCK clock does not stop		Min: max(24 nCK, 15 ns) / Max: (-)						ns
tZQCAL	ZQ Calibration Time		1	-	1	-	1	-	µs
tZQLAT	ZQ Calibration Latch Time		Min: max(30 ns, 8 nCK) / Max: (-)						ns
$t_{Cont\_Exit\_Delay}$	Registration of MRW Continuous Burst Mode Exit to next valid command delay		128	-	128	-	128	-	t_{CK}
t_{Cont_Exit}	Registration of MRW Continuous Burst Mode Exit to end of training mode		-	128	-	128	-	128	t_{CK}
$t_{TrkCalcInit}$	During t_{DQS2DQ} tracking initialization mode, this is the time from the end of latest DRAM data burst for the second DRAM-space MRR of a pair to the end of the corresponding calculation period[14]	-	-	256	-	256	-	256	t_{CK}

Table 155 — Input Timing requirements

Symbol	Parameter	Conditions	DDR5 -3200/ 3600/4000		DDR5-4400		DDR5-4800		
			Min	Max	Min	Max	Min	Max	Unit
$t_{TrkCalcCur}$	During tDQS2DQ tracking mode, this is the time from the end of latest DRAM data burst for the second DRAM-space MRR of a pair to the end of the corresponding calculation period. This parameter includes tTrKUpdate8.[15]	-	-	256	-	256	-	256	t_{CK}
$t_{TrkUpdate}$	The time for the DB to update MDQ to MDQS delay	-	-	32	-	32	-	32	t_{CK}

1. Including SSC according Section 14.5, “RX Spread Spectrum Clocking (SSC) Capability,” on page 185.
2. All specified timing parameters apply.
3. When Vref settings are updated, it is necessary to meet the Vref settling times defined in Table 189 in addition to meeting t_{MRD_L}.
4. Applies to the timing between MRW that updates the CW Page Control Word and the following MRW or MRR command targeting the paged control word address space (i.e. RWE0 to RWFF).
5. A t_{STAB} waiting time is required when changing the setting in RW84[3:0] (RDIMM Operating Speed) and RW85 (Fine Granularity Operating Speed).
6. For other commands, a waiting time t_{MRD_L2} applies for any control word listed in this set.
7. For other cases of n, see Table 190, “DFE_Vref Specification,” on page 218.
8. Measured to BRST_n HIGH-to-LOW crossing of VIH(DC)_BRST as defined in Table 166 and Figure 85 on page 182.
9. Measured from BRST_n LOW-to-HIGH crossing of VIH(AC)_BRST as defined in Table 166 and Figure 85 on page 182.
10. The range of tPBA_DQS_DELAY specifies the full range of when the minimum of 16 strobe edges can be sent by the host.
11. Results from the equation are rounded up to the next nCK.
12. When DFE Training Acceleration is enabled, the minimum waiting time from the last Write for a particular iteration to the first Write of the next iteration is determined by the larger of tDFETA_LoopUpdateWait [min] specified in this table and the minimum settling time for the parameter setting updated by the Training Accelerator logic (e.g. for DFE_Vref or VrefDQ, the minimum settling time could be much larger than tDFETA_LoopUpdateWait [min]).
13. During the t_{RPDX} window, the host is allowed to take a memory rank still in PDE out of power-down state using one CS_n pulse, but it must refrain from sending any additional commands to any memory rank that has already received its first PDX CS_n pulse. This additional CS_n pulse will appear as a NOP command in the BCOM[2:0]/BCS_n bus. By the end of the t_{RPDX} window, the DDR5DB01 device is required to process BCOM commands as defined in normal operation requirements.
14. This parameter also applies when Periodic Update registers, PG[A]RW[E1, E3, E5, E7], are written directly by MRW command, and it is measured from the last cycle of the MRW sequence on the BCOM[2:0] bus.
15. This parameter also applies when Periodic Update registers, PG[A]RW[F1, F3, F5, F7], are written directly by MRW command, and it is measured from the last cycle of the MRW sequence on the BCOM[2:0] bus.

Table 156 — Output timing requirements[1]

Symbol	Parameter	Conditions	DDR5-3200 to 4800		Unit
			Min	Max	
t_{PDM_RD}	MDQS to DQS Propagation Delay	1.1 V Operation[2,3,4]	1.1 + t_{CK}/4	1.62 + t_{CK}/4	ns
t_{PDM_WR}	DQS to MDQS Propagation Delay	1.1 V Operation[1,2]	1.1 + t_{CK}/4	1.62 + t_{CK}/4	ns
t_{TPM_DQD}	MDQ/MDQS to DQ/DQS and DQ/DQS to MDQ/MDQS Propagation Delay in Transparent Mode[5]	1.1 V Operation [1,2]	0.3	1.25	ns
D_{TPM_DQ}	Delta between shortest and longest propagation delays within each DQx/DQSx and MDQx/MDQSx nibble in Transparent Mode[5]	1.1 V Operation [1,2]	-	0.4	ns
t_{MRD_TM}	Delay between data direction changes in Transparent Mode	Number of clock cycles between Read to Write or Write to Read transactions in Transparent Mode	8[6]	-	t_{CK}
$t_{CMP\_MRD\_DLY}$	DRAM Read data comparator output delay in MRD training mode.[7]		-	16	t_{CK}
$t_{CMP\_MRD\_PW}$	Comparator output pulse width for each MRR operation in MRD training mode.[8]		4	-	t_{CK}
$t_{RCEN2DQ}$	Delay from internal DB Receive Enable to DQ response in MRE Training Mode		-	5	ns
t_{STAB_DB}	Stabilization time for BCK_t/BCK_c[9]	BCK_t/BCK_c stable	-	3.5	µs
t_{STAB_DBVLD}	Stabilization time for commands requiring use of data path[10]	BCK_t/BCK_c stable	-	4.14	µs
t_{STAB_DBCMD}	LRDIMM stabilization time for commands not requiring use of data path[11,12]	RCD DCK_t/DCK_c stable	-	3.5	µs
t_{STAB_DBDATA}	LRDIMM stabilization time for commands requiring use of data path[13,12]	RCD DCK_t/DCK_c stable	-	4.14	µs
$t_{SR\_PARKoff}$	Delay to RTT_PARK disabled by the DB	RTT_PARK disable triggered by PDE for Self Refresh	-	32	t_{CK}
		RTT_PARK disable triggered by Clock Stop condition	-	24	ns
t_{SR_PARKon}	Delay to RTT_PARK enabled by the DB	RTT_PARK enable triggered by first NOP after exit from Clock Stop	-	32	t_{CK}
		RTT_PARK enable triggered by exit from Clock Stop	-	3	µs
t_{RST_PARKon}	Delay to RTT_PARK enabled by the DB	RTT_PARK enable triggered by BRST_n rising edge	-	3.5	µs
t_{BCOMTM_Valid}	Time from sample evaluation to output on DQ pins.		-	20	ns
$t_{BCOMTM\_DQ\_Window}$	Time output is available on DQ pins.		2	-	t_{CK}
t_{WLO_DB}	The MDQx to DQx propagation delay during DWL training mode		0.3	1.25	ns
t_{WLOE_DB}	Delay error between the earliest and the latest DQx during DWL training mode		-	0.4	ns
t_{SDOn}	Delay from MRW command to DQS driven		Min: (-) / Max: max(32 nCK, 20 ns)		ns
t_{SDOff}	Delay from MRW command to DQS disabled		Min: (-) / Max: max(32 nCK, 20 ns)		ns
t_{LB_Entry}	Loopback Mode Entry Time	Delay from MRW that sets RW8D[0] = 1 to valid data driven on LBTXDQ, LBTXDQS.	-	32	t_{CK}
t_{LB_Exit}	Loopback Mode Exit Time	Delay from MRW that sets RW8D[0] = 0 to RTT_Loopback applied on LBTXDQ, LBTXDQS.	-	32	t_{CK}
$t_{DOUT\_LB\_A}$	Rising edge of DQS to rising edge of LBTX-DQS for phase A		-	10	ns
$t_{DOUT\_LB\_B}$	Falling edge of DQS to rising edge of LBTXDQS for phase B		-	10	ns
t_{SK_LBTX}	Skew between LBTXDQS and LBTXDQ for phase A or phase B		tbd	tbd	t_{CK}

Table 156 — Output timing requirements[1]

Symbol	Parameter	Conditions	DDR5-3200 to 4800		Unit
			Min	Max	
$t_{HW\_LBTXDQS}$	LBTXDQS HIGH Pulse width		tbd	tbd	t_{CK}
$t_{LW\_LBTXDQS}$	LBTXDQS LOW Pulse width		tbd	tbd	t_{CK}
t_{LBTXDQ_H}	LBTXDQ Output Time from LBDTXDQS		tbd	tbd	t_{CK}
t_{LBTXDQ_VW}	Data Valid Window of LBTXDQ (t_{LBTXDQ_H} - t_{SK_LBTX})		tbd	tbd	t_{CK}

1. See diagram (Figure 127, "Reference Load for Output Timing and Output Slew Rate," on page 222).
2. These parameters are only guaranteed after the correct speed range has been programmed in RW84[3:0] and RW85.
3. These values are defined for the OP[4:0] bits of the lower and upper nibble Read delay a control words PG[1:0]RW[E5:E4] at their power on default of '00_0000'. The tPDM_RD values are defined for DQS pre-launch settings in RW8F all cleared to zero.
4. The DRAM t_{DQSCK} parameter directly impacts the tPDM_RD/WR budget. These values assume that the DDR5 DRAM tDQSCK parameter is ~0.19 UI.
5. This parameter also applies to DQ Pass Through, as well as HWL and DWL training modes.
6. This value is defined as the minimum dead time between data transfers on the DQ/DQS data bus and the MDQ/MDQS data bus when changing data path direction.
7. Measured from when the last bits of the data burst reach the DDR5DB01 MDQ pins to the last DQ output toggling for a valid comparison result value.
8. DQ LOW pulses are only allowed in case of data comparison mismatch. For a sequence of MRR operations without any data comparison mismatch, the DQ output must remain stable HIGH (i.e. without LOW glitches).
9. This parameter also applies to control word writes to RW84/RW85.
10. Applies only to Self Refresh Exit with Clock Stop and frequency change. See timing diagrams in Figure 36 and Section 37 on page 30.
11. Measured from start of RCD DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface but does not require the use of data path (e.g., SRX, NOP, etc.).
12. Applies only to Self Refresh Exit with Clock Stop but without frequency change. See timing diagrams in Figure 38 and Figure 39 on page 31.
13. Measured from start of RCD DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the LRDIMM BCOM bus interface and requires the use of data path (e.g., WR, RD).

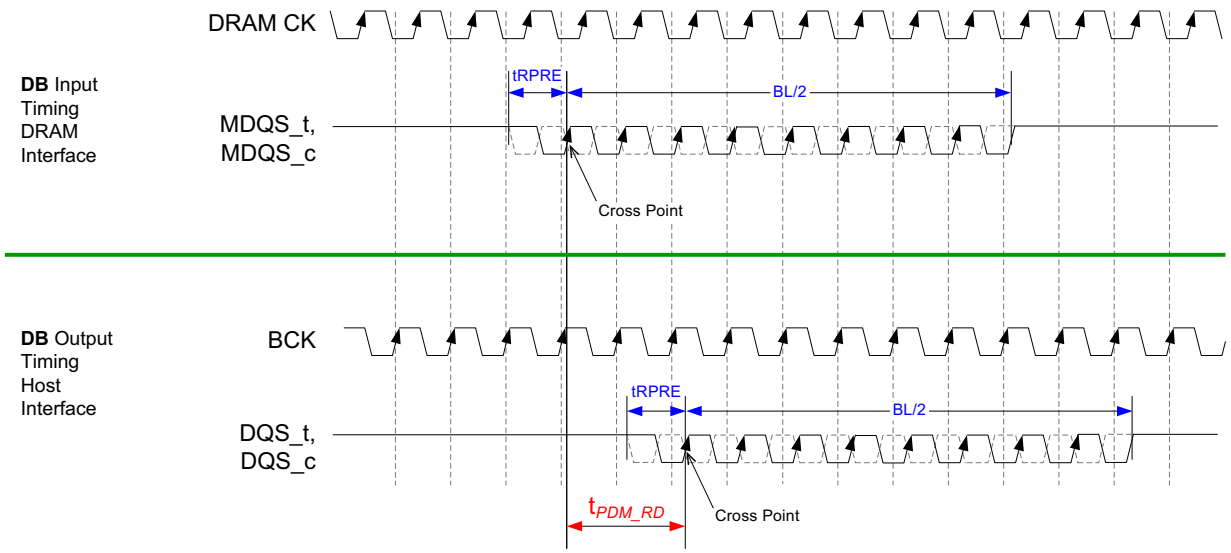
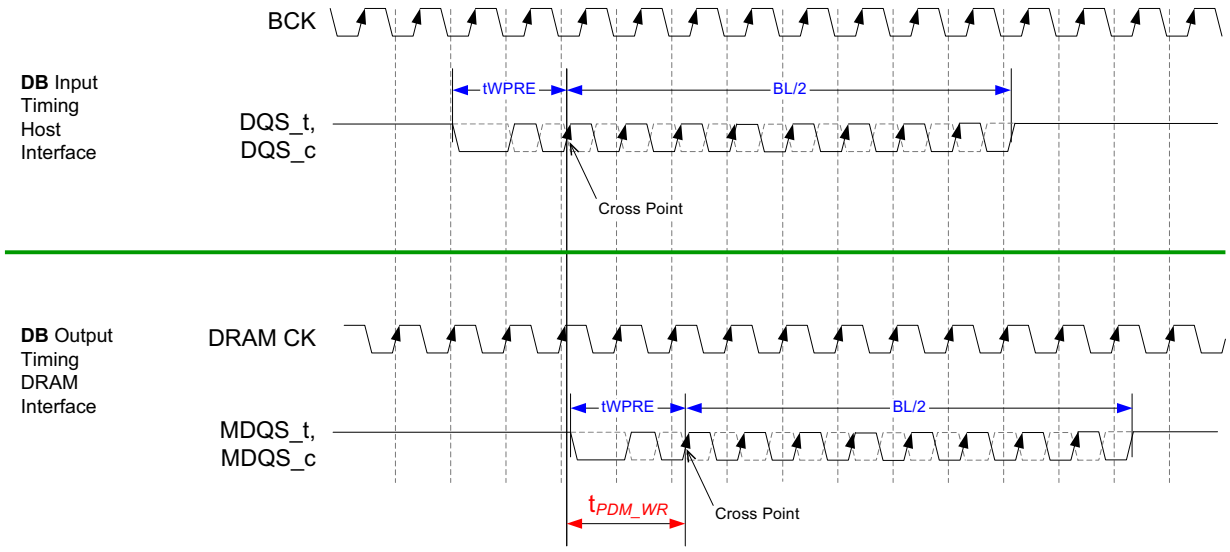


Figure 69 — tPDM_RD Latency Measurement



tPDM_WR = DQS (Host Interface) Input to MDQS (DRAM Interface) Output

Figure 70 — tPDM_WR Latency Measurement

11.1 DDR5DB01 Operating Specification for Different Package Ranks

Table 157 — DDR5DB01 Operating Specification for Different Package Ranks (from Rx to Ry)

Type	Symbol	Parameter	DDR5 - 3200-4800		Units
			Min[1, 2, 3]	Max	
RD-RD	T_{RDRD}	Read to Read Command Spacing	t_{RPRE} + BL/2 + [t_{RPST} – 0.5] + max [MRE(Rx) – MRE(Ry), [MRE(Rx) + MDQS_RD_Dly(Rx) – MRE(Ry) – MDQS_RD_Dly(Ry)]] + 2	-	tCK (avg)
WR-WR	T_{WRWR_MDQS}	Write to Write Command Spacing	t_{WPRE} + BL/2 + [t_{WPST} – 0.5] + [DWL(Rx) – DWL(Ry)] + 2	-	tCK (avg)
	T_{WRWR_MDQ}	Write to Write Command Spacing	BL/2 + [DWL(Rx) + tFinalWriteDelay(Rx)[4]] – [DWL(Ry) + tFinalWriteDelay(Ry)[4]] + 2	-	tCK (avg)
RD-WR	T_{RDWR_DQS}	Read to Write Command Spacing	t_{PDM_RD}(max)[5] + t_{PDM_WR}(max) + t_{WPRE} + BL/2 + 2 + [t_{RPST} – 0.5] – DQS_Prelauch + [MRE(Rx) – DWL(Ry)] + 2	-	tCK (avg)
	T_{RDWR_DQ}	Read to Write Command Spacing	t_{PDM_RD}(max)[5] + t_{PDM_WR}(max) + BL/2 + 2 + [0.25 – tRx_DQS2DQ(max)[6]] + [MRE(Rx) – DWL(Ry)] + 2	-	tCK (avg)
WR-RD	T_{WRRD_MDQS}	Write to Read Command Spacing	t_{RPRE} + BL/2 – 2 + [t_{WPST} – 0.5] + [DWL(Rx) – MRE(Ry)] + 2	-	tCK (avg)
	T_{WRRD_DQS}	Write to Read Command Spacing	t_{RPRE} – t_{PDM_RD}(min)[5] – t_{PDM_WR}(min) + BL/2 – 2 + [t_{WPST} – 0.5] + DQS_Prelauch + [DWL(Rx) – MRE(Ry)] + 2	-	tCK (avg)
	T_{WRRD_MDQ}	Write to Read Command Spacing	BL/2 – 2 + tFinalWriteDelay(Rx)[4] + [0.25 – tMDQS_RD_Dly[7]] + [DWL(Rx) – MRE(Ry)] + 2	-	tCK (avg)

1. The host is required to meet all of the minimum values in this table.
2. For each equation, Rx and Ry must be selected so that the equation is maximized.
3. The result of each equation is rounded up to the nearest tCK.
4. Note: tFinalWriteDelay(Rx) = tMdqWriteBaselineDelay(Rx) + tDram_DqsDelay_Change(Rx) + Per-bit_MDQ_Write_Delay. tDram_DqsDelay_Change can be positive or negative, can vary between periodic updates, and it is constrained by tDQS2DQ_temp and tDQS2DQ_volt parameters defined in the DDR5 SDRAM specification.
5. In some implementations, t_{PDM_RD} may include adjustment for PG[1:0]RW[E5:E4].
6. Refer to Table 173, “Rx [M]DQS Jitter Sensitivity Specification for DDR5-3200 to 4800,” on page 194.
7. MDQ Read timing offset from PG[1:0]RW[E5:E4].

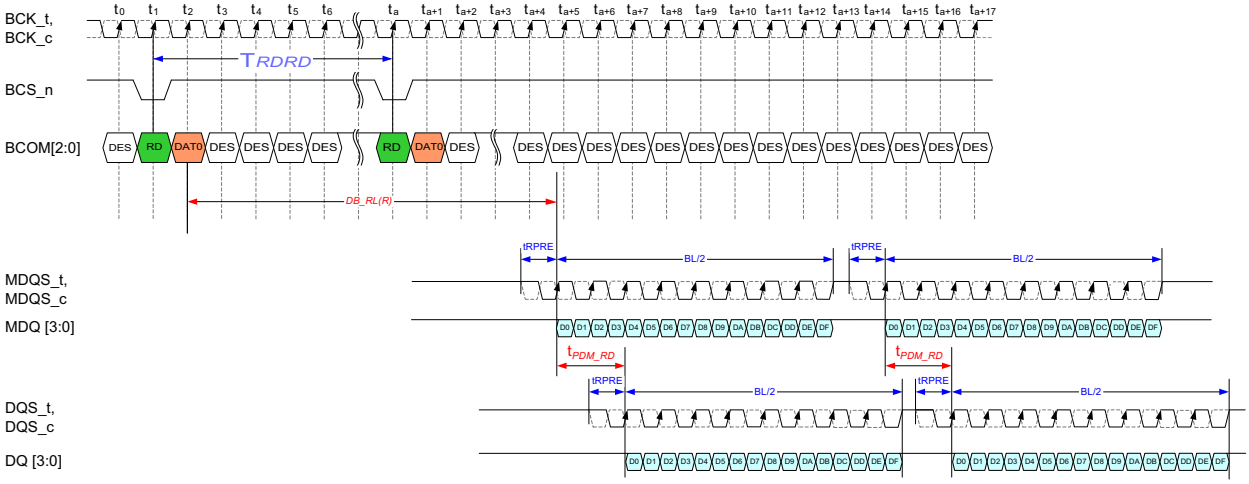


Figure 71 — Read to Read Command Spacing

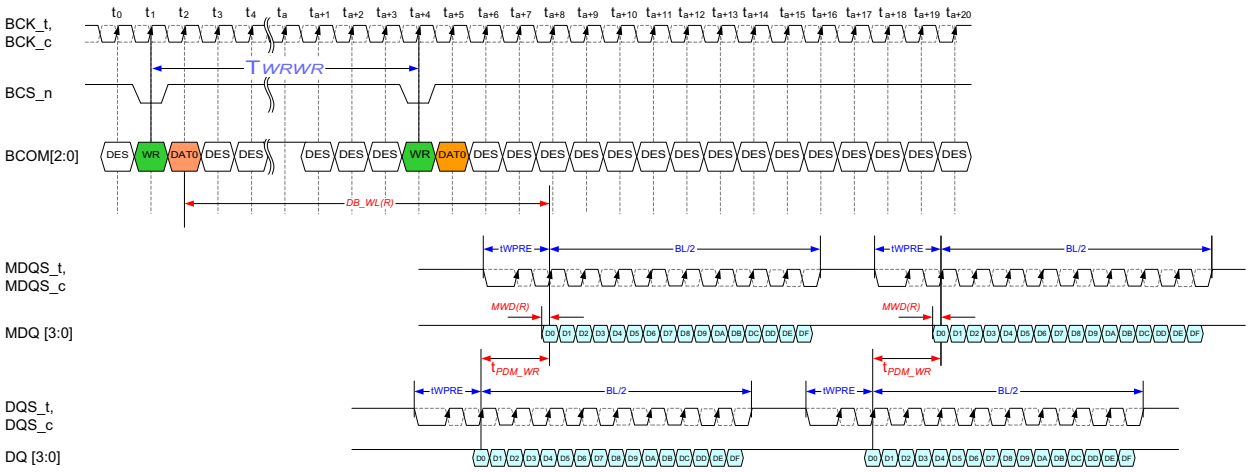


Figure 72 — Write to Write Command Spacing

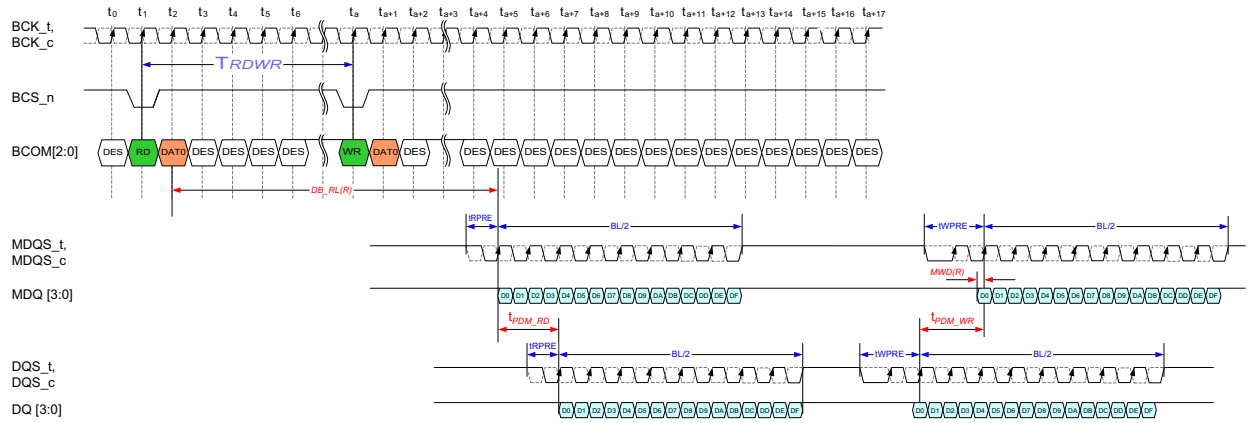


Figure 73 — Read to Write Command Spacing

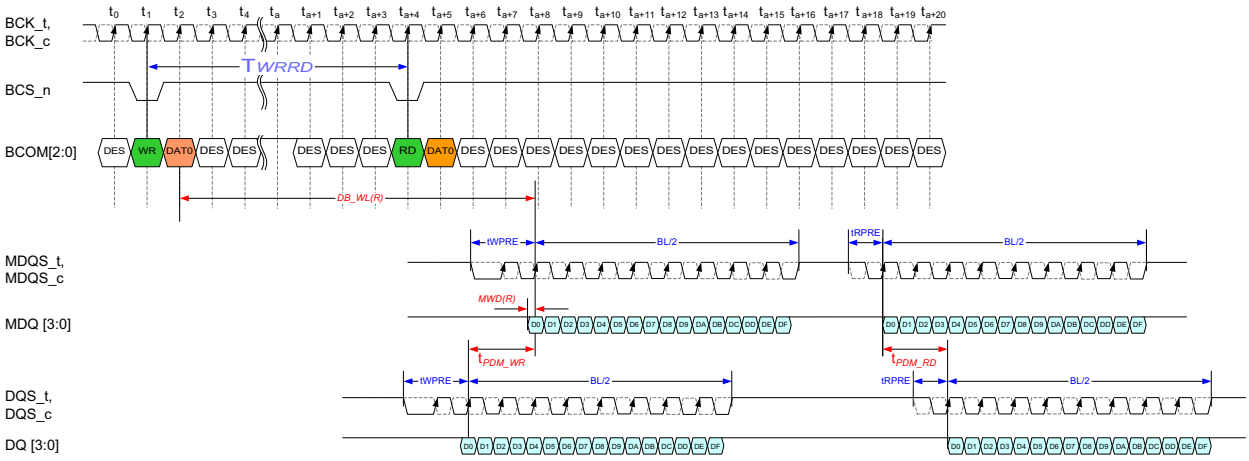
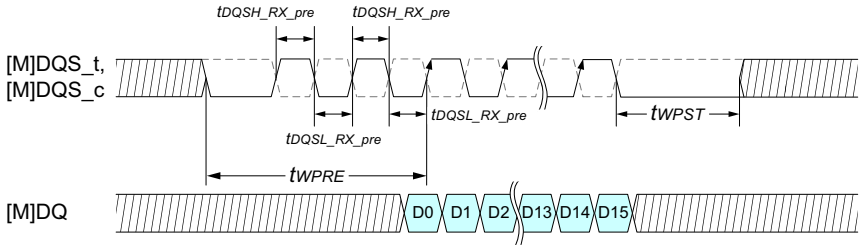


Figure 74 — Write to Read Command Spacing

11.2 Preamble Timings

11.2.1 RX Preamble Timings

During Write and Read operations, input receiver aligns the strobe with [M]DQ according to the preamble settings, and strobe should meet timing requirements (tDQSH_RX_pre, tDQSL_RX_pre) to guarantee enough timing margin by setting the window for strobe during the preamble time frame. On the Host DQ interface of the DDR5DB01 device, this timing requirement is applied to all configurations of preamble set by PG[8]RWE1[4:3], which is 2 t_{CK}, 3 t_{CK}, and 4 t_{CK} Write preamble, for Write to Write operations as well as normal Write operations. On the DRAM MDQ interface of the DDR5DB01 device, this timing requirement also applies to all configurations of preamble set by PG[8]RWE1[2:0], which are 1 t_{CK}, 2 t_{CK}(0010 Pattern), 2 t_{CK} (1110 pattern), 3 t_{CK}, and 4 t_{CK} Read preamble, for Read to Read operations as well as normal Read operations.



Note(s):

1. BL = 16, 4tCK Preamble
2. tDQSH_RX_pre and tDQSL_RX_pre are shown, and they apply to all toggles during preamble.
3. A second preamble during Write-to-Write or Read-to-Read operation will follow same requirement.

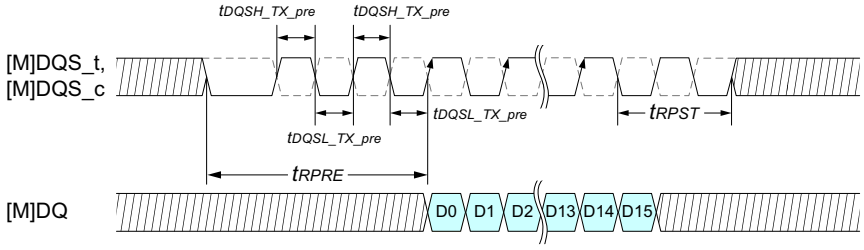
Figure 75 — [M]DQS Timing for Input Preamble during Write or Read Operations

Table 158 — Input Strobe Preamble Timing Parameters

Symbol	Parameter	DDR5 -3200/ 3600/4000		DDR5-4400		DDR5-4800		
		Min	Max	Min	Max	Min	Max	Unit
$t_{DQSL\_RX\_pre}$	Strobe's window of differentially LOW during Input preamble	TBD	TBD	TBD	TBD	TBD	TBD	t_{CK}
$t_{DQSH\_RX\_pre}$	Strobe's window of differentially HIGH during Input preamble	TBD	TBD	TBD	TBD	TBD	TBD	t_{CK}

11.2.2 TX Preamble Timings

During Write and Read operations the transmitted output strobe will meet timing requirements (tDQSH_TX_pre, tDQSL_TX_pre) to guarantee enough timing margin by setting the window for strobe during the preamble time frame. On the Host DQ interface of the DDR5DB01 device, this timing requirement is applied to all configurations of preamble set by PG[8]RWE1[2:0], which are 1 t_{CK}, 2 t_{CK}(0010 Pattern), 2 t_{CK} (1110 pattern), 3 t_{CK}, and 4 t_{CK} Read preamble, for Read to Read operations as well as normal Read operations. On the DRAM MDQ interface of the DDR5DB01 device, this timing requirement also applies to all configurations of preamble set by PG[8]RWE1[4:3], which is 2 t_{CK}, 3 t_{CK}, and 4 t_{CK} Write preamble, for Write to Write operations as well as normal Write operations.



Note(s):

1. BL = 16, 4tCK Preamble
2. tDQSH_TX_pre and tDQSL_TX_pre are shown, and they apply to all toggles during preamble.
3. A second preamble during Write-to-Write or Read-to-Read operation will follow same requirement.

Figure 76 — [M]DQS Timing for Output Preamble during Write or Read Operations

Table 159 — Output Strobe Preamble Timing Parameters

Symbol	Parameter	DDR5 -3200/3600/ 4000		DDR5-4400		DDR5-4800		
		Min	Max	Min	Max	Min	Max	Unit
$t_{DQSL\_TX\_pre}$	Strobe's window of differentially LOW during Output preamble	TBD	TBD	TBD	TBD	TBD	TBD	t_{CK}
$t_{DQSH\_TX\_pre}$	Strobe's window of differentially HIGH during Output preamble	TBD	TBD	TBD	TBD	TBD	TBD	t_{CK}

12 Electrical - Absolute Maximum Ratings

12.1 Absolute maximum ratings

Table 160 — Absolute maximum ratings over operating free-air temperature range

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V_{DD}	Supply voltage		– 0.3	1.4	V	1
V_{IN}	Receiver input voltage	See Note 2 and 3	– 0.3	V_{DD} + 0.5	V	1, 2, 3
V_{OUT}	Driver output voltage	See Note 2 and 3	– 0.3	V_{DD} + 0.5	V	1, 2, 3
I_{IK}	Input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{DD}$	-	-50	mA	1
I_{OK}	Output clamp current	$V_{OUT} < 0$ or $V_{OUT} > V_{DD}$	-	± 50	mA	1
I_{OUT}	Continuous output current	$0 < V_{OUT} < V_{DD}$	-	± 50	mA	1
I_{CCC}	Continuous current through each V_{DD} or V_{ss} pin		-	± 100	mA	1
T_{stg}	Storage temperature		– 55	+ 100	°C	1

NOTE(s):

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 1.4 V maximum.

12.2 Operating Electrical Characteristics

The DDR5DB01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 161 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit	Notes
V_{DD}	DC Supply voltage	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V	1
T_j	Junction temperature		0	-	125	°C	2
T_{case}	Case temperature	Measurement procedure JESD51-2	-	-	103	°C	3

NOTE(s):
1. DC bandwidth limited to 20 MHz.
2. For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
3. This spec is meant to guarantee a Tj of 125 °C by the DDR5DB01. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a DDR5DB01 shall not be higher than 125 °C.

13 AC and DC Global Definitions

13.1 Transmitter (Tx), Receiver (Rx) and Channel Definitions

Transmitter (Tx): Input to the transmitter is the data from the logical portion of the Data Buffer Core and output is at the package pins. The normal components contained in the transmitter are, but not limited to, the pre-driver and the output driver with the transmitter package. The DDR5 Data Buffer uses a differential forwarded strobe-source synchronous system, and single-ended data. The transmitter for a forwarded-strobe-based source synchronous system must include specification and test methodology for low and high frequency random and deterministic jitter and duty cycle error and must take into account Bounded Uncorrelated Jitter (BUJ), Duty cycle error etc. For single ended signaling cases, crosstalk and Simultaneous switching noise often impact the measurement of the Transmitter. Therefore, the Transmitter's decimated jitter component parameters and the BER must be specified.

Receiver (Rx): The normal components contained in the strobe receiver are: (1) receiver package, (2) input amplifier (to receive the strobe), and (3) optionally, a DLL and time adjustment circuitry, although these are typically not present in the DRAM or the Data Buffer, and distribution circuitry to distribute the strobe to all the receivers. The data input receives the single ended data and measures it against a reference voltage. The difference between the received signal and reference voltage is then sampled. However, the link may need some form of receiver equalization at the speeds that the DDR5 link needs to operate. Since there may not be input eye margin at the receiver pin, the receiver equalization specification may be defined based on a virtual receive sampler/slicer. This means that components of the receiver, which have nothing to do with inter symbol interference (ISI), will have to be specified in such a way as to avoid the impact of ISI. Hence items like receiver jitter, receiver jitter sensitivity, receiver amplitude sensitivity, which are typically orthogonal to ISI, will have to be specified in an ISI free environment. Either the infrastructure, or the test methodology will ensure that the correct amount of ISI, or no ISI, as the case might be, for that specific Rx parameter is used. The validation of the receiver is also dependent on either loop-back of data being enabled or restricting to receiver testing to be dependent on a pre-specified set of patterns and the accompanying pattern checker and error counters. The Receiver equalization will be evaluated in the presence of a set of pre-specified receiver testing golden channels. These receiver testing golden channels will attempt to span the ISI range to which the receiver needs to be designed. The key measurement parameter in this test is the stressed eye and the receiver's error sensitivity to the stressed eye. The requirements for these test features are described in APPENDIX - Clock, DQS and DQ Validation Methodology.

Channel: The channel is defined from the transmitter package pin to the receiver package pin and includes all the interconnect topology components included in the channel definition (connectors, sockets, and so on).However, this spec will not specify system platform level channel models and it will restrict itself to specifying the Golden Reference Transmitter and Receiver evaluation channels.

13.2 Bit Error Rate

Introduction

This section provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

13.2.1 General Equation

$$n = \left(\frac{1}{BER}\right)\left[-\ln(1-SLC) + \ln\left(\sum_{k=0}^{N}\frac{(n\cdot BER)^{k}}{k!}\right)\right]$$

Where:

n = number of bits in a trial

SLC = statistical level of confidence

BER = Bit Error Rate

k = intermediate number of specific errors found in trial

N = number of errors recorded during trial

If no errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left(\frac{1}{BER}\right)[-\ln(1-SLC)]$$

Testing to 99.5% confidence levels is recommended; however, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or N=0), using BER=10^{-9} and confidence level SLC=99.5%, the result is n=(1/BER)(-ln(1-0.995)) = 5.298 x109.

Results for commonly used confidence levels of 99.5% down to 70% are shown in Table 162.

Table 162 — Estimated Number of Transmitted Bits (n) for confidence level of 70% to 99.5%

Number of Error	n = ln(1 - SLC)/BER							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/*BER*	4.61/*BER*	2.99/*BER*	2.3/*BER*	1.90/*BER*	1.61/*BER*	1.39/*BER*	1.20/*BER*

13.2.2 Minimum Bit Error Rate (BER) Requirements

Table 163 specifies the UI_{AVG} and Bit Error Rate requirements over which certain receiver timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER = E^{-9}.

Table 163 — Minimum BER Requirements for RX Timing and Voltage Tests

Symbol	Parameter	DDR5-3200 - 4800			Unit	NOTE
		Min	Nom	Max		
UI_{AVG}	Average UI	0.999* nominal	1.000/f	1.001* nominal	ps	1
$N_{MIN\_UI\_Validation}$	Number of UI (min)	5.3×10^{9}		-	UI	2
BER_{Lane}	Bit Error Rate	-		E^{-16}	Events	3, 4, 5, 6

NOTES:
1. Average UI size, "f" is data rate.
2. # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at BER = E^{-9}.
3. This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link-layer-based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver, therefore, this parameter must be validated in selected systems using a suitable methodology as deemed by the platform.
4. Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.
5. This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx CA Voltage Sensitivity, Rx Clock Jitter Sensitivity, Rx CA Stressed Eye, Tx Clock Jitter, Tx QCA Jitter, and Tx QCA Stressed EH/EW specifications.
6. The BER for DDR5 during normal operation is E^{-16}. For validation purposes, the BER used is E^{-9}.

13.2.3 Unit Interval and Jitter Definitions

This document describes the UI and NUI Jitter definitions associated with the Jitter parameters specified in Rx Stressed Eye, Tx DQS Jitter, Tx DQ Jitter and Input Clock Jitter specifications.

13.2.4 Unit Interval

The times at which the differential crossing points of the clock occur are defined at t_1, t_2, …, t_{n-1}, t_n,..., t_K.

The UI at index "n" is defined as shown in Figure 77 (with n = 1,2,…) from an arbitrary time in steady state, where n = 0 is chosen as the starting crossing point.

Mathematical definition of UI is shown in Figure 77 and Figure 78.

$$\mathrm{UI}_n = t_n - t_{n-1}$$

Figure 77 — UI Definition in Terms of Adjacent Edge Timings

For the Single-Ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the BCK_t and BCK_c intersect (see Figure 78).

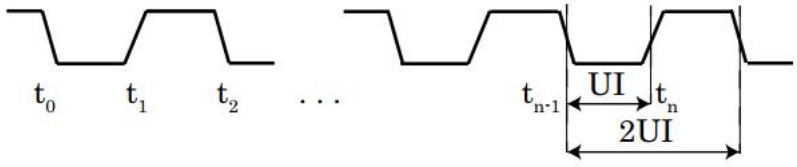


Figure 78 — UI definition Using Clock Waveforms

13.2.5 UI Jitter Definition

If a number of UI edges are computed or measured at times $t_1, t_2, \ldots, t_{n-1}, t_n, \ldots, t_K$, where K is the maximum number of samples, then the UI jitter at any instance "n" is defined in Figure 79, where T = the ideal UI size.

$$\mathrm{UI}_{(jit)n} = (t_n - t_{n-1}) - T;\ n = 1, 2, 3, \ldots, K$$

Figure 79 — UI Jitter of the "nth" UI Definition (in terms of ideal UI)

In a large sample with random Gaussian-like jitter (therefore very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in Figure 79 assumes starting from an instant of steady state, where n=0 is chosen as the starting point. 1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (*BER*) for the link.

13.2.6 UI-UI Jitter Definition

UI-UI (read as "UI to UI") jitter is defined to be the jitter between two consecutive UI as shown in Figure 80.

$$\mathrm{UI}_n = \mathrm{UI}_n - \mathrm{UI}_{n-1};\ n = 2, 3, \ldots, K$$

Figure 80 — UI - UI Jitter Definitions

13.2.7 Accumulated Jitter (Over "N" UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive "N" UI as shown in Figure 81.

$$T_{acc}^{N} = \sum_{p=m}^{m+N-1} (UI_p - \overline{UI}), \text{ where } m = 1, 2, ..., K\text{-}N$$

Figure 81 — Definition of Accumulated Jitter (over "N" UI)

where UI is defined in the equation shown in Figure 82.

$$\overline{UI} = \frac{\sum_{p=1}^{K} UI_p}{K}, \text{ where } p = 1, 2, ..., N, ..., K$$

Figure 82 — Definition of UI

14 RX Input Specification

14.1 [M]DQ/[M]DQS On Die Termination DC Electrical Characteristics

A functional representation of the on-die termination is shown in the figure below.

$$RTT = \frac{V_{DD} - V_{OUT}}{|I_{OUT}|}$$

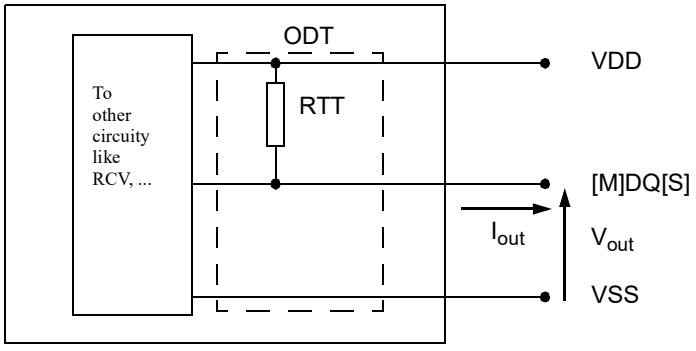


Figure 83 — On Die Termination

On Die Termination effective Rtt values supported are 240,120, 80, 60, 48, 40, 34 ohms (in addition to RTT_OFF).

The values in Table 164 are valid for the entire operating temperature range after proper ZQ calibration and assume R_{ZQ} = 240 Ω +/– 1%.

Table 164 — ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/1	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/1	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/1	1,2
120Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/2	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/2	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/2	1,2
80Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/3	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/3	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/3	1,2
60Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/4	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/4	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/4	1,2
48Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/5	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/5	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/5	1,2
40Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/6	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/6	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/6	1,2
34Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/7	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/7	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/7	1,2
[M]DQ-[M]DQ Mismatch Within Device	VOMdc = 0.8 * VDD	0	-	8	%	1,2,3,4

NOTE:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Section 15.3 on page 199
2. Pull-up ODT resistors are recommended to be calibrated at 0.8 * VDD. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDD and 0.95 * VDD.
3. [M]DQ to [M]DQ mismatch within device variation for a given component including [M]DQS_t and [M]DQS_c (characterized).
4. RTT variance range ratio to RTT nominal value in a given component, including [M]DQS_t and [M]DQS_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{\text{RTT}_{\text{MAX}} - \text{RTT}_{\text{MIN}}}{\text{RTT}_{\text{NOM}}} \times 100$$

14.2 LBTXDQ/LBTXDQS On Die Termination DC Electrical Characteristics

The DDR5DB01 device includes On-Die Termination resistance for the Loopback signals LBTXDQS and LBTXDQ. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DDR5DB01 devices via Control Word setting.

A functional representation of the on-die termination is shown in the figure below.

$$RTT = \frac{V_{DD} - V_{OUT}}{|I_{OUT}|}$$

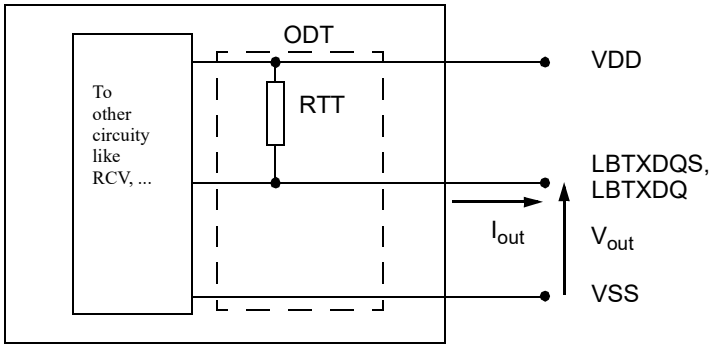


Figure 84 — Functional Representation of Looback On Die Termination

DDR5DB01 supports an effective Rtt On Die Termination value of 48 ohms (in addition to RTT_OFF) for Loopback signals.

The values in Table 165 are valid for the entire operating temperature range after proper ZQ calibration and assume R_{ZQ} = 240 Ω +/– 1%.

Table 165 — Loopback ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
48Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/5	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/5	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/5	1,2
Mismatch LBTXDQS - LBTXDQ Within Device	VOMdc = 0.8 * VDD	0	-	8	%	1,2,3,4

NOTE:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Section 15.3 on page 199
2. Pull-up ODT resistors are recommended to be calibrated at 0.8 * VDD. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDD and 0.95 * VDD.
3. Loopback ODT mismatch within device variation for a given component including LBTXDQS and LBTXDQ (characterized).
4. RTT variance range ratio to RTT nominal value in a given component, including LBTXDQS and LBTXDQ.

$$\text{LBTXDQS-LBTXDQ Mismatch in a Device} = \frac{RTT_{MAX} - RTT_{MIN}}{RTT_{NOM}} \times 100$$

14.3 Input CMOS Rail-to-Rail Levels for BRST_n

Table 166 — CMOS Rail-to-Rail Input Levels for BRST_n

Symbol	Parameter	Min	Max	Unit	NOTE
VIH(AC)_BRST	AC Input HIGH Voltage	0.8 * V_{DD}	V_{DD}	V	4
VIH(DC)_BRST	DC Input HIGH Voltage	0.7 * V_{DD}	VDD	V	2
VIL(DC)_BRST	DC Input LOW Voltage	VSS	0.3*VDD	V	1
VIL(AC)_BRST	AC Input LOW Voltage	VSS	0.2*VDD	V	5
TR_BRST	Rise Time	-	1	µs	
tPW_BRST	Minimum BRST_n pulse width	t_{Strap_Pulse}(min)	-	t_{CK}	3, 6

NOTE 1: After BRST_n is registered LOW, BRST_n level shall be maintained below VIL(DC)_BRST during tPW_BRST.
NOTE 2: Once BRST_n is registered HIGH, BRST_n level must be maintained above VIH(DC)_BRST.
NOTE 3: This definition is applied only in BCOM Strap Command sequences (see Figure 53, “Strap Example,” on page 52).
NOTE 4: Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 5: Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.
NOTE 6: tPW_BRST is the minimum LOW pulse width supported by the BRST_n input buffer based on parameter t_{Strap_Pulse} at the maximum operating frequency. See Table 155 on page 163.

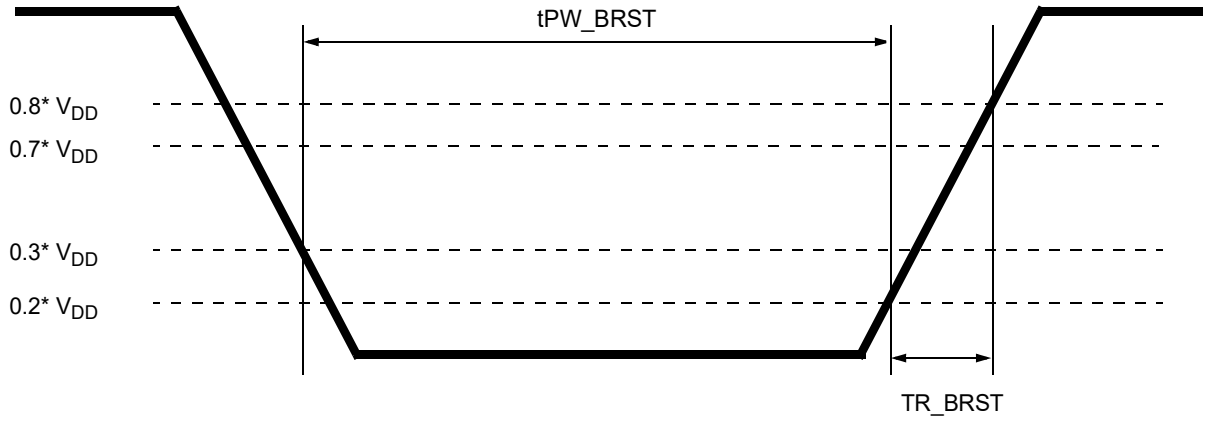


Figure 85 — BRST_n Input Slew Rate Definition

14.4 RX BCOM Input Receiver Specifications

Note: The following draft assumes internal BVref.

The BCS_n and BCOM input receiver mask for voltage and timing is shown in Figure 86. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR5DB01 input receiver to successfully capture a valid input signal. The mask is a receiver property for each pin, and it is not the valid data eye.

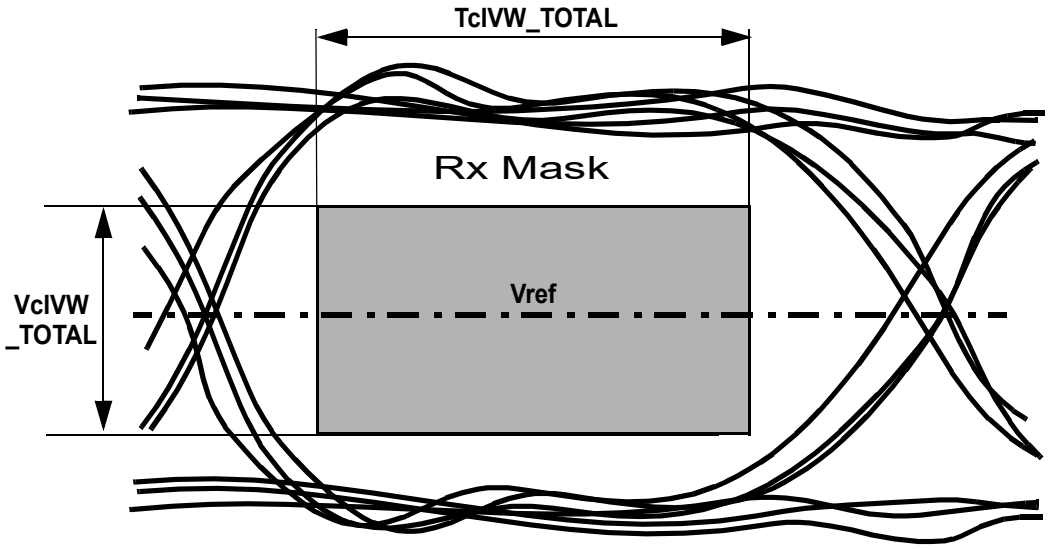


Figure 86 — BCS_n and BCOM Receiver Mask

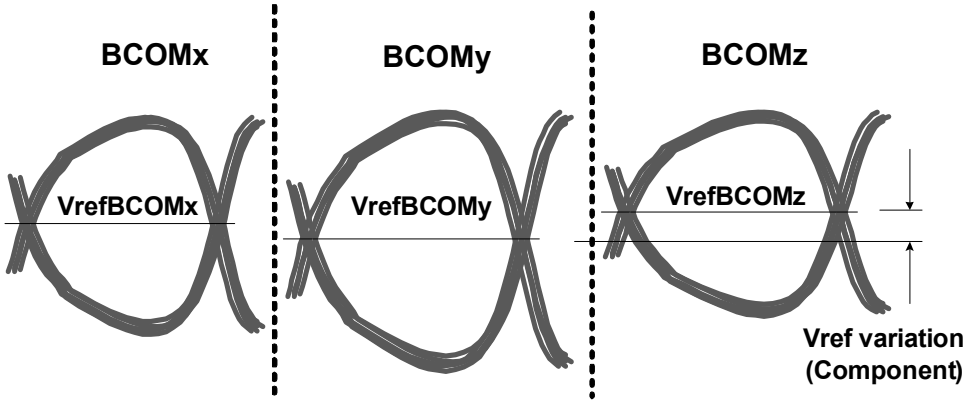
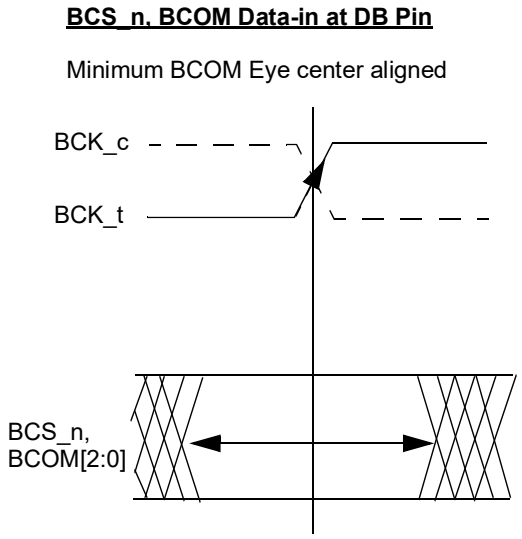
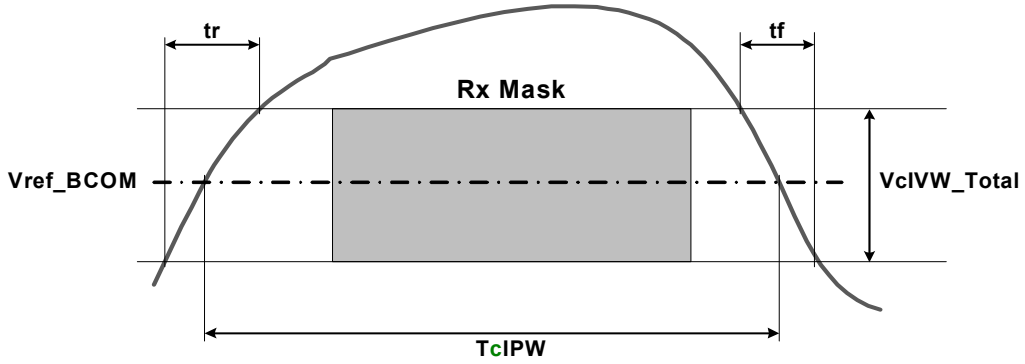


Figure 87 — Across pin BCOM voltage variation



TcIVW for all BCOM signals is defined as centered on the BCK_t/BCK_c crossing at the DB pin

Figure 88 — BCOM Timings at the Data Buffer



NOTE 1: SRIN_cIVW = VcIVW_TOTAL / (tr or tf)

Figure 89 — BCOM TcIPW and SRIN_cIVW definition (for each input pulse)

Table 167 — CTRL RX Receiver Voltage Margin and AC Timing by Speed Bin for DDR5 3200 - 4800

Speed		DDR5 -3200		DDR5-3600 to 4000		DDR5-4400 to 4800		Unit	Note
Symbol	Parameter	Min	Max	Min	Max	Min	Max		
Data Voltage and Timing									
VcIVW_TOTAL	Rx Mask p-p voltage total	-	90	-	85	-	80	mV	1,2, 3, 4
TcIVW_TOTAL	Rx timing window total	-	0.15	-	0.147	-	0.145	UI	1, 4
TcIPW	CTRL input pulse width	0.4	-	0.38	-	0.36	-	UI	5
tBCK2CTRL	BCK to CTRL offset	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	6
tCTRLCTRL	CTRL to CTRL offset	-	0.04	-	0.04	-	0.036	UI	7
SRIN_cIVW	Input Slew Rate over VcIVW_TOTAL	1	10	1	10	1	10	V/ns	8

* UI=tck(avg)min

NOTE 1: CTRL Rx mask voltage and timing total input valid window where VcIVW is centered around BVref. The CTRL Rx mask is applied per bit and includes voltage and temperature drift terms.

NOTE 2: Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above BVref and at least half of VcIVW_TOTAL(max) below BVref.

NOTE 3: The VcIVW voltage levels are centered around BVref.

NOTE 4: Overshoot and Undershoot Specifications see Section 14.16.

NOTE 5: CTRL minimum input pulse width defined at the BVref.

NOTE 6: BCK to CTRL is defined as the input offset for each CTRL input in the DDR5DB01 device measured at the package balls. Includes all DDR5DB01 process, voltage and temperature variation.

NOTE 7: CTRL to CTRL offset is defined as the magnitude of difference between the min and max BCK to CTRL offset at the DDR5DB01 package balls for a given component. Includes all DDR5DB01 voltage and temperature variation.

NOTE 8: Input slew rate over VcIVW Mask centered at BVref. For a given measurement, under the same conditions, the applied slew rate for all transition edges (slowest to fastest) must be within 2 V/ns of each other. This single-ended slew rate also applies to BCK_t and BCK_c.

14.5 RX Spread Spectrum Clocking (SSC) Capability

The system platform uses a reference clock, which is used to synthesize the Data Buffer clock. Spread Spectrum Clock (SSC) with up to –0.5% down spread in frequency must be supported by the clocking system. The frequency of the reference clock and therefore bit rate can be modulated from 0% to –0.5% of the nominal data rate/frequency, at a modulation rate in the range of 30 kHz to 33 kHz. The modulation profile of SSC must provide optimal or close to optimal EMI reduction. Typical profiles include a triangular profile. The DDR5DB01 must ensure that it functions normally even in the presence of SSC and truthfully lets SSC related components pass through to its output signals.

14.6 Input Single-ended Swing Requirements for Differential Clock

TBD

14.7 Input Slew Rate for Differential Clock (BCK_t, BCK_c)

Input slew rate for differential signals BCK_t/BCK_c are defined and measured as shown below.

Table 168 — Differential Input Slew Rate Definition for BCK_t/BCK_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
V_{IHdiff_CK}	Differential Input HIGH	0.75 * V_{DIFFpp}	-	mV	1, 2, 3, 4
V_{ILdiff_CK}	Differential input LOW	-	0.25 * V_{DIFFpp}	mV	1, 2, 3, 4

NOTE 1: Clock V_{DIFFpp}, V_{ILdiff_CK} and V_{IHdiff_CK} are defined in Figure 90.
NOTE 2: V_{DIFFpp} is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.
NOTE 3: Differential signal rising edge from V_{ILdiff_CK} to V_{IHdiff_CK} must be monotonic slope.
NOTE 4: Differential signal falling edge from V_{IHdiff_CK} to V_{ILdiff_CK} must be monotonic slope.

Table 169 — Differential Input Slew Rate BCK_t/BCK_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
SRIdiff	Differential Input Slew Rate	2	18	V/ns	1

NOTE 1: All parameters are defined over the entire clock common mode range.

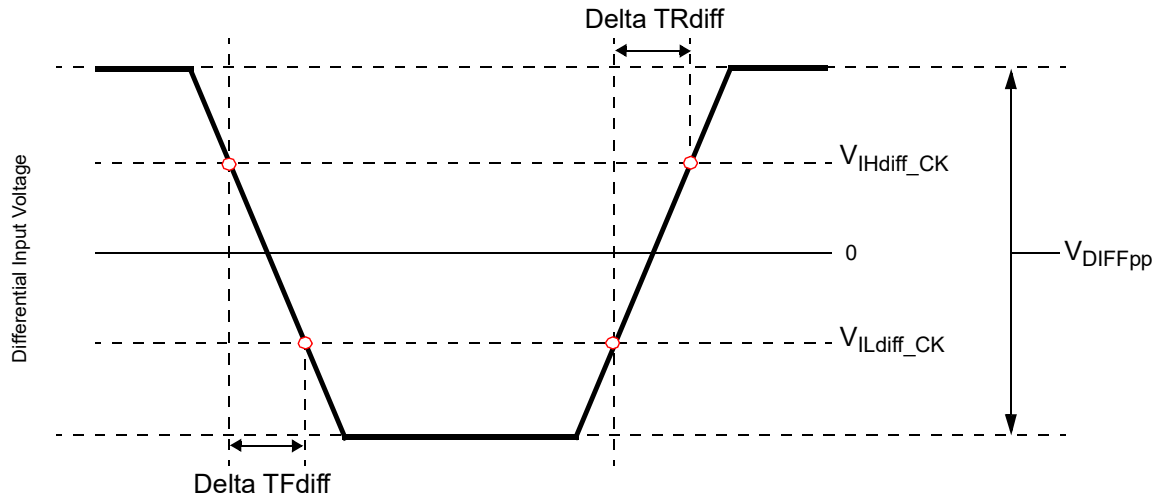


Figure 90 — Differential Input Slew Rate Definition for BCK_t/BCK_c

14.8 Input Clock Differential Cross Point Voltage

To achieve input BCOM[2:0]/BCS_n requirements as well as output skew parameters with respect to clock, the cross point voltage of differential input clock signals (BCK_t, BCK_c) must meet the requirements in Figure 91. The differential input cross point voltage VIX_CK (VIX_CK_FR and VIX_CK_RF) is measured from the actual cross point of BCK_t, BCK_c relative to the Vswing/2 of the BCK_t and BCK_c signals.

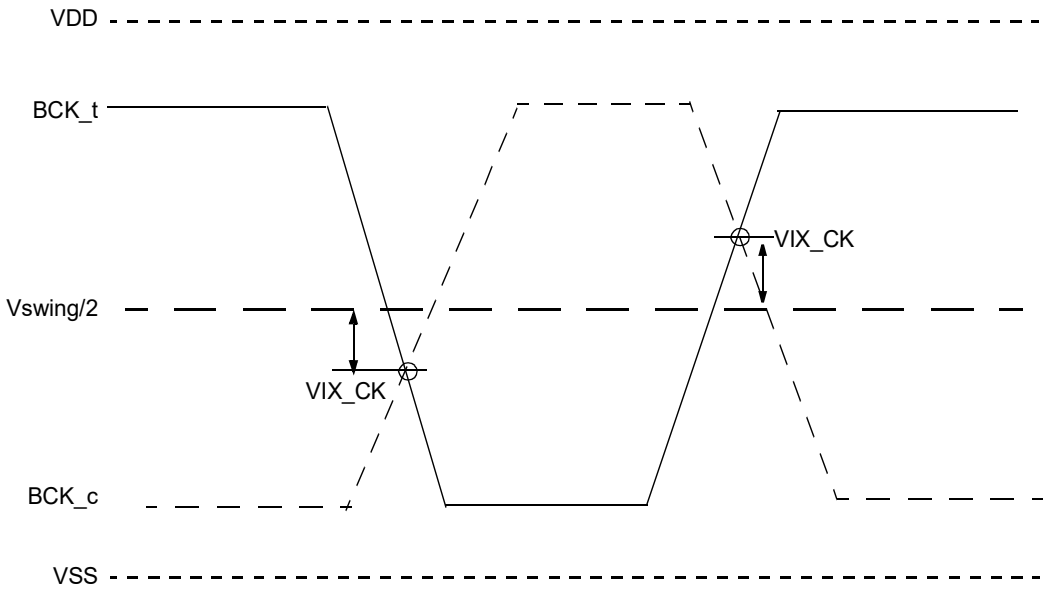


Figure 91 — Vix Definition (BCK)

Table 170 — Cross point voltage (VIX) for differential input signals (BCK)

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000/4400/4800		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
VIX_CK_Ratio	Clock differential input crosspoint voltage ratio	-	25	-	25	-	25	%	1, 2

NOTE(S):

1. The VIX_CK voltage is referenced to V_{swing}/2(mean) = (BCK_t voltage + BCK_c voltage) / 2, where the mean is over 1e6 UI.
2. VIX_CK_Ratio = (VIX_CK / Vdiff) * 100%, where Vdiff = |BCK_t voltage – BCK_c voltage|.

14.9 RX BCK Input Clock Jitter

Overview

The clock is being driven to the RCD for L/RDIMM modules, Figure 92.

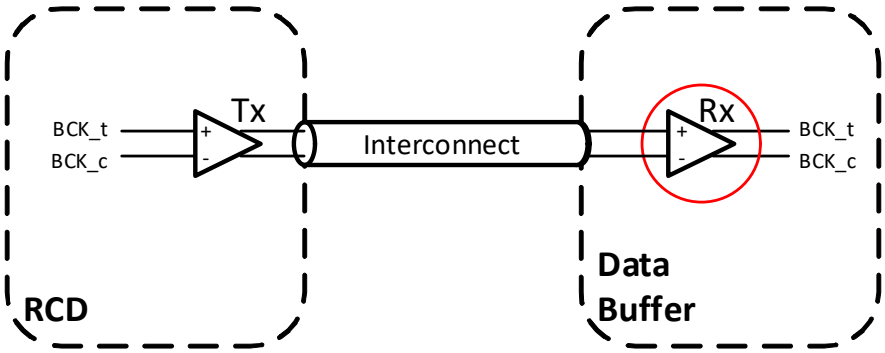


Figure 92 — RCD driving clock signals to the Data Buffer

14.9.1 Specification for Data Buffer Input Clock Jitter

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5DB01 device.

Table 171 — Input Clock Differential Jitter

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tCK	RCD Reference clock frequency	0.9999*f0	1.0001*f0	MHz	1, 12
tCK_Duty_UI	Duty Cycle	0.45	0.55	UI	4, 12
tCK_Duty_UI_Error	Duty Cycle Error	-	0.05	UI	1, 5, 12
tCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter	-	0.0037	UI (RMS)	3, 6, 12, 13
tCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter	-	0.030	UI	3, 7, 12, 13
tCK_1UI_Tj_NoBUJ	Tj value of 1-UI Jitter	-	0.090	UI	3, 7, 12, 13
tCK_NUI_Rj_NoBUJ, where N=2,3	Rj value of N-UI Jitter, where N=2,3	-	0.004	UI (RMS)	3, 8, 12, 13
tCK_NUI_Dj_NoBUJ, where N=2,3	Dj pp value of N-UI Jitter, where N=2,3	-	0.074	UI	3, 9, 12, 13
tCK_NUI_Tj_NoBUJ, where N=2,3	Tj value of N-UI Jitter, where N=2,3	-	0.140	UI	3, 9, 12, 13
tCK_NUI_Rj_NoBUJ, where N=4,5,6,...,30	Rj value of N-UI Jitter, where N=4,5,6,...,30	-	TBD	UI (RMS)	3, 10, 12, 13
tCK_NUI_Dj_NoBUJ, where N=4,5,6,...,30	Dj pp value of N-UI Jitter, N=4,5,6,...,30	-	TBD	UI	3, 11, 12, 13
tCK_NUI_Tj_NoBUJ, where N=4,5,6,...,30	Tj value of N-UI Jitter, N=4,5,6,...,30	-	TBD	UI	3, 11, 12, 13

Note(s):
1. f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600.
2. Rise and fall time slopes (V / nsec) are measured between +100 mV and -100 mV of the differential output of reference clock.
3. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DDR5DB01 component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
4. Duty Cycle defined as the ratio between any even UI and tCK.
5. Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.
6. Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD
7. Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
8. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. This extraction is to be done after software correction of DCD.
9. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
10. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. This extraction is to be done after software correction of DCD.
11. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 3 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
12. The validation methodology for these parameters will be covered in future ballots.
13. If the clock meets total jitter Tj at BER of 1E-16, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of 1E-16.

14.10 RX BCK Voltage Sensitivity

14.10.1 Overview

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

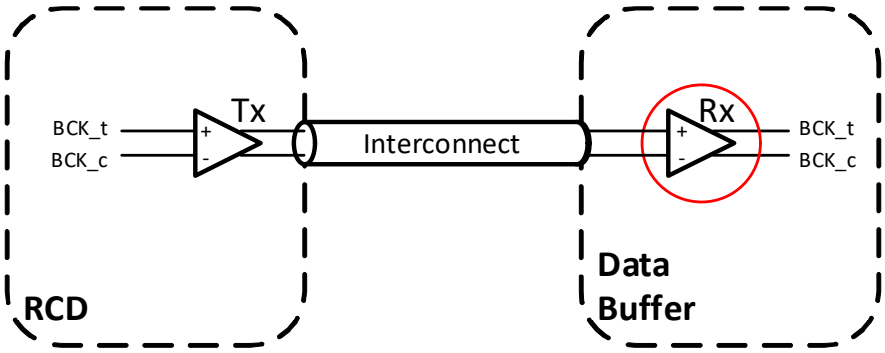


Figure 93 — Example of DDR5 Memory Interconnect

14.10.2 RX BCK Voltage Sensitivity Parameter

Differential input clock (BCK_t, BCK_c) VRx_CK is defined Table 172 and measured as in Figure 94. The clock receiver must pass the minimum BER requirements for DDR5.

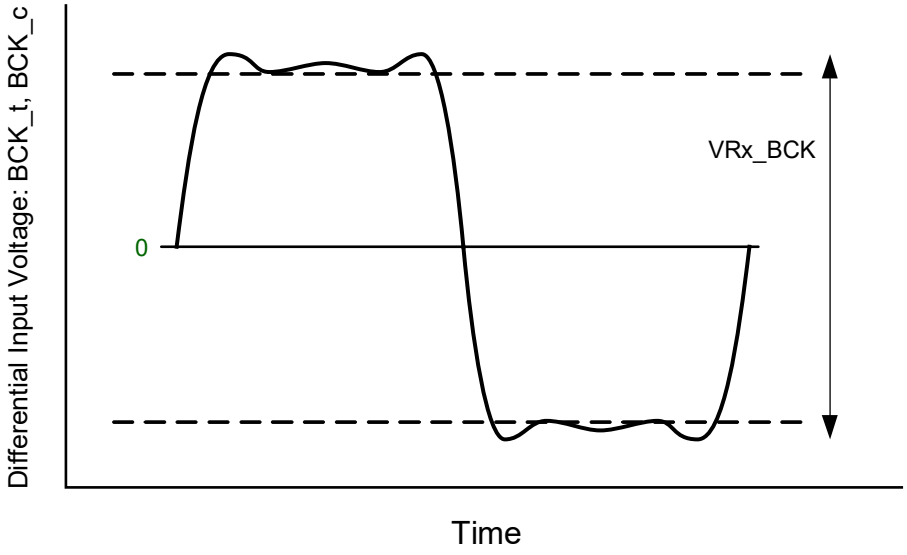


Figure 94 — VRx_BCK

14.11 Rx [M]DQS Voltage Sensitivity

14.11.1 Overview

The receiver strobe input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

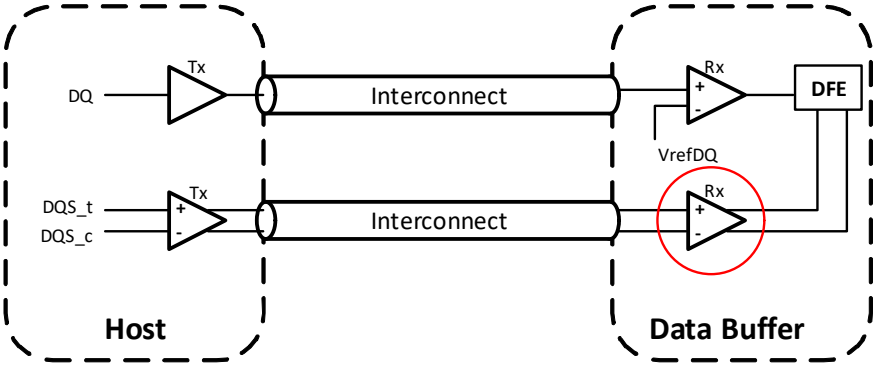


Figure 95 — Data Buffer's RX Forward Strobe for Jitter Sensitivity Testing

Input differential (DQS_t, DQS_c) VRx_DQS is defined in Table 172 and measured as shown in Figure 96. The receiver must pass the minimum BER requirements for DDR5.

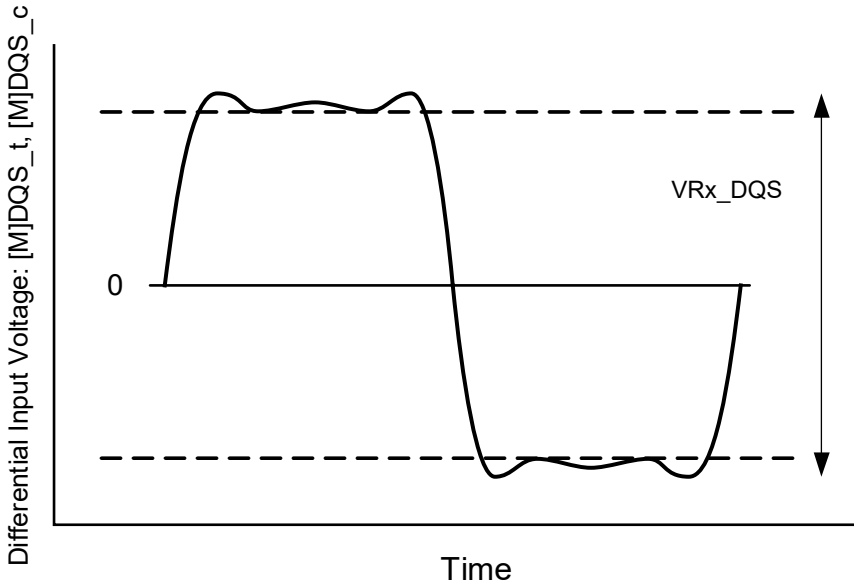


Figure 96 — VRx_DQS

14.12 RX [M]DQ Voltage Sensitivity

14.12.1 Overview

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD) and crosstalk noise.

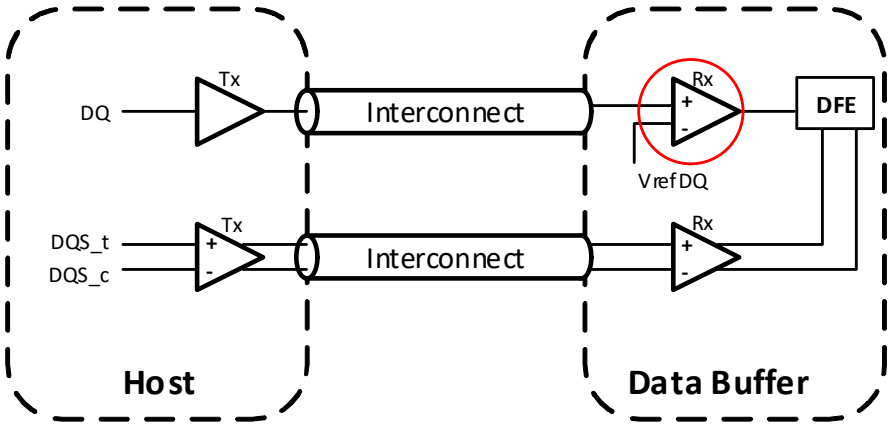


Figure 97 — Example of DDR5 Memory Interconnect

Input differential (DQS_t, DQS_c) VRx_DQ is defined in table Table 172 and measured as shown in Figure 98. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested with neither additive gain nor Rx Equalization set.

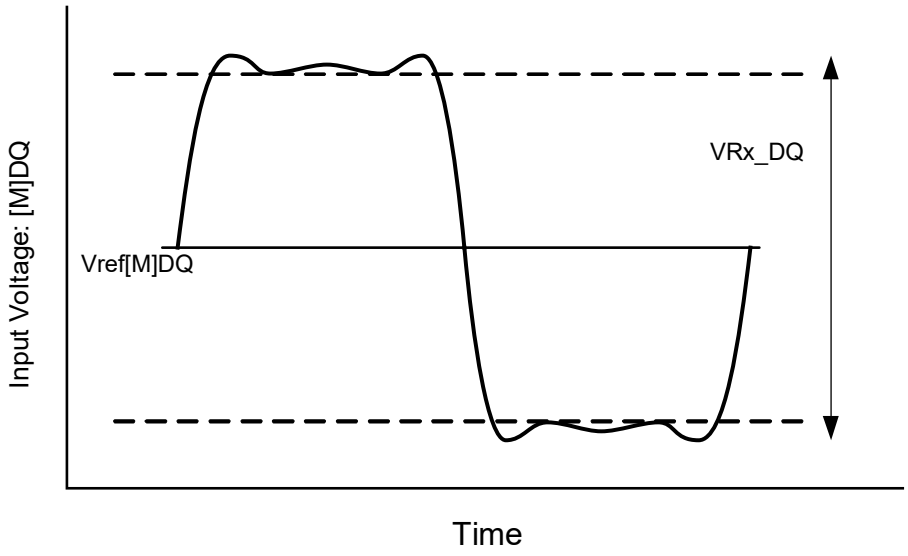


Figure 98 — VRx_DQ

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Table 172 — RX Voltage Sensitivity Parameters for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VRx_BCK	Minimum input clock voltage sensitivity (differential p-p)	-	100	-	90	-	85	-	80	-	75	mV	1, 3, 5
VRx_DQS	Minimum [M]DQS Rx input voltage sensitivity (differential p-p)	-	100	-	90	-	85	-	80	-	75	mV	1, 2, 3, 5
VRx_DQ	Minimum [M]DQ Rx input voltage sensitivity (p-p around Vref[M]DQ)	-	70	-	65	-	60	-	55	-	50	mV	1, 2, 3, 4

NOTE(S):
1. Refer to the minimum BER 1e-9 requirements for DDR5.
2. Test using clock-like pattern of repeating 3 “1s” and 3 “0s” without applying cross-talk or SSO conditions.
3. This test should be done in typical temperature and voltage conditions (i.e., VDD = 1.1 V, 25 °C).
4. This test should be done with default Vref[M]DQ settings.
5. The common-mode voltage that provides the best input voltage sensitivity performance can be chosen for this measurement.

14.13 RX [M]DQS Input Jitter Sensitivity

14.13.1 Overview

The receiver clock jitter sensitivity test provides the methodology for testing the receiver’s strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input while keeping the data input jitter free, noise free and ISI free. The receiver must pass the appropriate BER rate when the equivalent cross-talk pattern is applied through the combination of applied DCD and Rj.

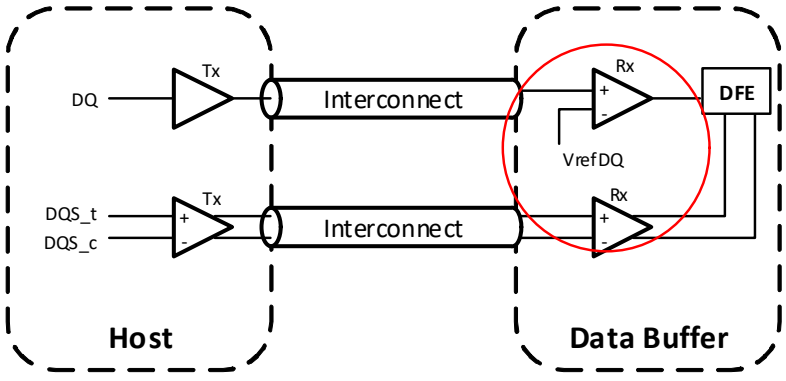


Figure 99 — Data Buffer’s RX Forward Strobe for Jitter Sensitivity Testing

14.13.2 RX [M]DQS Input Jitter Sensitivity Parameters for DDR5-3200 to 4800

The following table provides Rx DQS and MDQS Jitter Sensitivity Specification for the DDR5DB01 receivers when operating at various possible transfer rates. These parameters are tested with neither additive gain nor Rx Equalization set.

Table 173 — Rx [M]DQS Jitter Sensitivity Specification for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tRx_DQ_tMargin	DQ Timing Width	0.85	-	UI	1, 2, 3, 8, 9, 10
ΔtRx_DQ_tMargin_DCD_DQS	Degradation of timing width compared to tRx_DQ_tMargin, with DCD injection in [M]DQS	-	0.05	UI	1, 4, 8, 9, 10
ΔtRx_DQ_tMargin_Rj_DQS	Degradation of timing width compared to tRx_DQ _tMargin, with Rj injection in [M]DQS	-	0.075	UI	1, 5, 8, 9, 10
ΔtRx_DQ_tMargin_DCD_Rj_DQS	Degradation of timing width compared to tRx_DQ_tMargin, with both DCD and Rj injection in [M]DQS	-	0.125	UI	1, 2, 6, 8, 9, 10
tRx_DQS2DQ	Delay of any data lane relative to the DQS_t/DQS_c crossing	0	1	UI	1, 7, 8, 9, 10
tRx_MDQS2MDQ	Delay of any MDQ data lane relative to the MDQS_t/MDQS_c crossing	-0.1	0.1	UI	1, 7, 8, 9, 10

NOTE(S):

1. Validation methodology will be defined in future ballots.
2. tEach of ΔtRx_DCA_tMargin_DCD_DCK, ΔtRx_DCA_tMargin_DCD_Rj_DCK, and ΔRx_DQ_tMargin_DCD_Rj_DQS can be relaxed by up to 5% if tRx_DQ_tMargin exceeds the spec by at least by 5%
3. DQ Timing Width - timing width for any data lane using repetitive patterns (check notes 4 to 6 for the pattern) measured at BER=E-9.
4. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe [M]DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx Strobe Jitter Sensitivity Testing5. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
5. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe [M]DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx Strobe Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
6. Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe [M]DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx Strobe Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.
7. Delay of any data lane relative to the [M]DQS lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.
8. All measurements at BER=E-9.
9. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C) with default Vref[M]DQ settings.
10. The user has the freedom to set the voltage swing and slew rates for strobe and [M]DQ signals as long as they meet the specification.

14.13.3 Test Conditions for RX Strobe Jitter Sensitivity Tests

Table 174 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded clock when measuring the Rx Clock Jitter Sensitivity parameters specified in Table 173.

Table 174 — RX Strobe Jitter Sensitivity Specification for DDR5-3200 to 4800

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tRx_DQS_DCD	Applied DCD to the DQS	-	0.045	UI	1, 2, 3, 6, 7, 10
tRx_DQS_Rj	Applied Rj RMS to the DQS	-	0.00625	UI (RMS)	1, 2, 4, 6, 8, 10
tRx_DQS_DCD_Rj	Applied DCD and Rj RMS to the DQS	-	0.045 UI DCD + 0.00625 UI (RMS) Rj	UI	1, 2, 5, 6, 7, 9, 10

NOTE(S):
1. While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.
2. The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin.
3. Various DCD values should be tested, complying within the maximum limits.
4. Various Rj values should be tested, complying within the maximum limits.
5. Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table.
6. Although DDR5 has bursty traffic, in order to ensure that current available BERTs can be used for this test, a continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.
7. Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).
8. RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
9. Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).
10. The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification.

14.14 Rx DQ Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the Data Buffer’s receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

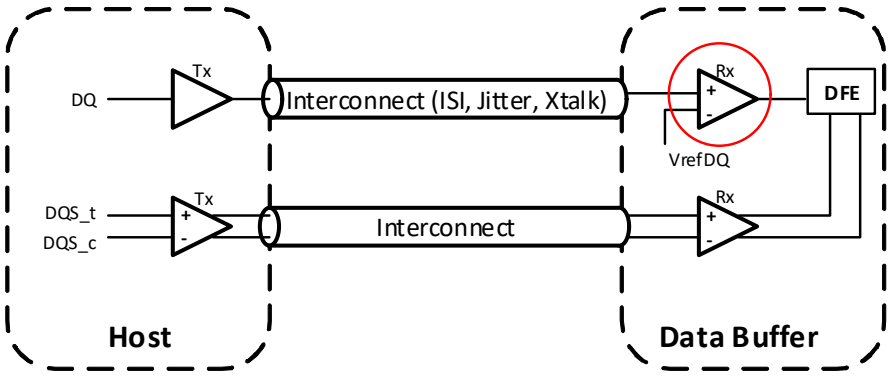


Figure 100 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter and Crosstalk

14.15 Parameters for DDR5 Host Stressed Eye Test

Table 175 — Test Conditions for Rx Stressed Eye Tests for DDR5-3200 to 4800
[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p=peak to peak]

Symbol	Parameter	DDR5-3200		DDR5-3600		DDR5-4000		DDR5-4400		DDR5-4800		Unit	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RxEH_Stressed_Eye	Eye height of stressed eye	-	65	-	65	-	65	-	55	-	55	mV	1, 2, 3, 4, 5, 6, 7
RxEW_Stressed_Eye	Eye width of stressed eye	-	0.20	-	0.20	-	0.20	-	0.20	-	0.20	UI	1, 2, 3, 4, 5, 6, 7
Vswing_Stressed_Eye	Vswing stress to meet above data eye	0	600	0	600	0	600	0	600	0	600	mV	1, 2
Sj_Stressed_Eye	Injected sinusoidal jitter at 200 MHz to meet above data eye	0	0.45	0	0.45	0	0.45	0	0.45	0	0.45	UI (p-p)	1, 2
Rj_Stressed_Eye	Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	0	0.04	0	0.04	0	0.04	0	0.04	0	0.04	UI RMS	1, 2
Vnoise_Stressed_Eye	Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz to meet above data eye	0	125	0	125	0	125	0	125	0	125	mV (p-p)	1, 2

NOTE(S):

Unit UI=tCK(avg).min/2

1. Must meet minimum BER requirement with eye at receiver after equalization per pin.
2. These parameters are applied on the reference channel (TBD).
3. Evaluated with no DC supply voltage drift.
4. Evaluated with no temperature drift.
5. Supply voltage noise limited according to DC bandwidth spec, see Recommended DC Operating Conditions.
6. The stressed eye is to be assumed to have a diamond shape.
7. The VrefDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4 Bias Step can be adjusted as needed, without exceeding the specifications, for this test.

14.16 Overshoot and Undershoot Specifications

TBD

15 TX Output Specifications

15.1 [M]DQ/[M]DQS Output Driver DC Electrical Characteristics

The values in Table 176 are valid for the entire operating temperature range after proper ZQ calibration and assume R_{ZQ} = 240 Ω+/– 1%.

Table 176 — M]DQ/[M]DQS Output Driver DC Electrical Characteristics

RON_{NOM}	Resistor	V_{OUT}	min	nom	max	Unit	Note
34 Ω	RON_{34Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/7	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/7	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/7	1, 2
	RON_{34Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/7	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/7	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/7	1, 2
40 Ω	RON_{40Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/6	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/6	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/6	1, 2
	RON_{40Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/6	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/6	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/6	1, 2
48 Ω	RON_{48Pd}	V_{OLdc} = 0.5 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/5	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/5	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/5	1, 2
	RON_{48Pu}	V_{OLdc} = 0.5 x V_{DD}	0.9	1.0	1.25	R_{ZQ}/5	1, 2
		V_{OMdc} = 0.8 x V_{DD}	0.9	1.0	1.1	R_{ZQ}/5	1, 2
		V_{OHdc} = 0.95 x V_{DD}	0.8	1.0	1.1	R_{ZQ}/5	1, 2
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} = 0.8 x V_{DD}	-10		10	%	1, 2, 4
Mismatch [M]DQ-[M]DQ within byte variation pull-dn, MM_{up}		V_{OMdc} = 0.8 x V_{DD}	0		10	%	1, 2, 3
Mismatch [M]DQ-[M]DQ within byte variation pull-dn, MM_{Pddd}		V_{OMdc} = 0.8 x V_{DD}	0		10	%	1, 2, 3

NOTE A functional representation of the output buffer is shown in Figure 101 Output impedance RON is defined by the value of the external reference resistor RZQ as defined in Table 176.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{(V_{DD} - V_{Out})}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off

$$RON_{PD} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off.

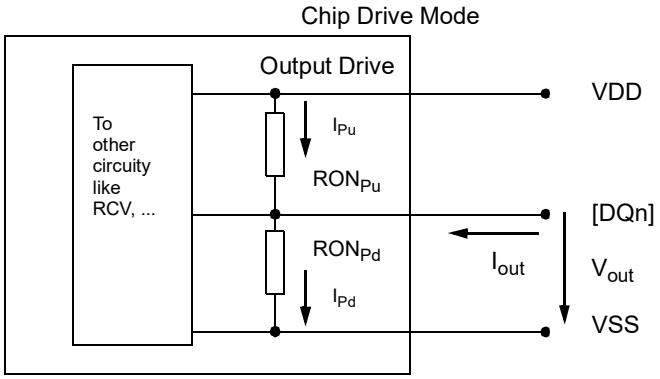


Figure 101 — Output Driver: Definition of Voltages and Currents

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Section 15.3 on page 199.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.8 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * V_{DD} and 0.95 * V_{DD}.
3. [M]DQ to [M]DQ mismatch within byte variation for a given component including [M]DQS_t and [M]DQS_c (characterized).
4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
   Measure RON_{Pu} and RON_{Pd}, both at 0.8 * V_{DD} separately. Ron-nom is the nominal Ron value:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

5. RON variance range ratio to RON nominal value in a given component, including [M]DQS_t and [M]DQS_c.

$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} x100$$

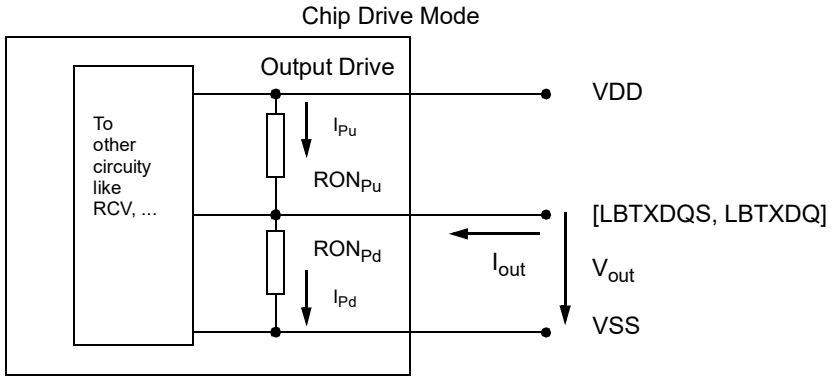
$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} x100$$

15.2 Output Driver DC Electrical Characteristics for LBTXDQS, LBTXDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in the figure below.

$RON_{Pu} = \frac{(V_{DD} - V_{Out})}{|I_{Out}|}$ under the condition that RON_{Pd} is turned off

$RON_{PD} = \frac{V_{Out}}{|I_{Out}|}$ under the condition that RON_{Pu} is turned off.



15.3 Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the tables shown below.

Table 177 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Note
R_{ONPD}	0.8 x VDD	90 - ($dR_{ONPD}dT$ x |ΔT|) - ($dR_{ONPD}dV$ x |ΔV|)	110+($dR_{ONPD}dT$ x |ΔT|) + ($dR_{ONPD}dV$ x |ΔV|)	%	1,2
R_{ONPU}	0.8 x VDD	90 - (dR_{ONPU} x |ΔT|) - (dR_{ONPU} x |ΔV|)	110 +(dR_{ONPU} x |ΔT|) + (dR_{ONPU} x |ΔV|)	%	1,2
R_{RTT}	0.8 x VDD	90 - ($dR_{RTT}dT$ x |ΔT|) - ($dR_{RTT}dV$ x |ΔV|)	110 + ($dR_{RTT}dT$ x |ΔT|) + ($dR_{RTT}dV$ x |ΔV|)	%	1,2

Notes:
1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)
2. $dR_{ONPD}dT$, $dR_{ONPD}dV$, $dR_{ONPU}dT$, $dR_{ONPU}dV$, $dR_{RTT}dV$, and $dR_{RTT}dT$ are not subject to production test but are verified by design and characterization.

.

Table 178 — Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ONPD}dT$	R_{ONPD} Temperature Sensitivity	0.0	0.1	%/°C
$dR_{ONPD}dV$	R_{ONPD} Voltage Sensitivity	0.0	0.1	%/mV
$dR_{ONPU}dT$	R_{ONPU} Temperature Sensitivity	0.0	0.1	%/°C
$dR_{ONPU}dV$	R_{ONPU} Voltage Sensitivity	0.0	0.1	%/mV
$dR_{RTT}T$	R_{RTT} Temperature Sensitivity	0.0	0.1	%/°C
$dR_{RTT}dV$	R_{TT} Voltage Sensitivity	0.0	0.1	%/mV

15.4 Single-ended AC & DC Output Levels

Table 179 — Single-ended AC & DC output levels

Symbol	Parameter	DDR5-3200-4800	Unit	Note
$V_{OH}(DC)$	DC output HIGH measurement level (for IV curve linearity)	0.95 x V_{DD}	V	
$V_{OM}(DC)$	DC output MID measurement level (for IV curve linearity)	0.80 x V_{DD}	V	
$V_{OL}(DC)$	DC output LOW measurement level (for IV curve linearity)	0.50 x V_{DD}	V	
$V_{OH}(AC)$	AC output HIGH measurement level (for output SR)	0.75 x V_{pk-pk}	V	1
$V_{OL}(AC)$	AC output LOW measurement level (for output SR)	0.25 x V_{pk-pk}	V	1

NOTE 1: V_{pk-pk} is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.

15.5 Differential AC Output Levels

Table 180 — Differential AC output levels

Symbol	Parameter	DDR5-3200-4800	Unit	Note
$V_{OHdiff}(AC)$	AC differential output HIGH measurement level (for output SR)	0.75 x $V_{diffpk-pk}$	V	1
$V_{OLdiff}(AC)$	AC differential output LOW measurement level (for output SR)	0.25 x $V_{diffpk-pk}$	V	1

NOTE 1: $V_{diffpk-pk}$ is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.

15.6 Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $VOL_{(AC)}$ and $V_{OH(AC)}$ for single-ended signals as shown in Table 181 and Figure 102.

Table 181 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

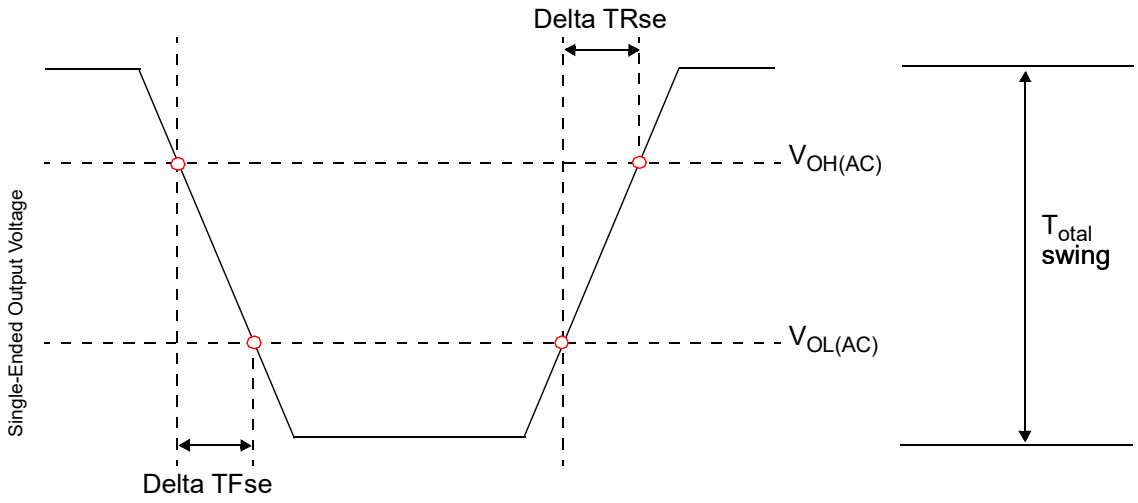


Figure 102 — Output Single-Ended Slew Rate Definition

Table 182 — Output Single-Ended Edge Rates Over Specified Operating Temperature Range

Symbol	Parameter	Conditions	DDR5-3200 to 4800		Unit
			Min	Max	
dV/dt_se_r	[M]DQ, [M]DQS rising edge single-ended Slew Rate[1,2]	1.1V operation	TBD	TBD	V/ns
dV/dt_se_f	[M]DQ, [M]DQS falling edge single-ended Slew Rate[1,2]	1.1V operation	TBD	TBD	V/ns

1. These parameters are for the DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, and MDQS[1:0]_c outputs.
2. Measured into 50-Ω reference load terminated to V_{DD}, as shown in Figure 127.

15.7 Differential Output Slew Rate

Output slew rates for differential signals DQS_t / DQS_c and MDQS_t / MDQS_c are defined and measured as shown in Table 183 and Figure 103.

Table 183 — Output Clock Differential Slew Rate Definition for DQS_t / DQS_c and MDQS_t / MDQS_c

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge (DQS_t / DQS_c and MDQS_t /MDQS_c).	25%	75%	[|25% - 75%|] / DeltaTRdiff
Differential output slew rate for falling edge (DQS_t / DQS_c and MDQS_t /MDQS_c).	75%	25%	[|75% - 25%|] / DeltaTFdiff
NOTE Differential output slew rate is verified by design and characterization, and may not be subject to production test.			

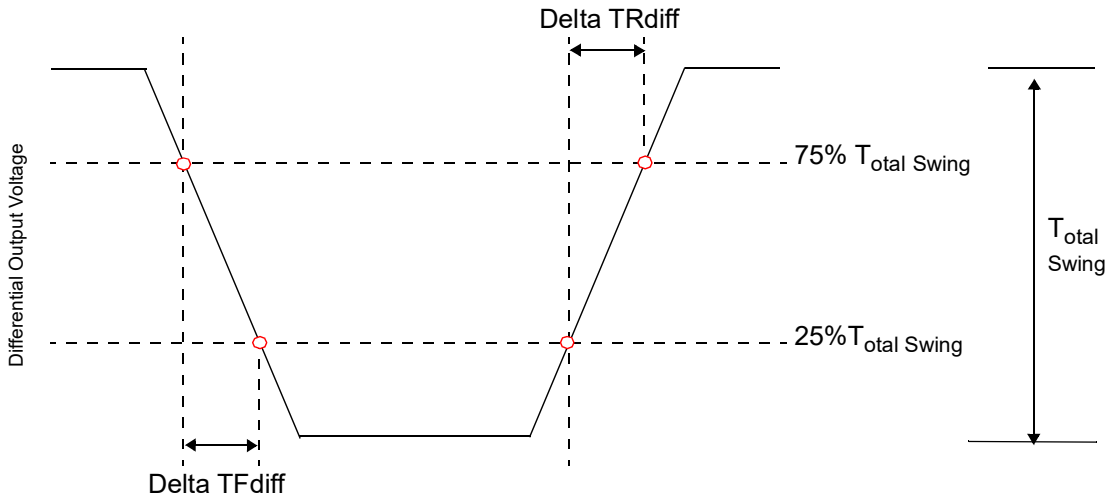


Figure 103 — Differential Output Slew Rate Definition for DQS_t / DQS_c and MDQS_t / MDQS_c

Table 184 — Output Differential Edge Rates Over Specified Operating Temperature Range

Symbol	Parameter	Conditions	DDR5-3200 - 4800		Unit
			Min	Max	
dV/dt_r	[M]DQS rising edge differential Slew Rate[1,2]	1.1V operation	tbd	tbd	V/ns
dV/dt_f	[M]DQS falling edge differential Slew Rate[1,2]	1.1V operation	tbd	tbd	V/ns

1. These parameters are for the DQS0_t/DQS0_c, DQS1_t/DQS1_c, MDQS0_t/MDQS0_c, and MDQS1_t/MDQS1_c outputs.
2. Measured into 50-Ω reference load terminated to V_{DD}, as shown in Figure 127.

15.8 Differential Output Cross Point Voltage

The differential cross point output voltage is defined as the max to min cross point measured on the differential signals DQS_t / DQS_c and MDQS_t / MDQS_c with respect to the output common mode voltage (V_{OCM}).

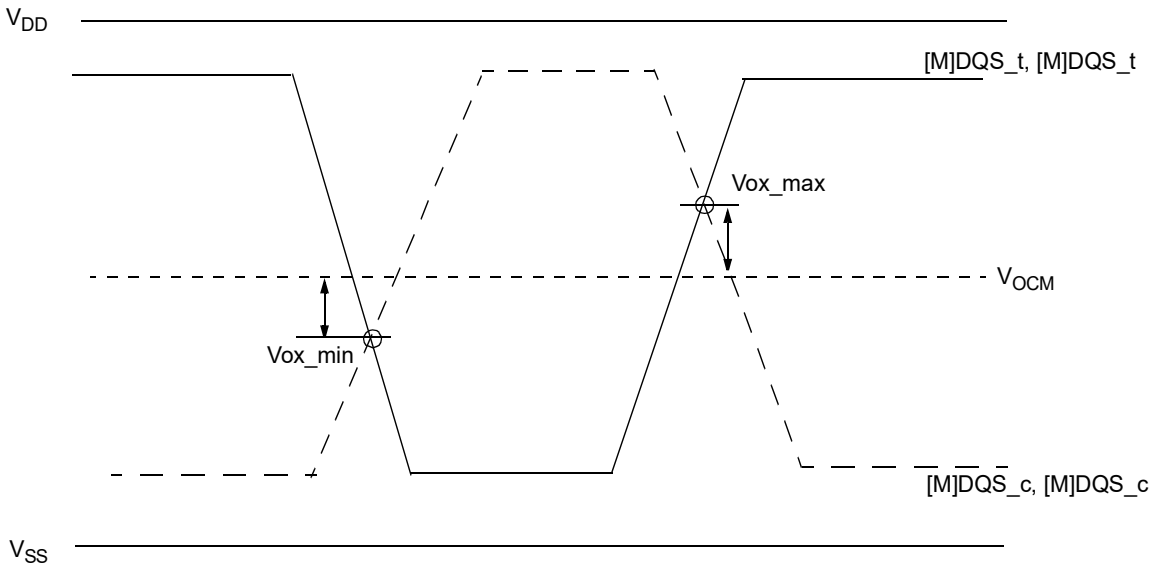


Figure 104 — Vox Definition (DQS and MDQS)

Table 185 — Output Cross Point Voltage for DQS_t / DQS_c and MDQS_t / MDQS_c

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		min	max		
Vox_DQS_Ratio	[M]DQS Differential Output Cross-Point Voltage Ratio	tbd	tbd	%	1, 2

NOTE 1: Referenced to V_{OCM} = avg ([M]DQS_t + [M]DQS_c)/2 where the average is over 1e6 UI.
NOTE 2: Vox_DQS_Ratio = 100 x (|Vox_DQS|/Vdiff_DQS pk-pk) where VdiffDQS pk-pk = 2 x |VDQS_t - VDQS_c|.

15.9 Tx DQS Jitter

15.9.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5DB01 device output jitter must not exceed maximum values specified in Table 186.

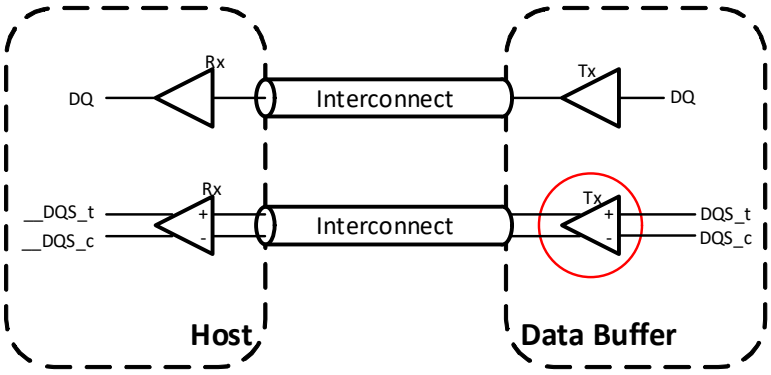


Figure 105 — Example of DQS TX

Table 186 — Tx DQS Jitter Parameters for DDR5-3200 to 4800

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tTx_DQS_1UI_Rj_NoBUJ	Rj Value of 1-UI Jitter without BUJ	-	tbd	UI (RMS)	1, 2, 3, 4, 8, 9, 10, 11
tTx_DQS_1UI_Dj_NoBUJ	Dj pp Value of 1-UI Jitter without BUJ	-	0.05	UI	1, 2, 4, 5, 8, 9, 10, 11
tTx_DQS_NUI_Rj_NoBUJ	Rj Value of N-UI Jitter without BUJ, where 1 < N < 4	-	tbd	UI (RMS)	1, 2, 4, 6, 8, 9, 10, 11
tTx_DQS_NUI_Dj_NoBUJ	Dj pp Value of N-UI Jitter without BUJ, where 1 < N < 4	-	0.10	UI	1, 2, 4, 7, 8, 9, 10, 11

NOTE(S):

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
3. Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.
4. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C).
5. Dj pp value of 1-UI jitter. Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
6. Rj Value of N-UI jitter. Without BUJ but on-die system like noise present, where 1 < N < 4. This extraction is to be done after software correction of DCD.
7. Dj pp RMS value of N-UI jitter. Without BUJ, but on-die system like noise present, where 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
8. See Section 13.2.2 for details on minimum BER requirements.
9. See Section 13.2.3 for details on UI, NUI and Jitter definitions.
10. Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test.
11. These parameters are tested using the continuous clock pattern which are sent out from the DDR5DB01 device without the need for sending out continuous MRR commands. Control Word Bit RW90 OP[0] is set to “1” to enable this feature.

15.10 Tx DQ Jitter

15.10.1 Overview

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 187.

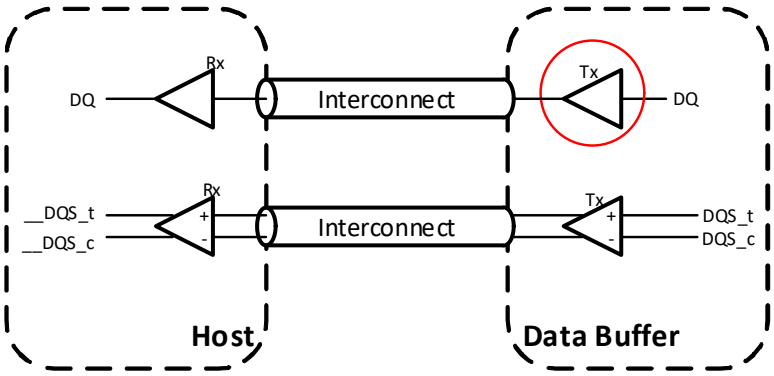


Figure 106 — Example of DQ TX

Table 187 — Tx DQ Jitter Parameters for DDR5-3200 to 4800

[BER=Bit Error Rate; DCD = Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
tTx_DQ_1UI_Rj_NoBUJ	Rj RMS of 1-UI jitter without BUJ	-	tbd	UI (RMS)	1, 2, 3, 4, 9, 10, 11, 12, 13
tTx_DQ_1UI_Dj_NoBUJ	Dj pp 1-UI jitter without BUJ	-	0.05	UI	1, 2, 4, 5, 9, 10, 11, 12, 13
tTx_DQ_NUI_Rj_NoBUJ	Rj RMS of N-UI jitter without BUJ, where 1 < N < 4	-	tbd	UI (RMS)	1, 2, 4, 6, 9, 10, 11, 12, 13
tTx_DQ_NUI_Dj_NoBUJ	Dj pp value of N-UI jitter without BUJ, where 1 < N < 4	-	0.10	UI	1, 2, 4, 7, 9, 10, 11, 12, 13
tTx_DQS2DQ	Delay of any data lane relative to strobe lane	-0.1	0.1	UI	4, 8, 9, 10, 12, 13

NOTES:

1. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
2. On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.
3. Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.
4. This test should be done in typical temperature and voltage conditions (i.e., V_{DD} = 1.1 V, 25 °C).
5. Dj pp value of 1-UI jitter without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
6. Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present, where 1 < N < 4. This extraction is to be done after software correction of DCD.
7. Dj pp value of N-UI jitter without BUJ, but on-die system like noise present, where 1 < N < 4. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.
8. Delay of any data lane relative to strobe lane, as measured at Tx output.
9. Vref noise level to DQ jitter should be adjusted to minimize DCD.
10. See Section 13.2.2 for details on the minimum BER requirements.
11. See Section 13.2.2 for details on UI, NUI and Jitter definitions.
12. Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test.
13. These parameters are tested using the continuous clock pattern which are sent out from the DDR5DB01 device without the need for sending out continuous MRR commands. Control Word Bit RW90 OP[0] is set to “1” to enable this feature.

15.11 TX Stressed Eye

15.11.1 TX DQ Stressed Eye

Tx DQ stressed eye height and eye width must meet minimum specification values at BER = E-9 and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings (RW8F OP[3:0]).

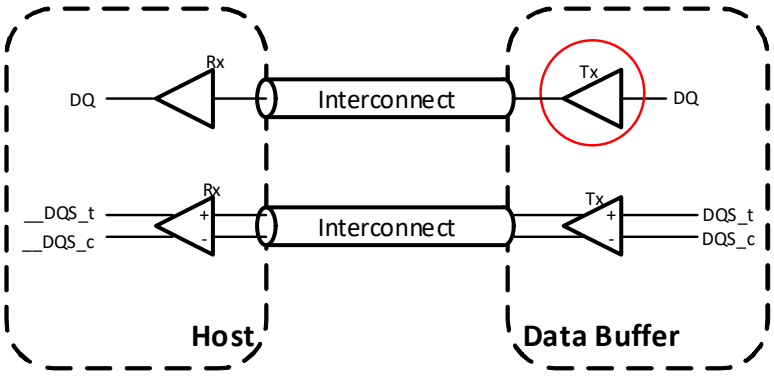


Figure 107 — Example of DQ TX

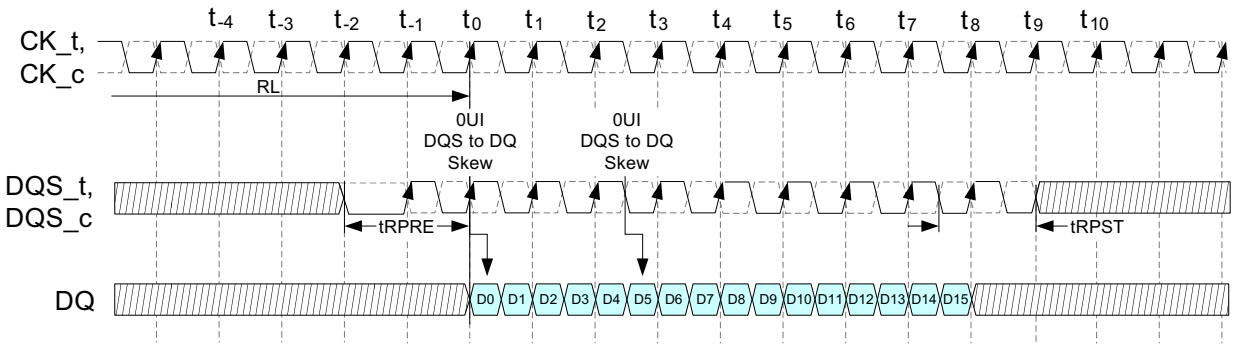


Figure 108 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 0 UI skew

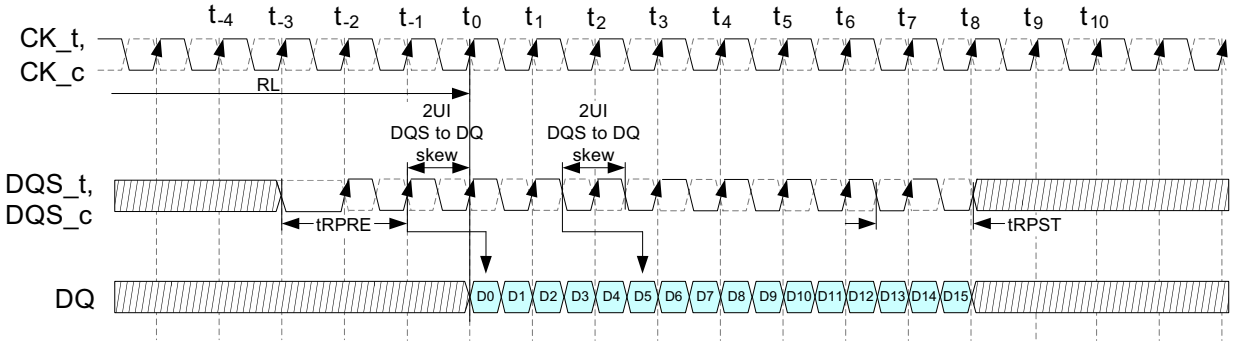


Figure 109 — Read burst example for pin DQx depicting bit 0 and 5 relative to the DQS edge for 2 UI skew with Read DQS Offset Timing set to 1 Clock (2UI)

15.11.2 TX MDQ Stressed Eye

Tx MDQ stressed eye height and eye width must meet minimum specification values at BER = E-9 and confidence level 99.5%. Tx MDQ Stressed Eye shows the MDQS to MDQ skew for both Eye Width and Eye Height. In order to support the full range of DRAM tRx_DQS2DQ, it is the responsibility of the Host to insure MDQ phases with respect to MDQS are adjusted accordingly via the MDQ Write Baseline Delay register settings (PG[1:0]RWE6 and PG[1:0]RWE7).

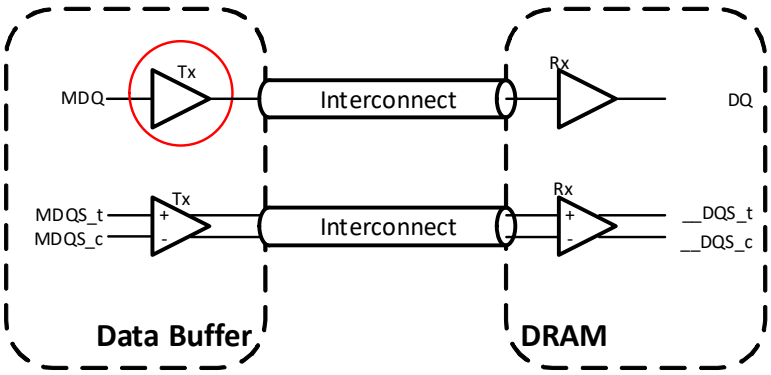


Figure 110 — Example of MDQ TX

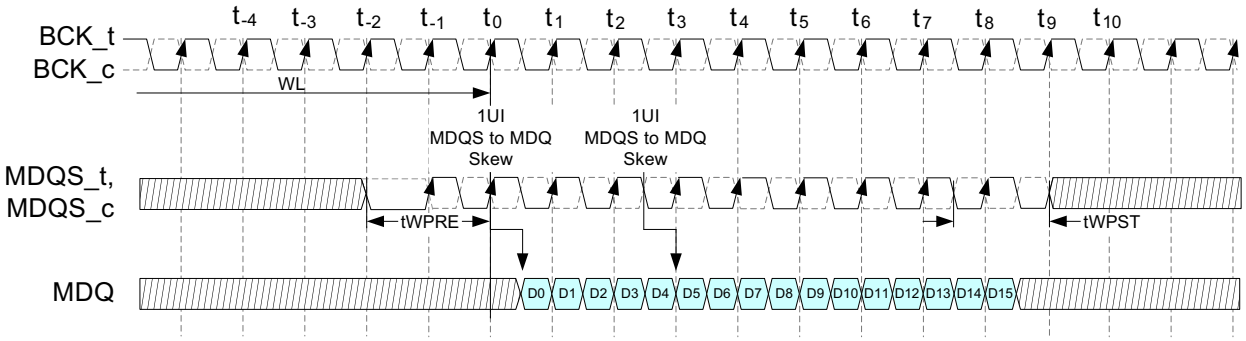


Figure 111 — Write burst example for pin MDQx depicting bit 0 and 5 relative to the MDQS edge for 1 UI skew

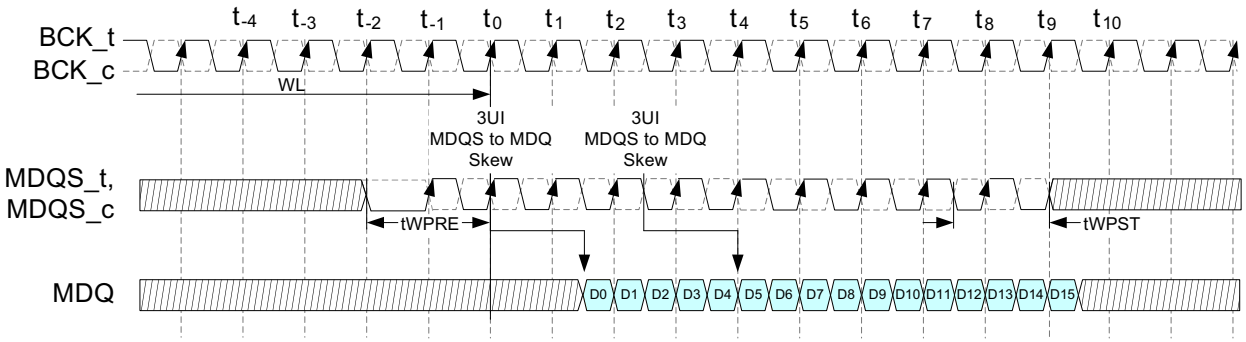


Figure 112 — Write burst example for pin MDQx depicting bit 0 and 5 relative to the MDQS edge for 3 UI skew with MDQ Write Baseline Delay Timing set to 1.5 Clock (3UI)

15.11.3 TX DQ and MDQ Stressed Eye Parameters

Table 188 — TX DQ and MDQ Stressed Eye Parameters for DDR5-3200 to 4800
[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Symbol	Parameter	DDR5-3200 to 4800		Unit	NOTE
		Min	Max		
TxEH_DQ_SES_1UI	Eye Height specified at the transmitter with a skew between [M]DQ and [M]DQS of 1UI	TBD	-	mV	1, 2, 3
TxEW_DQ_SES_1UI	Eye Width specified at the transmitter with a skew between [M]DQ and [M]DQS of 1UI	0.78	-	UI	1, 2, 3
TxEH_DQ_SES_2UI	Eye Height specified at the transmitter with a skew between [M]DQ and [M]DQS of 2UI	TBD	-	mV	1, 2, 3
TxEW_DQ_SES_2UI	Eye Width specified at the transmitter with a skew between [M]DQ and [M]DQS of 2UI	0.78	-	UI	1, 2, 3
TxEH_DQ_SES_3UI	Eye Height specified at the transmitter with a skew between [M]DQ and [M]DQS of 3UI	TBD	-	mV	1, 2, 3
TxEW_DQ_SES_3UI	Eye Width specified at the transmitter with a skew between [M]DQ and [M]DQS of 3UI	0.78	-	UI	1, 2, 3
TxEH_DQ_SES_4UI	Eye Height specified at the transmitter with a skew between [M]DQ and [M]DQS of 4UI	TBD	-	mV	1, 2, 3, 4
TxEW_DQ_SES_4UI	Eye Width specified at the transmitter with a skew between [M]DQ and [M]DQS of 4UI	0.78	-	UI	1, 2, 3, 4
TxEH_DQ_SES_5UI	Eye Height specified at the transmitter with a skew between [M]DQ and [M]DQS of 5UI	TBD	-	mV	1, 2, 3, 4
TxEW_DQ_SES_5UI	Eye Width specified at the transmitter with a skew between [M]DQ and [M]DQS of 5UI	0.78	-	UI	1, 2, 3, 4

NOTE(S):
1. Minimum BER E-9 and Confidence Level of 99.5% per pin, including Voltage and Temperature drift.
2. Refer to the minimum Bit Error Rate (BER) requirements for DDR5.
3. Mismatch is defined as [M]DQS to [M]DQ mismatch, in UI increments.
4. The number of UI's accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds N = 4,5 UI may not be applicable.

16 Vref Specifications

16.1 VrefDQ, VrefMDQ, and BVref Specifications

The internal VrefDQ, VrefMDQ, and BVref specifications parameters are Vref operating range, Vref step size, Vref set tolerance, Vref step time and Vref valid tolerance.

The Vref operating range specifies the minimum required Vref setting range for DDR5DB01 devices and is specific by a Vref min operating point and a Vref max operating point, as depicted in Figure 113 below.

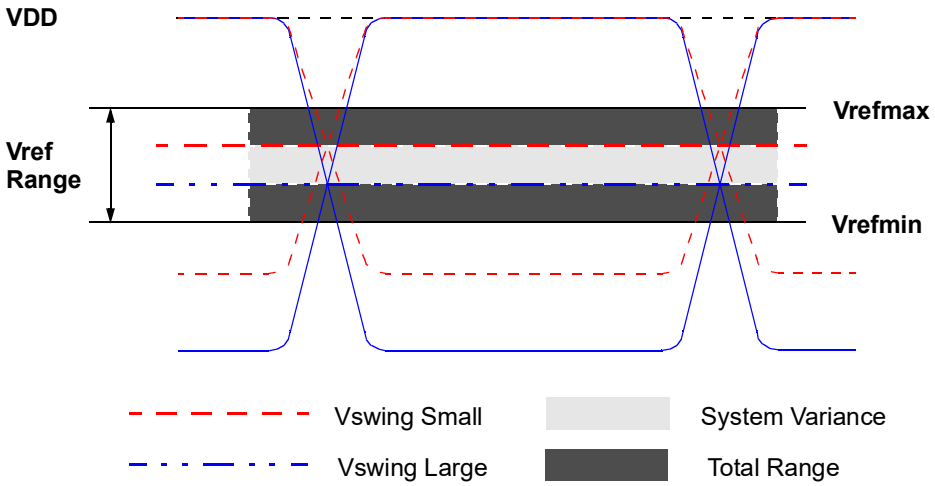


Figure 113 — Vref operating range (Vrefmin, Vrefmax)

The Vref step size is defined as the target voltage increment between adjacent steps. For a given design, the DDR5DB01 VrefDQ, VrefMDQ, and BVref step size must be within the range specified.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two parameters for Vref set tolerance uncertainty for different numbers of steps n. The Vref set tolerance is measured with respect to the ideal line which is based on two endpoints, where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the step size and Vref set tolerance is shown below in Figure 114.

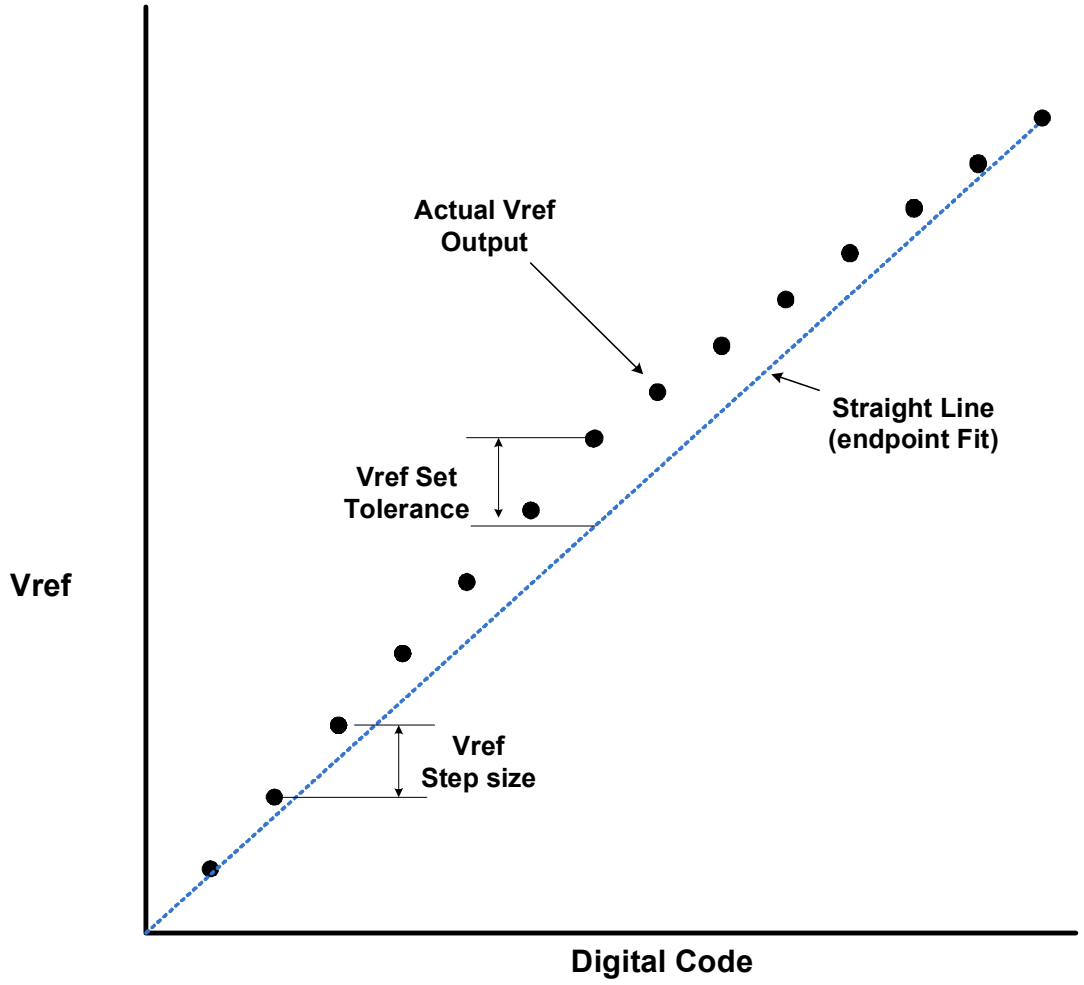


Figure 114 — Example of Vref set tolerance (max case only shown) and step size

The Vref increment/decrement step times are defined by Vref_time. Vref_time is defined from t0 to t1 as shown in the Figure 115 below where t0 is referenced to when the RW write occurs and t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance (Vref_val_tol).

The Vref valid level is defined by Vref_val_tol to qualify the step time t1 as shown in Figure 116. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for component level validation/characterization.

Vref_time is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to RW write command clock

t1 - is referenced to the Vref_val_tol

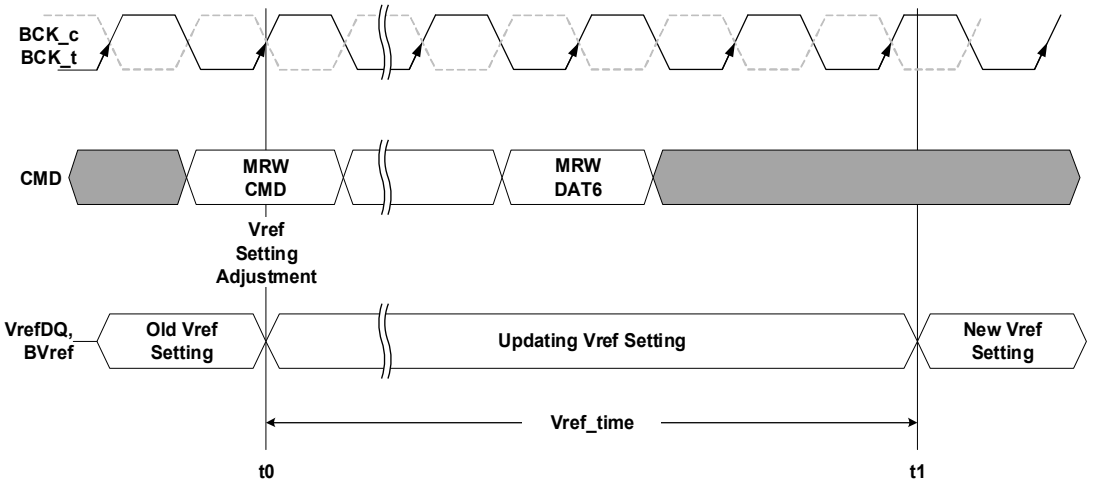


Figure 115 — Vref_time timing diagram

An MRW write to the (Internal Vref Control Word) is used to program the Vref value.

The minimum time required between two Vref MRW commands is Vref_time_short, for n < 16 steps, and Vref_time_long, for n ≥ 16 steps. See Table 189 on page 215 for details.

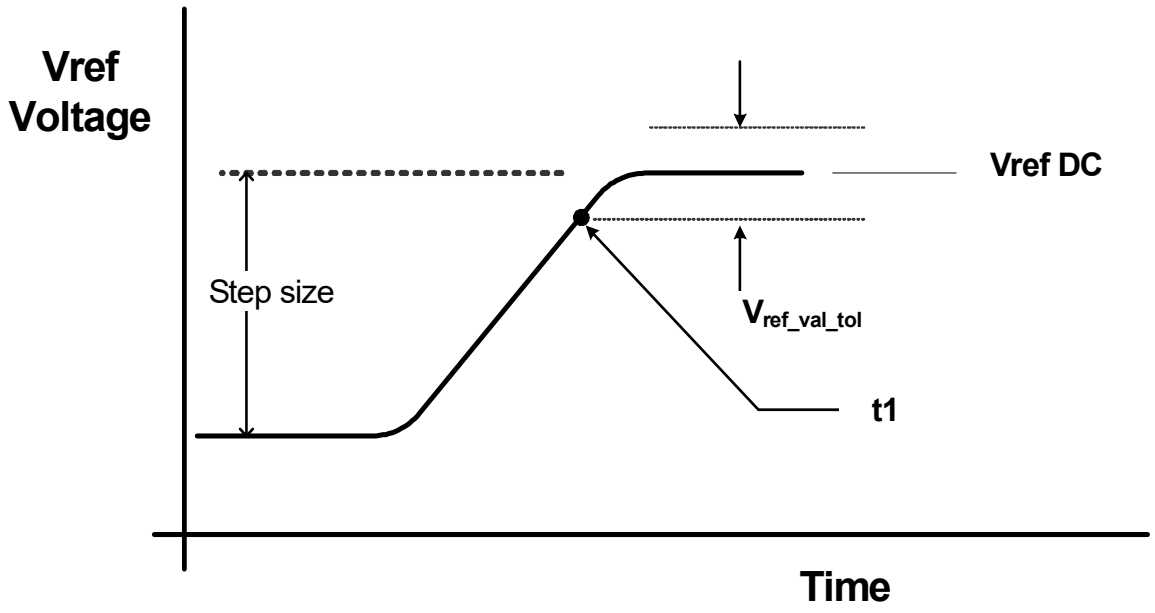


Figure 116 — Vref step single step size increment case

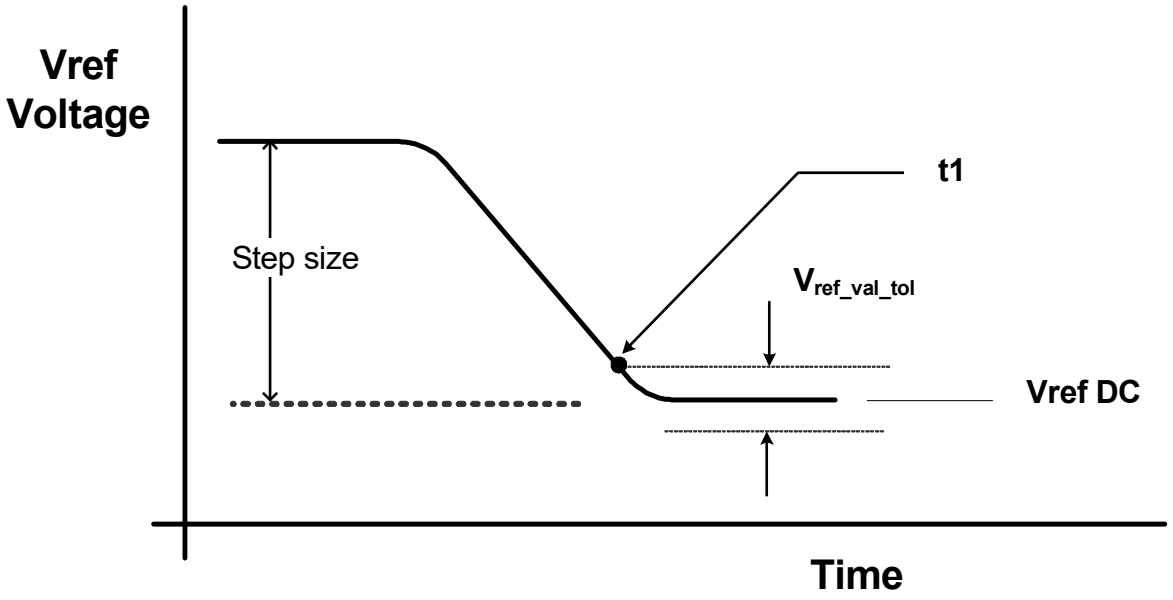


Figure 117 — Vref step single step size decrement case

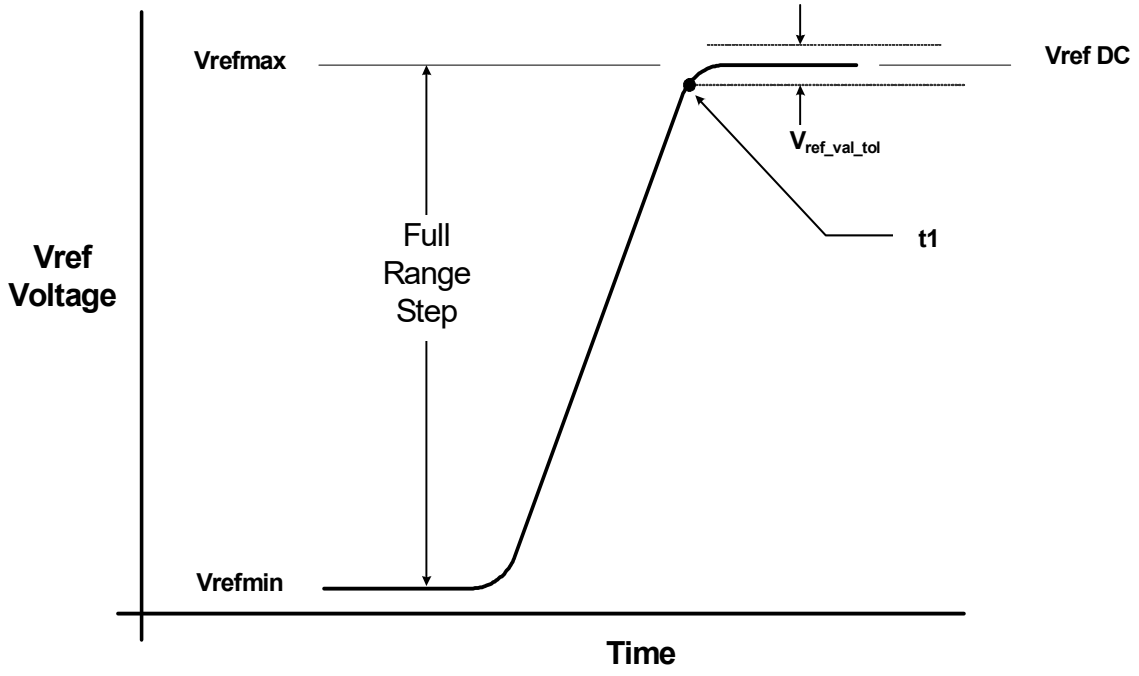


Figure 118 — Vref full step from Vrefmin to Vrefmax case

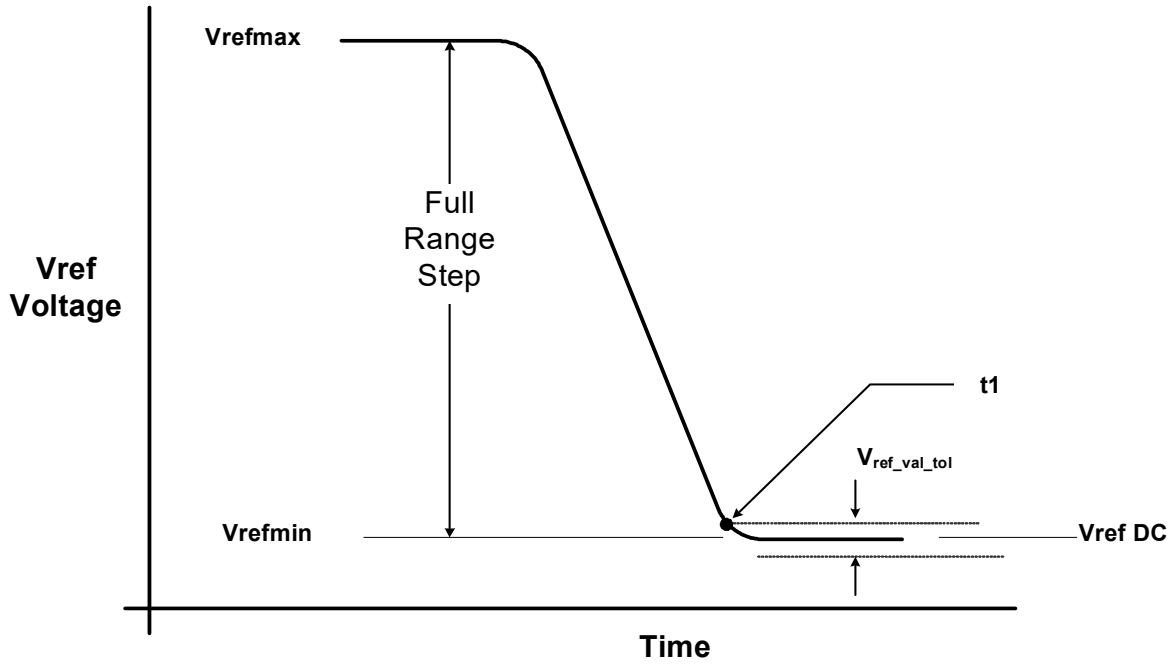


Figure 119 — Vref full step from Vrefmax to Vrefmin case

Table 189, "Internal Vref [M]DQ & BVref Specifications," below contains the internal Vref specifications that will be characterized at the component level for compliance. The characterization method is defined in a separate specification.

Table 189 — Internal Vref [M]DQ & BVref Specifications

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max Operating Point	Vref_max	97.5%	-	-	V_{DD}	1
Vref Min Operating Point	Vref_min	-	-	35%	V_{DD}	1
Vref Step size	Vref_step	0.41%	0.50%	0.59%	V_{DD}	2, 10
Vref Set Tolerance	Vref_set_tol	-1.625%	0.0%	1.625%	V_{DD}	3, 4, 6
	Vref_set_tol	- 0.15%	0.0%	0.15%	V_{DD}	3, 5, 7
Vref Step Time Short	Vref_time_short	-	-	150	ns	8, 11
Vref Step Time Long	Vref_time_long	-	-	500	ns	8, 11
Vref Valid Tolerance	Vref_val_tol	- 0.15%	0.0%	0.15%	V_{DD}	9

NOTE 1: Vref DC voltage referenced to VDD
NOTE 2: Vref step size increment/decrement range. Vref at DC level.
NOTE 3: Vref_new = Vref_old + n*Vref_step; n= number of steps; if increment use "+"; If decrement use "-".
NOTE 4: The minimum value of Vref setting tolerance = Vref_new - 1.625%*VDD. The maximum value of Vref setting tolerance = Vref_new + 1.625%*VDD. For n>4.
NOTE 5: The minimum value of Vref setting tolerance = Vref_new - 0.15%*VDD. The maximum value of Vref setting tolerance = Vref_new + 0.15%*VDD. For n< 4.
NOTE 6: Measured by recording the min and max values of the Vref output over the full range, drawing a straight line between those points and comparing all other Vref output settings to that line.
NOTE 7: Measured by recording the min and max values of the Vref output across 4 consecutive steps (n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
NOTE 8: Time from MRW command updating Vref to increment or decrement.
NOTE 9: Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
NOTE 10: Vref_step(avg) = (Vref_max - Vref_min)/ 125.
NOTE 11: The maximum value of Vref[M]DQ step time = 150ns for n<16 and 500ns for n≥16, where n = number of steps.

16.2 DFE_Vref Tolerance

16.2.1 DFE_Vref INL Tolerance

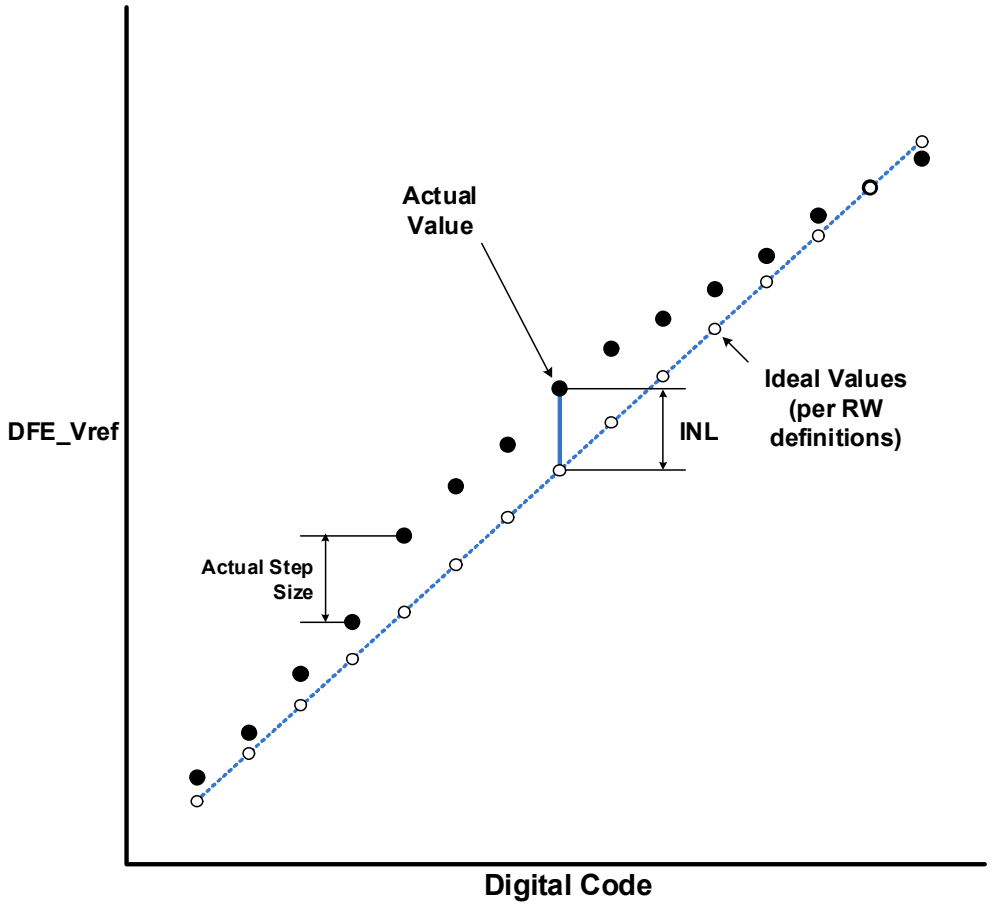


Figure 120 — Example of DFE_Vref INL Tolerance

Integral nonlinearity (INL) is the deviation between effective analog values and expected ideal values for the corresponding settings in Receiver DFE_Vref Control words as defined in PG[6]RW[E2, E6, EA, EE, F2, F6, FA, FE] and PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF].

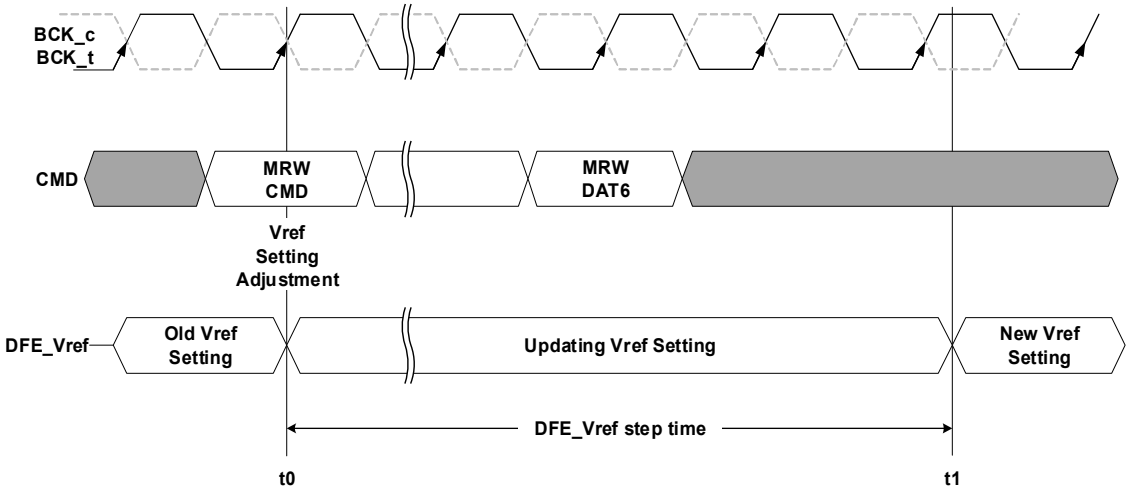


Figure 121 — DFE_Vref step time timing diagram

An MRW write to the (Internal Vref Control Word) is used to program the Vref value.

The minimum time required between two DFE_Vref MRW commands is DFE_Vref Step Time.

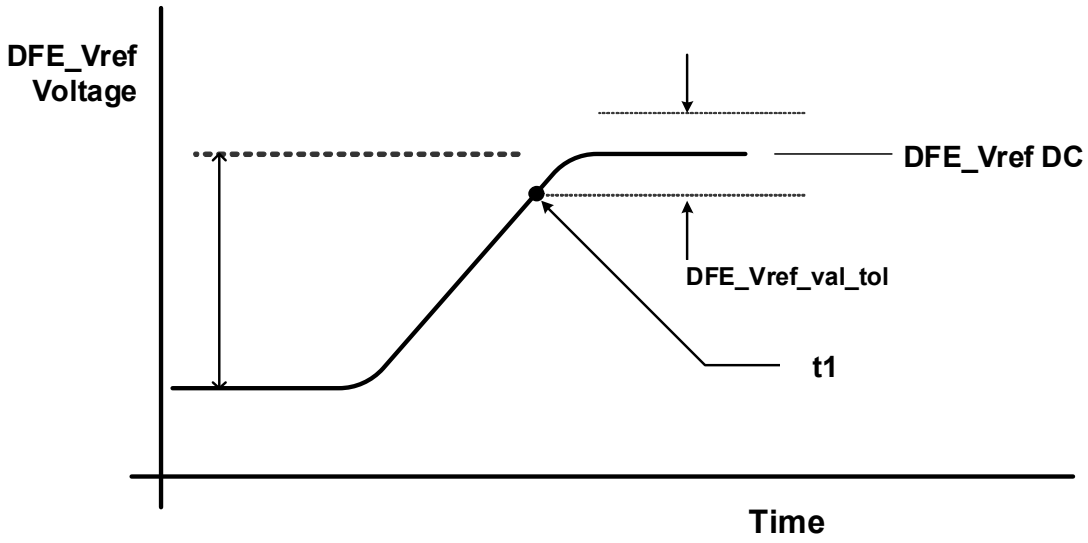


Figure 122 — DFE_Vref Increment Case

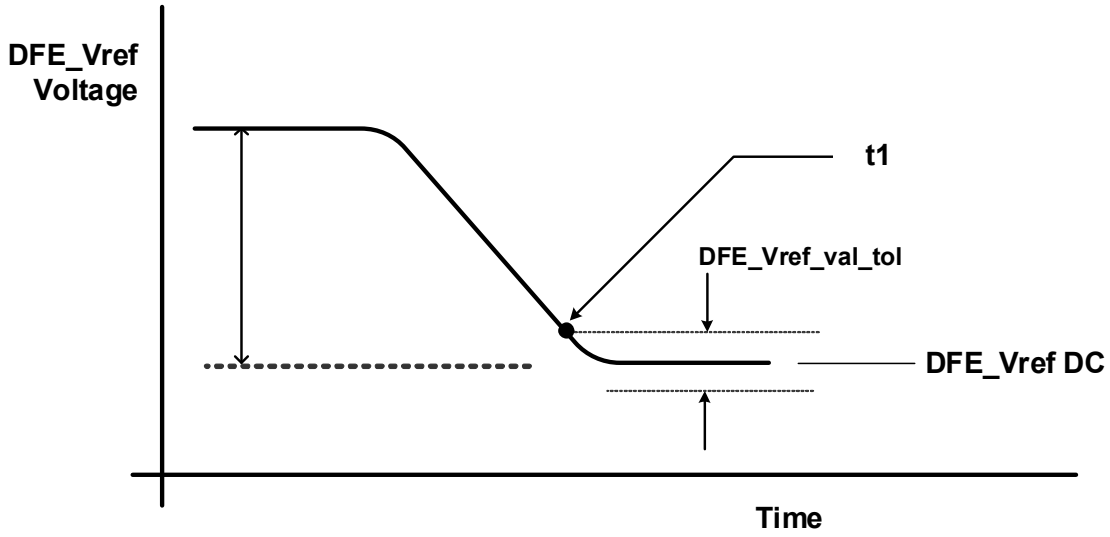


Figure 123 — DFE VREF Decrement Case

Table 190 below contains the DFE Training Vref specifications that will be characterized at the component level for compliance. The characterization method is described in Section 16.2.2 on page 219.

Table 190 — DFE_Vref Specification

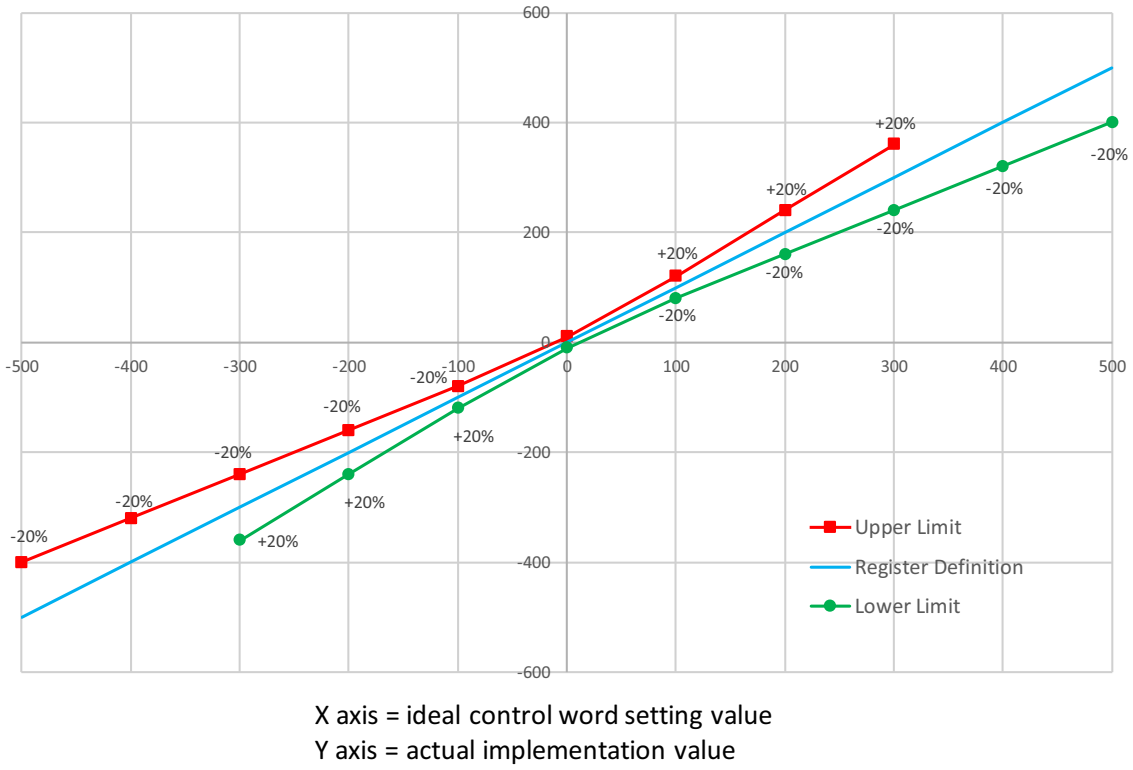
Parameter	Symbol	Min	Typ	Max	Unit	NOTE
DFE_Vref Step Time Short	DFE_Vref_Short_16	-	-	200	ns	1, 2
	DFE_Vref_Short_32	-	-	300	ns	1, 3
DFE_Vref Step Time Long	DFE_Vref_Long	-	-	600	ns	1, 4
DFE_Vref Valid Tolerance	DFE_Vref_val_tol	- 1.65	0	1.65	mV	1

NOTE 1: Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is used to qualify the step times which will be characterized at the component level.
NOTE 2: The maximum value of DFE_Vref step time = 200 ns for $n < 16$, where n = number of steps.
NOTE 3: The maximum value of DFE_Vref step time = 300 ns for $16 \leq n < 32$, where n = number of steps.
NOTE 4: The maximum value of DFE_Vref step time = 600 ns for $n \geq 32$, where n = number of steps.

Table 191 — DFE_Vref INL Tolerance

DFE_Vref Setting	Lower Limit	Upper Limit	NOTE
- 500 mV ~ 300 mV	-	V_ideal * 80%	1,3,4
- 300 mV ~ 0 mV	Min(V_ideal * 120%, V_ideal – 4 * LSB)	Max(V_ideal * 80%, V_ideal + 4 * LSB)	1,2,3,4
0 mV ~ + 300 mV	Min(V_ideal * 80%, V_ideal – 4 * LSB)	Max(V_ideal * 120%, V_ideal + 4 * LSB)	1,2,3,4
+300 mV ~ + 500 mV	V_ideal * 80%	-	1,3,4

1. V_ideal refers to the ideal DFE_Vref value based on the setting.
2. LSB is 2.5mV.
3. DFE_Vref must be monotonic.
4. The range values specified in the table are applicable for default VrefDQ and DFE Gain Offset setting, under VDD = 1.1V and 25°C ambient temperature.



X axis = ideal control word setting value
Y axis = actual implementation value

NOTE The values shown in this diagram should be considered examples for reference only.

Figure 124 — Illustration Example of DFE_Vref INL Tolerance

16.2.2 Measurement Steps

1. Make sure VrefDQ is at default setting, DFE_Vref setting is 0, power supply is 1.1V. Configure Margin Monitor RWA1[2:0] to 3'b001.
2. Sweep input signal from 1.1V to 0V to find the lowest level for HIGH and record this input signal HIGH level as V1 when HIGH-to-LOW transition starts.
3. Sweep input signal from 0V to 1.1V to find the highest level for LOW and record this input signal LOW level as V2 when LOW-to-HIGH transition starts.
4. Transition level V = (V1 + V2)/2.
5. Set DFE_Vref, wait for DFE_Vref Step Time to let the new setting settle.
6. Repeat steps 2 ~ 4, to get a new transition level V'.
7. Validate (V' - V) is within specification.
8. Repeat steps 2 ~ 7 until all the settings of DFE_Vref are measured.

17 Input/Output Capacitance

Table 192 — Silicon pad I/O Capacitance Values

Symbol	Parameter	Conditions	DDR5 - 3200-4800		Unit
			min	max	
C_{IO}	Input/Output capacitance, DQ IOs	see footnote[1,2]	0.4	0.9	pF
C_{IOD}	Delta capacitance over all DQ IOs of each interface (i.e., within the DQ/DQS group or the MDQ/MDQS group)	see footnote [2]	-	0.1	pF
C_{DQSD}	Delta capacitance between DQS_t and DQS_c (within each *DQS_t, *DQS_c pair)		-	0.04	pF
C_I	Input capacitance, Control inputs	see footnote[1,3]	0.2	0.8	pF
C_{ID}	Delta capacitance over all control inputs	see footnote [3]	-	0.1	pF
C_{CK}	Input capacitance, BCK_t, BCK_c	see footnote[1]	0.2	0.8	pF
C_{CKD}	Input capacitance delta BCK_t and BCK_c	see footnote[1,4]	-	0.04	pF
C_{OLB}	Output capacitance LB		-	0.9	pF
C_{IR}	Input Reset, BRST_n		-	3.0	pF

1. This parameter does not include package capacitance.
2. Data inputs are DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, MDQS[1:0]_c.
3. BCOM[2:0], BCS.
4. Absolute value BCK_t - BCK_c.

Table 193 — Package Electrical Specifications

Symbol	Parameter	DDR5-3200 - 4800		Unit	Notes
		Min	Max		
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	40	70	Ω	1, 2, 4
$Td_{I\ CTRL}$	Input CTRL pins Pkg Delay	5	20	ps	1, 3, 4
$DTd_{I\ CTRL}$	Delta CTRL pins Pkg Delay	-	3	ps	1,3, 4
$Z_{I\ DQS}$	Input/Output [M]DQS pins Zpkg	40	55	Ω	1, 2, 5
Td_{DQS}	Input/Output [M]DQS pins Pkg Delay	5	20	ps	1, 3, 5
DZ_{DQS}	Delta [M]DQS pins Zpkg (within each *DQS_t, *DQS_c pair)	-	2	Ω	1, 3, 5
DTd_{DQS}	Delta [M]DQS pins Pkg Delay (within each *DQS_t, *DQS_c pair)	-	1	ps	1, 3, 5
$Z_{I\ DQ}$	Input/Output [M]DQ pins Zpkg	40	55	Ω	1, 2, 5
Td_{DQ}	Input/Output [M]DQ pins Pkg Delay	5	30	ps	1, 3, 5
DZ_{DQ}	Delta [M]DQ pins Zpkg (for each [M]DQ nibble)	-	3	Ω	1, 3, 5
DTd_{DQ}	Delta [M]DQ pins Pkg Delay for all pins within the same interface (i.e., Host Side or DRAM Side)	-	4	ps	1, 3, 5
Z_{CK}	Input BCK pins ZPkg	40	65	Ω	1, 2, 8
Td_{CK}	Input BCK pins Pkg Delay	5	20	ps	1, 3
DZ_{BCK}	Delta Zpkg BCK_t and BCK_c	-	1	Ω	1, 2, 6
DTd_{BCK}	Delta Delay BCK_t and BCK_c	-	1	ps	1,3,7
$Z_{O\ ZQ}$	Output ZQCAL Zpkg	25	70	Ω	1, 2
$Z_{I\ LB}$	Output Loopback pins Zpkg	40	70	Ω	1, 2, 9
$Td_{I\ LB}$	Output Loopback pins Pkg Delay	5	30	ps	1, 3, 9
$DTd_{I\ LB}$	Delta Loopback pins Pkg Delay	-	1	ps	1, 3, 9

NOTE 1: This parameter is not subject to production test. It is verified by design and characterization. The package parasitics (L &C) are determined using package only samples. Package capacitance and inductance are computed from S-parameter models. The capacitance is derived with VDD, VSS shorted and all other signals floating. The inductance is derived with VDD, VSS shorted and all other signals shorted at the die side (not pin).
NOTE 2: Package only impedance (Zpkg) is calculated based on the computed Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT(Lpkg/Cpkg) (Lpkg and Cpkg for trace only, i.e. without including the ball).
NOTE 3: Package only delay (Tdpkg) is calculated based on computed Lpkg and Zpkg total for a given pin where: Tdpkg (total per pin) = SQRT(Lpkg*Cpkg) (Lpkg and Cpkg for trace only, i.e. without including the ball).
NOTE 4: This value applies to BCOM[2:0], BCS.
NOTE 5: This value applies to DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, MDQS[1:0]_c.
NOTE 6: Absolute value of ZCK_t - ZCK_c.
NOTE 7: Absolute value of TdBCK_t - TdBCK_c.
NOTE 8: Single-ended impedance.
NOTE 9: This value applies to LBTXDQ, LBTXDQS.

17.1 Electrostatic Discharge Sensitivity Characteristics

Table 194 — Electrostatic Discharge Sensitivity Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESD_{HBM}	1000	-	V	1, 2
Charged-device model (CDM)	ESD_{CDM}	250	-	V	1, 3

NOTE 1: State-of-the-art basic ESD control measures have to be in place when handling devices.
NOTE 2: Refer to JEDEC / ESDA Joint Standard JS-001 for measurement procedures.
NOTE 3: Refer to ANSI / ESDA / JEDEC Joint Standard JS-002 f for measurement procedures.

18 TEST Circuits and Switching waveforms

18.1 Parameter measurement information

All input pulses are supplied by generators having the following characteristics: 1400 MHz ≤ PRR (Pulse Repetition Rate) ≤ 2430 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

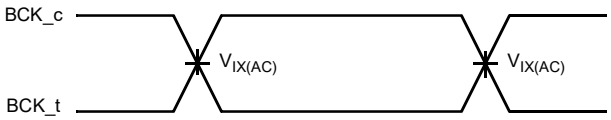
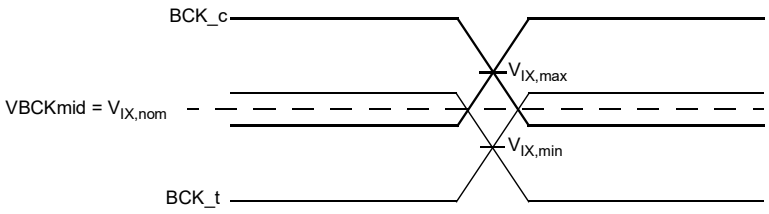


Figure 125 — Voltage waveforms; input clock



For V_{IX} Range testing common mode voltage of BCK_t and BCK_c is shifted around $V_{DD}/2$.
Functional Tests are performed with this V_{IX} shift.

Figure 126 — Input Waveforms V_{IX} range measurement

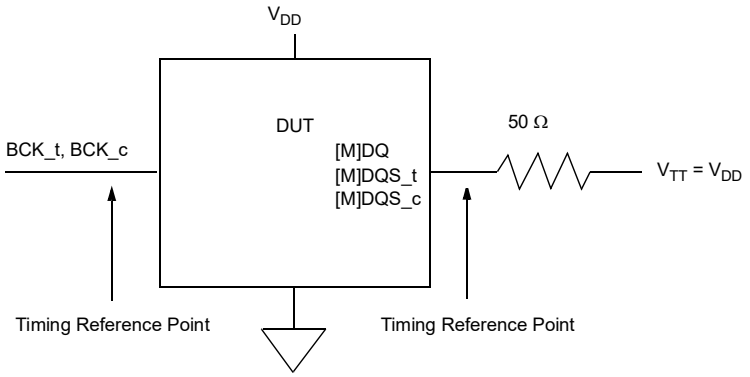


Figure 127 — Reference Load for Output Timing and Output Slew Rate

19 DC specifications, IDD Measurement Conditions

19.1 DC Electrical Characteristics

Table 195 — DC Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input current	$V_I = V_{DD}$ or GND	-	-	±5	µA
I_{ID}	Input current	Data inputs[1], $V_I = V_{DD}$ or GND	-	-	±25	µA

1. DQ[7:0], DQS[1:0]_t, DQS[1:0]_c, MDQ[7:0], MDQS[1:0]_t, MDQS[1:0]_c

19.2 IDD Specification Parameters and Test Conditions

In this chapter, IDD measurement conditions such as test load and patterns are defined. Figure 128 shows the setup and test load for IDD measurements.

- IDD currents are measured as time-averaged currents with all V_{DD} balls of the DDR5DB01 under test tied together.
- IDD currents can be measured for each speed bin. Each measurement shall use the minimum tCK (avg) for each speed bin as specified in Table 171 on page 189.
- **ATTENTION:** IDD values cannot be directly used to calculate IO power of the DDR5DB01. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 129.

For IDD measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} <= V_{IL(AC)}$.max.
- "1" and "HIGH" is defined as $V_{IN} >= V_{IH(AC)}$.min.
- Basic IDD Measurement Conditions are described in Table 196.
- Detailed IDD Measurement-Loop Patterns are described in Table 197 through Table 208.
- IDD Measurements are done after properly initializing the DDR5DB01. This includes but is not limited to setting
  Host interface RTT_WR = R_{ZQ}/4 (60 Ω in RW87);
  Host interface DQS_RTT_PARK = R_{ZQ}/7 (34 Ω in RW86);
  Host Interface DQ_ RTT_PARK = R_{ZQ}/7 (34 Ω in RW87);
  Host interface RON Pull-up and RON Pull-down = R_{ZQ}/7 (34 Ω in RW8A);
  DRAM interface MDQS_RTT_PARK and MDQ_RTT_PARK = R_{ZQ}/5 (48 Ω in RW8C);
  DRAM interface RON Pull-up and RON Pull-down = R_{ZQ}/7 (34 Ω in RW8B);
  Host interface DQ/DQS and DRAM interface DQ/DQS drivers enabled in RW8Aand RW8B respectively;
  Fixed burst length = 16(Fixed) in PG[8]RWE0;
  Write and Read CRC disabled in PG[8]RWE8;
  Read preamble = 2 nCK '0010' pattern and Write Preamble = 2 nCK in PG[8]RWE1
- Read post-amble = 1/2 nCK and Write post-amble = 1/2 nCK in PG[8]RWE1.
- **ATTENTION:** The IDD Measurement-Loop Patterns need to be executed at least one time before actual IDD measurement is started.

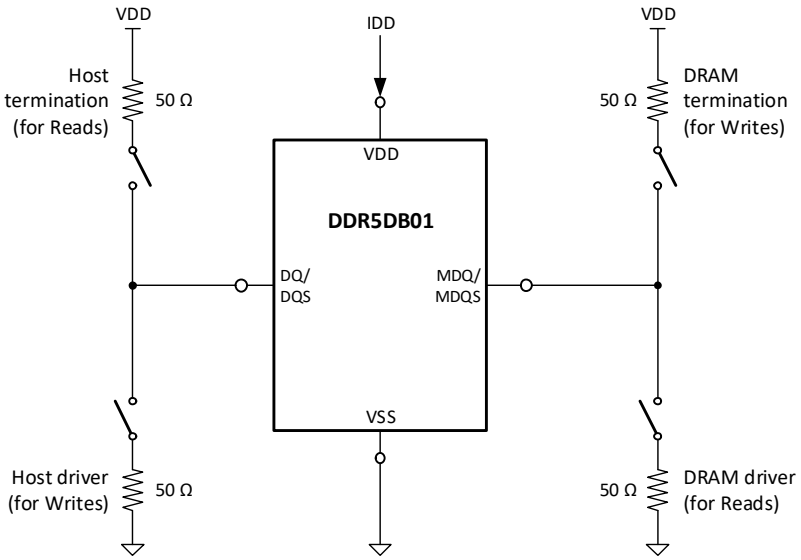


Figure 128 — Measurement Setup and Test Load for IDD Measurements

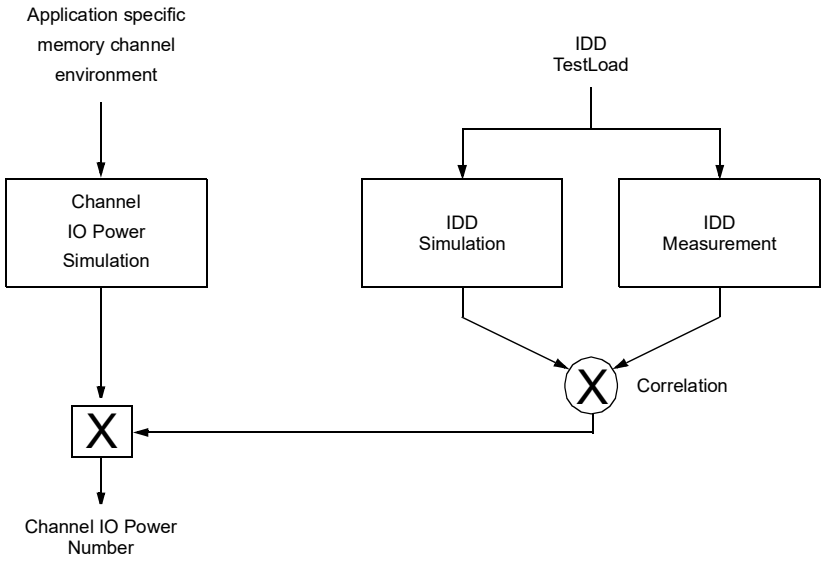


Figure 129 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDD Measurement

Table 196 — Basic IDD Measurement Conditions

Symbol	Description	Conditions
IDD3N1	**Active Idle Current with 50% LOW / 50% HIGH Host Side Data** **Pattern Details:** see Table 197	**External Clock:** On; **Host interface ODT:** RTT_WR = NA, RTT_NOM = NA, DQS_RTT_PARK = 34 Ω, DQ_RTT_PARK = 34 Ω.
IDD3N2	**Active Idle Current with 100% LOW Host Side Data** **Pattern Details:** see Table 198	
IDD3N3	**Active Idle Current with 100% HIGH Host Side Data** **Pattern Details:** see Table 199	
IDD3P1	**Power Down with ODT control with 50% LOW / 50% HIGH Host Side Data** **Pattern Details:** see Table 200	**External Clock:** On; **Host interface ODT:** RTT_WR = NA, RTT_NOM = NA, DQS_RTT_PARK = 34 Ω, DQ_RTT_PARK = 34 Ω.
IDD3P2	**Power Down without ODT control with 50% LOW / 50% HIGH Host Side Data** **Pattern Details:** see Table 200	**External Clock:** On; **Host interface ODT:** RTT_WR = NA, RTT_NOM = NA, DQS_RTT_PARK = disabled, DQ_RTT_PARK = disabled.
IDD4R1	**Operating Burst Read Current with 84% utilization and 50% LOW / 50% HIGH Host Side Data** **Data IO:** Seamless READ data burst with different data between one burst and the next one according to Table 201 on page 230 **Pattern Details:** see Table 201	**External clock:** On; **BL**: 16[1]; **Host interface Output Buffer:** RON = 34 Ω; **DRAM drive strength:** Ron = 50 Ω; **DRAM interface ODT:** MDQS_RTT_PARK = 48 Ω, MDQ_RTT_PARK = 48 Ω.
IDD4R2	**Operating Burst Read Current with 25% utilization and 50% LOW / 50% HIGH Host Side Data** **Pattern Conditions: see Table 202 on page 231** **Pattern Details:** see Table 202	
IDD4R3	**Operating Burst Read Current with 84% utilization and 100% LOW Host Side Data** **Pattern Details:** see Table 203	
IDD4R4	**Operating Burst Read Current with 25% utilization and 100% LOW Host Side Data** **Pattern Details**: see Table 204	
IDD4W1	**Operating Burst Write Current with 84% utilization and 50% LOW / 50% HIGH Host Side Data** **Data IO**: Seamless WRITE data burst with different data between one burst and the next one according to Table 205 **Pattern Details:** see Table 205	**External clock:** On; **BL**: 16; **Host drive strength:** Ron = 50 Ω; **Host interface ODT:** RTT_WR = 60 Ω; **DRAM interface Output Buffer:** RON = 34 Ω; **DRAM ODT:** RTT_WR = 50 Ω.
IDD4W2	**Operating Burst Write Current with 25% utilization and 50% LOW / 50% HIGH Host Side Data** **Pattern Details**: see Table 206	
IDD4W3	**Operating Burst Write Current with 84% utilization and 100% LOW Host Side Data** **Pattern Details:** see Table 207	
IDD4W4	**Operating Burst Write Current with 25% utilization and 100% LOW Host Side Data** **Pattern Details**: see Table 208	
IDD6R	**Static Reset Current Host Side** **Data IO:** V_{DD}	**External clock:** Off; **BCK_t and BCK_c:** HIGH.
IDD6S	**Self Refresh with Clock Stop Power Down Current** **Data IO:** V_{DD}	

Table 197 — IDD3N1 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Host Side Data[1]
toggling	0	0	Static HIGH	111 (DES)	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=00, D9=FF D10=FF, D11=00 D12=FF, D13=00 D14=00, D15=FF**
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF D7=00 D8=FF, D9=00 D10=00, D11=FF D12=00, D13=FF D14=FF D15=00**
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1: DQS signals toggle and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

Table 198 — IDD3N2 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Host Side Data[1]
toggling	0	0	Static HIGH	111 (DES)	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1: DQS signals toggle and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

Table 199 — IDD3N3 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Host Side Data[1]
toggling	0	0	Static HIGH	111 (DES)	**D0=FF, D1=FF D2=FF, D3=FF D4=FF, D5=FF D6=FF, D7=FF D8=FF, D9=FF D10=FF, D11=FF D12=FF, D13=FF D14=FF, D15=FF**
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	**D0=FF, D1=FF D2=FF, D3=FF D4=FF, D5=FF D6=FF, D7=FF D8=FF, D9=FF D10=FF, D11=FF D12=FF, D13=FF D14=FF, D15=FF**
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1: DQS signals toggle and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

Table 200 — IDD3P1 and IDD3P2 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Host Side Data[1]
toggling	0	0	Static HIGH	111 (DES)	**D0=00, D1=FF D2=FF D3=00 D4=FF, D5=00 D6=00, D7=FF D8=00, D9=FF D10=FF, D11=00 D12=FF D13=00 D14=00, D15=FF**
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF D7=00 D8=FF, D9=00 D10=00, D11=FF D12=00, D13=FF D14=FF D15=00**
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1: DQS signals toggle and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V_{DD}.

Table 201 — IDD4R1 - 84% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	DRAM Side Data[2]
toggling	0	0	0	**011 (RD)**	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=00, D9=FF D10=FF, D11=00 D12=FF, D13=00 D14=00, D15=FF**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	-
		4	1	111 (DES)	-
		5	1	111 (DES)	-
		6	1	111 (DES)	-
		7	1	111 (DES)	-
	1	8	0	**011 (RD)**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=FF D9=00 D10=00, D11=FF D12=00, D13=FF D14=FF, D15=00**
		9	1	101 (Rank 0, BL16)	-
		10	1	111 (DES)	-
		11	1	111 (DES)	-
		12	1	111 (DES)	-
		13	1	111 (DES)	-
		14	1	111 (DES)	-
		15	1	111 (DES)	-
	2	16-31	-	repeat Sub-Loop 0 & 1	
	3	32-37	1	111 (DES)	-
	4	38-75	-	repeat Sub-Loops 0, 1, 2, & 3, using Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD16 Commands.
NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command.

Table 202 — IDD4R2 - 25% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	DRAM Side Data[2]
toggling	0	0	0	**011 (RD)**	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=00, D9=FF D10=FF, D11=00 D12=FF, D13=00 D14=00, D15=FF**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	
		...	...	...	...
		...	...	...	...
		30	1	111 (DES)	
		31	1	111 (DES)	-
	1	32	0	**011 (RD)**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=FF, D9=00 D10=00, D11=FF D12=00, D13=FF D14=FF, D15=00**
		33	1	101 (Rank 0, BL16)	-
		34	1	111 (DES)	-
		35	1	111 (DES)	-
		...	...	...	...
		...	...	...	...
		62	1	111 (DES)	-
		63	1	111 (DES)	-
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD16 Commands, otherwise V_{DD}.
NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command, otherwise V_{DD}.

Table 203 — IDD4R3 - 84% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	DRAM Side Data[2]
toggling	0	0	0	**011 (RD)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	-
		4	1	111 (DES)	-
		5	1	111 (DES)	-
		6	1	111 (DES)	-
		7	1	111 (DES)	-
	1	8	0	**011 (RD)**	**D0=00 D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		9	1	101 (Rank 0, BL16)	-
		10	1	111 (DES)	-
		11	1	1111 (DES)	-
		12	1	111 (DES)	-
		13	1	111 (DES)	-
		14	1	111 (DES)	-
		15	1	111 (DES)	-
	2	16-31	-	repeat Sub-Loop 0 &1	
	3	32-37	1	111 (DES)	-
	4	38-75	-	repeat Sub-Loops 0, 1, 2, & 3, using Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD16 Commands.
NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command.

Table 204 — IDD4R4 - 25% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	DRAM Side Data[2]
toggling	0	0	0	**011 (RD)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	
		...	...	...	...
		...	...	...	...
		30	1	111 (DES)	
		31	1	111 (DES)	-
	1	32	0	**011 (RD)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		33	1	101 (Rank 0, BL16)	-
		34	1	111 (DES)	-
		35	1	111 (DES)	-
		...	...	...	...
		...	...	...	...
		62	1	111 (DES)	-
		63	1	111 (DES)	-
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to RD16 Commands, otherwise V_{DD}.
NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command, otherwise V_{DD}.

Table 205 — IDD4W1 - 84% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Data[2]
toggling	0	0	0	**010 (WR)**	**D0=00, D1=FF D2=FF D3=00 D4=FF, D5=00 D6=00, D7=FF D8=00, D9=FF D10=FF, D11=00 D12=FF, D13=00 D14=00, D15=FF**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	-
		4	1	111 (DES)	-
		5	1	111 (DES)	-
		6	1	111 (DES)	-
		7	1	111 (DES)	-
	1	8	0	**010 (WR)**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=FF, D9=00 D10=00, D11=FF D12=00, D13=FF D14=FF, D15=00**
		9	1	101 (Rank 0, BL16)	
		10	1	111 (DES)	-
		11	1	111 (DES)	-
		12	1	111 (DES)	-
		13	1	111 (DES)	-
		14	1	111 (DES)	-
		15	1	111 (DES)	-
	2	16-31	-	repeat Sub-Loop 0 & 1	
	3	32-37	1	111 (DES)	-
	4	38-75	-	repeat Sub-Loops 0, 1, 2, & 3, using Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR16 Commands.
NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command.

Table 206 — IDD4W2 - 25% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Data[2]
toggling	0	0	0	**010 (WR)**	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=00, D9=FF D10=FF, D11=00 D12=FF, D13=00 D14=00, D15=FF**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	-
		...	...	...	...
		...	...	...	...
		30	1	111 (DES)	-
		31	1	111 (DES)	-
	1	32	0	**010 (WR)**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=FF, D9=00 D10=00, D11=FF D12=00, D13=FF D14=FF, D15=00**
		33	1	101 (Rank 0, BL16)	-
		34	1	111 (DES)	-
		35	1	111 (DES)	-
		...	...	...	...
		...	...	...	...
		62	1	111 (DES)	-
		63	1	111 (DES)	-
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR16 Commands, otherwise V_{DD}.
NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command, otherwise V_{DD}.

Table 207 — IDD4W3 - 84% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Data[2]
toggling	0	0	0	**010 (WR)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	-
		4	1	111 (DES)	-
		5	1	111 (DES)	-
		6	1	111 (DES)	-
		7	1	111 (DES)	-
	1	8	0	**010 (WR)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		9	1	101 (Rank 0, BL16)	-
		10	1	111 (DES)	-
		11	1	111 (DES)	-
		12	1	111 (DES)	-
		13	1	111 (DES)	-
		14	1	111 (DES)	-
		15	1	111 (DES)	-
	2	16-31	-	repeat Sub-Loop 0 & 1	
	3	32-37	1	111 (DES)	-
	4	38-75	-	repeat Sub-Loops 0, 1, 2, & 3, using Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR16 Commands.
NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command.

Table 208 — IDD4W4 - 25% Utilization Measurement-Loop Pattern[1]

BCK_t, BCK_c	Sub-Loop	Cycle Number	BCS_n	BCOM	Data[2]
toggling	0	0	0	**010 (WR)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		1	1	101 (Rank 0, BL16)	-
		2	1	111 (DES)	-
		3	1	111 (DES)	-
		...	...	...	-
		...	...	...	-
		30	1	111 (DES)	-
		31	1	111 (DES)	-
	1	32	0	**010 (WR)**	**D0=00, D1=00 D2=00, D3=00 D4=00, D5=00 D6=00, D7=00 D8=00, D9=00 D10=00, D11=00 D12=00, D13=00 D14=00, D15=00**
		33	1	101 (Rank 0, BL16)	-
		34	1	111 (DES)	-
		35	1	111 (DES)	-
		...	...	...	-
		...	...	...	-
		62	1	111 (DES)	-
		63	1	111 (DES)	-
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0_t, [M]DQS0_c and [M]DQS1_t, [M]DQS1_c are used according to WR8 Commands, otherwise VDD.
NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR8 Command, otherwise VDD

20 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products.*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*

JESD21-C, *Configuration for Solid State Memories.*

JESD8-11A, *Definition of wide range non-terminated logic.*

JESD79-5, *DDR5 SDRAM Specification.*

JESD82-511, *DDR5RCD01 Specification.*

MO-276N, *Package Mechanical Outline.*

JS-001-2017, *Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test – Human Body Model (HBM) – Component Level.*

JS-002-2018, *ANSI/ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.*

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


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