JEDEC STANDARD

DDR5 Load Reduced (LRDIMM) and Registered Dual Inline Memory Module (RDIMM) Common Specification

JESD305

JANUARY 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2022
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2108

PRICE: Contact JEDEC

DDR5 LOAD REDUCED (LRDIMM) AND REGISTERED DUAL INLINE MEMORY MODULE (RDIMM) COMMON SPECIFICATION

Contents

1 Product Description 1
1.1 Related Documents 1
2 Environmental Requirements 2
3 Connector Pinout and Signal Description 3
4 Power Details 8
4.1 DIMM Voltage Requirements and Power-Up Sequence 8
4.2 Rules for PMIC Power-Up Sequence 8
4.3 Rules for PMIC Power Down Sequence 8
4.4 Rules for VDD and VDDQ Power Planes 8
5 Component Details 9
5.1 Component Types and Placement 10
5.2 Bulk and Distributed Decoupling Capacitance Guidelines 11
6 DIMM Design Details 12
6.1 Signal Groups 12
6.2 General Net Structure Routing Rules 13
6.2.1 Pre-RCD Address, Command and Control 15
6.2.2 Pre-RCD Clock 16
6.2.3 Post-RCD Clock, Control, Address and Command Groups 16
6.2.4 Post-RCD Address and Command Group 16
6.2.5 Post-RCD Clock and Control Groups 17
6.2.6 Pre-Data Buffer Data and Strobe Group (LRDIMM) 18
6.2.7 Post-Data Buffer Data and Strobe Group (LRDIMM) 20
6.2.8 Data and Strobe Group (RDIMM) 21
6.3 Design Rules 23
6.4 Impedance Targets 27
6.5 Rules for Compensation 27
6.5.1 Velocity 27
6.5.2 Via 27
6.6 Rules for Length Calculation 28
6.6.1 Pre-RCD and DQ/Strobe 28
6.6.2 Pre-DB (LRDIMM) 28
6.6.3 Post-DB (LRDIMM) 28
6.6.4 Pre-RCD Clock 28
6.6.5 Post-RCD Address/Command/Control/Clock 28
6.7 Rules for Registered and Load Reduced DIMM Designs 28
6.8 DQ Wiring to Support CRC 29
6.9 RDIMM and LRDIMM Configuration 30
6.9.1 DIMM Connectivity Wiring 30
6.9.2 Control Wiring 31
6.9.3 ALERT_n Circuit Wiring 31
6.9.4 RESET_n Circuit Wiring 32
6.10 ZQ Calibration Wiring 32
6.11 Sideband Bus Signal Wiring, Selection and Placement 33
7 DIMM Impedance Profile 34
8 Reference Stackup 35
9 Manufactured DIMMs 37

Contents (cont'd)

10 Serial Presence Detect Definition and Content 37
11 Product Label 37
12 JEDEC Process 37

Tables

Table 1 — DDR5 Product Family Attributes 2
Table 2 — (Example) Environmental Parameters 2
Table 3 — Pin Definitions 3
Table 4 — Input/Output Functional Description 4
Table 4 — Input/Output Functional Description (cont'd) 5
Table 5 — DDR5 288 Pin R/LR-DIMM Pin Wiring Assignments 6
Table 5 — DDR5 288 Pin R/LR-DIMM Pin Wiring Assignments (cont'd) 7
Table 6 — DDR5 R/LR- DIMM DC Operating Voltage 8
Table 7 — DDR5 x4/X8 SDRAM DIMM Pad Array 10
Table 8 — Registered and Load Reduced DIMM Decoupling Capacitor Guidelines 11
Table 9 — Simulation Conditions 14
Table 10 — Pre-RCD Address, Command and Control Length Definition Example 15
Table 11 — Pre-RCD Clock 16
Table 12 — Post-RCD Address and Command Length Definition Example 17
Table 13 — Pre-DB Lengths 19
Table 14 — Post-Data Buffer Data and Strobe Example (LRDIMM) 20
Table 15 — Example of 2Rx4 DQ/Strobe Lengths 22
Table 16 — Wiring 23
Table 16 — Wiring (cont'd) 24
Table 17 — Circuit Requirements 25
Table 18 — Spacing 26
Table 19 — SMBus Lengths 33
Table 20 — Example of Voltage Operating Conditions (for DRAM) 34
Table 21 — Example (12 layer) LRDIMM Stackup 35

Figures

Figure 1 — SDRAM Terminal Patterns (x4/x8) 9
Figure 2 — RDIMM 2Rx4 Topology 13
Figure 3 — LRDIMM 2Rx4 Topology 13
Figure 4 — RDIMM 2Rx4 Topology 15
Figure 5 — Pre-RCD Clock Topology Example 16
Figure 6 — Post-RCD Address and Command Topology Example 17
Figure 7 — Examples Pre-DB Data Topology (LRDIMM) 18
Figure 8 — Examples Post-Data Buffer Data and Strobe Net Structure (LRDIMM) 20
Figure 9 — Data Diagram Example (RDIMM) 21
Figure 10 — Example of DQ Wiring 29
Figure 11 — DDR5 2Rx4 (planar/3DS) Control Wiring 31
Figure 12 — Example Wiring of the ALERT_n Function - RDIMM and LRDIMM 31
Figure 13 — Example Wiring of the RESET_n Function - RDIMM and LRDIMM 32
Figure 14 — Block Diagram: Hub, PMIC, RCD, TS0, TS1 33
Figure 15 — Impedance Profile 34

DDR5 LOAD REDUCED (LRDIMM) AND REGISTERED DUAL INLINE MEMORY MODULE (RDIMM) COMMON SPECIFICATION

(From JEDEC Board Ballot JCB-21-32, formulated under the cognizance of the JC-45.1 Subcommittee on Registered DRAM Modules, Item 2273.07.)

1 Product Description

This standard defines the electrical and mechanical requirements for 288-pin, 1.1 Volt (VDD and VDDQ), DDR5 Registered (RDIMM) and Load Reduced (LRDIMM), Double Data Rate (DDR), Synchronous DRAM Dual In-Line Memory Modules (DIMM). These 288-pin Registered and Load Reduced DDR5 SDRAM DIMMs are intended for use in server, workstation, and database environments.

Reference design examples are included which provide an initial basis for DDR5 RDIMM and LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC5-4000, PC5-4800, PC5-5600, and PC5-6400 support. All DDR5 RDIMM and LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements, signal integrity, power delivery and efficiencies in the design.

1.1 Related Documents

JESD79-5, *DDR5 SDRAM Standard*

JESD300-5, *SPD5118 Hub & Serial Presence Detect Device Standard*

JESD301-1, *PMIC50x0 Power Management Integrated Circuit (PMIC) Device Specification*

JESD302-1, *TS5111, TS5110 Serial Bus Thermal Sensor Specification*

JESD400-5, *DDR5 Serial Presence Detect (SPD) Contents*

JESD401-5, *DDR5 DIMM Label*

JESD402-1, *Temperature Grade and Measurement Specifications for Components and Modules*

JESD403-1, *JEDEC Module Sideband Bus*

MO-210, *Square & andRectangular Die-Size, Ball Grid Array Family*

MO-329, 288 *pin DDR5 DIMM, 0.85 mm pitch*

1.1 Related documents (cont'd)

Table 1 — DDR5 Product Family Attributes

DIMM Organization	x80 (2x40) ECC (EC8) x72 (2x36) ECC (EC4)	Notes	Ref Specification(s)
DIMM Dimensions (nom)	133.35 mm x 31.25 mm		MO-329
Pin Count	288		MO-329
DDR5 SDRAMs Supported	8Gb, 16Gb, 32Gb	78/82-ball FBGA package for x4 and x8 devices	JESD79-5 MO-210 (AL, AN)
Capacity	(16Gb) 16GB - 1024GB (24Gb) 24GB – 1536GB	(DRAM) SDP, 2H, 4H, 8H, 16H	
SDRAM width	x4, x8	X8 is not used on LRDIMM	
Hub with Thermal Sensor	1024 byte		JESD300-5 JESD79-5
Voltage (External Supply)	VIN_Bulk: 12V (nominal)	Bulk input DC supply voltage from system	
	VIN_MGMT: 3.3V (nominal)	Management supply voltage from system	
Voltage (PMIC Output)	VDD: 1.1 V (nominal)	Supply voltage from PMIC	
	VDDQ: 1.1 V (nominal)	Supply voltage for I/O from PMIC	
	VPP: 1.8 V (nominal)	Pump voltage from PMIC	
	1.8V LDO (nominal)	From PMIC to HUB, TS	
	1.0V LDO Output (nominal)	From PMIC to HUB, TS, RCD	
DDR5 Interface	1.1V signaling	DRAM, RCD, Data Buffer	
I2C/I3C-Basic Interface	1.0V signaling	RCD, Hub, PMIC, Temp Sensors	JESD403-1

2 Environmental Requirements

Table 2 — (Example) Environmental Parameters

Symbol	Parameter	Rating	Units	
T_{OPR}	DRAM Operating Temperature	0 to +95	°C	
T_{STG}	Storage Temperature	-55 to +100	°C	

NOTE 1 Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs are at the minimum and maximum values. See JESD402-1 for details.

NOTE 2 Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

3 Connector Pinout and Signal Description

Table 3 — Pin Definitions

Pin Name	Description	Pin Name	Description
CA[6:0]_A **CA[6:0]_B**	Address and Command Bus	DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A **CS[1:0]_B**	Chip Select	CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B
PAR_A **PAR_B**	Parity input	DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clocks (true/positive)	DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clocks (complement/negative)	TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error	TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state	VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port	VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock	VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data	RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address	LBDQS	Loopback Data strobe output
LBDQ	Loopback Data output:		
NOTE 1 TDQSx and DQSx_t share a pin.			

3 Connector Pinout and Signal Description (cont'd)

Table 4 — Input/Output Functional Description

Symbol	Type	I/O Levels	Function
CK_t, CK_c,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA[6:0]_A **CA[6:0]_B**	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.
CS[1:0]_A **CS[1:0]_B**	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command codes. CS_n is also used to enter and exit the parts from power down mode and self-refresh mode. While not in self-refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self-refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
PAR_A **PAR_B**	Input	VDD	Each Command Address input parity is received on the DPAR pin and should maintain even parity across the channel CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
ALERT_n	Output	VDD	Alert: If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
RESET_n	CMOS Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
PCAMP	Input Output	3.6V (max)	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
HSCL	Input	VOUT_1.0 V	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard.
HSDA	Input/ Output	VOUT_1.0 V	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard.
HSA	Input	2.1 V max	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation
DQ[31:0]_A **DQ[31:0]_B**	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
CB[7:0]_A **CB[7:0]_B**	Input/ Output	VDD	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating
DQS[9:0]_A_t **DQS[9:0]_B_t** **DQS[9:0]_A_c** **DQS[9:0]_B_c**	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
TDQS[9:5]_A_t **TDQS[9:5]_B_t** **TDQS[9:5]_A_c** **TDQS[9:5]_B_c**	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs. Not used on LRDIMMs.

Table 5 — Input/Output Functional Description (cont'd)

Symbol	Type	I/O Levels	Function
DLBDQ	Output	VDDQ	Loopback Data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled the pin is either terminated or Hi-Z based on MR36: OP[2:0].
DLBDQS	Output	VDDQ	Loopback Data Strobe output: This is a single ended strobe with the rising edged aligned with Loopback Data edge, falling edge aligned with Data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36: OP[2:0].
RFU			Reserved for Future Use: No on DIMM electrical connection is present.
VIN_BULK	Supply		External power supply: 12 V, 4.25 V (min), 15 V (max)
VIN_MGMT	Supply		External power supply: 3.3 V, 3.0 V (min), 3.6 V (max)
VSS	Supply		Ground

3 Connector Pinout and Signal Description (cont'd)

Table 6 — DDR5 288 Pin R/LR-DIMM Pin Wiring Assignments

Front Side	Pin	Pin	Back side	Front Side	Pin	Pin	Back side
Pin Label			Pin Label	Pin Label			Pin Label
VIN_BULK	1	145	VIN_BULK	PAR_A	74	218	CK_c
RFU	2	146	VIN_BULK	VSS	75	219	VSS
VIN_MGMT	3	147	PCAMP		Key		
HSCL	4	148	HSA				
HSDA	5	149	RFU	CA0_B	76	220	RFU
VSS	6	150	RFU	VSS	77	221	CA1_B
DQ0_A	7	151	VSS	CA2_B	78	222	VSS
VSS	8	152	DQ2_A	VSS	79	223	CA3_B
DQ1_A	9	153	VSS	CA4_B	80	224	VSS
VSS	10	154	DQ3_A	VSS	81	225	CA5_B
DQS0_A_t	11	155	VSS	CA6_B	82	226	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c	VSS	83	227	PAR_B
VSS	13	157	DQS5_A_t, TDQS5_A_t	CS0_B_n	84	228	VSS
DQ4_A	14	158	VSS	VSS	85	229	CS1_B_n
VSS	15	159	DQ6_A	DLBDQ	86	230	VSS
DQ5_A	16	160	VSS	DLBDQS	87	231	RFU
VSS	17	161	DQ7_A	VSS	88	232	RFU
DQ8_A	18	162	VSS	CB4_B	89	233	VSS
VSS	19	163	DQ10_A	VSS	90	234	CB6_B
DQ9_A	20	164	VSS	CB5_B	91	235	VSS
VSS	21	165	DQ11_A	VSS	92	236	CB7_B
DQS1_A_t	22	166	VSS	DQS9_B_t, TDQS9_B_t	93	237	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c	DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	24	168	DQS6_A_t, TDQS6_A_t	VSS	95	239	DQS4_B_t
DQ12_A	25	169	VSS	CB0_B	96	240	VSS
VSS	26	170	DQ14_A	VSS	97	241	CB2_B
DQ13_A	27	171	VSS	CB1_B	98	242	VSS
VSS	28	172	DQ15_A	VSS	99	243	CB3_B
DQ16_A	29	173	VSS	DQ0_B	100	244	VSS
VSS	30	174	DQ18_A	VSS	101	245	DQ2_B
DQ17_A	31	175	VSS	DQ1_B	102	246	VSS
VSS	32	176	DQ19_A	VSS	103	247	DQ3_B
DQS2_A_t	33	177	VSS	DQS0_B_t	104	248	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c	DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	35	179	DQS7_A_t, TDQS7_A_t	VSS	106	250	DQS5_B_t, TDQS5_B_t
DQ20_A	36	180	VSS	DQ4_B	107	251	VSS

Table 7 — DDR5 288 Pin R/LR-DIMM Pin Wiring Assignments (cont'd)

Front Side	Pin	Pin	Back side	Front Side	Pin	Pin	Back side
Pin Label			Pin Label	Pin Label			Pin Label
VSS	37	181	DQ22_A	VSS	108	252	DQ6_B
DQ21_A	38	182	VSS	DQ5_B	109	253	VSS
VSS	39	183	DQ23_A	VSS	110	254	DQ7_B
DQ24_A	40	184	VSS	DQ8_B	111	255	VSS
VSS	41	185	DQ26_A	VSS	112	256	DQ10_B
DQ25_A	42	186	VSS	DQ9_B	113	257	VSS
VSS	43	187	DQ27_A	VSS	114	258	DQ11_B
DQS3_A_t	44	188	VSS	DQS1_B_t	115	259	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c	DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	46	190	DQS8_A_t, TDQS8_A_t	VSS	117	261	DQS6_B_t, TDQS6_B_t
DQ28_A	47	191	VSS	DQ12_B	118	262	VSS
VSS	48	192	DQ30_A	VSS	119	263	DQ14_B
DQ29_A	49	193	VSS	DQ13_B	120	264	VSS
VSS	50	194	DQ31_A	VSS	121	265	DQ15_B
CB0_A	51	195	VSS	DQ16_B	122	266	VSS
VSS	52	196	CB2_A	VSS	123	267	DQ18_B
CB1_A	53	197	VSS	DQ17_B	124	268	VSS
VSS	54	198	CB3_A	VSS	125	269	DQ19_B
DQS4_A_t	55	199	VSS	DQS2_B_t	126	270	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c	DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	57	201	DQS9_A_t, TDQS9_A_t	VSS	128	272	DQS7_B_t, TDQS7_B_t
CB4_A	58	202	VSS	DQ20_B	129	273	VSS
VSS	59	203	CB6_A	VSS	130	274	DQ22_B
CB5_A	60	204	VSS	DQ21_B	131	275	VSS
VSS	61	205	CB7_A	VSS	132	276	DQ23_B
ALERT_n	62	206	VSS	DQ24_B	133	277	VSS
VSS	63	207	RESET_n	VSS	134	278	DQ26_B
CS0_A_n	64	208	VSS	DQ25_B	135	279	VSS
VSS	65	209	CS1_A_n	VSS	136	280	DQ27_B
CA0_A	66	210	VSS	DQS3_B_t	137	281	VSS
VSS	67	211	CA1_A	DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
CA2_A	68	212	VSS	VSS	139	283	DQS8_B_t, TDQS8_B_t
VSS	69	213	CA3_A	DQ28_B	140	284	VSS
CA4_A	70	214	VSS	VSS	141	285	DQ30_B
VSS	71	215	CA5_A	DQ29_B	142	286	VSS
CA6_A	72	216	VSS	VSS	143	287	DQ31_B
VSS	73	217	CK_t	RFU	144	288	VSS

NOTE 1 Individual Annex Specifications for RDIMM and LRDIMM define pin use where multiple functions are possible.

4 Power Details

4.1 DIMM Voltage Requirements and Power-Up Sequence

The DIMM input voltage requirements and the SDRAM voltage requirements are not identical. The DIMM voltage requirements must meet the PMIC input voltage requirements. The PMIC output voltage requirements must meet the voltage requirements of SDRAM, RCD, Data Buffer, Hub and Temperature Sensors. There must be some allowance for a small voltage drop across the DIMM for both supply voltages and PMIC output voltages. Table 6 defines the requirements from the Host at the DIMM socket to the PMIC inputs, and the PMIC outputs.

Some DIMMs have lower current requirements. Each specific DIMM configuration must meet the voltage requirements for its worst-case load currents.

Table 8 — DDR5 R/LR- DIMM DC Operating Voltage

Symbol	Parameter	Voltage Rating (Volts)			Expected Current (Amps)[3]	Power State
		Min	Typ[4]	Max		
VIN_BULK	Host Supply Voltage	4.25	12.0	15	2.5 (maximum)	Operational
VIN_MGMT	Host Supply Voltage	3.0	3.3	3.6	0.110 (maximum)	Operational
VDD[1]	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
VDDQ[1]	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
VPP[1]	PMIC Output Supply Voltage	1.746	1.8	1.098	Note 5	Operational
1.8V LDO[2]	PMIC Output Supply Voltage	Note 6	1.8	Note 6	0.025 (maximum)	Operational
1.0V LDO[2]	PMIC Output Supply Voltage	Note 6	1.0	Note 6	0.020 (maximum)	Operational

NOTE 1 The SDRAM specification must be met and takes precedence over this document.
NOTE 2 PMIC, Hub, TS, RCD specifications must be met and takes precedence over this document.
NOTE 3 Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances.
NOTE 4 Typical voltage is platform dependent. This is a suggested value only.
NOTE 5 Maximum and Minimum Current ratings depend on PMIC (5000 or 5010), and number of DRAM and Data Buffers placed.
NOTE 6 See PMIC supplier datasheet for Minimum and Maximum ratings.

4.2 Rules for PMIC Power-Up Sequence

Refer to JESD301-1, PMIC50x0 Power Management IC Specification for sequence requirements.

4.3 Rules for PMIC Power Down Sequence

Refer to JESD301-1, PMIC50x0 Power Management IC Specification for sequence requirements.

4.4 Rules for VDD and VDDQ Power Planes

VDD and VDDQ are nominally the same voltage. Reference designs for RDIMM and LRDIMM raw cards will have individual planes for each voltage rail.

5 Component Details

The active components on the DIMM are the DDR5 SDRAM, RCD, Data Buffer (LRDIMM), PMIC, Temp Sensor, and Hub.

- The DDR5 SDRAM x4 and x8 are defined in JESD79-5 and MO-210
- The RCD component is defined in JESD82-511
- The Data Buffer is defined in JESD82-521
- The PMIC is defined in JESD301-1
- The Temperature Sensor is defined in JESD302-1
- The Hub (SPD) is defined in JESD300-5

The Annex Specification for each reference design will identify the maximum SDRAM package size the layout will accept. The SDRAM terminal pattern will determine if support balls are present in the reference design. Reference JEDEC MO-210 for terminal pattern features.

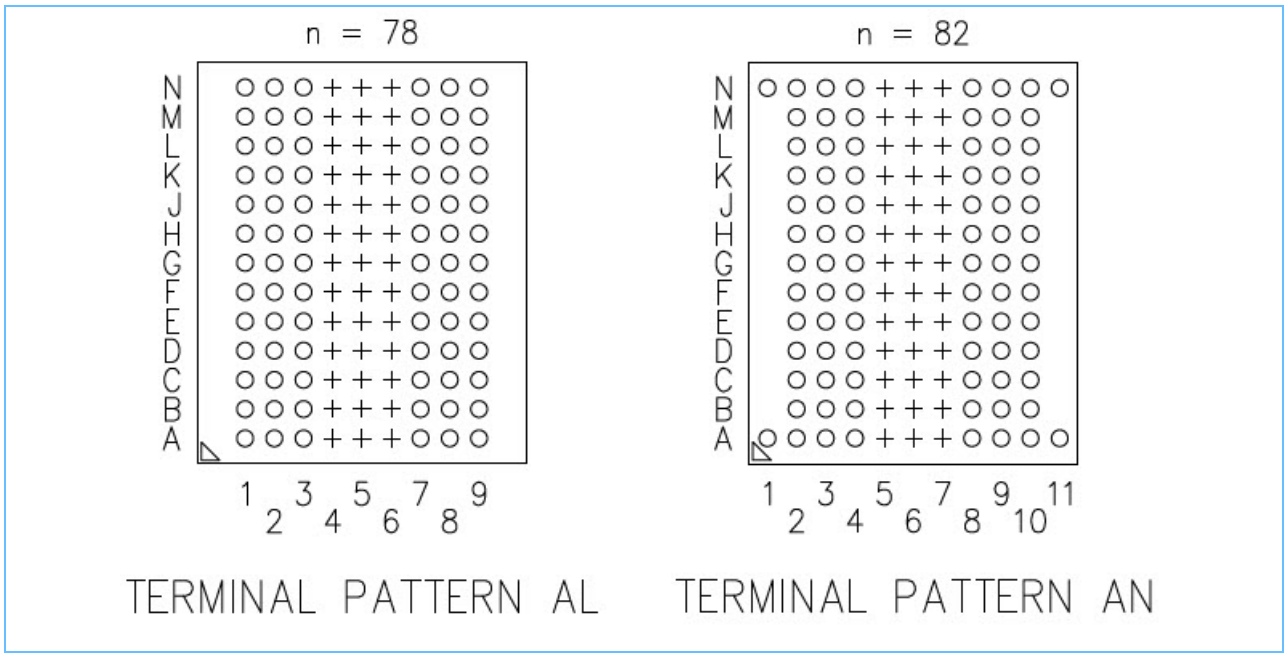

Figure 1 — SDRAM Terminal Patterns (x4/x8)

5 Component Details (cont'd)

Table 9 — DDR5 x4/X8 SDRAM DIMM Pad Array

Top View -- (MO-210 variations AL, AN (AN terminal pattern uses A1, A11, N1, N11 locations))

	1	2	3	4	5	6	7	8	9	10	11
		1	2	3	4	5	6	7	8	9	
A	NC[1]	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	NC[1]
B		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	
C		VSS	DQ0	DQS_t				DM_n[3] TDQS_t[3]	DQ1	VSS	
D		VDDQ	VSS	DQS_c				TDQS_c[2]	VSS	VDDQ	
E		VDD	DQ4[4]	DQ6[4]				DQ7[4]	DQ5[4]	VDD	
F		VSS	VDDQ	VSS				VSS	VDDQ	VSS	
G		CA_ODT	MIR	VDD				CK_t	VDDQ	TEN[5]	
H		ALERT_n	VSS	CS_n				CK_c	VSS	VDD	
J		VDDQ	CA4	CA0				CA1	CA5	VDDQ	
K		VDD	CA6	CA2				CA3	CA7	VDD	
L		VDDQ	VSS	CA8				CA9	VSS	VDDQ	
M		CA1	CA10	CA12				CA13	CA11	RESET_n	
N	NC[1]	VDD	VSS	VDD				VPP	VSS	VDD	NC[1]

NOTE 1 These balls are mechanical support balls for wide SDRAM packages.
NOTE 2 TDQS_c is not valid on x4 based SDRAM components.
NOTE 3 DM_n and TDQS_t are not valid on x4 based SDRAM components.
NOTE 4 DQ4, DQ5, DQ6 and DQ7 are not valid for x4 based SDRAM components.
NOTE 5 TEN must be tied low (VSS).

5.1 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR5 SDRAM signals.

Hub, PMIC and inductors are placed on secondary side and within zone defined in MO-329.

RCD and Temperature Sensors are placed on primary side of RDIMM and LRDIMM form factors except the RDIMM 1Rx8 which has Temperature Sensors on the secondary side.

Data Buffers are placed in Front-Back-Front-Back-Front configuration from RCD out to PCB sides.

5.2 Bulk and Distributed Decoupling Capacitance Guidelines

Table 10 — Registered and Load Reduced DIMM Decoupling Capacitor Guidelines

Signal	Guideline	Notes
VIN_BULK **VIN_MGMT**	Reference JESD301-1	
VDD	Distributed capacitance around SDRAM, Data Buffer should be such that impedance profile is met at each device.	See “DIMM Impedance Profile” Section for impedance profile threshold.
	Bulk capacitance, reference JESD301-1.	Capacitance at PMIC output.
VDDQ	Distributed capacitance around SDRAM and RCD should be such that impedance profile is met at each device.	See “DIMM Impedance Profile” Section for impedance profile threshold.
	Bulk capacitance, reference JESD301-1.	Capacitance at PMIC output.
VPP	Distributed capacitance around SDRAM should be such that impedance profile is met at each device.	See “DIMM Impedance Profile” Section for impedance profile threshold.
	Bulk capacitance, reference JESD301-1.	Capacitance at PMIC output.
1.8V LDO **1.0V LDO**	Reference respective JESD specifications for each active component.	Individual Annex Specifications will identify quantity, value, size, and location of placement.

NOTE 1 Total distributed decoupling capacitor values may vary by DIMM and may be staggered to achieve best overall impedance vs. frequency response.
NOTE 2 Bypass capacitors for DDR5 SDRAM devices are best located near the device power pins.
NOTE 3 Depending on the DRAM package size, capacitor placements may vary from raw card registration.

6 DIMM Design Details

6.1 Signal Groups

This specification categorizes DDR5 SDRAM timing-critical signals into specific groups. Figure 2 and Figure 3 summarizes the signals contained in each group for RDIMM and LRDIMM. All signal groups, except Data, implement a fly-by topology. Actual signal names in Annex may vary from individual reference design. The signal groups are:

Pre-RCD (LRDIMM & RDIMM)

- The Pre-RCD Address/Command and Control group includes: DCA[6:0]_[B:A], DCS[1:0]_[B:A]_n, DPAR_[B:A]
- The Pre-RCD Clock group includes: DCK_t and DCK_c
- The Pre-RCD Other group includes: ALERT_n, DRST_n
- The Pre-RCD Loopback group includes: DLBDQ_[B:A], DLBDQS_[B:A]

Data (DQ) and Strobe (DQS) - edge connector pin to Data Buffer (DB) (LRDIMM)

DQ and DQS - Data Buffer to SDRAM (LRDIMM)

DQ and DQS - edge connector pin to SDRAM (RDIMM)

Post-RCD to SDRAM (RDIMM and LRDIMM)

- The Post-RCD Address/Command group includes Q[B:A]CA[13:0]_[B:A]
- The Post-RCD Control group includes Q[B:A]CS[1:0]_[B:A]_n
- The Post-RCD Clock group includes Q[D:A]CK_[B:A]_t, Q[D:A]CK_[B:A]_c
- The Post-RCD Other group includes QRST_[B:A]_n, ALERT_[B:A]_n
- The Post-RCD Other group includes QLBDQ_[B:A], QLBDQS_[B:A] (RDIMM)

Post-RCD to Data Buffer (LRDIMM)

- The Post-RCD DB Control and Communication group for LRDIMM includes: BCS_[B:A]_n, BCOM[2:0]_[B:A], BRST_[B:A]_n, BCK_[B:A]_t, BCK_[B:A]_c
- Loopback group includes: QLBDQ_[B:A], QLBDQS_[B:A]

I2C/I3C (RDIMM and LRDIMM)

- The Host to Hub group: HSDA, HSCL, HSA
- The Hub local bus group: LSDA, LSCL

6.1 Signal Groups (cont'd)

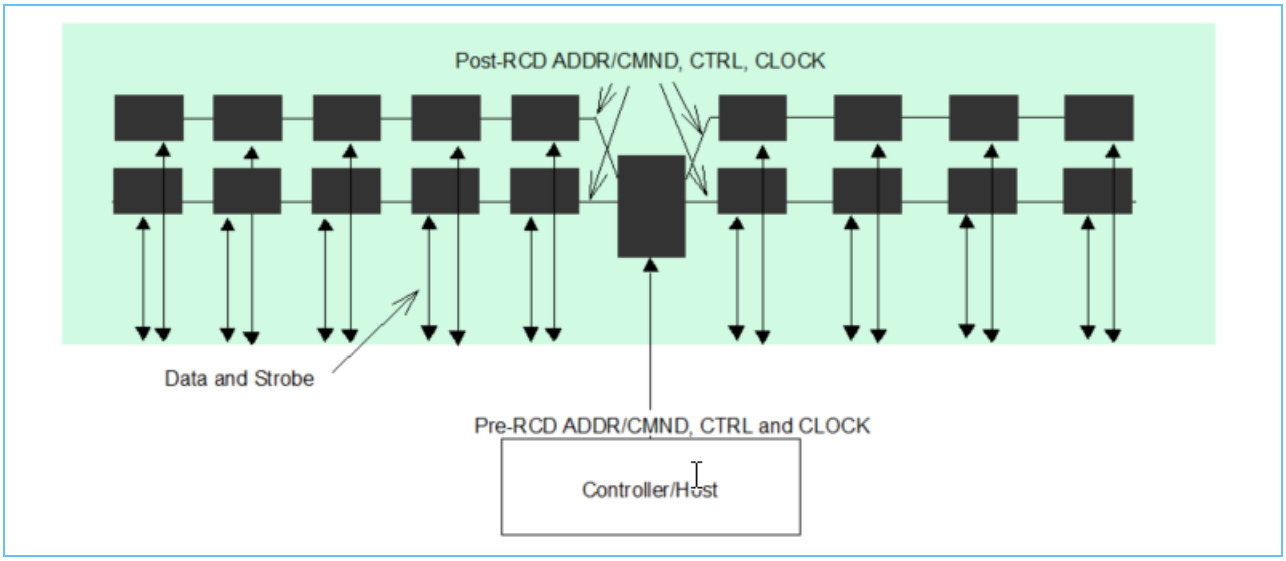

Figure 2 — RDIMM 2Rx4 Topology

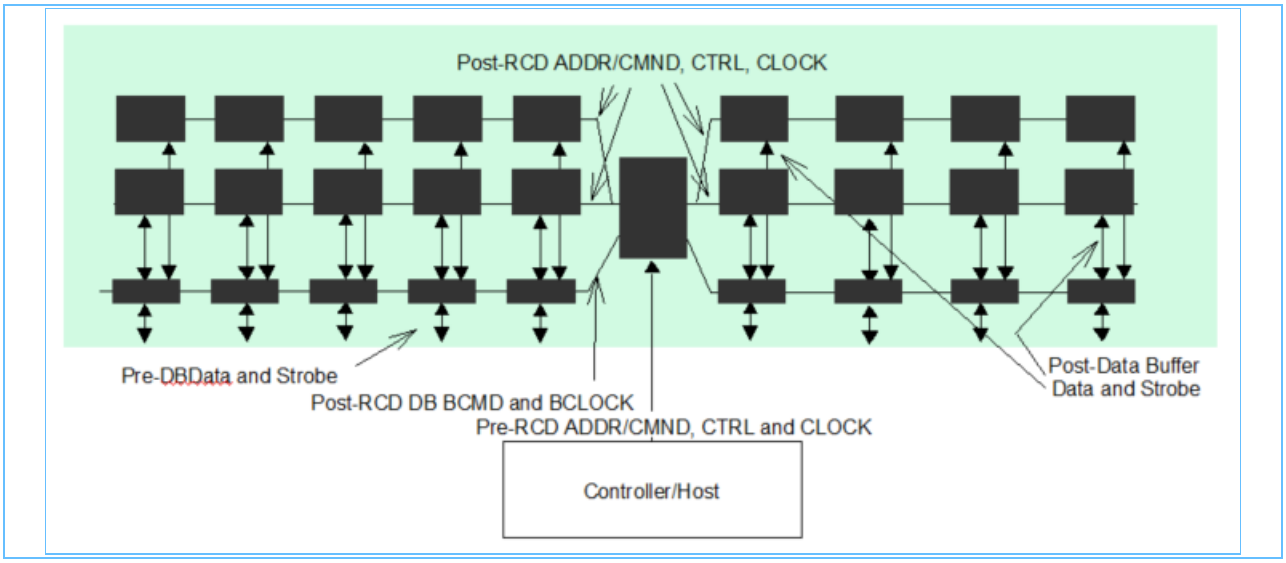

Figure 3 — LRDIMM 2Rx4 Topology

6.2 General Net Structure Routing Rules

The usual design process should be followed to develop an adequate design. Simulations are typically required, and timing budgets considered to verify adequate performance. Documenting line lengths alone does not ensure another design using those same line lengths will meet the intended speed. This is because there are parameters that are not documented that affect the design such as vias, length of the via path, routing layers used and how the actual line lengths fall within the minimum and maximum line length range. The design goal is to specify a tight range for a specific bus that has a well-controlled time relationship to the other critical signals, e.g., ADD/CMD to Clock.

6.2 General Net Structure Routing Rules (cont'd)

The approach to documenting DDR5 DIMM timing will be primarily simulation based for buses. Small groups of signals may be documented in terms of length only e.g., ALERT_n, RESET_n. A signal in each group will be documented in terms of length. Through simulation the other signals in the group will be adjusted such that the timing skew of the group is less than a specified number. This number will be identified and documented for each signal group.

The skew number is not a goal but merely the result of the design effort that produces a DIMM meeting the intended speed.

Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace segment length table that defines the length for the selected signal of the group. The Annex Specification will provide specific information for each signal group within the raw card design.

The remainder of this section provides a general overview of DDR5 net structure concepts and documents the routing rules to be followed in the design of the DDR5 DIMMs.

To use simulation almost exclusively, some conditions must be defined so that the same conclusion is reached using different simulation tools. See Table 9 for a definition of the simulation environment.

Table 11 — Simulation Conditions

Group	Parameter	Condition
Data **(RDIMM)** **(Pre-DB for LRDIMM)**	Motherboard Length	100 mm
	Motherboard Impedance	35 Ω (68 Ω differential for Strobes)
	Motherboard Configuration	One DIMM slot
	Routing Type	Stripline (Micro-strip)
	Driver	34 Ω DRAM with DRAM package (A different driver must be documented)
Post-DB DQ (LRDIMM)	Driver	34 Ω DRAM with DRAM package (A different driver must be documented)
Pre-RCD Addr/Cmnd, Ctrl	Motherboard Length	100 mm
	Motherboard Impedance	50 Ω (single ended)
	Motherboard Configuration	One DIMM per channel
	Driver	34 Ω DRAM with DRAM package (A different driver must be documented)
Pre-RCD Clock	Motherboard Length	100 mm
	Motherboard Impedance	50 Ω differential
	Motherboard Configuration	One DIMM per channel
	Driver	34 Ω DRAM with DRAM package (A different driver must be documented)
Post-RCD ADD/CMD	Driver	Registered Clock Driver
Post-RCD CTRL	Driver	Registered Clock Driver
Post-RCD CK[2]	Driver	Registered Clock Driver

NOTE 1 Any deviations from these conditions must be documented in the respective Annex Specification.
NOTE 2 Typically, these groups will be documented using length.

6.2.1 Pre-RCD Address, Command and Control

All signals except clock can be taken as a group within each channel since loading and signal rate are the same across ADD/CMD, and CTRL. Clock will be documented separately based on being routed as a differential pair.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one zero pattern should be used. Only steady state conditions should be included. To do this remove the first several clock periods. Remove the first five cycles if uncertain. For this group, VDD/2 should be used as the threshold for determining skew. Measure the time between the first and last crossing of VDD/2 of signals in the group. This is the skew to be documented.

Figure 4 illustrates the topology for the Pre-RCD ADD/CMD and CTRL. It will be used in conjunction with Table 11 to define the timing requirements for this group.

In this example, A0 is chosen as the net to be defined by length. All other signals will be adjusted in length such that the skew is met. In the example of Table 11, 30ps is chosen as the skew.

Actual skew value is to be determined by the respective reference design sponsor.

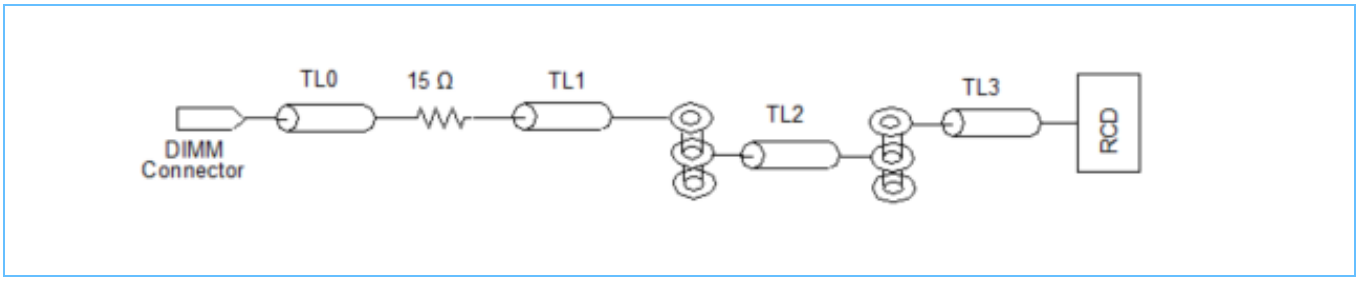

Figure 4 — RDIMM 2Rx4 Topology

Table 12 — Pre-RCD Address, Command and Control Length Definition Example

Signal	TL0	TL1	TL2	TL3	TL0+TL1+TL2+TL3 (Compensated[5])
DCA0_A	2.7	1.0	6.9	0.5	10.7
DCA0_B	2.7	0.4	7.4	.5	10.7

NOTE 1 DIMM vendor may adjust TL0 or TL1 length to accommodate component pin pitch and pad size discrepancy with reference design
NOTE 2 Signal DCA0_[B:A] may be anywhere within the timing skew
NOTE 3 Compensated tolerance length is ± 1.00 mm excluding pin pitch adjustment
NOTE 4 See 6.6.1 for Compensation
NOTE 5 Compensated length for Address and Command are ≤ 12.5 mm
NOTE 6 Compensated length for Chip Select is ≤ [ADD/CMD]max + 3.0 mm
NOTE 7 Match Sub-channel A C/A and Sub-channel B C/A group signal lengths to within 0.3 mm
NOTE 8 Match Sub-channel A CS and Sub-channel B CS group signal lengths to within 0.3 mm

6.2.2 Pre-RCD Clock

Clock is routed as differential pair.

Figure 5 illustrates the topology for the Pre-RCD Clock. It will be used in conjunction with Table 11 to define the requirements for this group. Since it is a single signal a timing tolerance is not required, and length alone will be used

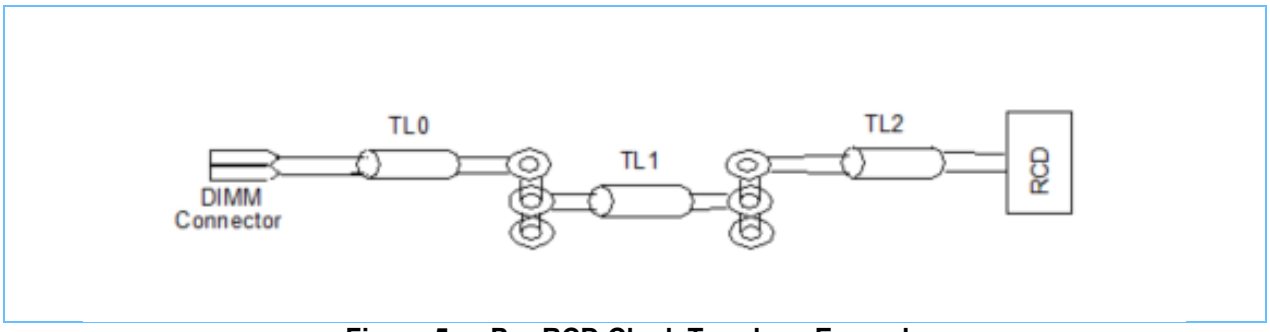

Figure 5 — Pre-RCD Clock Topology Example

Table 13 — Pre-RCD Clock

Signal	TL0	TL1	TL2	TL0+TL1+TL2 Compensated
CK_t	2.2	5.0	0.5	7.5
CK_c	2.2	5.0	0.5	7.5

NOTE 1 CK_t and CK_c compensated length to be within 0.1 mm
NOTE 2 Compensation = TL0/1.1 + Tl1 + TL2/1.1
NOTE 3 See 6.6.4 for Compensation

6.2.3 Post-RCD Clock, Control, Address and Command Groups

The DDR5 DIMMs implement a fly-by topology for routing CK, CTRL, and ADD/CMD signal groups independently for Channel A and Channel B. Each group, CK, ADD/CMD, and CTRL, will be documented separately. This division is based on possible loading differences.

6.2.4 Post-RCD Address and Command Group

Loading differences require the ADD/CMD group to be treated separately from the Clock and Control groups. The ADD/CMD group is further divided into RCD outputs of left side (Channel A) and a right side (Channel B) groups. Document the length of one signal in each group per Channel per RCD output. Use simulation to match the timing of the group to be within a defined skew.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this remove the first several clock periods. Remove the first five cycles if uncertain. VDD/2 should be used by this group as the threshold to determine skew. Where there are multiple ranks, rank 0 will be used to define skew. All rank 0 SDRAM locations must be evaluated separately. The maximum skew for all rank 0 SDRAMs is to be the skew documented. One method is graphical where all signals for a group at one SDRAM are plotted. Measure the time between the first and last signal crossing VDD/2. This is the skew for this DRAM. Repeat this for each rank 0 SDRAM on each Channel. The maximum is the skew to be documented.

Actual skew value is to be determined by the respective reference design sponsor. The skew is to be documented.

Figure 6 illustrates a topology example for the Post-RCD ADD/CMD. It will be used in conjunction with Table 12 to define the timing requirements for this group.

6.2.4 Post-RCD Address and Command Group (cont'd)

TL2 is not used in compensation method as length is the same for all signals at all DRAM pin locations.

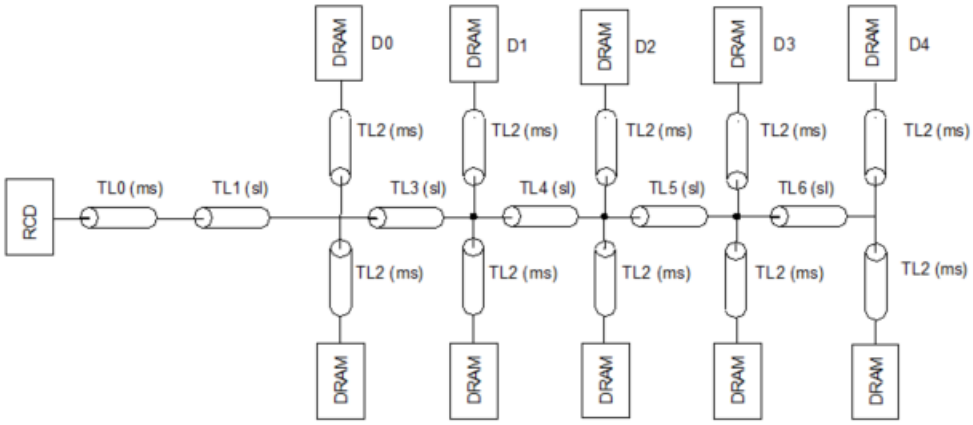

Figure 6 — Post-RCD Address and Command Topology Example

Table 14 — Post-RCD Address and Command Length Definition Example

Signal	TL0 (MS)	TL1 (SL)	TL3 (SL)	TL4 (SL	TL5 (SL)	TL6 (SL)	TL2 (MS)
QACA0_A	0.5	15.5	13.0	13.0	13.0	13.0	0.6
QBCA0_A	0.5	23.8	13.0	13.0	13.0	13.0	0.6
QACA0_B	0.5	15.6	13.0	13.0	13.0	13.0	0.6
QBCA0_B	0.5	23.9	13.0	13.0	13.0	13.0	0.6

NOTE 1 Signal QxCAx_x may be anywhere within the timing skew at each DRAM.
NOTE 2 TL3, TL4 may be of same segment length
NOTE 3 Via = Via length travel, add if signals change layers between DRAM
NOTE 4 Compensated tolerance length is ± 1.00 mm
NOTE 5 Compensation D0 = (TL0/1.1 + Via + TL1)
NOTE 6 Compensation D1 = (TL0/1.1 + Via + TL1 + Via + TL3)
NOTE 7 Compensation D2 = (TL0/1.1 + Via + TL1 + Via + TL3 + Via + TL4)
NOTE 8 Compensation D3 = (TL0/1.1 + Via + TL1 + Via + TL3 + Via + TL4 + Via +TL5)
NOTE 9 Compensation D4 = (TL0/1.1 + Via + TL1 + Via + TL3 + Via + TL4 + Via +TL5 + Via + TL6)

6.2.5 Post-RCD Clock and Control Groups

This group will use the same approach as the Post-RCD Address/Command Group. Clock and Control (Chip Select) will be documented in the Annex Specification separately when loading is different. Clock and Control segment length will be designed to align with Address/Command and will be defined in each raw card Annex. Refer to 6.2.4, Post-RCD Address/Command, for details.

Match Clock_t and Clock_c TLx segments to be within 0.1 mm. Match Clock_t and Clock_c compensated overall length to be within 0.1 mm.

6.2.6 Pre-Data Buffer Data and Strobe Group (LRDIMM)

This group contains the Data, Checkbits and Strobe signals. LRDIMM only uses x4 DRAM

There are 10 subgroups per Channel that are identified based on each strobe with half the Data bits coming from each side of the DIMM to each Data Buffer. Each subgroup (4 Data and a strobe pair) will be called a lane. Each lane for a x4 DRAM is also known as a nibble. The Strobe for each lane will be routed differentially and documented using length. One Data net within each lane will be documented in length. A timing skew will be documented for each lane. Skew will be applied to each lane separately. Each lane may have different timing. Figure 7 illustrates Pre-DB topologies. Table 13 depicts an example for Pre-Data Buffer Data, Checkbits and Strobe definition.

Actual skew value is to be determined by the respective reference design sponsor.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this remove the first several clock periods. Remove the first five cycles if uncertain. For this group a threshold is determined by looking at the cross point of the rising and falling edges in an eye pattern. Select a threshold that would provide the smallest skew. Where there are multiple ranks only evaluate the timing for SDRAMs making up rank 0. Measure the time between the first and last signal crossing. This is the skew for this lane. Repeat this for each lane. The maximum skew for each lane is to be documented.

DQS is not to be included in the skew measurement.

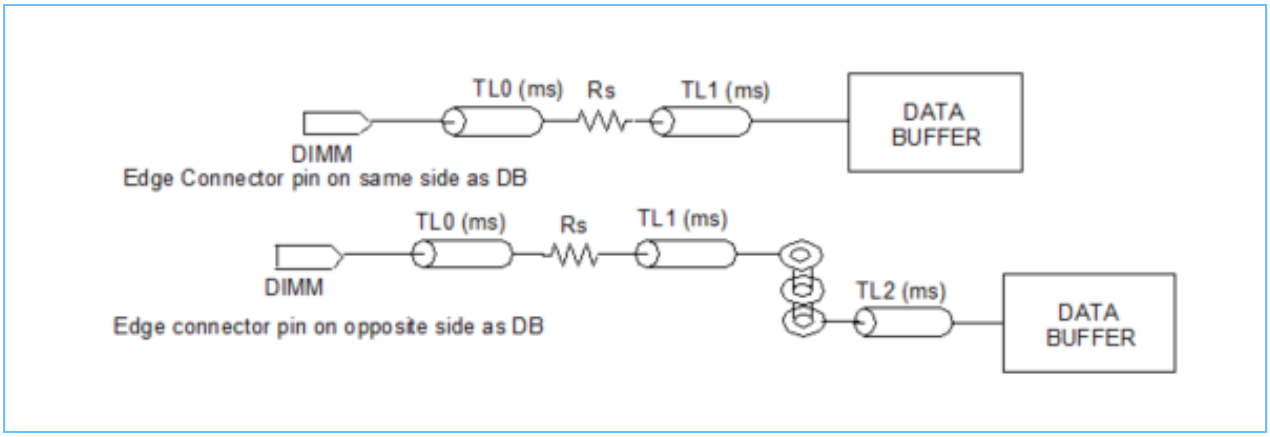

Figure 7 — Examples Pre-DB Data Topology (LRDIMM)

Table 15 — Pre-DB Lengths

Signal	TL0	TL1	TL2	TL0+TL1+TL2 (Compensated)	Rs (Ω)	Bus
DQS0_A_t, DQS0_A_c	3.5	1.0	na	4.1	15 ± 5%	-
DQ0_A	2.8	0.9	na	3.4	15 ± 5%	DQ[3:0]_A
DQS5_A_t, DQS5_A_c	3.6	0.5	0.4	4.1	15 ± 5%	-
DQ4_A	2.8	0.9	na	3.4	15 ± 5%	DQ[7:4]_A
…						
DQS4_A_t, DQS4_A_c	3.5	0.9	na	4.0	15 ± 5%	-
CB0_A	2.8	0.9	na	3.4	15 ± 5%	CB[3:0]_A
DQS9_A_t, DQS9_A_c	3.5	0.6	0.4	4.1	15 ± 5%	
CB6_A	2.8	0.9	1.9	5.1	15 ± 5%	CB[4:7]_A

Channel B will have a similar table for B-side Post-Data Buffer Data, Checkbits and Strobe.

NOTE 1 DIMM vendor may adjust TL0 or TL1 length to accommodate component pin pitch and pad size discrepancy with reference design.
NOTE 2 Signal DQx_x may be anywhere within the timing skew.
NOTE 3 All segments are microstrip.
NOTE 4 DQS_t to DQS_c match TLx segments to within 0.1mm.
NOTE 5 Compensated tolerance length is ± 1.00 mm excluding pin pitch adjustment.
NOTE 6 Compensation = (TL0/1.1 + TL1/1.1 + (VTL) + TL2/1.1)
NOTE 7 Compensated length for DQ Max is ≤ 7.0 mm
NOTE 8 Compensated DQ -to- DQ Skew ≤ 3.5 mm
NOTE 9 Compensated DQS -to- DQ skew [DQS-DQ] ≤ 3.5 mm.
NOTE 10 Compensated DQ to DQS min - na

6.2.7 Post-Data Buffer Data and Strobe Group (LRDIMM)

This group will follow an approach similar to the Pre-Data Buffer group. Actual skew value is to be determined by the respective reference design sponsor. The skew is to be documented.

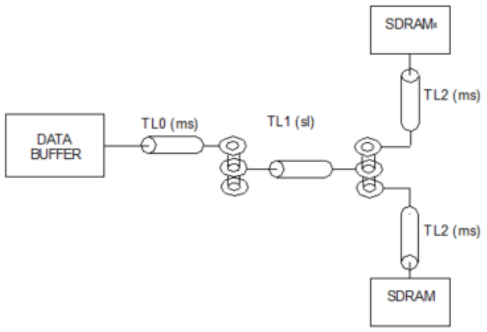

Figure 8 — Examples Post-Data Buffer Data and Strobe Net Structure (LRDIMM)

Table 16 — Post-Data Buffer Data and Strobe Example (LRDIMM)

Signal	TL0	TL1	TL2	TL0+TL1+TL2 (Compensated)	Bus
DQS0_A_t, DQS0_A_c	1.1	5.0	1.8	7.7	-
DQ0_A	0.6	6.2	0.6	7.3	DQ[3:0]_A
DQS5_A_t, DQS5_A_c	1.1	19.4	1.8	22.0	-
DQ4_A	0.4	19.9	0.6	20.7	DQ[7:4]_A
. .					
DQS4_A_t, DQS4_A_c	1.1	11.8	1.8	14.4	-
CB0_A	0.4	16.4	0.6	17.3	CB[3:0]_A
DQS9_A_t, DQS9_A_c	1.1	18.8	1.8	21.4	
CB4_A	0.6	18.2	0.6	19.3	CB[4:7]_A
Channel B will have a similar table for B-side Post-Data Buffer Data, Checkbits and Strobe.					

NOTE 1 Signal DQx_x may be anywhere within the timing skew
NOTE 2 Match DQS_t and DQS_c overall compensated length to be within 0.1 mm
NOTE 3 Compensated tolerance length is ± 1.00 mm
NOTE 4 Compensation = (TL0/1.1 + VTL + TL1)
NOTE 5 Compensated length for DQ Max ≤ 24 mm, and Strobe Max is ≤ 27.0 mm
NOTE 6 Compensated DQ and DQS minimum ≥ 8 mm
NOTE 7 Compensated DQ -to- DQ Skew ≤ 1.0 mm
NOTE 8 Compensated DQS -to- DQ skew [DQS-DQ] ≤ 6.0 mm

6.2.8 Data and Strobe Group (RDIMM)

This group contains the Data, Checkbits and Strobe signals. RDIMM can use x4 or x8 DRAM.

There are 9 (EC4) or 10 (EC8) subgroups per Channel that are identified based on each strobe with half the Data bits coming from each side of the DIMM to each DRAM. Each subgroup (4 Data or 8 Data, and a strobe pair) will be called a lane. Each lane for a x4 DRAM is also known as a nibble. Each lane for a x8 DRAM is known as a byte. The Strobe for each lane will be routed differentially and documented using length. One Data net within each lane will be documented in length. A timing skew will be documented for each lane. Skew will be applied to each lane separately. Each lane may have different timing. Figure 9 illustrates Data topologies. Table 15 depicts an example for Data, Checkbits and Strobe definition.

Actual skew value is to be determined by the respective reference design sponsor.

Simulations should be done at typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this remove the first several clock periods. Remove the first five cycles if uncertain. For this group a threshold is determined by looking at the cross point of the rising and falling edges in an eye pattern. Select a threshold that would provide the smallest skew. Where there are multiple ranks only evaluate the timing for SDRAMs making up rank 0. Measure the time between the first and last signal crossing. This is the skew for this lane. Repeat this for each lane. The maximum skew for each lane is to be documented.

Strobe is not to be included in the skew measurement.

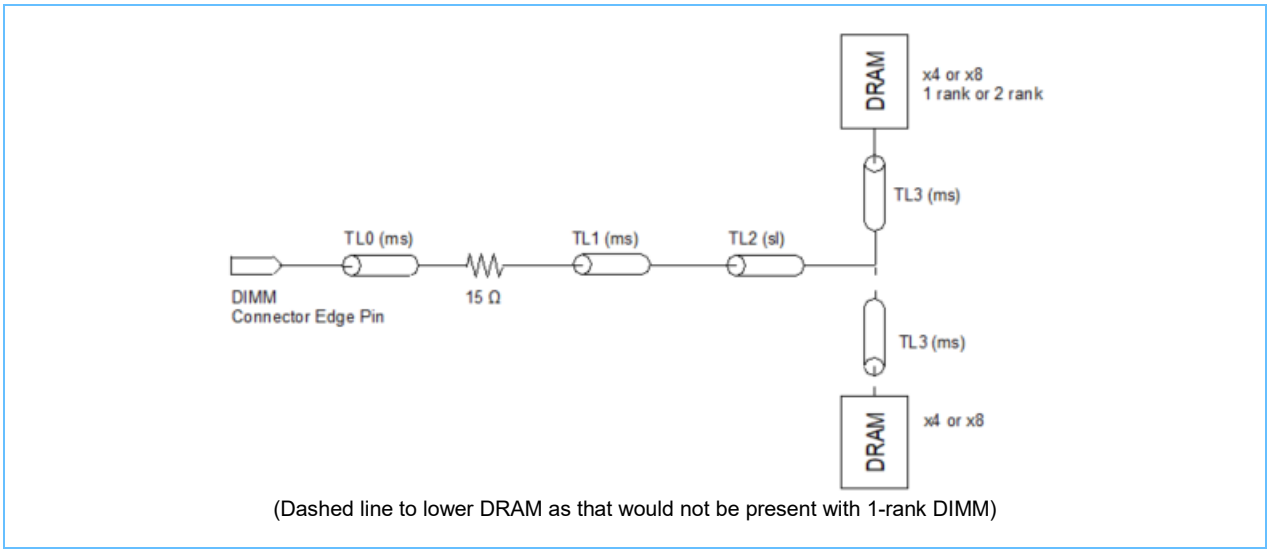

Figure 10 — Data Diagram Example (RDIMM)

Table 18 — Example of 2Rx4 DQ/Strobe Lengths

Signal	TL0 (ms)	TL1 (ms)	TL2 (sl)	TL3 (ms)	TL0+TL1+TL2 (Compensated)	Bus
DQS0_A_t, DQS0_A_c	3.2	0.8	7.1	1.8	11.8	-
DQ0_A	3.1	0.7	5.5	0.6	10.0	DQ[3:0]_A
DQS5_A_t, DQS5_A_c	3.2	0.8	18.9	1.8	23.5	-
DQ4_A	2.9	0.8	18.4	0.6	22.8	DQ[7:4]_A
. . .						
DQS4_A_t, DQS4_A_c	3.2	0.8	9.5	1.8	14.2	-
CB0_A	3.2	0.8	12.2	0.6	16.8	CB[3:0]_A
DQS9_A_t, DQS9_A_c	3.2	0.8	19.5	1.8	24.1	
CB4_A	2.9	0.8	17.9	0.6	22.3	CB[4:7]_A
		Channel B will have a similar table for B-side Post-Data Buffer Data, Checkbits and Strobe.				

NOTE 1 TL0, TL1 and TL3 are micro-strip and TL2 is stripline
NOTE 2 DIMM vendor may adjust TL0 or TL1 length to accommodate component pin pitch and pad size discrepancy with reference design
NOTE 3 Match DQS_t and DQS_c TL0 segments to be within 0.1 mm, and overall compensated length to be within 0.1 mm
NOTE 4 Signal DQx_x may be anywhere within the timing skew
NOTE 5 Compensated tolerance length is ± 1.00 mm
NOTE 6 Compensation = (TL0/1.1 +TL1/1.1 + Via + TL2)
NOTE 7 Compensated DQ and DQS minimum ≥ 8.5 mm
NOTE 8 Compensated DQ maximum ≤ 24 mm
NOTE 9 Compensated DQ -to- DQ Skew ≤ 1.0 mm
NOTE 10 Compensated DQS maximum ≤ 27 mm
NOTE 11 Compensated DQS -to- DQ skew [DQS-DQ] ≤ 5.0 mm

6.3 Design Rules

Table 19 — Wiring

(R/LR-DIMMs)	Channel-A		Channel-B	
MIR (Mirror)	Frontside DRAM	Backside DRAM	Frontside DRAM	Backside DRAM
	VSS	VDDQ	VDDQ	VSS
CA_ODT	Last SDRAM (Front/Back) from RCD	All Other SDRAM (Front/Back)	Last SDRAM (Front/Back) from RCD	All Other SDRAM (Front/Back)
	VDDQ	VSS	VDDQ	VSS
CAI	Top Row (Front/Back)	Bottom Row Front/Back)	Top Row (Front/Back)	Bottom Row Front/Back)
	VDDQ	VSS	VDDQ	VSS
TEN	All SDRAM	VSS	All SRDRAM	VSS
QCA	2Rx4 (RDIMM & LRDIMM)	Top Upper A (AB-CA/CS0,CK0B) B (BB-CA/CS0,CK1B)	Bottom Upper A (AB-CA/CS1,CK0D) B (BB-CA/CS1,CK1D)	
		Top Lower A (AA-CA/CS0,CK0A) B (BA-CA/CS0,CK1A)	Bottom Lower A (AA-CA/CS1,CK0C) B (BA-CA/CS1,CK1C)	
	1Rx4 (RDIMM)	Top A (AA-CA/CS0,CK0A) B (BA-CA/CS0,CK1A)	Bottom A (AACA,ABCS0,CK0C) B (BACA,BBCS0,CK1C)	
	2Rx8 (RDIMM)	Top A (AA-CA/CS0,CK0A) B (BA-CA/CS0,CK1A)	Bottom A (AA-CA/CS1,CK0C) B (BA-CA/CS1,CK1C)	
	1Rx8 (RDIMM)	Top/Bottom A (AA-CA/CS0,CK0A)	Top/Bottom B (BA-CA/CS0,CK1A)	
A13	If “MIR” pin tied to GND – A13 to A13, A12 to A12 If “MIR” pin tied to VDDQ – A13 to A12, A12 to A13			
NC/NU/RFU Pins	SDRAM - Not connected (Floating)			
	PMIC - GND corner pins. For all others, check with vendor			
LoopBack Data/Strobe	RDIMM	Each channel has a daisychain from RCD through DRAM. 2 row designs start at lower row SDRAM and continue through upper row ending with DRAM closest to RCD		
	LRDIMM	Each channel has a daisychain from RCD through DBs		
DCS1	Must be routed to RCD for all RDIMM and LRDIMM raw cards.			

Table 20 — Wiring (cont'd)

(R/LR-DIMMs)	Channel-A		Channel-B	
SDRAM	Nominal package (10.0x11.0), Maximum package (10.1x11.1) mm			
DIMM Outline	The outline is compliant with MO-329, Variation AAxx			
Via	- Signal vias must not be placed close together (except differential signals). Recommended to place power or GND via between Signal vias. - Signal vias under SDRAM are not to be placed vertically or horizontally adjacent in BGA grid. - 0.200 (Drill) / 0.400 (pad) / 0.600 (anti-pad) mm is standard size			
Component Pads	Pads for all other components are left to the reference card designer to define. Manufacturers of these R/LR-DIMM reference designs may adjust pad sizes and geometry.			
Inductor Area	Remove via and plane shapes/traces in between inductor pads on surface layer			
Temperature Sensor Location	**See Raw Card Annex for location and position**			
BGA Pad Size	SDRAM	0.350 mm		
	RCD, DB, TS	0.270 mm		

Table 21 — Circuit Requirements

		LDO 1.8V	LDO 1.0V	
SMBus	Hub	1.0uF	1.0uF	Place near device pin
	PMIC	0.1uF 4.7uF	0.1uF 4.7uF	
	RCD	na	0.1uF	
	TS[1,0]	0.1uF	0.1uF	

		Signal	RDIMM	LRDIMM
Impedance	Single Ended	DQ	35	35 / 35
		DCA / QCA	50	50
		BCOM	na	50
		ALERT / RESET	50	50
		LBDQ	50	50
		LBDQS	50	25
		SCL / SDA / PCAMP	50	50
		SAA / ZQ	na	na
	Differential Pairs SE by design (Diff Z @ 0.100 mm space)	DQS[1]	35 (68)	35 / (68) (Pre & Post)
		DCK[1]	50 (85)	50 (85)
		QCK[1]	25 (45-50)	25 (45-50)
		BCK[1]	na	25 (50)

1. Differential Impedance is result of single ended impedance traces at spacing of 0.100 mm. DIMM vendors may adjust spacing to optimize their design.

Series Resistor	DQ / Strobe (RDIMM & Pre-DB)	15 Ω	Place close to edge finger
	Addr/Cmnd/Ctrl	15 Ω	Pre-RCD, place close to edge finger

Termination (LRDIMM)	BCK_t/c	30 Ω Resistor to VDDQ for each at end of daisychain
	BCS_n, BCOM[2:0]	43 Ω Resistor to VDDQ at end of daisychain

Signals	Reference		
DQ, DQS, Address, Command, Control, Parity, Clock	Ground (VSS)		

Edge Finger Pin-1 Capacitor	Vin_Bulk	(1) 10 uF 0603	Applies to all raw cards for RDIMMs and LRDIMM
	Vin_Mgmt	(1) 4.7uF 0402	

Table 22 — Spacing

These are the spacing rules for traces and space including keepout requirements. Violations of the Rules are to be noted in the Annex for the specific raw card. It is preferred that additional details be included to identify the areas of the violations. These rules are for design of the reference card only. It is not required that these rules be met by individual manufacturers building from the reference designs. These design rules are intended to be used for the reference DIMM designs submitted to JEDEC for ballot. DIMMs manufactured from the reference designs may use modified rules to support their manufacturing process.

Category	Item	Value (mm)	
Spacing	copper to copper (Outer/Inner)	0.075 / 0.070	
	Pad to pad (For pads of different components that are soldered down)	0.200	
	Line to (N)SMD pad (12V / the others)	0.113 / 0.100	
	Line to line (Single / Diff pair)	0.100 / 0.090	
	Line to Shape	0.125	Where impedance is important, use the 0.20 rule.
	Shape to Shape	0.100	
	Via (pad) to NSMD pad (12V / the others / same Net)	0.113 / 0.100 / 0.100	
	Via (pad) to SMD pad (12V / the others / same Net)	0.113 / 0.100 / 0.020	
	Via (pad) to Via (pad)	0.125	
	Via (pad) to Line (Outer/Inner)	0.09 / 0.07	
	Drill wall to Board edge (nominal)	0.450	Nominal board edge and drill being centered in pad
Comp to Comp	IC to IC (max. PKG size)	0.250	Inductor is assumed IC. (Max PKG size 4.3mm)
	IC (max.) to Passive (nominal)	0.250	
	Passive to Passive (nominal PKG size)	0.250	
Copper Keepout	Board top edge (nom) to copper	0.250	
Component Keepout	DIMM w/o HS - Top edge of board to Passive (max.) or IC (max.)	0.300	Nominal board edge and package body max. size criteria
	DIMM w/ HS - Top edge of board to Passive (max.) or IC (max.)	TBD	
Traces	Outer Layer Trace Width (minimum)	0.90	
	Inner Layer Trace Width (minimum)	0.60	

NOTE 1 These design rules are intended to be used for the reference DIMM designs submitted to JEDEC for ballot. DIMMs manufactured from the reference designs may use modified rules to support their manufacturing process.

6.4 Impedance Targets

The impedances defined here are the RDIMM and LRDIMM reference design targets.

1. 50 Ω ± 10%
2. 35 Ω ± 5 ohms
3. 25 Ω ± 5 ohms

The differential signal pair (clock and strobe) traces are routed with the single ended traces defined above with 0.100 mm space (nominal).

Signal Type	Impedance (ohm)	Note
Pre-RCD Clock	50	
Post-RCD Clock	25	Differential with 0.100mm space is ~45-50 ohm
Pre-RCD Address, Command, Control	50	
Post RCD Address, Command, Control	50	
Data (RDIMM)	35	
Strobe (RDIMM)	35	Differential with 0.100mm space is ~68ohm
Data (LRDIMM)	35	
Strobe (LRDIMM)	35	Differential with 0.100mm space is ~68ohm
ALERT_n, RESET_n, PCAMP	50	
BCOM	50	
BCK	25	Differential with 0.100mm space is ~50 ohm
LBDQ	50	
LBDQS (RDIMM / LRDIMM)	50 / 25	
PWR_GOOD, SAA, ZQ	n/a	

6.5 Rules for Compensation

6.5.1 Velocity

Velocity compensation for microstrip line to stripline is to divide the microstrip length by a factor of 1.1

SL = MS/1.1

6.5.2 Via

Via compensation is 1x the length of via barrel traveled by the signal.

6.6 Rules for Length Calculation

Via = travel length of signal

6.6.1 Pre-RCD and DQ/Strobe

One Rank DIMM - TL0/1.1 + TL1/1.1 + Via +TL2 + Via + TL3/1.1

Two Rank DIMM - TL0/1.1 + TL1/1.1 + Via +TL2

6.6.2 Pre-DB (LRDIMM)

DB on side of signal edge pin - TL0/1.1 + TL1/1.1

DB on opposite side of signal edge pin - TL0/1.1 + TL1/1.1 + Via +TL2/1.1

6.6.3 Post-DB (LRDIMM)

DB to SDRAM - TL0/1.1 + Via + TL1

6.6.4 Pre-RCD Clock

Clock - TL0/1.1 + TL1/1.1 + Via +TL2

6.6.5 Post-RCD Address/Command/Control/Clock

1st SDRAM from RCD - TL0/1.1 + Via + TL1

Last SDRAM from RCD = TL0/1.1 + Via + TL1 + Via + TL3 + Via + TL4 + Via +TL5 + Via + TL6

6.7 Rules for Registered and Load Reduced DIMM Designs

The DRAM package is a significant factor in the performance of RDIMMs and LRDIMMs. DRAM packages vary between manufacturers and between DRAM die within a single company. It is challenging to create a DIMM design that can accommodate all DRAM designs that will physically fit on the DIMM.

To increase the number of suppliers and DRAM packages that a single reference design letter can cover, some changes to the variation that may be applied for manufacturing is defined. A design letter e.g.,, "A“ and registration e.g., "1" as in "A1", is a single reference design. An individual manufacturer may modify the design including the trace lengths within the rules below.

Rules for allowed variation:

1. Placement configuration must match the reference design.
2. Physical placement may be changed. There is no specific limit.
3. All routing topologies must be maintained. The lengths may be adjusted as defined for signal groups.
4. Clock routing lengths may be adjusted as needed to maintain timing to the address Pre and Post RCD.
5. Control routing lengths may be changed as needed to maintain timing to the Clock Pre and Post RCD.
6. Address routing lengths between the SDRAMs may be adjusted by +/- 3 mm relative to the reference design.
7. Address routing lengths between the RCD and the first SDRAMs may be adjusted by +/- 10 mm.
8. Maximum skew for the address bus at the SDRAMs must be less than or equal to the reference design. It is suggested that the skew of the reference design be simulated with the same tool that is used for the final manufactured design so that simulator differences are minimized.

6.8 DQ Wiring to Support CRC

DDR5 has a CRC feature has been added to support higher speeds. Generally, when using CRC, the bit order is 1:1 between the source and the destination. This is not true for DIMMs where the bit order is somewhat random based on minimizing routing length to maximize signal integrity. The CRC computation is based on a byte. For x4 based SDRAMs the computation is truncated to 4 bits, a nibble. See a DDR5 SDRAM specification JESD79-5 for a more complete explanation of how CRC is implemented. To fix the mapping issue the host must understand the bit order at the SDRAM to map the DQ bits into the CRC generator for WRITE commands so that the SDRAM will decode the CRC correctly. The same is true for READs.

When there is more than one rank on a DIMM the even ranks are on the front and the odd ranks are on the back. When DRAMs are placed back to back and are of a different package rank the DQ relationship between the even ranks and the odd ranks are fixed. To reduce the number of variations in the DQ mapping a couple of rules are defined.

Rule 1: Bits within a nibble and strobe pair must stay together.

Rule 2: Nibbles may be swapped within a byte.

Rule 3: Definition of mapping is for rank 0 only. All even ranks have the same DQ mapping. Even rank to odd rank mapping is to swap bit 0 with 1, swap bit 2 with 3, swap bit 4 with 5 and swap bit 6 with 7.

For DIMMs that use 3DS components, the rank definition applies to package ranks. The additional die within a 3DS component are logical ranks and are part of one package rank. Another way of looking at this is that each Chipselect (CS_n) used is one package rank. Where there is only one package rank, that rank may be placed on the front or the back or split between the front or back.

Use of CRC is an optional feature. It is required that all reference designs support CRC. The definition for CRC can be found in the JESD79-5 specification for DDR5 SDRAMs.

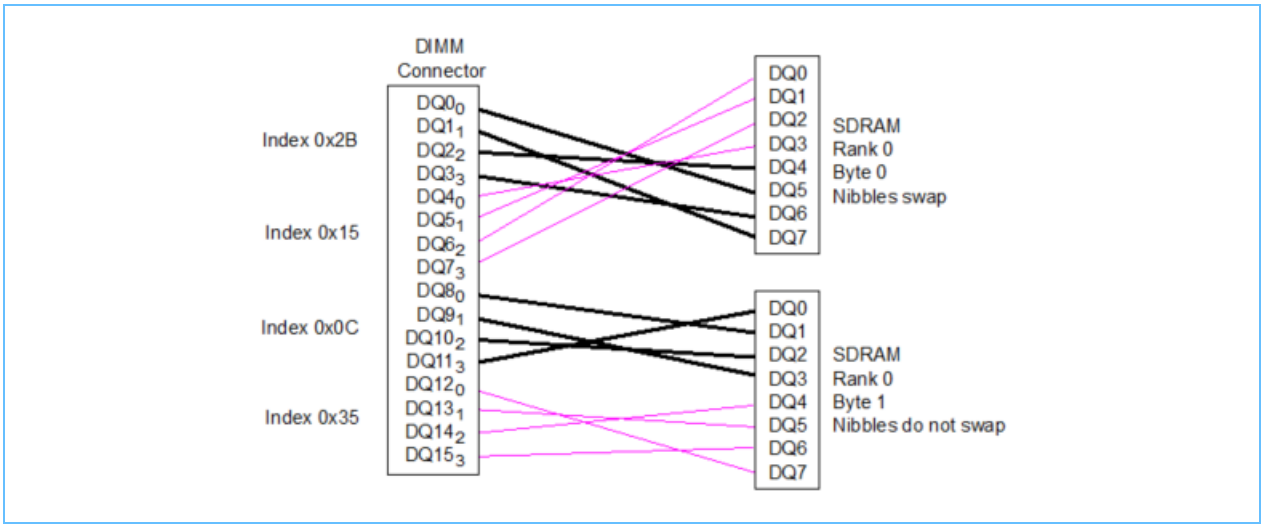

Figure 11 — Example of DQ Wiring

6.9 RDIMM and LRDIMM Configuration

6.9.1 DIMM Connectivity Wiring

2Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Top	Upper	QBCK	QBCS0	QBCA	0
Bottom	Lower	QCCK	QACS1	QACA	1
Bottom	Upper	QDCK	QBCS1	QBCA	1

2Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Top		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
Bottom	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

2Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Top	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]
Bottom		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

1Rx4					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QBCS0	QACA	0

1Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]

1Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

2Rx8					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QCCK	QACS1	QACA	1

2Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

2Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	
Bottom	[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]	

1Rx8					
DIMM Side	Row	Clock	CS	CA	Rank
Top	Lower	QACK	QACS0	QACA	0
Bottom	Lower	QACK	QACS0	QACA	0

1Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top			[15:8]				[31:24]			
Bottom	[7:0]				[23:16]				CB[7:0]	

1Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]				[23:16]					
Bottom			[15:8]				[31:24]		CB[7:0]	

6.9.2 Control Wiring

The figure defines the required control wiring for two row reference designs. The Design Specification Annex will include equivalent information in a clear manner for designs not covered in the following figure.

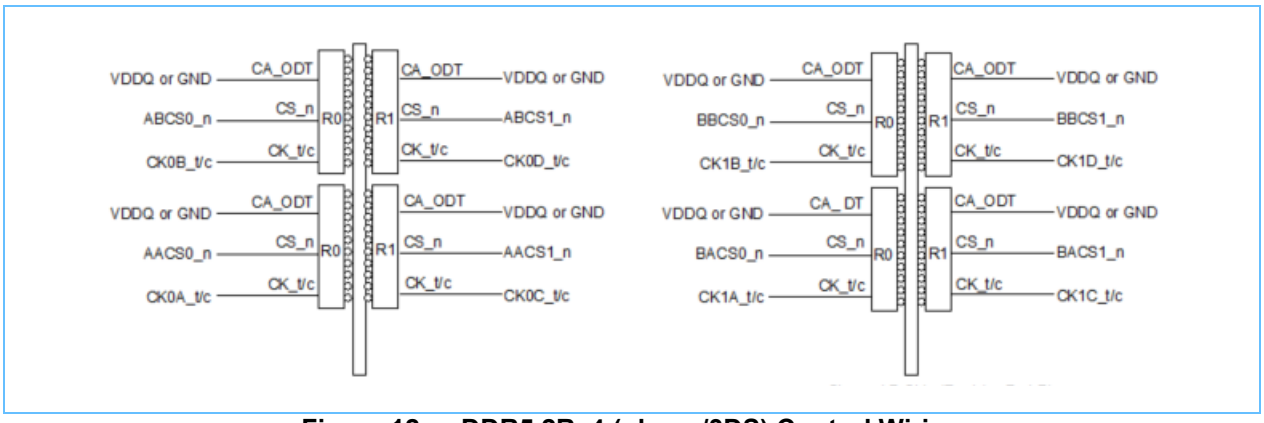

Figure 12 — DDR5 2Rx4 (planar/3DS) Control Wiring

6.9.3 ALERT_n Circuit Wiring

ALERT_n will be wired as a long fly-by connection with the RCD at one end. Connection will be from the ALERT_n pin of the RCD to the SDRAM ALERT_n pin of each in a daisychain manner for each channel. There will be a pull-up resistor to VDDQ at the end farthest SDRAM electrically from the register for each Channel. There will be a filter capacitor near the RCD pin for each channel. This circuit should be simulated to verify clean signal edges. Figure 12 demonstrates one possible wiring for this circuit.

The ALERT_n output of the RCD is connected to the ALERT_n pin of the edge pin connector.

Terminate with 47 Ω at end of daisychain of each Channel.

Place 10pF near RCD of each Channel

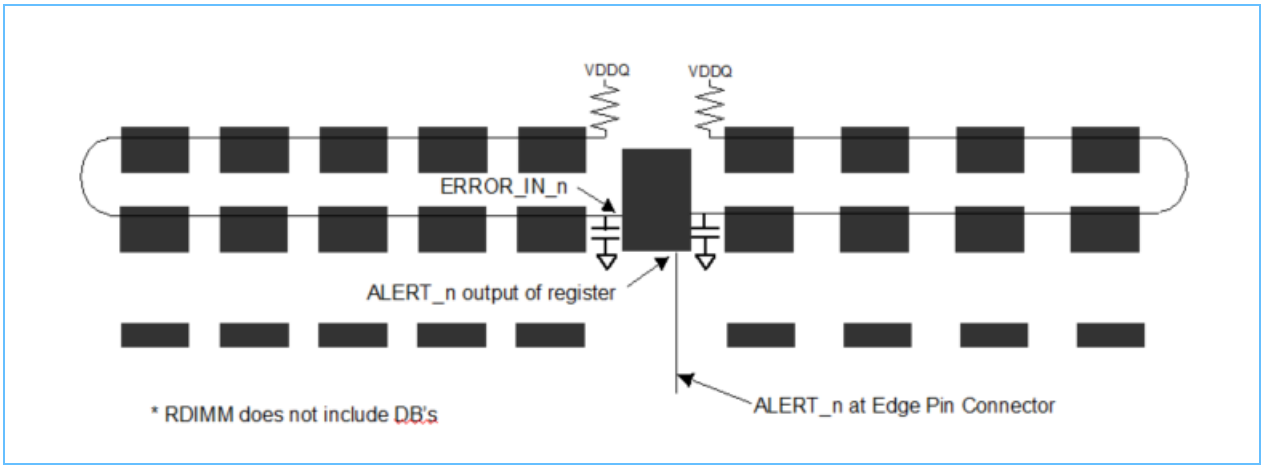

Figure 13 — Example Wiring of the ALERT_n Function - RDIMM and LRDIMM

6.9.4 RESET_n Circuit Wiring

RESET_n will be wired as a long fly-by connection with the RCD at one end for each SDRAM and DB channel. Connection will be from the RESET_n pin of the RCD to the SDRAM RESET_n pin of each in a daisychain manner for each SDRAM and DB channel. Figure 13 demonstrates one possible wiring for this circuit.

The RESET_n input pin of the RCD is connected to the RESET_n pin of the edge pin connector.

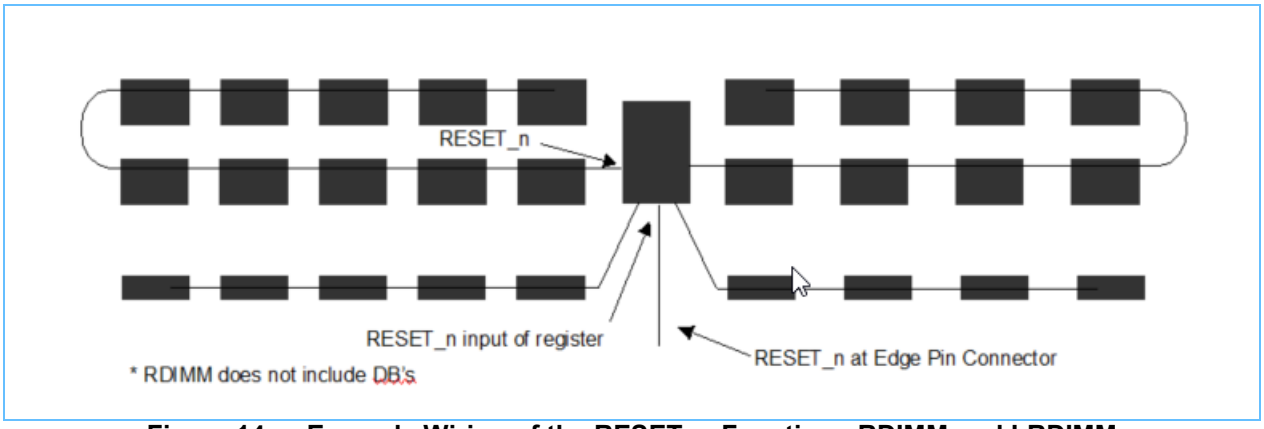

Figure 14 — Example Wiring of the RESET_n Function - RDIMM and LRDIMM

6.10 ZQ Calibration Wiring

DDR5 SDRAMs have a ZQ pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All DIMMs must connect a 240 Ω ± 1% resistor from this pin of each SDRAM to ground (VSS).

The DDR5RCD01 register has a ZQCAL pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All DIMMs must connect a 240 Ω ± 1% resistor from this pin of the register to ground (VSS).

The LRDIMM DDR5DB01 data buffer also has a ZQCAL pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All LRDIMMs must connect a 240 Ω ± 1% resistor from this pin of the DB to ground (VSS).

All components that have a ZQ pin must have its own ZQ resistor. Sharing is not allowed.

6.11 Sideband Bus Signal Wiring, Selection and Placement

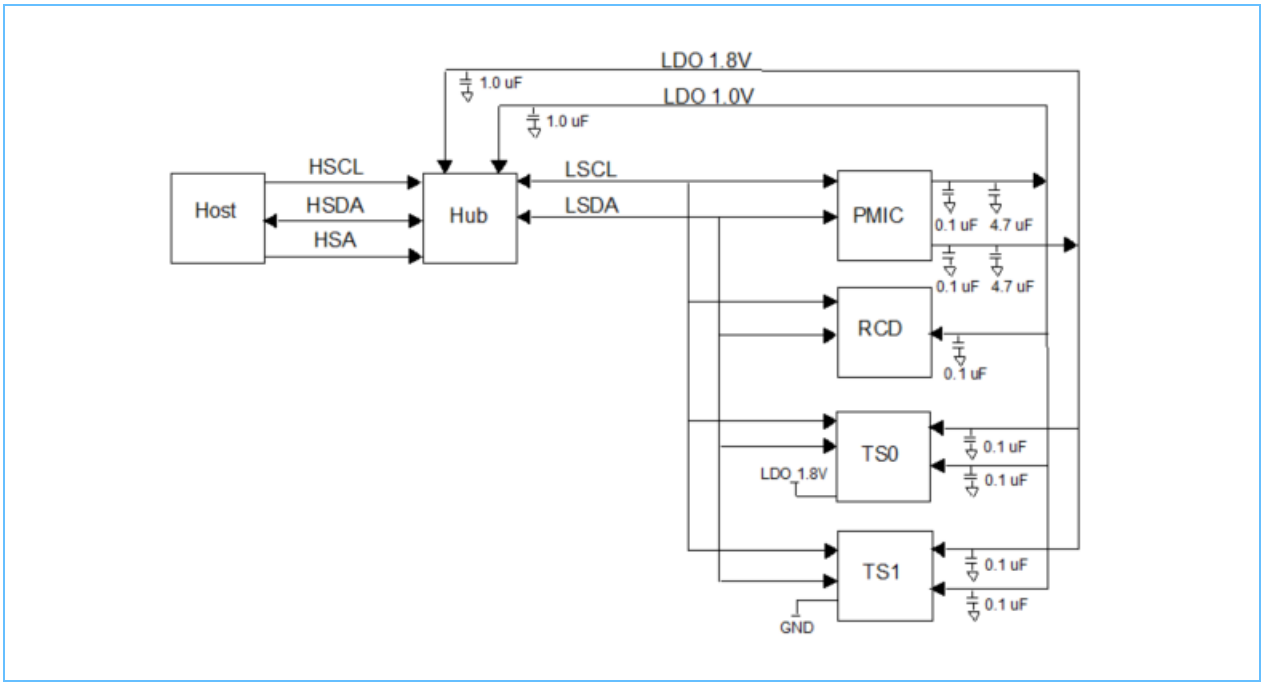

Figure 15 — Block Diagram: Hub, PMIC, RCD, TS0, TS1

Table 23 — SMBus Lengths

SMBus Signals	Gold Finger to Hub	<= 105 mm		
	Hub to PMIC	<= 10 mm		
	Hub to RCD	<= 25 mm		
	Hub to TS0	<= 80 mm	If possible, match these lengths to within a few mm.	
	Hub to TS1	<= 80 mm		

7 DIMM Impedance Profile

Applies to VDD, VDDQ and VPP voltage rails. Profile may differ for different DRAM devices (x4, x8, 3DS).

Frequency ranges f_1, f_2, f_3 are defined as: $f_1 \leq 2MHz$; $f_2 = 10MHz$; $f_3 = 20MHz$

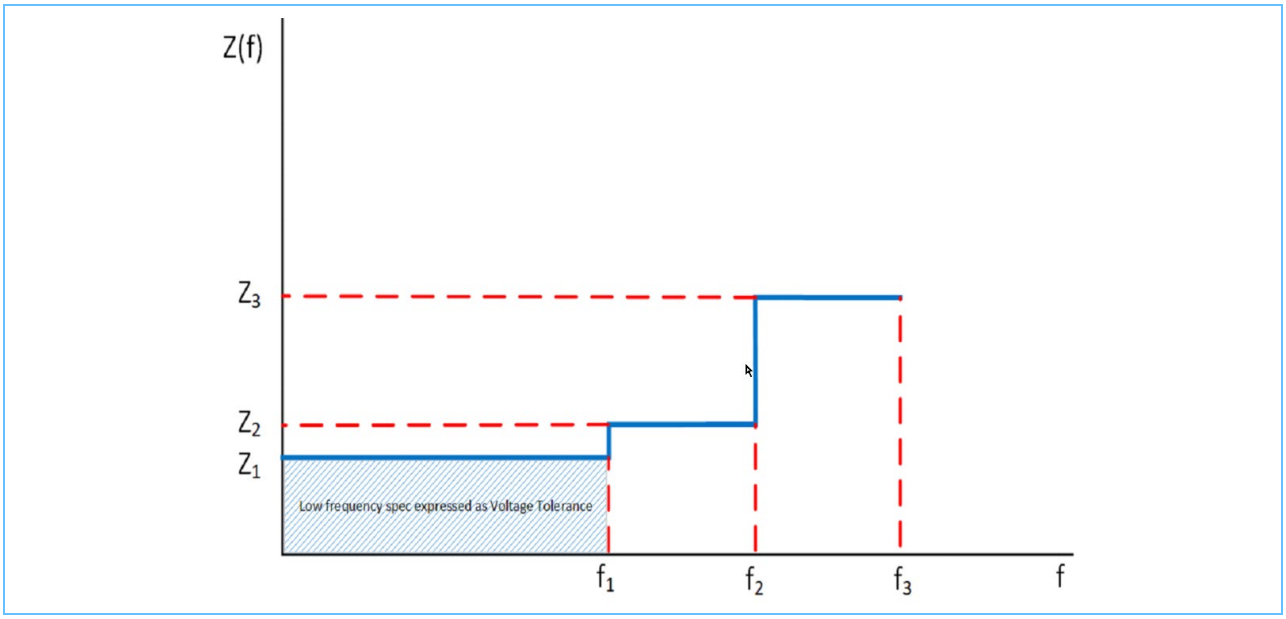

Figure 16 — Impedance Profile

Z(f) targets for each frequency range (Z_1, Z_2, Z_3).

Z_x is expressed as voltage tolerance based on DRAM input supply tolerances (-3%, +6%)

Table 24 — Example of Voltage Operating Conditions (for DRAM)

		Voltage Spec Freq: DC to 2 MHz				Z(f) Spec Freq: 2 to 10 MHz		Z(f) Spec Freq: 10 to 20 MHz		
DRAM	Symbol	Min (-3%)	Typ	Max (+6%)	Unit	Z_{max}	Unit	Z_{max}	Unit	Notes
Core Power	VPP	1.746	1.8	1.908	V	100	mOhm	170	mOhm	3,4,5
Supply voltage	VDDQ	1.067)	1.1	1.166	V	40	mOhm	80	mOhm	1,2,3,4,5
Supply Voltage	VDD	1.067	1.1	1.166	V	30	mOhm	50	mOhm	1,2,3,4,5

NOTE 1 VDDQ must be less than or equal to VDD. VDD must be within 66mV of VDDQ.
NOTE 2 AC parameters are measured separately on VDD and VDDQ.
NOTE 3 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations.
NOTE 4 Z(f) is per voltage domain per DRAM device. Per DRAM BGA pin is not required.
NOTE 5 Z(f) does not include the DRAM package and silicon die.
NOTE 6 DIMM vendors to verify the impedance with models reflecting the BOM.

The Annex Specification will contain the specific conditions as determined by each design sponsor.

8 Reference Stackup

This is an example. Each Raw Card Annex will contain a specific example reflective of the reference design stackup.

Table 25 — Example (12 layer) LRDIMM Stackup

Layer	Signal Description	Single-Ended Impedance		Copper (oz)	Dielectric Thickness (um)
		Trace Width (um)	Impedance (Ω)		
1	Addr / Ctrl	100	50	3/8 + Plating	
	DQ	200	35		
	Dielectric				75
2	Plane			1/2	
	Dielectric				70
3	Addr / Ctrl	75	50	1/2	
	Clock	200	25		
	Dielectric				115
4	Plane			1/2	
	Dielectric				70
5	Addr / Ctrl	75	50	1/2	
	DQ	125	35		
	Dielectric				115
6	Plane			1/2	
	Dielectric				122
7	Plane			1/2	
	Dielectric				115
8	Addr / Ctrl	75	50	1/2	
	DQ / Strobe	125	35		
	Clock	225	25		
	Dielectric				70
9	Plane			1/2	
	Dielectric				115
10	Addr / Ctrl	75	50	1/2	
	Clock	200	25		
	Dielectric				70
11	Plane			1/2	
	Dielectric				75
12	Addr / Ctrl	100	50	3/8 + Plating	
	DQ	200	35		

Table22 — Example (10-layer) RDIMM Stackup

Layer	Signal Description	Single-Ended Impedance		Copper (oz)	Dielectric Thickness (um)
		Trace Width (um)	Impedance (Ω)		
1	Addr / Ctrl	93	50	3/8 + Plating	
	DQ	190	35		
	Clock	270	25		
	Misc	93	50		
	Dielectric				75
2	Plane			1/2	
	Dielectric				70
3	Addr / Ctrl	74	50	1/2	
	DQ	145	35		
	Clock	248	25		
	Dielectric				115
4	Plane			1/2	
	Dielectric				70
5	Addr / Ctrl	63	50	1/2	
	DQ	136	35		
	Dielectric				115
6	Plane / Misc	63	50	1/2	
	Dielectric				122
7	Plane			1/2	
	Dielectric				115
8	Addr / Ctrl	74	50	1/2	
	DQ	145	35		
	Clock	248	25		
	Dielectric				70
9	Plane			1/2	
	Dielectric				115
10	Addr / Ctrl	93	50	3/8 + Plating	
	DQ	190	35		
	Misc	93	50		

9 Manufactured DIMMs

The Annex Specification documents a reference design that is intended to provide a solution that meets a set of specific requirements. There will always be improvements that can be made.

To allow manufactured DIMMs to be improved over the reference design or to accommodate other DRAM packages, minor changes to the trace lengths as defined in the length tables of a specific annex is allowed as long as the skew is equal to or reduced relative to the reference design. It is a requirement that improvements are not made that move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. To restrict the degree of change so that basic timing is maintained, the identified net for each table must meet the trace lengths defined for that table.

To improve on a reference design, the manufacturer must establish a baseline for the reference design. Any improvements to the baseline must have reduced skew relative to the baseline. The baseline may have different skew values compared to the Annex. The simulation environment and tools are the likely source of differences between the baseline and the Annex. Significant differences should be brought to the attention of the reference design sponsor or JEDEC in general.

10 Serial Presence Detect Definition and Content

This section is included for convenience. Refer to the DDR5 SPD Contents Master Specification (e.g., JESD400-5) for specific Addressing and Block information.

11 Product Label

Please refer to the JESD401-5 for the most up to date Label specification.

12 JEDEC Process

JEDEC provides PCB reference designs for DIMMs. The designs are divided into families. Registered and Load Reduced DIMMs are two of those. Letters (A, B, C etc.) are used to define specific configurations (raw cards) of DIMM such as 2 rank with x4 based SDRAMs. Additional characteristics may further refine cards into specific raw card (R/C) letters. Letter assignments are arbitrary and usually chronological. There is no other association to the letter assignments.

R/Cs are reviewed and balloted by JEDEC members of Task Group 451_1 before being placed on the JEDEC website as a reference design. This is called a “Registration”. The initial registration is 0. A specific card may be the registration of R/C A0 as example. Subsequent design updates to the reference design go through the same balloting process and increment the registration number from 0 to 1 or the next highest number.

This page intentionally left blank.

Standard Improvement Form JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC®