JEDEC STANDARD

DDR5 Clocked Unbuffered Dual Inline Memory Module with 4-bit ECC (EC4 CUDIMM) Raw Card D Annex

JESD323-B4-RCD

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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(From JEDEC Board Ballot number JCB-24-41, formulated under the cognizance of the JC-45.3 Subcommittee on Unbuffered DRAM Modules, item 2295.03).

1 Scope

This standard, JESD323-B4-RCD, "DDR5 Clocked Unbuffered Dual Inline Memory Module with 4-bit ECC (EC4 CUDIMM) Raw Card D Annex" defines the design detail of x8, 1 Package Rank DDR5 ECC CUDIMM with Clock Driver. The common feature of DDR5 CUDIMM such as the connector pinout can be found in the JESD323, DDR5 Clocked Unbuffered Dual Inline Memory Module (CUDIMM) Common Specification.

2 DDR5 CUDIMM Design File

Table 1 — DDR5 CUDIMM Design File

Raw card	Applicable Design File	Applicable BOM
D0	PC5-CUDIMM_RC_D0_R100_20240929.brd	PC5-CUDIMM_RC_D0_ R100_20240929_BOM.xlsx
NOTE 1	“Reference” design file updates will be released as needed. This DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only. In these cases the design files will not be updated.	

3 Module Configuration

Table 2 — Module Configuration

SDRAM			DIMM					
Die Density	Organization	Pkg Type	Maximum Capacity	Organization	# of SRDAM Die on DIMM	# of Package Ranks	# of Address signals Row / Col	MO-329 Variation
16Gb	2G x 8	SDP	16GB	2G x 72	10	1	16 / 10	ABxB
24Gb	3G x 8	SDP	24GB	3G x 72	10	1	17 / 10	ABxB
32Gb	4G x8	SDP	32GB	4G x 72	10	1	17 / 10	ABxB

4 SDRAM Configuration

Table 3 — SDRAM Configuration

Raw Card	Supported DRAM Outline (Width x Length) max.(mm)	# of Bank groups/ Banks in a group	SDRAM Package Type	Package Type	MO-210 Variation
D0	10.1 x 11.8	8/4	82 Ball FBGA	SDP	AN

NOTE 1 SDP is a single die per package.
NOTE 2 MO-210 variation AL is 78-ball FBGA is also acceptable for placement.

5 Supported Speeds

Table 4 — Supported Speeds

Raw Card	Speed	PC5-4400	PC5-4800	PC5-5600	PC5-6400	PC5-7200	PC5-8000	PC5-8800	Notes
D0	DDR5	Y	Y	Y	Y				1,2

NOTE 1 X reflects speed grades approved from previous ballots
NOTE 2 Y denotes speed grades newly supported

6 Design Deviations

1. None.

7 General Layout

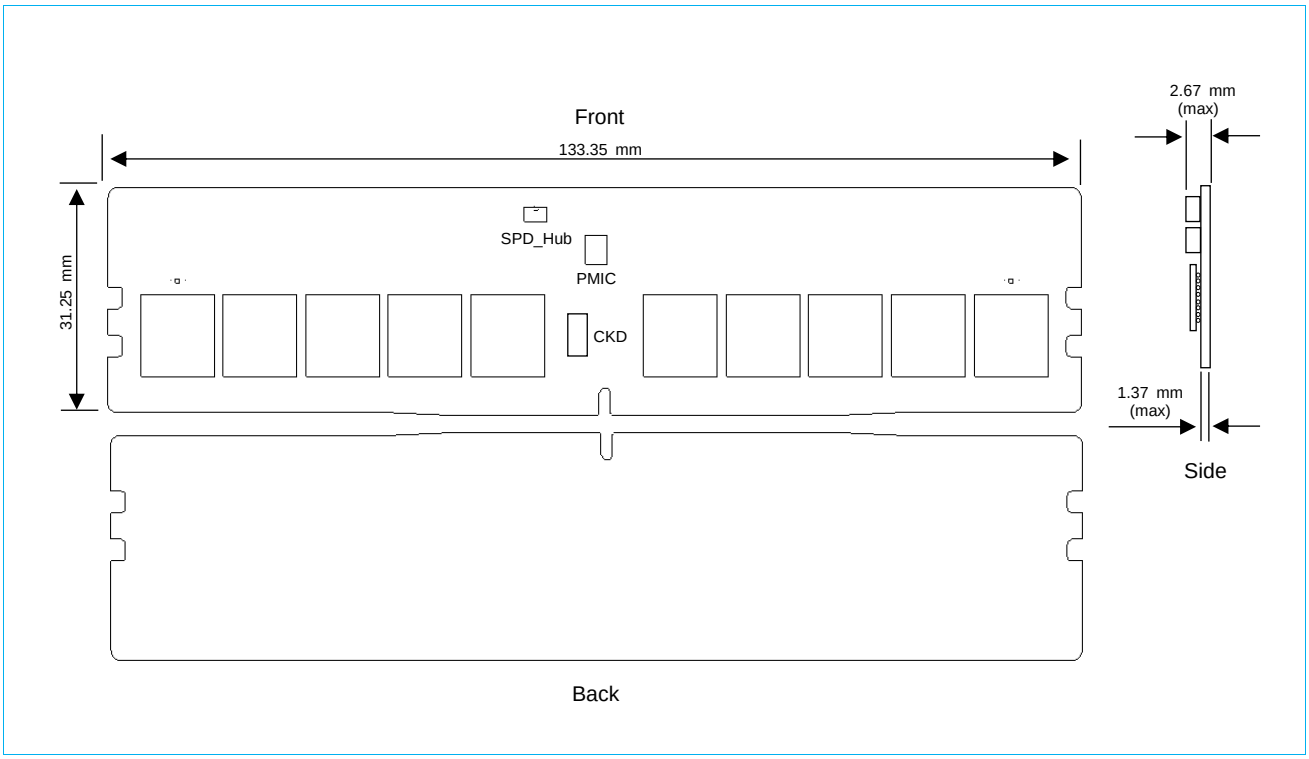


Figure 1 — General Layout

8 Functional Block Diagram

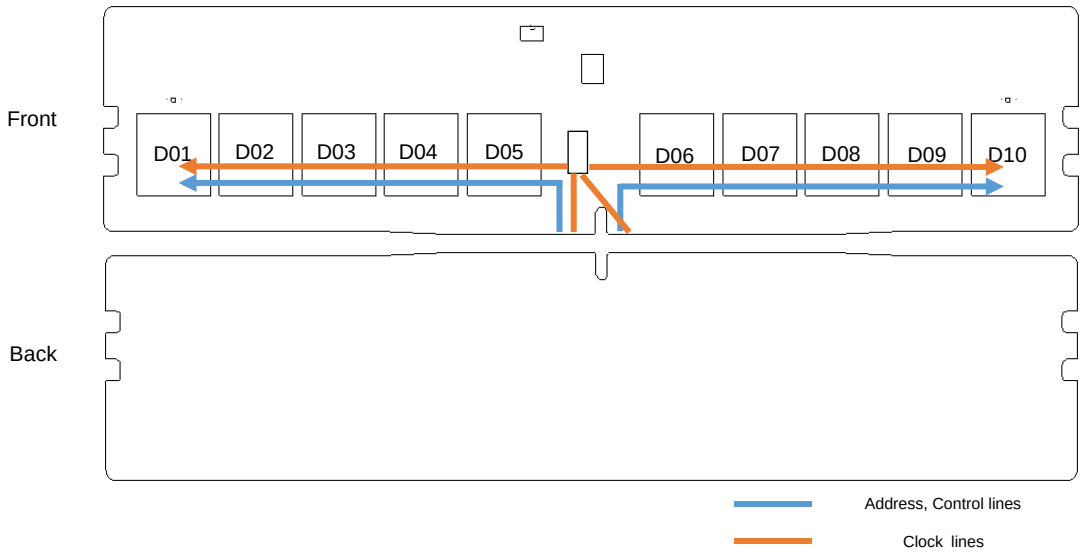


Figure 2 — X72 DIMM, Populated as One Package Ranks of x8 DDR5 SDRAMs (Part 1 of 3)

8 Functional Block Diagram (cont'd)

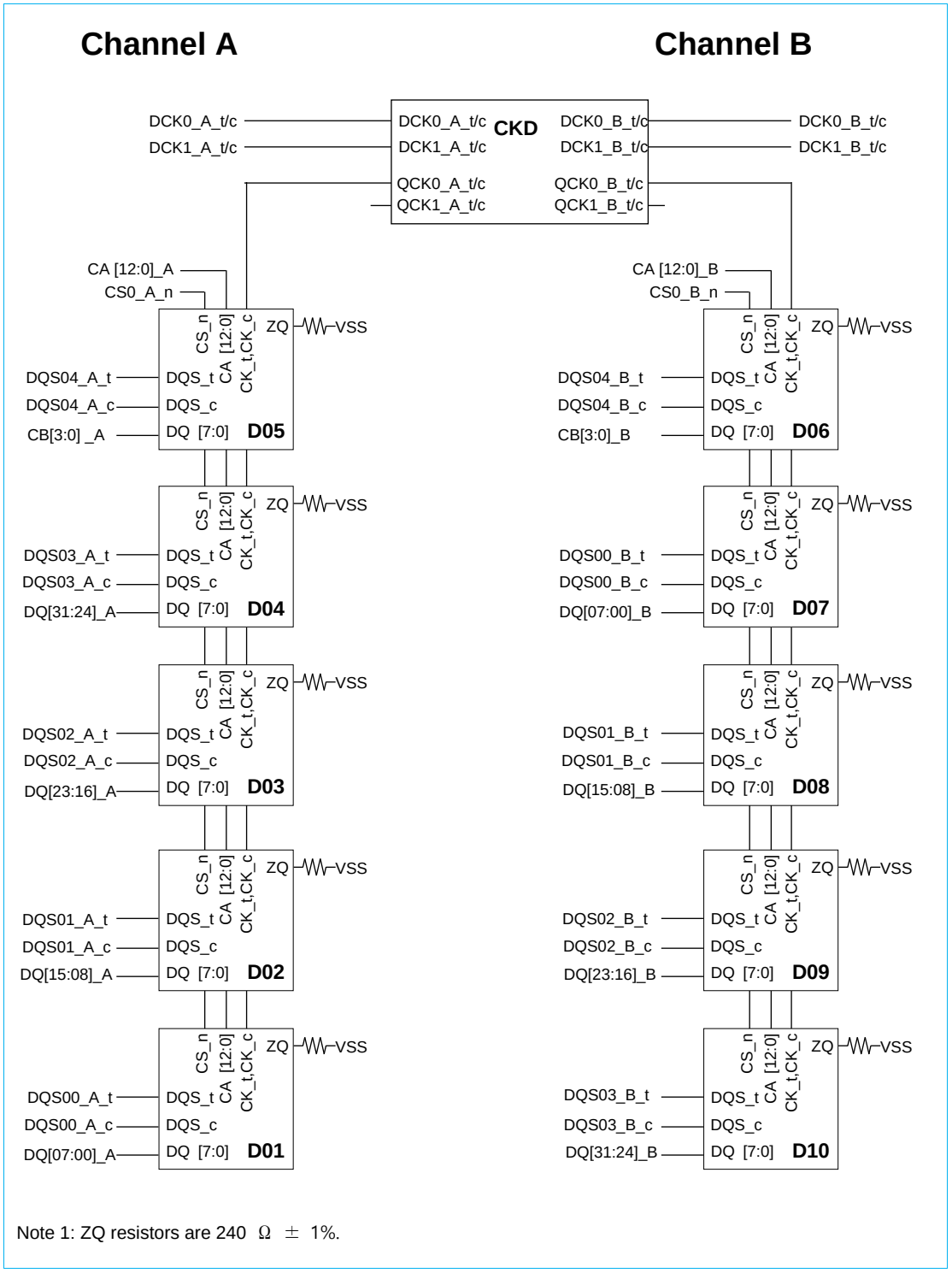


Figure 3 — X72 DIMM, Populated As One Package Ranks of x8 DDR5 SDRAMs (Part 2 of 3)

8 Functional Block Diagram (cont'd)

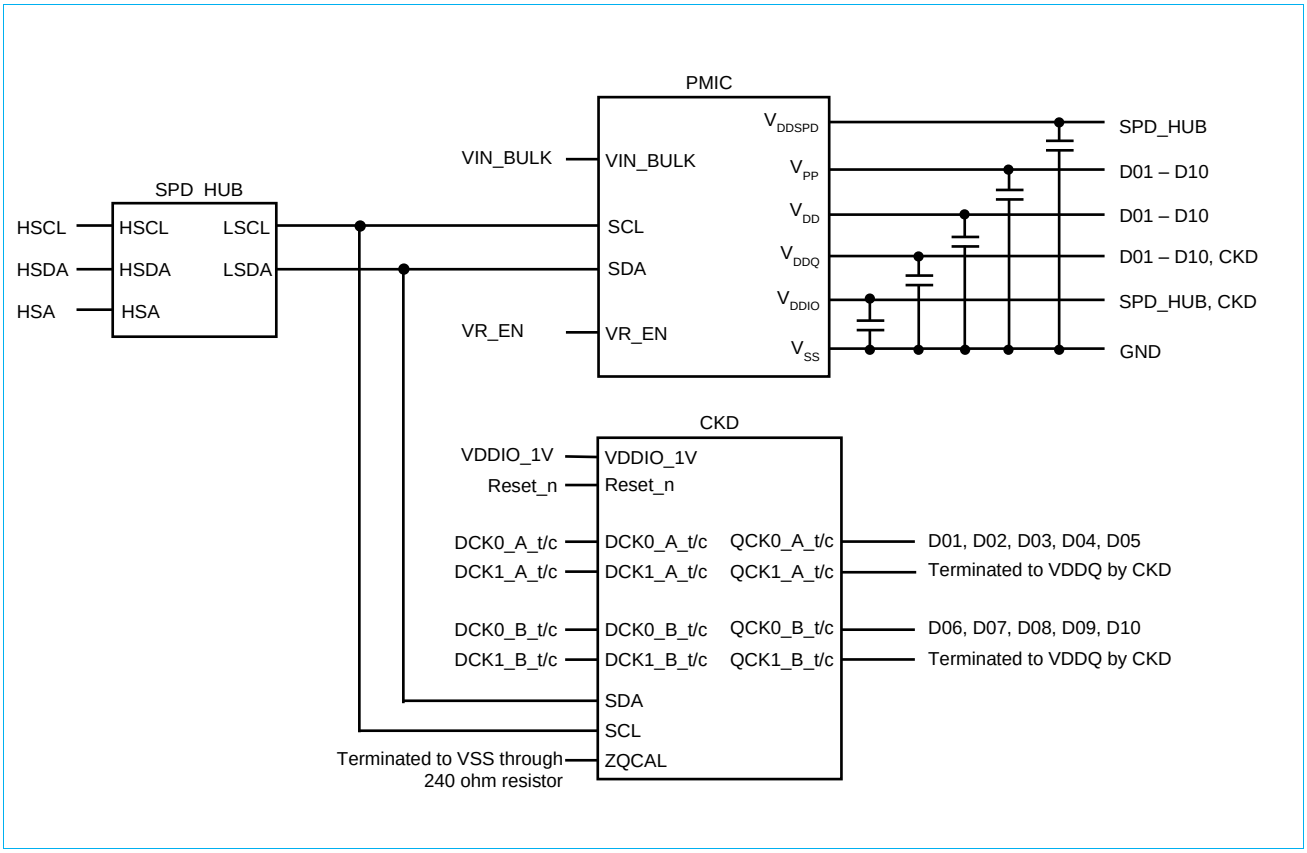


Figure 4 — X72 DIMM, Populated as One Package Ranks of x8 DDR5 SDRAMs (Part 3 of 3)

9 Sideband Bus Routing

Table 5 — Trace Lengths for Host and Local Signals

Raw Card	Signal	Total Etch Length (mm)
D0	HSCL (Gold Finger to Hub)	82.8
	HSDA (Gold Finger to Hub)	82.7
	HSA (Gold Finger to Hub)	89.3
	LSCL (Hub to PMIC)	20.27
	LSDA (Hub to PMIC)	21.98
	LSCL (Hub to CKD)	21.70
	LSDA (Hub to CKD)	23.74

NOTE 1 No via travel or compensation included

10 Pre Clock Net Structure

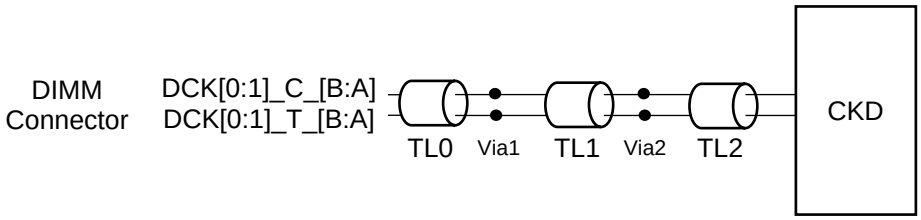


Figure 5 — Net Structure Routing for Clock to CKD – DCK[1:0]_[B:A]_t/c

Table 6 — Trace Lengths for Clock Net Structures

Raw Card	Signal	TL0 (MS)	Via1	TL1 (SL)	Via2	TL2 (MS)	Compensated Length CKD
D0	DCK0_A_t, DCK0_A_c	2.22	0.14	8.14	0.14	0.51	10.9
	DCK0_B_t, DCK0_B_c	2.65 2.92	0.14	7.76 7.51	0.14	0.51	10.9
	DCK1_A_t, DCK1_A_c	2.22	0.14	12.14	1.04	0.51	15.8
	DCK1_B_t, DCK1_B_c	2.28	0.14	12.08	1.04	0.51	15.8

NOTE 1 All distances are given in (mm). Refer to DDR5 Clocked Unbuffered Dual Inline Memory Module (CUDIMM) Common Specification (JESD324) for length matching rule.
NOTE 2 The segment lengths are not required to be met.
NOTE 3 _t/c segment lengths of differential pair to be within +/- 0.1 mm
NOTE 4 Microstrip sections are converted to equivalent Stripline by dividing by 1.1 for compensation.
NOTE 5 Via travel is compensated as 1 time the z-axis length of the traveled path less outer layer Cu thickness.
NOTE 6 All distances can be adjusted as necessary to align clock with Address.
NOTE 7 Compensated Length to CKD = TL0/1.1 + Via1 + TL1 + Via2 + TL2/1.1

11 Post Clock Net Structure

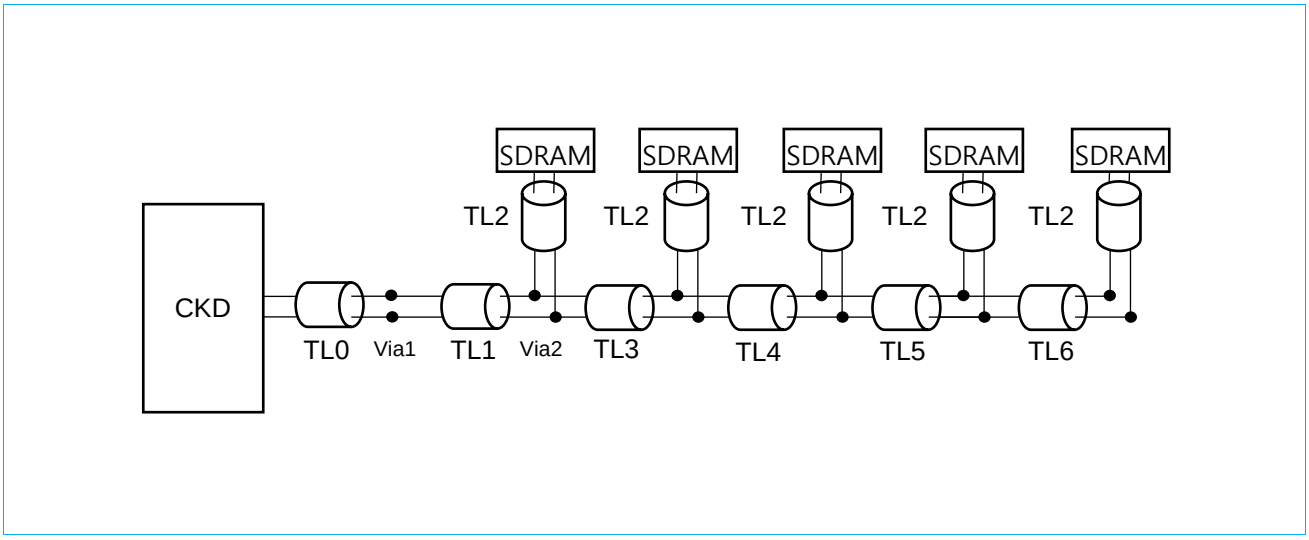


Figure 6 — Net Structure Routing for Clock to SDRAM Loads - QCK0_[B:A]_t/c

Table 7 — Trace Lengths for Clock Net Structures

Raw Card	Signal	TL0 (MS)	Via1	TL1 (SL)	Via2	TL2 (MS)	Comp 1st DRAM	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	Comp 5th DRAM
D0	QCK0_A_t, QCK0_A_c	0.54	0.63	12.88	0.63	0.57	15.14	13.6	13.6	16.6	14.6	73.55
	QCK0_B_t, QCK0_B_c	0.54	0.63	12.88	0.63	0.57	15.14	13.6	13.6	16.6	14.6	73.55

NOTE 1 All distances are given in (mm). Refer to DDR5 Clocked Unbuffered Dual Inline Memory Module (CUDIMM) Common Specification (JESD324) for length matching rule.
NOTE 2 The segment lengths are not required to be met.
NOTE 3 _t/c segment lengths of differential pair to be within +/- 0.1 mm
NOTE 4 Microstrip sections are converted to equivalent Stripline by dividing by 1.1 for compensation.
NOTE 5 Via travel is compensated as 1 time the z-axis length of the traveled path less outer layer Cu thickness.
NOTE 6 All distances can be adjusted as necessary to align clock with Address.
NOTE 7 Compensated Length 1st SDRAM = TL0/1.1 + Via1 + TL1 + Via2 + TL2/1.1
NOTE 8 Compensated Length 5th SDRAM = TL0/1.1 + Via1 + TL1 + Via2 + TL3 + TL4 + TL5 + TL6 + TL2/1.1

12 Data Net Structure – DQ, CB, DQS_t, DQS_c

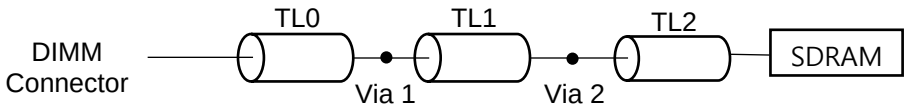


Figure 7 — Net Structure Routing for DQ, CB, DQS_t, DQS_c

Table 8 — R/C D0 – Trace Lengths for DQ[31:00]_A, CB[03:00]_A, DQS[04:00]_t_A, DQS[04:00]_c_A
Trace Lengths for DQ[31:00]_B, CB[03:00]_B, DQS[04:00]_t_B, DQS[04:00]_c_B

DQ strobes	TL0 (MS)		Via 1	TL1 (SL)		Via 2	TL2 (MS)		Compensated Length To DRAM
	Min	Max		Min	Max		Min	Max	
DQ[07:00]_A	2.08	2.08	0.14	12.45.	13.35	0.14 / 1.04	0.57	0.57	16.03
DQS00_t_A, DQS00_c_A	2.91	2.91	0.14	8.08	8.08	0.14	0.57	0.57	11.52
DQ[15:08]_A	2.08	2.08	0.14	9.75	10.65	0.14 / 1.04	0.57	0.57	13.33
DQS01_t_A, DQS01_c_A	2.91	2.91	0.14	6.18	6.18	1.04	0.57	0.57	10.52
DQ[23:16]_A	2.08	2.08	0.14	9.45	10.35	0.14 / 1.04	0.57	0.57	13.03
DQS02_t_A, DQS02_c_A	2.91	2.91	0.14	5.88	5.88	0.14	0.57	0.57	9.32
DQ[31:24]_A	2.08	2.08	0.14	10.75	11.65	0.14 / 1.04	0.57	0.57	14.33
DQS03_t_A, DQS03_c_A	2.91	2.91	0.14	6.48	6.48	1.04	0.57	0.57	10.82
CB[03:00]_A	2.08	2.08	0.55 / 0.63	12.09	12.17	0.63	0.57	0.57	15.75
DQS04_t_A, DQS04_c_A	2.91	2.91	0.63	8.93	8.93	0.63	0.57	0.57	13.34
DQ[07:00]_B	2.08	2.08	0.14	15.65	16.54	0.14 / 1.04	0.57	0.57	19.23
DQS00_t_B, DQS00_c_B	2.91	2.91	0.14	11.18	11.18	0.14	0.57	0.57	14.62
DQ[15:08]_B	2.08	2.08	0.14	11.95	12.85	0.14 / 1.04	0.57	0.57	15.53
DQS01_t_B, DQS01_c_B	2.91	2.91	0.14	8.98	8.98	1.04	0.57	0.57	13.32
DQ[23:16]_B	2.08	2.08	0.14	10.75	11.65	0.14 / 1.04	0.57	0.57	14.33
DQS02_t_B, DQS02_c_B	2.91	2.91	0.14	6.38	6.38	0.14	0.57	0.57	9.82
DQ[31:24]_B	2.08	2.08	0.14	9.45	10.35	0.14 / 1.04	0.57	0.57	13.03
DQS03_t_B, DQS03_c_B	2.91	2.91	0.14	5.88	5.88	1.04	0.57	0.57	10.22
CB[03:00]_B	2.08	2.08	0.55 / 0.63	16.69	16.77	0.63	0.57	0.57	20.35
DQS04_t_B, DQS04_c_B	2.91	2.91	0.55	13.98	13.98	0.63	0.57	0.57	18.32

NOTE 1 All distances are in (mm). Compensated length to be within a tolerance of ± 1.0 mm except pin pitch and pad size discrepancy.

NOTE 2 Segment lengths not required to be met. Compensated Length = TL0/1.1 + Via 1+ TL1 + Via 2 + TL2/1.1

13 Address and Command Net Structure Routing

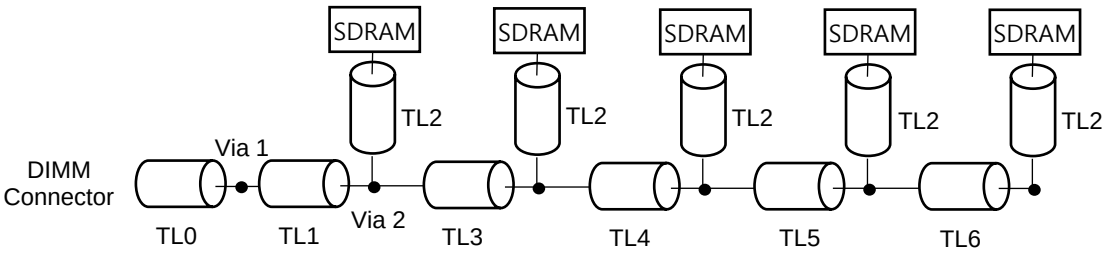


Figure 8 — Net Structure Routing for CA[12:00]_[B:A]

Table 9 — Trace Lengths for Address and Command Net Structures

Raw Card	Signal	TL0 (MS)	Via1	TL1 (SL)	Via2	TL2 (MS)	Comp 1st DRAM	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	Comp 5th DRAM
D0	CA00_A	2.08	1.04	25.52	1.04	0.57	30	13	13	13	13	82
	CA00_B	2.08	1.04	25.52	1.04	0.57	30	13	13	13	13	82

NOTE 1 All distances are given in (mm). Refer to DDR5 Clocked Unbuffered Dual Inline Memory Module (CUDIMM) Common Specification (JESD324) for length matching rule.

NOTE 2 Compensation 1st DRAM = TL0/1.1 + Via1 +TL1 + Via2 + TL2/1.1

NOTE 3 Compensation 5th DRAM = TL0/1.1 + Via1 +TL1 + TL3 + TL4 + TL5 + TL6 + Via2 +TL2/1.1

NOTE 4 All distances can be adjusted within these rules.
- Address routing lengths between the DRAMs (TL3, TL4, TL5, TL6) may be adjusted by +/- 3.0 mm relative to the reference design.
- The segment between the via and the DRAM ball (TL2) may also be changed as needed

14 Control Net Structure Routing

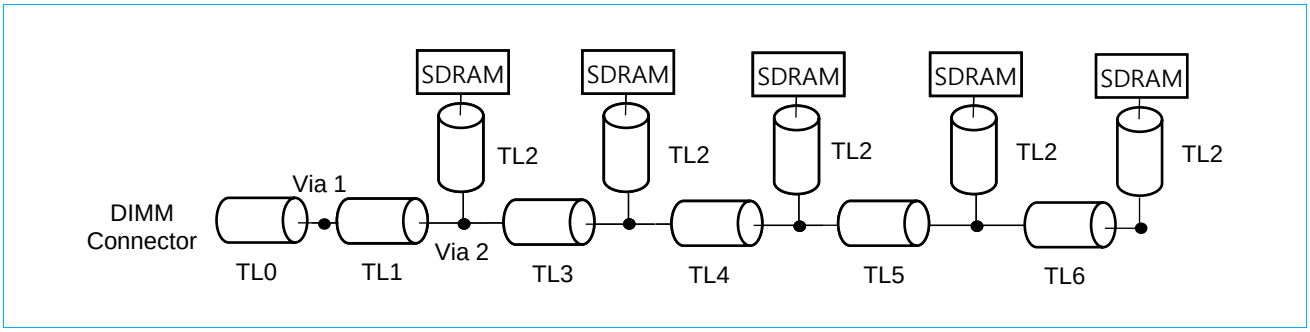


Figure 9 — Net Structure Routing for CS00_[B:A]

Table 10 — Trace Lengths for Control Net Structures

Raw Card	Signal	TL0 (MS)	Via1	TL1 (SL)	Via2	TL2 (MS)	Comp 1st DRAM	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	Comp 5th DRAM
D0	CS00_N (Ch. A)	2.08	1.04	25.52	1.04	0.57	30	13	13	13	13	82
	CS00_N (Ch. B)	2.08	0.14	27.32	0.14	0.57	30	13	13	13	13	82

NOTE 1 All distances are given in (mm). Refer to DDR5 Clocked Unbuffered Dual Inline Memory Module (CUDIMM) Common Specification (JESD324) for length matching rule.

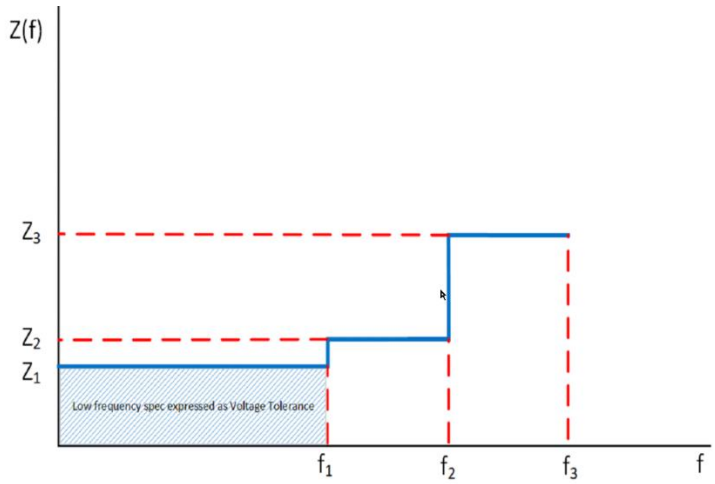
NOTE 2 Control routing length may be adjusted as needed to maintain timing to the clock

NOTE 3 Compensation 1st DRAM = TL0/1.1 + Via1 +TL1 + Via2 + TL2/1.1

NOTE 4 Compensation 5th DRAM = TL0/1.1 + Via1 +TL1 + TL3 + TL4 + TL5 + TL6 + Via2 + TL2/1.1

15 DIMM Impedance Profile

Applies to VDD, VDDQ, and VPP voltage rails for this raw card.
Frequency ranges f1, f2, f3 are defined as: f1 ≤ 2 MHZ; f2 = 10 MHz; f3 = 20 MHz



NOTE 1 Z(f) targets for each frequency range (Z_1, Z_2, Z_3).
NOTE 2 Z_x is expressed as voltage tolerance based on DRAM input supply tolerances (-3%, +6%)

Figure 10 — DIMM Impedance Profile

Table 11 — Voltage Operating Conditions

		Voltage Spec Freq: DC to 2 MHz				Z(f) Spec Freq: 2 to 10 MHz		Z(f) Spec Freq: 10 to 20 MHz		
DRAM	**Symbol**	**Min (-3%)**	**Typ**	**Max (+6%)**	**Unit**	**z_{max}**	**Unit**	**z_{max}**	**Unit**	**Notes**
Core Power	VPP	1.746	1.8	1.908	V	9.9	mOhm	18.4	mOhm	
Supply voltage	VDDQ	1.067	1.1	1.166	V	7.9	mOhm	14.9	mOhm	
	VDD	1.067	1.1	1.166	V	5.2	mOhm	9.4	mOhm	

NOTE 1 VDDQ must be less than or equal to VDD. VDD must be within 66 mV of VDDQ.
NOTE 2 AC parameters are measured separately on VDD and VDDQ.
NOTE 3 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations.
NOTE 4 Z(f) is per voltage domain per DRAM device. Per DRAM BGA pin is not required.
NOTE 5 Z(f) does not include the DRAM package and silicon die.

16 ALERT_n and RESET_n Net Structure Routing

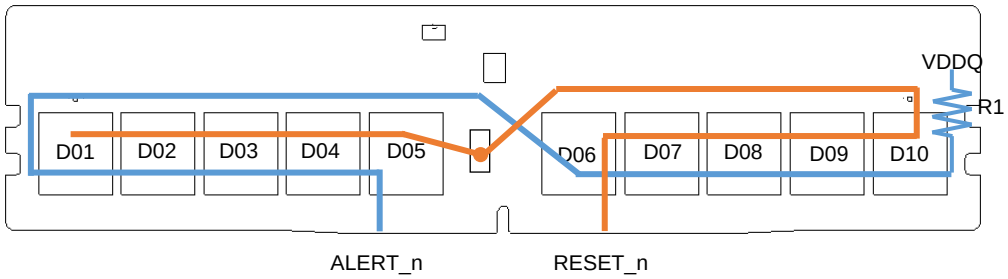


Figure 11 — Net Structure Routing for ALERT_n and RESET_n

Table 12 — Trace Lengths for ALERT_n and RESET_n

Raw Card	Signal	Total Etch Length (mm)	R1 (Ω)
D0	ALERT_n	216.8 (include stubs)	47±5%
	RESET_n	214.6(include stubs)	-

NOTE 1 All distances are given in mm. Length matching is not required but topology must be maintained.
NOTE 2 The values of R1 may be changed by DIMM manufacturer.

17 Electrically Induced Physical Damage (EIPD) Protection

Protection is provided to the Vin_bulk rail with a discrete Transient Voltage Suppressor TVS.

The Vin_bulk TVS will be an 0402 (1006 metric) footprint in artwork. The TVS for this raw card is placed near the PMIC. The DIMM supplier selects if the TVS is to be uni-directional or bi-directional. The TVS electrical characteristics to be VRWM minimum of 5.5 V and VRWM nominal of 6 V. Other characteristics to be determined by the DIMM supplier.

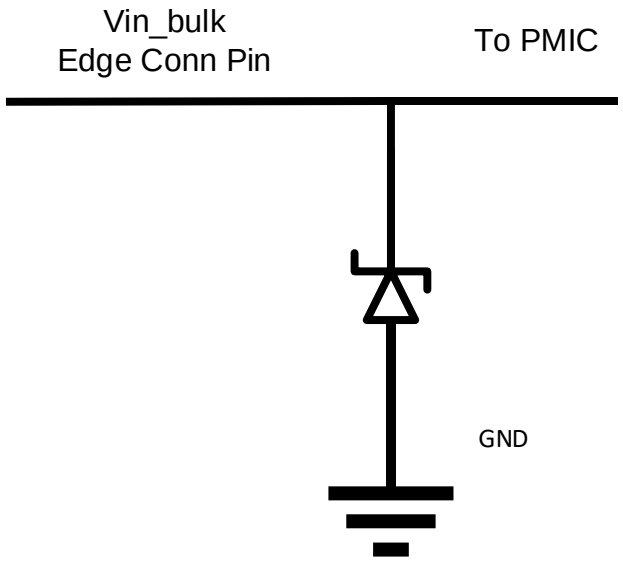


Figure 12 — Electrically Induced Physical Damage (EIPD) Protection

See Raw Card D0 registration for placement.

18 DIMM PMIC Configuration

This section defines operating mode, component type and/or values for DIMM VR.

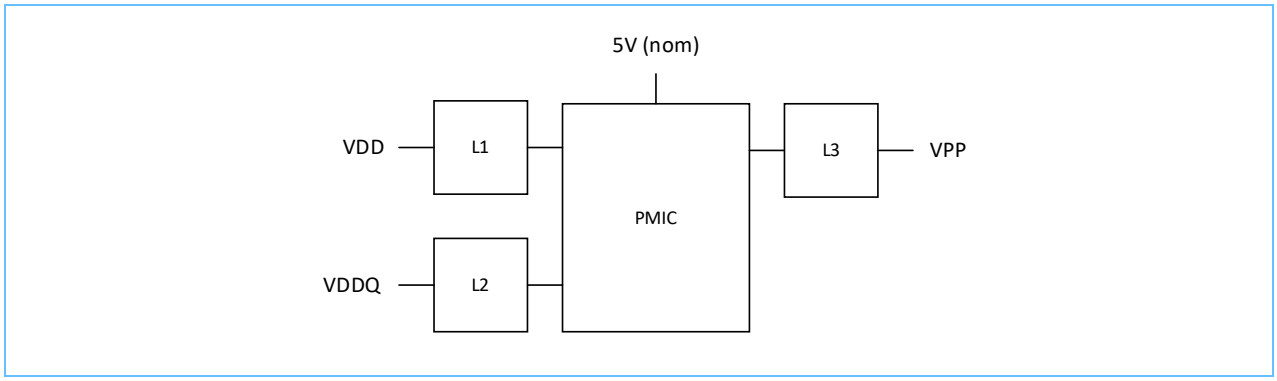


Figure 13 — DIMM PMIC Configuration

Table 13 — RC-D0 VR Settings

PMIC Type	Operation Mode	L1 (VDD)	L2 (VDDQ)	L3 (VPP)	Notes
P5100 Single Phase	Inductor (µH)	0.68 0.47	0.68 0.47	1.0 1.5	
	SWF (kHz)	750 1000 1250	750 1000 1250	750 1000 1250	

NOTE 1 Number of PMIC output capacitor can be determined by DIMM vendors.
NOTE 2 DIMM vendors may optimize SWF and inductor to optimize product.

DIMM PMIC Power Up and Power Down Sequencing and Soft Stop Time

Refer to JESD323 for requirements.

19 Function Control Word Programming

The Register is configured through Register Control Words (RCW).

Some of the Control Words are module PCB design specific and must be programmed the same way for all systems. These are the Control Words that are defined in Table 14.

Table 14 — RC D0 – SPD Programming

SPD Byte	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
229	0	0	0	0	0	0	1	0	02	VIN_Bulk – TVS
230	0	0	0	1	0	0	0	1	11	Module Nominal Height (31.25)
231[1]	0	0	0	0	0	0	0	1	01	Module Thickness (Front 1~2 mm / Back < 1 mm)
232	0	0	0	0	0	0	1	1	03	Reference Raw Card Used – D0
233[1]	1	0	0	0	0	0	0	1	81	Temperature Grade - XT, No Heat Spreader, Row-1
234	0	0	0	0	0	0	0	0	00	Module Organization – 1Rx8
235	0	0	1	0	1	0	1	0	2A	2 Channels, 4-bit ECC, 32 bit Channel Bus Width
244[1]	1	0	1	0	0	0	0	0	A0	CKD-RW00: CKD Configuration – Enabled QCK0 only
245[1]	0	1	0	1	0	1	0	1	55	CKD-RW02 QCK Driver Characteristics – Moderate
246[1]	0	0	0	0	0	0	0	0	00	CKD-RW03: QCK Output Diff Slew Rate - Moderate

NOTE 1 DIMM vendor has option to update these bytes to optimize product.

20 Cross Section Recommendations

The PCB edge connector contacts shall be gold plated.

Any exceptions to these design rules have been identified in the front of this annex

Table 15 — PCB Fabrication Table

Layer	Layer Description	Single-ended Impedances		Copper (oz)	Dielectric Thickness (µm)
		Trace Width (mm)	Impedance (ohm)		
1	Address (loaded), Other[3]	0.080	55±10%	0.3 + Plating	40
	DQ, Strobe & Address (unloaded), DCK	0.155	40±10%		
	QCK	0.31	25±15%		
	Dielectric				65
2	GND			0.5	15
	Dielectric				62
3	DQ, Strobe & Address (unloaded) DCK	0.130	40±10%	0.5	15
	Address (loaded), Other[3]	0.065	55±10%		
	Dielectric				395
4	GND			0.5	15
	Dielectric				62
5	QCK	0.28	25±15%	0.5	15
	DQ, Strobe	0.130	40±10%		
	Other[3]	0.065	55±10%		
	Dielectric				395
6	Address (loaded), Other[3]	0.065	55±10%	0.5	15
	DQ, Strobe & Address (unloaded), DCK	0.130	40±10%		
	Dielectric				62
7	GND			0.5	15
	Dielectric				65
8	Address (loaded), Other[3]	0.080	55±10%	0.3 + Plating	40
	DQ, Strobe & Address (unloaded) DCK	0.155	40±10%		
	QCK	0.31	25±15%		

NOTE 1 The recommended construction and impedance can be found in the PCB Fabrication Table. The values in the table were used in the simulations during development and in the initial DIMMs used to verify operation. Deviations should be kept to a minimum.

NOTE 2 Clock and Strobe differential impedance is the result of the single ended impedance with spacing in the DIMM design.

NOTE 3 “Other” refers to signals inclusive of – ALERT_n, RESET_n, Loopback and Sideband

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Standard Improvement Form **JEDEC Standard No. JESD323-B4-RCD**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 10th Street North
Suite 240S
Arlington, VA 22201

Email: angies@jedec.org

1. I recommend changes to the following:

☐ Requirement, clause _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


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