JEDEC STANDARD

DDR5 DIMM Label

JESD401-5D

Revision of JESD401-5C, December 2024

FEBRUARY 2026

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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(From JEDEC Board Ballot JCB-26-04, formulated under the cognizance of the JC-45 Committee on DRAM Modules, item 2268.20).

1 Scope

The following labels shall be applied to all DDR5 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A readable point size should be used, and the information may be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields. Unused letters in each field, such as ggg, are to be omitted when not needed.

Hybrid modules appear to the system with a “base module type” compatible interface. For example, an NVDIMM-N may be constructed with an RDIMM-style interface or an LRDIMM-style interface. What specific functions the module provides are described in an “Hybrid Media Type” field (‘n’), essentially a functional overlay on the base module type.

Module maximum speeds are not equivalent to DRAM maximum speeds. The speed of a module in megatransfers per second (MT/s) may be affected by the maximum speed of support components on the module or the system configuration for which the modules were designed. The DIMM label does, however, retain information about the DRAM speed grade used for the assembly. For example, if an RDIMM is constructed using DDR5-7200AN DRAMs, but uses support components that limit DIMM performance to 6400 MT/s speeds, the DIMM label will state “6400AN” in the wwwwaa field. In all cases, the user system BIOS must read the serial presence detect (SPD) on the module for the correct rounding algorithms to apply for timing of the interface. See JESD400-5 for details.

For MRDIMMs operating in Mux mode, the clock rate from the host to the module is twice the clock rate to the DRAMs. For example, an MRDIMM rated to 12800 MT/s/pin data rate will have a 6400 MHz clock rate to the multiplex registering clock driver (MRCD) on the module. The MRCD reduces the clock rate, sending a 3200 MHz clock to the DRAMs. For MRDIMMs operating in Rank mode, the clock to the MRCD and clock to the DRAMs is the same speed.

Terminology:

Rank or Package Rank: Collection of SDRAMs on a DIMM sharing a common chip select or copy of a chip select. Chip selects may be sourced by the host controller or by a redriver device such as registering clock driver.

Logical Rank: 3DS stacked DDR5 SDRAMs decode which internal die is selected by decoding chip identifiers (CIDs) in the command. Each package rank, therefore, may contain multiple logical ranks per package rank, increasing module capacity.

Channel: Addresses, clocks, data and associated signals that span the width of the DIMM interface from and to the host controller. For CAMM2s, a module may support one or two channels; in this context, the term channel refers to the organization of the related sub-channel logic at the host controller, i.e., one or two full host channels are connected to one CAMM2.

Sub-channel: The data across the width of the DDR5 standard DIMMs is divided into two independent sub-channels, each with half the data width of the full DDR5 channel. For example, an RDIMM with 80 data bits of width is internally divided into two sub-channels of 40 bits each (32 data bits and 8 ECC bits). For LPDDR5/5X CAMM2s, each LPDDR5 channel is divided into 4 sub-channels, each 16 bits wide. ECC is not supported.

1 Scope (cont'd)

Though technically a CAMM2 (compression attached memory module) is not a DIMM (dual in-line memory module), for the sake of documentation simplicity, a CAMM2 will be considered a kind of DIMM except when it is necessary to draw a distinction.

Example 1: DDR5 MRDIMM 2Rx8

In this example, the data width of each DDR5 component is 8 bits, arranged as two ranks which are multiplexed through MDB devices to provide a 40-bit word on each sub-channel.

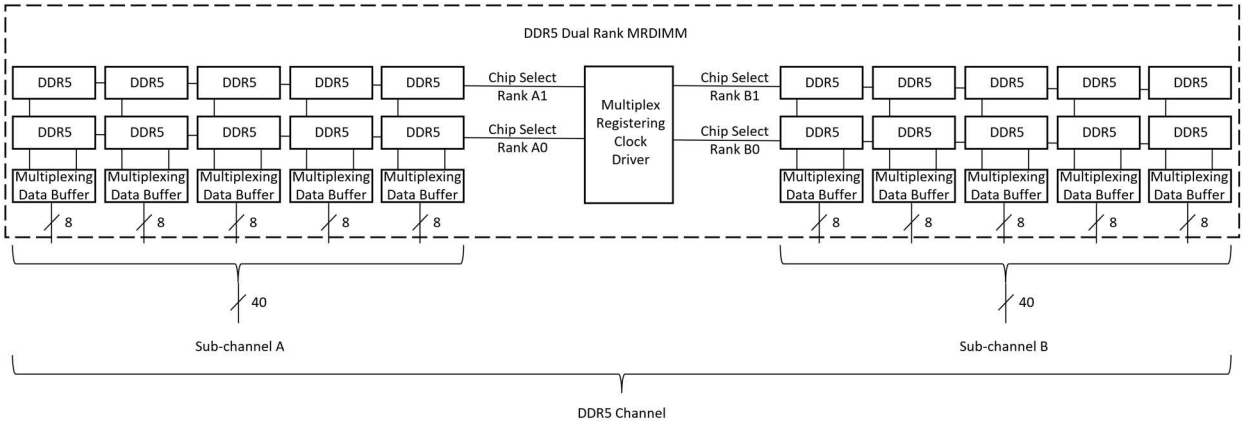


Figure 1 — Example: DDR5 MRDIMM 2Rx8

Example 2: LPDDR5/5X CAMM2 2 Channel 1Rx16

In this example, the data width of each LPDDR5/5X component is 32 bits, however, they are organized with separate chip selects for separate x16 data buses internally. This configuration therefore is referred to as "1Rx16", matching the component configuration, and consistent with the definition of "rank" as the data word width associated with each chip select. The sub-channels, however, are explicitly called out such that each 64 bit channel is still comprised of four x16 sub-channels, A through D.

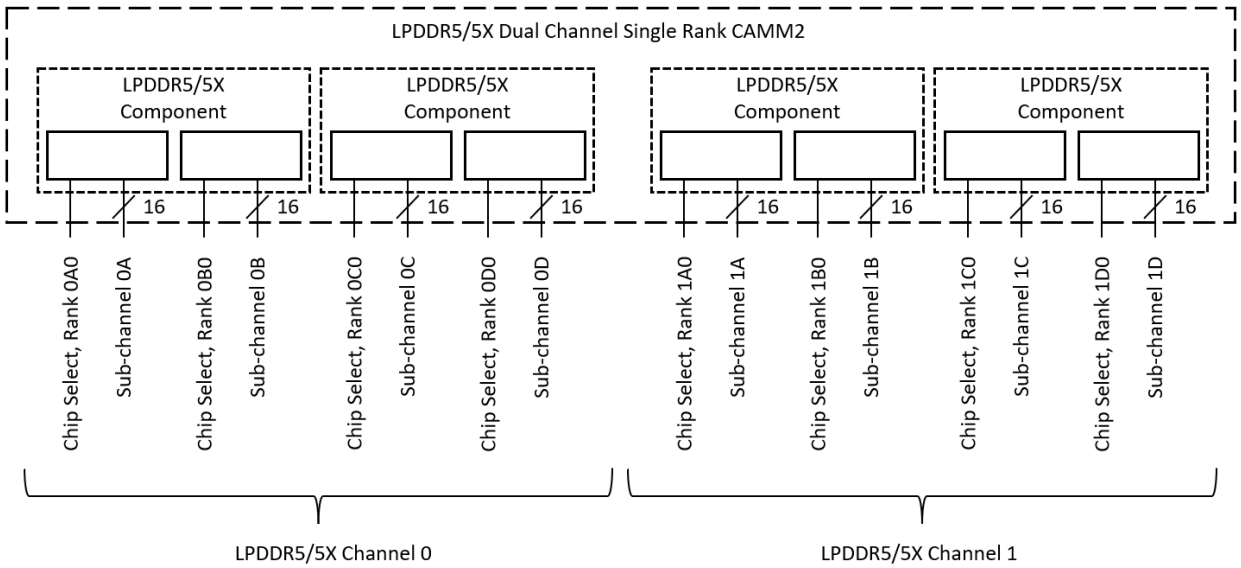


Figure 2 — Example 2: LPDDR5/5X CAMM2 2 Channel 1Rx16

1 Scope (cont'd)

Example 3: DDR5 CAMM2 1 Channel 4Rx8

Single channel versus dual channel CAMM2s are distinguished by the module type field m; for example, G refers to a single channel DDR5 CAMM2, and H refers to a dual channel DDR5 CAMM2.

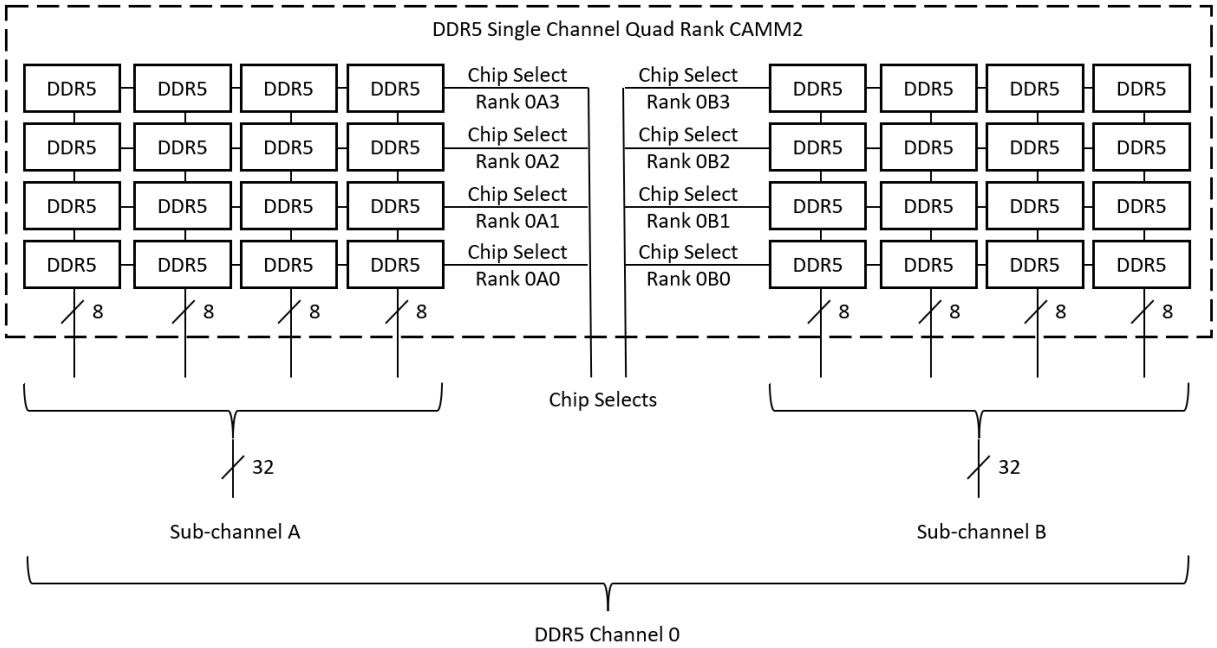


Figure 3 — Example 3: DDR5 CAMM2 1 Channel 4Rx8

Example 4: LPDDR5/5X CAMM2 2 Channel 4Rx16

The quad rank LPDDR CAMM2 uses LPDDR5/5X packages with multiple die sharing data lines but using independent chip selects. These designs may have the same module type (field m) and be differentiated by the LPDDR DRAM type installed; the type of device installed is defined in field hee.

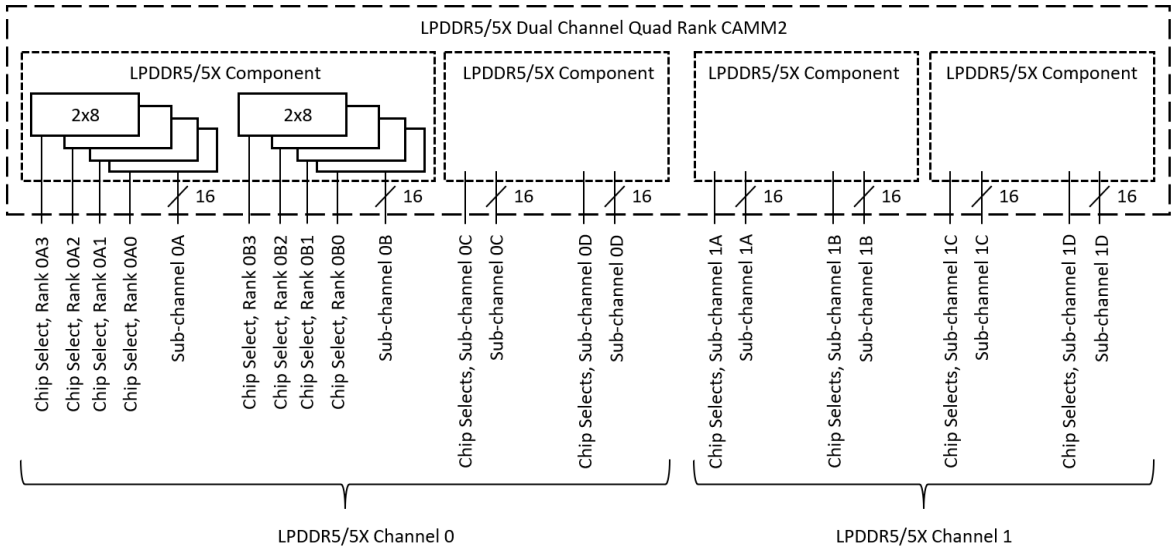


Figure 4 — LPDDR5/5X CAMM2 2 Channel 4Rx16

2 DDR5 DIMM Label Format for DRAM-only Module Types Except MRDIMM

DDR5 DIMM labels for DRAM-only memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

2.1 Module Type Section

ddr dimm_type

Where:

ddr = one of:

DDR5	LPDDR5	LPDDR5X	

dimm_type = one of:

UDIMM	EC4 UDIMM	SODIMM	EC4 SODIMM
EC4 RDIMM	EC8 RDIMM	EC8 LRDIMM	DDIMM
CAMM2	EC4 CAMM2	SOCAMM2	
CUDIMM	EC4 CUDIMM	CSODIMM	EC4 CSODIMM
CQDIMM	EC4 CQDIMM		

2.2 Technical Detail Section

ggg**GB** phee**Rx**ff **PC5-**wwwwaa**-**mccd.vv**-**bbss**-**ttt

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted). ggg**TB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)

phee**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.

p =
- 1 = 1 package rank of SDRAMs per sub-channel
- 2 = 2 package ranks of SDRAMs per sub-channel
- 4 = 4 package ranks of SDRAMs per sub-channel

hee =
- blank = monolithic DRAM (SDP = single die package)
- D2 = Dual die package (DDP); multi-load
- D4 = 4 die per package; multi-load
- D8 = 8 die per package; multi-load
- D16 = 16 die per package; multi-load
- S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
- S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
- S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
- S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank

R = rank(s)

xff = Device organization (data bit width) of SDRAMs used on this assembly
- x4 = x4 organization (4 DQ lines per SDRAM)
- x8 = x8 organization
- x16 = x16 organization

wwww = SDRAM/module maximum data rate in MT/s/data pin
- 3200 MT/s/pin
- 3600 MT/s/pin
- 4000 MT/s/pin

2.2 Technical Detail Section (cont'd)

4400 MT/s/pin
4800 MT/s/pin
5200 MT/s/pin
5600 MT/s/pin
6000 MT/s/pin
6400 MT/s/pin
6800 MT/s/pin
7200 MT/s/pin
7600 MT/s/pin
8000 MT/s/pin
8400 MT/s/pin
8800 MT/s/pin
9200 MT/s/pin

aa = SDRAM speed grade
aa = Speed grade, i.e., AN, B, BN, C

Table 1 — Examples of DDR5 Monolithic or DDP Components

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46

Table 1 — Examples of DDR5 Monolithic or DDP Components (cont'd)

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63
7600AN	54	54	54
7600B	61	61	61
7600BN	62	62	62
7600C	68	67	67
8000AN	56	56	56
8000B	64	64	64
8000BN	64	64	64
8000C	70	70	70
8400AN	60	60	60
8400B	68	68	68
8400BN	68	68	68
8400C	74	74	74
8800AN	62	62	62
8800B	71	71	71
8800BN	72	72	72
8800C	78	77	77
9200AN	66	66	66
9200B	74	74	74
9200BN	74	74	74
9200C	82	82	82

2.2 Technical Detail Section (cont'd)

Table 2 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52

Table 2 — Examples of DDR5 3DS Stacked Components (cont'd)

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63
7600AN 3DS	62	54	54
7600B 3DS	72	61	61
7600BN 3DS	72	62	62
7600C 3DS	76	67	67
8000AN 3DS	64	56	56
8000B 3DS	74	64	64
8000BN 3DS	74	64	64
8000C 3DS	80	70	70
8400AN 3DS	68	60	60
8400B 3DS	78	68	68
8400BN 3DS	78	68	68
8400C 3DS	84	74	74
8800AN 3DS	72	62	62
8800B 3DS	82	71	71
8800BN 3DS	82	72	72
8800C 3DS	88	77	77
9200AN 3DS	74	66	66
9200B 3DS	86	74	74
9200BN 3DS	86	74	74
9200C 3DS	92	81	81

2.2 Technical Detail Section (cont'd)

m = Module Type

Table 3 — Module Types Sub-channels per DIMM and Sub-channel and ECC Width

m	Description	Marketing Designator	Sub-Channels Per DIMM	Sub-channel Width (bits)	ECC Width (bits)
A	DDR5 Clocked Unbuffered DIMM	DDR5 CUDIMM	2	32	None
B	DDR5 EC4 Clocked Unbuffered DIMM	DDR5 EC4 CUDIMM	2	32	4
C	DDR5 EC4 Clocked Quad-Rank Unbuffered DIMM	DDR5 EC4 CQDIMM	2	32	4
D	DDR5 Differential DIMM	DDR5 DDIMM	2	32	8
E	DDR5 EC4 Unbuffered DIMM	DDR5 EC4 UDIMM	2	32	4
F	Dual Channel LPDDR5/LPDDR5X CAMM2	LPDDR5/5X CAMM2	8	16	None
G	Single Channel DDR5 CAMM2	DDR5 CAMM2	2	32	None
H	Dual Channel DDR5 CAMM2	DDR5 CAMM2	4	32	None
J	Dual Channel LPDDR5/LPDDR5X SOCAMM2	LPDDR5/5X SOCAMM2	8	16	None
K	DDR5 Clocked Quad-Rank Unbuffered DIMM	DDR5 CQDIMM	2	32	0
L	DDR5 EC8 Load Reduced DIMM	DDR5 EC8 LRDIMM	2	32	8
P	DDR5 EC4 Registered DIMM	DDR5 EC4 RDIMM	2	32	4
R	DDR5 EC8 Registered DIMM	DDR5 EC8 RDIMM	2	32	8
S	DDR5 Small Outline DIMM	DDR5 SODIMM	2	32	None
T	DDR5 EC4 Small Outline DIMM	DDR5 EC4 SODIMM	2	32	4
U	DDR5 Unbuffered DIMM	DDR5 UDIMM	2	32	None
V	DDR5 Clocked Small Outline DIMM	DDR5 CSODIMM	2	32	None
W	DDR5 EC4 Clocked Small Outline DIMM	DDR5 EC4 CSODIMM	2	32	4

NOTES:
ECC width is equivalent to the Bus Width Extension Per Sub-Channel (SPD byte 235, bits 4~3)
DIMM = Dual In-Line Memory Module
CAMM2 = Compression Attached Memory Module
SOCAMM2 = Small Outline Compression Attached Memory Module
CQDIMM = Clocked Quad-rank Dual In-Line Memory Module

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases
- Z = To be used when field cc = ZZ

vv = Pre-production revision
- 00 = Production release
- vv = Pre-production releases

bb = JEDEC SPD Revision level used on this DIMM, Base section, SPD byte 1
ss = JEDEC SPD Revision level used on this DIMM, Module specific section, SPD byte 192

2.2 Technical Detail Section (cont'd)

-ttt = Temperature grade (see JESD402-1 for details)
- -A1T = Operating Temperature Range A1T, -40 °C to +125 °C
- -A2T = Operating Temperature Range A2T, -40 °C to +105 °C
- -A3T = Operating Temperature Range A3T, -40 °C to +85 °C
- -ET = Operating Temperature Range ET, -25 °C to +105 °C
- -IT = Operating Temperature Range IT, -40 °C to +95 °C
- -NT = Operating Temperature Range NT, 0 °C to +85 °C
- -ST = Operating Temperature Range ST, -25 °C to +85 °C
- -RT = Operating Temperature Range RT, 0 °C to +45 °C
- -XT = Operating Temperature Range XT, 0 °C to +95 °C
- -ZZT = Vendor specific temperature range

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. The first letter in the cc field indicates which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level.

Table 4 — Pre-Production and Production DIMM Revisions

DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
Z	Z	Non-standard design

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA	Pre-production sample of raw card F0
ccd = F0	Production F0 module
ccd = FB	Pre-production sample of raw card F1
ccd = F1	Production F1 module

Some pre-production modules go through many design variations. The ".vv" field adds the revision level of the pre-production module (with an implied 0. lead-in). Production modules code ".vv" as ".00". When combined, ccd.vv examples include:

ccd.vv = FA.51	Pre-production sample of raw card F0, design revision 0.51
ccd.vv = F0.00	Production F0 module
ccd.vv = AAB.73	Pre-production sample of raw card AA1, design revision 0.73

The ".vv" field was optional until June 2025, and is mandatory thereafter. For modules already in production, this policy change is optional.

2.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> where

<vid> = DIMM Vendor ID, 4 characters (SPD bytes 512~513)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 514)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 515),
2 characters for week (SPD byte 516)
<serial> = Unique serial number assigned by manufacturer, 8 characters (SPD bytes 517~520)

(Format %02x%02x%02x%02x%02x%02x%02x%02x%02x)

Note: Field <mfgdate> uses BCD characters (0-9). Other fields support hex characters (0-F).

2.4 Part Number Section

PN:partnumber

Where:

partnumber = module part number (SPD bytes 521~550)

2.5 Machine Readable Section

2d_barcode

Where:

2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails**(S)**serialnumber**(P)**partnumber**(C)**countryoforigin

where technicaldetails, serialnumber, and partnumber are as defined in clauses 2.2 through 2.4 of this standard. The serialnumber field is exactly 21 characters long, including hyphens. The partnumber field comes from SPD bytes 521~550.

The countryoforigin field is exactly two alphabetic characters as defined in ISO 3166. It refers to the country where final assembly of the module was done. This field is optional until June 2026, and mandatory thereafter. For modules already in production, this policy change is optional.

2.5 Machine Readable Section (cont'd)

Some example country codes:

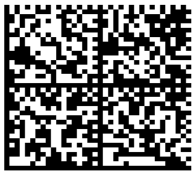
Country	Code
China	CN
Japan	JP
Republic of Korea	KR
Taiwan	TW
United States of America	US

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x), where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition; lower case characters (a-z) may be used for supplier specific information.

Delineated sections of the barcode may be in any order.

In order to allow additional room on future DIMM Labels for more details, the inclusion of 1D barcodes on labels shall be deprecated. Implementation of this policy shall begin immediately for CAMM2 and SOCAMM2 modules, and January 2028 for new designs of all other module types. For modules already in production, this policy change is optional.

2.6 Examples



DDR5 EC8 RDIMM
64GB 2Rx4 PC5-4400B-RA2-1110-IT
SN:802C26210112345678
PN:MTA12ASF2G72PA-4H4A0

Figure 5 — Example of DDR5 EC8 RDIMM

64 GB DDR5 RDIMM (two 40 bit sub-channels with 32-bit data and 8-bit ECC per sub-channel)
2 package ranks per sub-channel
using SDP DDR5 SDRAMs
x4 data organization per SDRAM
DDR5-4400 performance, Speed grade B: CAS Latency = 36
Raw card reference design file A revision 2 used for the assembly
DDR5 base SPD revision 1.1, module SPD revision 1.0
Operating temperature IT (-40 °C to +95 °C)
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2021 week 01
Unique product serial number 12345678
Part number MTA12ASF2G72PA-4H4A0
Barcode text
(L)64GB 2Rx4 PC5-4400B-RA2-1110-IT(S)802C26160112345678(P)MTA12ASF2G72PA-4H4A0

LPDDR5X CAMM2
32GB 1Rx16 PC5-6400-FF1-1010-IT
SN:802C03230312345678
PN:MTA32ASF4G72PA-4H4A0

Figure 6 — Example of LPDDR5 CAMM2

32 GB LPDDR5 CAMM2 (8 sub-channels with 16-bit data per sub-channel)
1 package rank per sub-channel
using SDP LPDDR5X SDRAMs
x16 data organization per SDRAM chip select
LPDDR5-6400 performance
Raw card reference design file F revision 1 used for the assembly
LPDDR5 base SPD revision 1.0, module SPD revision 1.0
Operating temperature IT (-40 °C to +95 °C)
Manufacturer code 80 2C
Manufacturing location 03 (vendor specific)
Manufacturing date 2023 week 03
Unique product serial number 12345678
Part number MTA32ASF4G72PA-4H4A0
Barcode text
(L)32GB 1Rx16 PC5-6400-FF1-1010-IT(S)802C030230312345678(P)MTA32ASF4G72PA-4H4A0

3 DDR5 DIMM Label Format for DRAM-only MRDIMM Module Types

DDR5 DIMM labels for DRAM-only memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label.

3.1 Module Type Section

DDR5 dimm_type

Where:

dimm_type = one of:
EC4 MRDIMM EC8 MRDIMM

3.2 Technical Detail Section

ggg**GB** phee**R**x**f** **PC5-**yyy**/**wwaa**-**mccd.vv**-**bbss**-**ttt

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted). ggg**TB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)
phee**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.
p =
1 = 1 package rank of SDRAMs per sub-channel
2 = 2 package ranks of SDRAMs per sub-channel
4 = 4 package ranks of SDRAMs per sub-channel
hee =
blank = monolithic DRAM (SDP = single die package)
D2 = Dual die package (DDP)
S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank
R = rank(s)
xf = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
yyy = Module maximum data rate in 100 MT/s/data pin in Mux mode
88: 8800 MT/s/pin
96: 9600 MT/s/pin
104: 10400 MT/s/pin
112: 11200 MT/s/pin
120: 12000 MT/s/pin
128: 12800 MT/s/pin
136: 13600 MT/s/pin -- reserved
144: 14400 MT/s/pin -- reserved
152: 15200 MT/s/pin -- reserved
160: 16000 MT/s/pin -- reserved
168: 16800 MT/s/pin -- reserved
176: 17600 MT/s/pin -- reserved
184: 18400 MT/s/pin -- reserved

3.2 Technical Detail Section (cont'd)

ww = SDRAM/module maximum data rate in 100 MT/s/data pin in Mux or Rank mode
- 32: 3200 MT/s/pin
- 36: 3600 MT/s/pin
- 40: 4000 MT/s/pin
- 44: 4400 MT/s/pin
- 48: 4800 MT/s/pin
- 52: 5200 MT/s/pin
- 56: 5600 MT/s/pin
- 60: 6000 MT/s/pin
- 64: 6400 MT/s/pin
- 68: 6800 MT/s/pin — reserved
- 72: 7200 MT/s/pin — reserved
- 76: 7600 MT/s/pin — reserved
- 80: 8000 MT/s/pin — reserved
- 84: 8400 MT/s/pin — reserved
- 88: 8800 MT/s/pin — reserved
- 92: 9200 MT/s/pin — reserved

aa = SDRAM speed grade
- aa = Speed grade, i.e., AN, B, BN, C

Table 5 — Examples of DDR5 Monolithic or DDP Components

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42

Table 5 — Examples of DDR5 Monolithic or DDP Components (cont'd)

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63
7600AN	54	54	54
7600B	61	61	61
7600BN	62	62	62
7600C	68	67	67
8000AN	56	56	56
8000B	64	64	64
8000BN	64	64	64
8000C	70	70	70
8400AN	60	60	60
8400B	68	68	68
8400BN	68	68	68
8400C	74	74	74
8800AN	62	62	62
8800B	71	71	71
8800BN	72	72	72
8800C	78	77	77
9200AN	66	66	66
9200B	74	74	74
9200BN	74	74	74
9200C	82	82	82

3.2 Technical Detail Section (cont'd)

Table 6 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52

Table 6 — Examples of DDR5 3DS Stacked Components (cont'd)

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63
7600AN 3DS	62	54	54
7600B 3DS	72	61	61
7600BN 3DS	72	62	62
7600C 3DS	76	67	67
8000AN 3DS	64	56	56
8000B 3DS	74	64	64
8000BN 3DS	74	64	64
8000C 3DS	80	70	70
8400AN 3DS	68	60	60
8400B 3DS	78	68	68
8400BN 3DS	78	68	68
8400C 3DS	84	74	74
8800AN 3DS	72	62	62
8800B 3DS	82	71	71
8800BN 3DS	82	72	72
8800C 3DS	88	77	77
9200AN 3DS	74	66	66
9200B 3DS	86	74	74
9200BN 3DS	86	74	74
9200C 3DS	92	81	81

3.2 Technical Detail Section (cont'd)

m = Module Type

Table 7 — Module Type Sub-channels per DIMM and Sub-channel and ECC Width

mm	Description	Marketing Designator	Sub-Channels Per DIMM	Sub-channel Width (Bits)	ECC Width (Bits)
M	DDR5 EC8 Multiplexed Rank DIMM	DDR5 EC8 MRDIMM	2	32	8
N	DDR5 EC4 Multiplexed Rank DIMM	DDR5 EC4 MRDIMM	2	32	4
NOTES: ECC width is equivalent to the Bus Width Extension Per Sub-Channel (SPD byte 235, bits 4~3) DIMM = Dual In-Line Memory Module					

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases
- Z = To be used when field cc = ZZ

vv = Pre-production revision
- 00 = Production release
- vv = Pre-production releases

bb = JEDEC SPD Revision level used on this DIMM, Base section, SPD byte 1

ss = JEDEC SPD Revision level used on this DIMM, Module specific section, SPD byte 192

-ttt = Temperature grade (see JESD402-1 for details)
- -A1T = Operating Temperature Range A1T, -40 °C to +125 °C
- -A2T = Operating Temperature Range A2T, -40 °C to +105 °C
- -A3T = Operating Temperature Range A3T, -40 °C to +85 °C
- -ET = Operating Temperature Range ET, -25 °C to +105 °C
- -IT = Operating Temperature Range IT, -40 °C to +95 °C
- -NT = Operating Temperature Range NT, 0 °C to +85 °C
- -ST = Operating Temperature Range ST, -25 °C to +85 °C
- -RT = Operating Temperature Range RT, 0 °C to +45 °C
- -XT = Operating Temperature Range XT, 0 °C to +95 °C
- -ZZT = Vendor specific temperature range

3.2 Technical Detail Section (cont'd)

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. The first letter in the cc field indicates which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level.

Table 8 — Pre-Production and Production DIMM Revisions

DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
Z	Z	Non-standard design

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0
ccd = F0 Production F0 module
ccd = FB Pre-production sample of raw card F1
ccd = F1 Production F1 module

Some pre-production modules go through many design variations. The ".vv" field adds the revision level of the pre-production module (with an implied 0. lead-in). Production modules code ".vv" as ".00". When combined, ccd.vv examples include:

ccd.vv = FA.51 Pre-production sample of raw card F0, design revision 0.51
ccd.vv = F0.00 Production F0 module
ccd.vv = AAB.73 Pre-production sample of raw card AA1, design revision 0.73

The ".vv" field was optional until June 2025, and is mandatory thereafter. For modules already in production, this policy change is optional.

3.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> where

<vid> = DIMM Vendor ID, 4 characters (SPD bytes 512~513)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 514)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 515),
2 characters for week (SPD byte 516)
<serial> = Unique serial number assigned by manufacturer, 8 characters (SPD bytes 517~520)

(Format %02x%02x%02x%02x%02x%02x%02x%02x%02x)

Note: Field <mfgdate> uses BCD characters (0-9). Other fields support hex characters (0-F).

3.4 Part Number Section

PN:partnumber

Where:

partnumber = module part number (SPD bytes 521~550)

3.5 Machine Readable Section

2d_barcode

Where:

2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails**(S)**serialnumber**(P)**partnumber**(C)**countryoforigin

where technicaldetails, serialnumber, and partnumber are as defined in clauses 2.2 through 2.4 of this standard. The serialnumber field is exactly 21 characters long, including hyphens. The partnumber field comes from SPD bytes 521~550.

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x), where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition; lower case characters (a-z) may be used for supplier specific information.

The countryoforigin field is exactly two alphabetic characters as defined in ISO 3166. It refers to the country where final assembly of the module was done. This field is optional until June 2026, and mandatory for new module designs thereafter. For modules already in production, this policy change is optional.

3.5 Machine Readable Section (cont'd)

Some example country codes:

Country	Code
China	CN
Japan	JP
Republic of Korea	KR
Taiwan	TW
United States of America	US

Delineated sections of the barcode may be in any order.

In order to allow additional room on future DIMM Labels for more details, the inclusion of 1D barcodes on labels shall be deprecated. Implementation of this policy shall begin January 2028 for new designs. For modules already in production, this policy change is optional.

3.6 Examples

DDR5 EC8 MRDIMM
128GB 4D2Rx4 PC5-88/64AN-MB0-1210-XT
SN:802C26210187654321
PN:NG128DD4G2-4D4B

Figure 7 — Example of DDR5 EC8 MRDIMM

128 GB DDR5 MRDIMM (two 40 bit sub-channels with 32-bit data and 8-bit ECC per sub-channel)
4 package ranks per sub-channel
using DDP DDR5 SDRAMs
x4 data organization per SDRAM
Maximum module data rate in Mux mode is 8800 Mbps/data pin
Maximum module data rate in Rank mode is 6400 Mbps/data pin
DRAM speed grade AN
Raw card reference design file B revision 0 used for the assembly
DDR5 base SPD revision 1.2, module SPD revision 1.0
Operating temperature range XT (0 °C to +95 °C)
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2021 week 01
Unique product serial number 802C26210187654321
Part number NG128DD4G2-4D4B
Barcode text
(L)128GB 4D2Rx4 PC5-88/64AN-MB0-1210-XT(S)802C26210187654321(P)NG128DD4G2-4D4B

DDR5 EC8 MRDIMM 128GB 4D2Rx4
PC5-88/64AN-MB0.73-1210-XT
SN:802C26210187654321
PN:NG128DD4G2-4D4B

Figure 8 — Example of DDR5 EC8 MRDIMM

Same example as Figure 7, with the following changes:
a. Moves 128GB 4D2Rx4 to the first line to reduce label X length.
b. Adds pre-production version 0.73 detail.
c. Country of Origin = Korea (in 2D barcode).
d. Barcode text
(L)128GB 4D2Rx4 PC5-88/64AN-MB0.73-1210-XT(S)802C26210187654321(P)NG128DD4G2-4D4B(C)KR

4 DDR5 DIMM Label Format for Hybrid Module Types

DDR5 DIMM labels for Hybrid memory modules contain four required sections: a module type section, a technical detail section, a serial number section, and a machine-readable section. The first three sections are recommended in order on the label, but the 4th section, machine readable, may be placed anywhere it fits on the label. In addition, modules with self-encryption have a section with an encryption identifier for data recovery, below the serial number section.

4.1 Module Type Section

DDR5 dimm_type

Where:

dimm_type = one of:

EC8 NVRDIMM-N EC4 NVRDIMM-N
EC8 NVLRDIMM-N EC4 NVLRDIMM-N
EC8 NVMRDIMM-N EC4 NVMRDIMM-N

4.2 Technical Detail Section

ggg**GB** phee**R**x**ff** **N**nn**5-**wwwwa**-**mccd.vv**-**bbss**-**ttt

MRDIMM-based hybrid module ONLY:

ggg**GB** phee**R**x**ff** **N**nn**5-**yyy**/**wwa**-**mccd.vv**-**bbss**-**ttt

Where:

ggg**GB** = Module total capacity, in gigabytes, for primary bus (ECC not counted). ggg**TB** for terabytes.
ggg is in natural numbers, e.g., 1GB, 2GB, 4GB, 1TB, etc. (no space between digits and units)
phee**R** = Number of package ranks of memory per DIMM and number of logical ranks per package rank.
p =
1 = 1 package rank of SDRAMs per sub-channel
2 = 2 package ranks of SDRAMs per sub-channel
4 = 4 package ranks of SDRAMs per sub-channel
hee =
blank = monolithic DRAM (SDP = single die package)
D2 = Dual die package (DDP)
S2 = Single load SDRAM stack (3DS), 2 logical ranks in each package rank
S4 = Single load SDRAM stack (3DS), 4 logical ranks in each package rank
S8 = Single load SDRAM stack (3DS), 8 logical ranks in each package rank
S16 = Single load SDRAM stack (3DS), 16 logical ranks in each package rank
R = rank(s)
xff = Device organization (data bit width) of SDRAMs used on this assembly
x4 = x4 organization (4 DQ lines per SDRAM)
x8 = x8 organization
x16 = x16 organization
nn = Module type
N = NVDIMM-N module type
ww(ww) = SDRAM/module maximum data rate in 100 MT/s/data pin in Rank mode (MT/s/data pin for non-MRDIMM configurations)
32(00): 3200 MT/s/pin
36(00): 3600 MT/s/pin

4.2 Technical Detail Section (cont'd)

40(00): 4000 MT/s/pin
44(00): 4400 MT/s/pin
48(00): 4800 MT/s/pin
52(00): 5200 MT/s/pin
56(00): 5600 MT/s/pin
60(00): 6000 MT/s/pin
64(00): 6400 MT/s/pin
68(00): 6800 MT/s/pin
72(00): 7200 MT/s/pin
76(00): 7600 MT/s/pin
80(00): 8000 MT/s/pin
84(00): 8400 MT/s/pin
88(00): 8800 MT/s/pin
92(00): 9200 MT/s/pin

aa = SDRAM speed grade
aa = Speed grade, i.e., AN, B, BN, C

yyy = Module maximum data rate in 100 MT/s/data pin (MRDIMM, operating in Mux mode)
88: 8800 MT/s/pin
96: 9600 MT/s/pin
104: 10400 MT/s/pin
112: 11200 MT/s/pin
120: 12000 MT/s/pin
128: 12800 MT/s/pin
136: 13600 MT/s/pin -- reserved
144: 14400 MT/s/pin -- reserved
152: 15200 MT/s/pin -- reserved
160: 16000 MT/s/pin -- reserved
168: 16800 MT/s/pin -- reserved
176: 17600 MT/s/pin -- reserved
184: 18400 MT/s/pin -- reserved

Examples:

Table 9 — Examples of DDR5 Monolithic Components

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN	24	24	24
3200B	26	26	26
3200BN	26	26	26
3200C	28	28	28
3600AN	26	26	26
3600B	30	30	30
3600BN	30	30	30
3600C	32	32	32
4000AN	28	28	28
4000B	32	32	32
4000BN	32	32	32
4000C	36	35	35
4400AN	32	32	32
4400B	36	36	36
4400BN	36	36	36

Table 9 — Examples of DDR5 Monolithic Components (cont'd)

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
4400C	40	39	39
4800AN	34	34	34
4800B	40	39	39
4800BN	40	40	40
4800C	42	42	42
5200AN	38	38	38
5200B	42	42	42
5200BN	42	42	42
5200C	46	46	46
5600AN	40	40	40
5600B	46	45	45
5600BN	46	46	46
5600C	50	49	49
6000AN	42	42	42
6000B	48	48	48
6000BN	48	48	48
6000C	54	53	53
6400AN	46	46	46
6400B	52	52	52
6400BN	52	52	52
6400C	56	56	56
6800AN	48	48	48
6800B	56	55	55
6800BN	56	56	56
6800C	60	60	60
7200AN	52	52	52
7200B	58	58	58
7200BN	58	58	58
7200C	64	63	63
7600AN	54	54	54
7600B	61	61	61
7600BN	62	62	62
7600C	68	67	67
8000AN	56	56	56
8000B	64	64	64
8000BN	64	64	64
8000C	70	70	70
8400AN	60	60	60
8400B	68	68	68
8400BN	68	68	68
8400C	74	74	74
8800AN	62	62	62
8800B	71	71	71

Table 9 — Examples of DDR5 Monolithic Components (cont'd)

DDR5 Monolithic Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
8800BN	72	72	72
8800C	78	77	77
9200AN	66	66	66
9200B	74	74	74
9200BN	74	74	74
9200C	82	82	82

Table 10 — Examples of DDR5 3DS Stacked Components

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
3200AN 3DS	26	24	24
3200B 3DS	30	26	26
3200BN 3DS	30	26	26
3200C 3DS	32	28	28
3600AN 3DS	30	26	26
3600B 3DS	34	30	30
3600BN 3DS	34	30	30
3600C 3DS	36	32	32
4000AN 3DS	32	28	28
4000B 3DS	38	32	32
4000BN 3DS	38	32	32
4000C 3DS	40	35	35
4400AN 3DS	36	32	32
4400B 3DS	42	36	36
4400BN 3DS	42	36	36
4400C 3DS	44	39	39
4800AN 3DS	34	34	34
4800B 3DS	46	39	39
4800BN 3DS	46	40	40
4800C 3DS	48	42	42
5200AN 3DS	42	38	38
5200B 3DS	50	42	42
5200BN 3DS	50	42	42
5200C 3DS	52	46	46
5600AN 3DS	46	40	40
5600B 3DS	52	45	45
5600BN 3DS	52	46	46
5600C 3DS	56	49	49
6000AN 3DS	48	42	42
6000B 3DS	56	48	48
6000BN 3DS	56	48	48

Table 10 — Examples of DDR5 3DS Stacked Components (cont'd)

DDR5 3DS Stacked Components			
SDRAM Speed Grade	**CAS Latency**	**tRCD in nCK**	**tRP in nCK**
6000C 3DS	60	53	53
6400AN 3DS	52	46	46
6400B 3DS	60	52	52
6400BN 3DS	60	52	52
6400C 3DS	64	56	56
6400C 3DS	64	56	56
6800AN 3DS	56	48	48
6800B 3DS	64	55	55
6800BN 3DS	64	56	56
6800C 3DS	68	60	60
7200AN 3DS	58	52	52
7200B 3DS	68	58	58
7200BN 3DS	68	58	58
7200C 3DS	72	63	63
7600AN 3DS	62	54	54
7600B 3DS	72	61	61
7600BN 3DS	72	62	62
7600C 3DS	76	67	67
8000AN 3DS	64	56	56
8000B 3DS	74	64	64
8000BN 3DS	74	64	64
8000C 3DS	80	70	70
8400AN 3DS	68	60	60
8400B 3DS	78	68	68
8400BN 3DS	78	68	68
8400C 3DS	84	74	74
8800AN 3DS	72	62	62
8800B 3DS	82	71	71
8800BN 3DS	82	72	72
8800C 3DS	88	77	77
9200AN 3DS	74	66	66
9200B 3DS	86	74	74
9200BN 3DS	86	74	74
9200C 3DS	92	81	81

m = Module Type (How DIMM appears electrically to the system)

4.2 Technical Detail Section (cont'd)

Table 11 — Module Type Sub-channels per DIMM and Sub-channel and ECC Width

mm	Description	Marketing Designator	Sub-Channels Per DIMM	Sub-channel Width (bits)	ECC Width (bits)
L	DDR5 EC8 Load Reduced DIMM	DDR5 EC8 LRDIMM	2	32	8
M	DDR5 EC8 Multiplexed Rank DIMM	DDR5 EC8 MRDIMM	2	32	8
P	DDR5 EC4 Multiplexed Rank DIMM	DDR5 EC4 MRDIMM	2	32	4
R	DDR5 EC8 Registered DIMM	DDR5 EC8 RDIMM	2	32	8

NOTES:
ECC width is equivalent to the Bus Width Extension Per Sub-Channel (SPD byte 235, bits 4~3)
DIMM = Dual In-Line Memory Module

cc = Reference design file used for this design (if applicable)
- A = Reference design for raw card 'A' is used for this assembly
- B = Reference design for raw card 'B' is used for this assembly
- AC = Reference design for raw card 'AC' is used for this assembly
- ZZ = None of the JEDEC standard reference designs were used for this assembly

d = Revision number of the reference design used (see table below)
- 0~9 = Production release revisions
- A~K = Pre-production releases
- Z = To be used when field cc = ZZ

vv = Pre-production revision
- 00 = Production release
- vv = Pre-production releases

bb = JEDEC SPD Revision level used on this DIMM, Base section, SPD byte 1
ss = JEDEC SPD Revision level used on this DIMM, Module specific section, SPD byte 192
-ttt = Temperature grade (see JESD402-1 for details)
- -A1T = Operating Temperature Range A1T, -40 °C to +125 °C
- -A2T = Operating Temperature Range A2T, -40 °C to +105 °C
- -A3T = Operating Temperature Range A3T, -40 °C to +85 °C
- -ET = Operating Temperature Range ET, -25 °C to +105 °C
- -IT = Operating Temperature Range IT, -40 °C to +95 °C
- -NT = Operating Temperature Range NT, 0 °C to +85 °C
- -ST = Operating Temperature Range ST, -25 °C to +85 °C
- -RT = Operating Temperature Range RT, 0 °C to +45 °C
- -XT = Operating Temperature Range XT, 0 °C to +95 °C
- -ZZT = Vendor specific temperature range

As modules are developed in JEDEC, samples of pre-standard approval designs are often distributed for evaluation. The first letter in the cc field indicates which raw card revision the pre-production module represents. For pre-production modules, a letter is used in the 'd' field in place of the target production level.

4.2 Technical Detail Section (cont'd)

Table 12 — Pre-Production and Production DIMM Revisions

DIMM Label Field 'd'		Resulting Production Revision
Pre-Production Revision	Production Revision	
A	0	Raw card revision 0
B	1	Raw card revision 1
C	2	Raw card revision 2
D	3	Raw card revision 3
E	4	Raw card revision 4
F	5	Raw card revision 5
G	6	Raw card revision 6
H	7	Raw card revision 7
J	8	Raw card revision 8
K	9	Raw card revision 9
Z	Z	Non-standard design

Pre-Production Example: A hypothetical release cycle of a raw card F, for example, may proceed like this:

ccd = FA Pre-production sample of raw card F0
ccd = F0 Production F0 module
ccd = FB Pre-production sample of raw card F1
ccd = F1 Production F1 module

Some pre-production modules go through many design variations. The ".vv" field adds the revision level of the pre-production module (with an implied 0. lead-in). Production modules code ".vv" as ".00". When combined, ccd.vv examples include:

ccd.vv = FA.51 Pre-production sample of raw card F0, design revision 0.51
ccd.vv = F0.00 Production F0 module
ccd.vv = AAB.73 Pre-production sample of raw card AA1, design revision 0.73

The ".vv" field was optional until June 2025, and is mandatory thereafter. For modules already in production, this policy change is optional.

4.3 Serial Number Section

SN:serialnumber

Where:

serialnumber = unique module serial number per ACPI specification; see uefi.org/acpi for details
<vid><mfgloc><mfgdate><serial> (Format %02x%02x%02x%02x%02x%02x%02x%02x%02x%02x) where
<vid> = DIMM Vendor ID, 4 characters (SPD bytes 512~513)
<mfgloc> = Manufacturing location, 2 characters (SPD byte 514)
<mfgdate> = Manufacturing date, 2 characters for year (SPD byte 515),
2 characters for week (SPD byte 516)
<serial> = Unique serial number assigned by manufacturer, 8 characters (SPD bytes 517~520)

Note: Field <mfgdate> uses BCD characters (0-9). Other fields support hex characters (0-F).

4.4 Part Number Section

PN:partnumber

Where:

partnumber = module part number (SPD bytes 521~550)

4.5 Physical Presence Security Identifier Section

PSID:psid

Where:

psid = Physical Presence Security ID, exactly 32 printable characters as defined by the Trusted Computing Group Storage Opal SSC Feature Set: PSID specification; see trustedcomputinggroup.org for details

This field is required for hybrid modules that incorporate self-encryption to allow data recovery.

4.6 Machine Readable Section

2d_barcode

Where:

2d_barcode follows DataMatrix ECC 200; see ISO/IEC 16022 for details; characters coded per ISO 8859-1

The size of the DataMatrix is not specified, but must contain sufficient data encoding space for at least the following textual information:

(L)technicaldetails**(S)**serialnumber**(P)**partnumber**(C)**countryoforigin, or

(L)technicaldetails**(S)**serialnumber**(P)**partnumber**(C)**countryoforigin**(K)**psid for modules supporting self-encryption

4.6 Machine Readable Section (cont'd)

where technicaldetails, serialnumber, partnumber, and psid are as defined in clauses 4.2 through 4.5 of this standard. The serialnumber field is exactly 21 characters long, including hyphens. The partnumber field comes from SPD bytes 521~550. The psid field, when included, is exactly 32 characters long.

The countryoforigin field is exactly two alphabetic characters as defined in ISO 3166. It refers to the country where final assembly of the module was done. This field is optional until June 2026, and mandatory for new module designs thereafter. For modules already in production, this policy change is optional.

Some example country codes:

Country	Code
China	CN
Japan	JP
Republic of Korea	KR
Taiwan	TW
United States of America	US

Other fields are permitted in the machine readable 2D barcode, and each section must start with (x), where x is a single section delineation character. Upper case characters (A-Z) in section delineation are reserved for JEDEC definition; lower case characters (a-z) may be used for supplier specific information. Delineated sections of the barcode may be in any order.

In order to allow additional room on future DIMM Labels for more details, the inclusion of 1D barcodes on labels shall be deprecated. Implementation of this policy shall begin January 2028 for all hybrid module types. For modules already in production, this policy change is optional.

4.7 Examples

DDR5 EC8 NVRDIMM-N
64GB 1Rx4 NN5-4400B-RZZZ-1112-XT
SN:802C26200112345678
PN:MTA12ASF2G72PA-4H4A0
PSID:876543218765432187654321876543 21

Figure 9 — Example of DDR5 EC8 NVRDIMM-N

64 GB DDR5 NVDIMM-N (dual sub-channel with 32-bit data and 8-bit ECC per sub-channel)
Appears as an RDIMM with 1 package rank per DIMM using SDP DDR5 SDRAMs with x4 data organization per SDRAM
DDR5-4400 performance, speed grade B: CAS Latency = 36
No standard raw card reference design file used for the assembly
DDR5 base SPD revision 1.1, module SPD revision 1.2
Extended operating temperature grade
Manufacturer code 80 2C
Manufacturing location 26 (vendor specific)
Manufacturing date 2020 week 01
Unique product serial number 12345678
Part number MTA12ASF2G72PA-4H4A0
PSID self-encryption key 876543218765432187654321876543 21
Barcode text
(L)64GB 1Rx4 NN5-4400B-RZZZ-1112-XT(S)802C26160112345678(P)MTA12ASF2G72-PA4H4A0(K)876543218765432187654321876543 21

Annex A — (Informative) Differences between Document Revisions

A.1 Differences between JESD401-5A and JESD401-5

- Clause 1 (Scope): Clarified terminology, picture of example module; fixed NVDIMM section adding nn field
- Added MRDIMM, deleted NVDIMM-P
- Separated DRAM speed from module speed
- Changed wording back for wwww to SDRAM speed
- Shortened MRDIMM label length using abbreviated speeds, added EC4 MRDIMM option
- Changed references of 2:1 to Mux, 1:1 to Rank

A.2 Differences between JESD401-5B and JESD401-5A

General:

- Added CAMM2, new speed grades, clocked DIMMs
- Converted m field to tables
- Removed single channel LP CAMM
- Added D4-16 package options
- Corrected typo for EC4 CSODIMM, added DDR5 prefix for all modules (consistent with LPDDR5/5X prefix)

Details:

Section	Changes
1	Added paragraphs for CAMM2
1	Added Figure 2 — Example 2: LPDDR5/5X CAMM2 2 Channel 1Rx16
	Added Figure 3 — Example 3: DDR5 CAMM2 1 Channel 4Rx8
	Added Figure 4 — Example 4: LPDDR5/5X CAMM2 2 Channel 4Rx16
2.1	Added CAMM2 and EC4 CAMM2 under ddr dimm_type
Table 1	Added rows for 7600AN through 8800C
Table 2	Added rows for 7600AN 3DS through 8800C 3DS
2.2	Converted m field to Table 3
2.6	Added new Figure 6 — Example of LPDDR5 CAMM2
Table 5	Added rows for 7600AN through 8800C
Table 6	Added rows for 7600AN 3DS through 8800C 3DS
3.2	Converted m field to Table 7
Table 9	Added rows for 7600AN through 8800C
Table 10	Added rows for 7600AN 3DS through 8800C 3DS
4.2	Converted m field to Table 11

A.3 Differences between JESD401-5B.01 and JESD401-5B

- Editorial revision to add new clocked memory modules CUDIMM and CSODIMM, which were inadvertently omitted from the ddr dimm_type field (Section 2.1) - approved by TG and committee.

A.4 Differences between JESD401-5C and JESD401-5B.01

- Added 2 new paragraphs after paragraph 2 in Clause 1
- Added “vv” to label format in Clause 2.2, 3.2, and 4.2
- Added more rows in Table 2, 5, 6,9, and 10
- Added examples of MRDIMM with content on different lines
- Added preproduction support material
- Changed Mbps to MT/s consistent with JESD79-5
- Added description of module speed versus DRAM speed
- Added 9200 bin information
- Un-reserved MRDIMM speeds to 12800 (mux mode)
- Wording regarding clock rate for MRDIMM
- Fixed figure reference in MRDIMM examples
- Eliminated CL description for MRDIMM DRAM speed

A.5 Differences between JESD401-5D and JESD401-5C

- Changed document title to DDR5 DIMM Label (instead of ... Labels) to align with the document naming convention spreadsheet, “JEDEC Standard List”
- All throughout: Corrected typographical errors like extra spaces
- Tables 2, 6, and 10: Corrected typos - from 92000C 3DS to 9200C 3DS
- Clause 2.1: Added SOCAMM2, CQDIMM, and EC4 CQDIMM
- Clause 2.2: Deleted one “m” in the module type code
- Table 3: Added row and NOTE under module type “m” for SOCAMM2, DDR5EC4 CQDIMM, and DDR5 CQDIMM; added NOTE for CQDIMM; and added “vv” for pre-production revision
- Table 4: Modified last paragraph for “vv” below the table
- Clause 2.3: Changed <serial> from 20 to 8 characters, added Note for <mfgdate> field
- Clause 2.5: Added countryoforigin, plus examples, for country code **C**
- Table 7: Added “vv” for pre-production revision below the table
- Table 8: Modified policy for the “vv” field
- Clause 3.3: Changed <serial> from 20 to 8 characters, added Note for <mfgdate> field
- Clause 3.5: Added countryoforigin, plus examples, for country code **C**
- Table 11: Added “vv” for pre-production revision
- Table 12: Modified policy for the “vv” field
- Clause 4.3: Changed <serial> from 20 to 8 characters, added Note for <mfgdate> field
- Clause 4.6: Added countryoforigin, plus examples, for country code **C**

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Standard Improvement Form **JEDEC JESD401-5D**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

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The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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