JEDEC STANDARD

JEDEC Module Sideband Bus (SidebandBus)

JESD403-1C.01

(Editorial Revision of JESD403-1C, December 2023)

August 2024

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by

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JEDEC MODULE SIDEBAND BUS (SIDEBANDBUS)

(From JEDEC Board Ballot JCB-23-37, formulated under the cognizance of the JC-45 Committee on DRAM Modules, item 2260.80).

1 Scope

This standard defines the assumptions for the system management bus for next generation memory solutions; covering the interface protocol, use of hub devices, and voltages appropriate to these usages.

2 Terminology

This standard has been updated to utilize terms with preferred social and cultural connotations.

Table 1 — Terminology

Term	Definition
CCC	Common command code.
Controller	A SidebandBus Controller device controls information flow on the I3C Basic bus. It drives the bus clock and coordinates data flow. It provides pull-up voltages on the Host bus data lines.
HID	Host identifier. This 3-bit field uniquely selects one out of up to eight Hub devices on the Host bus. It defines the three least significant bits of the Hub's I3C Basic device address.
Host	SidebandBus/I3C Basic bus Controller.
Host bus	I3C Basic bus between the Controller and Hubs or other I3C Target devices not isolated behind a Hub.
HSA	Host SidebandBus bus device ID address pin; input to a Hub or other Target device to distinguish between identical devices in the I3C Basic address range.
HSCL	Host SidebandBus bus clock, supplied by the Controller.
HSDA	Host SidebandBus data, connected from the Controller to Hubs or Host bus Target devices.
Hub	A SidebandBus Hub is a device that isolates loads on the I3C Basic bus, increasing the number of supported devices on a bus. It provides pull-up voltages on the local bus data lines.
I3C Basic	Serial bus specification defined in coordination with MIPI used as a basis for SidebandBus.
LID	Local identifier. This 4-bit device type identifier uniquely defines one of up to 15 devices on a local bus. It defines the four most significant digits of the local bus device's I3C Basic address.
Local bus	I3C Basic bus between a Hub and Target devices isolated by the Hub from the Host bus.
LSA	Local bus SidebandBus device ID address pin to distinguish between identical devices in the I3C Basic address range.
LSCL	Local SidebandBus clock, driven by the Hub to local bus Target devices.
LSDA	Local SidebandBus data, connected from the Hub to local bus Target devices.
Controller	Replacement for "Master" per the latest Terminology update
PEC	Packet error code.
PMIC	Power management integrated circuit; i.e., voltage regulator.
SA	SidebandBus device ID address pin, generically (Host or Local bus).
SCL	SidebandBus clock, generically (Host or Local bus).
SDA	SidebandBus data, generically (Host or Local bus).
SidebandBus	System management bus for next generation memory solutions, based on I3C Basic.
Target	Replacement for "Slave" per the latest Terminology update
SPD	Serial Presence Detect Hub device.
Target device	A SidebandBus Target device receives input from a Controller device or as pass-through on a Local bus from a Hub device.

3 Protocol

The JEDEC Module Sideband Bus (SidebandBus) architecture is compliant to and compatible with MIPI I3C Basic, a two-wire interface based on SDA (data) and SCL (clock) that is backward compatible with I^2C.

Extensions to I3C Basic include the definition of load-isolation hub devices to increase the number of supported devices and provide explicit identification of the physical location of such devices (e.g., slot identification). The specific reference documents are:

- MIPI Alliance Specification for I3C Basic℠ Version 1.0 – 19 July 2018
- MIPI I3C Basic℠ Target Reset Version 1.0 – 13 December 2018

This clause documents the additional details and conformance waivers to I3C Basic specification to enable the SidebandBus usage. In most cases, I3C Basic and SidebandBus are used interchangeably; differences between them are noted. For detailed operation of modes, please refer to I3C SDR mode in MIPI-I3C Specification above.

3.1 Pins

3.1.1 Serial Clock (SCL)

This pin/signal is used to strobe data in and out of the device. This signal driven is by the bus Controller using a push-pull driver to achieve higher data rates in I3C-SDR mode. It is also possible to use an open-drain driver in the bus Controller, provided that the board has a pull-up resistor connected between SCL and the I/O power supply.

3.1.2 Serial Data (SDA)

This bi-directional pin/signal is used to transfer data in or out of the device. It can operate in open drain mode or push-pull mode. A pull up resistor may be connected from Serial Data (SDA) to I/O power supply with on-die terminations on the Controller which could, optionally, be turned off in push-pull mode. If on-chip termination on the Controller is missing, a pull-up resistor must be present on the board.

3.2 I2C Mode

At power on, SidebandBus devices operate in I^2C mode at up to 1 MHz (FM+ / Fast Mode Plus). This is an open drain I/O mode where the pull-up to VDDIO is supplied by the host bus Controller for the Host bus, and the Hub device for the Local bus. On either Host or Local bus, pull-up may be supplied by external pull-up resistors as well, however, operation is limited to I^2C mode only in a configuration with external pull-ups.

- In-band interrupts are **not** supported in I2C Mode.
- SidebandBus does **not** support clock stretching in I2C Mode.
- Packet error codes (PECs) are **not** supported in I2C mode.
- Multi-Controller capability is **not** supported.
- SidebandBus devices must support bus RESET via a timed low pulse on the SCL line.
- Compliant to I3C Specification, all devices shall be able to handle (ACK and process the mandatory CCCs listed in Sec 4.5.2, and ACK/NACK other CCCs based on specific device requirements) broadcast CCCs when in I2C Mode. Host / Controller shall ensure functional dependency on CCCs are followed – for e.g., SETHID must be sent before SETAASA. Direct CCCs shall be NACK-ed, until the dynamic address is assigned with SETAASA CCC.

3.3 Bus Reset Schemes

SidebandBus devices shall support the SCL pulled-low timeout reset scheme.

3.3.1 Timed RESET

Bus timeout via a timeout pulse on SCL is required in both I^2C and I3C Basic mode. Availability of this function is documented in the DEVCAPS CCC.

To prevent a malfunctioning device from locking up the SidebandBus, a bus protocol RESET mechanism is defined. It uses a timeout mechanism on HSCL as shown in Figure 1. All devices (including a Hub, if present, and all Target devices behind the Hub) on an I^2C or I3C bus are RESET simultaneously. Bus reset operation works same way regardless of whether device is operating in I^2C or I3C Basic Bus mode.

To guarantee the device resets I^2C bus or I3C bus, the SCL clock input LOW time shall be greater than or equal to $t_{TIMEOUT}$(Max). The device does not reset the I2C bus or I3C bus if the HSCL clock input LOW time is less than $t_{TIMEOUT}$(Min).

If the SCL clock input LOW time is between $t_{TIMEOUT(Min)}$ and $t_{TIMEOUT(Max)}$, the device may or may not reset the I^2C bus or I3C Basic bus. Refer to Figure 1 for details.

When a SidebandBus Reset is detected, SidebandBus compliant devices shall do the following.

- Reset the interface to power on reset state and any pending command or transaction is cleared.
- All internal register values including error and interrupt status bits are preserved, except for PEC_ERR (PEC Error) and PROT_ERR (Protocol/Parity Error) fields reported in GET_STATUS CCC which shall be cleared to ‘b0. Exact register location / offset for these fields are device specific.
- The device resets to the I^2C mode of operation [power on state – PEC disabled, IBI disabled, Parity Enabled, HID set to ‘b111]. HUB devices shall not reset (but retain) HID, since they do not re-sample the HSA pin.
- Device floats SDA pin such that it gets pulled High by the external pull-up.

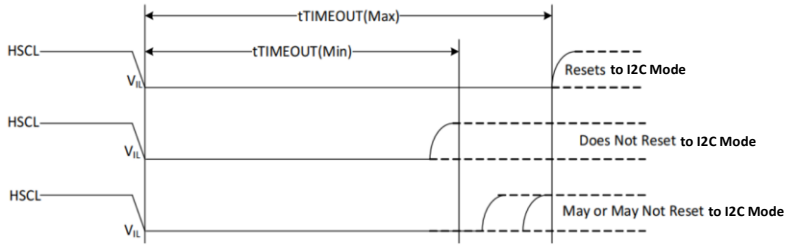


Figure 1 — I2C or I3C Basic Timed RESET

3.3.1.1 Impact of Timed RESET on I3C Devices

Pure MIPI-I3C Specification compliant Target devices that have no notion of timed-reset will ignore the timed-reset sustained SCL low condition, and not treat or report it as an error. An explanatory note on the above is available in the MIPI-I3C FAQ.

3.3.2 Pattern RESET

Pattern reset, also known as MIPI I3C Target Reset, will not be supported on JESD403-1 bus.

3.4 Bus Initialization Sequence

Figure 2 indicates the usage of SETHID and SETAASA for mode change including the effects of reset.

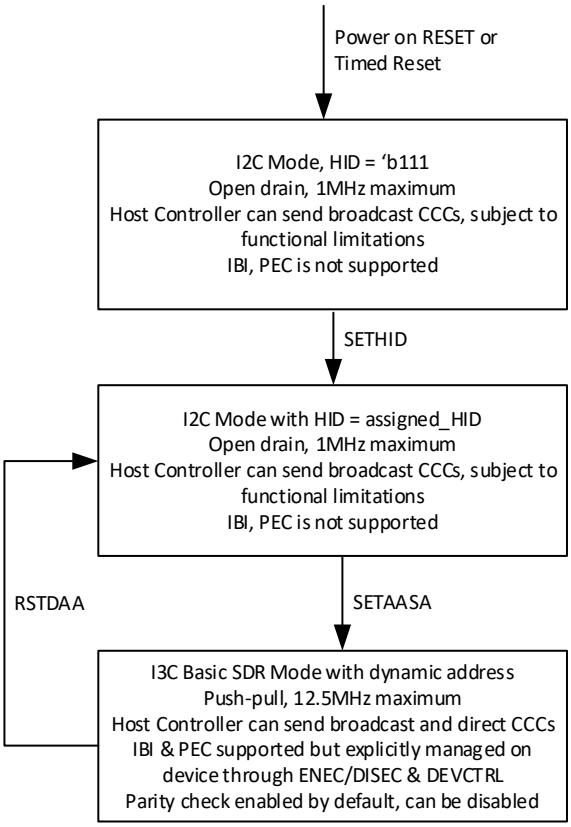


Figure 2 — State / Mode Transition Diagram

The recommended method to check if a dynamic address is assigned and the device is in I3C Basic mode is to issue a direct GET CCC like GETSTATUS. Direct CCCs shall only be ACK-ed once the dynamic address is assigned.

3.5 I3C Basic Mode

SidebandBus devices are put into I3C Basic single data rate (SDR) mode using the SETAASA common command code, which is preceded by a broadcast 7'h7E.

- Controller SCL clock stalling is supported.
- Secondary Controller support is not required.
- SDR mode only; no HDR modes supported.
- No mixing of device protocols. All devices will be in I^2C Mode OR I3C Basic Mode.
- Address arbitration optimization is not supported; (after a START, the first address byte is always in open-drain)
- Hot Join is not supported.
- Timing Control Support is not supported.

3.5.1 Address Assignment and Enumeration

SidebandBus uses a specific and structured addressing scheme as described below to identify DIMMs (memory modules) and devices on the DIMMs. Hence, I3C Basic's ENTDAA and PID based address enumeration scheme is not mandated.

3.5.1.1 Static Address

The 7-bit Static Address for each connected device on the bus is determined by the 4-bit Local Device address (LID, also known as Device Type Identifier, DTI) and the 3-bit Host Device address (HID). The HID bits are used to indicate the DIMM_ID on which the device resides and can range from 'b000 to 'b111, and default to 'b111, except the hub, which determines the HID from its own implementation specific mechanism like precision resistors.

I2C Bus and I3C Bus address:

— Target Address[6:3] = LID / DTI. The assigned DTI/LID values for known device types are documented in Section 4.2 Device Map of this standard.

— Target Address[2:0] = HID, also known as DIMM_ID

The Static Address is used for performing transactions on the bus when the device is in I2C mode.

3.5.1.2 Broadcast Address

The Sideband Bus standard uses 0x7E as the broadcast address, based on MIPI I3C Specification.

3.5.1.3 Address Enumeration and HID Assignment Through the HUB

The power on default value of the HID portion of the Static Address is 'b111. The Hub SPD detects the HID/DIMM_ID using the precision resistor and assists in the assignment of HID, also called DIMM_ID, using two modes.

3.5.1.3.1 HID Modification Scheme

In this mode, which is the power on default, the Hub SPD replaces the LSB 3-bits (HID) of the Target address for the addressed DIMM, except broadcast address of 0x7E, on **each** transaction to 'b111, as documented in Clause 5. Note that all devices power up with a default value of 'b111 for HID.

PEC is **not** supported in this mode.

This mode is in effect until a SETHID CCC is received. Once the Hub detects a SETHID CCC, the Hub shall no longer do the HID bit flipping, and shall transparently pass the incoming 7 bit Target address as is to the local bus. Note that a SETAASA can only be issued following SETHID.

3.5.1.3.2 HID Propagation with SETHID

The Host Controller shall issue a broadcast SETHID CCC to propagate and assign the HID on **all** connected devices, across Hubs. The Hub SPD replaces the 3 bits of the SETHID CCC's payload with its detected HID, known to it through mechanisms like precision resistor.

The devices receiving the SETHID CCC shall use the HID bits in the payload to update the LSB 3 bits of the Target address internally. Once this is done, the device shall only respond to the updated static address with received/assigned HID. A timed reset sets HID back to 'b111.

3.5.1.3.2 HID Propagation with SETHID (cont'd)

The SETHID CCC is documented in Section 3.5.2.7 Set HID Command (SETHID) Operation of this standard.

This assigned HID remains valid until a bus reset (SCL-timeout based reset) is detected or power cycle occurs. On any of these events the devices and the Hub SPD shall transition to the HID Modification Scheme.

3.5.1.3.3 HID Transparent Scheme

Once a SETHID CCC is successfully effectuated across the bus, the Hub SPD shall no longer perform the HID bit flipping and shall transparently pass the incoming 7 bit Target address as is to the local bus.

PEC can be optionally supported in this mode.

3.5.1.4 Dynamic Address

On reception of a SETAASA Command, the current static address is converted/deemed to be the dynamic address as well, and the device is in I3C Basic SDR mode of operation.

Note that SETAASA is a broadcast command, and the host issues just one SETAASA command to move the entire bus into I3C Basic SDR mode, with dynamic address assigned.

A dynamic address can be reset using the RSTDAA command or a bus reset (SCL low-timeout based) or a power-cycle. When the dynamic address is reset, the device shall keep its assigned HID and return to I2C open-drain mode. Note that the assigned HID is only reset to 'b111 on a timed-reset or a power-cycle.

3.5.1.5 Support for ENTDAA and 48-bit Provisional ID

SidebandBus compliance does not need ENTDAA and PID to be supported mandatorily, since the addressing scheme is based on the LID and HID concept as described above. Host bus Controllers on the SidebandBus should be aware of the bus topology and device types through alternate means like enumeration tables and should use SETAASA for dynamic address assignment and mode transition to I3C Basic SDR mode. If ENTDAA is not supported, SidebandBus devices shall NACK them, as with any other unsupported CCCs.

However, note that supporting ENTDAA and PID on SidebandBus devices enable these devices to be used with generic I3C Controllers that may want to use ENTDAA and/or SETNEWDA to re-assign addresses.

A JESD403-1 compliant Target device supporting ENTDAA that intends to be on the Local bus (behind the Hub), must follow the following rules. Please refer to Clause 3.9 on Interoperability considerations.

a. Must support ENTDAA **instead** of SETAASA.
b. These Target devices shall update the Instance_ID field of the 48 bit provisional ID with the HID value received in SETHID CCC.
c. DCR.Device_ID should be "1101_<DTI>". These Device ID values are reserved in MIPI DCR registry for JESD403-1 SidebandBus Standard.

Generic Target devices supporting ENTDAA can seamlessly co-exist with SidebandBus devices that do not support ENTDAA or PID, provided they can support the full dynamic address range. Refer to the enumeration sequence in Section 3.9 on Interoperability considerations.

3.5.1.5 HID Propagation with SETHID (cont'd)

The choice of SETAASA for enumeration is driven by the overall bus discovery and enumeration time with a fully loaded JESD403-1 bus with about 40 devices. It is recommended that all standard Sideband bus devices follow the SETAASA approach to enable bus enumeration with just 2 broadcast commands – SETHID and SETAASA.

3.5.2 Common Command Codes (CCCs)

The I3C Basic specification lists large number of Common Command Codes (CCC). Common command codes that are mandatory for Sideband Bus devices are listed in Table 2. All rules for CCCs documented in I3C Basic Specification are applicable and devices shall ignore all unsupported CCCs.

Note that some devices may have restrictions in cascading different transactions.

CCC is an I3C concept by definition, and shall always conform to I3C SDR timings, irrespective of whether the device has switched from I2C mode or not.

Prior to dynamic address assignment (SETAASA/P), the Target Device(s) may drive the ACK/NACK past the Open Drain SCL rising but before the next SCL falling transition, as a longer overlap in Open Drain is harmless. Immediately after the Open Drain ACK (upon the next SCL falling edge), the bus should transition to push pull mode (though still at 1Mhz) as described in the MIPI I3C Basic Specification V1.0, Section 5.1.2.3 "Handoff from Address ACK to SDR Controller Write Data" and Figure 32 "I3C Data Transfer – ACK by Target".

For additional details on how to handle an the ACK transition, please refer to the MIPI I3C Basic Specification V1.0, Section 5.1.2.3.1 "Transition from Address ACK to SDR Controller Write Data"

A host shall issue a STOP in the following conditions

- Immediately following an ENEC, DISEC, SETAASA, RSTDAA and SETHID CCCs.
- After a CCC operation, before any private device specific Write or Read transactions, and vice versa.
- After any direct CCC, before a broadcast CCC.

A host may use Repeat Start

- Between direct CCC and any other direct CCC
- Between any broadcast CCC and any other broadcast CCC
  Between any private Write or Read operation to any other private Write or Read mode operation.

3.5.2 Common Command Codes (CCCs) (cont'd)

Table 2 — Required CCCs

CCC	Mode	Code	Description	Notes
SETBUSCON	Broadcast	0x0C	Set Bus Context to JEDEC (128 decimal) for generic devices. This is optional for DDR5 components, but mandatory for generic devices that desire to sit on JESD403-1 bus.	
ENEC	Broadcast	0x00	Enable event interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable event interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I2C Mode (Reset dynamic address assignment)	2
SETAASA	Broadcast	0x29	Put the device in I3C Mode (Set all addresses to static address)	
SETHID	Broadcast	0x61	Hub updates 3-bit HID field, updates "T" bit with updated parity calculation for all devices behind hub and stops 3-bit HID translation	1
DEVCTRL	Broadcast	0x62	Configure hub and all devices behind hub	1
Reserved	Broadcast	0x63	Reserved	1
Reserved	Broadcast	0x64	Reserved	1
GETSTATUS	Direct Get	0x90	Get device status	
DEVCAPS	Direct	0xE0	Get device capabilities	1
Reserved	Direct	0xE1	Reserved	1
Reserved	Direct	0xE2	Reserved	1
Reserved	Direct	0xE3	Reserved	1

NOTE 1 JEDEC Specific command
NOTE 2 Direct RSTDAA is not supported since mix bus configuration is not supported. This direct CCC is deprecated in MIPI I3C v1.1 Specification

The following Common command codes are not required to be supported for baseline JESD403-1 Compliance but may **optionally** be supported to claim full compliance to MIPI I3C Specification and enable devices to be used on any generic I3C bus.

- ENTAS[0~3]
- ENTDAA
- SETMWL
- SETMRL
- SETNEWDA
- GETPID, GETBCR, GETDCR
- Any other CCC not specifically stated as supported in the MIPI I3C Basic Specification is not required

All Sideband Bus Target devices shall ignore any unsupported directed CCCs and ignore unsupported / unimplemented broadcast CCCs, in compliance with MIPI I3C Basic Specification. All broadcast CCCs subject to functional usage restrictions, can be issued by Controller / Host in I2C mode, as well, but direct GET/SET CCCs can only be issued in I3C mode (after dynamic address assignment is done).

Please refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of all MIPI standard I3C commands.

The following sub-clauses define the restrictions / customizations for Sideband Bus devices relative to Standard I3C CCCs. For all details of the specific CCCs, please refer to MIPI I3C Specification v1.0.

3.5.2.1 PEC Support for CCCs

If PEC is enabled, all CCCs will have an additional PEC byte, as the last byte of CCC, preceding a STOP or RESTART. If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

SETAASA and SETHID CCCs do not support PEC. PEC needs to be enabled explicitly on devices using the DEVCTRL CCC.

Note that when CCCs are cascaded with restarts, errors from previous transactions (before RESTART) may cause the current transaction to be NACKed.

3.5.2.2 Enable/Disable Events Command (ENEC/DISEC) Operation

The only event type mandatorily supported by SidebandBus devices for ENEC/DISEC Command are **Target Interrupt Requests**. All other event types are not required and ignored. After receiving an ENEC, devices shall be able to initiate IBI transactions either with a START on the bus (initiated by Controller) or when the bus is IDLE for a duration of t_{AVAL} or more.

The host shall end ENEC and DISEC CCC with a STOP, and these CCCs shall be effective on the device on this STOP. It should be noted that while the host can issue a DISEC broadcast when in I2C mode (prior to dynamic address assignment), an ENEC is recommended to be send only after devices are in I3C mode.

Generic devices desirous of complying to JESD403-1 Standard and be used on JEDEC Module Sideband bus must support SETBUSCONTEXT CCC with 128 (JEDEC) as the defining byte. Such devices would have ENHJ/DISHJ and ENCR/DISCR fields valid in this CCC, and the bus Controller/host shall use these fields to disable Hot Join and Controller Request.

Table 3 — ENEC/DISEC CCC (Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x00 (ENEC) / 0x01 (DISEC)								T	
	0	0	0	0	ENHJ / DISHJ *	0	ENCR / DISCR *	ENINT / DISINT	T	P
Note (*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.										

3.5.2.2 Enable/Disable Events Command (ENEC/DISEC) Operation (cont'd)

Table 4 — ENEC/DISEC CCC (Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x00 (ENEC) / 0x01 (DISEC)								T	
	0	0	0	0	ENHJ / DISHJ *	0	ENCR / DISCR *	ENINT / DISINT	T	
	PEC								T	P
NOTE (*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.										

Table 5 — ENEC/DISEC CCC (Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x80 (Direct ENEC) or 0x81 (Direct DISEC)								T	
Sr	DTI				Assigned_HID			W = 0	A	
	0	0	0	0	ENHJ/ * DISHJ	0	ENCR/ * DISCR	ENINT/ DISINT	T	P
NOTE (*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.										

Table 6 — ENEC/DISEC CCC (Direct, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x80 (Direct ENEC) or 0x81 (Direct DISEC)								T	
	PEC(8)								T	
Sr	DTI				Assigned_HID			W = 0	A	
	0	0	0	0	ENHJ/ * DISHJ	0	ENCR/* DISCR	ENINT/ DISINT	T	
	PEC(8)								T	P
NOTE (*) SidebandBus devices ignore HJ (Hot Join) and CR (Control Request) bits.										

3.5.2.3 Reset Dynamic Address Assignment Command (RSTDAA) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the RSTDAA Command.

The Host puts the SidebandBus device in I^2C mode by issuing RSTDAA CCC. When RSTDAA CCC is registered by the device, it resets the dynamic address and as a consequence disables IBI, PEC and Parity Checking. The host shall end this CCC with a STOP, and the CCC shall take effect on the device on the STOP.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Note that MIPI i3C Basic v1.1 Specification deprecates the Direct version of this CCC.

Table 7 — RSTDAA CCC (Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	o	W = 0	A	
	0x06 (Broadcast RSTDAA)								T	P

Table 8 — RSTDAA CCC (Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	o	W = 0	A	
	0x06 (Broadcast RSTDAA)								T	
	PEC(8)								T	P

3.5.2.4 Set All Addresses to Static Address Command (SETAASA) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the SETAASA Command. This command, being a broadcast command, is supported by the SidebandBus devices only when it is operating in I^2C mode; however, it still follows I3C SDR timings compliant to CCC definitions.

As the device is in I2C mode when SETAASA CCC is issued/received, SETAASA CCC does not support PEC function.

Since a mode change is involved, the SETAASA CCC must end with a STOP. The device shall change mode only after the STOP is seen on the bus.

Table 9 — SETAASA CCC (Broadcast)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	o	W = 0	A	
	0x29 (Broadcast SETAASA)								T	P

3.5.2.5 Get Device Status Command (GETSTATUS) Operation

Refer to the I3C Basic Version 1.0 Specification document for details on the encoding and usage of the GETSTATUS Command. This command, being a direct CCC, is only supported in I3C mode.

Table 10 — **GETSTATUS MSB-LSB Format** shows the format of the MSB and LSB sent by the SidebandBus device in response to a GETSTATUS command. When the device completes a GETSTATUS CCC operation, it does not modify any of the status bits within the device.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 10 — GETSTATUS MSB-LSB Format

Bits	Field	Description
15	PEC Error (PEC_ERR)	0 = No Error 1 = PEC Error Occurred This status is cleared by timeout reset. Additional reset mechanisms that are implementation/usage specific may exist.
14:8	Vendor Reserved	Vendor Specific
7:6	Activity Mode	Hard coded to all-zeros.
5	Protocol Error (PROT_ERR)	0 = No Error 1 = Protocol Error; Parity Error Occurred This status is cleared by timeout reset. Additional reset mechanisms that are implementation/usage specific may exist. Note that MIPI I3c Specification compliance requires that this status is self-cleared after a successful read of GETSTATUS. However, JESD403-1 compliant devices, as identified by devices that support DEVCAPS CCC, will NOT self-clear this status on read. This is to ensure that the status does not get lost with GETSTATUS reads with PEC Error and a re-read will provide the correct status.
4	Reserved	Hard coded to zero.
3:0	Pending Interrupt	Indicates the number of pending interrupts. The maximum number of pending interrupts tracked by a Target is device specific and must be documented in its specification. The mechanism to clear this status is also device specific.

Table 11 — GETSTATUS CCC (Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x90 (Direct GETSTATUS)								T	
Sr	DT!3	DTI2	DTI1	DTI0	HID [2:0]			R = 1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	Prot_Err	0	Pending Interrupt				T	Sr or P

3.5.2.5 Get Device Status Command (GETSTATUS) Operation (cont'd)

Table 12 — GETSTATUS CCC (Direct, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0x90 (Direct GETSTATUS)								T	
	PEC(8)								T	
Sr	DTI3	DTI2	DTI1	DTI0	HID[2:0]			R = 1	A	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	Prot_Err	0	Pending Interrupt				T	
	PEC(8)								T	Sr or P

When the device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, Prot_Err, and Pending Interrupt Bits [3:0] do not automatically get cleared. The Host Controller must explicitly clear the appropriate status register through Clear command by writing '1' to corresponding register or by issuing Global Clear command, using DEVCTRL CCC. Once the device clears the appropriate status register, only then will PEC_ERR, Prot_ERR, and Pending Interrupt Bits [3:0] get cleared.

After the host issues a Clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

3.5.2.6 Get Device Capability Command (DEVCAP) Operation

This is a SidebandBus specific command and is only supported by the device when it is operating in I3C mode, since this is a direct CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 13 and Table 14 show the format of the DEVCAP CCC Packet.

Table 13 — DEVCAP CCC (Direct, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0xE0 (Direct DEVCAP)								T	
Sr	DTI				HID [2:0]			R = 1	A	
	MSB (each bit defines capability); 1 = support; 0 = no support								T	
	LSB (each bit defines capability); 1 = support; 0 = no support								T	Sr or P

3.5.2.6 Get Device Capability Command (DEVCAP) Operation (cont'd)

Table 14 — DEVCAP CCC (Direct, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0xE0 (Direct DEVCAP)								T	
	PEC(8)								T	
Sr	DTI				HID = [2:0]			R = 1	A	
	MSB (each bit defines capability); 1 = support; 0 = no support								T	
	LSB (each bit defines capability); 1 = support; 0 = no support								T	
	PEC(8)								T	Sr or P

Table 15 — DEVCAP MSB-LSB Format shows the format of the MSB and LSB sent by a SidebandBus device in response to a DEVCAP command.

Table 15 — DEVCAP MSB-LSB Format

Bits	Field	Description
MSB[7]	GETBCR CCC Support	Return 1 if device implements GETBCR, else 0.
MSB[6]	GETDCR CCC Support	Return 1 if device implements GETDCR, else 0.
MSB[5]	SETMRL CCC Support	Return 1 if device implements SETMRL, else 0.
MSB[4]	SETMWL CCC Support	Return 1 if device implements SETMWL, else 0.
MSB[3]	GETPID CCC Support	Return 1 if device implements GETPID, else 0.
MSB[2]	Timer Based Reset	Return 1 if device implements timed-reset, else 0.
MSB[1]	Reserved	Reserved
MSB[0]	Reserved	Reserved
LSB[7:0]	Reserved	Reserved

3.5.2.7 Set HID Command (SETHID) Operation

This is a SidebandBus specific command and supported by the device even when it is operating in I^2C mode. The host shall send this CCC at a speed not exceeding 1 MHz to ensure error probability is minimized. The host may send SETHID multiple times before dynamic address is assigned and bus is moved to I3C mode. The host shall not issue this CCC in I3C Mode of operation (after dynamic address is assigned).

The host sends the CCC with HID[2:0] set to 'b000 (all other bits in this byte shall be zeros, as indicated in CCC format below), and the hub shall replace this field with the detected HID. Upon receiving SETHID Command, the SidebandBus device will update the static-address' LSB 3 bits with the HID[2:0] bits it received in the SETHID command packet.

As the device is in I2C mode when SETHID CCC is issued, SETHID CCC does **not** support PEC function.

Since this CCC involves address assignment, host shall always end SETHID CCC with a STOP.

Table 16 — SETHID CCC (Broadcast)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	o	W = 0	A	
	0x61 (Broadcast SETHID)								T	
	0	o	o	o	HID[2:0]			o	T	P

3.5.2.8 Configure SPD-Hub and All Devices Behind Hub Command (DEVCTRL) Operation

On a typical I^2C or I3C Basic bus there can be up to 120 devices. For certain operations such as selecting the I3C Basic Bus mode of operation or to enable or disable functions that are common to all devices such as Packet Error Check, the host must go through one device at a time which takes a significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak a different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I2C mode, it is recommended to limit this CCC to 1 MHz operation to minimize error probability and guarantee that the device has registered this command. Table 17 to Table 18 show examples of DEVCTRL CCC command packets.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W = 0 byte in PEC calculation.

The host shall follow any device imposed register access restrictions when DEVCTRL CCC is used to access device specific registers (i.e., RegMod = '1'). For example, if device specific register requires STOP operation for device to take in the effect of the setting, the host must use STOP operation when using DEVCTRL CCC to access device specific register.

3.5.2.8 Configure SPD-Hub and All Devices Behind Hub Command (DEVCTRL) Operation (cont'd)

Table 17 — DEVCTRL Command Operation (Broadcast, PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0	1	1	0	0	0	1	0	T	
	AddrMask[2:0]			StartOffset[1:0]		0	0	RegMod	T	
	DevID[6:0]							W = 0	T	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr or P

Table 18 — DEVCTRL Command Operation (Broadcast, PEC Enabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0	1	1	0	0	0	1	0	T	
	AddrMask[2:0]			StartOffset[1:0]		PEC_BL		RegMod	T	
	DevID[6:0]							0	T	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC(8)								T	Sr or P

3.5.2.8 Configure SPD-Hub and All Devices Behind Hub Command (DEVCTRL) Operation (cont'd)

Table 19 — DEVCTRL Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Uni-cast or Multi-cast Command Selection 000 = Uni-Cast Command; Target device responds if DevID[6:0] field matches with Target device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multi-Cast Command; Target and possible other device responds if DevID[6:3] field matches with Target's own 4-bit LID address 111 = Broadcast Command; All devices respond to this command All other encodings are reserved
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte. (Byte 0 or Byte 1 or Byte 2 or Byte 3) in DEVCTRL command data packet. Host can start any Byte and can have continuous access to next byte until STOP operation. When Byte 3 is reached, host shall issue a STOP. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC_BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for the DEVCTRL command data packet. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL command is going to be used for device specific offset register or general registers as identified in Byte 0 to Byte 3. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e., StartOffset[1:0] = Valid) 1 = End Device Specific Offset Address (the exact definition of this usage is device/implementation specific.). The host shall not use RegMod = '1' with Broadcast Command for bus configurations with different types of devices on the I3C bus, like DDR5.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL command data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a do not care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is do not care. For any other codes for AddrMask[2:0], the device always NACKs.

3.5.2.8 Configure SPD-Hub and All Devices Behind Hub Command (DEVCTRL) Operation (cont'd)

Table 20 — DEVCTRL Command Definition

Byte	Bit	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable[1]	
	[6]	Parity Disable	0 = Enable 1 = Disable[1]	
	[5]	RFU	RFU	
	[4:2]	RFU	RFU	
	[1]	RSVD - Reserved	X (0 or 1) = No action	
	[0]	RFU	RFU	
Byte 1	[7:5]	RFU	RFU	
	[4]	RFU	RFU	
	[3]	Global and IBI Clear	0 = No action 1 = Clear All Event and pending IBI[1,2]	Clears Pending Interrupt, PEC_Err and Parity_Err flags reported in GETSTATUS.
	[2]	RFU	RFU	RFU
	[1:0]	RFU	RFU	
Byte2	[7:0]	RFU	RFU	
Byte 3	[7:4]	RFU	RFU	
	[3:1]	RFU	RFU	
	[0]	RFU	RFU	

NOTE 1 Global Clear, PEC Enable, and Parity Disable only applicable after device is configured in I3C Bus mode.
NOTE 2 After Target device clears all events, it can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.
NOTE 3 RFU is "For Future Use"; RSVD is used by some devices and must be ignored.

3.5.2.9 SETBUSCON CCC

This CCC shall be supported by generic devices desirous of fine tuning their capabilities to meet the limitations and additions with respect to MIPI I3C Specification, as defined in this JESD403-1 Specification.

Standard DDR5 components that are naturally compliant to the requirement in this standard may NACK this CCC.

PEC is not supported for this CCC, since this CCC will be used by host/Controller as one of the very first configuration CCCs in I2C mode, before issuing SETHID and SETAASA. It is recommended that this CCC ends with a STOP.

Table 21 — SETBUSCON CCC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W = 0	A	
	0	0	0	0	1	1	0	0	T	
	JEDEC CONTEXT = 128 decimal								T	P

3.5.3 In Band Interrupts

In-Band interrupts is generated by the SidebandBus device if IBI is enabled with a broadcast or directed ENEC CCC, and device has a pending interrupt to be send. In I^2C mode, the in-band interrupt function is not supported; only I3C Basic Bus mode supports the in band interrupt function.

By default, all interrupt sources are disabled (i.e., set to '0'). The host may enable interrupts in the SidebandBus device. Once enabled, the device sends an IBI when that event occurs.

The cause of IBI generation and the exact format for the payload bytes is implementation or device specific and is documented in the corresponding device spec.

Interrupt arbitration is fully compliant with MIPI i3C Specification, with the lowest address winning. Arbitration is between devices for generated IBIs and also with the Target address of the Controller-initiated transactions.

The mechanics of IBI generation, including the arbitration mentioned above, is fully compliant with the I3C Basic Specification. Please refer to the MIPI I3C Basic specification for more details on IBI.

The MDB value shall always be 0x00, and additional payload bytes can be present.

IBI Re-transmission

SidebandBus devices may retransmit IBIs, which were partially accepted by the host (using the T-bit); until IBI is disabled with DISEC or interrupt sources cleared using device specific interrupt clear bits. The policy for determining when to re-transmit, like usage of hysteresis or delays, is usage dependent and beyond the scope of this standard.

Clearing Status Registers

Clearing interrupt status is beyond scope of the MIPI I3C Basic Specification and is implementation specific.

3.6 Transaction Types

Every register access transaction into a SidebandBus device starts with a START, an optional 0x7E broadcast address and ends with a STOP. Back to back Write transactions can be cascaded with a RESTART. For reads, a RESTART indicates the beginning of the read phase and an unsuccessful read is always terminated by host with a STOP. It should be noted that in alignment with I3C Specification, CCCs could also be cascaded with these read/write transactions using RESTARTs, subject to limitations described in this document and in CCC definitions.

Each register access transaction has an N-byte address phase and an M-byte data phase. The precise value of M and N is device specific. All I3C Bus data are transmitted with the most significant bit MSB first.

In full compliance with the MIPI I3C Basic Specification, for all transaction formats below, only the first byte after start (optional 0x7E or Target Address) is in open-drain mode for arbitration, in addition to the ACK/NACK bit. The T-bit for writes is Parity and for reads is the transition bit as documented in the MIPI I3C Basic Specification. A SidebandBus device detecting a parity error on any byte may disregard the rest of the transaction.

Table 22 — Write Transaction Format, without 0x7E

S / Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
	DataByte 0			T=Par	
	…			T=Par	
	DataByte M-1 / PEC (optional)			T=Par	P / Sr

Table 23 — Write Transaction Format, with 0x7E

S	0x7E		RnW=0	ACK	
Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
	DataByte 0			T=Par	
	…			T=Par	
	DataByte M-1 / PEC (optional)			T=Par	P / Sr

The optional 0x7E broadcast address at the beginning of the transaction enables any pending IBIs to be arbitrated against a host generated transaction.

3.6 Transaction Types (cont'd)

Table 24 — Read Transaction Format, without 0x7E

S / Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
Sr	DTI[3:0]	HID[2:0]	RnW=1	ACK	
	DataByte 0			T	
	…			T	
	DataByte M-1 / PEC (optional)			T	P / Sr

Table 25 — Read Transaction Format, with 0x7E

S	0x7E		RnW=0	ACK	
Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
Sr	DTI[3:0]	HID[2:0]	RnW=1	ACK	
	DataByte 0			T	
	…			T	
	DataByte M-1 / PEC (optional)			T=0	P / Sr

For a read transaction, the device may NACK the read portion of the transaction as indicated below until the response data is available/ready. The host is required to retry just the read portion, until the device ACKs the read.

Table 26 — Read Transaction Format, without 0x7E, with Host Retries

S / Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	
Sr	DTI[3:0]	HID[2:0]	RnW=1	ACK	
	DataByte 0			T	
	…			T	
	DataByte M-1 / PEC (optional)			T=0	P / Sr

3.6 Transaction Types (cont'd)

Table 27 — Read Transaction Format, with 0x7E and Host Retries

S	0x7E		RnW=0	ACK	
Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	
Sr	DTI[3:0]	HID[2:0]	RnW=1	ACK	
	DataByte 0			T	
	…			T	
	DataByte M-1 / PEC (optional)			T=0	P / Sr

The host may put a limit to no. of retires and terminate the read transaction with a STOP.

Table 28 — Unsuccessful Read Transaction Format, without 0x7E, with Host Retries

S / Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	P

Table 29 — Unsuccessful Read Transaction Format, with 0x7E and Host Retries

S	0x7E		RnW=0	ACK	
Sr	DTI[3:0]	HID[2:0]	RnW=0	ACK	
	AddressPhase-Byte0			T=Par	
	…			T=Par	
	AddressPhase-ByteN-1			T=Par	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	
Sr	DTI[3:0]	HID[2:0]	RnW=1	NACK	P

3.6.1 Parity Error Checking

By default, when a device is put in I3C mode, parity function is automatically enabled. The host can disable the function with DEVCTRL CCC. When parity function is disabled, the device simply ignores the "T=Par" bit information from the Host. The host shall always send the parity on the T-bit for writes.

Per the MIPI I3C Specification, all devices shall implement ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'. If even number of bits in the byte are '1', the parity bit value is '1'.

3.6.2 PEC Support

The optional appended PEC on the data stream covers the information transmission between the host and a Target device.

If the optional I3C broadcast address (7'h7E and W = 0) is present, SidebandBus devices will exclude it in its PEC calculation. Other than that, all devices will include all bytes, including the address byte, in its local PEC generation/checking logic.

All SidebandBus devices implement an 8-bit Packet Error Code (PEC) which is appended at the end of all I3C Bus transactions if PECs are enabled through DEVCTRL CCC.

The PEC is a CRC-8 value calculated on all the message bytes excluding START, Repeat START, STOP, T-bits, ACK, NACK, and IBI header (7'h7E followed by W = 0) bits. The algorithm for all CRC-8 calculations is as follows and the seed value is 0x0.

$$C(x) = x^8 + x^2 + x^1 + 1$$

PECs are disabled by default on power up or RESET. The host may optionally enable PEC function using DEVCTRL CCC. If enabled, the host must complete the burst length (or byte count) as indicated. In other words, the host must not interrupt the burst length (or byte count) prematurely for Write or Read operation. It is considered an illegal operation, and devices shall recover from the error condition with a STOP.

3.7 Error Handling

- Error detection required in I3C Basic Mode:
  - TE1 (recovery through STOP only, not through EXIT-HDR pattern or timeout)
  - TE2
- Error detection not required:
  - TE0
  - TE3
  - TE4
  - TE5

3.7.1 I2C Mode Error Handling

The I^2C Bus Target interface handles two types of errors: internal and PEC. These errors manifest as a Not-Acknowledge (NACK) for the read command (End bit is set). If an internal error occurs during a configuration write, the final write command receives a NACK just before the stop bit. If the Controller receives a NACK, the entire configuration transaction should be retried.

3.7.2 Error Handling in I3C Mode

There are two types of error checking done by the SidebandBus devices. I3C Bus Parity error checking and Packet Error checking. By default, the parity error checking is always enabled (in I3C Bus mode) and packet error checking is disabled. The Host may enable the packet error checking at any time. The parity error is calculated for each byte. The packet error is computed for the entire packet. The Host sends parity error information in "T" bit.

I3C Basic defines TE0, TE1, TE2, TE3, TE4, TE5, TE6 and CE0, CE1, CE2 errors. Only TE1 and TE2 errors are supported by SidebandBus devices. All other errors are not supported and not applicable.

3.7.2 Error Handling in I3C Mode (cont'd)

A parity error shall be reported in GETSTATUS's Protocol Error bit (#5) and a Packet Error Check (PEC) Error shall be reported in GETSTATUS's PEC_ERR bit (#15). In both cases, pending interrupt in GETSTATUS shall be incremented. Devices may choose to support only 1 pending interrupt.

Devices shall ignore/discard transactions with a Parity error or a PEC Error, until STOP. Note that this essentially means that TE2 and TE3 error exit conditions are limited to just STOP. (This implies timeout and HDR-EXIT patterns are excluded from TE1 error exit and repeated-start is excluded from TE2 error exit).

3.8 Bus Clear

JESD403-1 compliant devices support the following described Bus Clear capability in I2C mode only. This bus clear method cannot guarantee bus clear of a device on the bus that is in I3C mode.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the Target device is in the middle of outputting data for read operation. For these events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

3.9 Interoperability Considerations

JESD403-1 bus is fine tuned to specific usages of the MIPI I3C Specification. To ensure interoperability between different kinds of devices, the SETBUSCON CCC (incorporated in MIPI I3C v1.1 Specification) may be used, as follows.

A generic MIPI-I3C Specification compliant device **may** support a CONTEXT value of 128 for the SETBUSCON CCC, to suit itself to be used on a JESD403-1 bus. The CONTEXT value of 128 reserved in MIPI BUSCONTEXT registry for JEDEC JESD403-1 bus. When SETBUSCON broadcast CCC is received with a value of 128, Target device shall do the following.

A. Support ALL Dynamic Addresses [Reserved address per MIPI I3C Spec will be used on JESD403-1 bus].
B. Masks TE0 Error
C. Masks TE2 error exit on RESTART
D. Disable IBI by clearing internal IBI-Enable flag (Need explicit ENEC to enable IBI again).
E. Will Disable IBI (clear internal IBI-Enable) when a RSTDAA is received.
F. Partially accepted IBIs will be re-transmitted, in the next opportunity. The delay for re-transmission is usage specific and beyond the scope of the MIPI-I3C/JESD403-1 Standard.

A JESD403-1 compliant device **may** choose to support ENTDAA instead of SETAASA. The following rules should be followed by such devices.

A. SETAASA must NOT be supported.
B. Must support ENTDAA scheme w/PID, BCR, and DCR

3.9 Interoperability Considerations (cont'd)

C. If the device intents to be on the JESD403-1 local bus (behind the hub), it must support the following for Address assignment
    1. These Target devices shall update the PID.INST_ID field with the HID value received in SETHID CCC.
    2. DCR.Device_ID should be "1101_<DTI>". These Device ID values are reserved in MIPI DCR registry for JESD403-1 bus Specification.
D. To sit on the host bus (before the hub), these devices must support the full range of dynamic addresses (0-127), with no address values reserved. Note that the host must pick a value that does not conflict with the DTI, HID combinations for all devices on local bus in this configuration. [TE0 error must be masked].
E. Must support TE3, TE4 error detection.
F. May support additional CCCs, as documented in I3C Specification.

3.9.1 Types of Devices

Based on the above, there can be 3 types of devices.

1. **JESD403-1** device: Device strictly implementing JESD403-1 mandated requirements, nothing more. Such devices ***may*** support SETBUSCONTEXT=JEDEC and use SETAASA only.
2. **JESD403-1+** device: A device that supports SETBUSCONTEXT=JEDEC, with ENTDAA instead of SETAASA, as described above with DTI/HID based DCR and INST_ID and sits on the local bus behind a HUB.
3. **Generic** device: A device that supports SETBUSCONTEXT=JEDEC but does **not** recognize HID/DTI based DCR/INST_ID assignments.

3.9.2 Discovery and Enumeration with Different Types of Devices

Table 30 describes the bus discovery and enumeration process for a bus that will instantiate all the above kinds of devices.

Table 30 — Interoperability Considerations

Step #	Host / Controller Action	Dedicated JESD403-1 device [JESD403-1]	Full I3C Compliant JESD403-1 Device [JESD403-1+]	Generic I3C Device [GENERIC]
1	Issue SETBUSCONTEXT=JEDEC broadcast	Ignores/NACKs	ACKs and does the following: - Disables IBI and PEC (Need explicit ENEC to enable IBI again). - Masks TE0 Error - Masks TE2 error exit on RESTART - Partially accepted IBIs will be re-transmitted	
2	Issue DISEC broadcast (to cover short-term disconnects) can be removed in future versions) (Note 4)	Disables IBI	Disables IBI	Disables IBI
3	Issue SETHID broadcast	SA updated w/HID	SA and PID.INST_ID updated with HID	NACKs
4	Use SETDASA to assign DA to any device with ‘known’ SA, for generic (non-JESD403-1) devices. DA value should be outside of JESD403-1’s {DTI,HID} range.	NA	NA	DA assigned
5	Issue ENTDAA until NACK’ed to discover all devices supporting ENTDAA	NACK	ACK w/DCR = JEDEC, INST_ID=HID	ACK w/other INST_ID, HID
6	Controller assigns DA for each ENTDAA device	NA	Host assigns DA based on DCR and INST_ID	DA assigned. Host ensures value is outside of JESD03’s {DTI,HID} range.
7	Issue SETAASA broadcast Host may issue this CCC multiple times to overcome any parity error concerns.	DA assigned	DA assigned, if not already	DA assigned, if not already
8	Issue ENEC(broadcast or direct), if and as required	Enable IBI	Enable IBI	Enable IBI

3.9.2 Discovery and Enumeration with Different Types of Devices (cont'd)

The following should be noted.

1. SPD-Hub must send ENTDAA and broadcast CCCs always across host and local bus, if not generic devices must be limited to host bus, and not local bus.
2. Same sequence to be followed on power-on-reset; after issuing a timed-reset (for in-band-reset) or after issuing RSTDAA (from step#4)
3. It is recommended that the Controller follows slower/OD speeds (1 MHz) timing even for CCCs, until (including) SETAASA is completed. Duplicate CCCs may also be issued.
4. JESD403-1 does not support HJ, Sec Controller. A generic I3C device may support these capabilities, and the host would need to disable it during bus configuration with DISEC.

3.10 Multi-Controller Usages

JESD403-1 compliant devices may be used in a simplistic multi-Controller environment through the following process. Only one of the Controllers may **own** the bus (generate transactions) at a time.

Bus ownership handover is negotiated through back/side channels and is beyond the scope of this standard. When the bus is handed over, all devices are handed over in I2C/open-drain mode with PEC and IBI disabled. The devices however retain the assigned static address.

The following steps would be done by the relinquishing and new Controllers.

- Relinquishing Controller, when ready to handover
    - Issues (**optional**) DISEC broadcast to disable IBI
    - Issues (**optional**) DEVCTRL broadcast to disable PEC
    - Issues RSTDAA broadcast to remove DA, back to I2C/OD mode, IBI and PEC is disabled.
- New Controller must now re-enumerate and assign dynamic address to all devices.
    - If only dedicated-JESD403-1 devices are present on the bus
        - DISEC, SETAASA, ENEC (if and when required) – in that order
    - If generic I3C device exists on the bus, [DA needs to be assigned to all]
        - DISEC, **SETDASA, ENTDAA**, SETAASA, ENEC – in that order
    - Goes through full initialization and bus enumeration
        - Timed-reset, SETBUSCON=JEDEC, DISEC, SETHID, SETDASA, ENTDAA, SETAASA, ENEC (if and when required) – in that order.

4 Hub Architecture

The SidebandBus architecture uses a hub device to isolate the main (host) bus and one or more local buses, as shown in Figure 3.

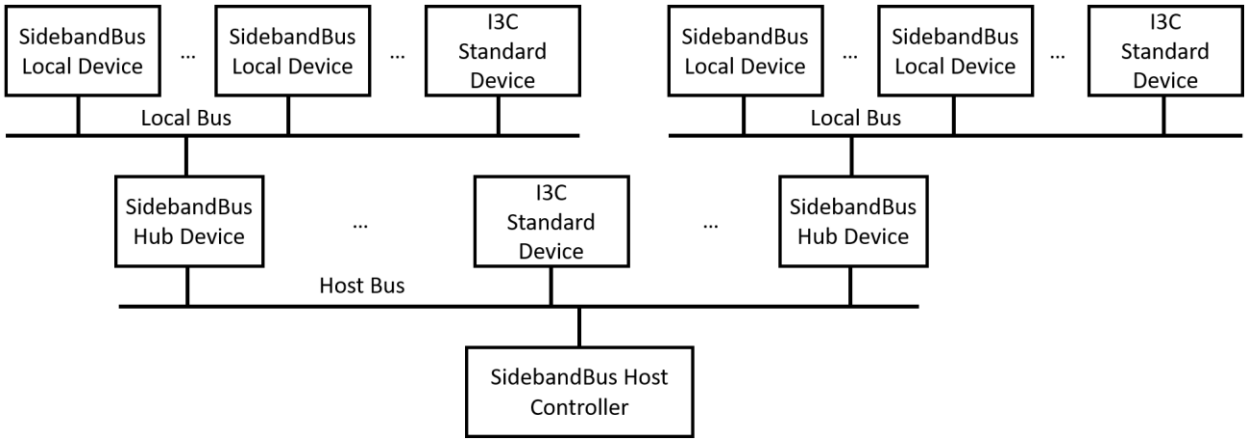


Figure 3 — SidebandBus Topology with Host Bus and Local Buses

SidebandBus uses a broadcast mechanism that detects and manipulates the least significant three bits of a device address in order to expand the address range of the overall bus. The SidebandBus architecture assigns specific static addresses for all JEDEC standard devices. These static addresses become the initial dynamic address of the device as well when the SETAASA common command code is issued.

The SPD-Hub Device monitors the LID code. When it detects the Host access is for the Target device, it compares the last 3 bits of the HID information coming from the host against its own unique HID code that it has stored at power on. It compares each 3 bits one at a time. If there is a match, the SPD device substitutes that bit with ‘1’ and forward it to the local device interface. If there is a mis-match, the SPD device substitutes that bit with ‘0’ and forwards it to the local device interface. As a result, only the targeted local device will see its last three HID bits as ‘111’ and all non-targeted local devices will see its last three HID bits as anything other than ‘111’ which is not a valid code.

Figure 4 gives an example of Host accessing local RCD Device on DIMM0. Figure 4 shows Host sends 7-bit address 1011 000. Each SPD hub device receives this address. Each Hub device forwards the first four bits of binary address ‘1011’ (LID) on the local device interface. Each Hub compares last 3 bits of binary address ‘000’ from the host against its own unique HID code and substitutes the bit on the local device interface.

4 Hub Architecture (cont'd)

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58

Figure 4 — Example Addressing of a DIMM-Specific SidebandBus Devices

Use of Reserved I3C Addresses

The SidebandBus implementation of HID/LID address mechanisms can cause potential address conflicts with certain reserved I3C addresses. Specifically, the addresses 101 1110 and 110 1110 are reserved in I3C Basic for broadcast address single bit error detection. Potential devices in a DIMM slot 6 (RCD/MRCD/CKD and PMIC2, respectively) use these reserved addresses for normal operation. Host controllers must be aware of these potential conflicts for testing or runtime use.

4.1 Local Bus Power

SidebandBus hubs require two external power supplies, VDDSPD and VDDIO, typically provided on a memory module by a separate PMIC voltage regulator. VDDSPD is nominally 1.8 V, and VDDIO is nominally 1.0 V. Figure 5 shows these connections between devices.

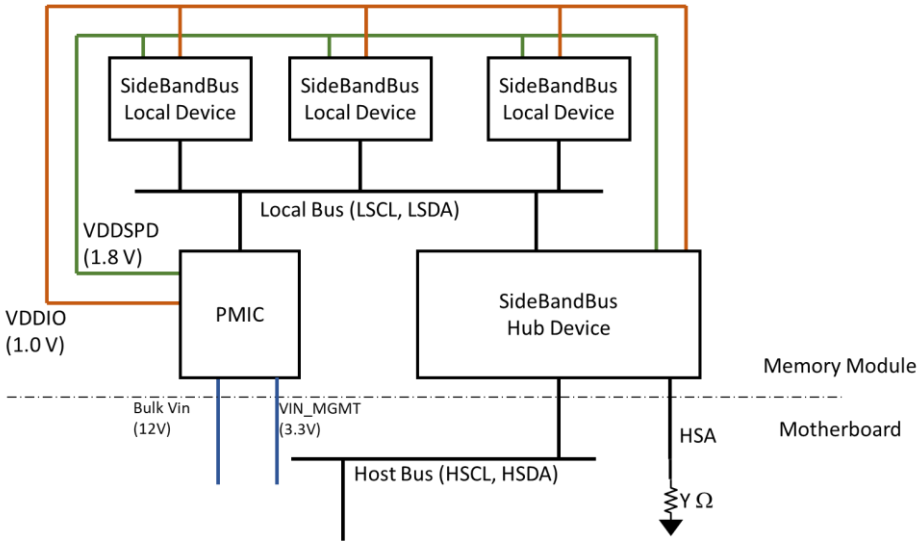


Figure 5 — Bus Power Connections

Sideband Bus communication initially begins in I2C mode which is an open drain protocol running at a maximum speed of 1 MHz. When the host assigns dynamic address to bus devices, the I/Os switch to I3C-SDR mode, a combination of open drain and push-pull modes operating at max of 12.5 MHz.

In open drain mode, the JESD403-1 hub devices provide current source pull-ups to VDDIO on the LSDA signal. The LSCL signal is always operated in push-pull mode. Figure 6 shows these I/O drivers and the location of the pull-up current source.

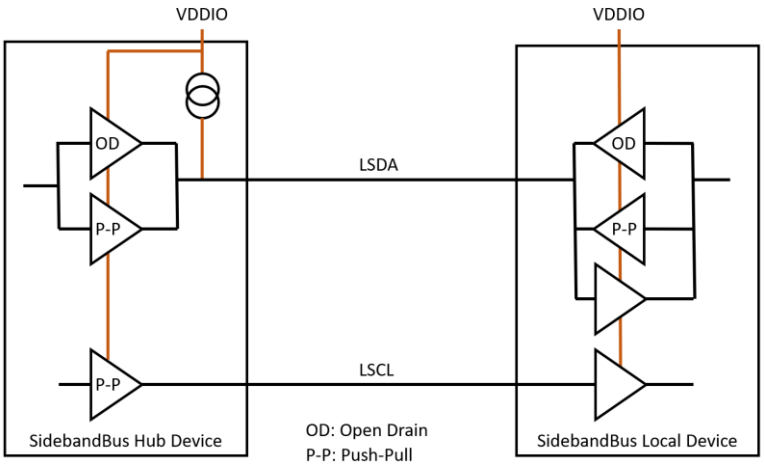


Figure 6 — Hub and Local Device I/O Drivers

4.1 Local Bus Power (cont'd)

For standard SidebandBus implementations, no external pull-up resistors are required on SidebandBus clock or data signals. However, SidebandBus may be used in some non-standard configurations.

One example is where some non-standard devices may require an I/O voltage on the local bus higher than 1.0 V. This configuration is allowed using external pull-up resistors on the LSCL and LSDA to the non-standard I/O voltage. All standard SidebandBus devices continue to operate at the 1.0 V local bus levels; i.e., VIL and VIH are not affected by this mode of operation. The Hub must be programmed to disable its internal current source on the local bus signals and operate in open drive mode only. Any time an I/O voltage other than 1.0 V is used, I3C-SDR mode is not supported, and the bus must operate in I^2C mode only. As shown in Figure 7, VDDSPD and VDDIO are supplied to all standard components, however the non-standard device may use VDDSPD, VDDIO or the non-standard voltage labelled VDDLB. The supplies that are required by the non-standard device is beyond the scope of this document.

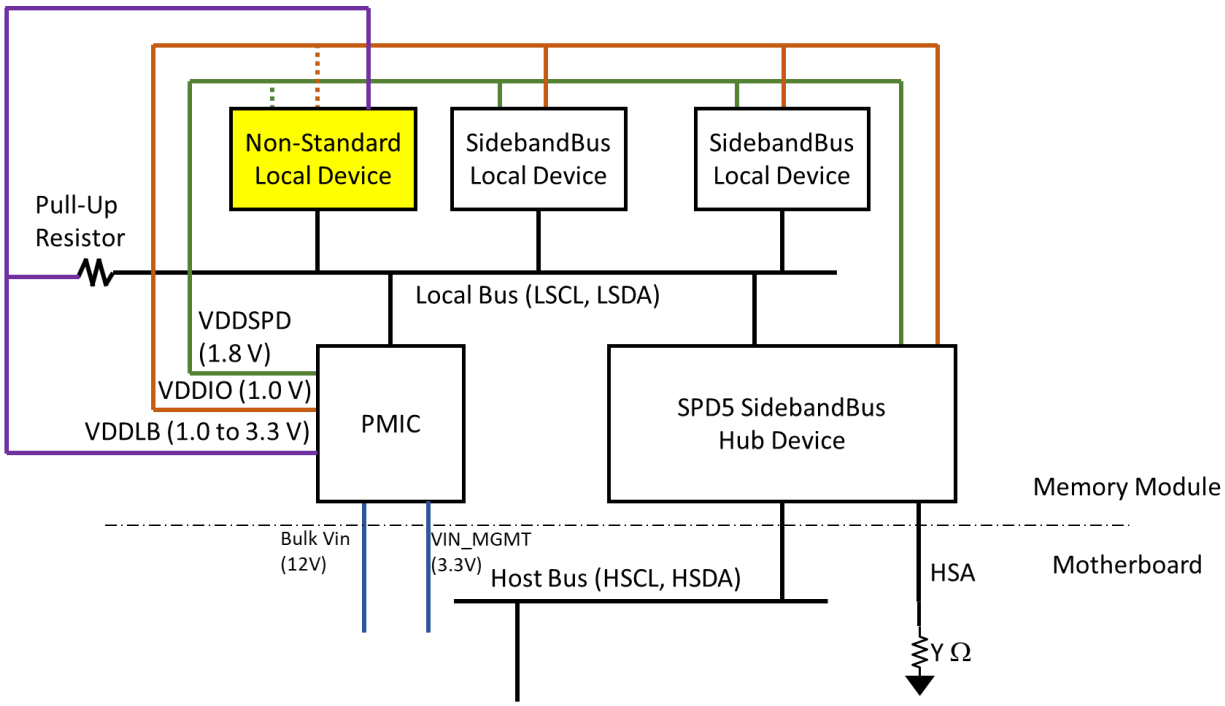


Figure 7 — Non-Standard Devices on SidebandBus Local Bus

Another non-standard configuration allowed by SidebandBus is a non-standard voltage on the Host bus. In this configuration, the Host controller disables its internal current source and uses external pull-up resistors to the non-standard I/O voltage on the Host bus signals HSCL and HSDA. The Hub device I/O levels remain unchanged; i.e., V_{IL} and V_{IH} operate as 1.0 V compatible signals. In this configuration, the Host bus operates in I^2C mode only. I3C-SDR mode is not supported.

The I/O voltage on the Host bus and the Local bus are not required to be the same level. These non-standard configurations may be mixed. For I3C-SDR mode to be used, however, both Host and Local buses must be operated at 1.0 V.

4.2 Device Map

The JEDEC standard SidebandBus devices are listed in Table 31and Table 32.

4.2.1 Hub Devices

Table 31 — SidebandBus Hub Device Addresses

Standard	Device Type (DTI)	Host ID	Marketing Designator	Description
JESD300-5	1010	000 – 111	SPD5118	DDR5 SPD with Hub and thermal sensor, 8 Kb of non-volatile memory
	1010	000 – 111	SPD5108	DDR5 SPD with Hub and no thermal sensor, 8 Kb of non-volatile memory
JESD303-1	0100	000 – 111	DMB501	Differential DIMM memory buffer, first buffer
	0101	000 – 111	DMB501	Differential DIMM memory buffer, second buffer

4.2.2 Local Bus Devices

Table 32 — SidebandBus Local Bus Device Addresses

Standard	Device Type (DTI)	Local ID	Marketing Designator	Description
JESD82-511	1011	111	DDR5 RCD01	DDR5 registering clock driver
JESD301-1	1001	111	PMIC5000	DDR5 voltage regulator for high powered servers, first PMIC
			PMIC5010	DDR5 voltage regulator for low powered servers, first PMIC
			PMIC5100	DDR5 voltage regulator for client systems, first PMIC
	1000	111	PMIC5000	DDR5 voltage regulator for high powered servers, second PMIC
			PMIC5010	DDR5 voltage regulator for low powered servers, second PMIC
			PMIC5100	DDR5 voltage regulator for client systems, second PMIC
	1100	111	PMIC5000	DDR5 voltage regulator for high powered servers, third PMIC
			PMIC5010	DDR5 voltage regulator for low powered servers, third PMIC
			PMIC5100	DDR5 voltage regulator for client systems, third PMIC
JESD302-1	0010	111	TS5111	DDR5 thermal sensor, first sensor, wide voltage range
	0110			DDR5 thermal sensor, second sensor, wide voltage range
	0010		TS5110	DDR5 thermal sensor, first sensor, narrow voltage range
	0110			DDR5 thermal sensor, second sensor, narrow voltage range

5 Electrical Characteristics

The SidebandBus electrical characteristics allow for a 1.0 V I/O interface, which is described here in detail. For 1.8 V and 3.3 V details, please refer to MIPI I3C Basic Specification v1.0.

The I3C IO utilizes a combination of push-pull drivers and open drain modes where the host controller supplies active pull-up on the host bus and the hub provides active pull-up on the local bus. Parameters are shown in Table 33.

Table 33 — DC Electrical Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Comments
VDDIO	Input Supply Voltage		0.95	1.0	1.05	V	
I_{LI}	Input leakage current		--		+/- 5	µA	
I_{LO}	Output leakage current		--		+/- 5	µA	
V_{IL}	Input low voltage	--	-0.3		0.3	V	
V_{IH}	Input high voltage	--	0.7		1.05	V	Devices that implement and intent to work on legacy I2C buses, shall meet 1.8 V and 3.3 V as documented in MIPI I3C Specification and the same should be documented in the component/device data sheets.
V_{OL}	Output low voltage		--		0.3	V	
V_{OH}	Output high voltage		0.75		-	V	
I_{OL}	Output low current - HSDA, LSDA, LSCL	V_{OL} = 0.3 V	3		-	mA	
I_{OH}	Output High current - HSDA, LSDA, LSCL	V_{OH} = VDDIO - 0.3 V	-		-3	mA	
Slew_Rate	Output Slew Rate (HSDA, LSDA, LSCL)	See NOTE 1	0.1		1.0	V/ns	This is with reference to reference load of 50 Ohm resistive load.

NOTE 1 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 8 and Figure 9 shows the timing measurement points. For slew rate measurements, the V_{OH} level shown in Figure 9 is a function of R_{ON} value; $V_{OH} = \{1.1/(R_{on} + 50)\} * 50$.

5 Electrical Characteristics (cont'd)

Table 34 — Output Ron Spec

Symbol	Parameter	Min	Max	Units	Notes
R_{ON}	HSDA, LSCL, LSDA Output Pullup and Pulldown Driver Impedance	20	100	Ohm	1
NOTE 1 Pulldown $R_{ON} = V_{OUT}/I_{OUT}$; Pullup $R_{ON} = (V_{IO} - V_{OUT})/I_{OUT}$.					

Table 35 — Input Parameters

Symbol	Parameter [1,2]	Test Condition	Min	Max	Units
C_{IN}	Input capacitance (HSDA, HSCL, LSDA)	--	--	5	pF
t_{SP}	Pulse width of spikes which must be suppressed by the input filter in I^2C mode. See Note 3.	Single glitch, f < 100 KHz	--	--	ns
		Single glitch, f >= 100 KHz	0	50	
NOTE 1 T_A = 25 °C, f = 400 kHz. NOTE 2 Verified by design and characterization, not necessarily tested on all devices. NOTE 3 Spike filter is optional, and if implemented will be active only in I2C mode. Spike filter shall be permanently disabled on receiving SETAASA CCC. Specifically, I3C OD mode does not have spike filter.					

6 Timing Parameters

The SidebandBus is designed to support 1 MHz operation in I2C mode on power up, and up to 12.5 MHz data transfer rates in I3C Basic mode once initialized.

Note that the equivalent MIPI I3C Specification timing symbol is in braces.

6.1 Test Load and ATE Measurement Methodology

For ATE tests, all IO timing (e.g., t_{DOUT}, also known as t_{SCO}) is based on a resistive reference load of 50 ohms. This test condition is only for compliance testing of devices.

Note that JEDEC t_{DOUT} definition is similar as $t_{SCO,}$ since with a resistive load measurement, $t_R = t_F = \sim 0$.

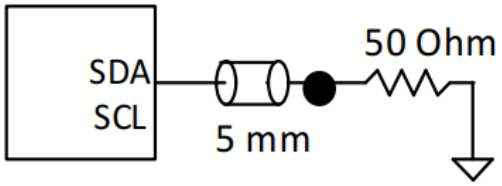


Figure 8 — Output Slew Rate and Timing Reference Load

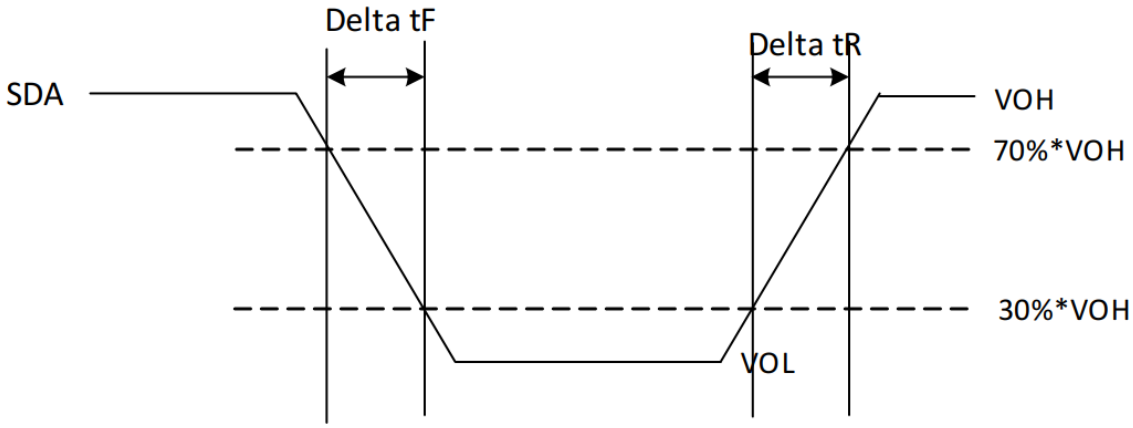


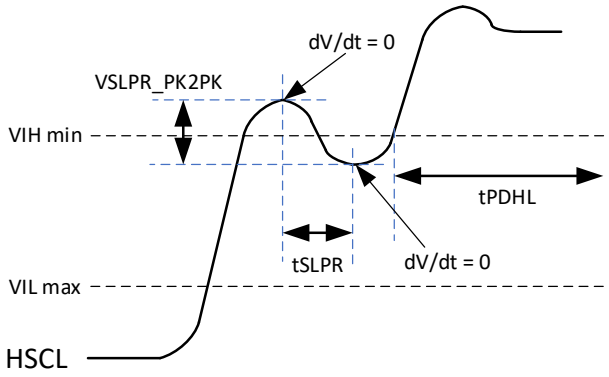
Figure 9 — Output Slew Rate Measurement Points

HSCL Monotonicity

Due to non-deterministic loading (number of DIMMs populated) on an unterminated bus, there can be reflections on the bus causing slope reversal on the HSCL signal on the input receiver of the SPD5 HUB.

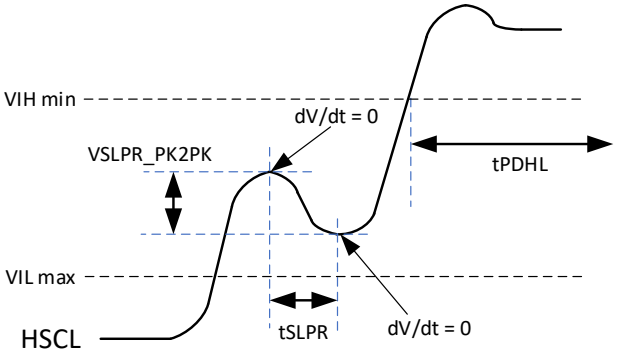
The SPD5 Hub device must tolerate tSLPR and tSLPR_PK2PK slope reversal on HSCL in I3C mode as shown in Figures 10 through 12 and defined in Table 36.

6.1 Test Load and ATE Measurement Methodology (cont'd)



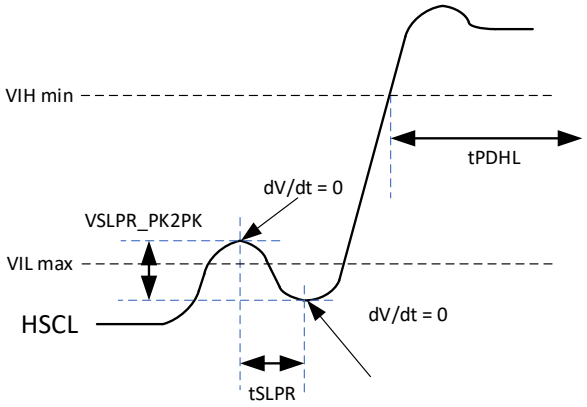
Note: tPDHL is for reference only in this diagram, refer to measurement methodology for details on this parameter.

Figure 10 — Slope Reversal on HSCL at VIH



Note: tPDHL is for reference only in this diagram, refer to measurement methodology for details on this parameter.

Figure 11 — Slope Reversal on HSCL between VIL and VIH



Note: tPDHL is for reference only in this diagram, refer to measurement methodology for details on this parameter.

Figure 12 — Slope Reversal on HSCL at VIL

6.1 Test Load and ATE Measurement Methodology (cont'd)

Table 36 — Slope Reversal

Symbol	Parameter	Min	Max	Units	Note
t_{SLPR}	Pulse width of slope reversal which must be suppressed[1]	0	2.6	ns	1
SLPR_PK2PK	The peak to peak voltage of slope reversal which must be suppressed	0	150	mV	1
NOTE 1 These parameters apply in I_3C mode.					

6.2 ACIO Timing

Table 37 — ACIO Timing Specification

Symbol[12]	Parameter	I²C Mode Open Drain		I3C Basic Push-Pull[1]		Units	Notes
		Min	Max	Min	Max		
f_{SCL}	Clock frequency	0.01	1	0.01	12.5	MHz	
t_{HIGH}	Clock pulse width high time	260	--	35	--	ns	15
t_{LOW}	Clock pulse width low time	500	--	35	--	ns	15
$t_{TIMEOUT}$	Detect clock low timeout (for SCL timeout reset)	10	50	10	50	ms	
t_{R_HSCL}	Host SCL rise time	--	120	--	min((25e6 - (1.6*fSCL)) *1e-15, 15.4ns)	ns	2,3,8, 13,14,15
t_{F_HSCL}	Host SCL fall time	--	120	--	min((25e6 - (1.6*fSCL)) *1e-15, 15.4ns)	ns	2,3,8, 13,14,15
t_{R_HSDA}	Host SDA rise time	--	300	--	min((25e6 - (1.6*fSCL)) *1e-15, 15.4ns)	ns	2,3,8, 13,14
t_{F_HSDA}	Host SDA fall time	--	120	--	min((25e6 - (1.6*fSCL)) *1e-15, 15.4ns)	ns	2,3,8, 13,14
t_{R_Local}	Local SCL/SDA fall time	--	120	--	5	ns	2,3, 8
t_{F_Local}	Local SCL/SDA fall time	--	120	--	5	ns	2,3, 8
$t_{SU:DAT}$ [t_{su_PP}]	Data in setup time	50	--	8	--	ns	2
$t_{SU:STA}$ [t_{CBSr}]	Start condition setup time	260	--	19.2	--	ns	2, 9
$t_{HD:STA}$ [t_{CASr}]	Start condition hold time	260	--	38.4	--	ns	2, 9
$t_{SU:STO}$ [t_{CBP}]	Stop condition setup time	260	--	19.2	--	ns	2, 9

Table 37 — ACIO Timing Specification (cont'd)

Symbol[12]	Parameter	I²C Mode Open Drain		I3C Basic Push-Pull[1]		Units	Notes
		Min	Max	Min	Max		
t_{BUF}	Time between Stop Condition and next Start Condition	500	--	500	--	ns	2,4
t_{AVAL}	Bus Available time (no edges seen on HSDA and HSCL)			1	--	µs	
$t_{HD:DAT}$ [t_{SCO}]	HSCL Falling Clock In to HSDA Data Out Hold Time (Equivalent I3C value is t_{DOUT})	0.5	350	N/A	N/A	ns	5
t_{DOUT} [t_{SCO}]	HSCL Falling Clock In to HSDA Valid Data Out Time	N/A	N/A	0.5	12	ns	6, 10
t_{DOFFT} [t_{SCO}]	HSCL Rising Clock In to SDA Output Off	N/A	N/A	0.5	12	ns	6, 11
t_{DOFFC} [t_{SCO}]	HSCL Rising Clock In to Controller SDA Output Off	N/A	N/A	0.5	t_{HIGH}	ns	7
$t_{CL\_r\_DAT\_f}$ [t_{CASr}]	HSCL Rising Clock In to Controller Driving HSDA Signal Low	N/A	N/A	40	-	ns	9, 10

NOTE 1 I3C mode with Open Drain operation follows timing values as shown in I2C Mode - Open Drain column.

NOTE 2 See Figure 14 for input timing parameter definition.

NOTE 3 See Figure 13 for voltage threshold definition for rise and fall times.

NOTE 4 If PEC is enabled, tWR_RD_DELAY_PEC_EN timing parameter also applies.

NOTE 5 See Figure 16 for output timing parameter definition.

NOTE 6 JESD403-1 device must be in I3C mode to guarantee tDOUT and tDOFFT values. See Figure 17, Figure 18, Figure 19, and Figure 20

NOTE 7 JESD403-1 device must be in I3C mode. The Host guarantees tDOFFC value. See Figure 18. Also refer to MIPI Alliance Specification for I3C BasicSM Version 1.0-19 July 2018, section 5.1.2.3.2, Transition from Address ACK to Mandatory Byte during IBI.

NOTE 8 The MIPI-I3C specified max tR/tF is 60 ns with a 50 pF load. JESD403-1 Specification defined rise/fall times are with test loads and actual rise/fall times would depend on bus topology.

NOTE 9 tSU:STA is similar to tCBSr on I3C; tHD:STA is similar to tCASr on I3C and tSU:STO is similar to tCBP on MIPI-I3C, since JESD403-1 specification has timings defined with resistive 50 ohm load resulting in tR and tF being negligible.

NOTE 10 JESD403-1 defined tDOUT is similar to MIPI-I3C's tSCO, since tDOUT is defined with a resistive load. JESD403-1 defines a larger value to enable various kinds of designs with very slow turn around. This also results in a larger tCL_r_DAT_f.

NOTE 11 JESD403-1 defined tDOFFT, though similar to MIPI-I3C's tDOUT and is defined differently to add clarity for bus hand-off process in the timing diagram.

NOTE 12 The Symbol is parenthesis is the closest equivalent MIPI-I3C terminology.

NOTE 13 The formula min((25e6 - (1.6*fSCL))*1e-15, 15.4ns) defines the value as the lowest of either the frequency calculation or 15.4 ns, whichever is less. For example, 12.5M Hz = 5 ns, 8 MHz = 12.2 ns, and 6 MHz = 15.4 ns but frequencies lower than 6 Mhz will be capped at 15.4 ns.

NOTE 14 System and module boards are responsible for ensuring that the HSCL/HSDA slope reversal specifications are not violated.

NOTE 15 Regardless of tR or tF time, tHIGH and tLOW shall always be satisfied.

6.2 ACIO Timing (cont'd)

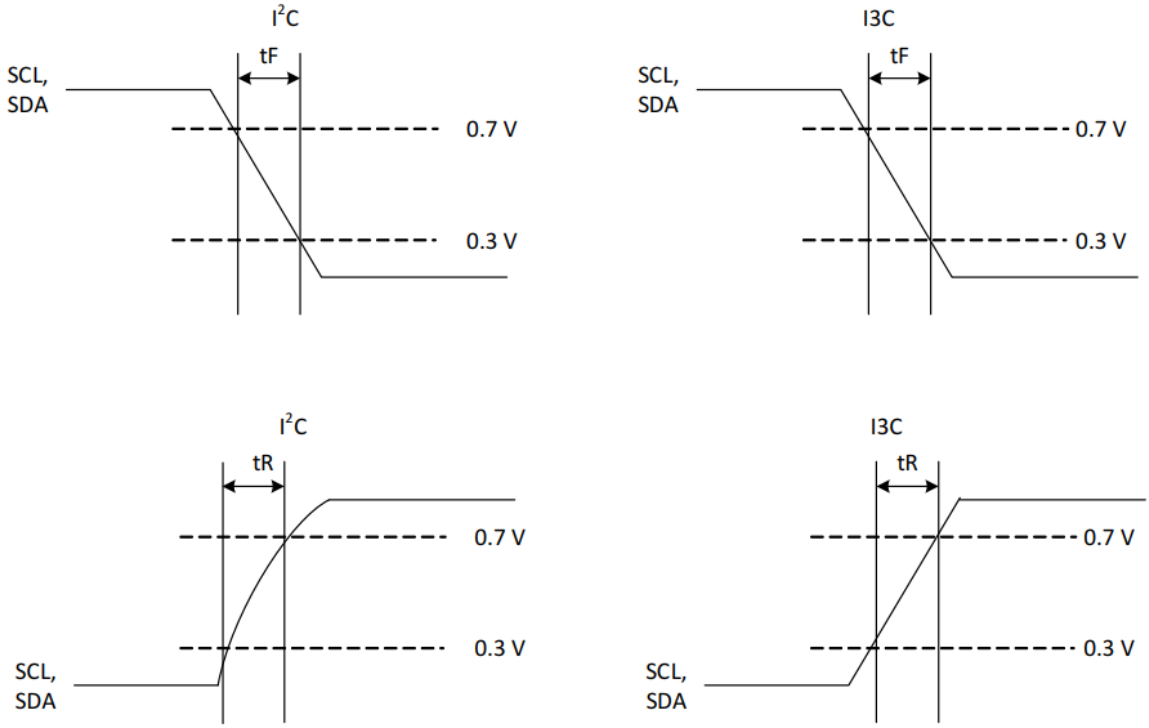


Figure 13 — Rise and Fall Time Parameter Definition

6.2 ACIO Timing (cont'd)

Figures 14 through 16 show the timing diagram for Data Bus Input and Data Output parameters.

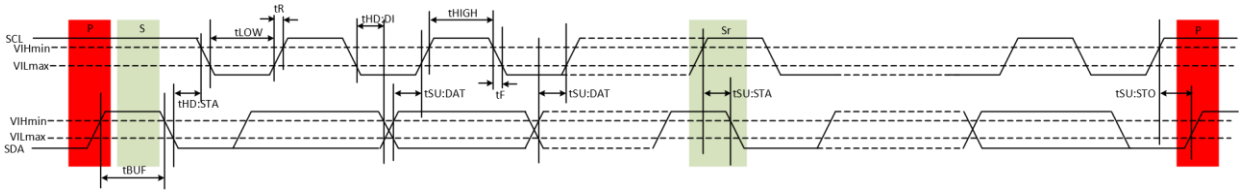


Figure 14 — I2C or I3C Basic Bus AC Input Timing Parameter Definition

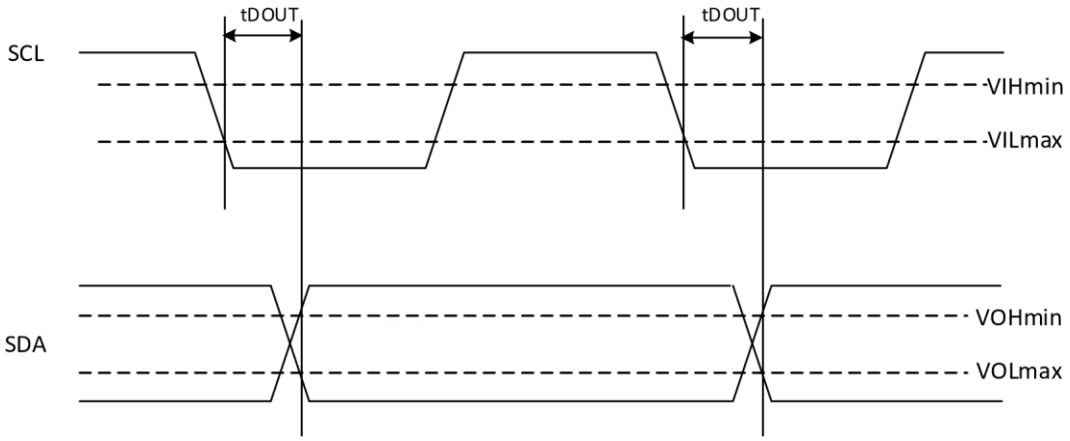


Figure 15 — I3C Basic Bus AC Data Output Timing Parameter Definition

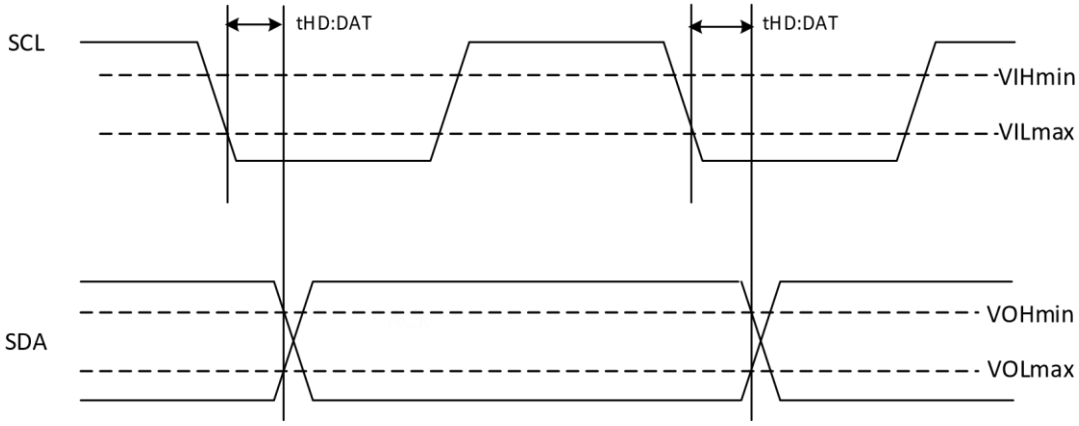


Figure 16 — I2C Bus AC Data Output Timing Parameter Definition

6.2 ACIO Timing (cont'd)

Figures 17 through 20 describe the T-bit usage and timing in different scenarios.

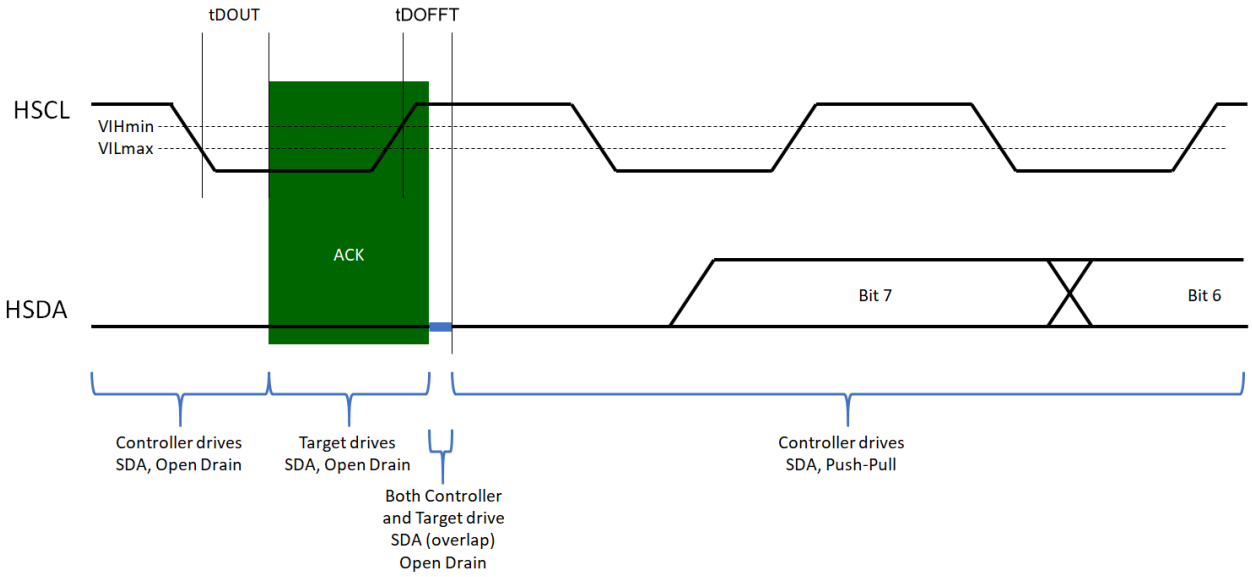


Figure 17 — Target Open Drain to Controller Push-Pull Hand Off Operation

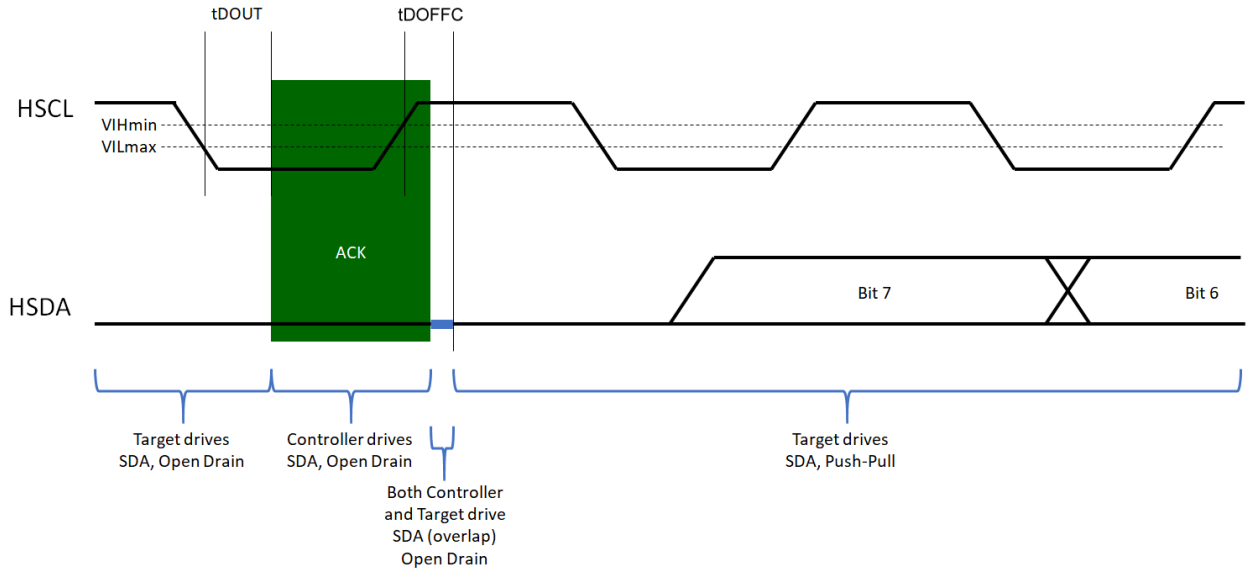


Figure 18 — Controller Open Drain (ACK) to Target Push-Pull Hand Off Operation

6.2 ACIO Timing (cont'd)

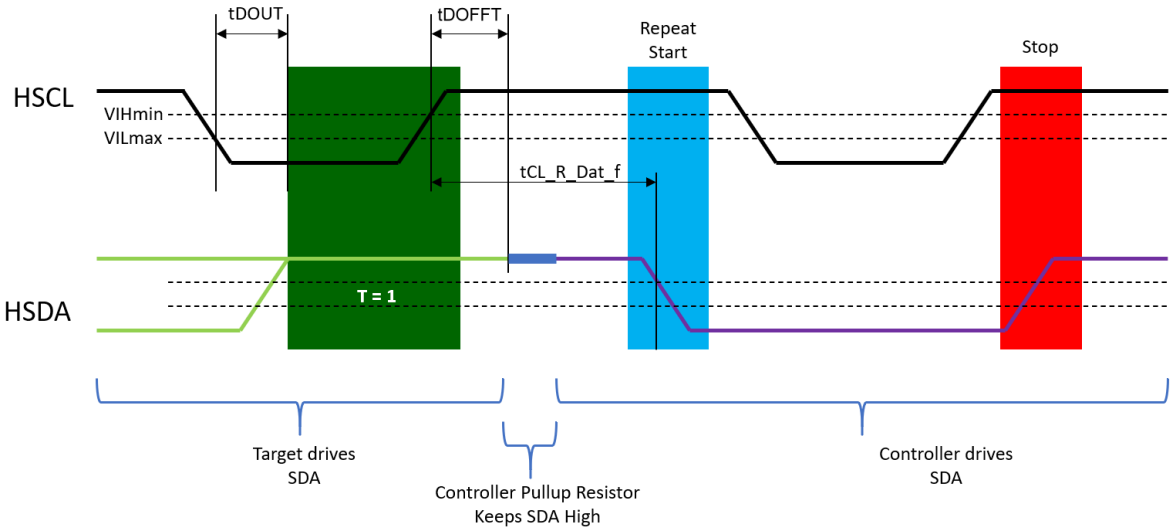


Figure 19 — T=1; Controller Ends Read with Repeated START and STOP Waveform

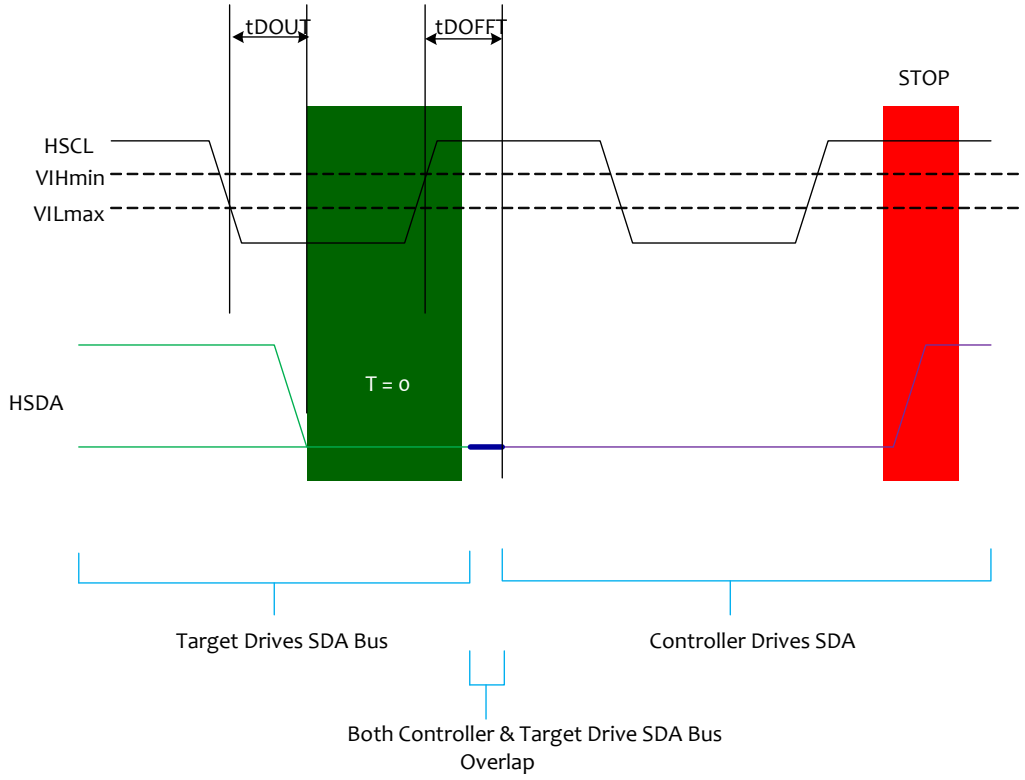


Figure 20 — T=0; Target Ends Read; Controller Generates STOP

6.3 Hub Propagation Delays

A JESD403-1 compliant Hub device must follow the following between the Host and Local bus pins.

Table 38 — Hub Specific ACIO Timing Specification

Symbol	Parameter	I^2C Mode - Open Drain		I3C Basic Push-Pull[1]		Units	Notes
		Min	Max	Min	Max		
t_{PDHL}	Propagation Delay, HSDA to LSDA and HSCL to LSCL		6		6	ns	1
t_{PDLH}	Propagation Delay, LSDA to HSDA		6		6	ns	1

NOTE 1 See Figure 21 for timing definition.

6.3 Hub Propagation Delays (cont'd)

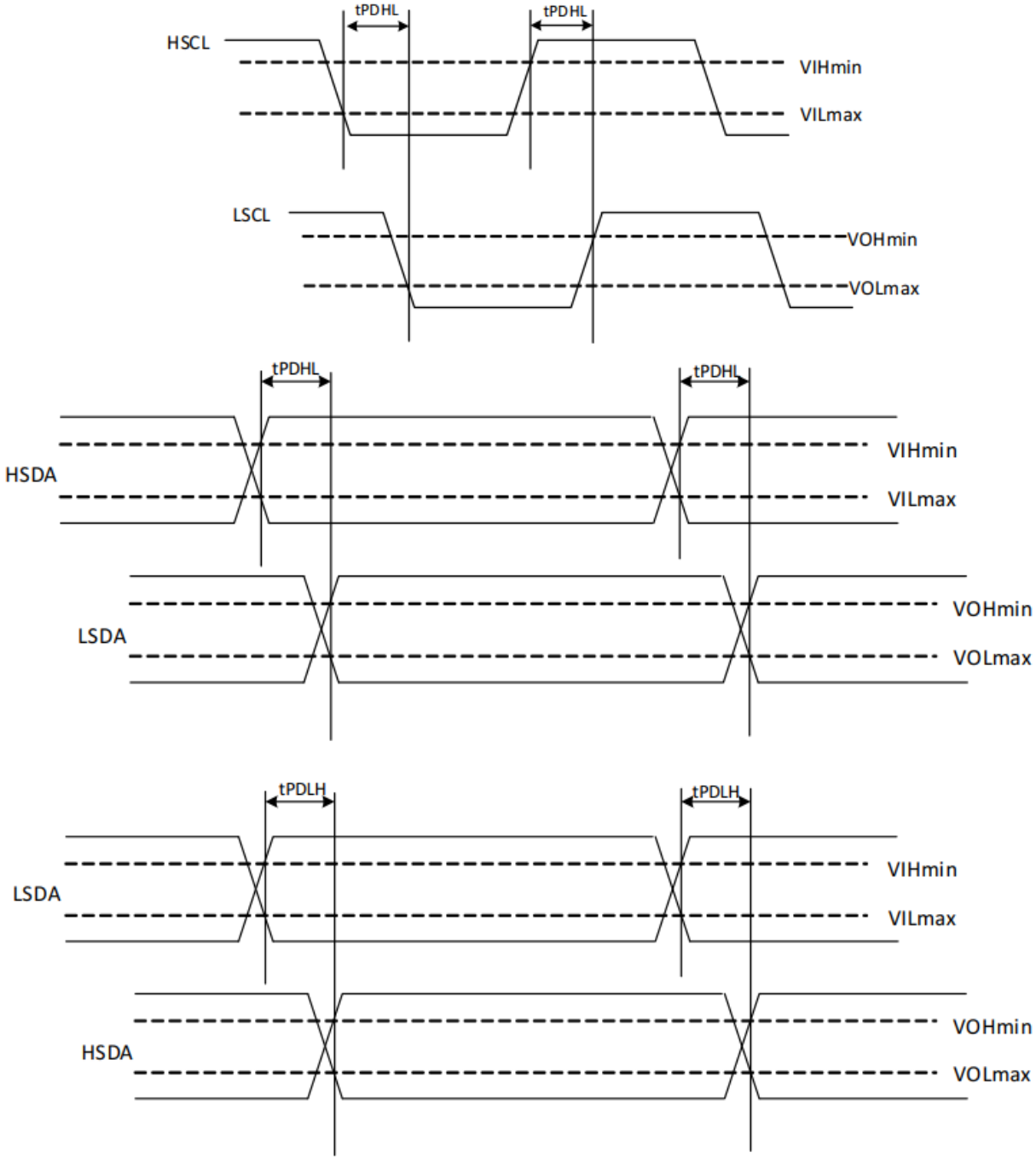


Figure 21 — Propagation Delays Through a HUB Device

6.4 Protocol Level Timing

The following timing definitions allow device settling time due to impact of first CCC or due to PEC recalculation. The usage of such CCC combination should be infrequent, and these timing definitions will typically need to be enforced by software.

Table 39 — Protocol Level and JESD403-1 Specific Timing Specification

Symbol	Parameter	I^2C Mode - Open Drain		I3C Basic Push-Pull[1]		Units	Notes
		Min	Max	Min	Max		
t_{INIT}	Time from power on to first command	10	--	10	--	ms	
t_{RST}	Device reinitialization time			TBD	TBD	ms	
t_{IBI_ISSUE}	Time to issue IBI after an event is detected when Bus is available	-	-	-	15	µs	
$t_{CLR\_I3C\_CMD\_Delay}$	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation; PEC Disabled	-	-	2.5	-	µs	
	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation; PEC Enabled	-	-	15	-	µs	
$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay	3	-	3	-	µs	1,2,3
$t_{WR\_RD\_DELAY\_PEC\_EN}$	Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	N/A	N/A	8	-	µs	4,5,6
$t_{I2C\_CCC\_Update\_Delay}$	SETHID CCC or SETAASA CCC to any other CCC or Read/Write Command delay	2.5	-	-	-	µs	
$t_{I3C\_CCC\_Update\_Delay}$	RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	-	-	2.5	-	µs	
t_{CCC_Delay}	Any CCC to RSTDAA CCC delay	N/A	N/A	2.5	-	µs	

NOTE 1 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.
NOTE 2 The device sends NACK if Host does not satisfy $t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$ timing parameter.
NOTE 3 This timing parameter restriction is only applicable when PEC function is disabled in SPD5 Hub. If PEC is enabled, this timing parameter does not apply.
NOTE 4 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.
NOTE 5 This timing parameter restriction is only applicable when PEC function is enabled in SPD5 Hub. If PEC is disabled, this timing parameter does not apply.
NOTE 6 The device sends NACK if Host does not satisfy $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter.

7 Physical Layout

The SidebandBus architecture assumes a two-tiered topology: a host bus between a Controller and Hub devices, and one or more Local buses between Hubs and Local bus Target devices. Standard I3C devices may share either Host or Local buses, though device addressing issues must be dealt with by the host controller.

The Host bus is designed for a maximum of 9 loads; one Host controller and up to 8 Target devices or Hubs.

Each local bus is designed for up to 8 devices. Simulations on the topology shown in Figure 22 exhibit a preference for a star routing topology from the hub to the local bus devices rather than flyby.

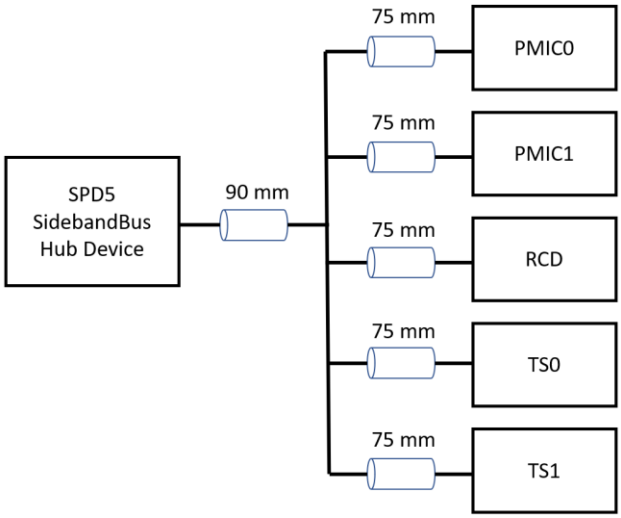


Figure 22 — Star Topology Used in SidebandBus Simulations

Device maximum input loading is 4 pF per device. Variations from this require additional simulation to ensure signal quality.

8 Memory Modules

The SidebandBus primary target application is for systems with memory modules such as registered dual in-line memory modules (RDIMMs). An example RDIMM such as that shown in Figure 23 may have one SPD5 device as the SidebandBus Hub redriving the Host bus to the Local bus which includes a registering clock driver (RCD), two PMIC voltage regulators, and two thermal sensing devices.

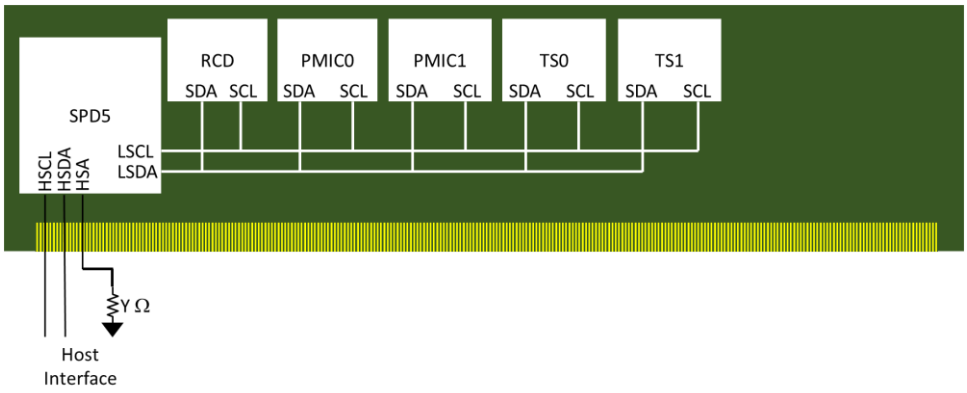


Figure 23 — Typical RDIMM SidebandBus Devices

High end server systems typically employ many RDIMMs, each of which must be uniquely addressed. These RDIMMs are addressed up to 8 modules per SidebandBus by assigning each a slot ID using resistor values on the HSA pin for each slot. Figure 24 shows a system with 8 DIMMs on one SidebandBus Host bus.

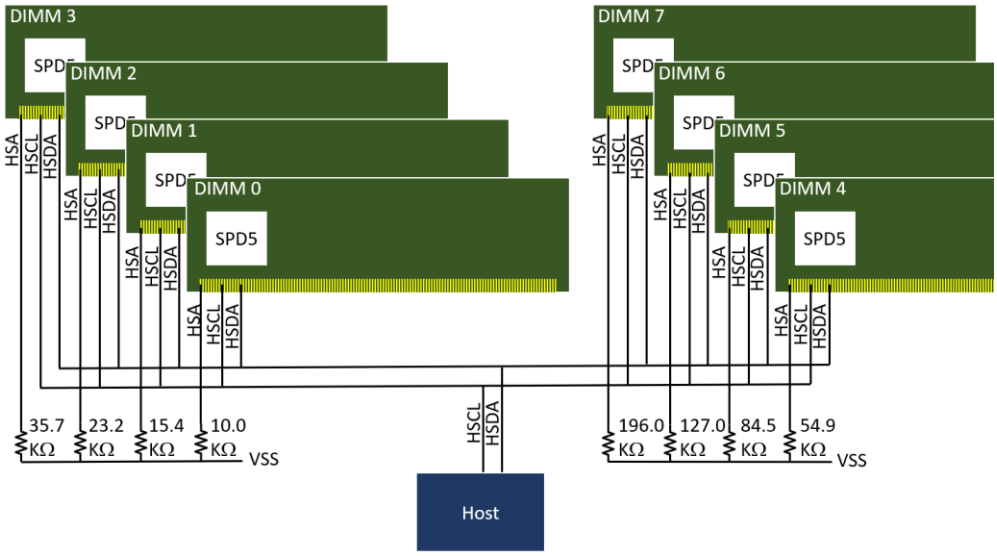


Figure 24 — Unique Slot IDs for Multiple RDIMMs on a SidebandBus

Annex A - (Informative) Differences between Various Revisions

A.1 Differences Between JESD403-1A and JESD403-1.01

This annex briefly describes changes made to this standard, JESD403-1A, compared to its predecessor, JESD403-1.01 (July 2021). Some editorial changes are not included.

Section	Description of change
6.1	Updated clause to add HSCL monotonicity on 16 Sep 2021 per item 2260.56 Figures 10 through 12 added Table 36 (Slope Reversal) added Empty columns removed from Slope Table on 21 Sep 2021
6.2	Old Table 36 (ACIO Timing Specification) renumbered to Table 37
6.3	Old Table 37 (Hub Specific ACIO Timing document) renumbered to Table 38

A.2 Differences Between JESD403-1B and JESD403-1A

1. Updated Table of Contents to the standard format
2. Rephrased “Controller” and “Target” in Table 1 – Terminology
3. Modified Table 33
4. Reformatted Table 36 to add a NOTES column
5. Updated NOTE numbers in Table 39
6. Modified Figures 10 through 12

A.3 Differences Between JESD403-1C and JESD403-1B

1. Added a clause on “Use of Reserved I3C Addresses” on page 29 (after Figure 4)
2. Modified Table 33 to change the maximum values for VDDIO and VIH from 1.25 V to 1.05 V

A.4 Differences Between JESD403-1C.01 and JESD403-1C

1. Updated Table 37 – ACIO Timing Specifications to:
    a. Relax the tR_HSDA maximum value for I^2C Mode from 120 ns to 300 ns,
    b. Modified the t_R row into t_{R_HSCL}, t_{R_HSDA}, and t_{R_Local},
    c. Modified the t_F row into t_{F_HSCL}, t_{F_HSDA}, and t_{F_Local},
    d. Added notes 13 to 15
2. Reformatted the Table of Contents to add the document title at the top of each page per the new Style Manual for Standards and Other Publications of JEDEC, Document Number JM7A.

Standard Improvement Form

JEDEC Standard JESD403-1C.01

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