JEDEC STANDARD

Low Power Double Data Rate Interface for Non-Volatile Memory (LPDDR4X-NVM) Standard

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Low Power Double Data Rate Interface for Non-volatile Memory (LPDDR4X-NVM) Standard

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Low Power Double Data Rate Interface for Non-Volatile Memory (LPDDR4X-NVM) Standard

(From JEDEC Board Ballot JCB-25-47, formulated under the cognizance of the JC-42.6 subcommittee on Low Power Memories, item number 1887.99A).

1 Scope

This standard defines the Low Power Double Data Rate interface for Non-Volatile memory (LPDDR4X-NVM) standard. This standard describes features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this specification is to define the minimum set of requirements for a JEDEC compliant 16 bit single channel LPDDR4X-NVM device. LPDDR4X-NVM density ranges from 128Mb through 32Gb. This document was created using aspects of the following standards: DDR2 (JESD79-2), DDR3 (JESD79-3), DDR4 (JESD79-4), LPDDR (JESD209), LPDDR2 (JESD209-2) LPDDR3 (JESD209-3), LPDDR4 (JESD209-4D) and LPDDR4X (JESD209-4-1A).

The LPDDR4X-NVM standard adopts substantial functionality from the LPDDR4 and LPDDR4X specifications to provide an interface to a multi-bank non-volatile memory array. When practical, LPDDR4X-NVM functionality is adopted directly from the LPDDR4/4X specifications. When necessary, existing infrastructure is modified or new infrastructure is created. This revision of the LPDDR4X-NVM specification describes a dual-port memory with a read-only LPDDR4X interface and a read-write capable Serial Peripheral Interface (SPI). Additional functionality includes an interrupt output signal (INT_n) and a device reset input signal (DEVRST_n).

Each aspect of the standard was considered and approved by committee ballot(s). The accumulation of these ballots was then incorporated into the JEDEC Board Ballot JCB-25-47 to prepare the LPDDR4X-NVM standard.

2 Die Configuration, Pad Order, Package Ballout, and Pin Definition

2.1 Die Configuration

The LPDDR4X-NVM specification supports a single channel x16 die configuration.

Figure 1 shows the signals used for the single channel x16 configuration.

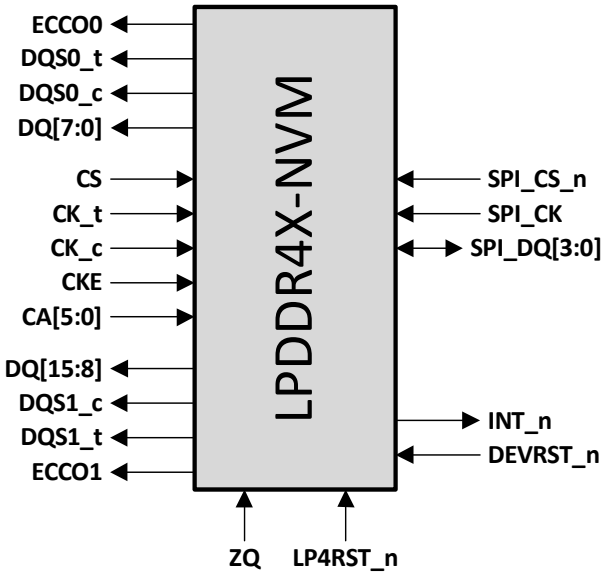


Figure 1 — Single Channel x16 Die

Figure 2 and Figure 3 show simplified block diagrams of the LPDDR4X-NVM device. The standard device is available with the legacy 8-bank LPDDR4 architecture. An optional 8-bank configuration where each bank is partitioned into two sub-banks is also available. The sub-bank architecture allows for READ pipelining between sub-banks within a single bank. The optional architecture uses an upper order row address to specify the target sub-bank. Note that the sub-banks are not specified with a bank address bit but are identified with the highest order (non-bank) row address.

2.1 Die Configuration (cont'd)

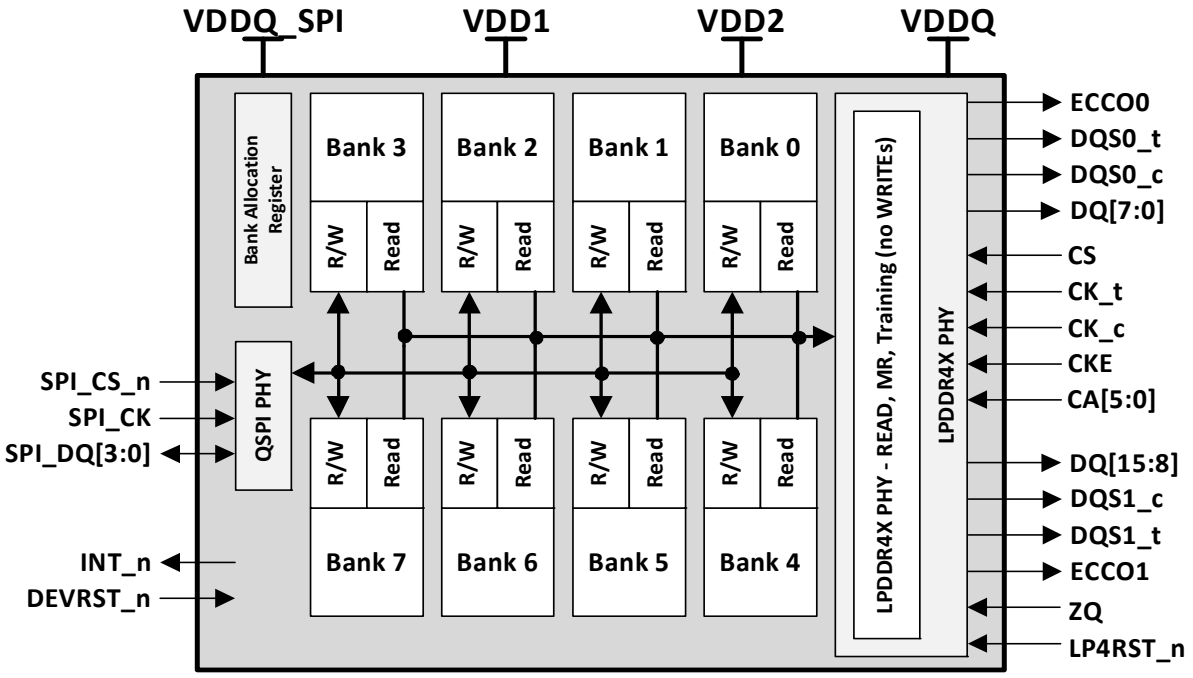


Figure 2 — LPDDR4X-NVM Block Diagram, Standard 8-bank Architecture

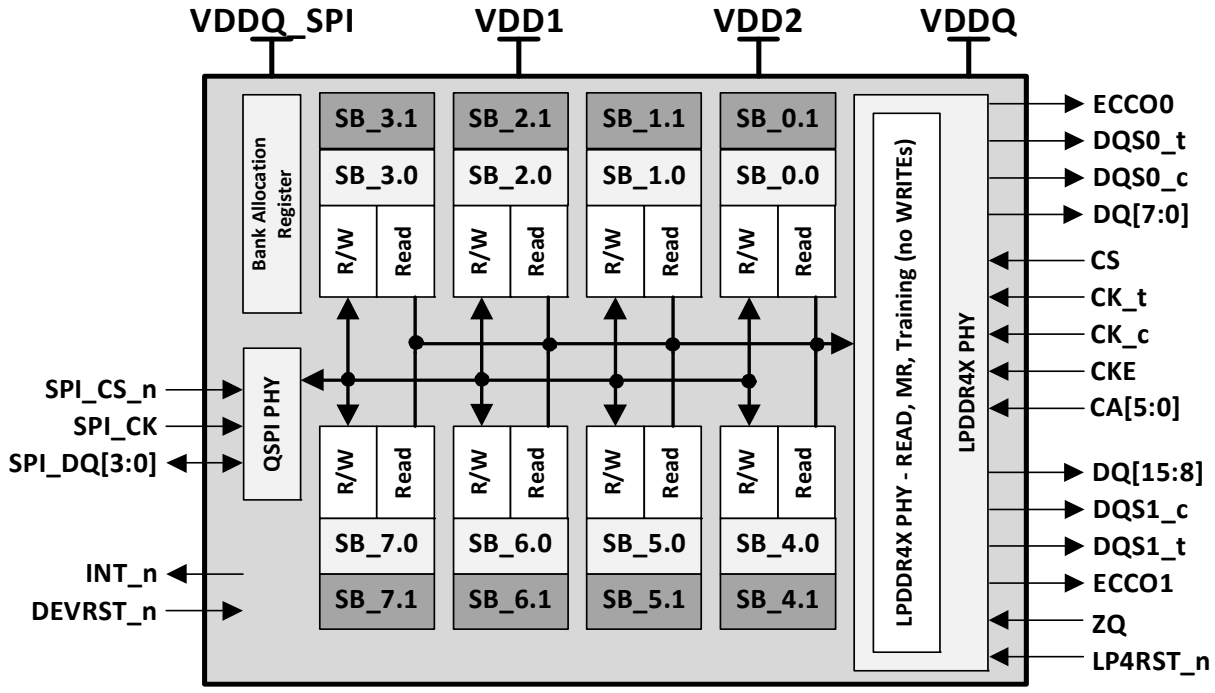
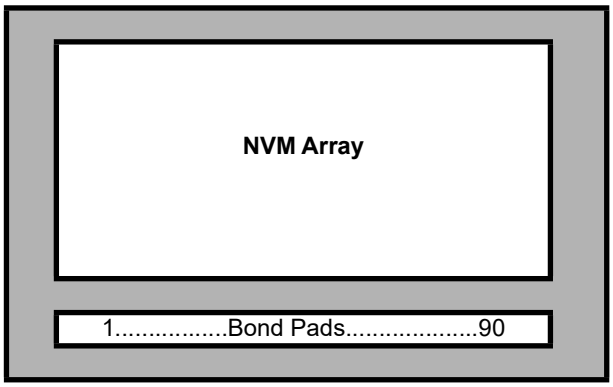


Figure 3 — LPDDR4X-NVM Block Diagram, Optional SubBank (SB) Architecture

2.2 Pad Order

Bottom Left	
1	DIE_NUM
2	DEVRST_n
3	INT_n
4	SPI_DQ3
5	VDDQ_SPI
6	VSS
7	SPI_DQ2
8	SPI_CK
9	SPI_CS_n
10	SPI_DQ1
11	VDDQ_SPI
12	VSS
13	SPI_DQ0
14	VDD2
15	VSS
16	VDD1
17	VDD2
18	VSS
19	VSSQ
20	DQ8
21	VDDQ
22	DQ9
23	VSSQ
24	DQ10
25	VDDQ
26	DQ11
27	VSSQ
28	DQS1_t
29	DQS1_c
30	VDDQ
31	ECCO1
32	VSSQ
33	DQ12
34	VDDQ
35	DQ13
36	VSSQ
37	DQ14
38	VDDQ
39	DQ15
40	VSSQ
41	ZQ
42	VDDQ
43	VDD2
44	LP4RST_n
45	VDD1

46	VSS
47	CA5
48	CA4
49	VDD2
50	CA3
51	CA2
52	VSS
53	CK_c
54	CK_t
55	VDD2
56	CKE
57	CS
58	VSS
59	CA1
60	CA0
61	VDD2
62	VSS
63	VDD1
64	VSSQ
65	DQ7
66	VDDQ
67	DQ6
68	VSSQ
69	DQ5
70	VDDQ
71	DQ4
72	VSSQ
73	ECCO0
74	VDDQ
75	DQS0_c
76	DQS0_t
77	VSSQ
78	DQ3
79	VDDQ
80	DQ2
81	VSSQ
82	DQ1
83	VDDQ
84	DQ0
85	VSSQ
86	VSS
87	VDD2
88	VDD1
89	VSS
90	VDD2
Bottom Right	



NOTE 1 Applications are strongly advised to follow bit/byte assignments. Bit or Byte swapping at the application level requires extensive review of SPI/LPDDR4X bit/byte mapping, MR and calibration features assigned to specific data bits/bytes.

NOTE 2 Additional pads are allowed for memory mfg-specific pads (“DNU”), or additional power pads as long as the extra pads are grouped with like-named pads.

2.3 Package Ballout

2.3.1 123 ball 1CHx16 Discrete Package, 0.80 mm x 0.80 mm using MO-216

0.80 mm pitch (X-axis), 0.80 mm pitch (Y-axis), 12 rows.

0.80 mm Pitch

0.80 mm Pitch	1	2	3	4	5	6	7	8	9	10	11	12
A		DNU				NC	NC				DNU	DNU
B	DNU	RFU	VSS	VDD2	ZQ0	NC	NC	ZQ1	VDD2	VSS	RFU	DNU
C	RFU	DQ0	VDDQ	DQ7	VDDQ	NC	NC	VDDQ	DQ15	VDDQ	DQ8	RFU
D	VSS	DQ1	ECCO0	DQ6	VSS	NC	NC	VSS	DQ14	ECCO1	DQ9	VSS
E	VDDQ	VSS	DQS0_t	VSS	VDDQ			VDDQ	VSS	DQS1_t	VSS	VDDQ
F	VSS	DQ2	DQS0_c	DQ5	VSS			VSS	DQ13	DQS1_c	DQ10	VSS
G	VDD1	DQ3	VDDQ	DQ4	VDD2			VDD2	DQ12	VDDQ	DQ11	VDD1
H	VSS	DNU	VSS	VDDQ_SPI	VSS			VSS	VDDQ_SPI	VSS	LP4RST_n	VSS
J	VDD2	CA0	CS1	CS0	VDD2	SPI_DQ0	VSS	VDD2	CA2	CA3	CA4	VDD2
K	VSS	CA1	VSS	CKE0	CKE1	SPI_DQ1	INT_n	CK_t	CK_c	VSS	CA5	VSS
L	VDD2	VSS	VDD2	VSS	SPI_CS_n	SPI_CK	SPI_DQ3	DEVRST_n	VSS	VDD2	VSS	VDD2
M	DNU	DNU				SPI_DQ2	VSS				DNU	DNU

NOTE 3 Top View, A1 in top left corner.
NOTE 4 Die pad VSS and VSSQ signals are combined to VSS package balls.

2.4 Pin Definition and Description

Table 1 — Pin Definition and Description

Symbol	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs for the LPDDR4X interface. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK.
CKE[1:0]	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. CKE[1] connects to the Rank 1 die in a two die package. CKE[0] connects to the Rank 0 die in a two die package and is used as CKE in a single die package.
CS[1:0]	Input	**Chip Select:** CS is part of the command code. CS[1] is used to indicate Rank 1 in a two die package. CS[0] is used to indicate Rank 0 in a two die package and is used as CS in a single die package.
CA[5:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table.
DQ[15:0]	I/O	**Data Input/Output:** Bi-direction data bus. Outputs during READ transactions, inputs during CA bus training.
DQS[1:0]_t, DQS[1:0]_c	Output	**Data Strobe:** DQS_t and DQS_c are differential output clock signals used to strobe data during a READ. The Data Strobe is generated by the memory for a READ and is edge-aligned with Data.
ECCO[1:0]	Output	**Error Correction Code Output:** The ECC Outputs (per byte lane) can be configured for the following using Mode Register settings: 1. ECC Outputs disabled during read transactions 2. The ECCO signals are used during Read transactions to output ECC information.
ZQ[1,0]	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor. ZQ[1] connects to the Rank 1 die in a two die package. ZQ[0] connects to the Rank 0 die in a two die package and is used as ZQ in a single die package.
VDDQ, VDD1, VDD2, VDDQ_SPI	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	**Ground Reference:** Power supply ground reference
LP4RST_n	Input	**LP4RST_n:** When asserted LOW, the LP4RST_n signal resets the LPDDR4X interface. LP4RST_n does not include a weak pull-up.
DEVRST_n	Input	**DEVRST_n:** The DEVRST_n pin is used to re-initiate the Power-On Reset (POR) process. All volatile registers will be returned to their default state during the reset process. DEVRST_n includes a weak pull-up.
INT_n	Output	**INT_n:** Open drain output indicates to the host system that an internal event has occurred. INT_n includes a weak (internal) pull-up.The recommended (external) pull-up resistor for the INT_n output is 5K to 10K ohms.
SPI_CS_n	Input	**SPI_CS_n:** Low enabled chip select for the SPI interface.
SPI_CK_n	Input	**SPI_CK_n:** The clock signal for the SPI interface.
SPI_DQ[3:0]	I/O	**SPI_DQ[3:0]:** The SPI data bus supports both the x1 SPI (default) and x4 (QSPI) interfaces.
DIE_NUM	Input	**DIE_NUM:** This input is compared to an upper-order address bit during SPI transactions when two die are assembled in a single package. On the SPI interface, the Rank 0 device is indicated when the DIE_NUM input is bonded to VSS and the Rank 1 device when DIE_NUM is bonded to VDDQ_SPI.
NOTE 1 Consult manufacturer data sheet for manufacturer specific behavior of stacked die devices.		

2.5 ZQ Wiring

Standard LPDDR4X-NVM package ballmaps allocate one ZQ ball per die.

(See Section 4.20.2, 'ZQ External Resistor, Tolerance, and Capacitive Loading' for more information.)

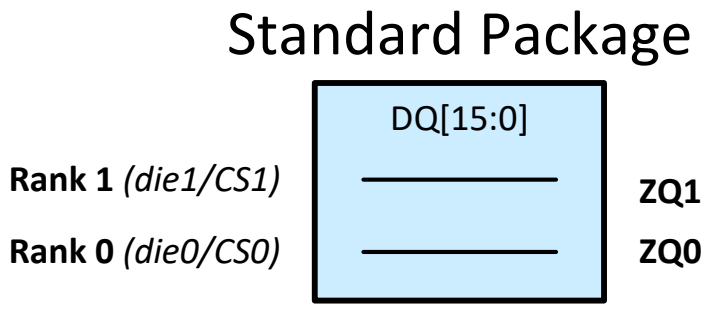


Figure 4 — ZQ Wiring Overview

Below are specific wiring notes for multi-die LPDDR4X-NVM packages.

1. For multi-die packages:
   - ZQ0 is connected to the rank 0 LPDDR4X-NVM device
   - ZQ1 is connected to the rank 1 LPDDR4X-NVM device (if present)

3 Functional Description

LPDDR4X-NVM is a high-speed synchronous nonvolatile memory device. The device is comprised of 8-banks with device densities ranging from 128 Mb to 32 Gb. The devices implement a two-port architecture that includes a Quad IO Serial Peripheral Interface (QSPI) port and a single channel x16 LPDDR4X interface. The LPDDR4X port is read-only and the SPI port supports both read and write operations.

The Serial Peripheral Interface (SPI) port on the LPDDR4X-NVM device performs a number of functions intended to enhance device performance and allow for ease of adoption.

1. Offload the LPDDR4X-NVM interface from performing WRITE operations. Performing Program and Erase operations can occur over the SPI port without diminishing any of the READ bandwidth on the LPDDR interface.
2. Transferring WRITE operations away from the LPDDR interface eliminates the need for time-consuming write training. Eliminating write training shortens the time required until the LPDDR interface is ready for operation.
3. The SPI port allows booting from a legacy boot path. A Quad-SPI boot option is available on many SoC devices.

A 4-bit Quad-SPI (QSPI) port was chosen because of its universal adoption by SoC devices targeting the automotive ecosystem. Performance of the SPI port is a secondary concern because the expectation is that only a small amount of code/data will be accessed during the boot process before high-speed read access is available over the LPDDR interface. A secondary reason for using QSPI is that the interface is well understood and its definition (within this JEDEC specification) can be made unambiguous.

Single-channel LPDDR4X-NVM devices contain the following number of bits:

128 Mb has 134,217,728 bits

256 Mb has 268,435,456 bits

512 Mb has 536,870,912 bits

1 Gb has 1,073,741,824 bits

2 Gb has 2,147,483,648 bits

4 Gb has 4,294,967,296 bits

8 Gb has 8,589,934,592 bits

16 Gb has 17,179,869,184 bits

32 Gb has 34,359,738,368 bits

LPDDR4X-NVM devices use a 2 or 4 clock architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycles, during which command information is transferred on the positive edge of the clock. See command truth table for details.

The LPDDR4X interface uses a double data rate architecture on the DQ pins to achieve high speed operation. A read access on the LPDDR4X interface consists of a single 256 (or 512) bit wide, data transfer from the internal NVM array using 16 (or 32) corresponding 16-bit wide, one half-clock-cycle data transfers at the I/O pins, referred to as the Burst Length (BL). Read accesses from the LPDDR4X-NVM device are burst oriented; accesses start at a selected location and continue for 16 (BL16) or 32 (BL32) address locations in a programmed sequence.

The LPDDR4X-NVM specification describes four different READ sequences:

1. The Legacy READ sequence is available on devices using a high-speed NVM technology and is compatible with the JEDEC LPDDR4X standard. The Legacy READ is described in Section 4.1.1.

2. The Non-Volatile READ sequence minimizes the CA bus footprint for shorter latency NVM technologies. The NVR READ is described in Section 4.1.2.

3 Functional Description (cont'd)

3. The Modified READ sequence is available on devices using a longer latency NVM technology and requires that the host controller comprehend the increased number of row addresses and the smaller row size. The Modified READ is described in Section 4.1.3.

4. The Modified READ with the optional PRE-ACTIVATE command. The PRE-ACTIVATE command is used to support higher densities when using the Modified READ command. The Modified READ using PRE-ACTIVATE is described in section 4.1.4

Manufacturers are expected to support only one of the READ transactions on a device.

Prior to normal operation, the LPDDR4X-NVM device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

3.1 LPDDR4X-NVM Addressing

Table 2 — LPDDR4X-NVM Addressing x

	Legacy JEDEC READ		Modified JEDEC READ		Non-Volatile READ (NVR)	
	BL16	**BL32**	**BL16**	**BL32**	**BL16**	**BL32**
Max Device Density	32Gb	32Gb	1Gb	2Gb	2Gb	4Gb
Max Using Pre-Activate	n.a.		32Gb	32Gb	n.a.	
Configuration	1x 16DQ x 8-bank (single channel)					
Channels (per die)	1					
Number of Banks	8					
Array Pre-Fetch (bits)	256	512	256	512	256	512
Row Size (Bytes)	32	64	32	64	32	64
Number of Rows (1Gb density example)	4,194,304	2,097,152	4,194,304	2,097,152	4,194,304	2,097,152
Bank Address	BA0 - BA2		BA0 - BA2		na	
Row Addresses (wo PRE)	R0 - R23	R0 - R22	R0 - R18	R0 - R18	R0 - R22	R0 - R22
Row Addresses (with PRE)	na		R0 - R23	R0 - R23	na	
Column Addresses	C2 - C3	C2 - C4	C2 - C3	C2 - C4	na	
Burst Starting Address Boundary	64 - bit		64 - bit		256 - bit	512 - bit

NOTE 1 During RD/CAS2 transactions, the lower two column addresses (A0 - A1) are assumed to be "zero" and are not transmitted on the CA bus.

NOTE 2 For device densities not requiring upper order ROW bits, the respective values in the command cycles must be driven to a valid 1 or 0 level

NOTE 3 During NVR1/2 transactions, the lower "column" addresses are assumed to be "zero" and are not transmitted on the CA bus.

3.2 Simplified LPDDR4X-NVM State Diagrams

The LPDDR4X-NVM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specifications.

The truth tables provide complementary information to the state diagram; they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For command definitions, see Section 4, Command Definitions and Timing Diagrams.

3.2.1 Bank Allocation Register

The LPDDR4X-NVM device is a dual port memory with banks allocated to either the LPDDR4X port or the SPI port. The 8-banks are allocated according the their respective bits in the Bank Allocation Register (BAR). If a bit in the BAR is 1, the corresponding bank is allocated to the LPDDR4X port. If a bit in the BAR is a 0, the corresponding bank is allocated to the SPI port.

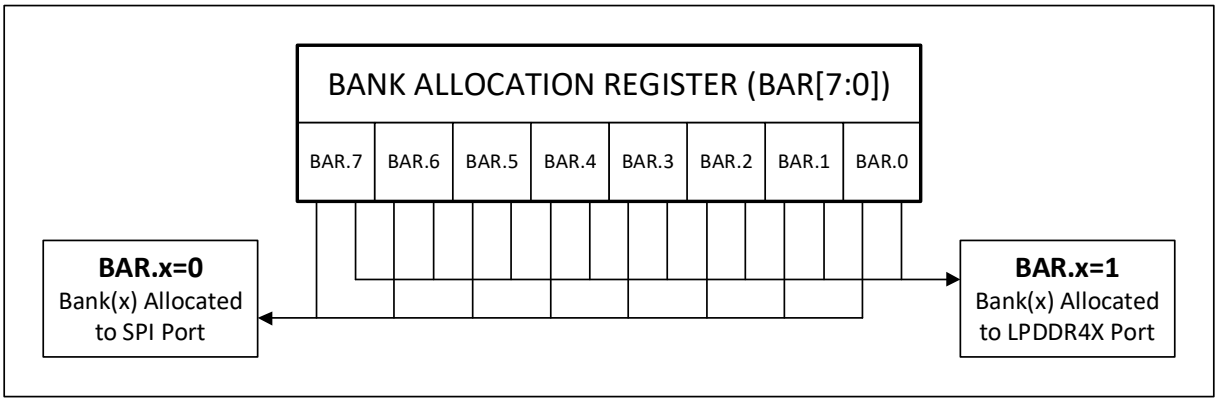


Figure 5 — Bank Allocation Register

3.2.2 LPDDR4X Port State Diagram

The State Diagram for the LPDDR4X Port is described in Figure 6. The diagram narrowly describes the state diagram for the LPDDR4X Port. Only banks that are allocated to the LPDDR4X Port are included in this description. The SPI Port and the banks allocated to the SPI Port are not described in a State Diagram. Note that the LPDDR4X-NVM device introduces an optionally supported READ transaction that use the Non-Volatile Read (NVR) command. The NVR based read lowers the command bus overhead to initiate a read transaction to four clock cycles (NVR1-NVR2) instead of the (Legacy and Modified) JEDEC READ that requires eight clocks (ACT1-ACT2-RD1-CAS2) or the Modified JEDEC READ using PREACTIVATE that uses ten clocks (PRE-ACT1-ACT2-RD1-CAS2).

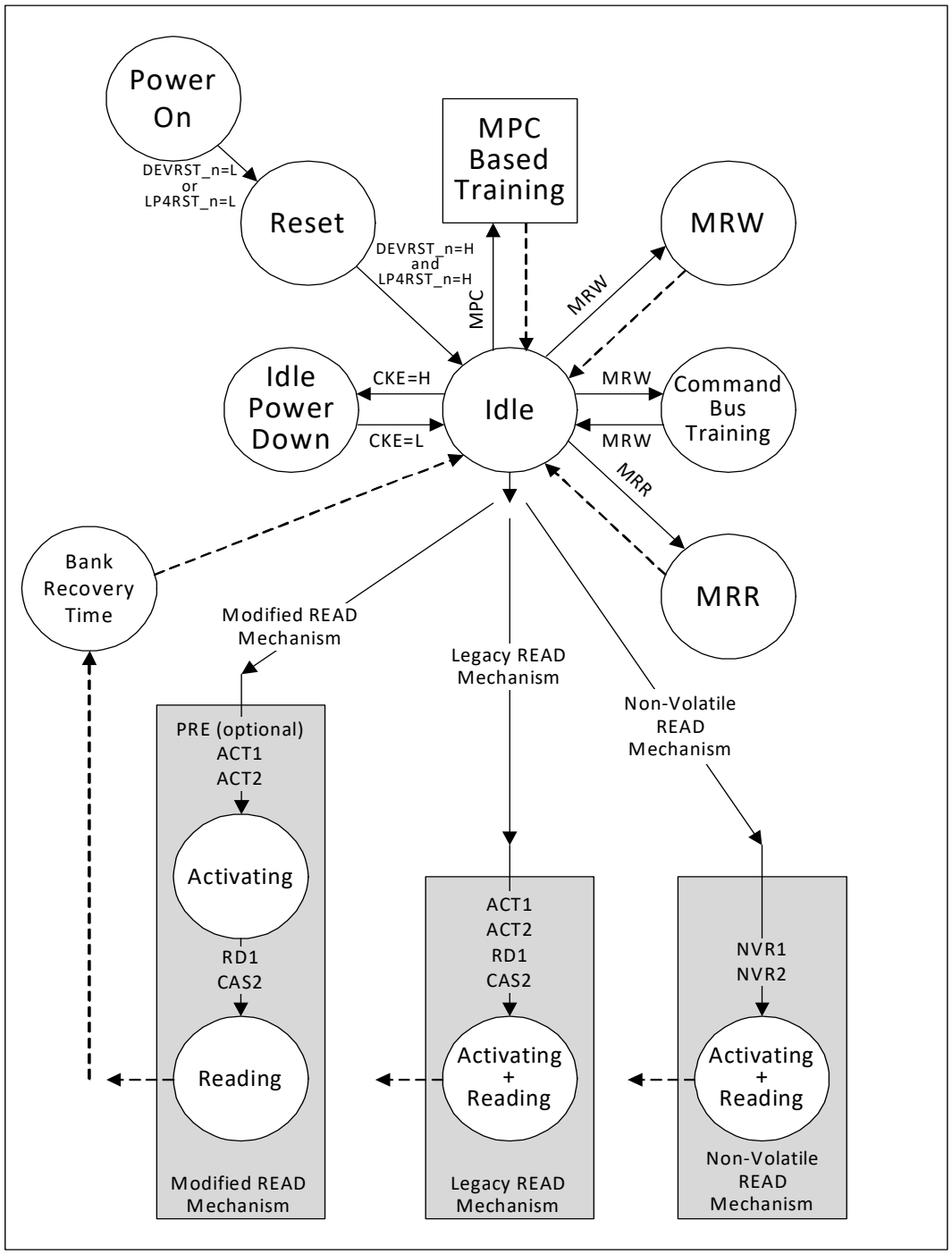
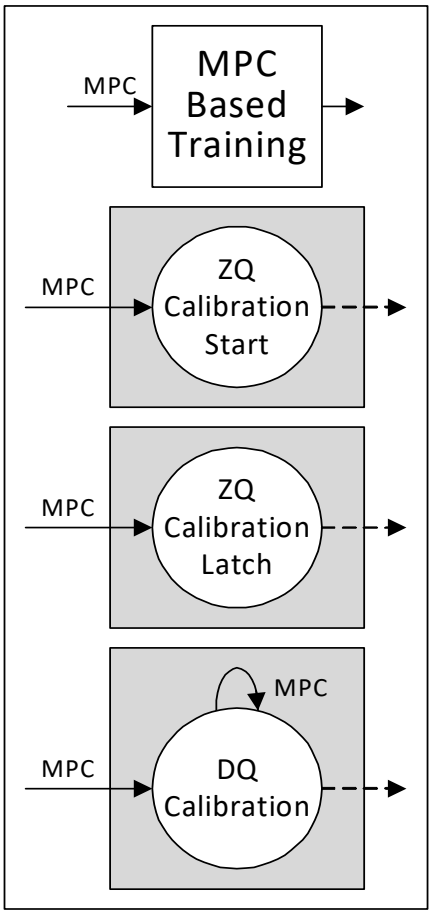


Figure 6 — LPDDR4X-NVM Interface State Diagram

3.2.3 Multi-Purpose Command (MPC) Based Training State Diagram

The LPDDR4X-NVM interface is simpler to train than its LPDDR4X-DRAM counterpart due to its read-only nature. MPC based training is only needed for ZQ calibration and DQ (READ) calibration.



NOTE 1 In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training.
See Section 4.11 for more information.

NOTE 2 In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training.
See Section 4.18 for more information.

NOTE 3 This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

NOTE 4 The LP4RST_n pin can be asserted from any state, and will cause the LPDDR4X interface to go to the Reset State. Similarly, the DEVRST_n can be asserted from any state, and will cause the entire device to go to the reset state. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on either RESET input.

Figure 7 — LPDDR4X-NVM Interface Training State Diagram

3.3 Power-up, Initialization, and Power-off Procedure

For power-up and reset initialization, in order to allow the LPDDR4X-NVM device to function properly, default values of the following MR settings are defined as shown in Table 3.

Table 3 — MRS Default Settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] is enabled
RL	MR2 OP[2:0]	000_B	RL = 6
ECCO	MR3 OP[7:6]	00_B	Read ECC Output is disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
V_{REF}CA Setting	MR12 OP[6]	1_B	V_{REF}CA Range[1] enabled
V_{REF}CA Value	MR12 OP[5:0]	011101_B	Range1: 50.3% of V_{DDQ}

3.3.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4X-NVM device. Unless specified otherwise, these steps are mandatory.

1. While applying power (after Ta), DEVRST_n is recommended to be LOW (≤0.2 x V_{DD1}) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while DEVRST_n is held LOW. Power supply voltage ramp requirements are provided in Table 4. V_{DD1} must ramp at the same time or earlier than V_{DDQ_SPI}. V_{DDQ_SPI} must ramp at the same time or earlier than V_{DD2}. and VDD2 must ramp at the same time or earlier than VDDQ.

Table 4 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DDQ_SPI}
	V_{DDQ_SPI} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV
NOTE 1 Ta is the point when any power supply first reaches 300 mV. NOTE 2 Voltage ramp conditions in Table 2 apply between Ta and power-off (controlled or uncontrolled). NOTE 3 Tb is the point at which all supply and reference voltages are within their defined ranges. NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20 ms. NOTE 5 The voltage difference between any V_{SS} and V_{SSQ} pins must not exceed 100 mV.	

2. Following the completion of the voltage ramp (Tb), DEVRST_n must be maintained LOW. DQ, ECCO, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

3. Beginning at Tb, DEVRST_n must remain LOW for at least tINIT1(Tc), after which DEVRST_n can be deasserted to HIGH(Tc). LP4RST_n must be held LOW from Tb to the end of tINIT2. All other input signals are “Don’t Care.”

3.3.1 Voltage Ramp and Device Initialization (cont'd)

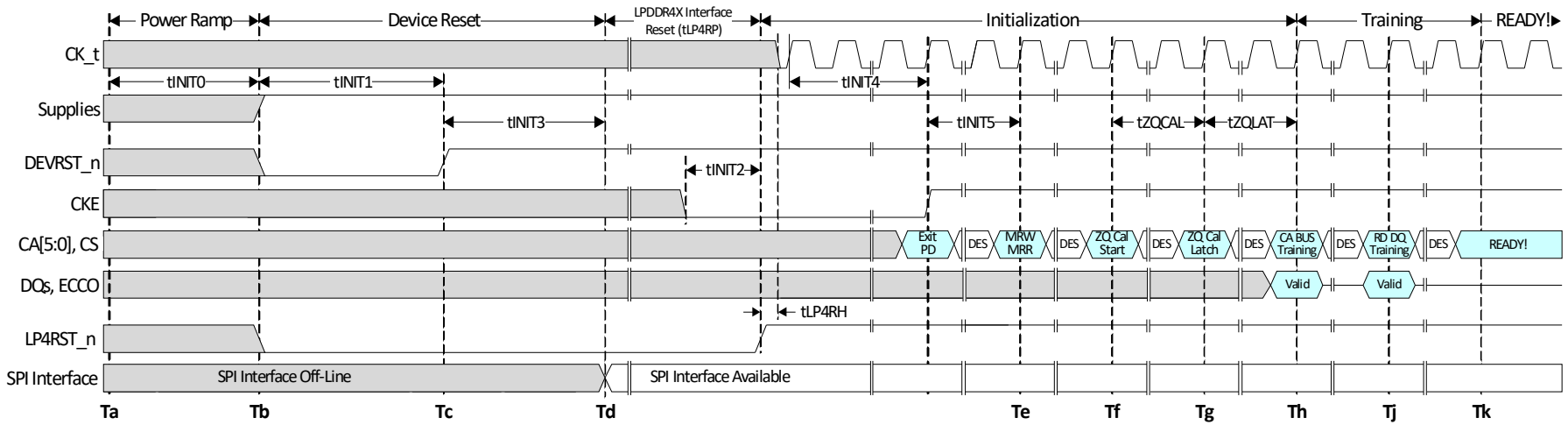


Figure 8 — Power Ramp and Initialization Sequence

4. After DEVRST_n is de-asserted(Tc), wait for at least tINIT3 (Td) before the LPDDR4X-NVM interface reset (LP4RST_n) process initiates. LP4RST_n must remain LOW for at least tLP4RP from Td, after which LP4RST_n can be deasserted to HIGH. At least tINIT2 before LP4RST_n deassertion, CKE is required to be set LOW. Clock (CK_t, CK_c) is required to be started and stabilized for tINIT4 before CKE goes active. CS is required to be maintained at LOW when the controller activates CKE. The SPI interface also becomes available at Td and the host also starts communicating with the SPI port by asserting SPI_CS LOW.

5. After setting CKE high, wait minimum of tINIT5 to issue any Mode Register Read (MRR) or Mode Register Write (MRW) commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and input termination values, the LPDDR-NVR host controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate the VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4X-NVM device share one external ZQ resistor, the controller must not overlap the (independent) ZQ calibration sequence of each LPDDR4X-NVM device. The ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and CA ODT to the calibrated values.

3.3.1 Voltage Ramp and Device Initialization (cont'd)

7. After tZQLAT is satisfied (Th), the command bus (internal V_{REF}CA, CS, and CA) should be trained for high-speed operation by issuing a MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V_{REF}CA and align CS/CA with CK for high-speed operation. The LPDDR4X-NVM device will power-up with receivers configured for low-speed operations, and V_{REF}CA set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

   NOTE The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See Section 4.14 for information on how to enter/exit the Command Bus training mode.

8. After Command Bus Training (CBT) has completed, the Multi-Purpose Command (MPC) Read Calibration command is used (repeatedly at Tj) by the host MCU to calibrate its own VrefDQ and also its READ data capture timing.

9. At Tk the LPDDR4X-NVM device is ready for normal operation, and is ready to accept any valid command. Any mode registers that have not previously been set up for normal operation should be written at this time.

Table 5 — Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Maximum voltage-ramp time
tINIT1	1	-	µs	Minimum DEVRST_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE low time before DEVRST_n high
tINIT3	400	-	µs	Time to SPI bus available after DEVRST_n high after power-up
tINIT4	5	-	tCK	Minimum stable clock before first CKE high
tINIT5	2	-	µs	Minimum idle time before first MRW/MRR command
tZQCAL	1	-	µs	ZQ calibration time
tZQLAT	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time.
tCKb	Note *1,2	Note *1,2	ns	Clock cycle time during boot
tZQRESET	Max(50ns, 3tCK)	-	ns	ZQ Calibration Reset Time
tLP4RH	20	-	ns	Reset Hold - LP4RST_n deasserted before CK recognized
tLP4RP	100	-	ns	Interface Reset Pulse Width (LP4RST_n)

NOTE 1 Min tCKb guaranteed by LPDDR4X-NVM test is 18 ns.
NOTE 2 The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

3.3.2 Device Reset with Stable Power (DEVRST_n)

The following sequence is required for Device Reset after the power reaches a stable state.

1. Assert DEVRST_n below 0.2 x V_{DDQ_SPI} anytime when device reset is needed. DEVRST_n needs to be maintained for minimum tPW_RST. CKE must be pulled LOW at least 10 ns before de-asserting DEVRST_n.
   - All device registers (LPDDR4X and SPI) are loaded with their default values.
   - All embedded operations (erase, program, ...) are terminated
2. Wait for the Stable Power Reset time (tSPR) to expire
3. Perform the LPDDR4X bus initialization sequence starting from the beginning of tINIT4 (See “Power Ramp and Initialization Sequence” on page 14.).

Table 6 — Stable Power Reset Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RST	200	-	ns	Minimum DEVRST_n low Time for Reset Initialization with stable power
tCKE_DEVRST	10	-	ns	CKE LOW before DEVRST_n high
tSPR	MSV	-	µs	Stable Power Reset recovery time for the SPI and LPDDR4X buses after DEVRST_n high
NOTE 1 MSV (Manufacturer Specific Values) are specified in the READ-ID Table (Table 135).				

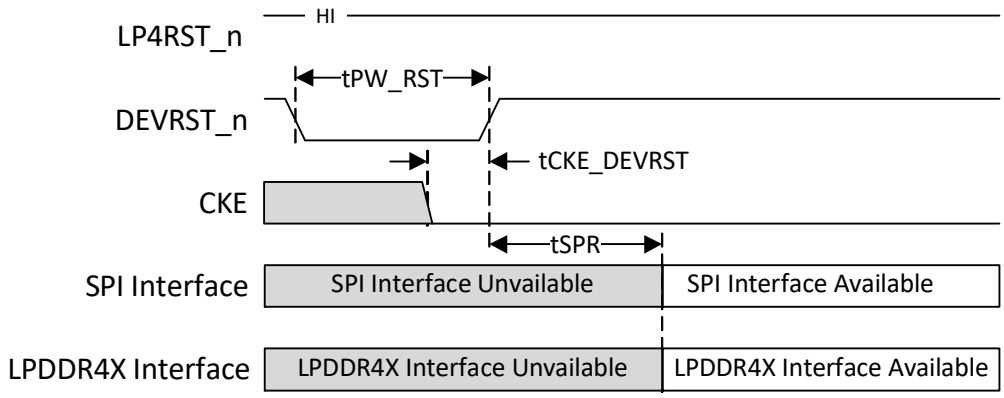


Figure 9 — Stable-Power Device Reset Timing

3.3.3 LPDDR4X Interface Reset with Stable Power (LP4RST_n)

A dedicated LPDDR4X input signal (LP4RST_n) is used to return the LPDDR4X interface to the default state. While the LP4RST_n signal is asserted (LOW), all LPDDR4X inputs are ignored and outputs are placed into the High-Z state. LP4RST_n must remain LOW for at least tLP4RP, after which LP4RST_n can be deasserted to HIGH. At least tINIT2 before LP4RST_n deassertion, CKE is required to be set LOW. All other LPDDR4X input signals are “Don’t Care.” After LP4RST_n is deasserted, wait at least tCKCKEH before activating CKE and after setting CKE HIGH, wait a minimum of tXP to issue commands on the LPDDR4X interface.

Upon completion of an LPDDR4X interface reset, the default values are loaded into the LPDDR4X Mode Registers . The LPDDR4X interface will be ready for new operations after tLP4RH has elapsed.

Note that the LPDDR4X Interface Reset only impacts the LPDDR4X interface, activity in the rest of the device is not interrupted. The LP4RST_n input is ignored during PoR.

3.3.3 LPDDR4X Interface Reset with Stable Power (LP4RST_n) (cont'd)

Table 7 — Mode Registers Set to Defaults After LPDDR4X Interface Reset

Mode Register #	Register Name	Comments
MR1	Bus Configuration 1	Burst Length, Read Preamble, Read Postamble
MR2	Bus Configuration 2	Read Latency
MR3	IO Configuration	Pull-up Cal Point, Pull-down Drive Strength, ECC over ECCO
MR11	ODT Control	CA ODT Strength
MR12	VrefCA Control	VrefCA Setting, VrefCA Range
MR13	Register Control	Frequency Set Point (FSP) Read/Write, Frequency Set Point Operation Mode
MR22	ODT Configuration	CK ODT Enable, CS ODT Enable, CA ODT Enable

Table 8 — LPDDR4X Interface Reset Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT2	10	-	ns	Minimum CKE low time before LPRST_n high
tCKCKEH	max(1.75ns, 3nCK)	-	ns	CK valid before CKE high
tXP	max(7.5ns, 5nCK)	-	ns	Exit Power Down to next valid command
tLP4RP	100	-	ns	Interface Reset Pulse Width (LP4RST_n)
tLP4RH	20	-	ns	LP4RST_n deasserted before CK recognized

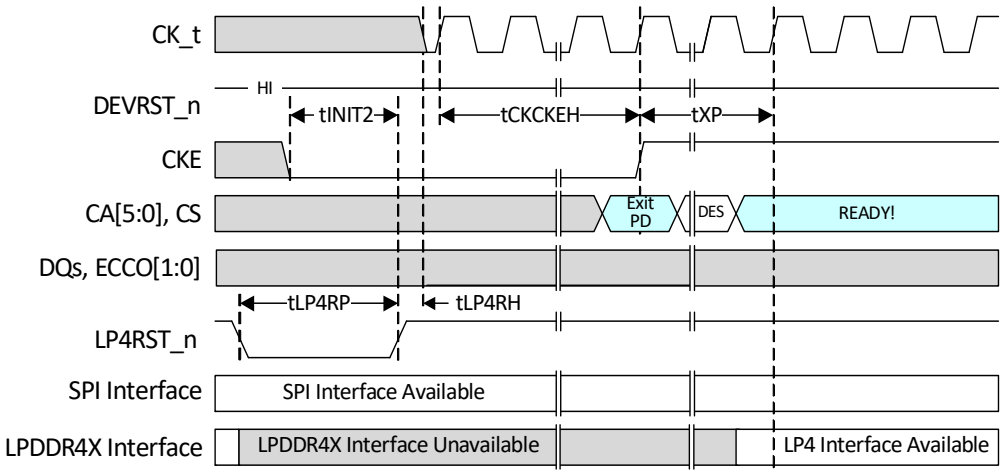


Figure 10 — LPDDR4X Interface Reset Timing

3.3.4 Power-Off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (≤0.2 X V_{DD2}) and all other inputs must be between VIL_CKEmin and VIH_CKEmax. The device outputs remain at High-Z while CKE is held LOW. DQ, ECCO, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. DEVRST_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Table 9 — Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DDQ_SPI}
	V_{DDQ_SPI} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV
NOTE 1 Tx is the point where any power supply drops below the minimum value specified. NOTE 2 Tz is the point where all power supplies are below 300mV. After T_Z, the device is powered off. NOTE 3 The voltage difference between any of V_{SS}, V_{SSQ} pins must not exceed 100 mV. NOTE 4 V_{DD1} must be higher than V_{DD2} during Power-Off.	

3.3.5 Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300 mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

The maximum Power-Off ramp time is tPOFF.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 10 — Timing Parameters Power Off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-Off ramp time

3.4 Mode Register Definition

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM

Table 11 shows the mode registers for LPDDR4X-NVM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 11 — Mode Register Assignment in LPDDR4X-NVM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CATR	~~SCLS~~	~~SE mode~~	RZQI		~~RFM Support~~	~~Latency Mode~~	~~Refresh mode~~
1	RPST	~~nWR (for AP)~~			RD-PRE	~~WR PRE~~	BL	
2	~~WR Lev~~	~~WLS~~	~~WL~~			RL		
3	~~DBI-WR~~	ECCO-RD	PDDS			~~PPRP~~	~~WR PST~~	PU-CAL
4	Temperature Sensor Data							
5	LPDDR4X-NVM Manufacturer ID							
6	Revision ID-1							
7	Revision ID-2							
8	IO Width		Density				Type	
9	~~Manufacturer Specific Test Register~~							
10	~~RFU~~							ZQ-Reset
11	~~Reserved~~	CA ODT			~~Reserved~~	~~DQ ODT~~		
12	~~CBT Mode for Byte Mode~~	VR-CA	V_{REF}CA					
13	FSP-OP	FSP-WR	~~DMD~~	~~RRO~~	VRCG	VRO	RPT	CBT
14	~~RFU~~	~~VR(dq)~~	~~V_{REF}(DQ)~~					
15	Lower-Byte Invert Register for DQ Calibration							
16	~~PASR Bank Mask~~							
17	~~PASR Segment Mask~~							
18	~~DQS Oscillator Count - LSB~~							
19	~~DQS Oscillator Count - MSB~~							
20	Upper-Byte Invert Register for DQ Calibration							
21	~~RFU~~							
22	~~ODTD for x8 2ch(Byte) mode~~	ODTD-CA	ODTE-CS	ODTE-CK		SOC ODT		
23	~~DQS interval timer run time setting~~							
24	~~RAAMMT~~	~~RAAIMT~~						~~RFM~~
25	~~PPR Resource~~							
26	~~RFU~~						~~SCL~~	
27	~~RFU~~							
28	~~RFU~~							
29	~~RFU~~							
30	~~Reserved for testing - SDRAM will ignore~~							
31	~~Bytemode Vref Selection~~	~~RFU~~						
32	DQ Calibration Pattern “A” (default = 5AH)							
33	~~RFU~~							
34	~~RFU~~							
35	~~RFU~~							
36	~~RFU~~							~~RAADEC~~
37	~~RFU~~							
38	~~RFU~~							
39	~~Reserved for testing - SDRAM will ignore~~							
40	DQ Calibration Pattern “B” (default = 3CH)							
41-63	~~RFU~~							

NOTE 1 The grayed out address/field entries are RESERVED FOR FUTURE USE (RFU) for the LPDDR4X-NVM device but may have been used (or RFU) in LPDDR4 DRAM devices.

NOTE 2 The register fields shown in light green are set up as Frequency Set Point (FSP) register pairs for use during bus training (see Section 4.15).

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (c ont'd)

Table 12 — MR0 Register Information (MA[5:0] = 00_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CATR	RFU		RZQI		RFU		

Table 13 — MR0 Register Functions

Function	Register Type	Operand	Data	Notes
RZQI (Built-in Self-Test for RZQ)	Read Only	OP[4:3]	00_B: RZQ Self-Test Not Supported 01_B: ZQ pin may connect to V_{SSQ} or float 10_B: ZQ-pin may short to V_{DDQ} 11_B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to V_{SSQ} or float, nor short to V_{DDQ})	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	0_B: CA for this rank is not terminated 1_B: Manufacturer specific	5

NOTE 1 RZQI MR value, if supported, will be valid after the following sequence:
a. MPC ZQCal Start followed by tZQCAL followed by MPC ZQCal Latch followed by tZQLAT.
b. RZQI value will be lost after Reset.

NOTE 2 If the ZQ-pin is connected to V_{SSQ} to set default calibration, OP[4:3] shall be set to 01_B. If the ZQ-pin is not connected to V_{SSQ}, either OP[4:3] = 01_B or OP[4:3] = 10_B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

NOTE 3 In the case of possible assembly error, the LPDDR4X-NVM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.

NOTE 4 If ZQ Self-Test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).

NOTE 5 CATR functionality is Manufacturer specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the manufacturer device datasheet for details.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 14 — MR1 Register Information (MA[5:0] = 01_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST	RFU			RD-PRE	RFU	Burst Length	

Table 15 — MR1 Register Functions

Function	Register Type	Operand	Data	Notes
Burst Length	Write Only	OP[1:0]	00_B: BL=16 Sequential (default) 01_B: BL=32 Sequential Others: Reserved	1
RD-PRE (RD Preamble Type)		OP[3]	0_B: RD Preamble = Static (default) 1_B: RD Preamble = Toggle	2,4,5
RPST (RD Postamble Length)		OP[7]	0_B: RD Postamble = 0.5*tCK (default) 1_B: RD Postamble = 1.5*tCK	3,4,5

NOTE 1 On-The-Fly Burst Length functionality is not supported.

NOTE 2 For Read operations this bit must be set to select between a "toggling" preamble and a "Non-toggling" Preamble. See 4.3, Read Preamble and Postamble, for a drawing of each type of preamble.

NOTE 3 OP[7] provides an optional READ postamble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.

NOTE 4 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be read from with an MRR command to this MR address.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 16 — Burst Sequence for Legacy JEDEC Read and Modified JEDEC Read (ACT1-ACT2-RD-CAS2)

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																		
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																			
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																			
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																			
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																			
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

NOTE 1 C0-C1 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 The starting burst address is on 64-bit boundaries.

Table 17 — Burst Sequence for Non-Volatile READ (NVR1-NVR2)

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																		
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	NA	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																			
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

NOTE 1 For BL-16: C0-C3 are assumed to be '0', and are not transmitted on the command bus.

NOTE 2 For BL-16: The starting burst address is on 256-bit boundaries.

NOTE 3 For BL-16: There is no C4.

NOTE 4 For BL-32: C0-C4 are assumed to be '0', and are not transmitted on the command bus.

NOTE 5 For BL-32: The starting burst address is on 512-bit boundaries.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 18 — MR2 Register Information (MA[5:0] = 02_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU					RL		

Table 19 — MR2 Register Functions

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write Only	OP[2:0]	000_B: RL=6 (default) 001_B: RL=12 010_B: RL=16 011_B: RL=22 100_B: RL=28 101_B: RL=32 110_B: RL=36 111_B: RL=40	1,2,3

NOTE 1 See Section 4.8 Read Latencies for detail.

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 20 — MR3 Register Information (MA[5:0] = 03_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	ECCO-RD	PDDS			RFU		PU-CAL

Table 21 — MR3 Register Functions

Function	Register Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write Only	OP[0]	0B: VDDQ*0.6 1B: VDDQ*0.5 (default)	1
PDDS (Pull-Down Drive Strength)		OP[5:3]	000B: RFU 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 (default) 111B: Reserved	1,2,3
ECCO-RD (ECC Output Enable)		OP[6]	0B: Disabled (default) 1B: Enabled	2,3,4

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
NOTE 4 When enabled (OP[6]=1B) ECC information is output on the ECCO signal for the device. See Section 10.7 LPDDR4X-NVM Error Correction Code Output.

Table 22 — MR4 Register Information (MA[5:0] = 04_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Temperature Sensor Data (TSD)							

Table 23 — MR4 Register Functions

Function	Register Type	Operand	Data	Notes
Temperature Sensor Data (TSD)	Read Only	OP[7:0]	Most recent temperature measurement	1,2

NOTE 1 Temperature sensing is initiated over the SPI bus.
NOTE 2 See Section 4.19 for details.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 24 — MR5 Register Information (MA[5:0] = 05_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
LPDDR4X-NVM Manufacturer ID							

Table 25 — MR5 Register Functions

Function	Register Type	Operand	Data	Notes
Manufacturer ID	Read Only	OP[7:0]	See JEP166, Manufacturer ID Codes	

Table 26 — MR6 Register Information (MA[5:0] = 06_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Table 27 — MR6 Register Functions

Function	Register Type	Operand	Data	Notes
LPDDR4X-NVM Rev ID-1	Read Only	OP[7:0]	xxxx $xxxx_B$: Manufacturer Specific- Rev ID-1	1
NOTE 1 MR6 is manufacturer specific.				

Table 28 — MR7 Register Information (MA[5:0] = 07_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Table 29 — MR7 Register Functions

Function	Register Type	Operand	Data	Notes
LPDDR4X-NVM Rev ID-2	Read Only	OP[7:0]	xxxx $xxxx_B$: Manufacturer Specific- Rev ID-2	1
NOTE 1 MR7 is manufacturer specific.				

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 30 — MR8 Register Information (MA[5:0] = 08_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width		Density				Type	

Table 31 — MR8 Register Functions

Function	Register Type	Operand	Data	Notes
Type	Read Only	OP[1:0]	00_B: 32 byte row size 01_B: 64 byte row size All Others: Reserved	
Density		OP[5:2]	Density= 1Mb x 2^n 0000_B: n=0, Density= 1Mb x 2^0 = 1Mb 0001_B: n=1, Density= 1Mb x 2^1 = 2Mb . . . 1111_B: n=15, Density= 1Mb x 2^{15} = 32Gb	
IO Width		OP[7:6]	00_B: x16 (per channel) All Others: Reserved	

Table 32 — MR10 Register Information (MA[5:0] = $0A_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							ZQ-Reset

Table 33 — MR10 Register Functions

Function	Register Type	Operand	Data	Notes
ZQ-Reset	Write Only	OP[0]	0_B: Normal Operation (Default) 1_B: ZQ Reset	1,2

NOTE 1 See Table 86, ZQCal Timing Parameters for calibration latency and timing.
NOTE 2 If the ZQ-pin is connected to V_{DDQ} through R_{ZQ}, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 34 — MR11 Register Information (MA[5:0] = $0B_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved	CA ODT			Reserved			

Table 35 — MR11 Register Functions

Function	Register Type	Operand	Data	Notes
CA ODT (CA Bus Receiver On-Die-Termination)	Write Only	OP[6:4]	000B: Disable (Default) 001B: RZQ/1 010B: RZQ/2 011B: RZQ/3 100B: RZQ/4 101B: RZQ/5 110B: RZQ/6 111B: RFU	1,2,3

NOTE 1 All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 36 — MR12 Register Information (MA[5:0] = $0C_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR-CA	VREFCA					

Table 37 — MR12 Register Functions

Function	Register Type	Operand	Data	Notes
VREFCA (VREFCA Setting)	Read/ Write	OP[5:0]	000000B: -- Through -- 110010B: See table below (011101B: default) All Others: Reserved	1,2,3, 5,6
VR-CA (VREFCA Range)		OP[6]	0B: VREFCA Range[0] enabled 1B: VREFCA Range[1] enabled (default)	1,2,4, 5,6

NOTE 1 This register controls the V_{REF}CA levels. Refer to Table 38 - VREF Settings for Range[0] and Range[1] for actual voltage of V_{REF}CA.

NOTE 2 A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See Section 4.10 on MRR Operation.

NOTE 3 A write to OP[5:0] sets the internal V_{REF}CA level for FSP[0] when MR13 OP[6]=0_B, or sets the internal VrefCA level for FSP[1] when MR13 OP[6]=1_B. The time required for V_{REF}CA to reach the set level depends on the step size from the current level to the new level. See Section 4.13 on V_{REF}CA training for more information.

NOTE 4 A write to OP[6] switches the LPDDR4X-NVM between two internal V_{REF}CA ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}CA register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.

NOTE 5 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with a MRR command to this address.

NOTE 6 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 38 — V_{REF}CA Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (% of V_{DDQ})				Range[1] Values (% of V_{DDQ})				Notes
V_{REF}CA Settings for MR12	OP[5:0]	000000_B	15.0%	011010_B	30.5%	000000B	32.9%	011010_B	48.5%	1,2,3,4
		000001_B	15.6%	011011_B	31.1%	000001B	33.5%	011011_B	49.1%	
		000010_B	16.2%	011100_B	31.7%	000010_B	34.1%	011100_B	49.7%	
		000011_B	16.8%	011101_B	32.3%	000011_B	34.7%	011101_B default	50.3%	
		000100_B	17.4%	011110_B	32.9%	000100_B	35.3%	011110_B	50.9	
		000101_B	18.0%	011111_B	33.5%	000101_B	35.9%	011111_B	51.5%	
		000110_B	18.6%	100000_B	34.1%	000110_B	36.5%	100000_B	52.1%	
		000111_B	19.2%	100001_B	34.7%	000111_B	37.1%	100001_B	52.7%	
		001000_B	19.8%	100010_B	35.3%	001000_B	37.7%	100010_B	53.3%	
		001001_B	20.4%	100011_B	35.9%	001001_B	38.3%	100011_B	53.9%	
		001010_B	21.0%	100100_B	36.5%	001010_B	38.9%	100100_B	54.5%	
		001011_B	21.6%	100101_B	37.1%	001011_B	39.5%	100101_B	55.1%	
		001100_B	22.2%	100110_B	37.7%	001100_B	40.1%	100110_B	55.7%	
		001101_B	22.8%	100111_B	38.3%	001101_B	40.7%	100111_B	56.3%	
		001110_B	23.4%	101000_B	38.9%	001110_B	41.3%	101000_B	56.9%	
		001111_B	24.0%	101001_B	39.5%	001111_B	41.9%	101001_B	57.5%	
		010000_B	24.6%	101010_B	40.1%	010000_B	42.5%	101010_B	58.1%	
		010001_B	25.1%	101011_B	40.7%	010001_B	43.1%	101011_B	58.7%	
		010010_B	25.7%	101100_B	41.3%	010010_B	43.7%	101100_B	59.3%	
		010011_B	26.3%	101101_B	41.9%	010011_B	44.3%	101101_B	59.9%	
		010100_B	26.9%	101110_B	42.5%	010100_B	44.9%	101110_B	60.5%	
		010101_B	27.5%	101111_B	43.1%	010101_B	45.5%	101111_B	61.1%	
		010110_B	28.1%	110000_B	43.7%	010110_B	46.1%	110000_B	61.7%	
		010111_B	28.7%	110001_B	44.3%	010111_B	46.7%	110001_B	62.3%	
		011000_B	29.3%	110010_B	44.9%	011000_B	47.3%	110010_B	62.9%	
		011001_B	29.9%	All Others: Reserved		011001_B	47.9%	All Others: Reserved		

NOTE 1 These values may be used for MR12 OP[5:0] to set the V_{REF}CA levels in the LPDDR4x-NVM.

NOTE 2 The range may be selected in the MR12 register by setting OP[6] appropriately.

NOTE 3 The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA are provided to allow for faster switching between terminated and un-terminated operation, or between different high frequency settings which may use different terminations values.

NOTE 4 Voltage step size is 0.6% (1/167).

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 39 — MR13 Register Information (MA[5:0] = $0D_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	RFU	RFU	VRCG	VRO	RPT	CBT

Table 40 — MR13 Register Functions

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write Only	OP[0]	0_B: Normal Operation (default) 1_B: Command Bus Training Mode Enabled	1
RPT (Read Preamble Training Mode)		OP[1]	0_B : Disable (default) 1_B : Enable	
VRO (V_{REF} Output)		OP[2]	0_B: Normal operation (default) 1_B: Output the V_{REF}CA value on DQ bits	2
VRCG (V_{REF} Current Generator)		OP[3]	0_B: Normal Operation (default) 1_B: V_{REF} Fast Response (high current) mode	3
FSP-WR (Frequency Set Point Write/Read)		OP[6]	0_B: Frequency-Set-Point[0] (default) 1_B: Frequency-Set-Point [1]	4
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0_B: Frequency-Set-Point[0] (default) 1_B: Frequency-Set-Point [1]	5

NOTE 1 A write to set OP[0]=1 causes the LPDDR4X-NVM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See Section 4.14 on Command Bus Training for more information.

NOTE 2 When set, the LPDDR4X-NVM will output the V_{REF}CA voltage on DQ pins. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF}CA levels. The DQ pins used for V_{REF}CA output are manufacturer specific.

NOTE 3 When OP[3]=1, the V_{REF}CA circuit uses a high-current mode to improve V_{REF}CA settling time.

NOTE 4 FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V_{REF}CA Setting, V_{REF}CA Range. For more information, refer to Section 4.15, Frequency Set Point.

NOTE 5 FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V_{REF}CA Setting, V_{REF}CA Range. For more information, refer to Section 4.15 Frequency Set Point section.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 41 — MR15 Register Information (MA[5:0] = $0F_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-Byte Invert Register for DQ Calibration							

Table 42 — MR15 Register Functions

Function	Register Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write Only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55H	1,2,3
NOTE 1 This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted. NOTE 2 ECCO[0] is not inverted, and always transmits the "true" data contained in MR32/MR40. NOTE 3 No ECC Output function is enacted during DQ Read Calibration, even if ECCO is enabled in MR3-OP[6].				

Table 43 — MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	ECCO[0]	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 44 — MR20 Register Information (MA[5:0] = 14_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper-Byte Invert Register for DQ Calibration							

Table 45 — MR20 Register Functions

Function	Register Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write Only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0B: Do not invert 1B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55H	1,2,3
NOTE 1 This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted. NOTE 2 ECCO[1] is not inverted, and always transmits the "true" data contained in MR32/MR40. NOTE 3 No ECC Output function is enacted during DQ Read Calibration, even if ECCO is enabled in MR3-OP[6].				

Table 46 — MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	ECCO[1]	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 47 — MR22 Register Information (MA[5:0] = 16_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

Table 48 — MR22 Register Functions

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write Only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 (illegal if MR3 OP[0]=0_B) 010_B: RZQ/2 011_B: RZQ/3 (illegal if MR3 OP[0]=0_B) 100_B: RZQ/4 101_B: RZQ/5 (illegal if MR3 OP[0]=0_B) 110_B: RZQ/6 (illegal if MR3 OP[0]=0_B) 111_B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non-terminating rank)		OP[3]	0_B: ODT-CK Enabled (Default) 1_B: ODT-CK Disabled	2,3,4
ODTE-CS (CS ODT enable for non-terminating rank)		OP[4]	0B: ODT-CS Enabled (Default) 1B: ODT-CS Disabled	2,3,4
ODTD-CA (CA ODT termination disable)		OP[5]	0_B: ODT-CA Enabled (Default) 1_B: ODT-CA Disabled	2,3,4

NOTE 1 All values are "typical".

NOTE 2 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.

NOTE 3 There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

NOTE 4 The ODT_CA signal has been eliminated on the LPDDR4X-NVM device. The legacy package location for ODT_CA has been changed to RFU.

3.4.1 Mode Register Assignment and Definition in LPDDR4X-NVM (cont'd)

Table 49 — MR32 Register Information (MA[5:0] = 20_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "A" (default = 5AH)							

Table 50 — MR32 Register Functions

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write Only	OP[7:0]	X_B: An MPC command with OP[6:0]= 1000011_B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "$5A_H$"is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	

Table 51 — MR40 Register Information (MA[5:0] = 28H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B" (default = 3CH)							

Table 52 — MR40 Register Functions

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write only	OP[7:0]	XB: A default pattern "3CH" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3, 4

NOTE 1 The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and ECCO[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H , then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B.

NOTE 2 MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the ECCO[1:0] pins.

NOTE 3 The data pattern is not transmitted on the ECCO[1:0] pins if ECCO-RD is disabled via MR3-OP[6].

NOTE 4 No ECC Output function is enacted during DQ Read Calibration, even if ECCO is enabled in MR3-OP[6].

4 Command Definitions and Timing Diagrams

4.1 READ Operations

Read operations on LPDDR4X-NVM devices need to consider the fundamental differences between DRAM and nonvolatile memory array architectures. The initial LPDDR4X-NVM expectation is for either a 32 or 64 byte (256b/512b) row as compared with the 2K byte rows found in LPDDR4 DRAM devices. The smaller row size results in a dramatically higher row count than LPDDR4X DRAM devices of a given density. The higher row count makes it difficult to fit within the legacy Active transactions (ACT-1/ACT-2) used with LPDDR4X DRAM. The placement of the row (and column) bits are supported by the different READ transactions described below.

The LPDDR4X-NVM specification describes four different read transaction formats.

1. Legacy JEDEC READ - supported in devices that have fast NVM
2. Non-Volatile READ - Modified read sequence to minimize CA bus overhead for fast NVM
3. Modified JEDEC READ - remapped row bits to accommodate longer latency NVM
4. Modified JEDEC READ with PRE-ACTIVATE - Adding new command to extend density range

LPDDR4X-NVM devices are expected to support only one of the READ transactions as a part ordering option. The READ transaction format supported will largely depend upon array read access time and device density.

The LPDDR4X-NVM device begins the target data retrieval only after the target row is fully identified during the command cycles. Note that an LPDDR4X read transaction using a burst length of 16 or 32 beats (BL16, BL32) is able to retrieve the entire LPDDR4X-NVM row that has been specified. Once the target row has been identified, the LPDDR4X-NVM device retrieves the target data and is ready to output the data according to the Read Latency (RL) setting in Mode Register 2. The retrieved data is output in a manner that is identical to LPDDR4X DRAM devices with the expected preamble, postamble, pipelining and merging behavior. Preamble and postamble behavior is specified using Mode Register 1. A read operation will initiate a burst read operation, where data is transferred from the LPDDR4X-NVM device on successive clock cycles. Burst interrupts are not supported. For the Legacy JEDEC READ and the Non-Volatile READ, the row is considered “closed” upon retrieval of the target data and the target bank becomes available for the next read request. For the Modified JEDEC READ, a row can be considered “open” and the ACT1-ACT2 commands are not required if the same row is accessed in the next READ operation. For all of the read transactions there is no need for a precharge operation prior to performing a subsequent “activate/read” operation.

4.1.1 Legacy JEDEC READ Sequence

The Legacy JEDEC READ sequence (shown in Figure 11) follows the JEDEC LPDDR4X series of commands (ACT1-ACT2-RD1-CAS2). Note that the retrieval of the target data is delayed until the target row is identified during the CAS2 command. The time required between the Active (ACT1-ACT2) and the Read (RD1-CAS2) is reduced to four clocks (tRCD=4nCK) to allow for the proper sequencing of the required commands. While a tRCD of more than four clocks is allowed, it is recommended that the Activate (ACT1-ACT2) commands be immediately followed by the Read (RD1-CAS2) commands to minimize overall read latency. Once the target row has been identified, the retrieval process will have the target data ready to be output according the Read Latency (RL) setting. The starting location within the read burst is specified by the two least significant column address bits (for BL16) and three least significant bits (for BL32) provided by the CAS2 command.

The minimum time interval between ACTIVATE commands to the same bank (or sub-bank) is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

4.1.2 Non-Volatile READ Sequence

The Non-Volatile READ sequence (shown in Figure 12) is a performance enhancement that reduces read transaction overhead on the CA bus from eight clocks (JEDEC READ) down to four clocks. The four clock reduction is accomplished by placing all of the target row bits into the NVR1 and NVR2 commands. The NVR transaction strategy has a maximum density limitation of 2Gb (32B rows) or 4Gb (64B rows) which is adequate for many applications targeted by the LPDDR4X-NVM device. One way to think of the NVR sequence is as a “pseudo-ACTIVATE” command that launches a read operation once the target row is identified. Once the target row has been identified, the retrieval process will have the target data ready to be output according the Read Latency (RL) setting. The timings used during the Non-Volatile READ sequence (NVR-1 - NVR-2) are identical to the (RD-1 - CAS-2) timings used during the JEDEC READ sequences (compare Figure 11 and Figure 12 as an example). The Non-Volatile READ sequence does not specify a “column” addresses and always starts with the least significant word of the burst length.

4.1.3 Modified JEDEC READ Sequence

The Modified JEDEC READ sequence (shown in Figure 13) follows the JEDEC LPDDR4X series of commands (ACT1-ACT2-RD1-CAS2). Note that the retrieval of the target data is initiated when the target row is identified during the ACT2 command. The time required between the Active (ACT1-ACT2) and the Read (RD1-CAS2) is specified as tRCD and allows for an extended period of time to retrieve the target row from the NVM array. Once the target data has been retrieved (after tRCD), the RD1-CAS2 is issued and the target data begins to be output on the DQs after RL clock cycles. The starting location within the read burst is specified by the two least significant column address bits (for BL16) and three least significant bits (for BL32) provided by the CAS2 command.

The Modified JEDEC READ requires that the “row” address bits be completely described in the ACT1-ACT2 command cycles. This requirement means that only the lowest order column bits remain in the RD1-CAS2 cycles and the upper order (DRAM) column bits migrate to the low order row bits in the ACT1-ACT2 cycles. The row bits that normally reside in the ACT1-ACT2 cycles are “pushed up” in the row sequencing.

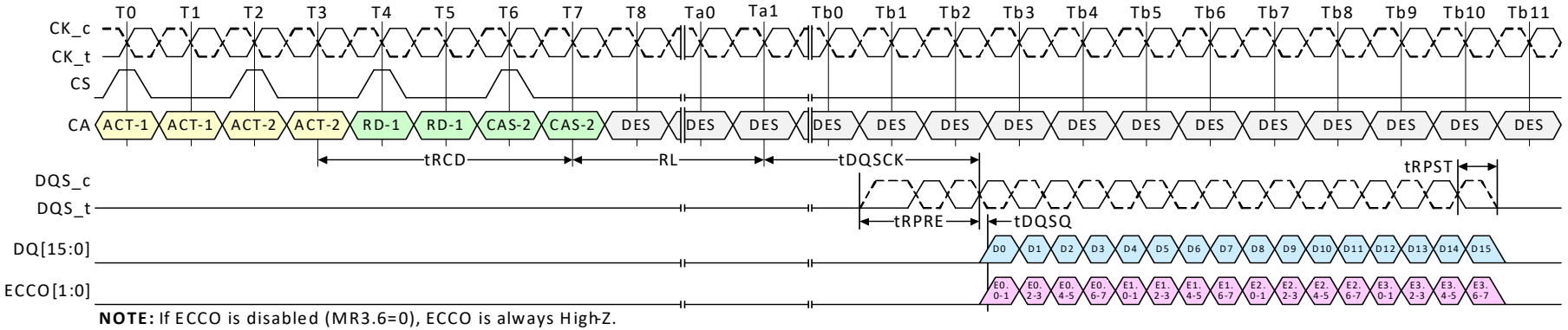
The minimum time interval between ACTIVATE commands to the same bank (or sub-bank) is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

4.1.4 Modified JEDEC READ with PRE-ACTIVATE Sequence

A PRE-ACTIVATE command is optionally supported for the Modified JEDEC READ to increase the number of row addresses (Figure 14). A READ transaction using the PRE-ACTIVATE command is sequenced as: PRE-ACT1-ACT2-RD-CAS2 and allows for support of densities up to 32Gb. The PRE-ACTIVATE command is expected to be placed on the command bus prior to the normal ACT1-ACT2 commands to specify a upper order row addresses within the target bank. The row bits from the PRE-ACTIVATE and the subsequent ACT1-ACT2 completely identify the target row within the specified bank. The timings are identical to the Modified JEDEC READ sequence except for the addition of the (two clock) PRE-ACTIVATE placement on the CA bus.

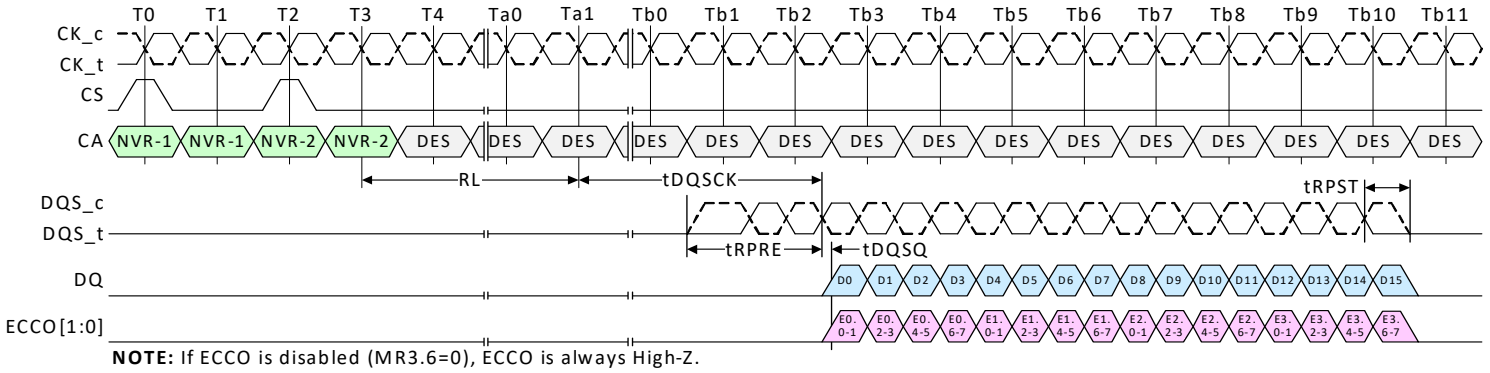
4.1.5 ECC over ECCO *(re-purposed Data Mask Inversion (DMI) from LPDDR4 DRAM)*

LPDDR4X-NVM devices repurpose the legacy DMI pin to transport Error Correction Code (ECC) syndrome information from the memory to the host during READ transactions. The DMI[1:0] signals have been renamed Error Correction Code Out (ECCO[1:0]). Syndrome information is transported over both ECCO[1:0] signals while the DQ[15:0] bus is sending data. The syndrome information resides in the user NVM array along with its corresponding data. 32 bits of syndrome information is transported during a BL16 (32B) READ transaction and 64 bits of syndrome information is transported during a BL32 (64B) READ transaction. The syndrome information is defined by the customer and is programmed along with the data into the NVM array. Syndrome information is output during READ transactions as shown in Figure 11 through Figure 14.



NOTE: If ECCO is disabled (MR3.6=0), ECCO is always High-Z.

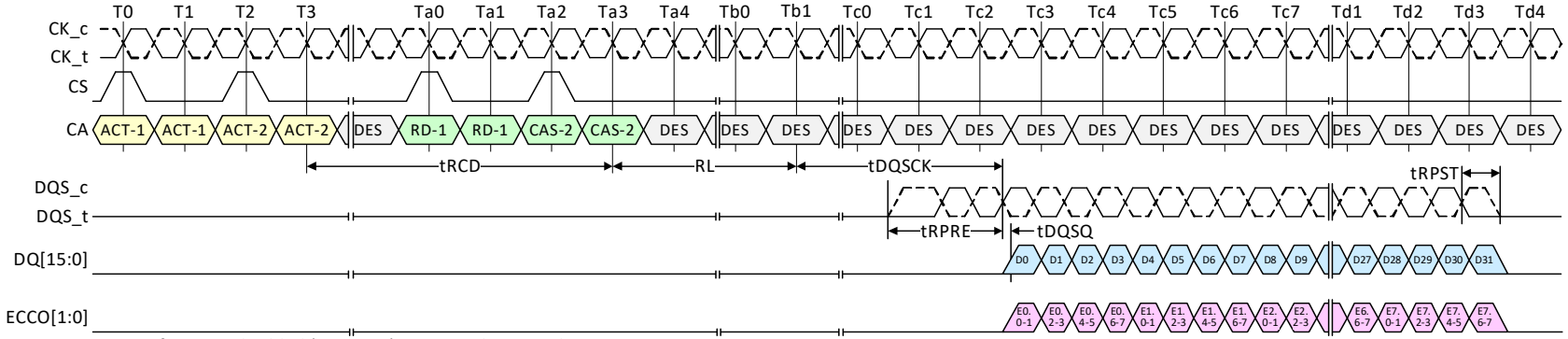
Figure 11 — Legacy JEDEC READ Transaction (BL16 shown)



NOTE: If ECCO is disabled (MR3.6=0), ECCO is always High-Z.

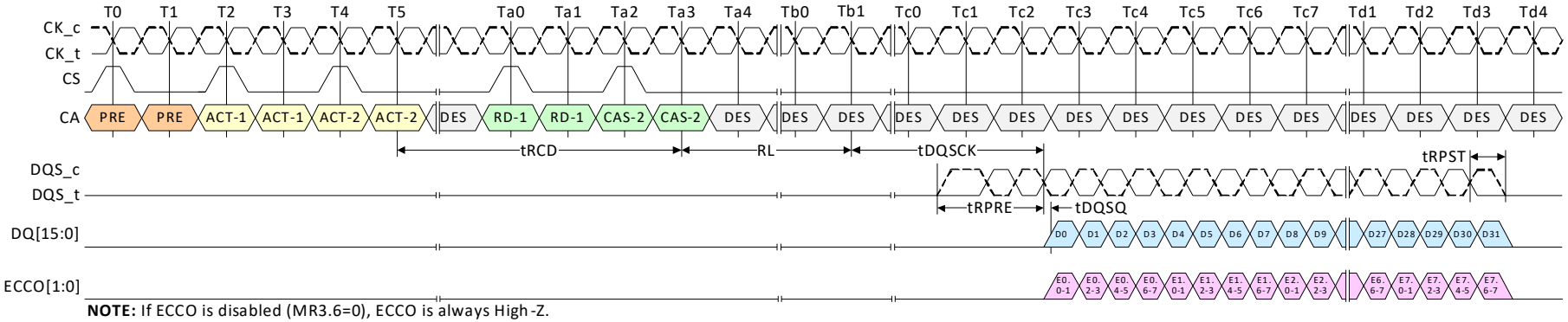
Figure 12 — Non-Volatile READ Transaction (BL16 shown)

4.1.5 ECC over ECCO (cont'd)



NOTE: If ECCO is disabled (MR3.6=0), ECCO is always High-Z.

Figure 13 — Modified JEDEC READ Transaction (BL32 shown)



NOTE: If ECCO is disabled (MR3.6=0), ECCO is always High-Z.

Figure 14 — Modified JEDEC READ Transaction Using PRE-ACTIVATE (BL32 shown)

4.1.6 ACTIVATE (ACT) Command

The ACTIVATE command launches a READ transaction sequence. The ACTIVATE command, Figure 15, is composed of two consecutive commands, Activate-1 command and Activate-2. The Activate-1 command is issued by holding CS HIGH, CA0 HIGH and CA1 LOW at the first rising edge of the clock and the Activate-2 command issued by holding CS HIGH, CA0 HIGH and CA1 HIGH at the first rising edge of the clock. The bank addresses BA0, BA1 and BA2 are used to select the desired bank. Row addresses are used to determine which row to activate within the selected bank. The ACTIVATE command must be applied before a READ operation can be executed. The device can accept a READ command at tRCD after the ACTIVATE command is issued.

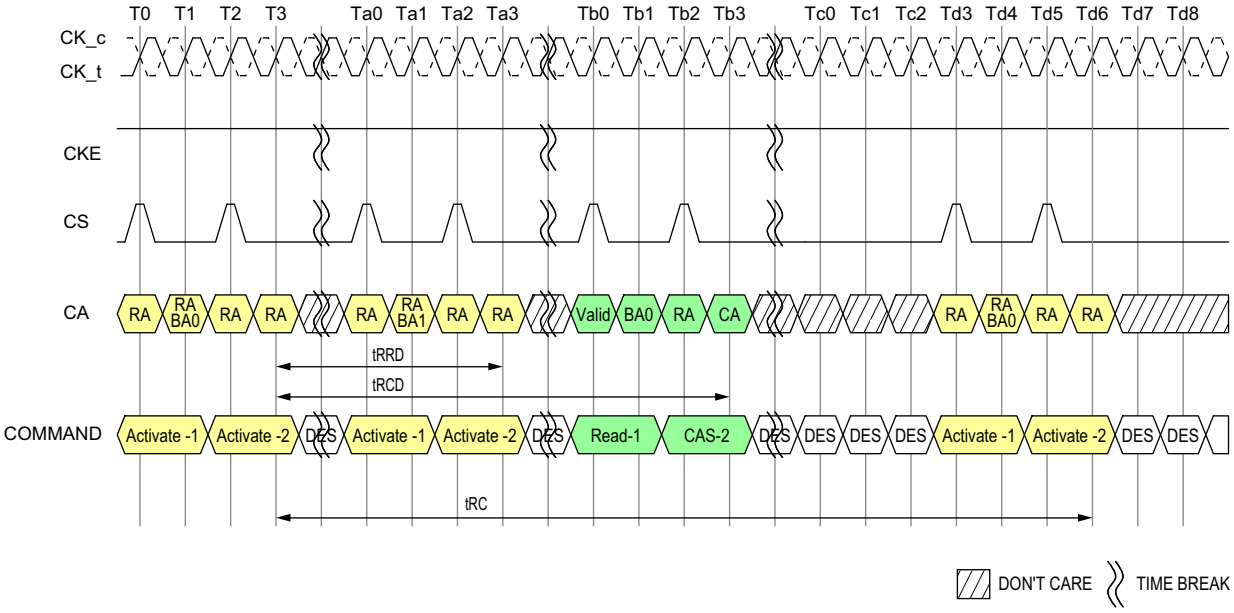


Figure 15 — ACTIVATE (ACT) Command

4.1.7 PRE-ACTIVATE (PRE) Command

The PRE-ACTIVATE (PRE) command is optionally included in devices that support the Modified JEDEC READ command. The PRE command allows for up to five additional row address bits. These additional row bits allow for support of device densities up to 32Gb. The PRE command is issued prior to the ACT1-ACT2 commands to fully identify the target row within the target bank. It is suggested (but not required) that the PRE command be issued immediately prior to the ACT1 command to minimize the overall latency of a read operation.

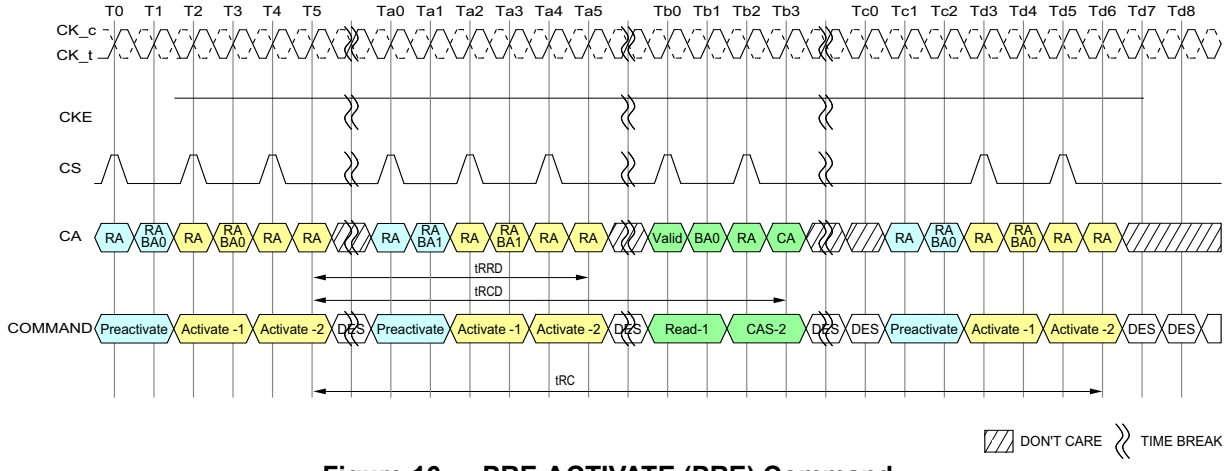


Figure 16 — PRE-ACTIVATE (PRE) Command

4.1.8 Non-Volatile READ (NVR) Command

The optional Non-Volatile READ (NVR) command launches a READ transaction that requires a smaller footprint on the Command Address bus when compared with the JEDEC READ operation. The NVR READ sequence is shown in Figure 14. The NVR READ consumes four clocks to specify the target bank and row. This four clock NVR launch overhead (NVR1-NVR2) compares with eight clocks required for the JEDEC READ transaction (ACT1-ACT2-RD1-CAS2). The four clock savings results in a significant reduction in the time taken to retrieve target data from the LPDDR4X-NVM device. The timing constraints for NVR READs between banks (tRCN) and within the same bank (tRRDN) is shown in Figure 17.

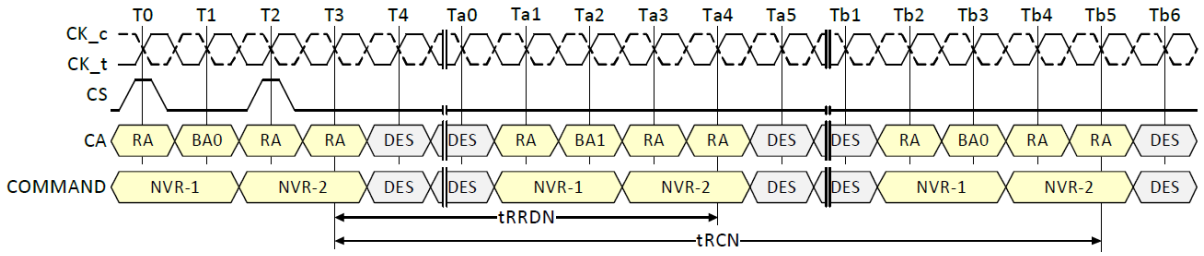


Figure 17 — Non-Volatile READ (NVR) Command

4.2 Core Timing

Table 53 presents the Core AC timings.

Table 53 — Core AC Timings

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note
Core Parameters			**533**	**1066**	**1600**	**2133**	**2667**	**3200**	**3733**	**4266**		
Exit Power-Down to next valid command delay	tXP	MIN	max(7.5ns, 5nCK)								ns	
Legacy JEDEC READ												
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	max(MSV, 8nCK)								ns	3
CAS-to-CAS delay	tCCD	MIN	BL/2								tCK(avg)	
RAS-to-CAS delay	tRCD	MIN	4								tCK(avg)	
Active bank-A to active bank-B	tRRD	MIN	4								tCK(avg)	2
Non-Volatile READ												
NVR to NVR (bank-A to bank-A)	tRCN	MIN	max(MSV, 8nCK)								ns	3
NVR to NVR (bank-A to bank-B)	tRRDN	MIN	BL/2								tCK(avg)	
Modified JEDEC READ												
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	max(MSV, 8nCK)								ns	3
CAS-to-CAS delay	tCCD	MIN	BL/2								tCK(avg)	
RAS-to-CAS delay	tRCD	MIN	max(MSV, 4nCK)								ns	1
Active bank-A to active bank-B	tRRD	MIN	4								tCK(avg)	2
Modified JEDEC READ Using PRE-ACTIVATE												
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	max(MSV, 10nCK)								ns	3
CAS-to-CAS delay	tCCD	MIN	BL/2								tCK(avg)	
RAS-to-CAS delay	tRCD	MIN	max(MSV, 4nCK)								ns	1
Active bank-A to active bank-B	tRRD	MIN	6								tCK(avg)	2

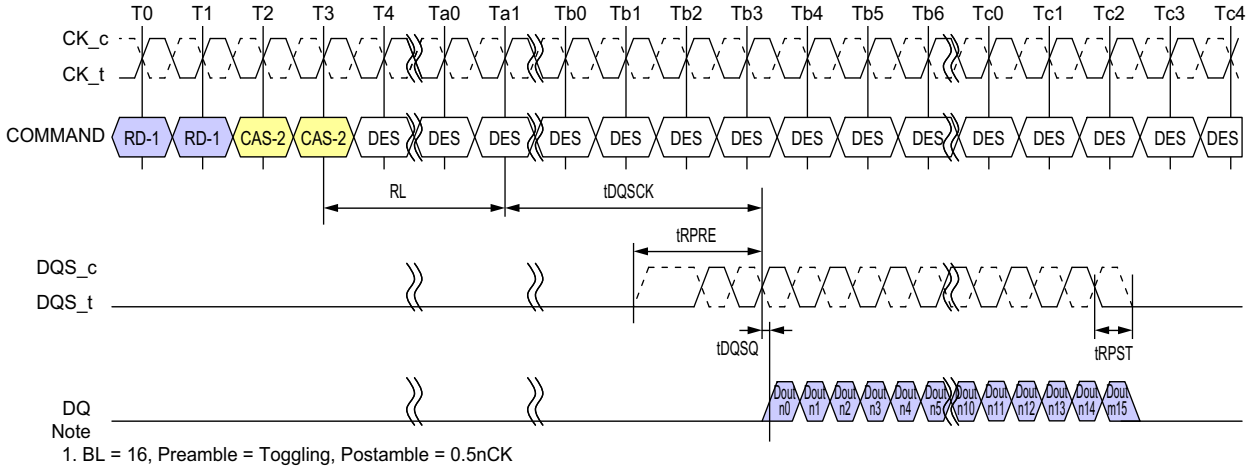
NOTE 1 Longer latency NVM technologies will require the extended tRCD allowed in the Modified JEDEC READ transaction.
NOTE 2 Devices supporting 4266 Mbps specification shall support these timings at lower data rates.
NOTE 3 MSV (Manufacturer Specific Values) are specified in the READ-ID Table (Table 135).

4.3 Read Preamble and Postamble

The DQS strobe for the LPDDR4X-NVM (Figure 18 and Figure 19) requires a preamble prior to the first latching edge (the rising edge of DQS_t with DATA "valid"), and it requires a postambleble after the last latching edge. The preamble and postamble lengths are set via mode register writes (MRW). While the figures show a BL16 transaction, BL32 burst lengths are also supported.

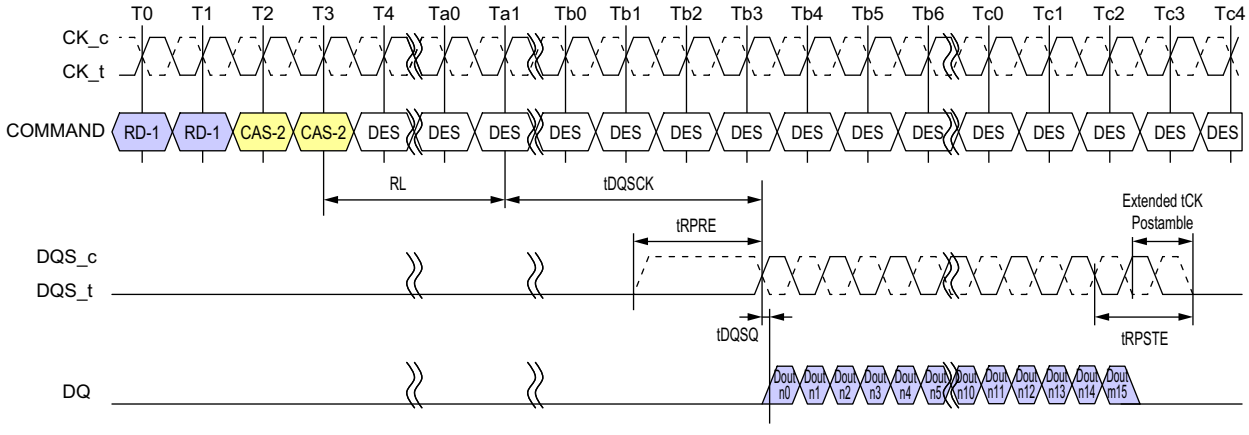
For READ operations the preamble is 2*tCK, but the preamble is static (no-toggle) or toggling, selectable via mode register.

LPDDR4X-NVM will have a DQS Read postamble of 0.5*tCK (or extended to 1.5*tCK). Standard DQS postamble will be 0.5*tCK driven by the device for Reads. A mode register setting instructs the device to drive an additional (extended) one cycle DQS Read postamble. The drawings below show examples of DQS Read postamble for both standard (tRPST) and extended (tRPSTE) postamble operation.



Note
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS and DQ terminated to VSSQ.
3. DQS_t/DQS_c is "don't care" prior to the start of tRPRE.
   No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure 18 — DQS Read Preamble and Postamble: Toggling Preamble and 0.5nCK Postamble

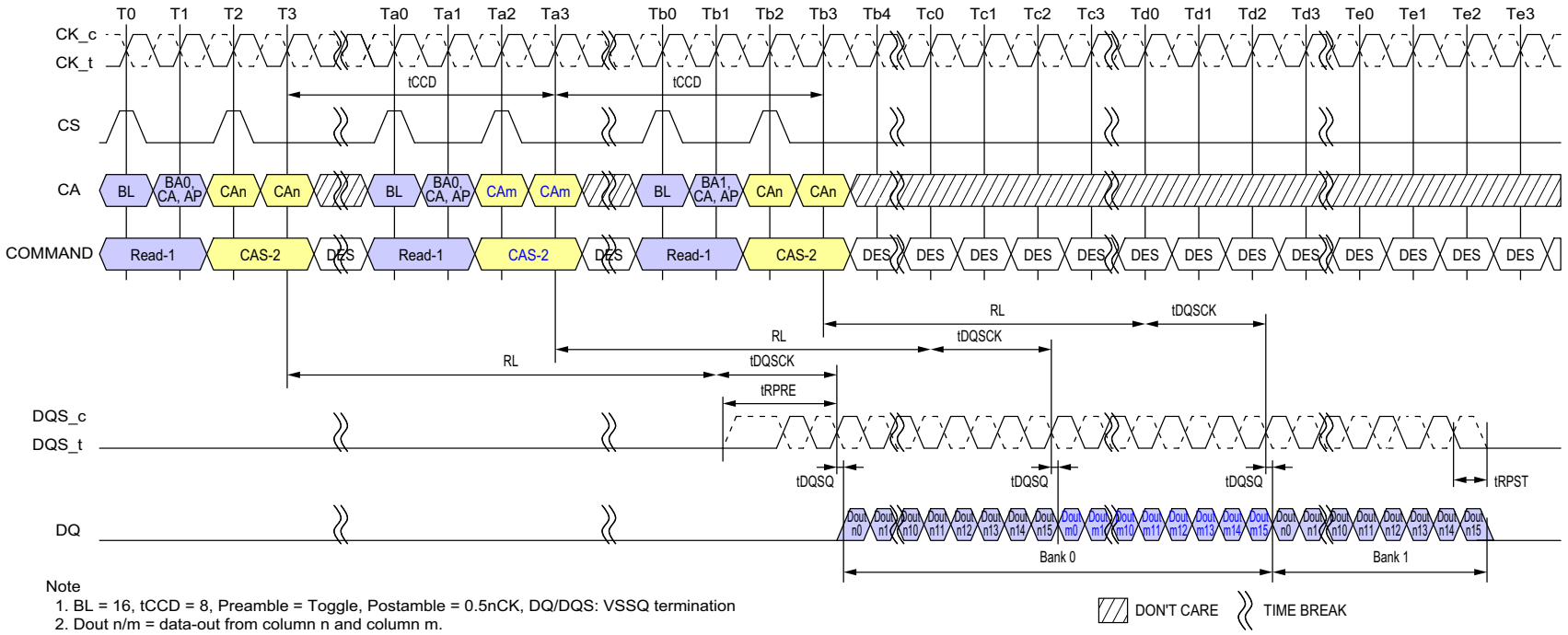


Note
1. BL = 16, Preamble = Static, Postamble = 1.5nCK (Extended)
2. DQS and DQ terminated to VSSQ.
3. DQS_t/DQS_c is "don't care" prior to the start of tRPRE.
   No transition of DQS is implied, as DQS_t/DQS_c can be HIGH, LOW, or HI-Z prior to tRPRE.

Figure 19 — DQS Read Preamble and Postamble: Static Preamble and 1.5nCK Postamble

4.4 Burst Read Operation

The READ command completes the JEDEC READ transaction sequence. A burst Read command (Figure 15, Figure 17, and Figure 20) is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table (Table 96). The command address bus inputs determine the starting column address for the burst. The two low-order address bits are not transmitted on the CA bus and are implied to be “0”, so that the starting burst address is always a multiple of four (ex. 0x0, 0x4, 0x8, 0xC) for BL16 and (0x0, 0x4, 0x8, 0xC, 0x10, 0x14, 0x18, 0x1C) for BL32 transactions. The read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL * tCK + tDQSCK + tDQSQ after the rising edge of Clock that completes a read command. The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e., post-preamble) rising edge of the data strobe. Each subsequent data out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle postamble, or for a 1.5-cycle postamble if the programmable postamble bit is set in the mode register. The RL is programmed in the mode registers. Pin timings for the data strobe are measured relative to the cross-point of DQS_t and DQS_c



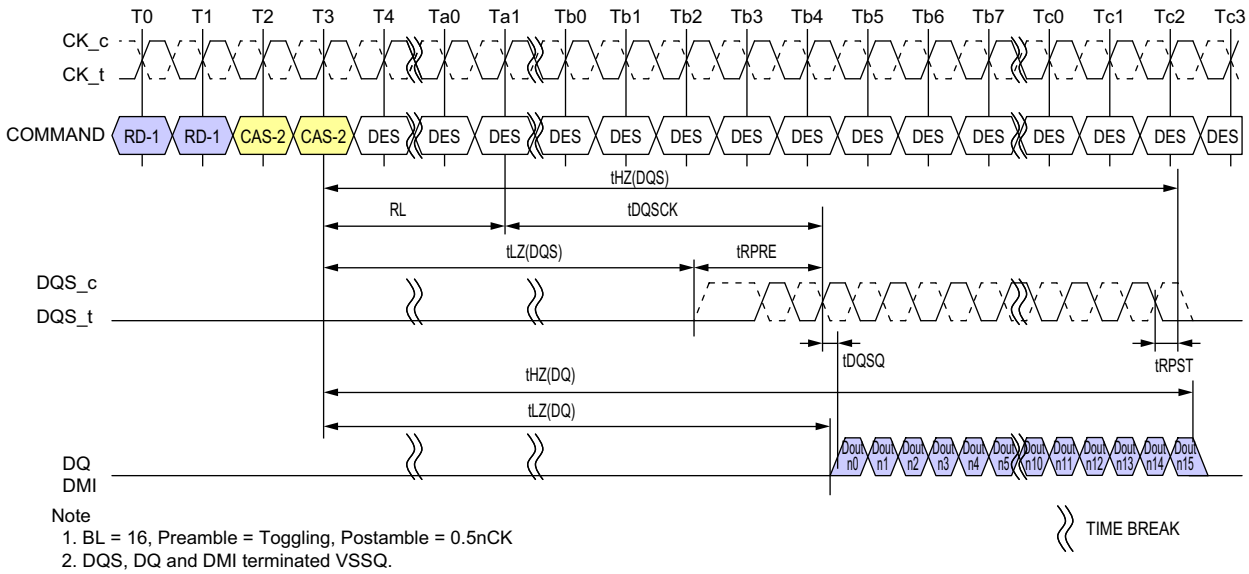
Note
1. BL = 16, tCCD = 8, Preamble = Toggle, Postamble = 0.5nCK, DQ/DQS: VSSQ termination
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 20 — Seamless Burst Read

The seamless Burst READ operation is supported by placing a READ command at every tCCD(Min) interval for BL16 (or every 2 x tCCD(Min) for BL32). The seamless Burst READ can access any open bank.

4.5 Read Timing

The read timing is shown in Figure 21.



Note
1. BL = 16, Preamble = Toggling, Postamble = 0.5nCK
2. DQS, DQ and DMI terminated VSSQ.
3. Output driver does not turn on before an end point of tLZ(DQS) and tLZ(DQ).
4. Output driver does not turn off before an end point of tHZ(DQS) and tHZ(DQ)

Figure 21 — Read Timing

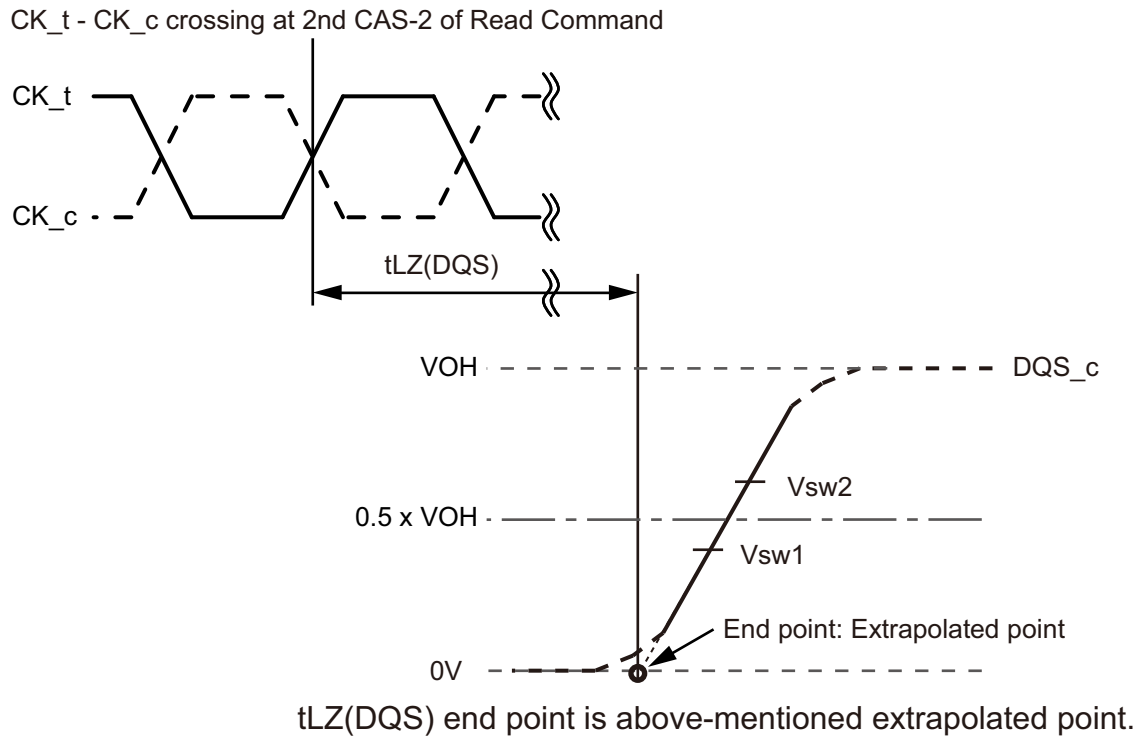
4.5.1 tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ).

This section shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

4.5.2 tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment)

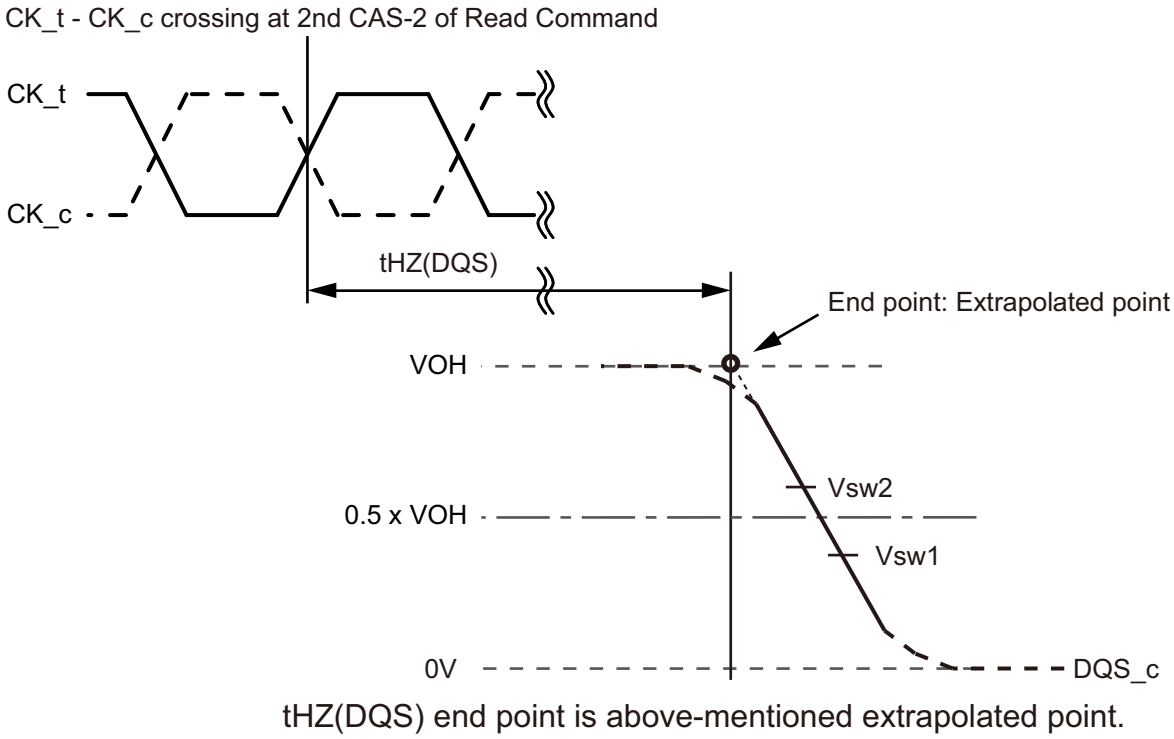
The calculation method is shown in Figure 22, Figure 23, and Table 54.



Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQS_t and DQS_C = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

Figure 22 — tLZ(DQS) Method for Calculating Transitions and End Point

4.5.2 tLZ(DQS) and tHZ(DQS) Calculation for ATE (Automatic Test Equipment) (cont'd)



Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQS_t and DQS_C = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

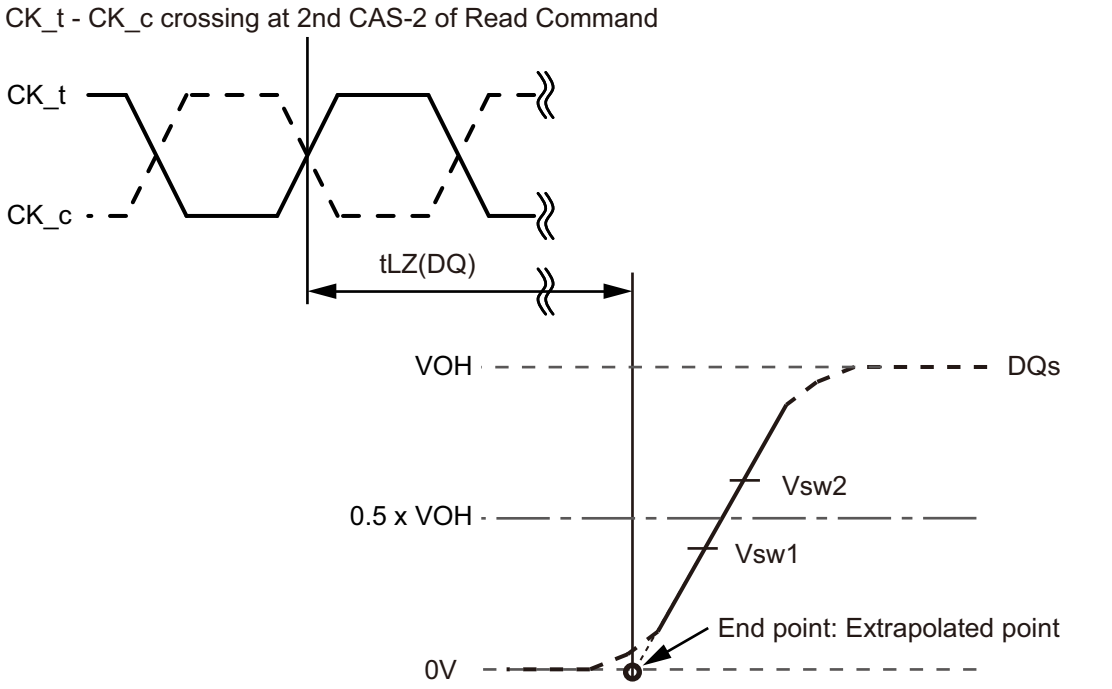
Figure 23 — tHZ(DQS) Method for Calculating Transitions and End Point

Table 54 — Reference Voltage for tLZ(DQS), tHZ(DQS) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	0.4 x VOH	0.6 x VOH	
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	0.4 x VOH	0.6 x VOH	

4.5.3 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment)

The calculation method is shown in Figure 24, Figure 25, and Table 55.

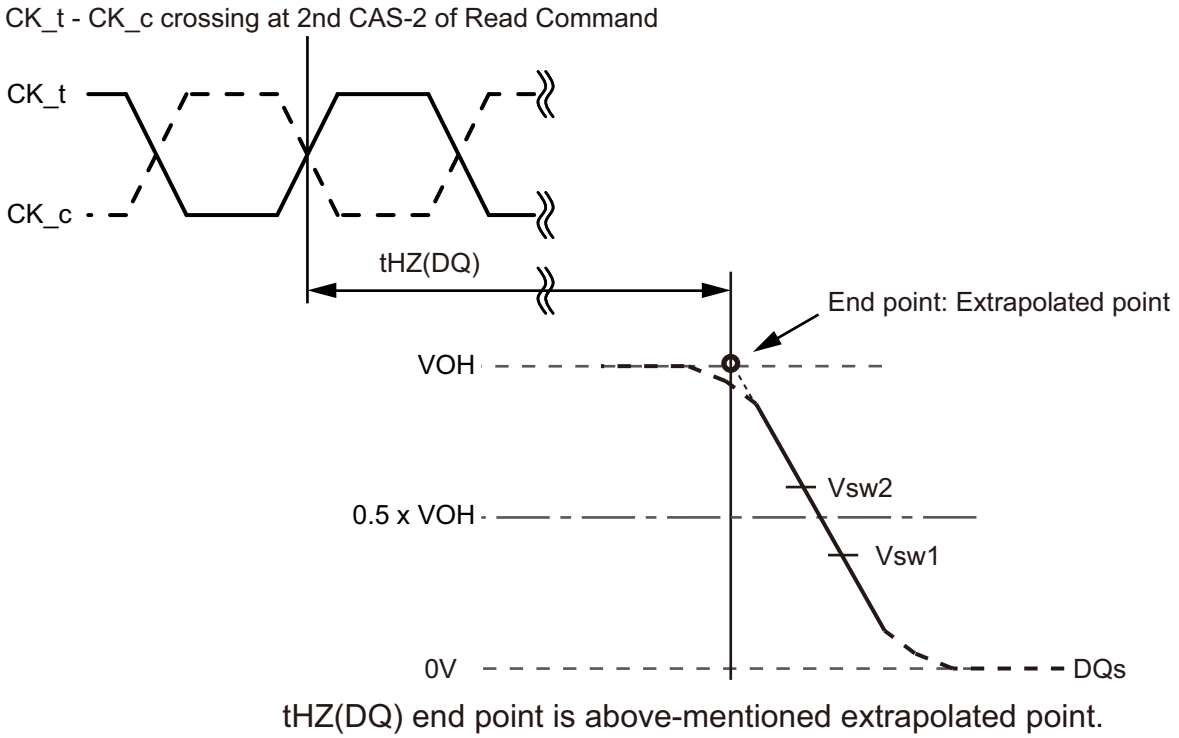


tLZ(DQ) end point is above-mentioned extrapolated point.

Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

Figure 24 — tLZ(DQ) Method for Calculating Transitions and End Point

4.5.3 tLZ(DQ) and tHZ(DQ) Calculation for ATE (Automatic Test Equipment) (cont'd)



Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQ and DMI = 50ohm to VSSQ.
3. The VOH level depends on MR22 OP[2:0] and MR3 OP[0] settings as well as device tolerances. Use the actual VOH value for tHZ and tLZ measurements.

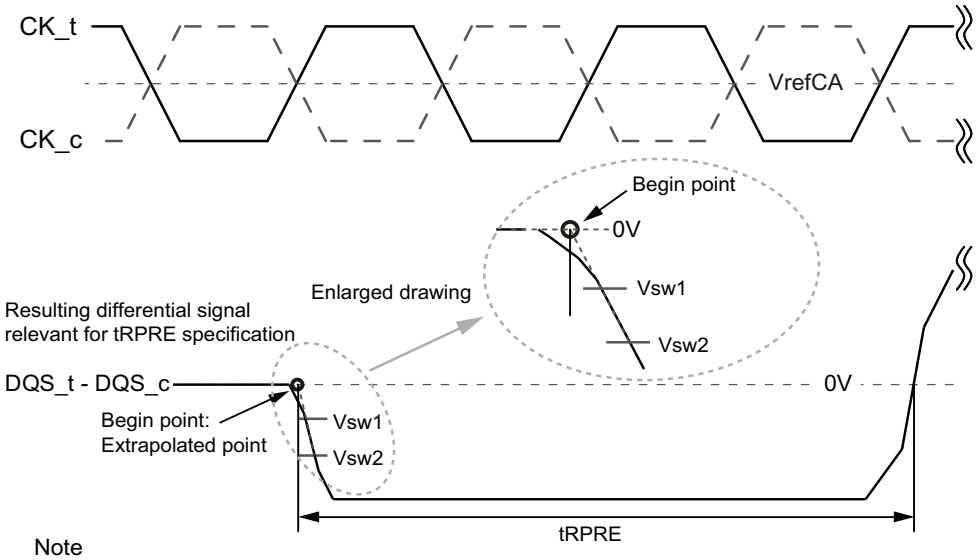
Figure 25 — tHZ(DQ) Method for Calculating Transitions and End Point

Table 55 — Reference Voltage for tLZ(DQ), tHZ(DQ) Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	0.4 x VOH	0.6 x VOH	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	0.4 x VOH	0.6 x VOH	

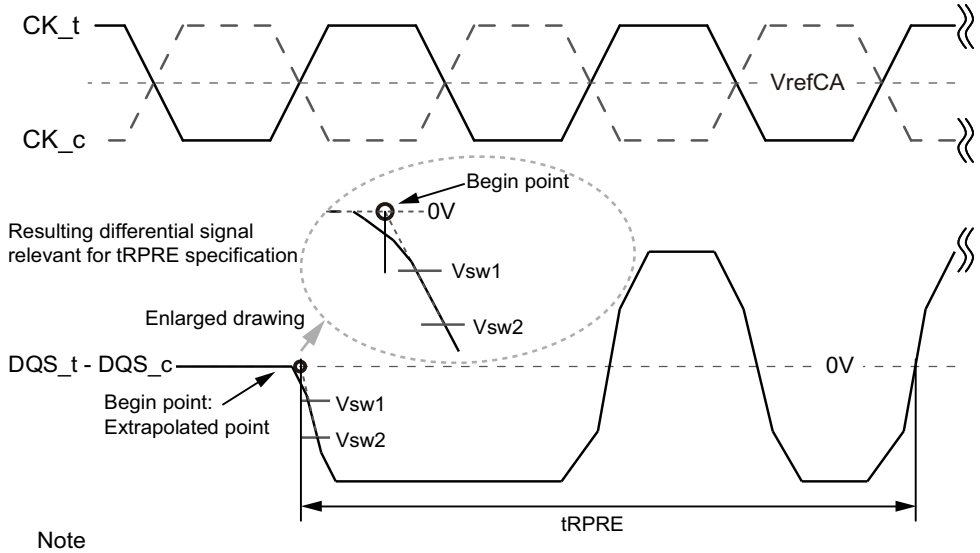
4.5.4 tRPRE Calculation for ATE (Automatic Test Equipment)

The method for calculating differential pulse widths for tRPRE is shown in Figure 26, Figure 27, and Table 56.



Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Static

Figure 26 — Method for Calculating tRPRE Transitions and Endpoints



Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
3. Preamble = Toggle

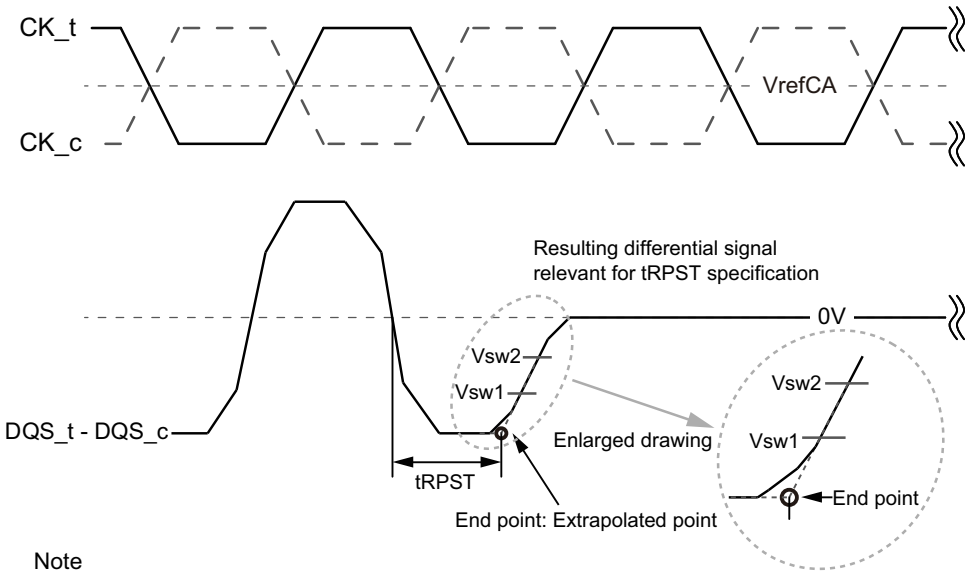
Figure 27 — Method for Calculating tRPRE Transitions and Endpoints

Table 56 — Reference Voltage for tRPRE Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t, DQS_c differential Read Preamble	tRPRE	-(0.3 x VOH)	-(0.7 x VOH)	

4.5.5 tRPST Calculation for ATE (Automatic Test Equipment)

The method for calculating differential pulse widths for tRPST is shown in Figure 28, Table 57, and Table 58.



Note
1. Conditions for Calibration: Pull Down Driver Ron = 40ohm, VOH = VDDQ x 0.5
2. Termination condition for DQS_t, DQS_c, DQ and DMI = 50ohm to VSSQ.
3. Read Postamble: 0.5tCK
4. The method for calculating differential pulse widths for 1.5 tCK Postamble is same as 0.5 tCK Postamble.

Figure 28 — Method for Calculating tRPST Transitions and Endpoints

Table 57 — Reference Voltage for tRPST Timing Measurements

Measured Parameter	Measured Parameter Symbol	Vsw1[V]	Vsw2[V]	Note
DQS_t, DQS_c differential Read Postamble	tRPST	-(0.7 x VOH)	-(0.3 x VOH)	

Table 58 — Read AC Timing

Parameter	Symbol	Min/Max	Data Rate								Unit
Read Timing			533	1066	1600	2133	2667	3200	3733	4266	
READ preamble	tRPRE	Min	1.8								tCK(avg)
0.5 tCK READ postamble	tRPST	Min	0.4								tCK(avg)
1.5 tCK READ postamble	tRPST	Min	1.4								tCK(avg)
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	Min	(RL x tCK) + tDQSCK(Min) - 200ps								ps
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	Max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) - 100 ps								ps
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	Min	(RL x tCK) + tDQSCK(Min) - (tRPRE(Max) x tCK) - 200 ps								ps
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	Max	(RL x tCK) + tDQSCK(Max) +(BL/2 x tCK) + (RPST(Max) x tCK) - 100 ps								ps
DQS-DQ skew	tDQSQ	Max	0.18								UI
NOTE UI = User Interval = tCK/2											

4.6 tDQSCK Timing Table

The timing parameters are provided in Table 59.

Table 59 — tDQSCK Timing Table

Parameter	Symbol	Min	Max	Unit	Notes
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c - Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c - Voltage Variation	tDQSCK_volt	-	7	ps/mV	3

NOTE 1 Includes process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.

NOTE 2 tDQSCK_temp max delay variation as a function of Temperature.

NOTE 3 tDQSCK_volt max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. tDQSCK_volt should be used to calculate timing variation due to V_{DDQ} and V_{DD2} noise < 20 MHz. Host controller does not need to account for any variation due to V_{DDQ} and V_{DD2} noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement V_{DDQ} = V_{DD2} is assumed.

4.6.1 CK to DQS Rank to Rank variation

The rank to rank variation is provided in Table 60.

Table 60 — tDQSCK_rank2rank Timing Table

Parameter	Symbol	Min/Max							Unit	Note
Read Timing			1600	1866	2133	2400	3200	4266		
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	Max	1.0						ns	1,2

NOTE 1 The same voltage and temperature is applied to tDQS2CK_rank2rank.

NOTE 2 tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

4.7 Rank to Rank Timings

Rank to Rank Timings describe how many clock cycles are required between adjacent READ and WRITE transactions from different ranks. Note that LPDDR4X-NVM devices do not support WRITE operations. The sequential transactions described include: READ to READ, READ to WRITE and WRITE to READ. The ranks can be either NVM and NVM or a mix of NVM and DRAM. Figure 29 shows the two rank circuit arrangement.

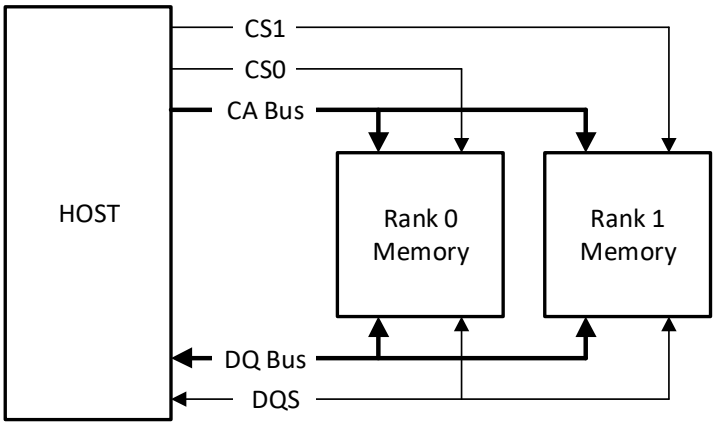


Figure 29 — Rank to Rank Circuit Arrangement

Table 61 — Rank to Rank Transaction Timings (with WRITE DQ_ODT off)

		Trailing Transaction *(earliest)*	
		RD or MRR (DRAM or NVM)	WR (DRAM only)
Leading Transaction *(latest)*	RD or MRR (DRAM or NVM)	BL/2 + tRPST + RU((tDQSCK(max) - tDQSCK(min)) / tCK)	RL + RU(tDQSCK(min) / tCK) + BL/2 + tRPST - WL + tWPRE
	WR (DRAM only)	WL + RU(tDQSS(max)/tCK) + BL/2 + tWPST - RL - RU(tDQSCK(min)/tCK) + tPRE	not applicable (no WRITES to LPDDR4X-NVM)
NOTE 1 RED indicates timings from the leading bus transaction, BLUE indicates timings from the trailing bus transaction.			

Table 62 — Rank to Rank Transaction Timings (with WRITE DQ_ODT on)

		Trailing Transaction *(earliest)*	
		RD or MRR (DRAM or NVM)	WR (DRAM only)
Leading Transaction *(latest)*	RD or MRR (DRAM or NVM)	BL/2 + tRPST + RU((tDQSCK(max) - tDQSCK(min)) / tCK)	RL + RU(tDQSCK(min) / tCK) + BL/2 + tRPST - tWDQS_on
	WR (DRAM only)	tWDQS_off - RL - RU(tDQSCK(min)/tCK) + tPRE	not applicable (no WRITES to LPDDR4X-NVM)
NOTE 1 RED indicates timings from the leading bus transaction, BLUE indicates timings from the trailing bus transaction			

4.8 Read Latencies

The read latencies are provided in Table 63.

Table 63 — Read Latencies

Read Latency [nCK]	Lower Clock Frequency Limit [MHz] (>)	Upper Clock Frequency Limit [MHz] (≤)	Notes
6	10	266	1,2
12	266	533	
16	533	800	
22	800	1066	
28	1066	1333	
32	1333	1600	
36	1600	1866	
40	1866	2133	

NOTE 1 The LPDDR4X-NVM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL value

4.9 Postamble and Preamble Merging Behavior

The DQS strobe for the device requires a preamble prior to the first latching edge (the rising edge of DQS_t with data valid), and it requires a postamble after the last latching edge. The preamble and postamble options are set via Mode Register Write commands.

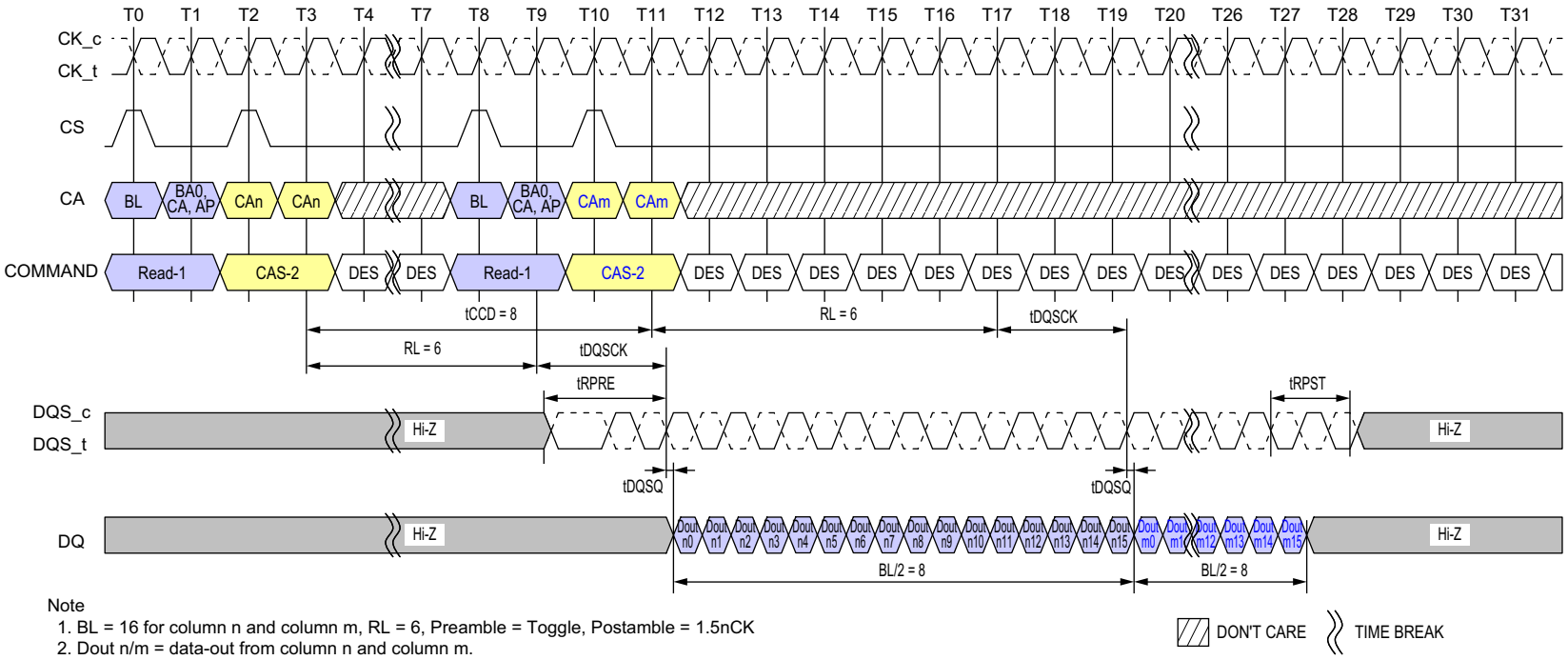
In Read to Read operations with tCCD=BL/2, postamble for 1st command and preamble for 2nd command will disappear to create consecutive DQS latching edge for seamless burst operations.

But in the case of Read to Read operations with command interval of tCCD+1,tCCD+2, etc., they will not completely disappear because it’s not seamless burst operations.

Timing diagrams in this material describe Postamble and Preamble merging behavior in Read to Read operations with tCCD+n.

4.9.1 Read to Read Operation

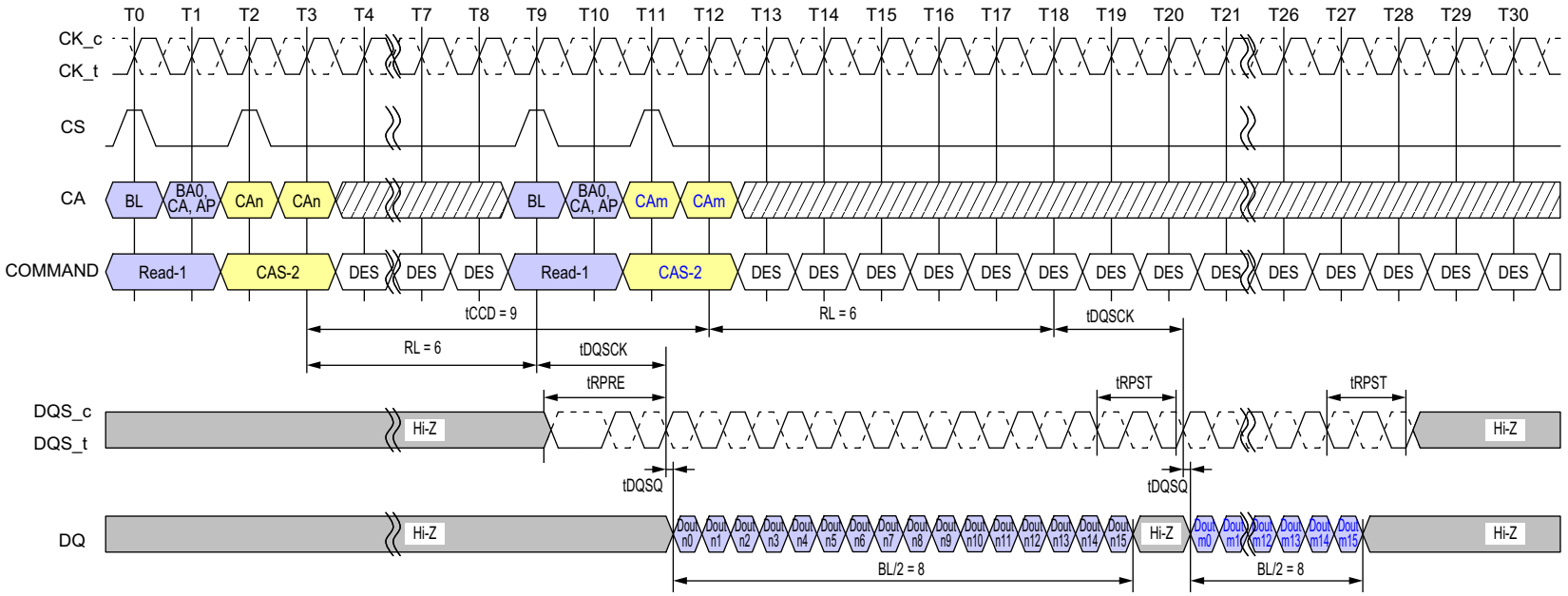
Read to read operation is shown in Figure 30 through Figure 42.



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 30 — Seamless Reads Operation: tCCD = Min, Preamble = Toggle, 1.5nCK Postamble

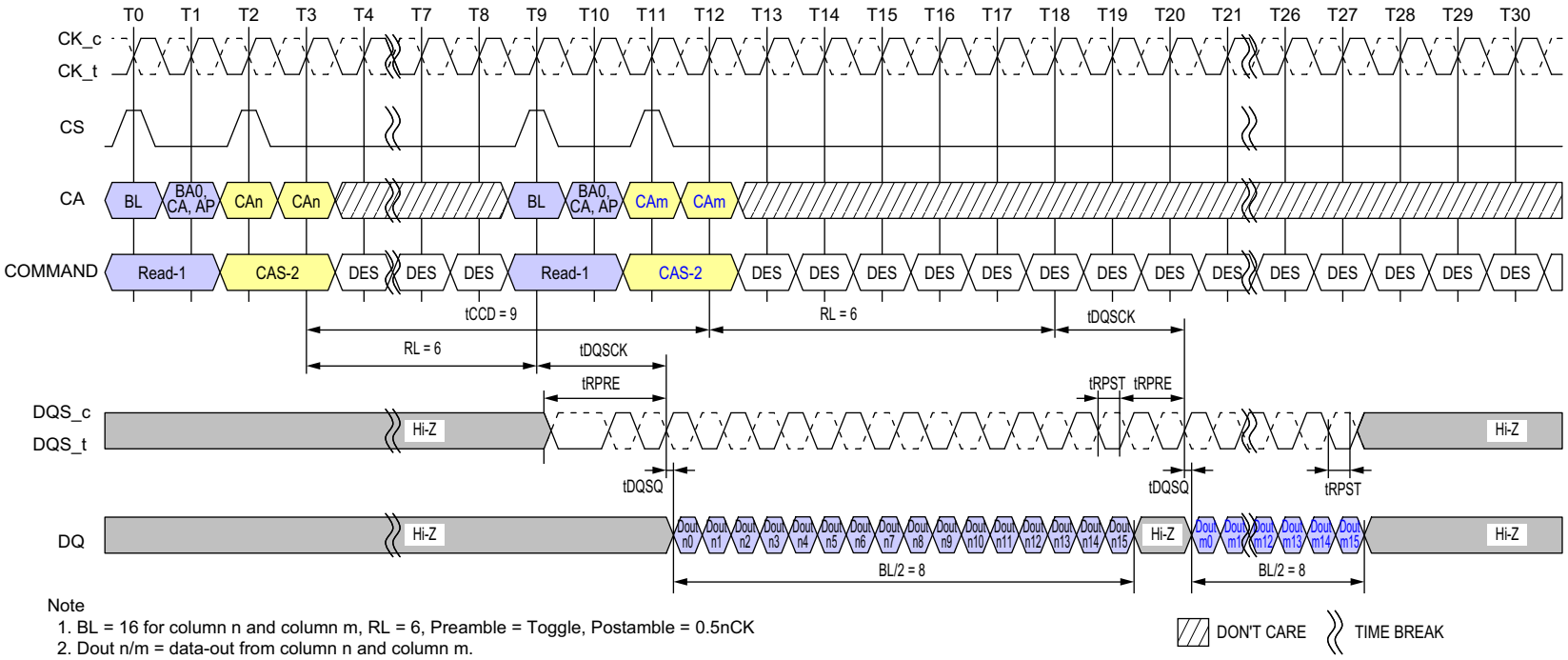
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 31 — Consecutive Reads Operation: tCCD = Min +1, Preamble = Toggle, 1.5nCK Postamble

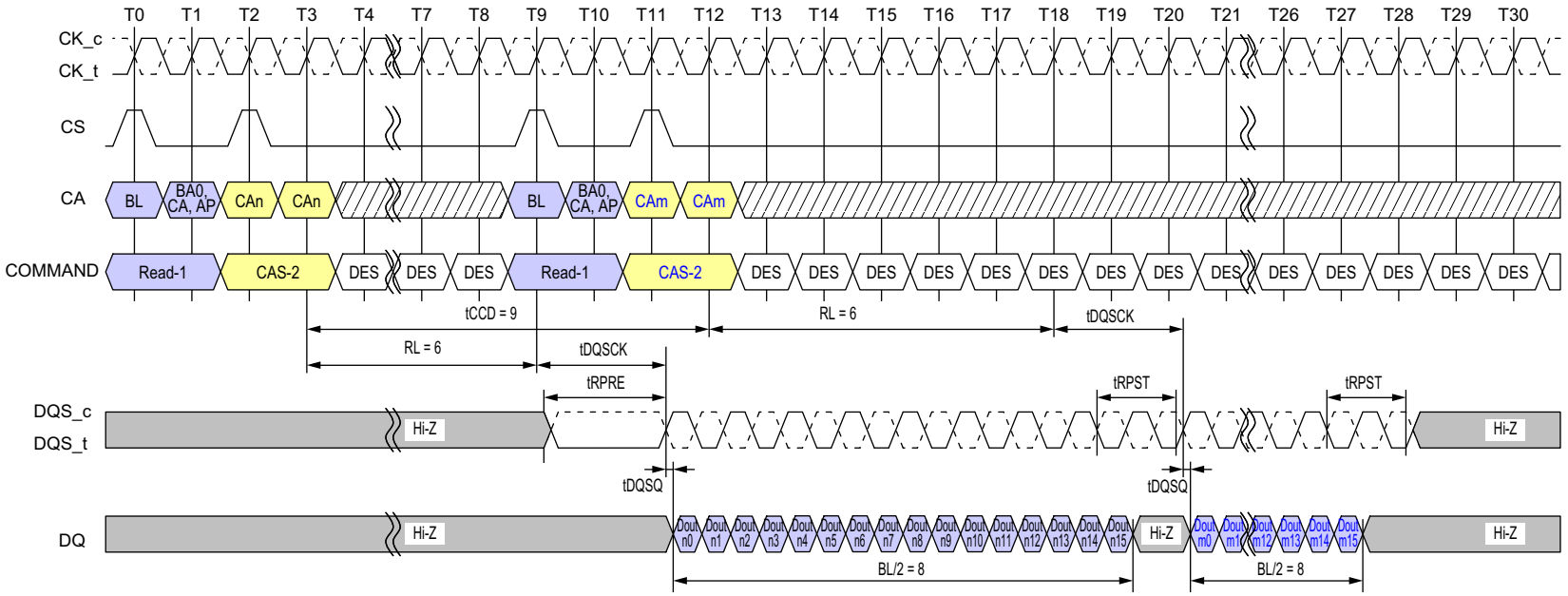
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 32 — Consecutive Reads Operation: tCCD = Min +1, Preamble = Toggle, 0.5nCK Postamble

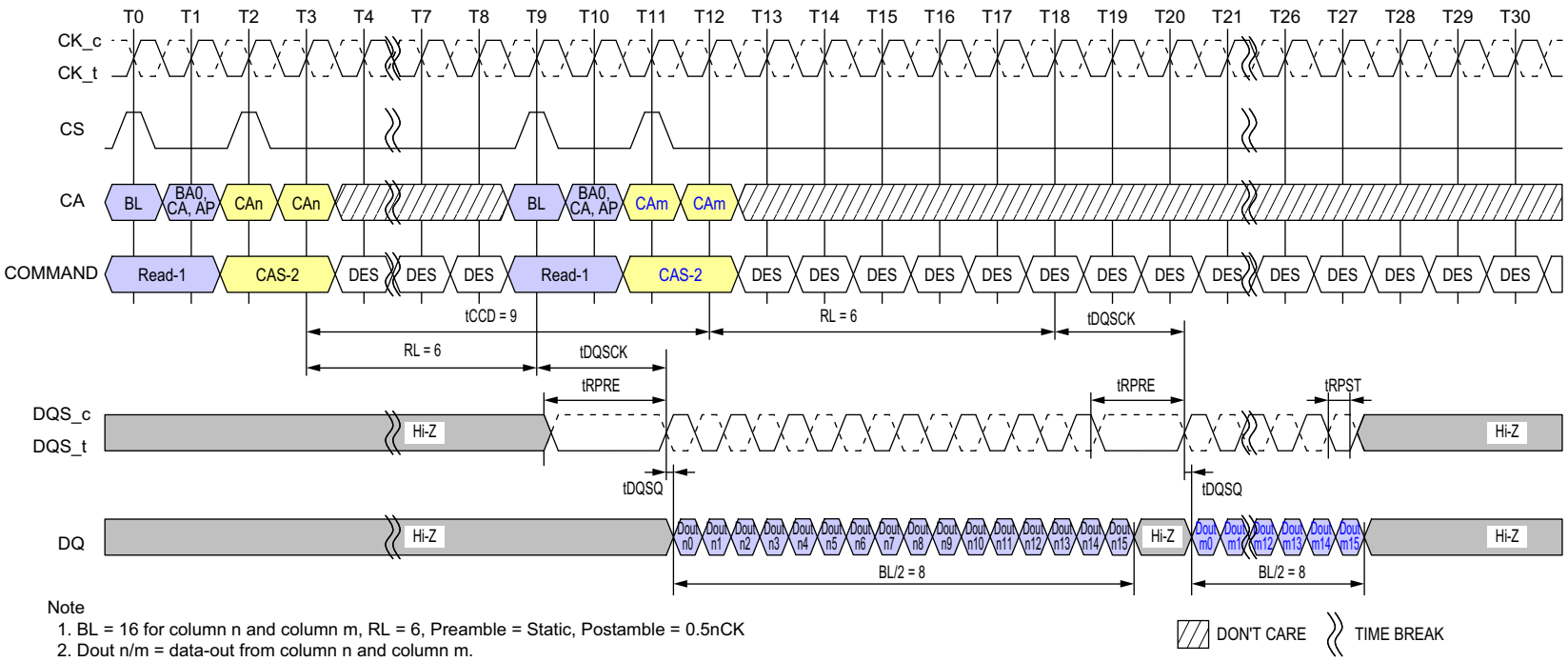
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 33 — Consecutive Reads Operation: tCCD = Min +1, Preamble = Static, 1.5nCK Postamble

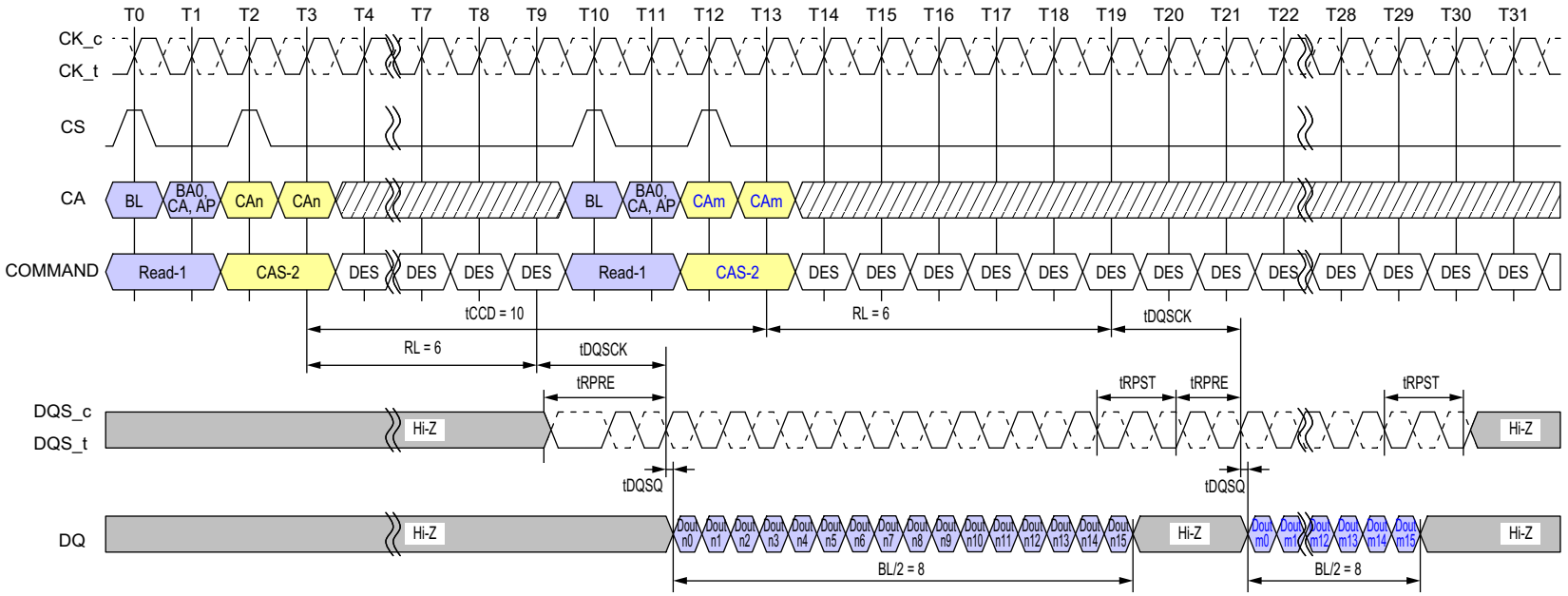
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 34 — Consecutive Reads Operation: tCCD = Min +1, Preamble = Static, 0.5nCK Postamble

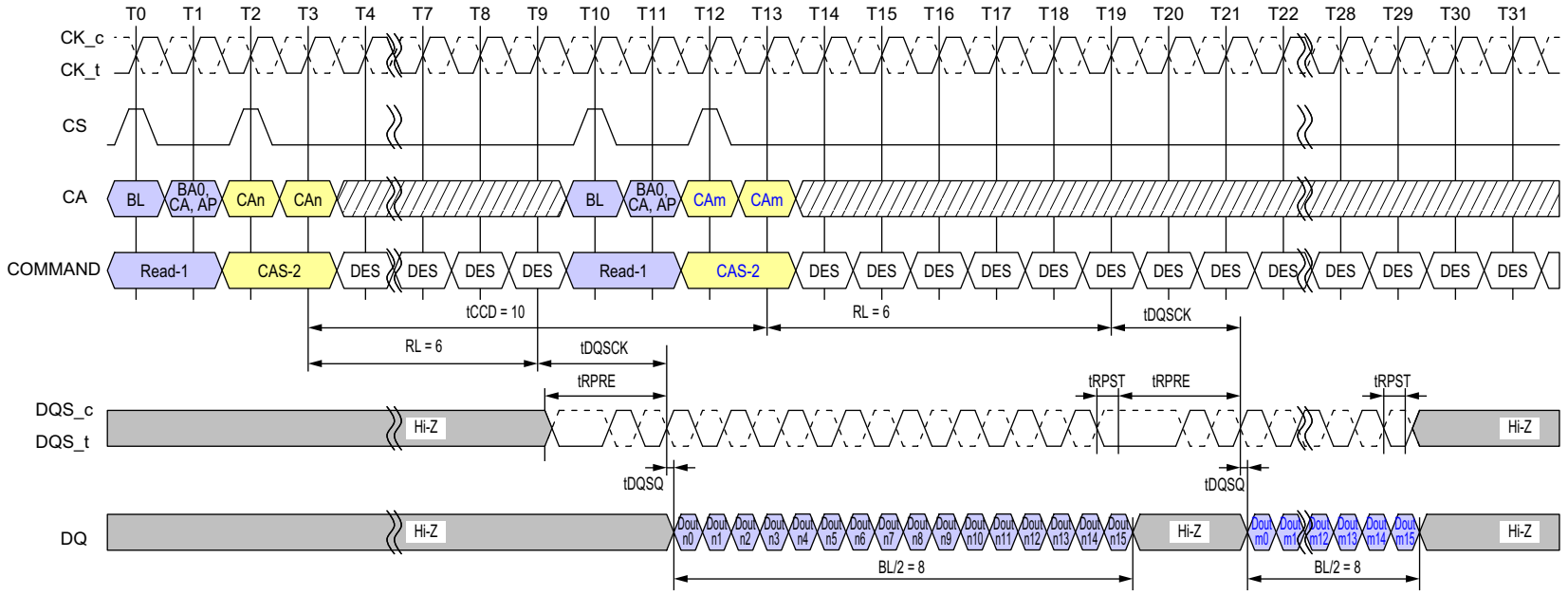
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 35 — Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 1.5nCK Postamble

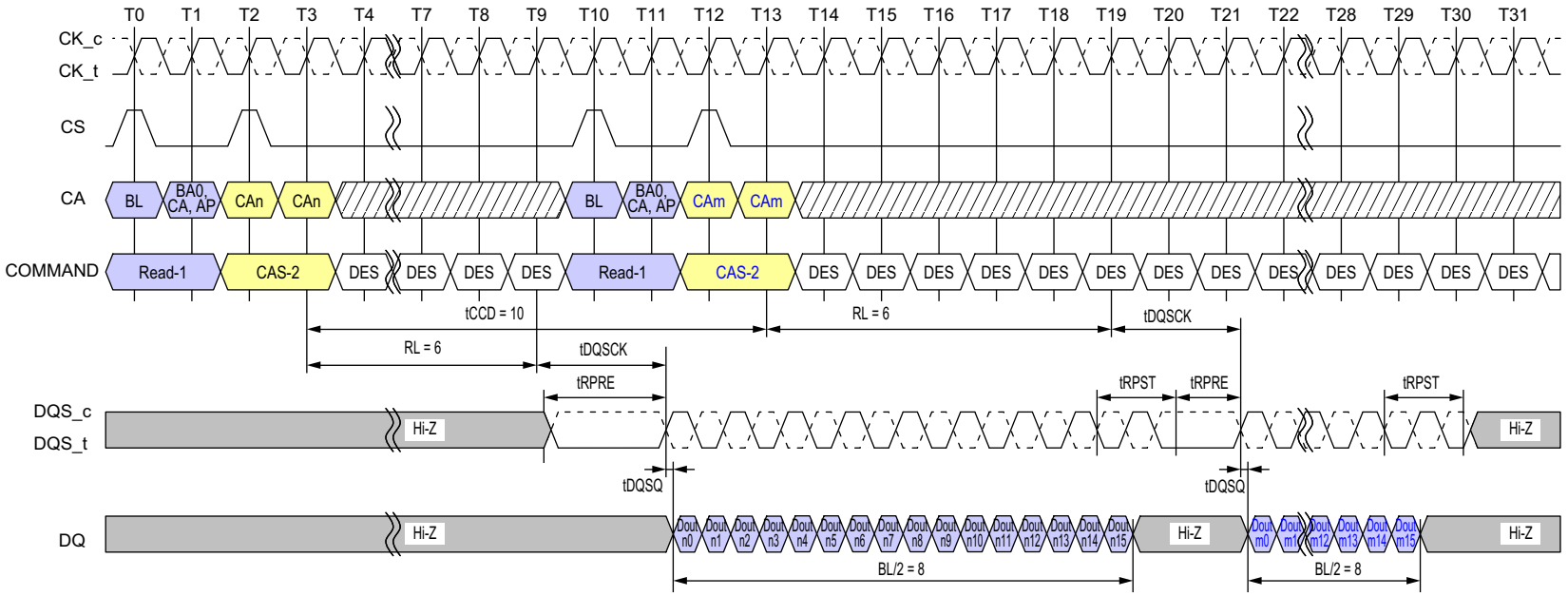
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 36 — Consecutive Reads Operation: tCCD = Min +2, Preamble = Toggle, 0.5nCK Postamble

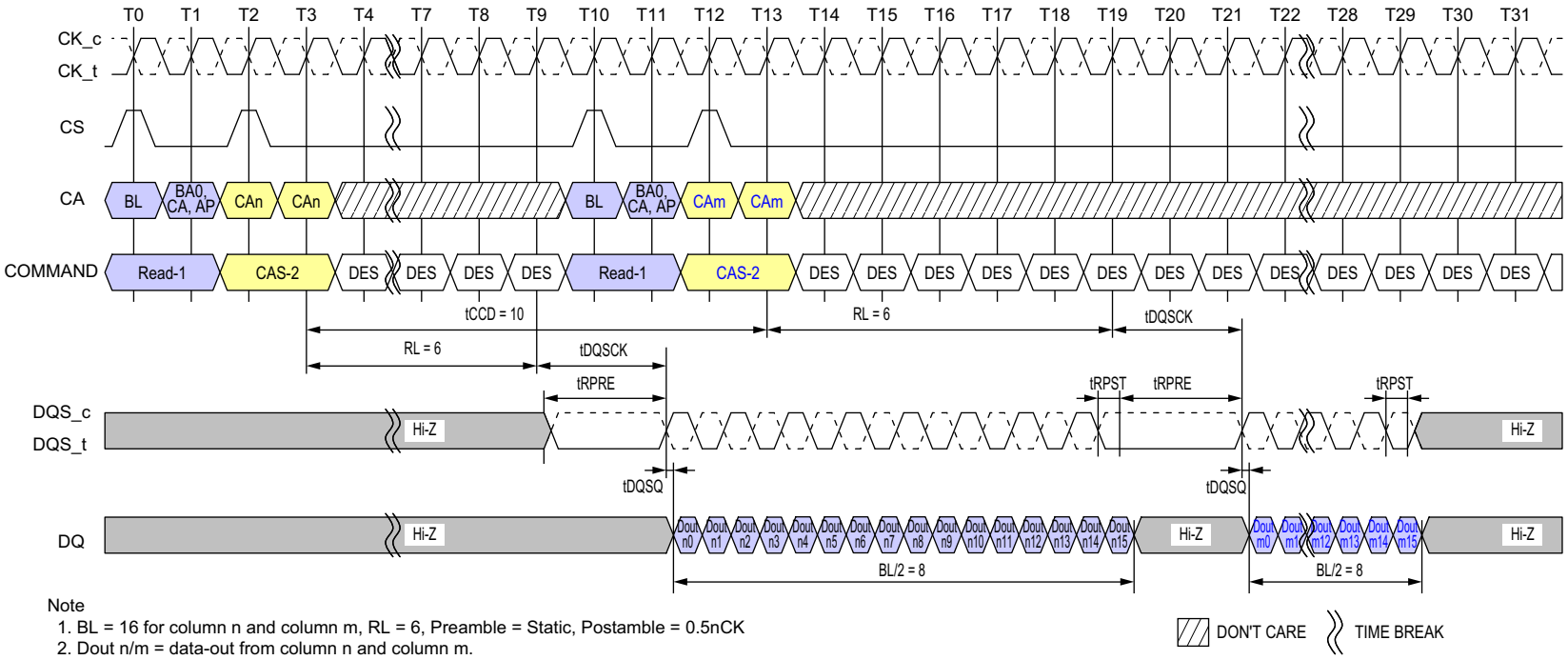
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 37 — Consecutive Reads Operation: tCCD = Min +2, Preamble = Static, 1.5nCK Postamble

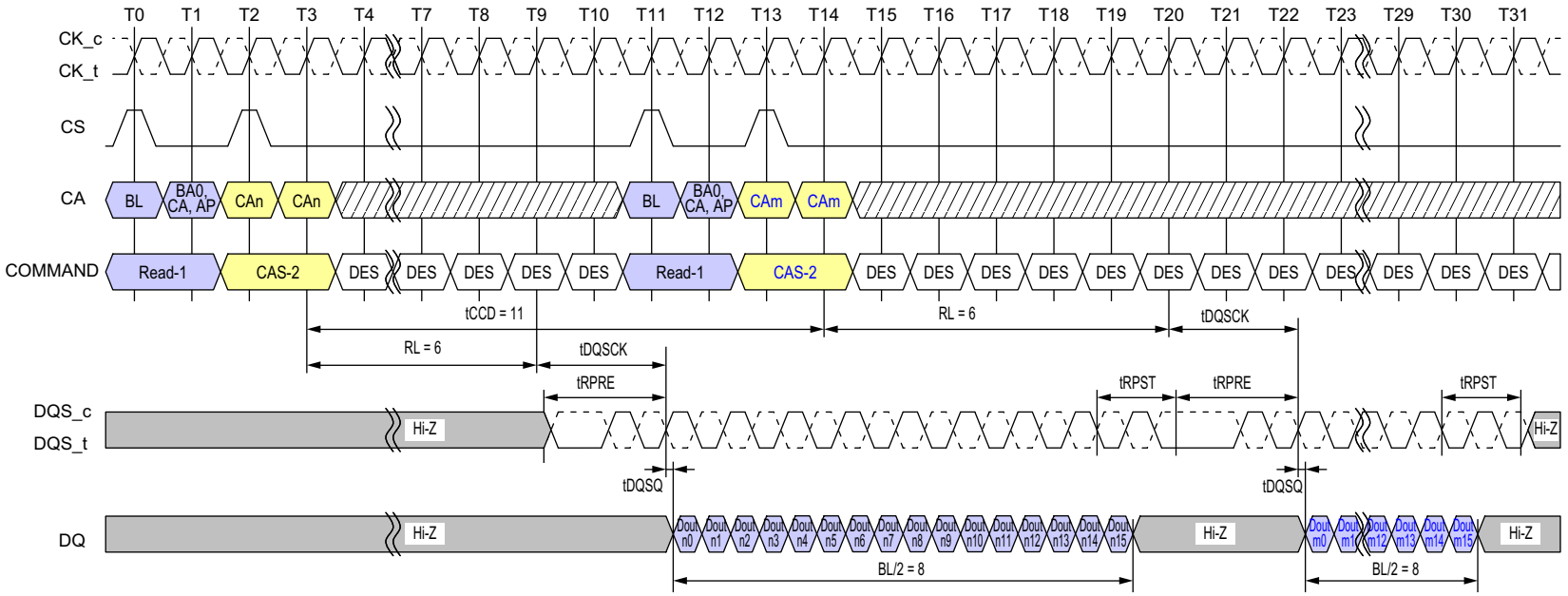
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 38 — Consecutive Reads Operation: tCCD = Min +2, Preamble = Static, 0.5nCK Postamble

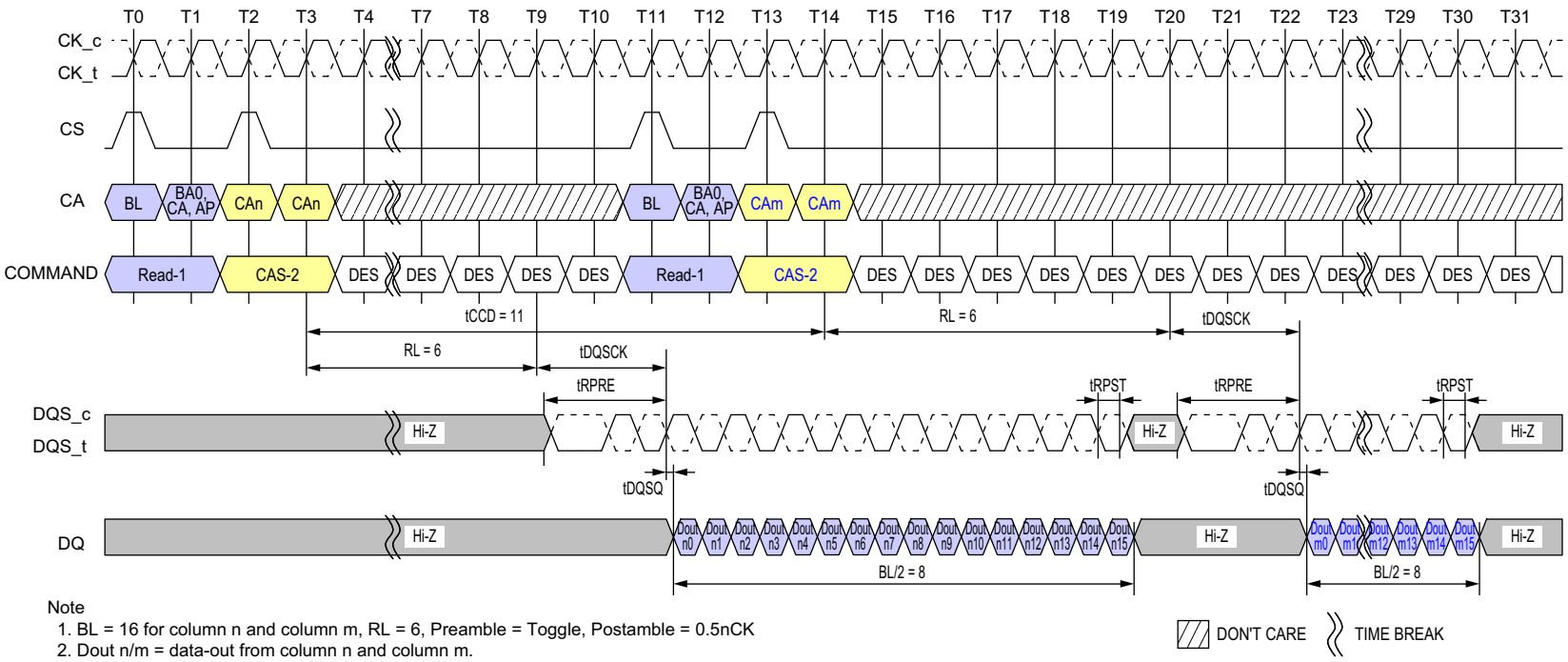
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 39 — Consecutive Reads Operation: tCCD = Min +3, Preamble = Toggle, 1.5nCK Postamble

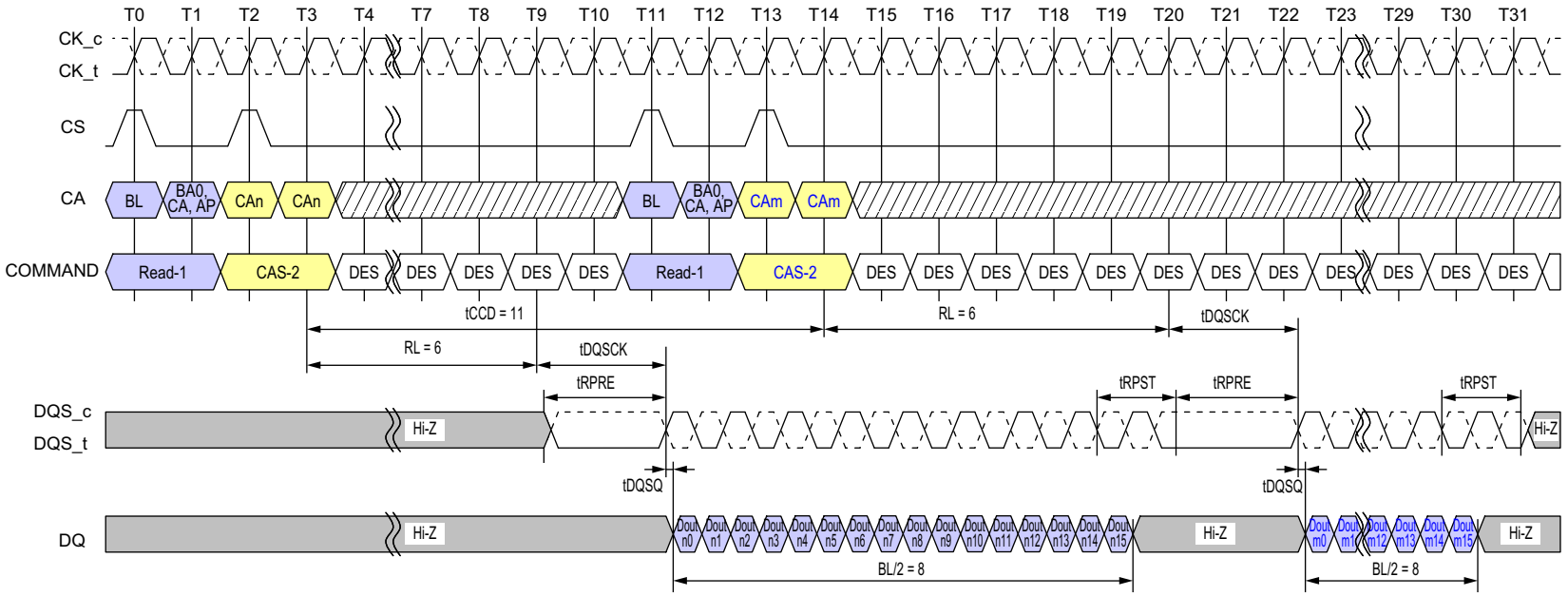
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Toggle, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 40 — Consecutive Reads Operation: tCCD = Min +3, Preamble = Toggle, 0.5nCK Postamble

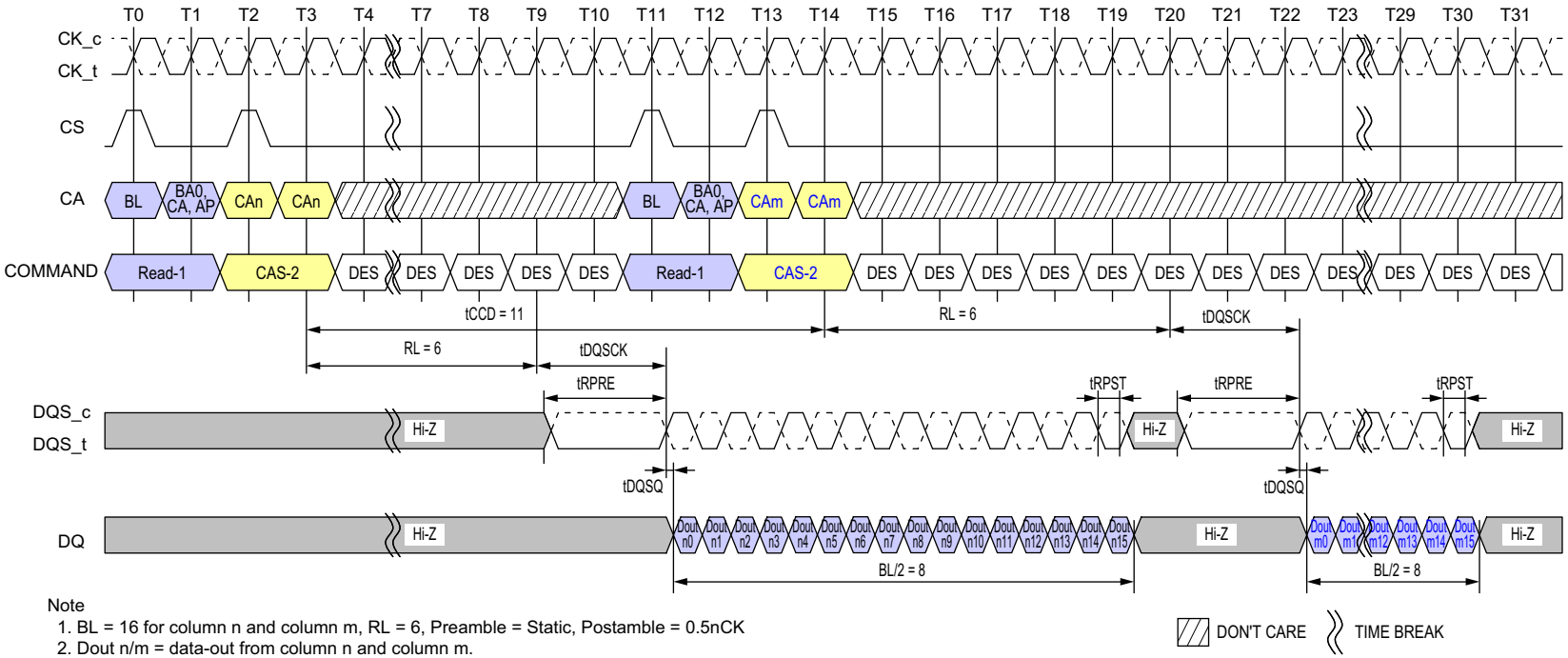
4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 1.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 41 — Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 1.5nCK Postamble

4.9.1 Read to Read Operation (cont'd)



Note
1. BL = 16 for column n and column m, RL = 6, Preamble = Static, Postamble = 0.5nCK
2. Dout n/m = data-out from column n and column m.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 42 — Consecutive Reads Operation: tCCD = Min +3, Preamble = Static, 0.5nCK Postamble

4.10 Mode Register Read (MRR)

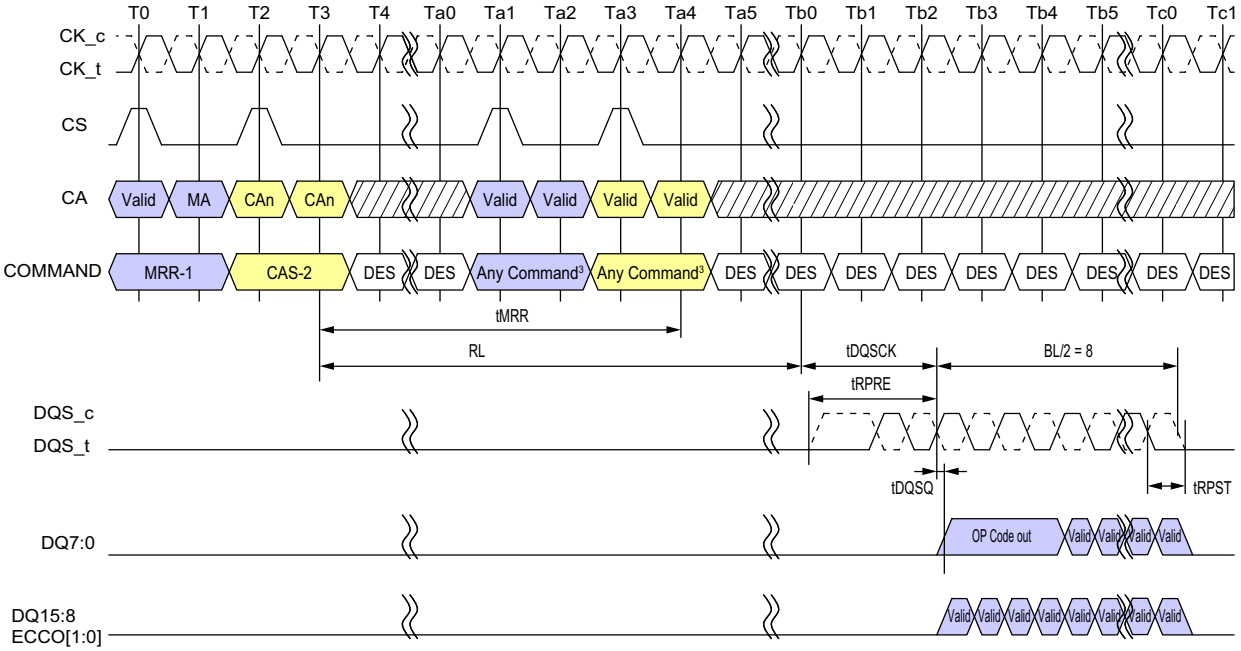
The Mode Register Read (MRR) command is used to read configuration and status data from the LPDDR4X-NVM mode registers. The MRR command is initiated with CS and CA[5:0] in the proper state as defined by the Command Truth Table. The mode register address operands (MA[5:0]) allow the user to select one of 64 registers. The mode register contents are available on the first 4UI's data bits of DQ[7:0] after RL x tCK + tDQSCK + tDQSQ following the MRR command (UI=Unit Interval=tCK/2). Subsequent data bits contain valid but undefined content. DQS is toggled for the duration of the Mode Register READ burst. The MRR has a command burst length 16. Reference Table 64 and Figure 43.

MRR operation must not be interrupted.

Table 64 — DQ Output Mapping

UI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DQ0	OP0				V											
DQ1	OP1				V											
DQ2	OP2				V											
DQ3	OP3				V											
DQ4	OP4				V											
DQ5	OP5				V											
DQ6	OP6				V											
DQ7	OP7				V											
DQ8-15	V															
ECCO0-1	V															

NOTE 1 UI = User Interval = tCK/2
NOTE 2 MRR data are extended to first 4 UI's for controller to sample data easily.
NOTE 3 ECCO does not apply during normal MRR. The ECCO signal is driven to a valid level during MRR.
NOTE 4 The read preamble and postamble of MRR are same as normal read.

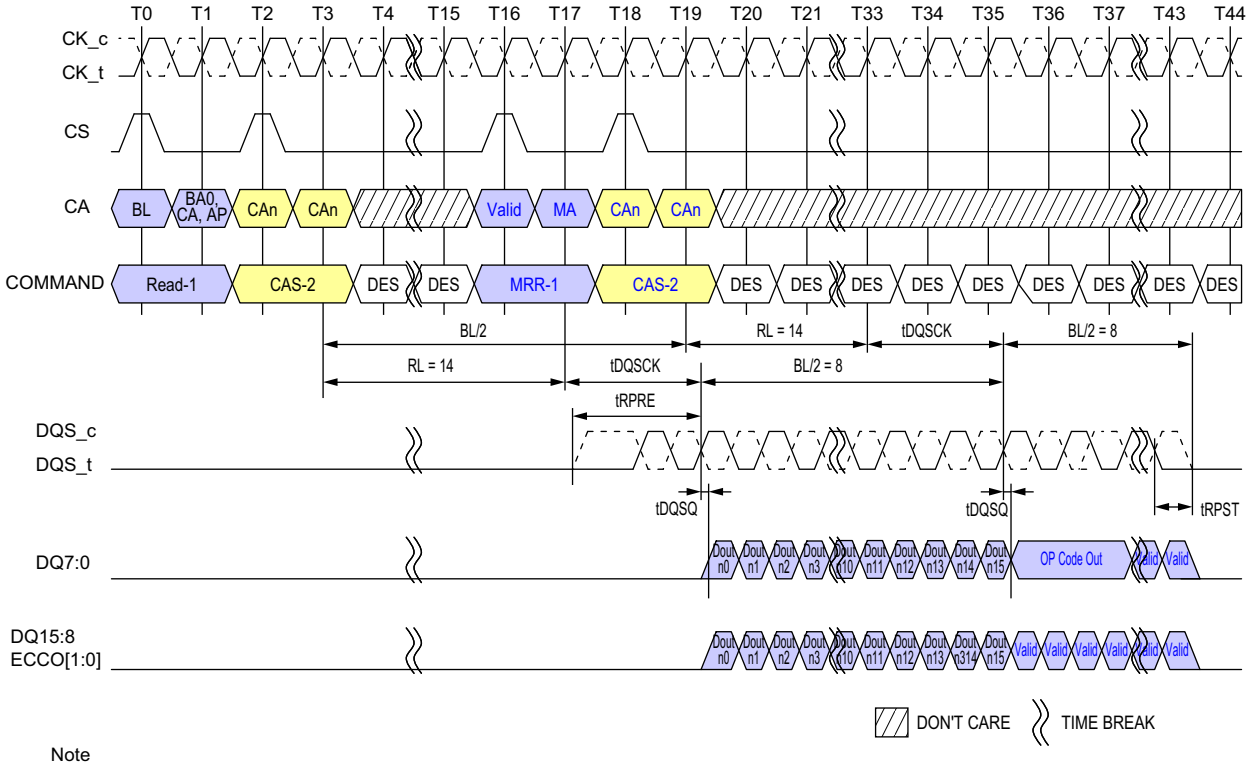


Note
1. Only BL=16 is supported
2. Only DES is allowed during tMRR period
3. There are some exceptions about issuing commands after tMRR. Refer to MRR/MRW Timing Constraints Table for detail.
4. ECCO is in Disable mode.
5. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.
6 . DQ/DQS: VSSQ termination

Figure 43 — Mode Register Read Operation

4.10.1 MRR after Read Command

After a prior READ command, the MRR command must not be issued earlier than BL/2 clock cycles in order to avoid the collision of Read burst data on the device's internal Data bus. Reference Figure 44 and Figure 46.

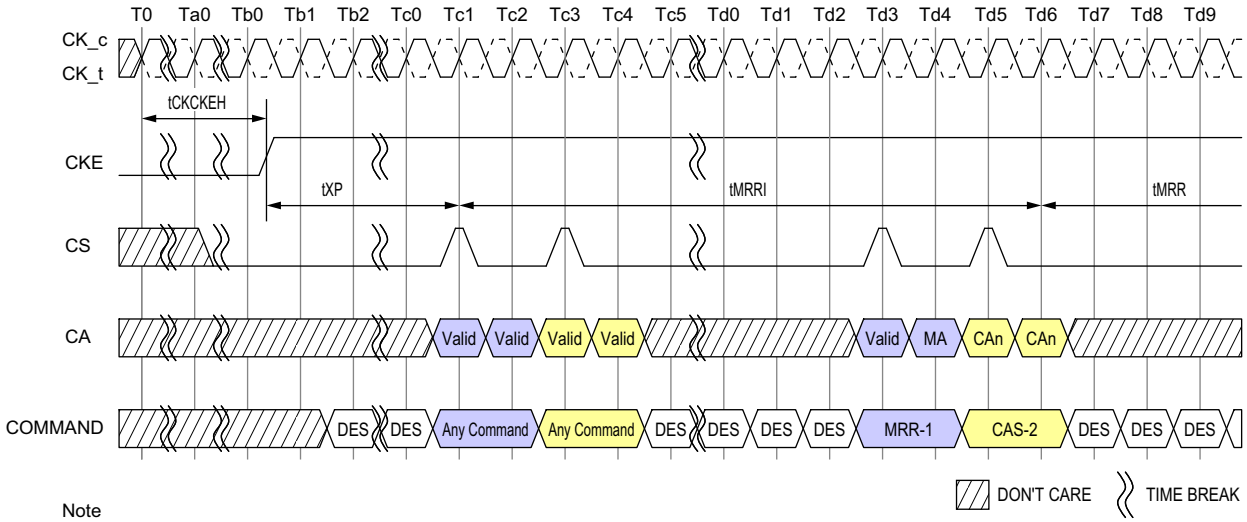


Note
1. The minimum number of clock cycles from the burst READ command to the MRR command is BL/2.
2. Read BL = 16, MRR BL = 16, RL = 14, Preamble = Toggle, Postamble = 0.5nCK, ECCO = Disable, DQ/DQS: VSSQ termination
3. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

Figure 44 — READ to MRR Timing

4.10.2 MRR after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the mode register read (MRR) command. This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the MRR data path after exit from power-down mode. Reference Figure 45 and Table 65.



Note
1. Only DES is allowed during tMRR period.
2. DES commands except tMRR period are shown for ease of illustration; other commands may be valid at these times.

Figure 45 — MRR following Power-Down Exit

Table 65 — Mode Register Read/Write AC Timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min	tRCD + 3nCK	-	
MODE REGISTER READ command period	tMRR	Min	8	nCK	
MODE REGISTER WRITE command period	tMRW	Min	MAX(10ns, 10nCK)	-	
Mode register set command delay	tMRD	Min	max(14ns, 10nCK)	-	

4.11 Mode Register Write (MRW)

The Mode Register Write (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated by setting CKE, CS, and CA[5:0] to valid levels at a rising edge of the clock (see Command Truth Table, Table 96). The mode register address and the data written to the mode registers is contained in CA[5:0] according to the Command Truth Table. The MRW command period is defined by tMRW. Mode register Writes to read-only registers have no impact on the functionality of the device. Reference Figure 46.

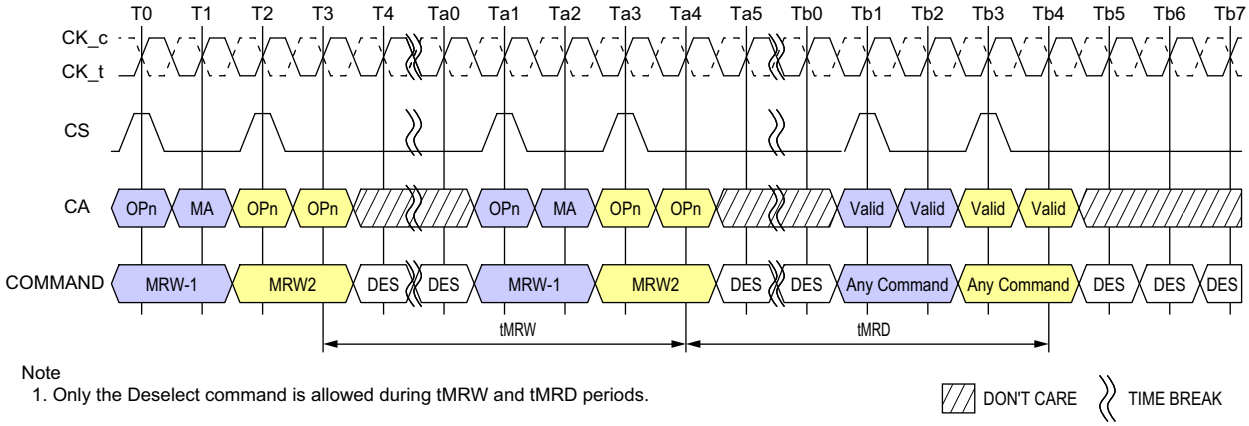


Figure 46 — Mode Register Write Timing

4.11.1 Mode Register Write

MRW can be issued from either a Bank-Idle or Bank-Active state. Certain restrictions may apply for MRW from an Active state (Reference Table 66 and Table 67).

Table 66 — Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State LPDDR4X-NVM	Command	Intermediate State LPDDR4X-NVM	Next State LPDDR4X-NVM
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading	Bank(s) Active
	MRW	Mode Register Writing	Bank(s) Active

Table 67 — MRR/MRW Timing Constraints

From Command	To Command	Minimum Delay between "From Command" and "To Command"	Unit	Notes
MRR	MRR	tMRR	-	
	RD	tMRR	-	
	MRW	RL+RU(tDQSCK(max)/tCK)+BL/2+ 3	nCK	1
RD	MRR	BL/2	nCK	
MRW		tMRD	-	
Power Down Exit		tXP+tMRRI	-	
MRW	RD	tMRD	-	
	MRW	tMRW	-	
RD/ RD DQ CAL	MRW	RL+BL/2+RU(tDQSCKmax/tCK) +RD(tRPST) +max(RU(7.5ns/tCK),8nCK)	nCK	

NOTE 1 RU is an abbreviation for Round Up (to the next higher integer clock cycle).

4.12 V_{REF} Current Generator (VRCG)

LPDDR4X-NVM V_{REF} current generators (VRCG) incorporate a high current mode to reduce the settling time of the internal V_{REF}CA level during training and when changing frequency set points during operation. The high current mode is enabled by setting MR13[OP3] = 1. Only Deselect commands may be issued until tVRCG_ENABLE is satisfied. tVRCG_ENABLE timing is shown in Figure 47 and Table 68.

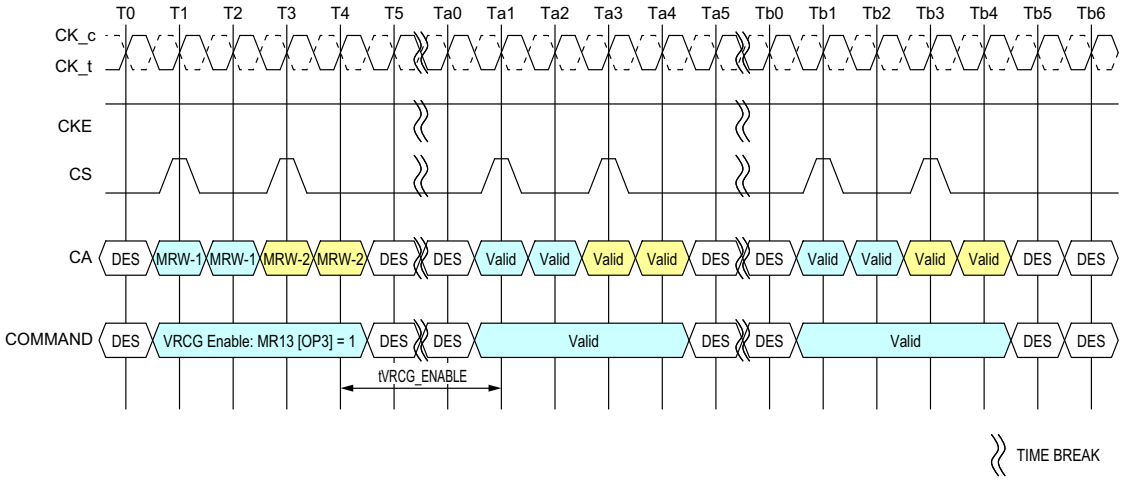


Figure 47 — VRCG Enable Timing

VRCG high current mode is disabled by setting MR13[OP3] = 0. Only Deselect commands may be issued until tVRCG_DISABLE is satisfied. tVRCG_DISABLE timing is shown in Figure 48 and Table 121.

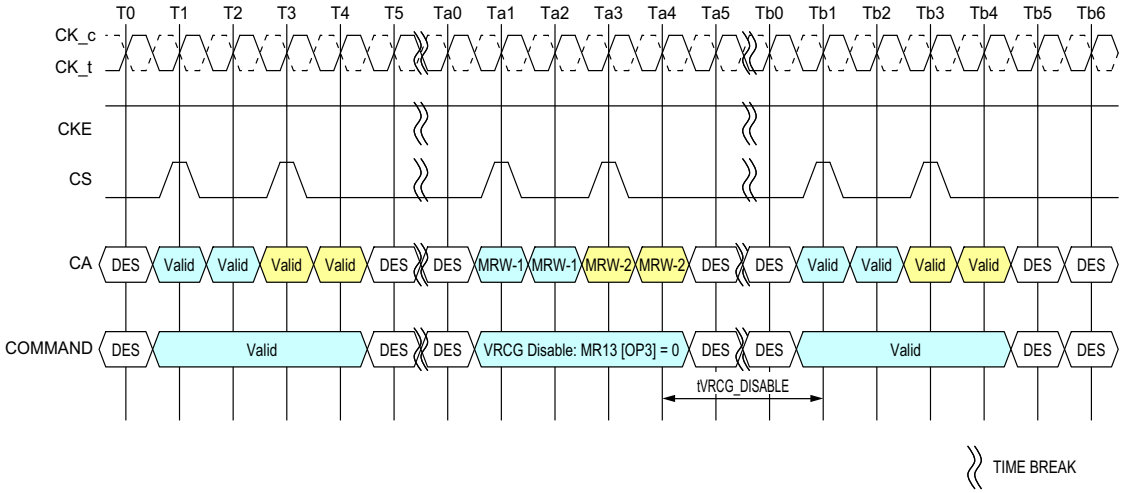


Figure 48 — VRCG Disable Timing

Note that LPDDR4X-NVM devices support V_{REF}CA range and value changes without enabling VRCG high current mode.

Table 68 — VRCG Enable/Disable Timing

Speed		533, 1066, 1600, 2133, 2667, 3200, 3733, 4266Mbps		Units	NOTE
Parameter	Symbol	MIN	MAX		
V_{REF} high current mode enable time	tVRCG_ENABLE	-	200	ns	
V_{REF} high current mode disable time	tVRCG_DISABLE	-	100	ns	

4.13 V_{REF}CA Training

The device internal V_{REF}CA specification parameters are voltage operating range, step size, V_{REF} set tolerance, V_{REF} step time and V_{REF} valid level.

The voltage operating range specifies the minimum required V_{REF} setting range for LPDDR4X-NVM devices. The minimum range is defined by V_{REF}max and V_{REF}min as depicted in Figure 49.

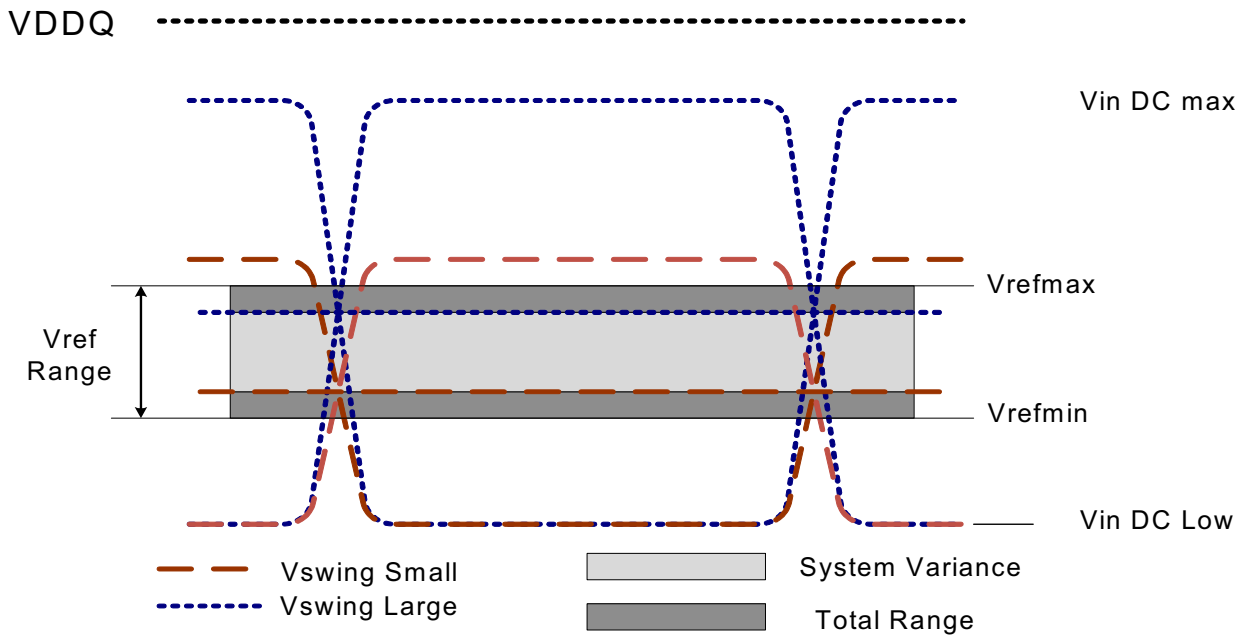


Figure 49 — V_{REF} Operating Range (V_{REF}min, V_{REF}max)

The V_{REF} step size is defined as the step size between adjacent steps. However, for a given design, the LPDDR4X-NVM device has one value for V_{REF} step size that falls within the range.

The V_{REF} set tolerance is the variation in the V_{REF} voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for V_{REF} set tolerance uncertainty. The range of V_{REF} set tolerance uncertainty is a function of number of steps n.

The V_{REF} set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max V_{REF} values for a specified range. An example of the step size and V_{REF} set tolerance is shown in Figure 50.

4.13 V_{REF}CA Training (cont'd)

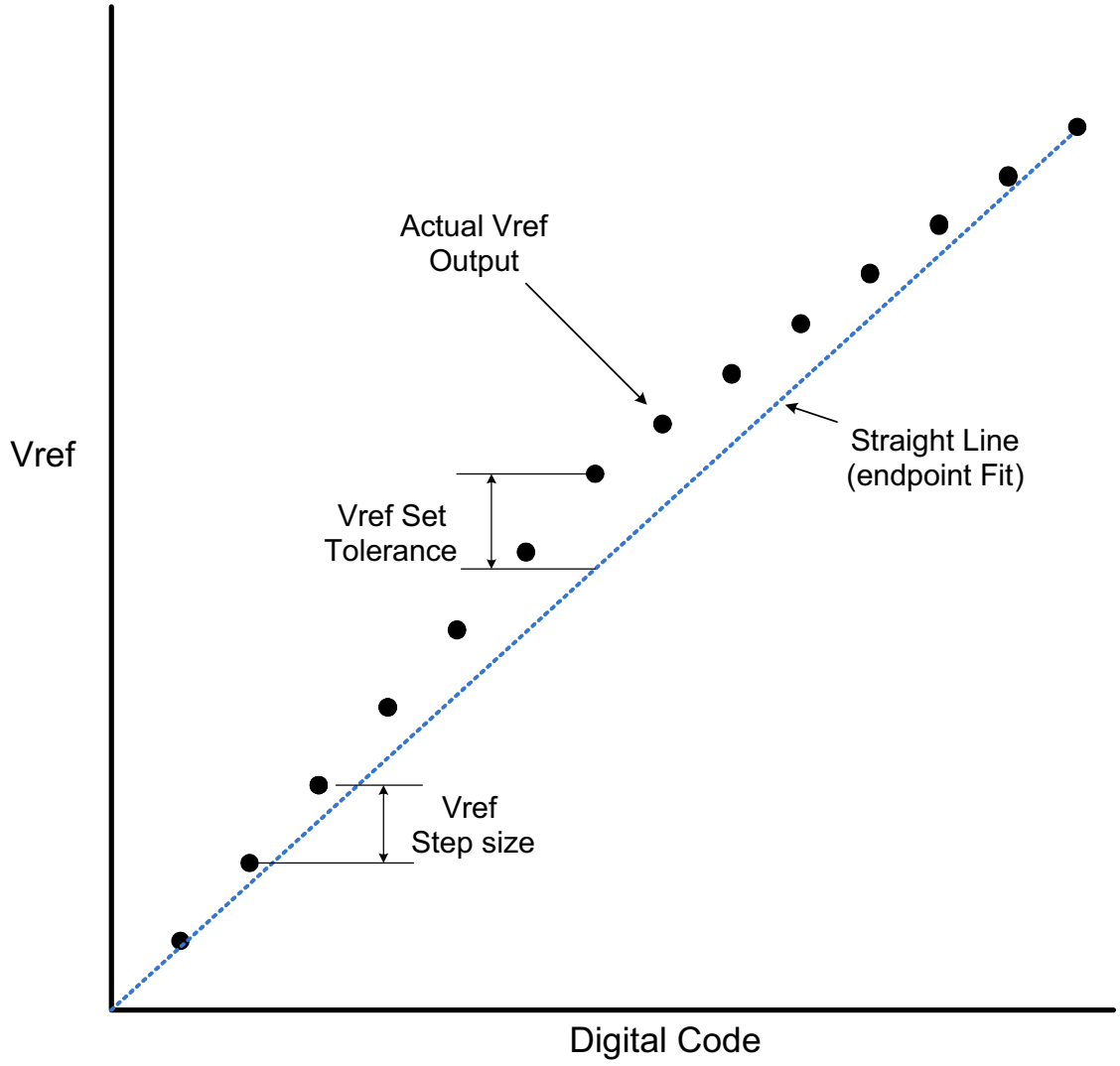


Figure 50 — Example of V_{REF} Set Tolerance (only Max Case is Shown) and Step Size

The V_{REF} increment/decrement step times are define by V_{REF}_time-short, Middle and long. The V_{REF}_time-short, V_{REF}_time-Middle and V_{REF}_time-long is defined from TS to TE as shown in Figure 51 where TE is referenced to when the V_{REF} voltage is at the final DC level within the V_{REF} valid tolerance(V_{REF}_val_tol).

The V_{REF} valid level is defined by V_{REF}_val tolerance to qualify the step time TE as shown in Figure 45. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any V_{REF} increment/decrement adjustment. This parameter is only applicable for component level validation/characterization.

V_{REF}_time-Short is for a single step size increment/decrement change in V_{REF} voltage.

V_{REF}_time-Middle is at least 2 step sizes increment/decrement change within the same V_{REF}CA range in V_{REF} voltage.

V_{REF}_time-Long is the time including up to V_{REF}min to V_{REF}max or V_{REF}max to V_{REF}min change across the V_{REF}CA Range in V_{REF} voltage.

TS - is referenced to MRS command clock
TE - is referenced to the V_{REF}_val_tol

4.13 V_{REF}CA Training (cont'd)

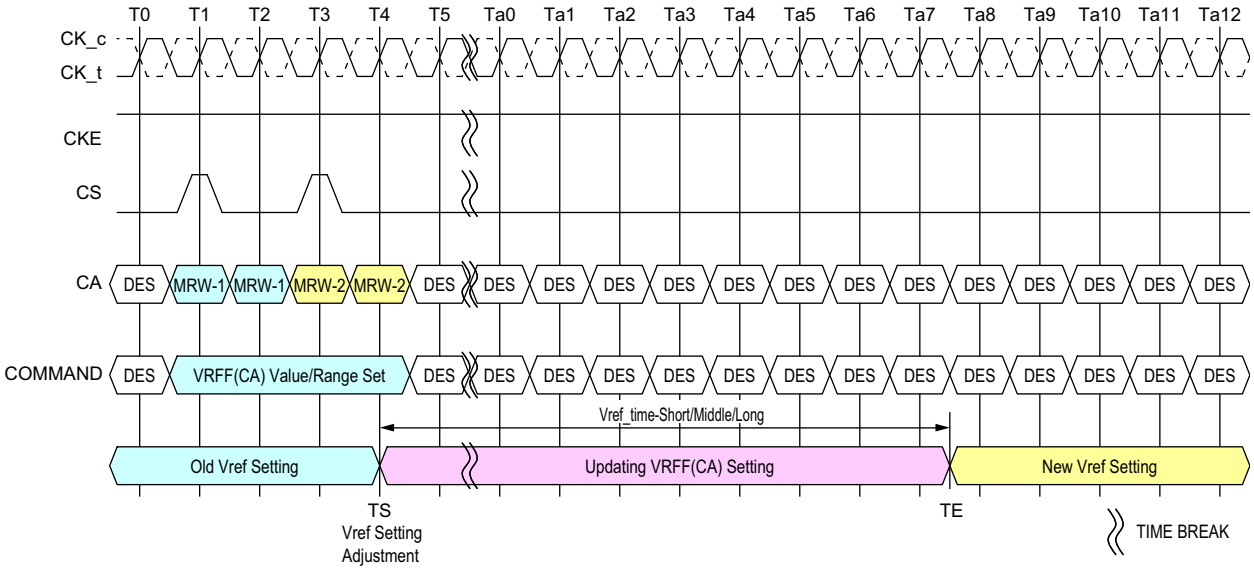


Figure 51 — V_{REF}_time for Short, Middle, and Long Timing Diagram

The MRW command to the mode register bits are as follows.

MR12 OP[5:0] : V_{REF}CA Setting
MR12 OP[6] : V_{REF}CA Range

4.13 V_{REF}CA Training (cont'd)

The minimum time required between two V_{REF} MRS commands is V_{REF}_time-short for single step and V_{REF}_time-Middle for a full voltage range step. Reference Figure 52 through Figure 55.

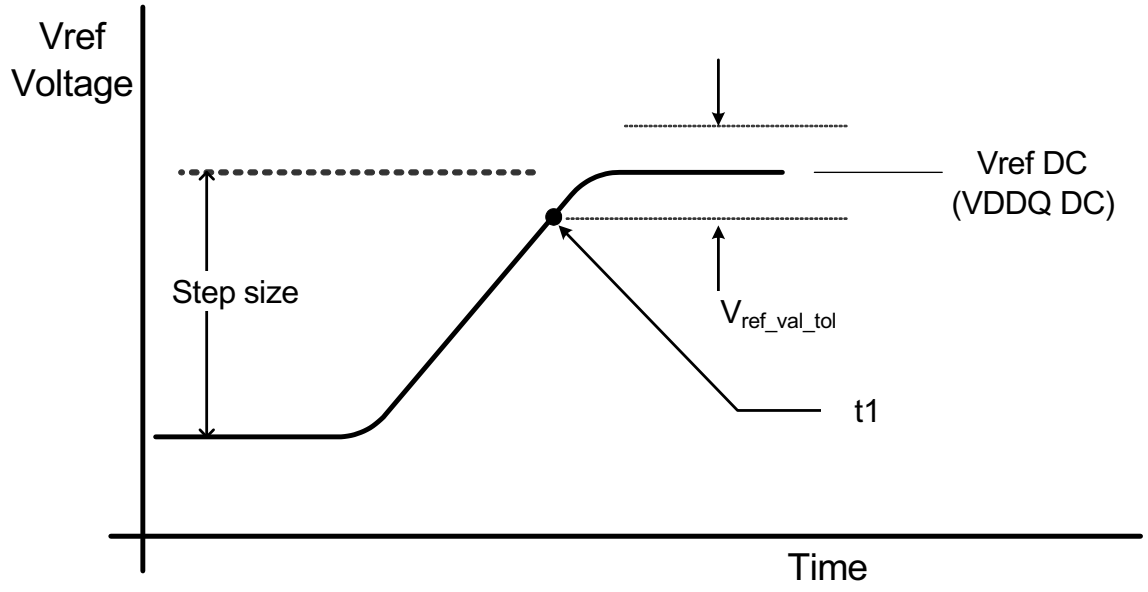


Figure 52 — V_{REF} Step Single Step Size Increment Case

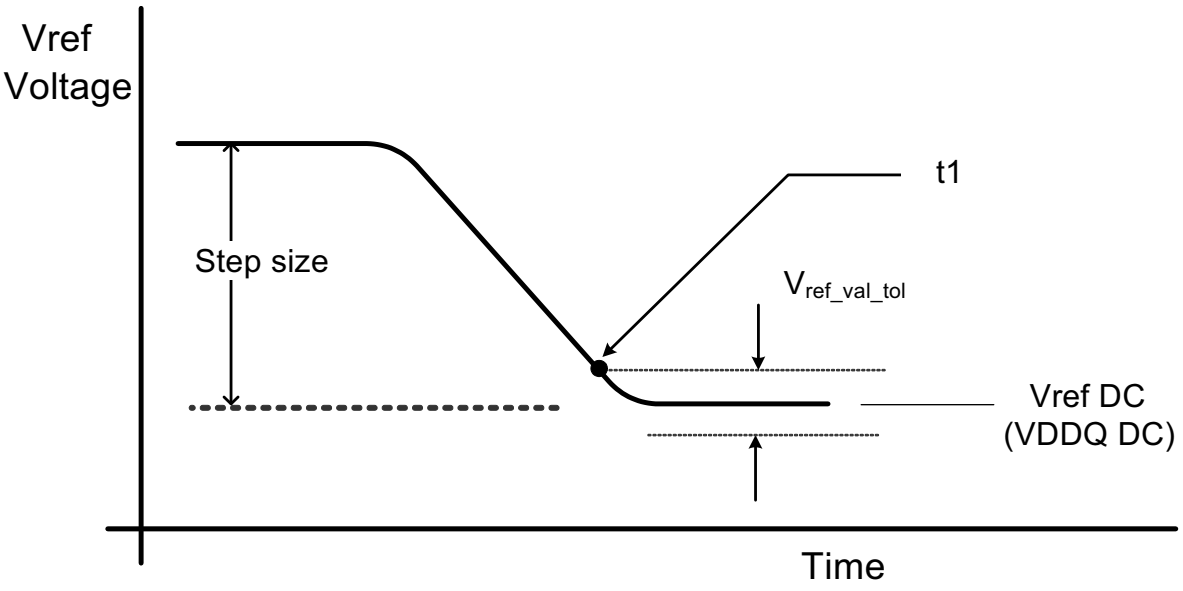


Figure 53 — V_{REF} Step Single Step Size Decrement Case

4.13 V_{REF}CA Training (cont'd)

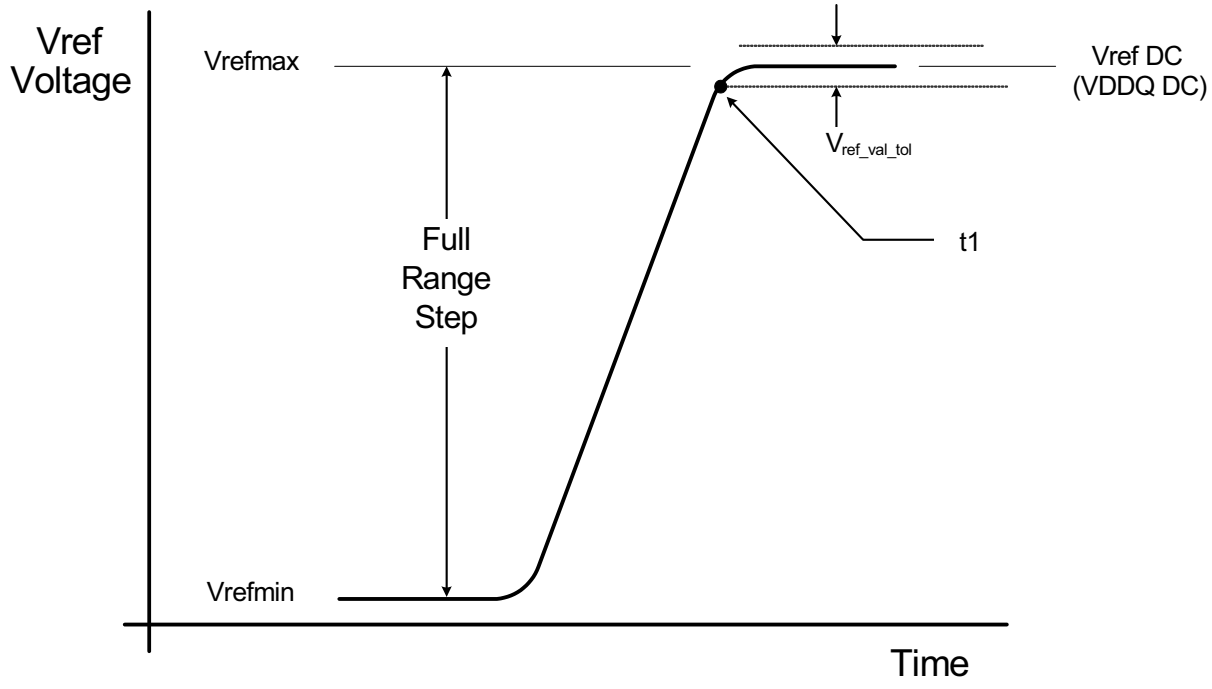


Figure 54 — V_{REF} Full Step from V_{REF}min to V_{REF}max Case

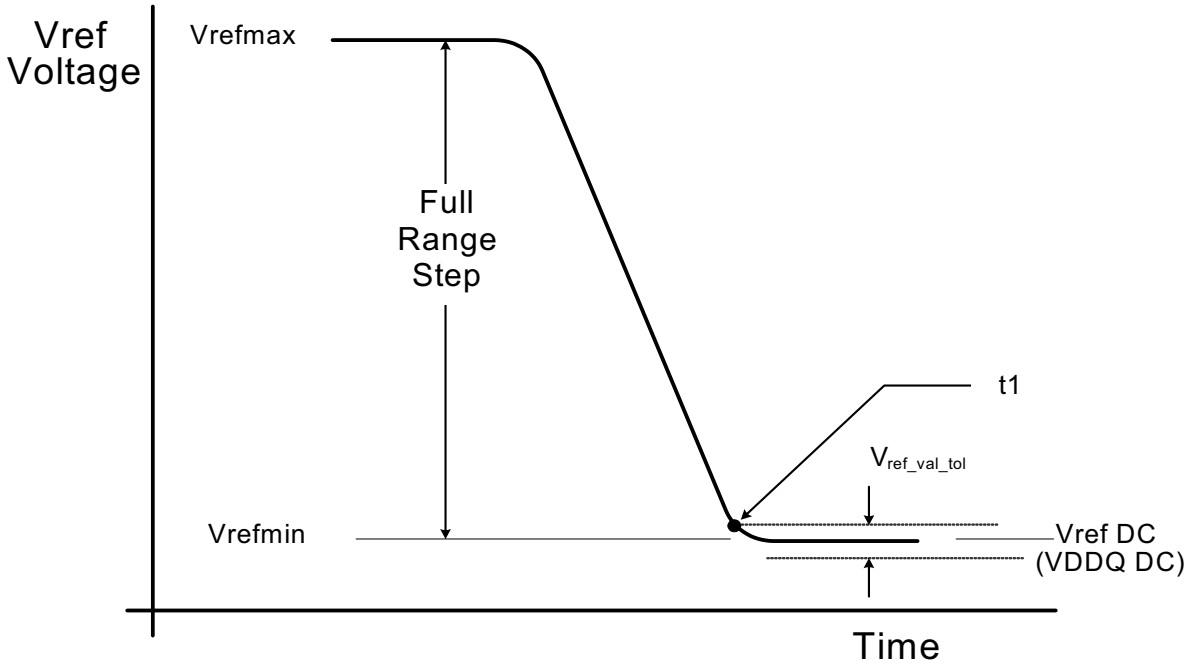


Figure 55 — V_{REF} Full Step from V_{REF}max to V_{REF}min Case

4.13 V_{REF}CA Training (cont'd)

Table 69 contains the CA internal V_{REF} specifications that will be characterized at the component level for compliance.

Table 69 — CA Internal V_{REF} Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
V_{REF} Max operating point Range0	V_{REF}_max_R0	-	-	44.9%	V_{DDQ}	1,11
V_{REF} Min operating point Range0	V_{REF}_min_R0	15%	-	-	V_{DDQ}	1,11
V_{REF} Max operating point Range1	V_{REF}_max_R1	-	-	62.9%	V_{DDQ}	1,11
V_{REF}Min operating point Range1	V_{REF}_min_R1	32.9%	-	-	V_{DDQ}	1,11
V_{REF} Step size	V_{REF}_step	0.50%	0.60%	0.70%	V_{DDQ}	2
V_{REF}Set Tolerance	V_{REF}_set_tol	-11	0	11	mV	3,4,6
		-1.1	0	1.1	mV	3,5,7
V_{REF} Step Time	V_{REF}_time-Short	-	-	100	ns	8
	V_{REF}_time_Middle	-	-	200	ns	12
	V_{REF}_time-Long	-	-	250	ns	9
	V_{REF}_time_weak	-	-	1	ms	13,14
V_{REF} Valid tolerance	V_{REF}_val_tol	-0.10%	0.00%	0.10%	V_{DDQ}	10

NOTE 1 V_{REF} DC voltage referenced to V_{DDQ}_DC.

NOTE 2 V_{REF} step size increment/decrement range. V_{REF} at DC level.

NOTE 3 V_{REF}_new = V_{REF}_old + n*V_{REF}_step; n= number of steps; if increment use "+"; If decrement use "-".

NOTE 4 The minimum value of V_{REF} setting tolerance = V_{REF}_new - 11mV. The maximum value of V_{REF} setting tolerance = V_{REF}_new + 11mV. For n>4.

NOTE 5 The minimum value of V_{REF} setting tolerance = V_{REF}_new - 1.1mV. The maximum value of V_{REF} setting tolerance = V_{REF}_new + 1.1mV. For n≤ 4.

NOTE 6 Measured by recording the min and max values of the V_{REF} output over the range, drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 7 Measured by recording the min and max values of the V_{REF} output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other V_{REF} output settings to that line.

NOTE 8 Time from MRS command to increment or decrement one step size for V_{REF}.

NOTE 9 Time from MRS command to increment or decrement V_{REF}min to V_{REF}max or V_{REF}max to V_{REF}min change across the V_{REF}CA Range in V_{REF} voltage.

NOTE 10 Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. V_{REF} valid is to qualify the step times which will be characterized at the component level.

NOTE 11 LPDDR4X-NVM range 0 or 1 set by MR12 OP[6].

NOTE 12 Time from MRS command to increment or decrement more than one step size up to a full range of V_{REF} voltage within the same V_{REF}CA range.

NOTE 13 Applies when VRCG high current mode is not enabled, specified by MR13[OP3] = 0.

NOTE 14 V_{REF}_time_weak covers all V_{REF}CA Range and Value change conditions are applied to V_{REF}_time_Short/Middle/Long.

4.14 Command Bus Training

4.14.1 Command Bus Training Details

The LPDDR4X-NVM command bus must be trained before enabling termination for high-frequency operation. LPDDR4X-NVM devices provide an internal $V_{REF}CA$ that defaults to a level suitable for un-terminated, low frequency operation, but the $V_{REF}CA$ must be trained to achieve suitable receiver voltage margin for terminated, high-frequency operation. The training mode described here centers the internal $V_{REF}CA$ in the CA data eye and at the same time allows for timing adjustments of the CS and CA signals to meet setup/hold requirements. Because it can be difficult to capture commands prior to training the CA inputs, the training mode described here uses a minimum of external commands to enter, train, and exit the Command Bus Training mode.

NOTE it is up to the system designer to determine what constitutes “low-frequency” and “high-frequency” based on the capabilities of the system. Low-frequency should then be defined as an operating frequency in which the system can reliably communicate with the LPDDR4X-NVM device before Command Bus Training is executed.

The LPDDR4X-NVM device uses Frequency Set-Points to enable multiple operating settings for the die. The LPDDR4X-NVM defaults to FSP-OP[0] at power-up, which has the default settings to operate in un-terminated, low-frequency environments. Prior to training, the mode register settings should be configured by setting MR13 OP[6]=1B (FSP-WR[1]) and setting all other mode register bits for FSP-OP[1] to the desired settings for high-frequency operation. Prior to entering Command Bus Training, the LPDDR4X-NVM device will be operating from FSP-OP[x]. Upon Command Bus Training entry when CKE is driven LOW, the LPDDR4X-NVM device will automatically switch to the alternate FSP register set (FSP-OP[y]) and use the alternate register settings during training (See note 6 in Figure 56 for more information on FSP-OP register sets). Upon training exit when CKE is driven HIGH, the LPDDR4X-NVM device will automatically switch back to the original FSP register set (FSP-OP[x]), returning to the “known-good” state that was operating prior to training. The training values for $V_{REF}CA$ are not retained by the device in FSP-OP[y] registers, and must be written to the registers after training exit.

1. To enter Command Bus Training mode, issue a MRW-1 command followed by a MRW-2 command to set MR13 OP[0]=1B (Command Bus Training Mode Enabled).
2. After time tMRD, CKE may be set LOW, causing the LPDDR4X-NVM device to switch from FSP-OP[x] to FSP-OP[y], and completing the entry into Command Bus Training mode. A status of DQS_t, DQS_c, DQ and ECCO are as follows, and ODT state of DQS_t, DQS_c, DQ and ECCO will be followed by MR11 OP[2:0] and MR13 OP[7]: FSP-OP except output pins.
   - DQS_t[0], DQS_c[0] become input pins for capturing DQ[6:0] levels by its toggling.
   - DQ[5:0] become input pins for setting $V_{REF}CA$ Level.
   - DQ[6] becomes a input pin for setting $V_{REF}CA$ Range.
   - DQ[7] and ECCO[0] become input pins and their input level is a Valid level or floating, either way is fine.
   - DQ[13:8] become output pins to feedback its captured CA[5:0] value via command bus by CS signal.
   - DQS_t[1], DQS_c[1],ECCO[1] and DQ[15:14] become output pins or disable, it means that the device may drive to a valid level or left floating.
3. At time tCAENT later, the device can accept to change its $V_{REF}CA$ Range and Value using input signals of DQS_t[0], DQS_c[0] and DQ[6:0] from existing value that’s setting via MR12 OP[6:0]. The mapping between MR12 OP code and DQs is shown in Table 70 At least one $V_{REF}CA$ setting is required before proceed to next training steps.
4. The new $V_{REF}CA$ value must “settle” for time tV_{REF}_LONG before attempting to latch CA information.
5. To verify that the receiver has the correct $V_{REF}CA$ setting and to further train the CA eye relative to clock (CK), values latched at the receiver on the CA bus are asynchronously output to the DQ bus.
6. To exit Command Bus Training mode, drive CKE HIGH, and after time tV_{REF}_LONG issue the MRW-1 command followed by the MRW-2 command to set MR13 OP[0]=0B. After time tMRW the LPDDR4X-NVM is ready for normal operation. After training exit the LPDDR4X-NVM will automatically switch back to the FSP-OP registers that were in use prior to training.

The relation between the value input on DQ[6:0] and the $V_{REF}CA$ value used during training is shown in Table 70. The value maps as indicated for MR12 OP[6:0].

4.14.1 Command Bus Training Details (cont'd)

Table 70 — Mapping of MR12 OP[6:0] Code and DQ[6:0] Input Pins

Inputs/Outputs	Mapping						
MR12 OP Code	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Number	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0

The relation between the captured CA[5:0] input pins and the DQ[13:8] output pins is shown in Table 71.

Table 71 — Mapping of CA[5:0] Input pins and DQ[13:8] Output pins

Inputs/Outputs	Mapping					
CA Number	CA5	CA4	CA3	CA2	CA1	CA0
DQ Number	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8

Command Bus Training may be executed from the IDLE state.

4.14.1.1 Training Sequence for Single-rank Systems

Note that the single-rank example shown here is assuming an initial low-frequency, non-terminated operating point, training a high-frequency, terminating operating point. The green text is low-frequency, magenta text is high-frequency. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-OP[x], See note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels to set up high-frequency operating parameters.
3. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode.
4. Drive CKE LOW, and change CK frequency to the high-frequency operating point.
5. Perform Command Bus Training (V_{REF}CA, CS, and CA).
6. Exit training, a change CK frequency to the low-frequency operating point prior to driving CKE HIGH, then issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the device).
7. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the device and setting all applicable mode register parameters.
8. Issue MRW-1 and MRW-2 commands to switch to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained and you may proceed to other training or normal operation.

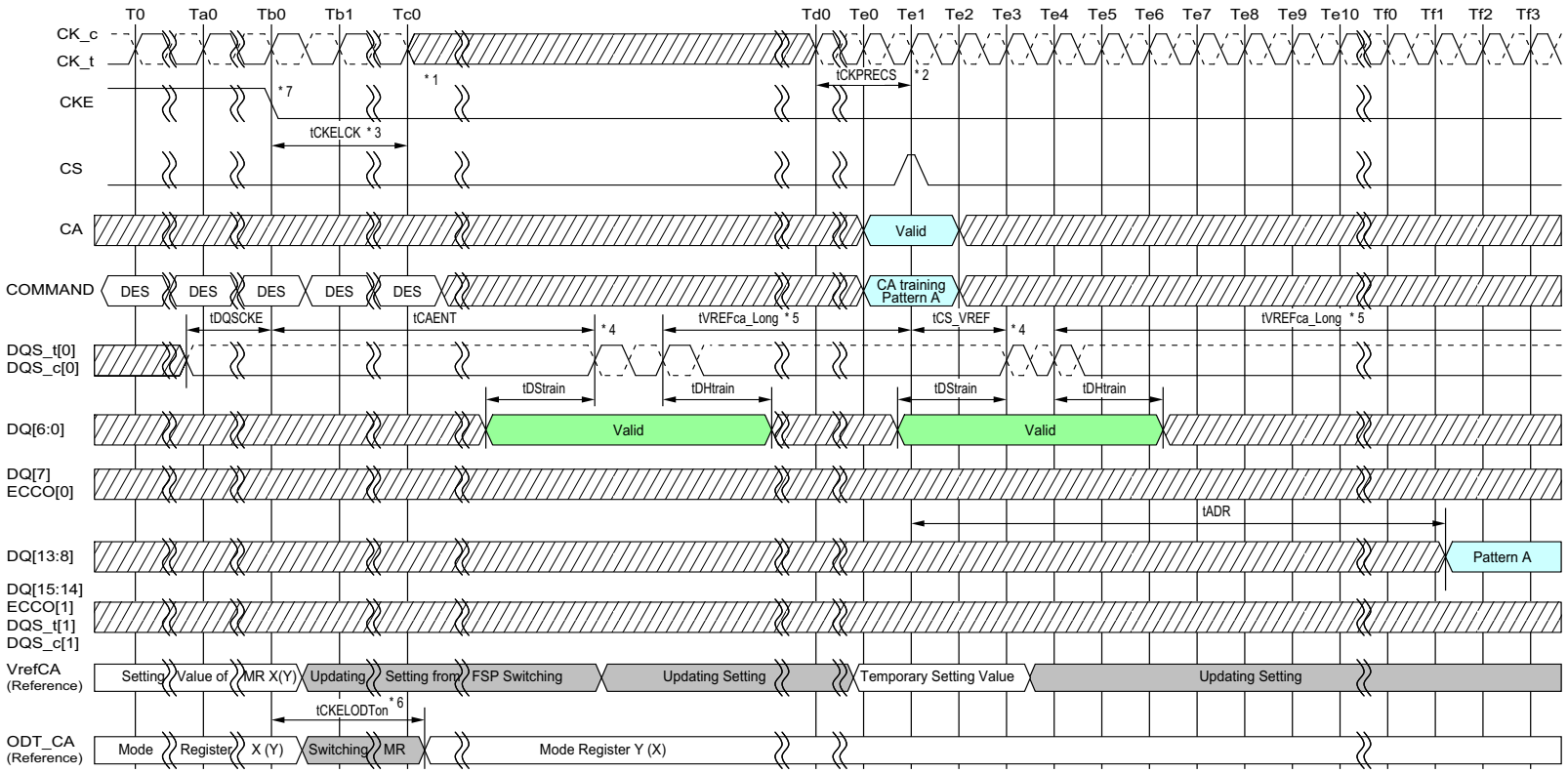
4.14.1.2 Training Sequence for Multi-rank Systems

Note that the multi-rank example shown here assumes an initial low-frequency operating point, training a high-frequency operating point. The green text is low-frequency, magenta text is high-frequency. Any operating point may be trained from any known good operating point.

1. Set MR13 OP[6]=1B to enable writing to Frequency Set Point 'y' (FSP-WR[y]) (or FSP-WR[x], See Note).
2. Write FSP-WR[y] (or FSP-WR[x]) registers for all channels and ranks to set up high frequency operating parameters.
3. Read MR0 OP[7] on all channels and ranks to determine which die are terminating, signified by MR0 OP[7]=1B.
4. Issue MRW-1 and MRW-2 commands to enter Command Bus Training mode on the terminating rank.
5. Drive CKE LOW on the terminating rank (or all ranks), and change CK frequency to the high-frequency operating point.
6. Perform Command Bus Training on the terminating rank (V_{REF}CA, CS, and CA).
7. Exit training by driving CKE HIGH, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands to write the trained values to FSP-WR[y] (or FSP-WR[x]). When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the device).
8. Issue MRW-1 and MRW-2 command to enter training mode on the non-terminating rank (but keep CKE HIGH)
9. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point.
10. Drive CKE LOW on the non-terminating (or all) ranks. The non-terminating rank(s) will now be using FSP-OP[y] (or FSP-OP[x]).
11. Perform Command Bus Training on the non-terminating rank (V_{REF}CA, CS, and CA).
12. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[x] (or FSP-OP[y]) to turn off termination.
13. Exit training by driving CKE HIGH on the non-terminating rank, change CK frequency to the low-frequency operating point, and issue MRW-1 and MRW-2 commands. When CKE is driven HIGH, the device will automatically switch back to the FSP-OP registers that were in use prior to training (i.e. trained values are not retained by the device).
14. Write the trained values to FSP-WR[y] (or FSP-WR[x]) by issuing MRW-1 and MRW-2 commands to the device and setting all applicable mode register parameters.
15. Issue MRW-1 and MRW-2 commands to switch the terminating rank to FSP-OP[y] (or FSP-OP[x]), to turn on termination, and change CK frequency to the high frequency operating point. At this point the Command Bus is trained for both ranks and you may proceed to other training or normal operation.

4.14.1.3 Command Bus Training Timing Diagrams

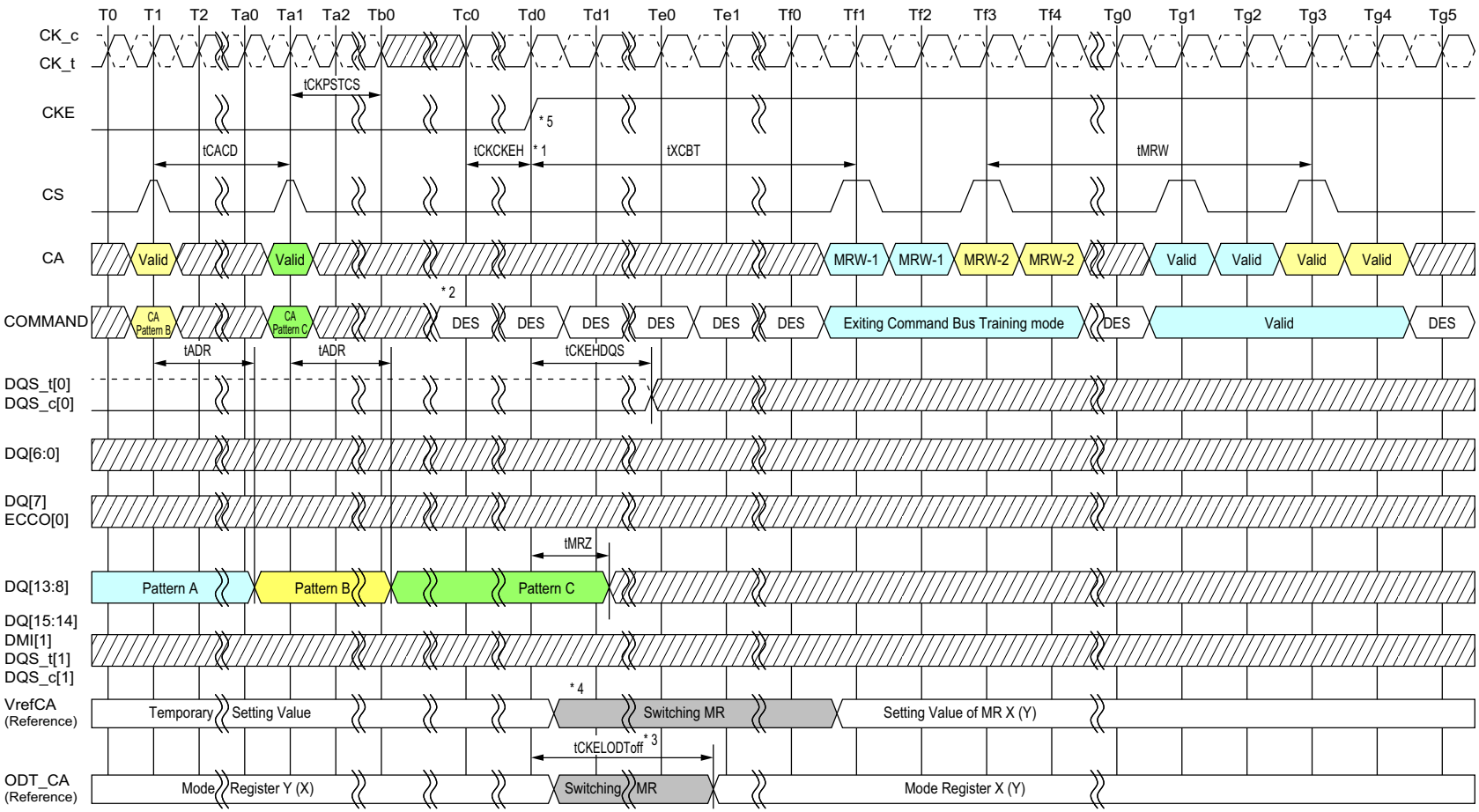
The basic Timing diagrams of Command Bus Training are shown in Figure 56 through Figure 58.



NOTES : 1. After tCKELCK clock can be stopped or frequency changed any time.
2. The input clock condition should be satisfied tCKPRECS.
3. Continue to Drive CK and Hold CS pins low until tCKELCK after CKE is low (which disables command decoding).
4. The device may or may not capture first rising/falling edge of DQS_t/c due to an unstable first rising edge. Hence provide at least consecutive 2 pulses of DQS signal input is required in every DQS input signal at capturing DQ6:0 signals. The captured value of DQ6:0 signal level by each DQS edges are overwritten at any time and the device updates its VREFca setting of MR12 temporary after time tVREFca_Long.
5. tVREF_LONG may be reduced to tVREF_SHORT if the following conditions are met: 1) The new Vref setting is a single step above or below the old Vref setting, and 2) The DQS pulses a single time, or the new Vref setting value on DQ[6:0] is static and meets tDSTRAIN/tDHTRAIN for every DQS pulse applied.
6. When CKE is driven LOW, the device will switch its FSP-OP registers to use the alternate (i.e. non-active) set. Example: If the device is currently using FSP-OP[0], then it will switch to FSP-OP[1] when CKE is driven LOW. All operating parameters should be written to the alternate mode registers before entering Command Bus Training to ensure that ODT settings, RL setting, etc., are set to the correct values. If the alternate FSP-OP has ODT_CA disabled then termination will not enable in CA Bus Training mode.
7. When CKE is driven low in Command Bus Training mode, the LPDDR4X-NVM will change operation to the alternate FSP, i.e. the inverse of the FSP programmed in the FSP-OP mode register.

Figure 56 — Entering Command Bus Training Mode and CA Training Pattern Input and Output with V_{REF}CA Value Update

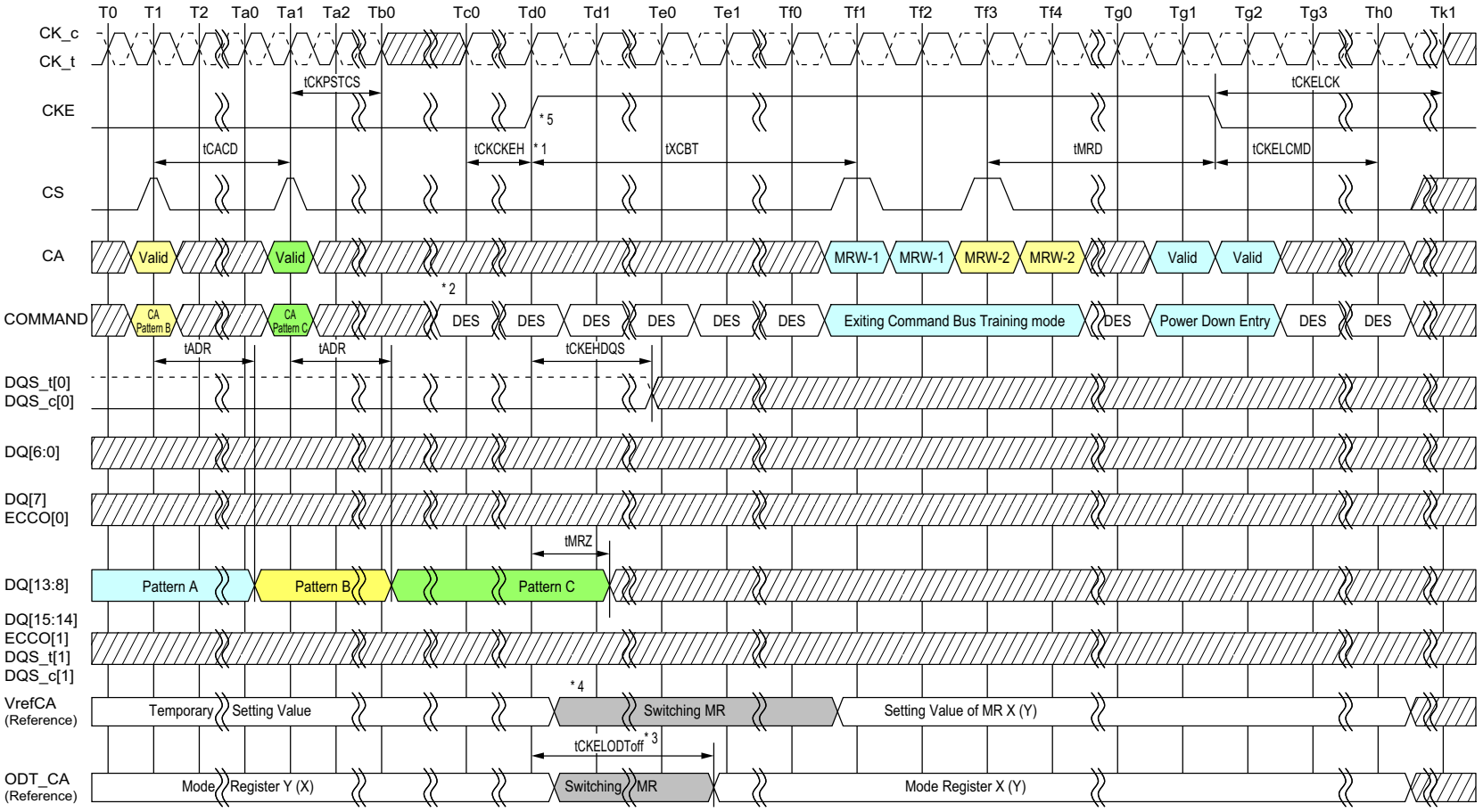
4.13.1.3 Command Bus Training Timing Diagrams (cont'd)



NOTES : 1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high.
When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)
2. CS must be Deselect (low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the device's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).
Example: If the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device, and must be written to the FSP-OP register set before returning to operation at the trained frequency.
Example: VREF(ca) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4X-NVM will revert to the FSP in operation when Command Bus Training mode was entered.

Figure 57 — Consecutive V_{REF}CA Value Updates

4.13.1.3 Command Bus Training Timing Diagrams (cont'd)



NOTES : 1. Clock can be stopped or frequency changed any time before tCKCKEH. CK must meet tCKCKEH before CKE is driven high.
When CKE is driven high the clock frequency must be returned to the original frequency (the frequency corresponding to the FSP at which Command Bus Training mode was entered)

2. CS must be Deselect (low) tCKCKEH before CKE is driven high.
3. When CKE is driven high, the device's ODT_CA will revert to the state/value defined by FSP-OP prior to Command Bus Training mode entry, i.e. the original frequency set point (FSP-OP, MR13-OP[7]).
Example: If the device was using FSP-OP[1] for training, then it will switch to FSP-OP[0] when CKE is driven HIGH.
4. Training values are not retained by the device, and must be written to the FSP-OP register set before returning to operation at the trained frequency.
Example: VREF(ca) will return to the value programmed in the original set point.
5. When CKE is driven high the LPDDR4X-NVM will revert to the FSP in operation when Command Bus Training mode was entered.

Figure 58 — Exiting Command Bus Training Mode with Power Down Entry

4.14.1.4 Command Bus Training AC Timing Table

Table 72 — Command Bus Training AC Timing

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4266		
Command Bus Training Timing												
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)								-	
Data Setup for V_{REF} Training Mode	tDStrain	Min	2								ns	
Data Hold for V_{REF} Training Mode	tDHtrain	Min	2								ns	
Asynchronous Data Read	tADR	Max	20								ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)								tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10								ns	1
First CA Bus Training Command Following CKE Low	tCAENT	Min	250								ns	
V_{REF} Step Time – multiple steps	$tV_{REF}CA\_LONG$	Max	250								ns	
V_{REF} Step Time – one step	$tV_{REF}CA\_SHORT$	Max	100								ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tck + tXP (tXP = max(7.5ns, 5nCK))								-	
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))								-	
Minimum delay from CS to DQS toggle in command bus training	tCS_V_{REF}	Min	2								tCK	
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS		10								ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)								-	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5								ns	
ODT turn-on Latency from CKE	tCKELODTon	Min	20								ns	
ODT turn-off Latency from CKE	tCKELODToff	Min	20								ns	
Command Bus Training Timing												
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK, 200ns)								-	3
	tXCBT_Middle	Min	Max(5nCK, 200ns)								-	3
	tXCBT_Long	Min	Max(5nCK, 250ns)								-	3

Table 72 — Command Bus Training AC Timing (cont'd)

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4266		
NOTE 1 DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level. NOTE 2 If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR. NOTE 3 Exit Command Bus Training Mode to next valid command delay Time depends on value of V_{REF}CA setting: MR12 OP[5:0] and V_{REF}CA Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 76.												

4.15 Frequency Set Point

Frequency Set-Points allow the LPDDR4X-NVM CA Bus to be switched between two differing operating frequencies, with changes in voltage swings and termination values, without ever being in an untrained state which could result in a loss of communication to the device. This is accomplished by duplicating all CA Bus mode register parameters, as well as other mode register parameters commonly changed with operating frequency. These duplicated registers form two sets that use the same mode register addresses, with read/write access controlled by MR bit FSP-WR (Frequency Set-Point Write/Read) and the device operating point controlled by another MR bit FSP-OP (Frequency Set-Point Operation). Changing the FSP-WR bit allows MR parameters to be changed for an alternate Frequency Set-Point without affecting the LPDDR4X-NVM device's current operation. Once all necessary parameters have been written to the alternate Set-Point, changing the FSP-OP bit will switch operation to use all of the new parameters simultaneously (within tFC), eliminating the possibility of a loss of communication that could be caused by a partial configuration change.

Parameters which have two physical registers controlled by FSP-WR and FSP-OP are shown in Table 73.

Table 73 — Mode Register Function with Two Physical Registers

MR#	Operand	Function	Note
MR1	OP[3]	RD-PRE (RD Preamble Type)	
	OP[7]	PST (RD Postamble Length)	
MR2	OP[2:0]	RL (Read latency)	
MR3	OP[0]	PU-Cal (Pull-up Calibration Point)	
	OP[5:3]	PDDS (Pull-Down Drive Strength)	
	OP[6]	ECCO (ECC Output during READ Enable)	
MR11	OP[6:4]	CA ODT (CA Bus Receiver On-Die-Termination)	
MR12	OP[5:0]	$V_{REF}CA$ ($V_{REF}CA$ Setting)	
	OP[6]	$V_{REF}CA$ ($V_{REF}CA$ Range)	
MR22	OP[2:0]	SoC ODT (Controller ODT Value for VOH calibration)	
	OP[3]	ODTE-CK (CK ODT enabled for non terminating rank)	
	OP[4]	ODTE-CS (CS ODT enable for non-terminating rank)	
	OP[5]	ODTD-CA (CA ODT termination disable)	

NOTE 1 Supporting the two physical registers for Burst Length: MR1 OP[1:0] is optional.
Applications requiring support of both manufacturer options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to manufacturer data sheets for detail.

See Mode Register Definition for more details.

4.14 Frequency Set Point (cont'd)

Table 74 shows how the two mode registers for each of the parameters above can be modified by setting the appropriate FSP-WR value, and how device operation can be switched between operating points by setting the appropriate FSP-OP value. The FSP-WR and FSP-OP functions operate completely independently.

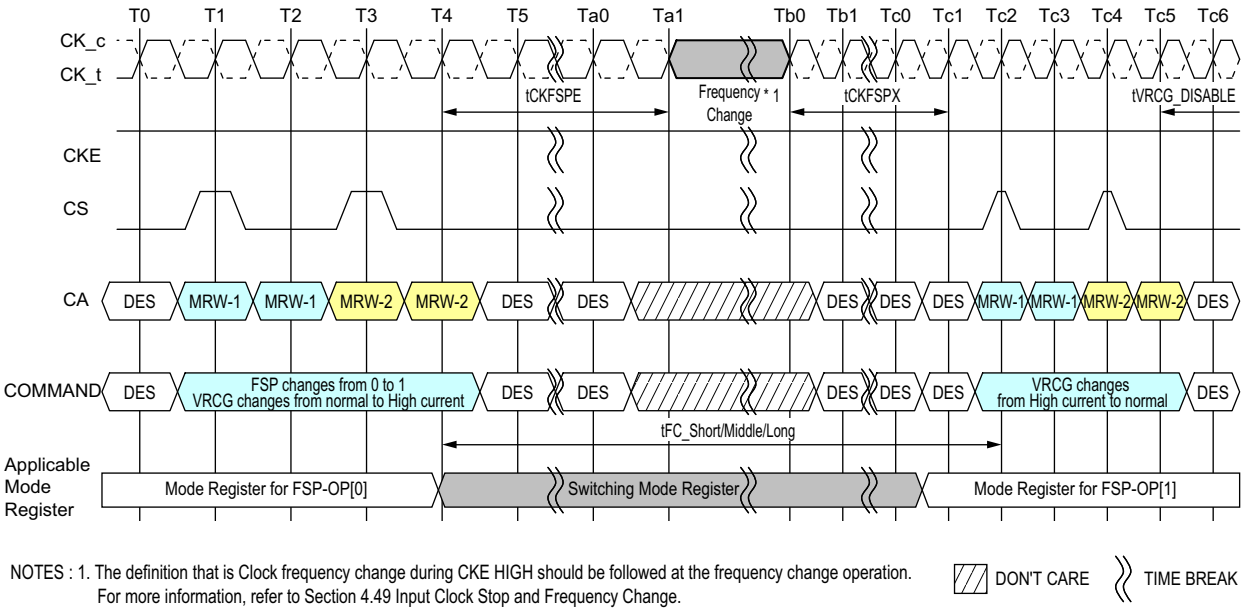
Table 74 — Relation between MR Setting and LPDDR4X-NVM Device Operation

Function	MR# and Operand	Data	Operation	Note
FSP-WR	MR13 OP[6]	0 (Default)	Data write to Mode Register N for FSP-OP[0] by MRW Command. Data read from Mode Register N for FSP-OP[0] by MRR Command.	1
		1	Data write to Mode Register N for FSP-OP[1] by MRW Command. Data read from Mode Register N for FSP-OP[1] by MRR Command.	
FSP-OP	MR13 OP[7]	0 (Default)	Device operates with Mode Register N for FSP-OP[0] setting.	2
		1	Device operates with Mode Register N for FSP-OP[1] setting.	

NOTE 1 FSP-WR stands for Frequency Set Point Write/Read.
NOTE 2 FSP-OP stands for Frequency Set Point Operating Point.

4.15.1 Frequency Set Point Update Timing

The Frequency set point update timing is shown in Figure 59 and Table 75. When changing the frequency set point via MR13 OP[7], the VRCG setting: MR13 OP[3] have to be changed into V_{REF} Fast Response (high current) mode at the same time. After Frequency Change time (tFC) is satisfied. VRCG can be changed into Normal Operation mode via MR13 OP[3].



NOTES : 1. The definition that is Clock frequency change during CKE HIGH should be followed at the frequency change operation. For more information, refer to Section 4.49 Input Clock Stop and Frequency Change.

Figure 59 — Frequency Set Point Switching Timing

4.15.1 Frequency Set Point Update Timing (cont'd)

Table 75 — AC Timing Table

Parameter	Symbol	Min/ Max	Data Rate								Unit	Note
			533	1066	1600	2133	2667	3200	3733	4266		
Frequency Set Point parameters												
Frequency Set Point Switching Time	tFC_Short	MIN	200								ns	1
	tFC_Middle	MIN	200								ns	1
	tFC_Long	MIN	250								ns	1
Valid Clock Requirement after Entering FSP Change	tCKFSPE	MIN	max(7.5ns, 4nCK)								-	
Valid Clock Requirement before 1st Valid Command after FSP change	tCKFSPX	MIN	max(7.5ns, 4nCK)								-	

NOTE 1 Frequency Set Point Switching Time depends on value of $V_{REF}CA$ setting: MR12 OP[5:0] and $V_{REF}CA$ Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in Table 76.

Table 76 — tFC Value Mapping

Application	Step Size		Range	
	From FSP -OP0	To FSP-OP1	From FSP -OP0	To FSP-OP1
tFC_Short	Base	A single step size increment/decrement	Base	No Change
tFC_Middle	Base	Two or more step size increment/decrement	Base	No Change
tFC_Long	-	-	Base	Change

NOTE 1 As well as change from FSP-OP1 to FSP-OP0.

Table 77 provides an example of tFC value mapping when FSP-OP moves from OP0 to OP1.

Table 77 — tFC Value Mapping Example

Case	From/To	FSP-OP: MR13 OP[7]	$V_{REF}CA$ Setting: MR12: OP[5:0]	$V_{REF}CA$ Range: MR12 OP[6]	Application	Note
1	From	0	001100	0	tFC_Short	1
	To	1	001101	0		
2	From	0	001100	0	tFC_Middle	2
	To	1	001110	0		
3	From	0	Don't Care	0	tFC_Long	3
	To	1	Don't Care	1		

NOTE 1 A single step size increment/decrement for $V_{REF}CA$ Setting Value.
NOTE 2 Two or more step size increment/decrement for $V_{REF}CA$ Setting Value.
NOTE 3 $V_{REF}CA$ Range is changed. In this case changing $V_{REF}CA$ Setting doesn't affect tFC value.

4.15.1 Frequency Set Point Update Timing (cont'd)

The LPDDR4X-NVM device defaults to FSP-OP[0] at power-up. Both Set-Points default to settings needed to operate in un-terminated, low-frequency environments. To enable the LPDDR4X-NVM device to operate at higher frequencies, Command Bus Training mode should be utilized to train the alternate Frequency Set-Point (Figure 60). See the section Command Bus Training for more details on this training mode.

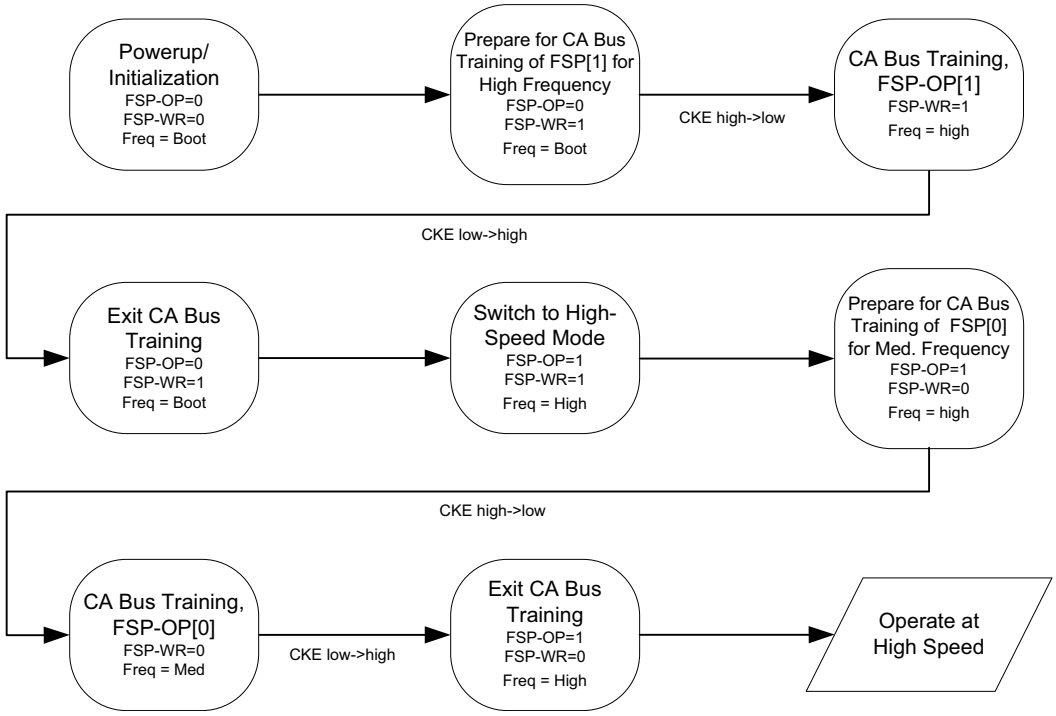


Figure 60 — Training Two Frequency Set-Points

Once both Frequency Set-Points have been trained, switching between points can be performed by a single MRW followed by waiting for tFC (Figure 61).

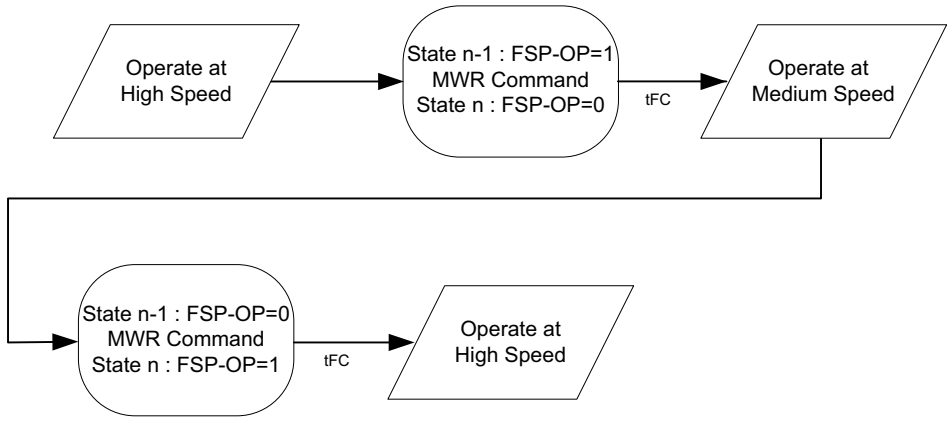


Figure 61 — Switching Between Two Trained Frequency Set-Points

Switching to a third (or more) Set-Point can be accomplished if the memory controller has stored the previously-trained values (in particular the V_{REF}CA calibration value) and re-writes these to the alternate Set-Point before switching FSP-OP (Figure 62).

4.15.1 Frequency Set Point Update Timing (cont'd)

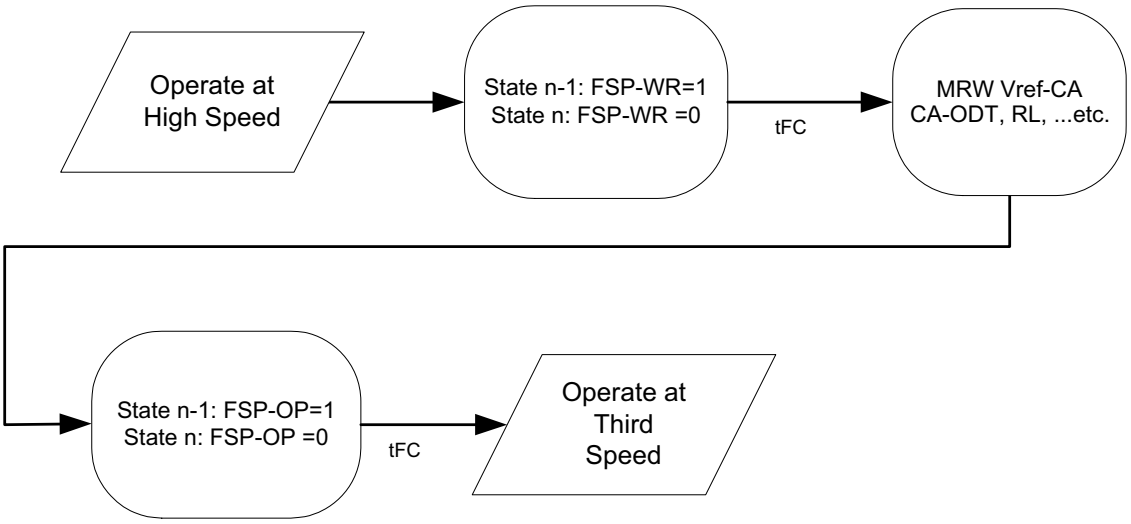


Figure 62 — Switching to a Third Trained Frequency Set-Point

4.16 RD DQ Calibration

4.16.1 RD DQ Calibration for x16 Mode

LPDDR4X-NVM devices feature a RD DQ Calibration training function that outputs a 16-bit user-defined pattern on the DQ pins. RD DQ Calibration is initiated by issuing a MPC-1 [RD DQ Calibration] command followed by a CAS-2 command, causing the LPDDR4X-NVM device to drive the contents of MR32 followed by the contents of MR40 on each of DQ[15:0] and ECCO[1:0]. The pattern can be inverted on selected DQ pins according to user-defined invert masks written to MR15 and MR20.

4.16.1.1 RD DQ Calibration Training Procedure

Reference Figure 63 and Figure 64.

The procedure for executing RD DQ Calibration is:

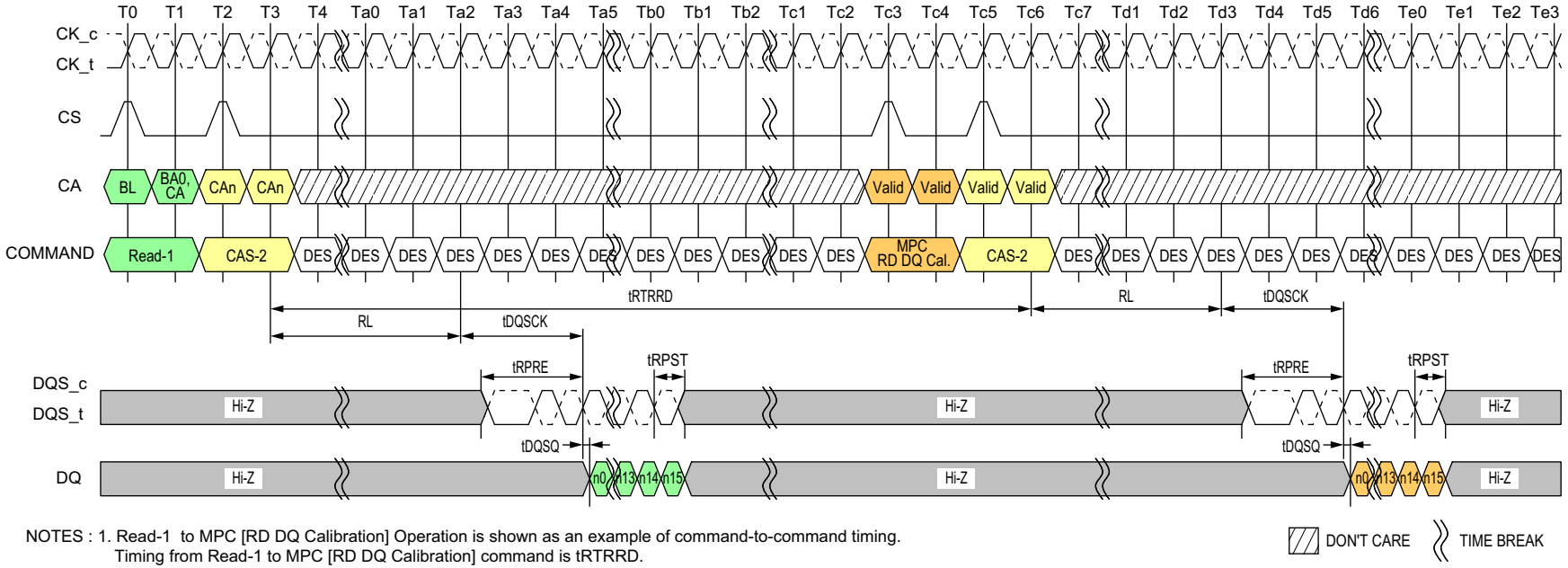
- Issue MRW commands to write MR32 (first eight bits), MR40 (second eight bits), MR15 (eight-bit invert mask for byte 0), and MR20 (eight-bit invert mask for byte 1).
  - Optionally this step could be skipped to use the default patterns
    - MR32 default = 5Ah
    - MR40 default = 3Ch
    - MR15 default = 55h
    - MR20 default = 55h
- Issue an MPC-1 [RD DQ Calibration] command followed immediately by a CAS-2 command.
  - Each time an MPC-1 [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4X-NVM device, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
  - The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit (see Table 78).
  - Note that the pattern is driven on the ECCO pins, but no data bus inversion function is enabled, even if ECCO is enabled in the device mode register.
  - The MPC-1 [RD DQ Calibration] command can be issued every tCCD seamlessly, and tRTRRD delay is required between Array Read command and the MPC-1 [RD DQ Calibration] command as well the delay required between the MPC-1 [RD DQ Calibration] command and an array read.
  - The operands received with the CAS-2 command must be driven LOW.
- DQ Read Training can be performed with any or no banks active with CKE high.

Table 78 — Invert Mask Assignments

DQ Pin	0	1	2	3	ECCO[0]	4	5	6	7
MR15 bit	0	1	2	3	N/A	4	5	6	7

DQ Pin	8	9	10	11	ECCO[1]	12	13	14	15
MR20 bit	0	1	2	3	N/A	4	5	6	7

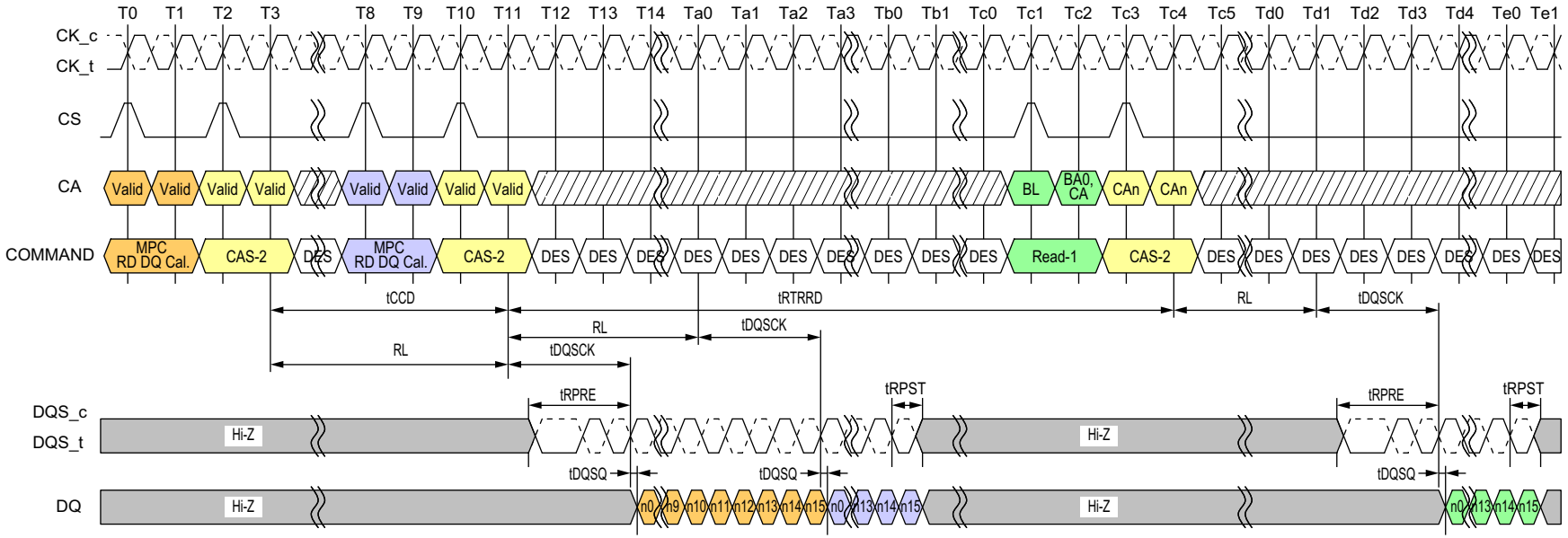
4.15.1.1 RD DQ Calibration Training Procedure (cont'd)



NOTES : 1. Read-1 to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.
Timing from Read-1 to MPC [RD DQ Calibration] command is tRTRRD.
2. MPC [RD DQ Calibration] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
3. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.
4. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 63 — DQ Read Training Timing: Read to Read DQ Calibration

4.15.1.1 RD DQ Calibration Training Procedure (cont'd)



NOTES : 1. MPC [RD DQ Calibration] to MPC [RD DQ Calibration] Operation is shown as an example of command-to-command timing.
2. MPC [RD DQ Calibration] to Read-1 Operation is shown as an example of command-to-command timing.
3. MPC [RD DQ Calibration] uses the same command-to-data timing relationship (RL, tDQSCK, tDQSQ) as a Read-1 command.
4. Seamless MPC [RD DQ Calibration] commands may be executed by repeating the command every tCCD time.
5. Timing from MPC [RD DQ Calibration] command to Read-1 is tRTRRD.
6. BL = 16, Read Preamble: Toggle, Read Postamble: 0.5nCK.
7. DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 64 — DQ Read Training Timing: Read DQ Cal. to Read DQ Cal. / Read

4.16.1.2 DQ Read Training Example

An example of DQ Read Training output is shown in Table 79. This shows the 16-bit data pattern that will be driven on each DQ when a DQ Read Training command is executed. This output assumes the following mode register values are used:

- MR32 = 1CH
- MR40 = 59H
- MR15 = 55H
- MR20 = 55H

Table 79 — DQ Read Calibration Bit Ordering and Inversion Example

Pin		Bit Sequence →															
	Invert	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DQ0	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ1	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ2	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ3	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
ECCO[0]	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ4	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ5	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ6	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ7	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ8	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ9	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ10	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ11	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
ECCO[1]	Never	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ12	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ13	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
DQ14	Yes	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
DQ15	No	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

NOTE 1 The patterns contained in MR32 and MR40 are transmitted on DQ[15:0] and ECCO[1:0] when RD DQ Calibration is initiated via a MPC-1 [RD DQ Calibration] command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern is 27H, then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B *(written in hex: 27H)*.

NOTE 2 MR15 and MR20 may be used to invert the MR32/MR40 data pattern on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the ECCO[1:0] pins.

NOTE 3 ECCO [1:0] outputs status follows Table 79.

NOTE 4 No ECC Output (ECCO) function is enacted during RD DQ Calibration, even if ECCO is enabled in MR3-OP[6].

4.16.1.3 MPC of Read DQ Calibration after Power-Down Exit

Following the power-down state, an additional time, tMRRI, is required prior to issuing the MPC of Read DQ Calibration command (Figure 65). This additional time (equivalent to tRCD) is required in order to be able to maximize power-down current savings by allowing more power-up time for the Read DQ data in MR32 and MR40 data path after exit from standby, power-down mode.

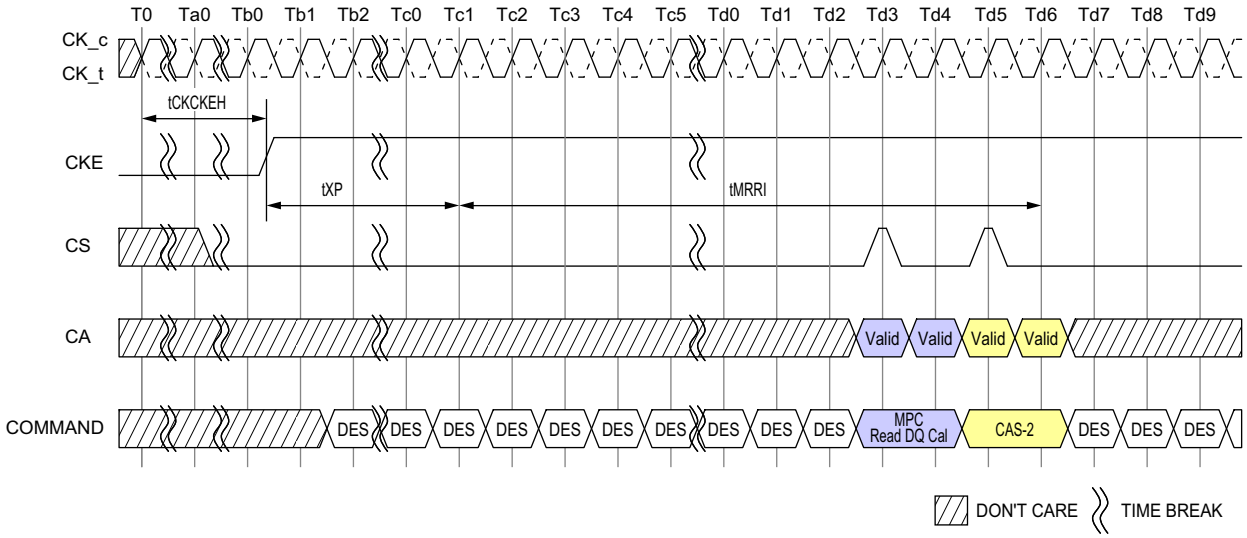


Figure 65 — MPC Read DQ Calibration following Power-Down State

4.17 READ Preamble Training

LPDDR4X-NVM READ Preamble Training is supported through the MPC function.

This mode can be used to train or read level the DQS receivers. Once READ Preamble Training is enabled by MR13[OP1] = 1, the LPDDR4X-NVM device will drive DQS_t LOW, DQS_c HIGH within tSDO and remain at these levels until an MPC DQ READ Calibration command is issued.

During READ Preamble Training the DQS preamble provided during normal operation will not be driven by the device. Once the MPC DQ READ Calibration command is issued, the device will drive DQS_t/DQS_c and DQ like a normal READ burst after RL and tDQSCK. Prior to the MPC DQ READ Calibration command, the device may or may not drive DQ[15:0] in this mode.

While in READ Preamble Training Mode, only READ DQ Calibration commands may be issued.

- Issue an MPC [RD DQ Calibration] command followed immediately by a CAS-2 command.
  - Each time an MPC [RD DQ Calibration] command followed by a CAS-2 is received by the LPDDR4X-NVM device, a 16-bit data burst will, after the currently set RL, drive the eight bits programmed in MR32 followed by the eight bits programmed in MR40 on all I/O pins.
  - The data pattern will be inverted for I/O pins with a '1' programmed in the corresponding invert mask mode register bit.
  - Note that the calibration pattern is driven on the ECCO pins even if ECCO is enabled in the device mode register.
  - This command can be issued every tCCD seamlessly.
  - The operands received with the CAS-2 command must be driven LOW.

READ Preamble Training is exited within tSDO after setting MR13[OP1] = 0.

Reference Figure 66 and Table 80.

4.16 READ Preamble Training (cont'd)

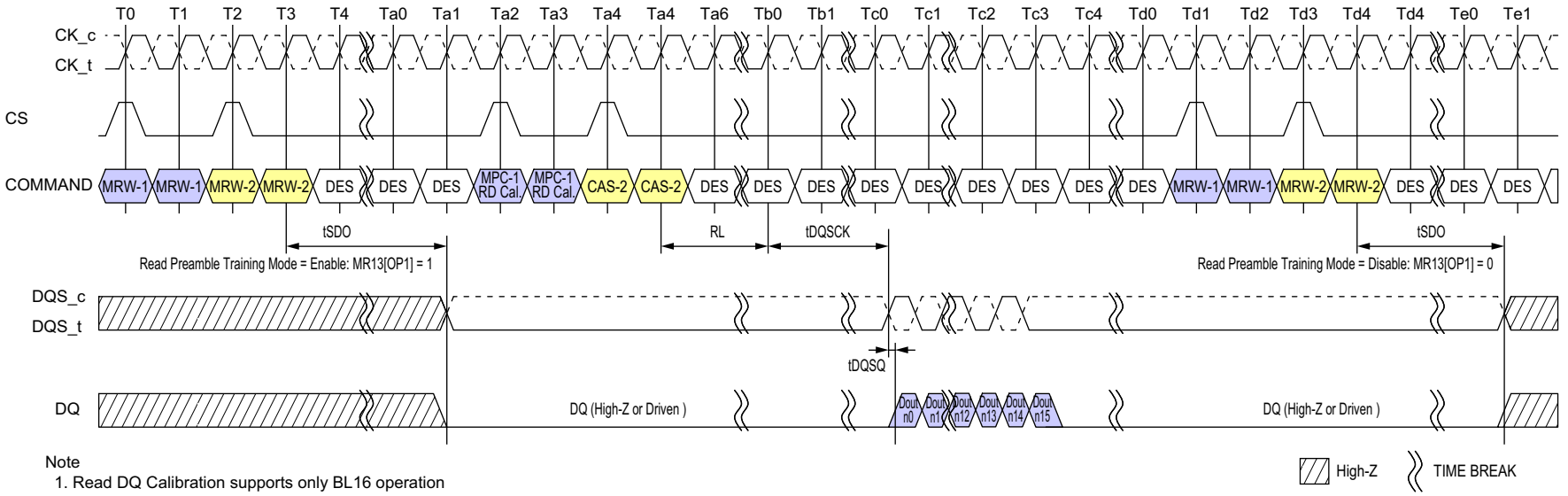


Figure 66 — Read Preamble Training

Table 80 — Timing Parameters

Parameter	Symbol	Min	Max	Unit	Notes
Delay from MRW command to DQS Driven	tSDO	-	Max(12nCK, 20ns)	-	

4.18 Multi-Purpose Command (MPC)

LPDDR4X-NVM devices use the MPC command to issue a NOP and to access various training modes. The MPC command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK, as defined by the Command Truth Table (Table 96). The MPC command has three operands (OP[6:0]) that are decoded to execute specific commands in the device. OP[6] is a special bit that is decoded on the first rising CK edge of the MPC command. When OP[6]=0 then the device executes a NOP (no operation) command, and when OP[6]=1 then the device further decodes one of three training commands.

When OP[6]=1 and when the training command includes a Read operation, the MPC command must be followed immediately by a CAS-2 command. For training commands that Read the device, read latency (RL) is counted from the second rising CK edge of the CAS-2 command with the same timing relationship as any normal Read command. The operands of the CAS-2 command following a MPC Read command must be driven LOW.
The following MPC commands must be followed by a CAS-2 command:

- Read DQ Calibration

All other MPC-1 commands do not require a CAS-2 command, including:

- NOP
- Start ZQ Calibration
- Latch ZQ Calibration

Table 81 — MPC Command Definition

LPDDR4X-NVM Command	SDR Command Pins			SDR CA Pins						CK_t EDGE	Notes
	CKE		CS	CA0	CA1	CA2	CA3	CA4	CA5		
	CK_t(n-1)	CK_t(n)									
MPC (Train, NOP)	H	H	H	L	L	L	L	L	OP6	R1	1, 2
			L	OP0	OP1	OP2	OP3	OP4	OP5	R2	

Table 82 — MPC Command Definition for OP[6:0]

Function	Operand	Data	Notes
Training Modes	OP[6:0]	$0XXXXXX_B$: NOP 1000001_B: RFU 1000011_B: RD DQ Calibration (MR32/MR40) 1000101_B: RFU 1000111_B: RFU 1001001_B: RFU 1001011_B: RFU 1001101_B: RFU 1001111_B: ZQCal Start 1010001_B: ZQCal Latch All Others: Reserved	1, 2

NOTE 1 See command truth table (Table 96) for more information.
NOTE 2 MPC commands for Read training operations must be immediately followed by CAS-2 command consecutively without any other commands in-between. MPC command must be issued first before issuing the CAS-2 command.

4.17 Multi-Purpose Command (MPC) (cont'd)

Table 83 — Timing Constraints for Training Commands

Previous Command	Next Command	Minimum Delay	Unit	Notes
RD/MRR	MPC [RD DQ Calibration]	tRTRRD	nCK	1
MPC [RD DQ Calibration]	RD/MRR	tRTRRD	nCK	1
	MPC [RD DQ Calibration]	tCCD	nCK	
NOTE 1 tRTRRD = RL + RU(tDQSCK(max)/tCK) + BL/2 + RD(tRPST) + max(RU(7.5ns/tCK),8nCK)				

4.19 Temperature Sensor

LPDDR4X-NVM devices optionally include a temperature sensor whose value can be read from MR4 over the LPDDR4X interface or from the TEMP_SENSE register over the SPI interface. The sensor can be used to determine whether AC timing derating is required in an elevated temperature range. Either the temperature sensor or the device tOPER may be used to determine whether operating temperature requirements are being met.

A SPI Write Any Register operation to the TEMP_SENSE Register initiates a temperature sensing operation. The LPDDR4X-NVM device then goes into the BUSY state for up to t_{TEMP}=100us while the temperature is being measured before returning to the READY state. Once the measurement has completed and the device has returned to the READY state, the measured value can be retrieved from either MR4 (LPDDR4X bus) or by performing a Read Any Register operation from the TEMP_SENSE Register (SPI bus). While the device is BUSY, during the temperature measurement period, the LPDDR4X-NVM interface is fully functional but the MR4 and TEMP_SENSE registers contain invalid data should not be accessed.

The actual temperature (in Celsius) is calculated using the measured_temperature value by applying the following equation:

Table 84 — Temperature Sensor Translation Examples

Measured_temperature	Actual_temperature
0000 0000b	below minimum temperature spec
0000 0001b	-40°C
0000 0010b	-39°C
0000 0011b	-38°C
...	...
0010 1001b	0°C
...	...
1001 0010b	+105°C
...	...
10100110b	+125°C
...	...
1011 1101b	+148°C
1011 1110b	+149°C
1011 1111b	+150°C
xxxx xxxxb - 1111 1110b	RFU
1111 1111b	above maximum temperature spec
NOTE RFUs are applied to all temperatures above the maximum temperature specified for the device.	

4.18 Temperature Sensor (cont'd)

Table 85 — Temperature Sensor Characteristics

Parameter	Max	Units
Temperature Sensor Accuracy	+/- 7.5	°C
NOTE These parameters are guaranteed by characterization.		

4.20 ZQ Calibration

The MPC command is used to initiate ZQ Calibration, which calibrates the output driver impedance across process, temperature, and voltage. ZQ Calibration occurs in the background of device operation.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start and ZQCal Latch. ZQCal Start initiates the device's calibration procedure, and ZQCal Latch captures the result and loads it into the device's drivers.

A ZQCal Start command may be issued anytime the LPDDR4X-NVM device is not in a power-down state. A ZQCal Latch Command may be issued anytime outside of power-down after tZQCAL has expired and all DQ bus operations have completed. The CA Bus must maintain a Deselect state during tZQLAT to allow CA ODT calibration settings to be updated. The following mode register fields that modify I/O parameters cannot be changed following a ZQCal Start command and before tZQCAL has expired:

- PU-Cal (Pull-up Calibration VOH Point)
- PDDS (Pull Down Drive Strength and Rx Termination)
- CA-ODT (CA ODT Value)

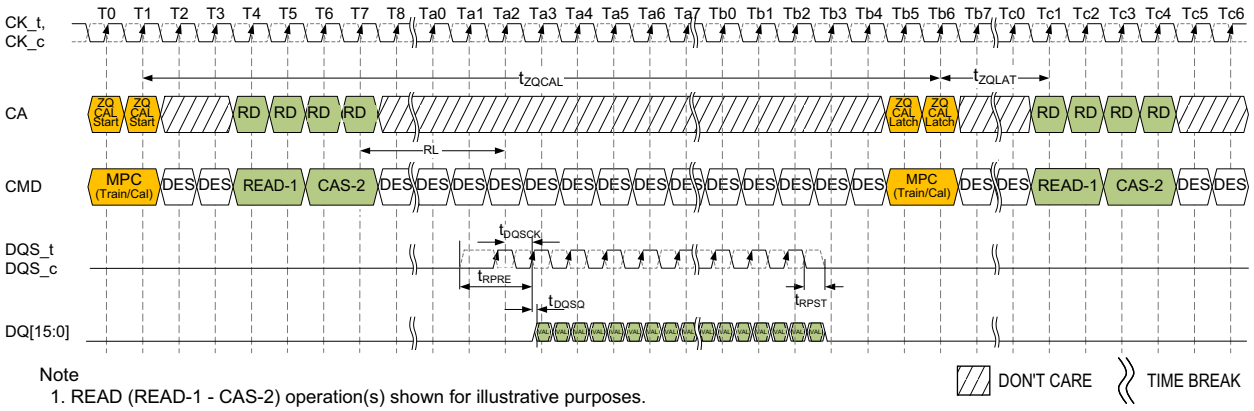
4.20.1 ZQCal Reset

The ZQCal Reset command resets the output impedance calibration to a default accuracy of +/- 30% across process, voltage, and temperature. This command is used to ensure output impedance accuracy to +/- 30% when ZQCal Start and ZQCal Latch commands are not used. See Table 86 and Figure 67.

The ZQCal Reset command is executed by writing MR10 OP[0]=1B.

Table 86 — ZQCal Timing Parameters

Parameter	Symbol	Min/Max	Value	Unit
ZQ Calibration Time	tZQCAL	MIN	1	us
ZQ Calibration Latch Time	tZQLAT	MIN	max(30ns,8nCK)	ns
ZQ Calibration Reset Time	tZQRESET	MIN	max(50ns,3nCK)	ns



Note
1. READ (READ-1 - CAS-2) operation(s) shown for illustrative purposes.
   Any single or multiple valid commands may be executed within the tZQCAL time and prior to latching the results.
2. Before the ZQ-Latch command can be executed, any prior commands utilizing the DQ bus must have completed.

Figure 67 — ZQCal Timing

4.20.2 ZQ External Resistor, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and V_{DDQ}.

If the system configuration shares the CA bus to form a x32 (or wider) channel, the ZQ pin of each die's x16 channel shall use a separate ZQCal resistor.

If the system configuration has more than one rank and if the ZQ pins of both ranks are attached to a single resistor, then the LPDDR4X-NVM controller must ensure that the ZQCal's don't overlap.

The total capacitive loading on the ZQ pin must be limited to 25 pF.

Example: If a system configuration shares a CA bus between 'n' channels to form a n * 16 wide bus, and no means are available to control the ZQCal separately for each channel (i.e., separate CS, CKE, or CK), then each x16 channel must have a separate ZQCal resistor.

Example: For a x32, two rank system, each x16 channel must have its own ZQCal resistor, but the ZQCal resistor can be shared between ranks on each x16 channel. In this configuration, the CS signal can be used to ensure that the ZQCal commands for Rank[0] and Rank[1] don't overlap.

4.21 Pull Up/Pull Down Driver Characteristics and Calibration

The characteristics and calibration are shown in Table 87 through Table 89.

Table 87 — Pull-down Driver Characteristics, with ZQ Calibration

R_{ONPD},nom	Resistor	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.9	1	1.1	RZQ/6
48 Ohm	R_{ON48PD}	0.9	1	1.1	RZQ/5
60 Ohm	R_{ON60PD}	0.9	1	1.1	RZQ/4
80 Ohm	R_{ON80PD}	0.9	1	1.1	RZQ/3
120 Ohm	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 Ohm	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

NOTE All value are after ZQ Calibration. Without ZQ Calibration R_{ONPD} values are ± 30%.

Table 88 — Pull-Up Characteristics, with ZQ Calibration

VOH_{PU},nom	VOH,nom(mV)	Min	Nom	Max	Unit
V_{DDQ} x 0.5	300	0.9	1	1.1	VOH,nom
V_{DDQ} x 0.6	360	0.9	1	1.1	VOH,nom

NOTE 1 All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%.
NOTE 2 VOH,nom (mV) values are based on a nominal V_{DDQ} = 0.6V.

Table 89 — Valid Calibration Points

VOHPU,nom	ODT Value					
	240	120	80	60	48	40
V_{DDQ} x 0.5	VALID	VALID	VALID	VALID	VALID	VALID
V_{DDQ} x 0.6	DNU	VALID	DNU	VALID	DNU	DNU

NOTE 1 Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
NOTE 2 If the VOH(nom) calibration point is changed, then re-calibration is required.
NOTE 3 DNU = Do Not Use

4.22 On Die Termination for Command/Address Bus

ODT (On-Die Termination) is a feature of the LPDDR4X-NVM device that allows the device to turn on/off termination resistance for CK_t, CK_c, CS and CA[5:0] signals.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the host controller to turn on and off termination resistance for any memory device via Mode Register setting.
A simple functional representation of the LPDDR4X-NVM device ODT feature is shown in Figure 68.

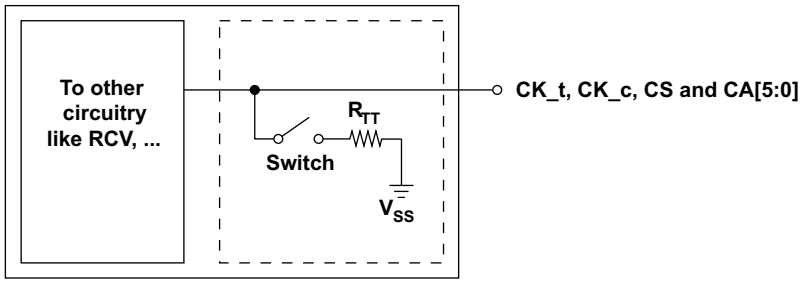


Figure 68 — Functional Representation of CA ODT

4.22.1 ODT Mode Register and ODT State Table

ODT termination values are set and enabled via MR11. The CA bus (CK_t, CK_c, CS, CA[5:0]) ODT resistance values are set by MR11 OP[6:4]. The default state for the CA is ODT disabled.

ODT is applied on the CA bus to the CK_t, CK_c, CS and CA[5:0] signals. Generally, only one termination load will be present even if multiple devices are sharing the command signals. LPDDR4X-NVM uses mode registers exclusively to enable CA termination. Before enabling CA termination via MR11, all ranks should have appropriate MR22 termination settings programmed. In multi-rank systems, the terminating rank should be trained first, followed by the nonterminating rank(s). See Table 90.

Table 90 — Command Bus ODT State

ODTE-CA MR11[6:4]	ODTD-CA MR22[5]	ODTF-CK MR22[3]	ODTF-CS MR22[4]	ODT State for CA	ODT State for CK_t/CK_c	ODT State for CS
Disabled[1]	Valid[2]	Valid[2]	Valid[2]	Off	Off	Off
Valid[2]	0	0	0	On	On	On
Valid[2]	0	0	1	On	On	Off
Valid[2]	0	1	0	On	Off	On
Valid[2]	0	1	1	On	Off	Off
Valid[2]	1	0	0	Off	On	On
Valid[2]	1	0	1	Off	On	Off
Valid[2]	1	1	0	Off	Off	On
Valid[2]	1	1	1	Off	Off	Off

NOTE 1 Default Value.
NOTE 2 "Valid" means "0 or 1".
NOTE 3 The state of CA Bus ODT does not change upon entering Power-Down Mode. This maintains termination for alternate ranks in multi-rank systems.
NOTE 4 The host should configure only one die to enable ODT_CK in the two die MCP device.

4.22.2 ODT Mode Register and ODT Characteristics

The characteristics are provided in Figure 69 and Table 91 and Table 92.

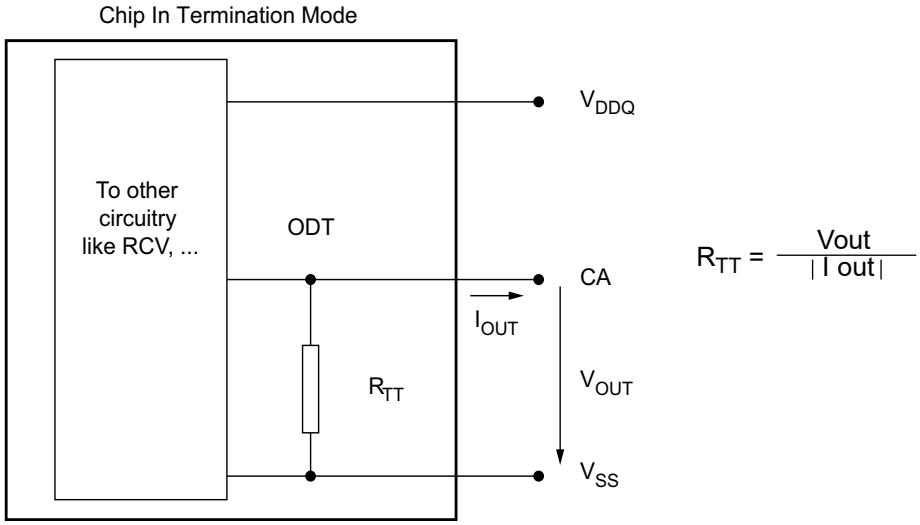


Figure 69 — On Die Termination for CA

4.22.2 ODT Mode Register and ODT Characteristics (cont'd)

Table 91 — ODT DC Electrical Characteristics

(assuming RZQ = 240 Ω +/-1% over the entire operating temperature range after a proper ZQ calibration)

MR11[6:4]	R_{TT}	Vout	Min	Nom	Max	Unit	Note
001	240 Ω	VOLdc= 0.20 * V_{DDQ}	0.8	1.0	1.1	RZQ	1,2
		VOMdc= 0.50 * V_{DDQ}	0.9	1.0	1.1	RZQ	1,2
		VOHdc= 0.75 * V_{DDQ}	0.9	1.0	1.3	RZQ	1,2
010	120 Ω	VOLdc= 0.20 * V_{DDQ}	0.8	1.0	1.1	RZQ/2	1,2
		VOMdc= 0.50 * V_{DDQ}	0.9	1.0	1.1	RZQ/2	1,2
		VOHdc= 0.75 * V_{DDQ}	0.9	1.0	1.3	RZQ/2	1,2
011	80 Ω	VOLdc= 0.20 * V_{DDQ}	0.8	1.0	1.1	RZQ/3	1,2
		VOMdc= 0.50 * V_{DDQ}	0.9	1.0	1.1	RZQ/3	1,2
		VOHdc= 0.75 * V_{DDQ}	0.9	1.0	1.3	RZQ/3	1,2
100	60 Ω	VOLdc= 0.20 * V_{DDQ}	0.8	1.0	1.1	RZQ/4	1,2
		VOMdc= 0.50 * V_{DDQ}	0.9	1.0	1.1	RZQ/4	1,2
		VOHdc= 0.75 * V_{DDQ}	0.9	1.0	1.3	RZQ/4	1,2
101	48 Ω	VOLdc= 0.20 * V_{DDQ}	0.8	1.0	1.1	RZQ/5	1,2
		VOMdc= 0.50 * V_{DDQ}	0.9	1.0	1.1	RZQ/5	1,2
		VOHdc= 0.75 * V_{DDQ}	0.9	1.0	1.3	RZQ/5	1,2
110	40 Ω	VOLdc= 0.20 * V_{DDQ}	0.8	1.0	1.1	RZQ/6	1,2
		VOMdc= 0.50 * V_{DDQ}	0.9	1.0	1.1	RZQ/6	1,2
		VOHdc= 0.75 * V_{DDQ}	0.9	1.0	1.3	RZQ/6	1,2
Mismatch CA-CA within clk group		0.50* V_{DDQ}	-		2	%	1,2,3

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Section 4.23 on voltage and temperature sensitivity.

NOTE 2 Pull-Down ODT resistors are recommended to be calibrated at 0.50*V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.75*V_{DDQ} and 0.2*V_{DDQ}.

NOTE 3 CA to CA mismatch within clock group (CA,CS) variation for a given component including CK_t and CK_c (characterized).

$$CA - CA_{Mismatch} = \frac{RODT(max) - RODT(min)}{RODT(avg)}$$

4.23 Output Driver and Termination Resistor Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 92 and Table 93.

Table 92 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	0.50 x VDDQ	90-($dR_{on}dT$ x |ΔT|)-($dR_{on}dV$ x |ΔV|)	110+($dR_{on}dT$ x |ΔT|)+($dR_{on}dV$ x |ΔV|)	%	1,2
VOH_{PU}	0.50 x VDDQ	90-(dVOHdT x |ΔT|)-(dVOHdV x |ΔV|)	110+(dVOHdT x |ΔT|)+(dVOHdV x |ΔV|)	%	1,2,5
$R_{TT(I/O)}$	0.50 x VDDQ	90-($dR_{on}dT$ x |ΔT|)-($dR_{on}dV$ x |ΔV|)	110+($dR_{on}dT$ x |ΔT|)+($dR_{on}dV$ x |ΔV|)	%	1,2,3
$R_{TT(In)}$	0.50 x VDDQ	90-($dR_{on}dT$ x |ΔT|)-($dR_{on}dV$ x |ΔV|)	110+($dR_{on}dT$ x |ΔT|)+($dR_{on}dV$ x |ΔV|)	%	1,2,4

NOTE 1 ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration).
NOTE 2 $dR_{ON}dT$, $dR_{ON}dV$, dVOHdT, dVOHdV, $dR_{TT}dV$, and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.
NOTE 3 This parameter applies to Input/Output pin such as DQS, DQ and ECCO.
NOTE 4 This parameter applies to Input pins such as CK, CA and CS.
NOTE 5 Refer to 4.21 Pull Up/Pull Down Driver Characteristics for VOH_{PU}.

Table 93 — Output Driver and Termination Resistor Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	%/°C
$dR_{ON}dV$	R_{ON} Voltage Sensitivity	0.00	0.20	%/mV
dVOHdT	VOH Temperature Sensitivity	0.00	0.75	%/°C
dVOHdV	VOH Voltage Sensitivity	0.00	0.35	%/mV
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	%/°C
$dR_{TT}dV$	R_{TT} Voltage Sensitivity	0.00	0.20	%/mV

4.23.1 ODT for Command/Address Update Time

ODT for Command/Address update time after Mode Register set are shown in Figure 70 and Table 94.

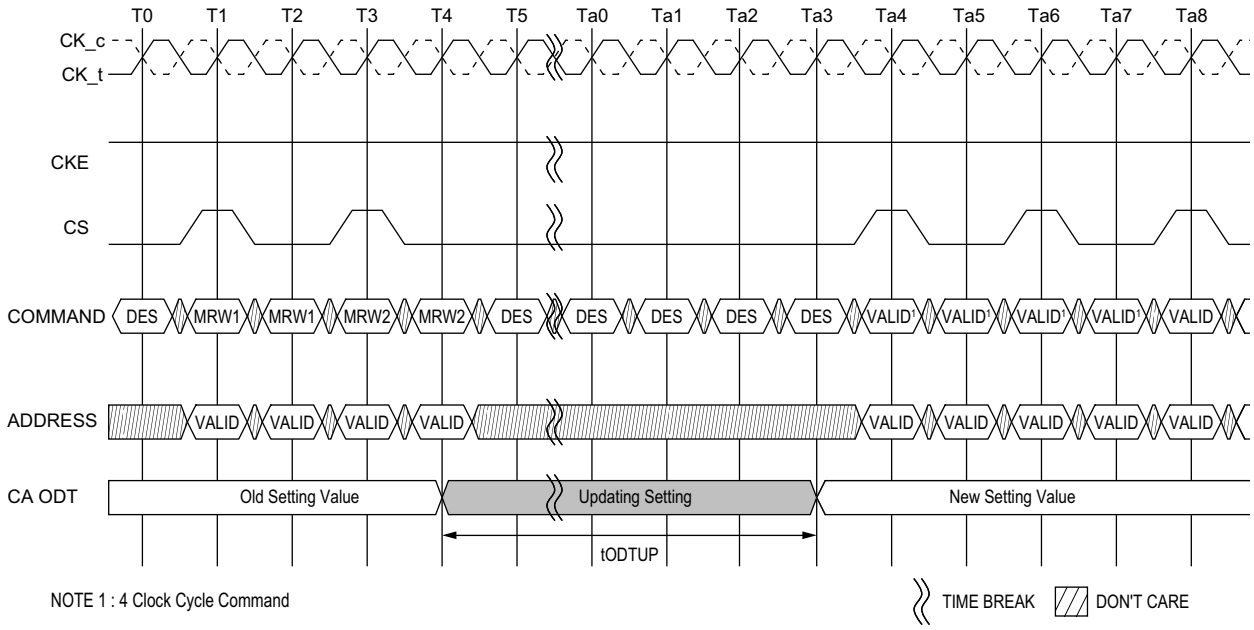


Figure 70 — ODT for Command/Address Setting Update Timing in 4 Clock Cycle Command

Table 94 — ODT CA AC Timing

Speed		LPDDR4-1600/1866/2133/2400/3200/4266		Units	NOTE
Parameter	Symbol	MIN	MAX		
ODT CA Value Update Time	tODTUP	RU(20ns/tCK(avg))	-		

4.24 LPDDR4X-NVM Interface Power-Down Mode

4.24.1 Power-Down Entry and Exit

(Reference Figure 71 through Figure 77 and Table 95.)

Power-down is asynchronously entered when CKE is driven LOW. Only the LPDDR4X interface is powered down when CKE goes LOW. CKE must not go LOW while the following operations are in progress:

- Mode Register Read
- Mode Register Write
- Read
- V_{REF}CA Range and Value setting via MRW
- Command Bus Training mode Entering/Exiting via MRW
- VRCG High Current mode Entering/Exiting via MRW

CKE can go LOW while any other operations are in progress. The power-down IDD specification will not be applied until such operations are complete. Power-down entry and exit are shown in Figure 71.

Entering power-down deactivates the input and output buffers, excluding CKE and LP4RST_n. To ensure that there is enough time to account for internal delay on the CKE signal path, CS input is required stable Low level and CA input level is don’t care after CKE is driven LOW, this timing period is defined as tCKELCS. Clock input is required after CKE is driven LOW, this timing period is defined as tCKELCK. CKE LOW will result in deactivation of all input receivers except LP4RST_n after tCKELCK has expired. In power-down mode, CKE must be held LOW; all other input signals except LP4RST_n are "Don't Care". CKE LOW must be maintained until tCKE,min is satisfied.

The power-down state is asynchronously exited when CKE is driven HIGH. CKE HIGH must be maintained until tCKE,min is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH.

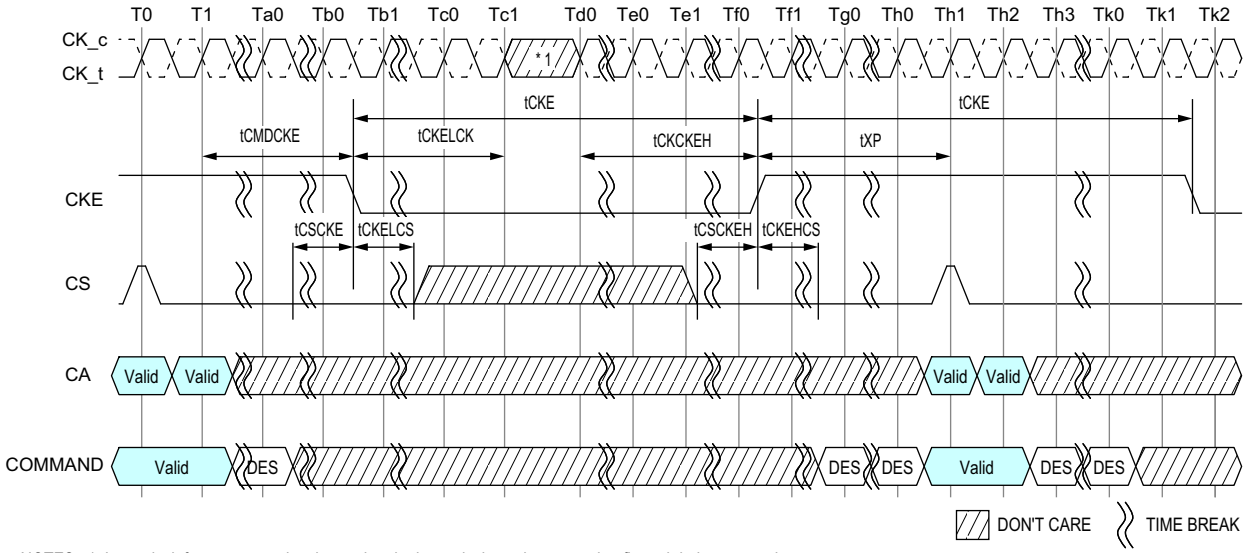
Clock frequency change or Clock Stop is inhibited during tCMDCKE, tCKELCK, tCKCKEH, tXP, tMRWCKEL and tZQCKE periods.

If power-down occurs when all banks are idle, this mode is referred to as idle power-down. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

VDDQ may be turned off during power-down after tCKELCK is satisfied (Refer to Figure 71 about tCKELCK). Prior to exiting power-down, VDDQ must be within its minimum/maximum operating range.

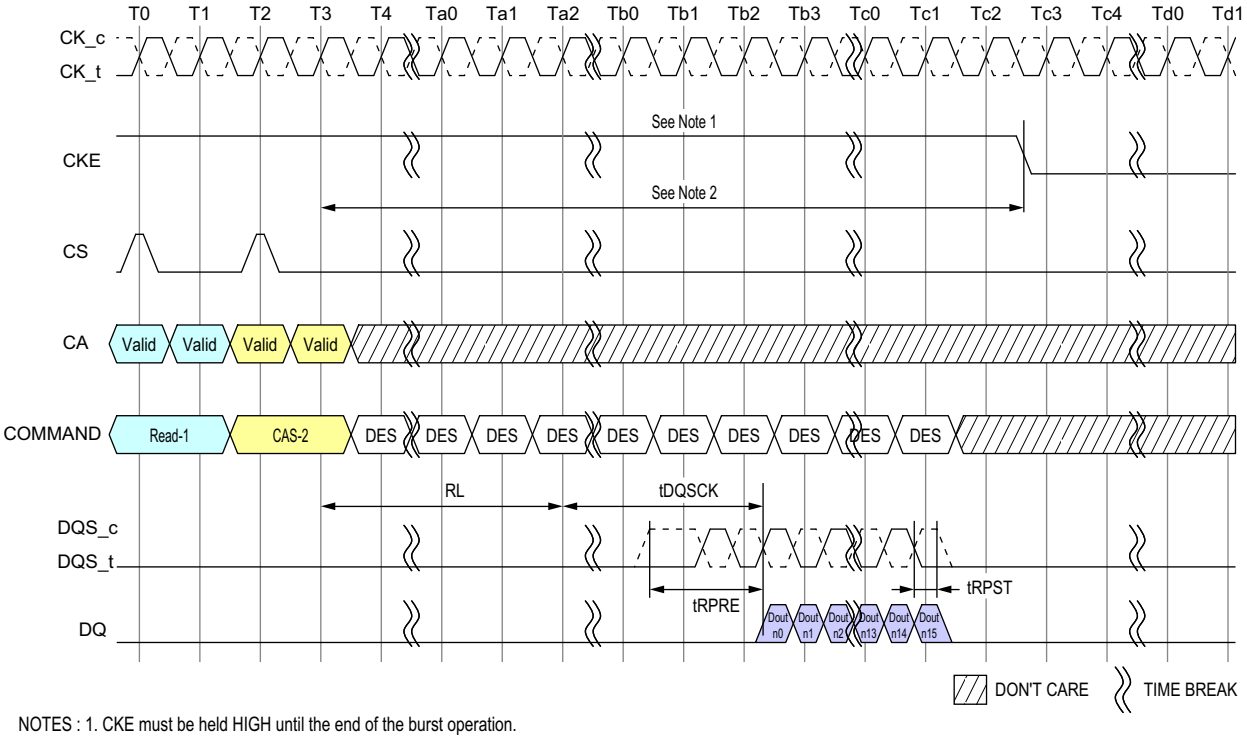
When CA, CK and/or CS ODT is enabled via MR11 OP[6:4] and also via MR22 settings, the rank providing ODT will continue to terminate the command bus in all device states including power-down when VDDQ is stable and within its minimum/maximum operating range.

4.24.1 Power-Down Entry and Exit (cont'd)



NOTES : 1. Input clock frequency can be changed or the input clock can be stopped or floated during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of tCKCKEH of stable clock prior to power-down exit and the clock frequency is between the minimum and maximum specified frequency for the speed grade in use.

Figure 71 — Basic Power-Down Entry and Exit Timing



NOTES : 1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Read Command to falling edge of CKE signal is as follows.
Read Post-amble = 0.5nCK : MR1 OP[7]=[0] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 1tCK
Read Post-amble = 1.5nCK : MR1 OP[7]=[1] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 2tCK

Figure 72 — Read to Power-Down Entry

4.24.1 Power-Down Entry and Exit (cont'd)

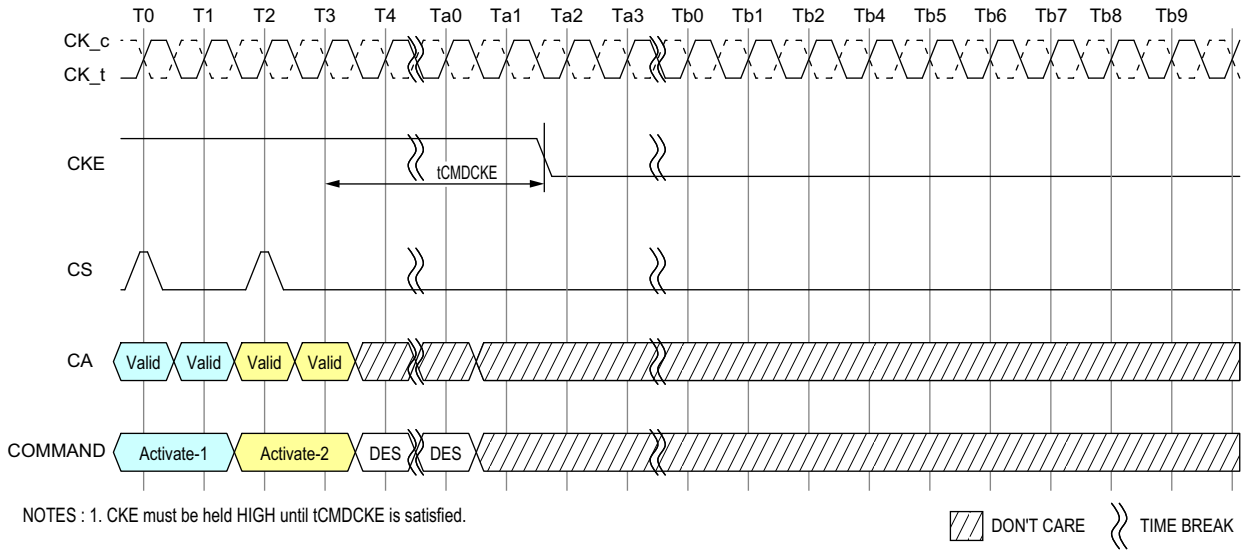
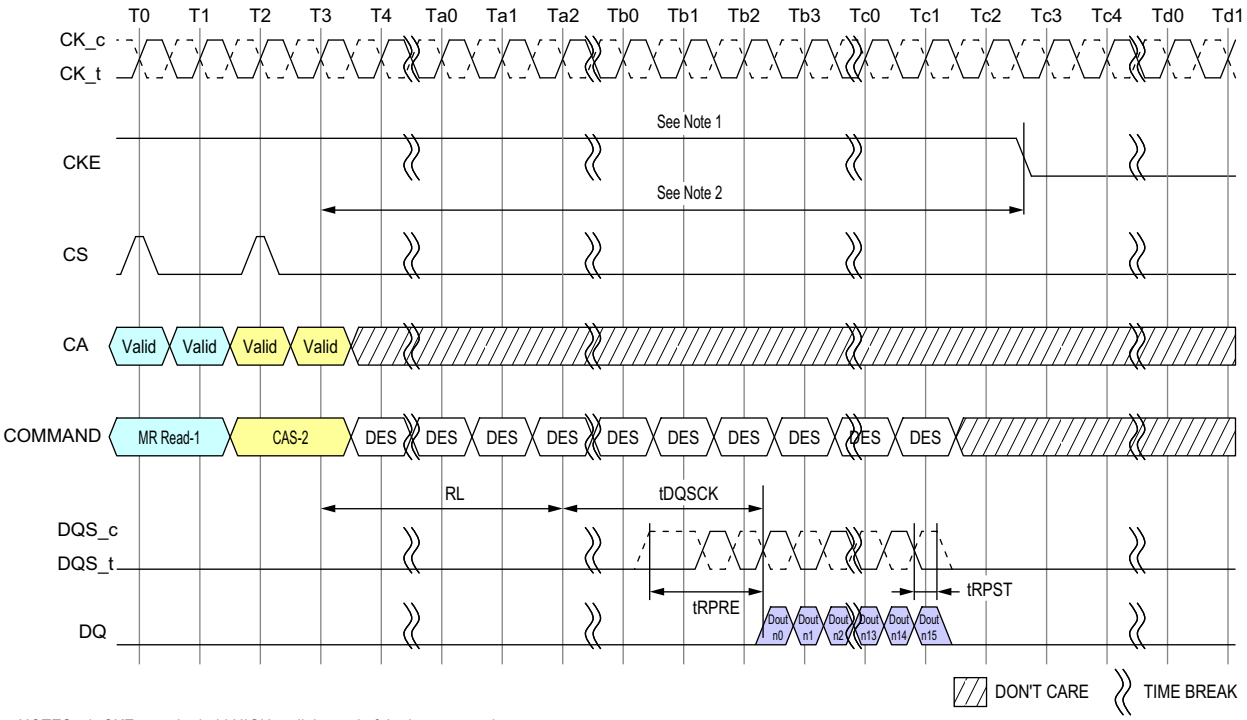


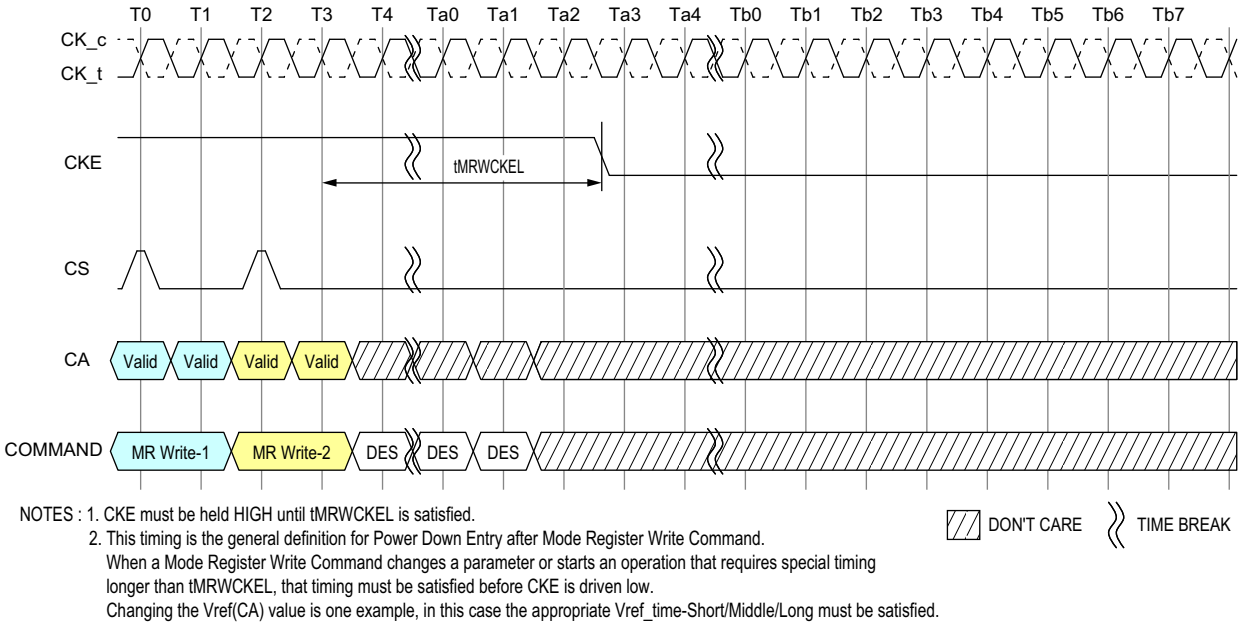
Figure 73 — Activate Command to Power-Down Entry



NOTES : 1. CKE must be held HIGH until the end of the burst operation.
2. Minimum Delay time from Mode Register Read Command to falling edge of CKE signal is as follows:
Read Post-amble = 0.5nCK : MR1 OP[7]=[0] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 1tCK
Read Post-amble = 1.5nCK : MR1 OP[7]=[1] : (RL x tCK) + tDQSCK(Max) + ((BL/2) x tCK) + 2tCK

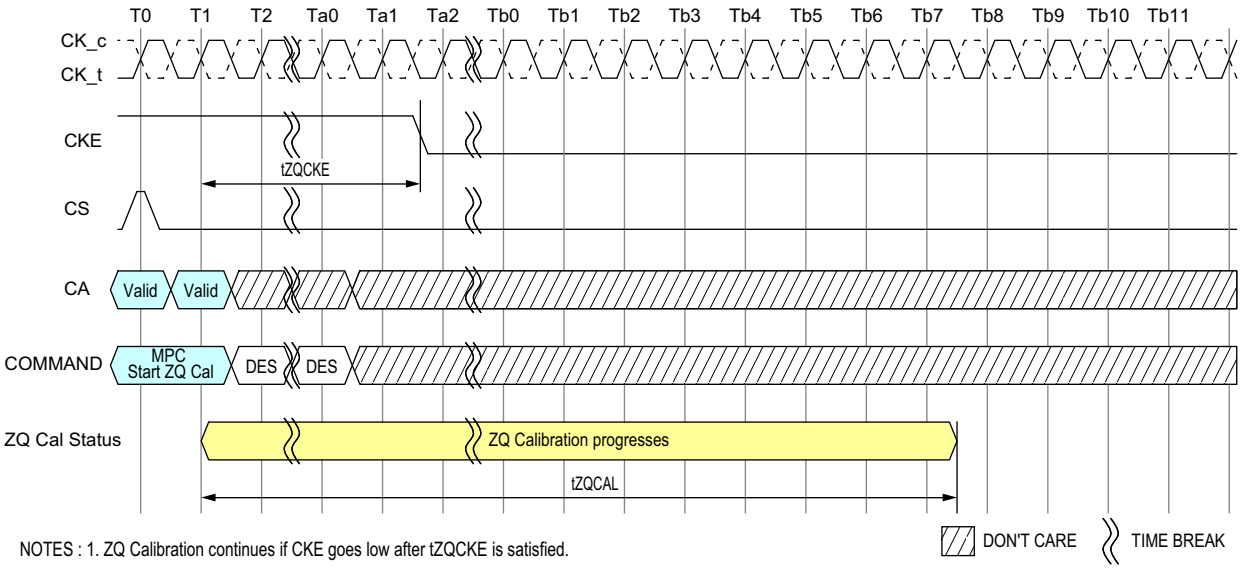
Figure 74 — Mode Register Read to Power-Down Entry

4.24.1 Power-Down Entry and Exit (cont'd)



NOTES : 1. CKE must be held HIGH until tMRWCKEL is satisfied.
2. This timing is the general definition for Power Down Entry after Mode Register Write Command.
When a Mode Register Write Command changes a parameter or starts an operation that requires special timing longer than tMRWCKEL, that timing must be satisfied before CKE is driven low.
Changing the Vref(CA) value is one example, in this case the appropriate Vref_time-Short/Middle/Long must be satisfied.

Figure 75 — Mode Register Write to Power-Down Entry



NOTES : 1. ZQ Calibration continues if CKE goes low after tZQCKE is satisfied.

Figure 76 — Multi-Purpose Command for Start ZQ Calibration to Power-Down Entry

4.24.1 Power-Down Entry and Exit (cont'd)

Table 95 — Power-Down AC Timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Note
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	Max(7.5ns, 4nCK)	-	
Delay from valid command to CKE input LOW	tCMDCKE	Min	Max(1.75ns, 3nCK)	ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns	
Valid CS Requirement after CKE Input low	tCKELCS	Min	Max(5ns, 5nCK)	ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)	ns	1
Exit power- down to next valid command delay	tXP	Min	Max(7.5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns, 5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	Min	Max(14ns, 10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	Min	Max(1.75ns, 3nCK)	ns	1

NOTE 1 Delay time has to satisfy both analog time(ns) and clock count(nCK).
For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown In Figure 77.

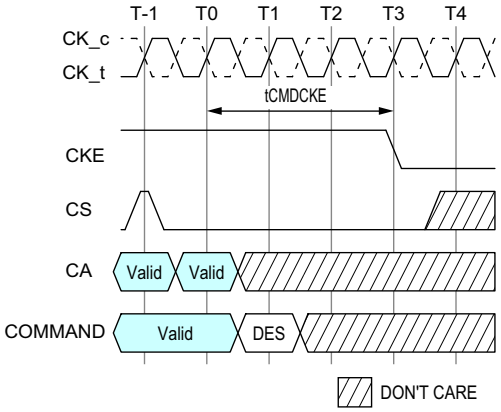


Figure 77 — tCMDCKE Timing

4.25 Input Clock Stop and Frequency Change

LPDDR4X-NVM devices support input clock frequency change during CKE LOW under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Any Activate or NVR commands have executed to completion prior to changing the frequency;
- The related timing conditions (tRCD) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of tCKELCK after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of tCKCKEH prior to CKE going HIGH

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4X-NVM devices support clock stop during CKE LOW under the following conditions:

- CK_t and CK_c are don't care during clock stop;
- Any Activate or NVR command has executed to completion prior to stopping the clock;
- The related timing conditions (tRCD) have been met prior to stopping the clock;
- The initial clock frequency shall be maintained for a minimum of tCKELCK after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of tCKCKEH prior to CKE going HIGH

The LPDDR4X-NVM interface supports input clock frequency change during CKE HIGH under the following conditions:

- tCK(abs)min is met for each clock cycle;
- Any Activate, Read, NVR, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
- The related timing conditions (tRCD, tMRW, tMRR, etc.) have been met prior to changing the frequency;
- CS shall be held LOW during clock frequency change;
- The LPDDR4X-NVM device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK+tXP.

After the input clock frequency is changed, additional MRW commands may be required to set the RL, etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR4X-NVM devices support clock stop during CKE HIGH under the following conditions:

- CK_t is held LOW and CK_c is held HIGH during clock stop;
- CS shall be held LOW during clock stop;
- Any Activate, Read, NVR, MPC, Mode Register Write or Mode Register Read commands must have executed to completion, including any associated data bursts and extra 4 clock cycles must be provided prior to stopping the clock;
- The related timing conditions (tRCD, tMRW, tMRR, tZQLAT, etc.) have been met prior to stopping the clock;
- MPC(Zqcal Start) commands are required to have 4 additional clocks prior to stopping the clock (same as CKE=L case).
- The LPDDR4X-NVM device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2*tCK+tXP.

4.26 LPDDR4X Command Truth Table

LPDDR4X interface operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4X interface must be reset (see Section 3.3.3) or the device power-cycled (see Section 3.3.1) and then restarted through the specified initialization sequence before normal operation can continue.

CKE signal has to be held High when the commands listed in the command truth table are input.

4.26.1 Command Truth Table

Table 96 presents the Command Truth Table.

Table 96 — LPDDR4X Command Truth Table

	SDR Command Pins	SDR CA Pins (6)							
LPDDR4X-NVM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,5
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
CAS-2 (MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,4
	L	C2	C3	C4	C5	C6	C7	R2	
Mode Register Write-1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,7
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,7
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,5,8
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Modified READ									
Pre-Activate (PRE)	H	H	H	L	H	R19	R20	R1	1,3,6,13, 16
	L	BA0	BA1	BA2	R21	R22	R23	R2	
Modified Activate -1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,3,6,13
	L	BA0	BA1	BA2	R16	R10	R11	R2	
Modified Activate -2 (ACT-2)	H	R17	R18	R6	R7	R8	R9	R1	1,6,9,13
	L	R0	R1	R2	R3	R4	R5	R2	
Modified Read -1 (RD-1)	H	L	H	L	L	L	V	R1	1,2,5,13
	L	BA0	BA1	BA2	V	V	V	R2	
Modified CAS-2 (Read-2)	H	L	H	L	L	H	V	R1	1,4,13, 14
	L	C2	C3	C4/V	V	V	V	R2	
Legacy READ									
Legacy Activate -1 (ACT-1)	H	H	L	R18/R17	R19/R18	R20/R19	R21/R20	R1	1,3,6,13
	L	BA0	BA1	BA2	R22/R21	R16/R15	R17/R16	R2	
Legacy Activate -2 (ACT-2)	H	R23/R22	V	R12/R11	R13/R12	R14/R13	R15/R14	R1	1,6,9,13
	L	R6/R5	R7/R6	R8/R7	R9/R8	R10/R9	R11/R10	R2	
Legacy Read -1 (RD-1)	H	L	H	L	L	L	V	R1	1,2,5,13
	L	BA0	BA1	BA2	V	R5/R4	V	R2	
Legacy CAS-2 (Read-2)	H	L	H	L	L	H	R4/R3	R1	1,4,13, 14,15
	L	C2	C3	R0/C4	R1/R0	R2/R1	R3/R2	R2	
Non-Volatile READ									
Nonvolatile Read-1	H	H	R16	R17	R18	R19	R20	R1	1,13
	L	R10	R11	R12	R13	R14	R15	R2	
Nonvolatile Read-2	H	R22	R5	R6	R7	R8	R9	R1	1,10,13
	L	R21	R0	R1	R2	R3	R4	R2	

Table 96 — LPDDR4X Command Truth Table (cont'd)

	SDR Command Pins	SDR CA Pins (6)							
LPDDR4X-NVM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
RFU	H	L	***All Unused Combinations***				V	R1	11,12
	L	V						R2	

NOTE 1 All LPDDR4X-NVM commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.

NOTE 2 "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.

NOTE 3 Bank addresses BA[2:0] determine which bank is to be operated upon.

NOTE 4 For CAS-2 commands (MRR-2 or MPC (Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero.

NOTE 5 Read-1, Mode Register Read-1 or MPC (Only Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Read-1 or Mode Register Read-1 or MPC (Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.

NOTE 6 Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.

NOTE 7 MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.

NOTE 8 MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

NOTE 9 For device densities not requiring A27 and A28, A27 and A28 must both be driven High for every ACT-2 command to maintain backward compatibility. For device densities not requiring A28, A28 must be driven High for every ACT-2 command to maintain backward compatibility.

NOTE 10 NVR1 must be immediately followed by the NVR2 command consecutively without any other commands in between.

NOTE 11 RFU Commands shall not be issued by the host controller.

NOTE 12 All Commands not described shall be ignored by the memory device.

NOTE 13 LPDDR4X-NVM devices optionally support four different READ transactions. The Legacy JEDEC READ (ACT1 - ACT2 - RD1 - CAS2), the NVR READ (NVR1 - NVR2), the Modified JEDEC READ (ACT1-ACT2-RD1-CAS2) and the Modified JEDEC READ using PRE-ACTIVATE (PRE-ACT1-ACT2-RD1-CAS2). It is expected that devices will only support one of the READ transactions.

NOTE 14 The C4 column bit is required in devices that support BL32 (64 byte row).

NOTE 15 For the Legacy READ commands, the addressing supports both BL16 and BL32. Most of the table row and column entries are shown as "x / y" where x (left of "/") represents the address in BL16 mode and y (right of "/") represents the address in BL32 mode.

NOTE 16 The optional Pre-Activate command (PRE) adds five upper order ROW bits to the target address. The five additional ROW bits supports up to 32Gb of device density. The 32Gb maximum density is due to the addressing limitations on the SPI port.

5 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device.

This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 97 — Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS} (V_{DD1}=3.0 V)	V_{DD1}	-0.4	4.0	V	1
V_{DD1} supply voltage relative to V_{SS} (V_{DD1}=1.8 V)	V_{DD1}	-0.4	2.4	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.4	V	1
V_{DDQ} supply voltage relative to V_{SS}	V_{DDQ}	-0.4	1.4	V	1
V_{DDQ_SPI} supply voltage relative to V_{SS} (V_{DDQ_SPI} =1.8 V)	V_{DDQ_SPI}	-0.4	2.4	V	1
V_{DDQ_SPI} supply voltage relative to V_{SS} (V_{DDQ_SPI} =1.2 V)	V_{DDQ_SPI}	-0.4	1.6	V	1
Voltage on LPDDR interface balls relative to V_{SS}	VIN, VOUT	-0.4	1.4	V	
Voltage on non-LPDDR interface balls relative to V_{SS} (V_{DD1}=1.8 V)	VIN, VOUT	-0.4	2.4	V	
Voltage on non-LPDDR interface balls relative to V_{SS} (V_{DD1}=3.0 V)	VIN, VOUT	-0.4	4.0	V	
Storage Temperature	TSTG	-55	125	°C	2

NOTE 1 See "Power-Ramp" in Section 3.3, for relationships between power supplies.

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the LPDDR4X-NVM device. For the measurement conditions, please refer to JESD51-2.

6 AC and DC Operating Conditions

The operating conditions are provided in Table 98 through Table 101.

6.1 Recommended DC Operating Conditions

Table 98 — Recommended DC Operating Conditions

LPDDR4X-NVM	Symbol	Min	Typ	Max	Unit	Notes
Core 1 Power (Option 1)	V_{DD1}	2.70	3.00	3.60	V	1,2,5
Core 1 Power (Option 2)	V_{DD1}	1.70	1.80	1.95	V	1,2,5
Core 2 Power/Input Buffer Power	V_{DD2}	1.06	1.10	1.17	V	1,2,3
LPDDR4X I/O Buffer Power	V_{DDQ}	0.57	0.60	0.65	V	2,3,4
SPI I/O Buffer Power (Option 1)	V_{DDQ_SPI}	1.70	1.80	1.95	V	2,3,6
SPI I/O Buffer Power (Option 2)	V_{DDQ_SPI}	1.14	1.20	1.30	V	2,3,7
SPI I/O Buffer Power (Option 3)	V_{DDQ_SPI}	1.06	1.10	1.17	V	2,3,8

NOTE 1 V_{DD1} uses significantly less current than V_{DD2}.
NOTE 2 The voltage range is for DC voltage only. DC is defined as the voltage supplied at the device and is inclusive of all noise up to 20 MHz at the device package ball.
NOTE 3 VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20 MHz.
NOTE 4 Pull up, pull down and ZQ calibration tolerance spec is valid only in normal V_{DDQ} tolerance range (0.57 V - 0.65 V).
NOTE 5 LPDDR4X-NVM device will operate with a VDD1 of either 3.0V or 1.8V (device/manufacturer ordering option)
NOTE 6 Specification from JESD8-31.
NOTE 7 Specification from JESD8-26.
NOTE 8 VDDQ_SPI=1.1V aligns with the VDD2 (Core 2) supply levels.

6.2 Input Leakage Current

Table 99 — Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-4	4	µA	1,2,3

NOTE 1 For CK_t, CK_c, CKE, CS, CA, LP4RST_n. Any input $0V \le V_{IN} \le V_{DDQ}$ (All other pins not under test = 0 V).
NOTE 2 For DEVRST_n, SPI_CK and SPI_CS_n. Any input $0V \le V_{IN} \le V_{DDQ\_SPI}$ (All other pins not under test = 0 V).
NOTE 3 CA ODT is disabled for CK_t, CK_c, CS, and CA.

6.3 Input/Output Leakage Current

Table 100 — Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output Leakage Current	I_{OZ}	-5	5	µA	1,2,3

NOTE 1 For DQ, DQS_t, DQS_c, ECCO. Any I/O $0V \le V_{OUT} \le V_{DDQ}$.
NOTE 2 For SPI-DQ and INT_n. Any I/O $0V \le V_{OUT} \le V_{DDQ\_SPI}$.
NOTE 3 I/Os status are disabled: High Impedance and ODT Off.

6.4 Operating Temperature Range

Table 101 — Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-40	85	C°
Elevated		-40	105	C°
Others		See Manufacturer Data Sheet		C°

NOTE 1 Operating Temperature is the case surface temperature on the center-top side of the LPDDR4X-NVM device. For the measurement conditions, please refer to JESD51-2.

NOTE 2 Some applications require operation of LPDDR4X-NVM across wide temperature ranges. For LPDDR4X-NVM devices, derating may be necessary to operate across wide temperature ranges.

NOTE 3 Either the device case temperature rating or the temperature sensor (see Section 4.19) may be used to determine the need for AC timing derating and/or monitor the operating temperature.

7 AC and DC Input/Output Measurement Levels

7.1 1.1V High-Speed LVCMOS (HS_LVCMOS, LPDDR4 Related Signals)

This section covers voltage levels for: CKE and LP4RST_n. All voltages are referenced to ground except where noted.

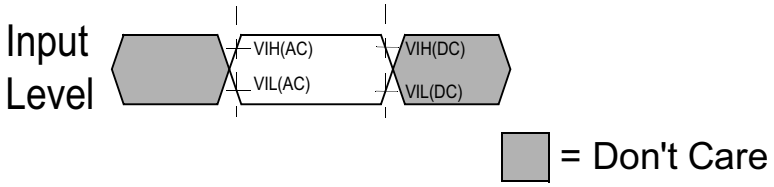
7.1.1 Levels for VDD2=1.1V

7.1.1.1 Input Level for CKE

This definition applies to CKE. Table 102 provides the input level; Figure 78 shows the timing.

Table 102 — LPDDR4X-NVM Input Level for CKE

Parameter	Symbol	Min	Max	Unit	Note
Input high level (AC)	VIH(AC)	$0.75*V_{DD2}$	$V_{DD2}+0.2$	V	1
Input low level (AC)	VIL(AC)	-0.2	$0.25*V_{DD2}$	V	1
Input high level (DC)	VIH(DC)	$0.65*V_{DD2}$	$V_{DD2}+0.2$	V	
Input low level (DC)	VIL(DC)	-0.2	$0.35*V_{DD2}$	V	
NOTE 1 Refer to LPDDR4X-NVM AC Over/Undershoot section.					



Note
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

Figure 78 — LPDDR4X-NVM Input AC Timing Definition for CKE

7.1.1.2 Input Level for LP4RST_n

This definition applies to LP4RST_n. Table 103 provides the input level; Figure 79 shows the timing.

Table 103 — LPDDR4X-NVM Input Level for LP4RST_n

Parameter	Symbol	Min	Max	Unit	Note
Input high level	VIH	$0.80*V_{DD2}$	$V_{DD2}+0.2$	V	1
Input low level	VIL	-0.2	$0.20*V_{DD2}$	V	1
NOTE 1 Refer to LPDDR4X-NVM AC Over/Undershoot section.					

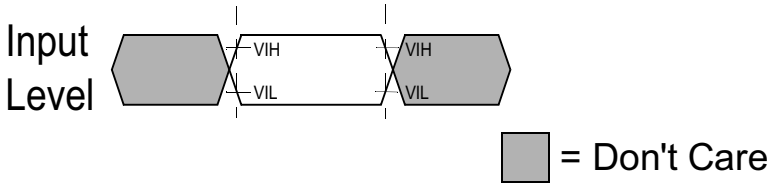


Figure 79 — Input AC Timing Definition for LP4RST_n

7.1.2 AC Over/Undershoot

Table 104 provides the specifications; Figure 80 shows the LPDDR4X address and control pins.

Table 104 — LPDDR4X-NVM AC Over/Undershoot

Parameter	Specification
Maximum peak Amplitude allowed for overshoot area	0.35 V
Maximum peak Amplitude allowed for undershoot area	0.35 V
Maximum overshoot area above V_{DD}/V_{DDQ}	0.8 V-ns
Maximum undershoot area below V_{SS}/V_{SSQ}	0.8 V-ns

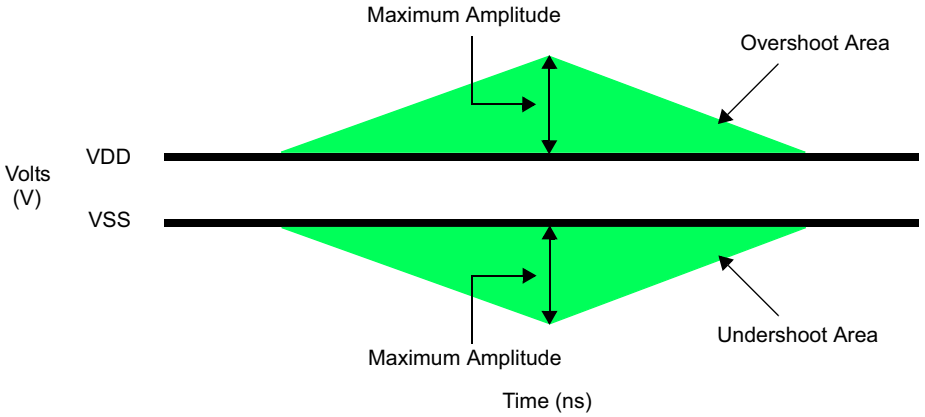


Figure 80 — AC Overshoot and Undershoot Definition for Address and Control Pins

7.2 1.2V and 1.8V High-Speed LVCMOS (HS_LVCMOS, SPI, and Related Signals)

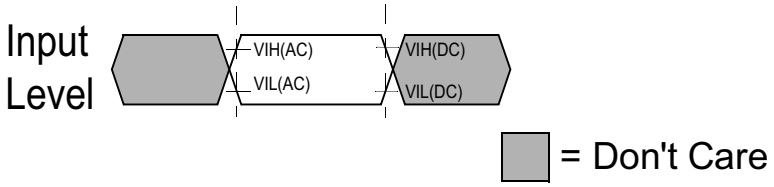
This section covers voltage levels for: SPI_CS_n, SPI_CK, SPI_DQ[3:0], INT_n, DEVRST_n and DIE_NUM. All voltages are referenced to ground except where noted.

7.2.1 Levels for VDDQ_SPI=1.8V (from JESD8-31)

7.2.1.1 Input Levels for VDDQ_SPI=1.8V

Table 105 — Input Levels (VDDQ_SPI = 1.8V)

Parameter	Symbol	Min	Max	Unit
Input HIGH Level (AC)	$V_{IH(AC)}$	0.8 * VDDQ_SPI	VDDQ_SPI + 0.3	V
Input LOW Level (AC)	$V_{IL(AC)}$	-0.3	0.20 * VDDQ_SPI	V
Input HIGH Level (DC)	$V_{IH(DC)}$	0.7 * VDDQ_SPI	VDDQ_SPI + 0.3	V
Input LOW Level (DC)	$V_{IL(DC)}$	-0.3	0.30 * VDDQ_SPI	V



Note
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

Figure 81 — VDDQ_SPI = 1.8V Input AC/DC Timing Definition

7.2.1.2 Output Levels for VDDQ_SPI=1.8V

Table 106 — Output Levels (VDDQ_SPI = 1.8V)

Parameter	Symbol	Min	Max	Unit
Output HIGH Voltage	$V_{IH(AC)}$	0.75 * VDDQ_SPI	-	V
Output LOW Voltage	$V_{IL(AC)}$	-	0.25 * VDDQ_SPI	V

7.2.1.3 AC Input Overshoot and Undershoot for VDDQ_SPI=1.8V

Table 107 — AC Input Overshoot/Undershoot (VDDQ_SPI = 1.8V)

Parameter	Specification	Unit
Maximum peak amplitude allowed for overshoot area (above VDDQ_SPI)	0.30 * VDDQ_SPI	V
Maximum peak amplitude allowed for undershoot area (below VSS)	0.30 * VDDQ_SPI	V
Maximum overshoot area above VDDQ_SPI	1.2	V * ns
Maximum undershoot area below VSS	1.2	V * ns

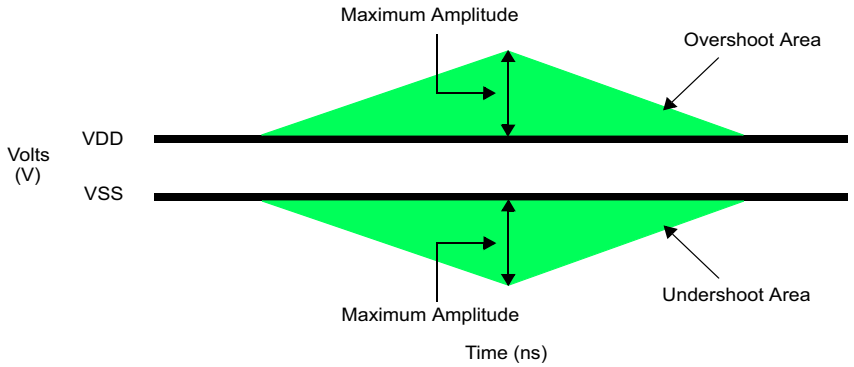


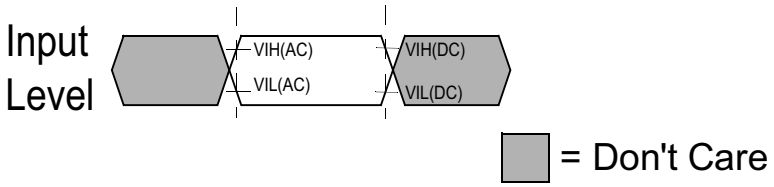
Figure 82 — AC Overshoot and Undershoot Definition for SPI Input Pins (VDDQ_SPI=1.8V)

7.2.2 Levels for VDDQ_SPI=1.2V (from JESD8-26)

7.2.2.1 Input Levels for VDDQ_SPI=1.2V

Table 108 — Input Levels (VDDQ_SPI = 1.8V)

Parameter	Symbol	Min	Max	Unit
Input HIGH Level (AC)	$V_{IH(AC)}$	0.8 * VDDQ_SPI	VDDQ_SPI + 0.2	V
Input LOW Level (AC)	$V_{IL(AC)}$	-0.2	0.20 * VDDQ_SPI	V
Input HIGH Level (DC)	$V_{IH(DC)}$	0.7 * VDDQ_SPI	VDDQ_SPI + 0.2	V
Input LOW Level (DC)	$V_{IL(DC)}$	-0.2	0.30 * VDDQ_SPI	V



Note
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

Figure 83 — VDDQ_SPI = 1.2V Input AC/DC Timing Definition

7.2.2.2 Output Levels for VDDQ_SPI=1.2V

Table 109 — Output Levels (VDDQ_SPI = 1.2V)

Parameter	Symbol	Min	Max	Unit
Output HIGH Voltage	$V_{IH(AC)}$	0.80 * VDDQ_SPI	-	V
Output LOW Voltage	$V_{IL(AC)}$	-	0.20 * VDDQ_SPI	V

7.2.2.3 AC Input Overshoot and Undershoot for VDDQ_SPI=1.2V

Table 110 — AC Input Overshoot/Undershoot (VDDQ_SPI = 1.2V)

Parameter	Specification	Unit
Maximum peak amplitude allowed for overshoot area (above VDDQ_SPI)	0.35	V
Maximum peak amplitude allowed for undershoot area (below VSS)	0.35	V
Maximum overshoot area above VDDQ_SPI	0.8	V * ns
Maximum undershoot area below VSS	0.8	V * ns

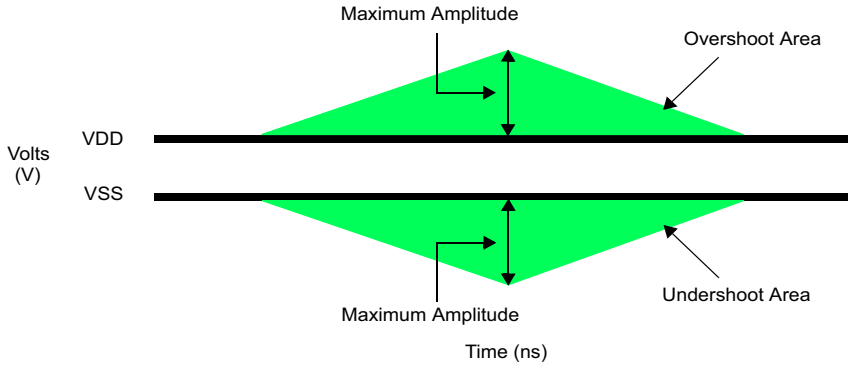


Figure 84 — AC Overshoot and Undershoot Definition for SPI Input Pins (VDDQ_SPI=1.2V)

7.3 Differential Input Voltage

7.3.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0 V.

Figure 85 and Table 111 show the input voltage.

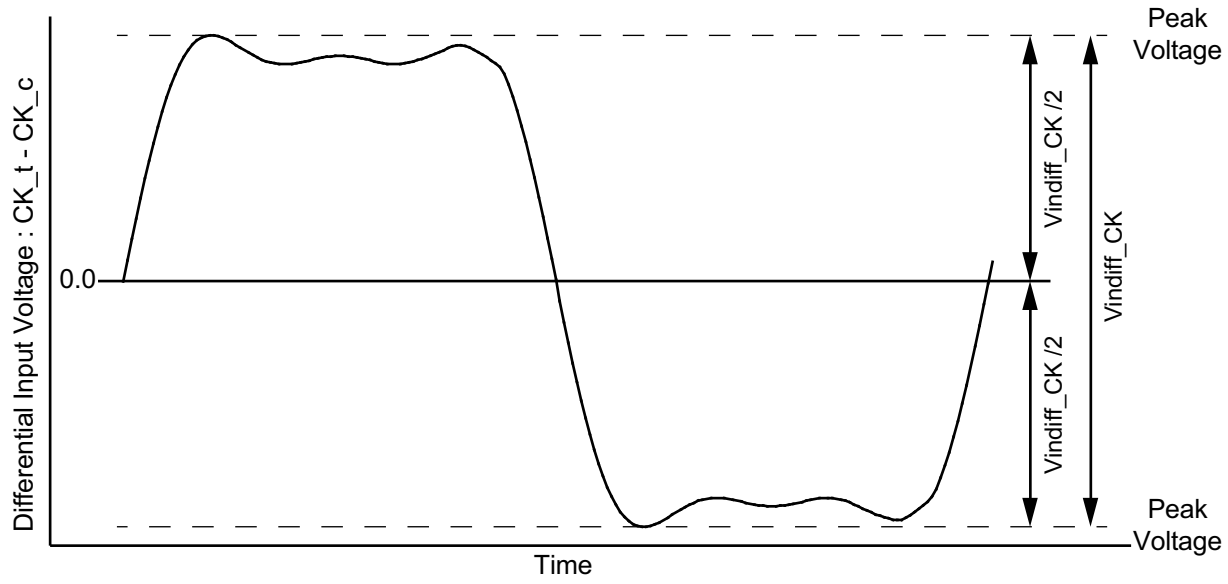


Figure 85 — CK Differential Input Voltage

Table 111 — CK Differential Input Voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
CK differential input	Vindiff_CK	420	-	380	-	360	-	mV	1, 2

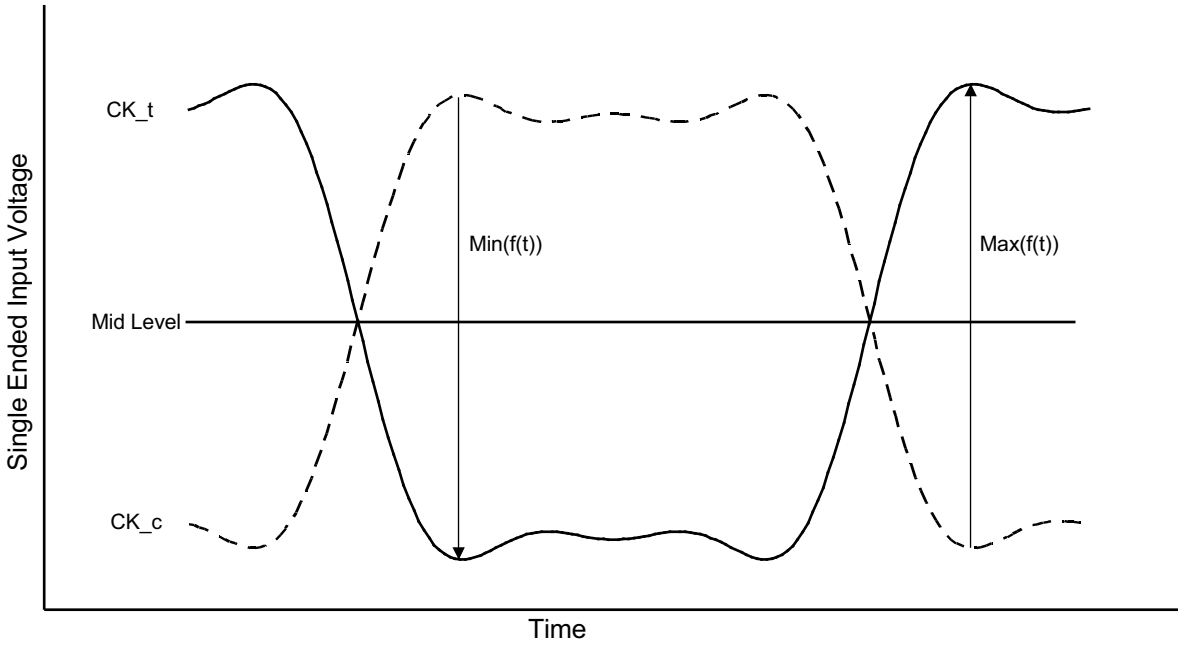
NOTE 1 These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1866.

NOTE 2 The peak voltage of Differential CK signals is calculated in a following equation.
Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

7.3.2 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals are calculated in the following equation (see Figure 86).

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

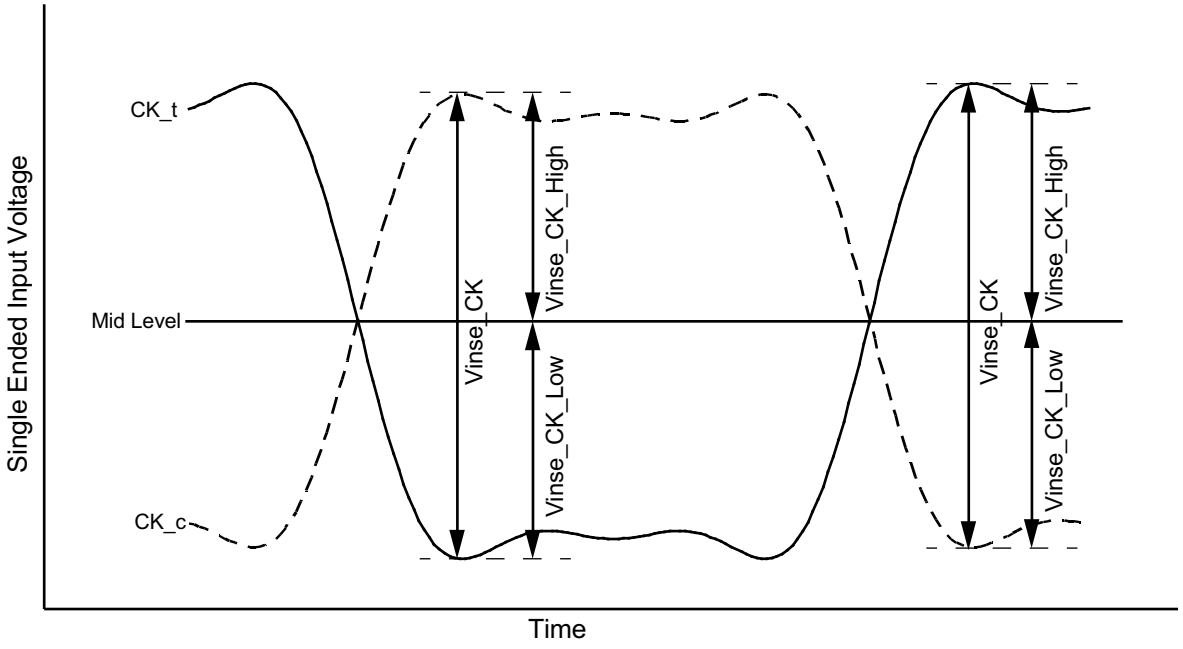


NOTES : 1. $V_{REF}CA$ is LPDDR4X-NVM internal setting value by V_{REF} Training.

Figure 86 — Definition of Differential Clock Peak Voltage

7.3.3 Single-Ended Input Voltage for Clock

The minimum input voltage needs to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver. (See Figure 87 and Table 112.)



NOTES : 1. $V_{REF}CA$ is LPDDR4X-NVM internal setting value by V_{REF} Training.

Figure 87 — Clock Single-Ended Input Voltage

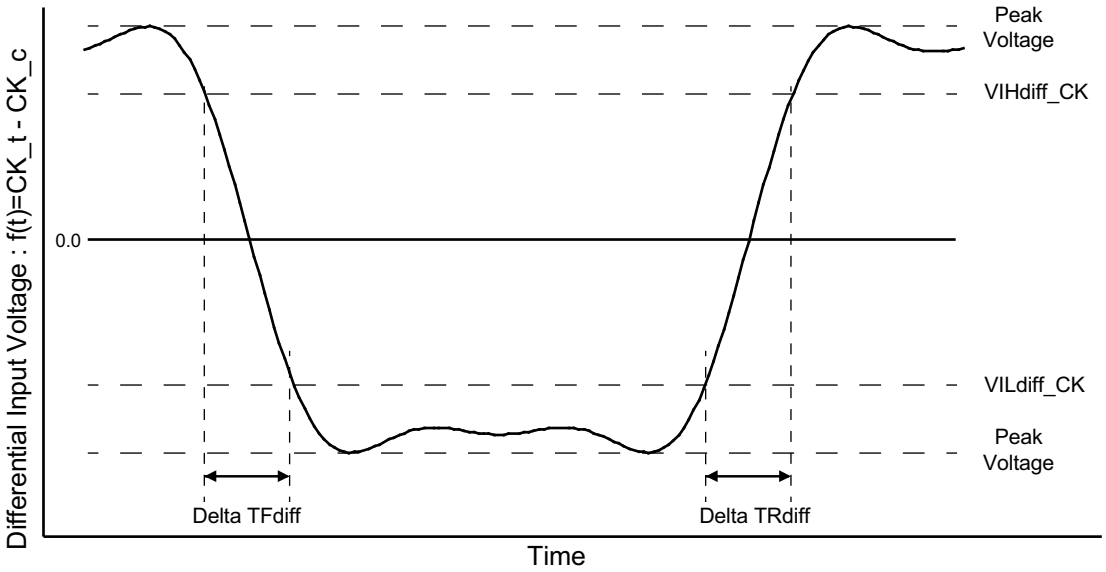
Table 112 — Clock Single-Ended input voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock Single-Ended input voltage	Vinse_CK	210	-	190	-	180	-	mV	1
Clock Single-Ended input voltage High from $V_{REF}CA$	Vinse_CK_High	105	-	95	-	90	-	mV	1
Clock Single-Ended input voltage Low from $V_{REF}CA$	Vinse_CK_Low	105	-	95	-	90	-	mV	1

NOTE 1 These requirements apply for DQ operating frequencies at or below 1333 Mbps for all speed bins for the first column, 1600/1866.

7.3.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 88 and Table 113 through Table 115.



NOTES : 1. Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
2. Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

Figure 88 — Differential Input Slew Rate Definition for CK_t, CK_c

Table 113 — Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge(CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTFdiff

Table 114 — Differential Input Level for CK_t, CK_c

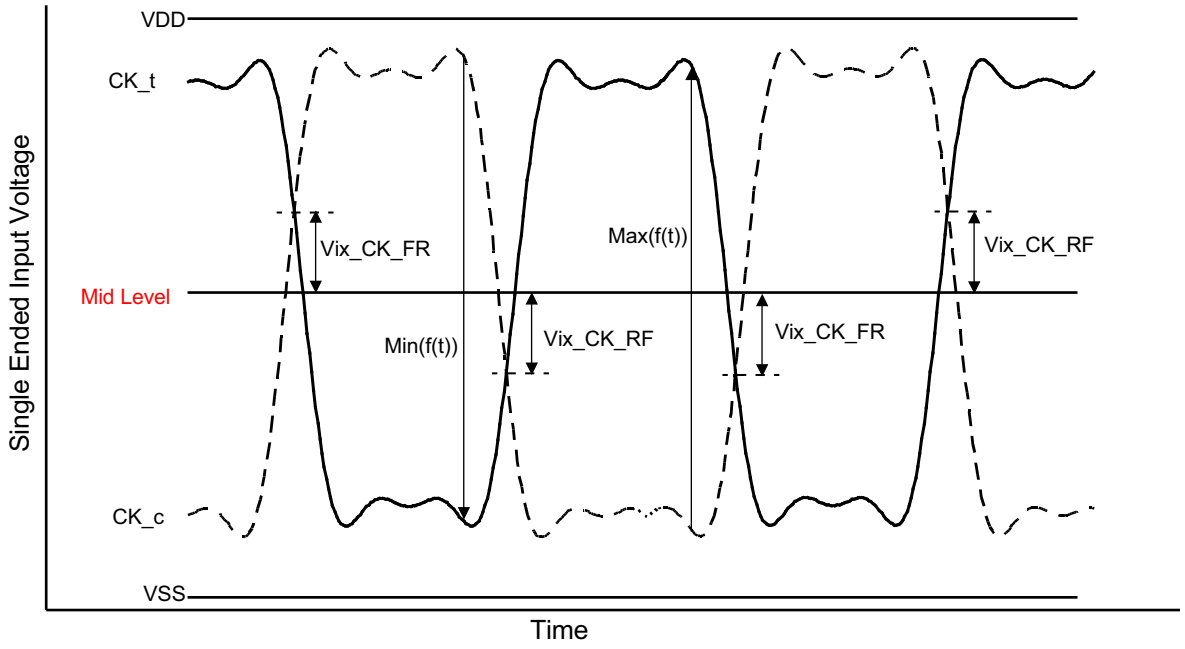
Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input High	VIHdiff_CK	175	-	155	-	145	-	mV	1
Differential Input Low	VILdiff_CK	-	-175	-	-155	-	-145	mV	1
NOTE 1 These requirements apply for DQ operating frequencies at or below 1333 Mbps for all speed bins for the first column, 1600/1866.									

Table 115 — Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	V/ns	

7.3.5 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK_t, CK_c) are shown in Figure 89 and must meet the requirements in Table 116. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level.



NOTES : 1. The base level of Vix_CK_FR/RF is V_{REF}CA that is LPDDR4X-NVM internal setting value by V_{REF} Training.

Figure 89 — Vix Definition (Clock)

Table 116 — Cross Point Voltage for Differential Input Signals (Clock)

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock Differential input cross point voltage ratio	Vix_CK_ratio	-	25	-	25	-	25	%	1,2,**3**,4,5

NOTE 1 These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column,1600/1866.

NOTE 2 Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|

NOTE 3 Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))

NOTE 4 Vix_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
Vix_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.

NOTE 5 In LPDDR4X-NVM un-terminated case, CK mid-level is calculated as:
High level = VDDQ, Low level=VSS, Mid-level = VDDQ/2.

7.4 Single Ended Output Slew Rate

The single ended slew rate is provided in Figure 90 and Table 117.

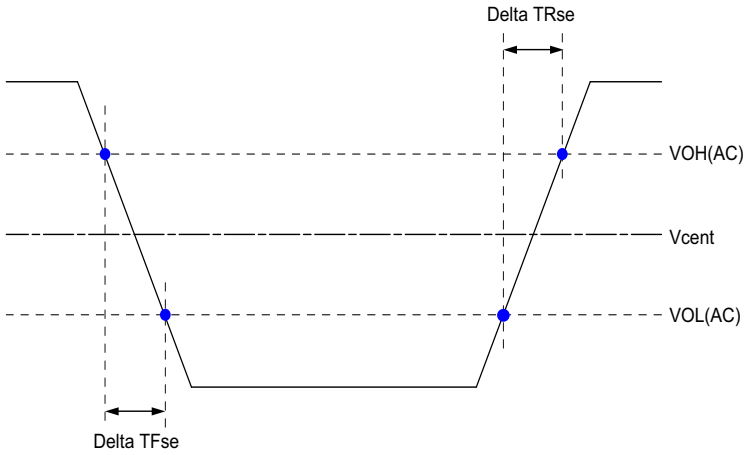


Figure 90 — Single Ended Output Slew Rate Definition

Table 117 — Output Slew Rate (Single Ended) for 0.6 V V_{DDQ}

Parameter	Symbol	Value		Units
		Min	Max	
Single Ended Output Slew Rate (VOH=V_{DDQ} * 0.5)	SRQse	3	9	V/ns
Output Slew Rate Matching Ratio (Rise to Fall)	-	0.8	1.2	-

NOTE 1 Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single Ended Signals

NOTE 2 Measured with output reference load.

NOTE 3 The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

NOTE 4 The output slew rate for falling and rising edges is defined and measured between VOL(AC) = 0.2*VOH(DC) and VOH(AC) = 0.8*VOH(DC).

NOTE 5 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

7.5 Differential Output Slew Rate

The slew rate is provided in Figure 91 and Table 118

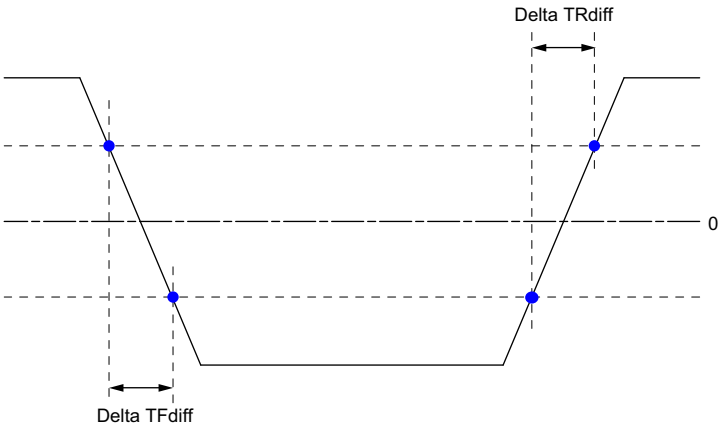


Figure 91 — Differential Output Slew Rate Definition

Table 118 — Differential Output Slew Rate for 0.6 V V_{DDQ}

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (VOH=V_{DDQ}/3)	SRQdiff	6	18	V/ns

NOTE 1 Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals

NOTE 2 Measured with output reference load.

NOTE 3 The output slew rate for falling and rising edges is defined and measured between VOL(AC)= -0.8*VOH(DC) and VOH(AC)= 0.8*VOH(DC).

NOTE 4 Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

7.6 Overshoot and Undershoot for LVSTL

The levels are provided in Table 119 and Figure 92.

Table 119 — AC Overshoot/Undershoot Specification

Parameter		Data Rate				Units
		1600	1866	3200	4266	
Maximum peak amplitude allowed for overshoot area. (See Figure 92)	Max	0.3	0.3	0.3	0.3	V
Maximum peak amplitude allowed for undershoot area. (See Figure 92)	Max	0.3	0.3	0.3	0.3	V
Maximum area above V_{DD}. (See Figure 92)	Max	0.1	0.1	0.1	0.1	V-ns
Maximum area below V_{SS}. (See Figure 92)	Max	0.1	0.1	0.1	0.1	V-ns

NOTE 1 V_{DD} stands for V_{DD2} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{DD} stands for V_{DDQ} for DQ, ECCO, DQS_t and DQS_c.

NOTE 2 V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{SS} stands for V_{SSQ} for DQ, ECCO, DQS_t and DQS_c.

NOTE 3 Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.

NOTE 4 Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

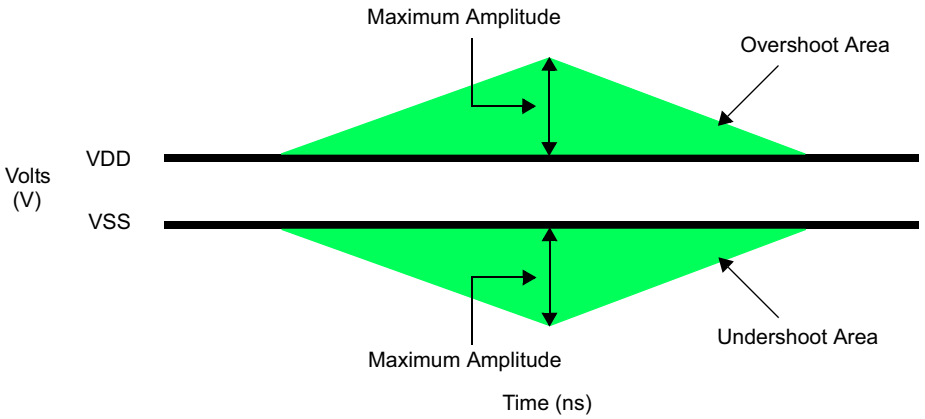
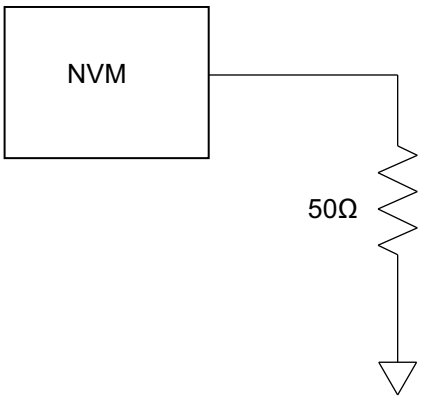


Figure 92 — Overshoot and Undershoot Definition

7.7 LPDDR4 Driver Output Timing Reference Load

These 'Timing Reference Loads' (Figure 93) are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Note
1. All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

Figure 93 — Driver Output Reference Load for Timing and Slew Rate

7.8 LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell for the LPDDR4X-NVM device is comprised of a pull-up and a pull-down driver. Note that the pull-down terminator for a normal LVSTL I/O cell has been eliminated due to the (largely) read-only nature of the DQs on the LPDDR4X-NVM device. The basic cell is shown in Figure 94.

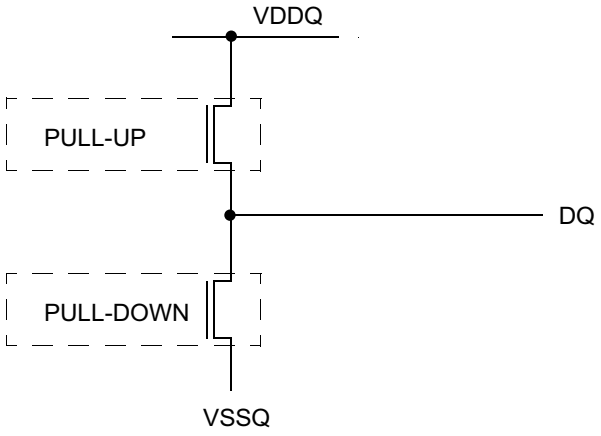


Figure 94 — LVSTL I/O Cell

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to calibrated as below procedure.

1. First calibrate the pull-down device against a 240 Ω resister to V_{DDQ} via the ZQ pin. (Figure 95.)
   - Set Strength Control to minimum setting.
   - Increase drive strength until comparator detects data bit is less than $V_{DDQ}/2$.
   - NMOS pull-down device is calibrated to 240 Ω.

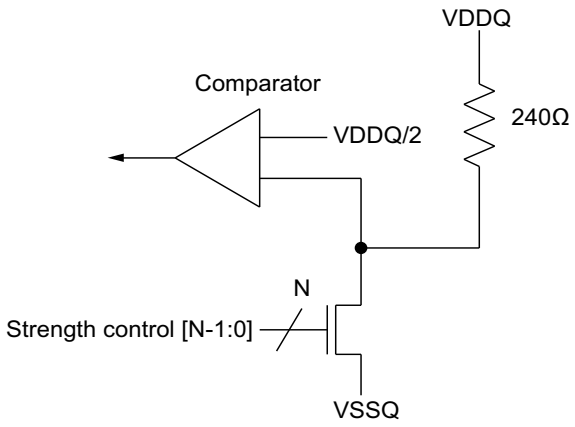


Figure 95 — Pull-down calibration

2. Then calibrate the pull-up device against the calibrated pull-down device. (Figure 96.)
   - Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
   - Set Strength Control to minimum setting.
   - Increase drive strength until comparator detects data bit is greater than VOH target.
   - NMOS pull-up device is now calibrated to VOH target.

7.8 LVSTL (Low Voltage Swing Terminated Logic) IO System (cont'd)

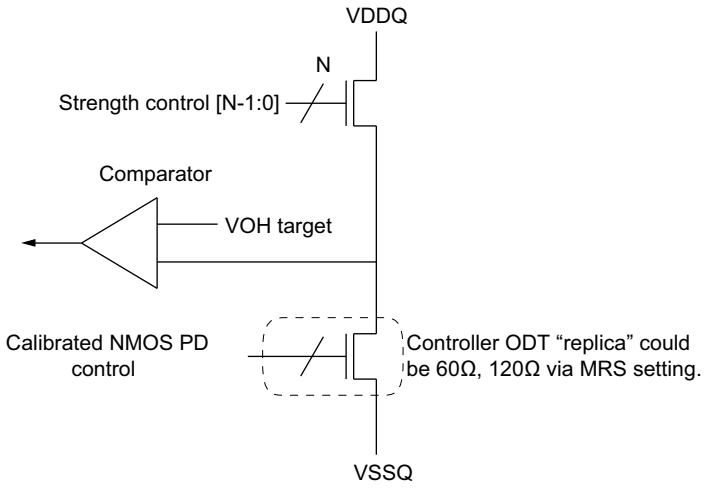


Figure 96 — Pull-up Calibration

7.9 SPI, INT_n, DEVRST _n Input and Output Measurement Levels

The device SPI, INT_n and DEVRST_n input and output voltages must be within the VDDQ_SPI voltage range. The voltage parameters for each of the ranges are defined in JESD8-26 (1.2 V) and JESD8-31 (1.8 V).

8 Input/Output Capacitance

The input/output capacitance is provided in Table 120.

Table 120 — Input/Output Capacitance

Parameter	Interface	Symbol		Capacitance	Units	Notes
Input capacitance, CK_t and CK_c	LPDDR	CCK	Min	0.5	pF	1,2
			Max	0.9	pF	1,2
Input capacitance delta, CK_t and CK_c		CDCK	Min	0.0	pF	1,2,3
			Max	0.09	pF	1,2,3
Input capacitance, All other input-only pins		CI	Min	0.5	pF	1,2,4
			Max	0.9	pF	1,2,4
Input capacitance delta, All other input-only pins		CDI	Min	-0.1	pF	1,2,5
			Max	0.1	pF	1,2,5
Input/output capacitance, DQ, ECCO, DQS_t, DQS_c		CIO	Min	0.7	pF	1,2,6
			Max	1.3	pF	1,2,6
Input/output capacitance delta, DQS_t, DQS_c		CDDQS	Min	0.0	pF	1,2,7
			Max	0.1	pF	1,2,7
Input/output capacitance delta, DQ, ECCO		CDIO	Min	-0.1	pF	1,2
			Max	0.1	pF	1,2
Input/output capacitance, ZQ pin		CZQ	Min	0.0	pF	1,2
			Max	5.0	pF	1,2
SPI Input Capacitance (SPI_CS_n, SPII_CK, DEVRST_n)	SPI + MISC	CIN_SPI	Min	0.0	pF	1,2,8
			Max	6.0	pF	1,2,8
SPI IO Capacitance (SPI_DQ[3:0], INT_n)		CIO_SPI	Min	0.0	pF	1,2,8
			Max	8.0	pF	1,2,8

NOTE 1 This parameter applies to the die device only (does not include package capacitance).

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, V_{DDQ_SPI}, V_{SS}, V_{SSQ} applied and all other pins floating.

NOTE 3 Absolute value of CCK_t - CCK_c.

NOTE 4 CI applies to CS_n, CKE, CA0~CA5.

NOTE 5 CDI = CI - 0.5 * (CCK_t + CCK_c)

NOTE 6 ECCO loading matches DQ and DQS.

NOTE 7 Absolute value of CDQS_t - CDQS_c.

NOTE 8 This parameter applies to the SPI, DEVRST_n, INT_n signals of a die device only (does not include package capacitance)

9 IDD Specification Parameters And Test Conditions

9.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:
LOW: VIN ≤ VIL(DC) MAX
HIGH: VIN ≥ VIH(DC) MIN
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See Table 121 through Table 129

Differences exist between Measurement Conditions for devices with different row sizes and burst lengths during the four different read operations.

During standby conditions the CA bus is driven as described in Table 121. Standby measurements assume an idle SPI bus with no embedded operations (e.g. Erase or Program).

During read operations the DQs drive outputs as described for BL16 (Table 124) and BL32 (Table 123).

The tables describe the IDD measurement conditions for:

1. Standby - With and without an activated row and with or without CK/CA switching. Note that only the Modified JEDEC Read supports an open row policy.
2. Row Activation - Only the Modified JEDEC Read supports an open row policy. The Legacy JEDEC Read and the Non-Volatile Read performs both the activation and the read functions within the RL period.
3. Modified Read - Targets a longer latency NVM with tRCD times specified by the device manufacturer. Explicit row activation and open rows are supported.
4. Legacy Read - The Legacy Read command performs both the activation and the read functions within the RL period. Open rows are not supported.
5. Non-Volatile Read (NVR) - The NVR command performs both the activation and the read functions within the RL period. Open rows are not supported.

Table 121 — Definition of Switching for CA Input Signals

Switching for CA								
CK_t edge	**R1**	**R2**	**R3**	**R4**	**R5**	**R6**	**R7**	**R8**
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE 1 CS must always be driven LOW.
NOTE 2 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
NOTE 3 The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

9.1 IDD Measurement Conditions (cont'd)

Table 122 — Data Pattern for IDD4R for BL=16

	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	ECCO	No. of 1's
BL0	1	1	1	1	1	1	1	1	V	8
BL1	1	1	1	1	0	0	0	0	V	4
BL2	0	0	0	0	0	0	0	0	V	0
BL3	0	0	0	0	1	1	1	1	V	4
BL4	0	0	0	0	0	0	1	1	V	2
BL5	0	0	0	0	1	1	1	1	V	4
BL6	1	1	1	1	1	1	0	0	V	6
BL7	1	1	1	1	0	0	0	0	V	4
BL8	1	1	1	1	1	1	1	1	V	8
BL9	1	1	1	1	0	0	0	0	V	4
BL10	0	0	0	0	0	0	0	0	V	0
BL11	0	0	0	0	1	1	1	1	V	4
BL12	0	0	0	0	0	0	1	1	V	2
BL13	0	0	0	0	1	1	1	1	V	4
BL14	1	1	1	1	1	1	0	0	V	6
BL15	1	1	1	1	0	0	0	0	V	4
BL16	1	1	1	1	1	1	1	1	V	8
BL17	1	1	1	1	0	0	0	0	V	4
BL18	0	0	0	0	0	0	0	0	V	0
BL19	0	0	0	0	1	1	1	1	V	4
BL20	1	1	1	1	1	1	0	0	V	6
BL21	1	1	1	1	0	0	0	0	V	4
BL22	0	0	0	0	0	0	1	1	V	2
BL23	0	0	0	0	1	1	1	1	V	4
BL24	0	0	0	0	0	0	0	0	V	0
BL25	0	0	0	0	1	1	1	1	V	4
BL26	1	1	1	1	1	1	1	1	V	8
BL27	1	1	1	1	0	0	0	0	V	4
BL28	0	0	0	0	0	0	1	1	V	2
BL29	0	0	0	0	1	1	1	1	V	4
BL30	1	1	1	1	1	1	0	0	V	6
BL31	1	1	1	1	0	0	0	0	V	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE 1 Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4R pattern programming.
NOTE 2 The ECCO signal is allowed to be in either the disabled state (output all 0s) or the enabled state (output User ECC data).
NOTE 3 The values on DQ[7:0] are repeated on each of the byte lanes.

9.1 IDD Measurement Conditions (cont'd)

Table 123 — Data Pattern for IDD4R for BL=32

	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	ECCO	No. of 1's
BL0	1	1	1	1	1	1	1	1	V	8
BL1	1	1	1	1	0	0	0	0	V	4
BL2	0	0	0	0	0	0	0	0	V	0
BL3	0	0	0	0	1	1	1	1	V	4
BL4	0	0	0	0	0	0	1	1	V	2
BL5	0	0	0	0	1	1	1	1	V	4
BL6	1	1	1	1	1	1	0	0	V	6
BL7	1	1	1	1	0	0	0	0	V	4
BL8	1	1	1	1	1	1	1	1	V	8
BL9	1	1	1	1	0	0	0	0	V	4
BL10	0	0	0	0	0	0	0	0	V	0
BL11	0	0	0	0	1	1	1	1	V	4
BL12	0	0	0	0	0	0	1	1	V	2
BL13	0	0	0	0	1	1	1	1	V	4
BL14	1	1	1	1	1	1	0	0	V	6
BL15	1	1	1	1	0	0	0	0	V	4
BL16	1	1	1	1	1	1	0	0	V	6
BL17	1	1	1	1	0	0	0	0	V	4
BL18	0	0	0	0	0	0	1	1	V	2
BL19	0	0	0	0	1	1	1	1	V	4
BL20	0	0	0	0	0	0	0	0	V	0
BL21	0	0	0	0	1	1	1	1	V	4
BL22	1	1	1	1	1	1	1	1	V	8
BL23	1	1	1	1	0	0	0	0	V	4
BL24	0	0	0	0	0	0	1	1	V	2
BL25	0	0	0	0	1	1	1	1	V	4
BL26	1	1	1	1	1	1	0	0	V	6
BL27	1	1	1	1	0	0	0	0	V	4
BL28	1	1	1	1	1	1	1	1	V	8
BL29	1	1	1	1	0	0	0	0	V	4
BL30	0	0	0	0	0	0	0	0	V	0
BL31	0	0	0	0	1	1	1	1	V	4
BL32	0	0	0	0	0	0	1	1	V	2
BL33	0	0	0	0	1	1	1	1	V	4
BL34	1	1	1	1	1	1	0	0	V	6
BL35	1	1	1	1	0	0	0	0	V	4
BL36	1	1	1	1	1	1	1	1	V	8
BL37	1	1	1	1	0	0	0	0	V	4
BL38	0	0	0	0	0	0	0	0	V	0
BL39	0	0	0	0	1	1	1	1	V	4
BL40	0	0	0	0	0	0	1	1	V	2
BL41	0	0	0	0	1	1	1	1	V	4

Table 123 — Data Pattern for IDD4R for BL=32 (cont'd)

	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	ECCO	No. of 1's
BL42	1	1	1	1	1	1	0	0	V	6
BL43	1	1	1	1	0	0	0	0	V	4
BL44	1	1	1	1	1	1	1	1	V	8
BL45	1	1	1	1	0	0	0	0	V	4
BL46	0	0	0	0	0	0	0	0	V	0
BL47	0	0	0	0	1	1	1	1	V	4
BL48	1	1	1	1	1	1	1	1	V	8
BL49	1	1	1	1	0	0	0	0	V	4
BL50	0	0	0	0	0	0	0	0	V	0
BL51	0	0	0	0	1	1	1	1	V	4
BL52	1	1	1	1	1	1	0	0	V	6
BL53	1	1	1	1	0	0	0	0	V	4
BL54	0	0	0	0	0	0	1	1	V	2
BL55	0	0	0	0	1	1	1	1	V	4
BL56	0	0	0	0	0	0	0	0	V	0
BL57	0	0	0	0	1	1	1	1	V	4
BL58	1	1	1	1	1	1	1	1	V	8
BL59	1	1	1	1	0	0	0	0	V	4
BL60	0	0	0	0	0	0	1	1	V	2
BL61	0	0	0	0	1	1	1	1	V	4
BL62	1	1	1	1	1	1	0	0	V	6
BL63	1	1	1	1	0	0	0	0	V	4
No. of 1's	32	32	32	32	32	32	32	32		

NOTE 1 Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.
NOTE 2 The ECCO signal is allowed to be in either the disabled state (output all 0s) or the enabled state (output User ECC data).
NOTE 3 The values on DQ[7:0] are repeated on each of the byte lanes.

9.1.1 Modified JEDEC Read

Table 124 — CA Pattern for IDD4R for BL=16 (Modified JEDEC Read)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE 1 BA[2:0] = 010, C[9:4] = 000000 or 111111, Burst Order C[3:2] = 00 or 11
NOTE 2 CA pins are kept low with DES CMD to reduce ODT current.
NOTE 3 This table applies to the BL16 Modified JEDEC Read with a previously activated row.

9.1.1 Modified JEDEC Read (cont'd)

Table 125 — CA Pattern for IDD4R for BL=32 (Modified JEDEC Read)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

NOTE 1 BA[2:0] = 010, C[9:5] = 00000 or 11111, Burst Order C[4:2] = 000 or 111.

NOTE 2 This table applies to the Modified JEDEC Read with a previously activated row.

9.1.2 Legacy JEDEC Read

Table 126 — CA Pattern for IDD4R for BL=16 (Legacy JEDEC Read)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	ACT-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	ACT-2	L	L	L	L	L	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+5	HIGH	LOW		L	H	L	L	L	L
N+6	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+7	HIGH	LOW		L	H	H	H	H	H
N+8	HIGH	HIGH	ACT-1	H	H	H	H	H	H
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	ACT-2	H	H	H	H	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+13	HIGH	LOW		L	H	L	L	H	L
N+14	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+15	HIGH	LOW		H	H	H	H	H	H

NOTE 1 BA[2:0] = 010 or 101
NOTE 2 R[23:0] = 0..0 or 1..1 for 32B row, R[22:0] = 0..0 or 1..1 for 64B row
NOTE 3 C[3:2] = 00 or 11 for 32B row, C[4:2] = 000 or 111 for 64B row
NOTE 4 This table applies to the Legacy JEDEC Read. Both Activation and Read activities are performed within the RL period.

9.1.2 Legacy JEDEC Read (cont'd)

Table 127 — CA Pattern for IDD4R for BL=32 (Legacy JEDEC Read)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	ACT-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	ACT-2	L	L	L	L	L	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+5	HIGH	LOW		L	H	L	L	L	L
N+6	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+7	HIGH	LOW		L	H	H	H	H	H
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	ACT-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	L	L
N+18	HIGH	HIGH	ACT-2	L	L	L	L	L	L
N+19	HIGH	LOW		L	L	L	L	L	L
N+20	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+21	HIGH	LOW		L	H	L	L	L	L
N+22	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+23	HIGH	LOW		L	H	H	H	H	H
N+24	HIGH	HIGH	LOW	DES	L	L	L	L	L
N+25	HIGH	LOW	LOW	DES	L	L	L	L	L
N+26	HIGH	HIGH	LOW	DES	L	L	L	L	L
N+27	HIGH	LOW	LOW	DES	L	L	L	L	L
N+28	HIGH	HIGH	LOW	DES	L	L	L	L	L
N+29	HIGH	LOW	LOW	DES	L	L	L	L	L
N+30	HIGH	HIGH	LOW	DES	L	L	L	L	L
N+31	HIGH	LOW	LOW	DES	L	L	L	L	L

NOTE 1 BA[2:0] = 010 or 101

NOTE 2 R[23:0] = 0..0 or 1..1 for 32B row, R[22:0] = 0..0 or 1..1 for 64B row

NOTE 3 C[3:2] = 00 or 11 for 32B row, C[4:2] = 000 or 111 for 64B row

NOTE 4 This table applies to the Legacy JEDEC Read. Both Activation and Read activities are performed within the RL period.

9.1.3 Non-Volatile Read (NVR)

Table 128 — CA Pattern for IDD4R for BL=16 (NVR Read)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	NVR-1	H	L	L	L	L	L
N+1	HIGH	LOW		L	L	L	L	L	L
N+2	HIGH	HIGH	NVR-2	L	L	L	L	L	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	NVR-1	H	H	H	H	H	H
N+9	HIGH	LOW		H	H	H	H	H	H
N+10	HIGH	HIGH	NVR-2	H	H	H	H	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE 1 R[22:0] = 000 0000 0000 0000 0000 0000 or 111 1111 1111 1111 1111 1111, C[4:2] = 000 for 64B row or C[3:2] = 00 for 32B row.

NOTE 2 CA pins are kept low with DES CMD to reduce ODT current.

NOTE 3 This table applies to the NVR Read. Both Activation and READ activities are performed within the RL period.

9.1.3 Non-Volatile Read (NVR) (cont'd)

Table 129 — CA Pattern for IDD4R for BL=32 (NVR Read)

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	NVR-1	H	L	L	L	L	L
N+1	HIGH	LOW		L	L	L	L	L	L
N+2	HIGH	HIGH	NVR-2	L	L	L	L	L	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	NVR-1	H	H	H	H	H	H
N+17	HIGH	LOW		H	H	H	H	H	H
N+18	HIGH	HIGH	NVR-2	H	H	H	H	H	H
N+19	HIGH	LOW		H	H	H	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

NOTE 1 R[22:0] = 000 0000 0000 0000 0000 0000 or 111 1111 1111 1111 1111 1111, C[4:2] = 000.

NOTE 2 CA pins are kept low with DES CMD to reduce ODT current.

NOTE 3 This table applies to the NVR Read. Both Activation and READ activities are performed within the RL period.

9.2 IDD Specifications

I_{DD} values are for the entire operating voltage range, and all of them are for the entire standard temperature range. See Table 130 for a description of current consumption related to various LPDDR4X bus activities. Current consumption related to SPI activities is described in Table 131.

Table 130 — LPDDR4 I_{DD} Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus is stable ODT disabled Only relevant for Modified READ	$I_{DD}0_1$	V_{DD1}	6, 9
	$I_{DD}0_2$	V_{DD2}	6, 9
	$I_{DD}0_Q$	V_{DDQ}	2, 6, 9
	$I_{DD}0_{Q\_SPI}$	V_{DDQ_SPI}	6, 9
Idle power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus is stable ODT disabled	$I_{DD}2P_1$	V_{DD1}	6, 7, 8, 9
	$I_{DD}2P_2$	V_{DD2}	6, 7, 8, 9
	$I_{DD}2P_Q$	V_{DDQ}	2, 6, 7, 8, 9
	$I_{DD}2P_{Q\_SPI}$	V_{DDQ_SPI}	6, 7, 8, 9
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus is stable ODT disabled	$I_{DD}2PS_1$	V_{DD1}	6, 7, 8, 9
	$I_{DD}2PS_2$	V_{DD2}	6, 7, 8, 9
	$I_{DD}2PS_Q$	V_{DDQ}	2, 6, 7, 8, 9
	$I_{DD}2PS_{Q\_SPI}$	V_{DDQ_SPI}	6, 7, 8, 9
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus is stable ODT disabled	$I_{DD}2N_1$	V_{DD1}	6, 7, 8, 9
	$I_{DD}2N_2$	V_{DD2}	6, 7, 8, 9
	$I_{DD}2N_Q$	V_{DDQ}	2, 6, 7, 8, 9
	$I_{DD}2N_{Q\_SPI}$	V_{DDQ_SPI}	6, 7, 8, 9

Table 130 — LPDDR4 I_{DD} Specification Parameters and Operating Conditions (cont'd)

Parameter/Condition	Symbol	Power Supply	Notes
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus is stable ODT disabled	$I_{DD}2NS_1$	V_{DD1}	6, 7, 8, 9, 10
	$I_{DD}2NS_2$	V_{DD2}	6, 7, 8, 9, 10
	$I_{DD}2NS_Q$	V_{DDQ}	2, 6, 7, 8, 9, 10
	$I_{DD}2NS_{Q\_SPI}$	V_{DDQ_SPI}	6, 7, 8, 9, 10
Active power-down standby current: tCK = tCKmin; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus is stable ODT disabled	$I_{DD}3P_1$	V_{DD1}	6, 9
	$I_{DD}3P_2$	V_{DD2}	6, 9
	$I_{DD}3P_Q$	V_{DDQ}	2, 6, 9
	$I_{DD}3P_{Q\_SPI}$	V_{DDQ_SPI}	6, 9
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus is stable ODT disabled	$I_{DD}3PS_1$	V_{DD1}	6, 9
	$I_{DD}3PS_2$	V_{DD2}	6, 9
	$I_{DD}3PS_Q$	V_{DDQ}	3, 6, 9
	$I_{DD}3PS_{Q\_SPI}$	V_{DDQ_SPI}	6, 9
Active non-power-down standby current: tCK = tCKmin; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus is stable ODT disabled	$I_{DD}3N_1$	V_{DD1}	6, 9
	$I_{DD}3N_2$	V_{DD2}	6, 9
	$I_{DD}3N_Q$	V_{DDQ}	3, 6, 9
	$I_{DD}3N_{Q\_SPI}$	V_{DDQ_SPI}	6, 9

Table 130 — LPDDR4 I_{DD} Specification Parameters and Operating Conditions (cont'd)

Parameter/Condition	Symbol	Power Supply	Notes
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus is stable ODT disabled	$I_{DD}3NS_1$	V_{DD1}	6, 9
	$I_{DD}3NS_2$	V_{DD2}	6, 9
	$I_{DD}3NS_Q$	V_{DDQ}	3, 6, 9
	$I_{DD}3NS_{Q\_SPI}$	V_{DDQ_SPI}	6, 9
Operating burst READ current: tCK = tCKmin; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$I_{DD}4R_1$	V_{DD1}	6, 7, 8, 9, 11, 12
	$I_{DD}4R_2$	V_{DD2}	6, 7, 8, 9, 11, 12
	$I_{DD}4R_Q$	V_{DDQ}	4, 6, 7, 8, 9, 11, 12
	$I_{DD}4R_{Q\_SPI}$	V_{DDQ_SPI}	6, 7, 8, 9, 11, 12

NOTE 1 Published I_{DD} values are the maximum of the distribution of the arithmetic mean.

NOTE 2 I_{DD} current specifications are tested after the device is properly initialized.

NOTE 3 Measured currents are the summation of V_{DDQ} and V_{DD2}.

NOTE 4 Guaranteed by design with output load = 5pF and RON = 40 Ω.

NOTE 5 For all I_{DD} measurements, VIHCKE = 0.8 x V_{DD2}, VILCKE = 0.2 x V_{DD2}.

NOTE 6 Applicable to Modified JEDEC Read.

NOTE 7 Applicable to Legacy JEDEC Read.

NOTE 8 Applicable to Non-Volatile Read (NVR).

NOTE 9 SPI bus is idle with no embedded operations being performed.

NOTE 10 The $I_{DD}2NS$ specs should be the same as the $I_{DD}SB$ specs because both interfaces are idle and there are no embedded operations.

NOTE 11 For the Modified READ, IDD4 assumes continual gapless reads from an already open row.

NOTE 12 For the Legacy READ and Non-Volatile READ, IDD4 assumes continual gapless reads from closed rows.

9.2 IDD Specifications (cont'd)

Table 131 — SPI I_{DD} Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Standby current: LPDDR4X bus idle SPI bus idle	$I_{DD}SB_1$	V_{DD1}	5, 6, 7
	$I_{DD}SB_2$	V_{DD2}	5, 6, 7
	$I_{DD}SB_Q$	V_{DDQ}	5, 6, 7
	$I_{DD}SB_{Q\_SPI}$	V_{DDQ_SPI}	5, 6, 7
Read current: LPDDR4X bus idle Quad Mode Enabled tCK = tCK min	$I_{DD}RD_1$	V_{DD1}	3
	$I_{DD}RD_2$	V_{DD2}	3
	$I_{DD}RD_Q$	V_{DDQ}	3
	$I_{DD}RD_{Q\_SPI}$	V_{DDQ_SPI}	3
Erase current: LPDDR4X bus idle SPI bus idle	$I_{DD}ER_1$	V_{DD1}	5, 6
	$I_{DD}ER_2$	V_{DD2}	5, 6
	$I_{DD}ER_Q$	V_{DDQ}	5, 6
	$I_{DD}ER_{Q\_SPI}$	V_{DDQ_SPI}	5, 6
Program current: LPDDR4X bus idle SPI bus idle	$I_{DD}PG_1$	V_{DD1}	5, 6
	$I_{DD}PG_2$	V_{DD2}	5, 6
	$I_{DD}PG_Q$	V_{DDQ}	5, 6
	$I_{DD}PG_{Q\_SPI}$	V_{DDQ_SPI}	5, 6

NOTE 1 Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
NOTE 2 I_{DD} current specifications are tested after the device is properly initialized.
NOTE 3 Guaranteed by design with output load = 5pF and RON = 40 Ω.
NOTE 4 For all I_{DD} measurements, VIH_SPI=0.8 x V_{DDQ_SPI}, VIL_SPI=0.2 x V_{DDQ_SPI}, VIHCKE = 0.8 x V_{DD2}, VILCKE = 0.2 x V_{DD2}.
NOTE 5 LPDDR4X bus idle: CK_t =LOW, CK_c =HIGH, CKE is LOW, CS is LOW, All banks are idle, CA inputs LOW, ODT off
NOTE 6 SPI bus idle: SPI_CS_n=HIGH, SPI_CK=LOW, SPI_DQ[3:0]=HIGH-Z
NOTE 7 The I_{DD}SB specs should be the same as the I_{DD}2NS specs because both interfaces are idle and there are no embedded operations.

10 Serial Peripheral Interface Port

10.1 SPI Port Introduction

The 4-bit Quad-SPI (QSPI) port is included as a second memory port that is compatible with legacy SPI infrastructure found on virtually all host controllers.

The SPI transaction protocol is partially described by the relationship between the CS# and CK signals. Clock Polarity (CPOL) and Clock Phase (CPHA) is defined by how the CK signal behaves when CS# transitions from the HIGH to LOW state at the beginning of a SPI transaction. LPDDR4X-NVM devices only support the CPOL=CPHA=00 mode of operation where CK is required to be LOW when CS# transitions LOW, input data is latched on the leading (rising) edge of CK and output data is driven after the trailing (falling) edge of CK. Note that host side memory controllers often latch the memory's output data on the next falling clock edge to improve timing margins and achieve higher clock rates. Table 132 and Figure 97 describe the CPOL and CPHA nomenclature.

Table 132 — CK Phase and Polarity Relationship with CS#

CPOL/CPHA	CPOL	CPHA	Description
00	0	0	CK LOW when CS# goes LOW,
			Data input latched on leading (rising) edge of CK
			Data output after falling CK
01	0	1	CK LOW when CS# goes LOW,
			Data input latched on trailing (falling) edge of CK
			Data output after rising CK
10	1	0	CK HIGH when CS# goes LOW,
			Data input latched on leading (falling) edge of CK
			Data output after rising CK
11	1	1	CK HIGH when CS# goes LOW,
			Data input latched on trailing (rising) edge of CK
			Data output after falling CK

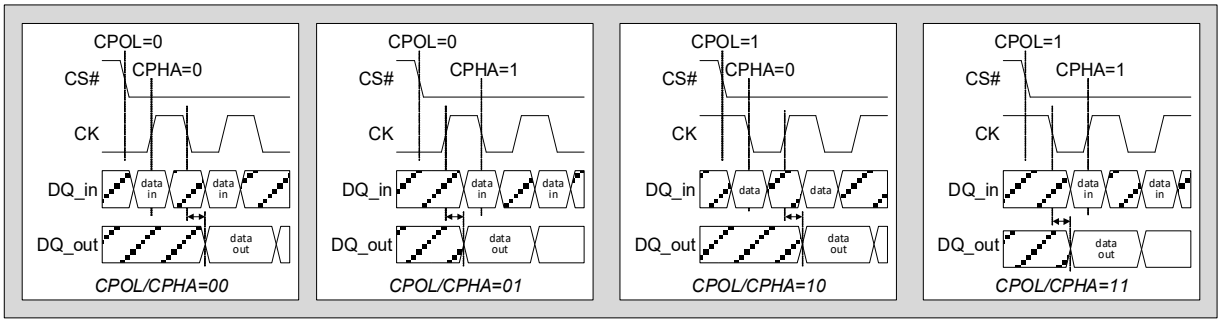


Figure 97 — CK Phase and Polarity Relationship with CS# (only Mode 00 Supported)

10.2 SPI/QSPI Timings

The minimalist SPI/QSPI timings can be described in three timing diagrams.

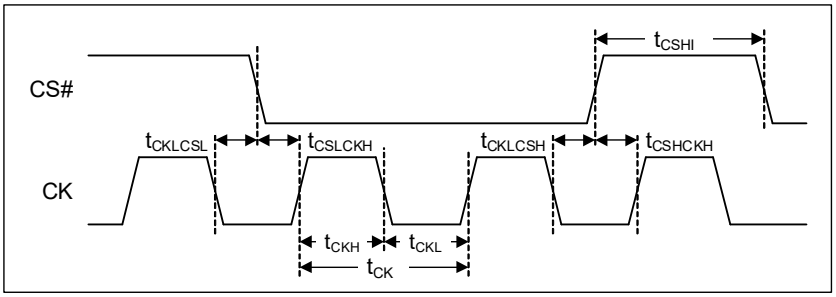


Figure 98 — CK and CS# Timings

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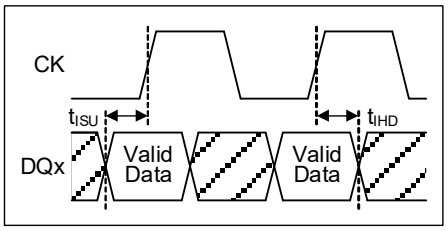

Figure 99 — CK to DQ Input (CS# = LOW)

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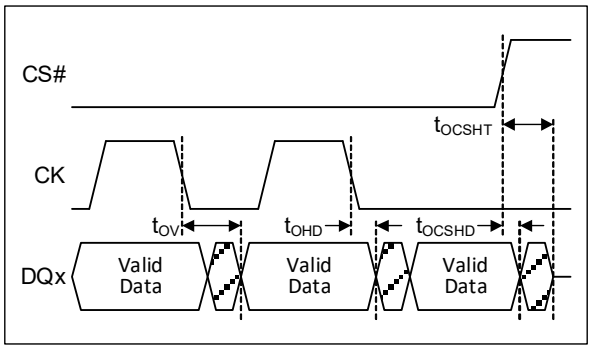

Figure 100 — CK/CS# to DQ Output

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10.2 SPI/QSPI Timings (cont'd)

Table 133 — SPI/QSPI Timings

Parameter	Symbol	MIN	MAX	Unit
Clock Period	t_{CK}	10	-	ns
Clock LOW Time	t_{CKL}	45	55	% t_{CK}
Clock HIGH Time	t_{CKH}	45	55	% t_{CK}
CS# HIGH Between Transactions (after READs)	t_{CSHI_1}	100	-	ns
CS# HIGH Between Transactions (after Write/Erase/Program)	t_{CSHI_2}	100	-	ns
CK LOW Prior to CS# Transitioning LOW	t_{CKLCSL}	8	-	ns
CS# LOW Prior to CK Transitioning HIGH	t_{CSLCKH}	8	-	ns
CK LOW Prior to CS# Transitioning HIGH	t_{CKLCSH}	8	-	ns
CS# HIGH Prior to CK Transitioning HIGH	t_{CSHCKH}	8	-	ns
Input Data Setup Time	t_{ISU}	2	-	ns
Input Data Hold Time	t_{IHD}	2	-	ns
CK to Output Data Valid	t_{OV}	-	8	ns
Output Data Hold Time	t_{OHD}	1	-	ns
Output Data Valid After CS# HIGH	t_{OCSHD}	0	-	ns
Output Data Tri-State after CS# HIGH	t_{OCSHT}	-	20	ns

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10.3 SPI Command and Transaction Description

Table 134 describes the mandatory SPI commands that must be supported by all LPDDR4X-NVM devices. LPDDR4X-NVM manufacturers are allowed to support additional commands.

10.3.1 SPI Transaction Construction

SPI transactions on the LPDDR4X-NVM device are assembled using the following fields:

1. an 8-bit Command Code specifying what operation to perform
2. a 3-byte (24b) or 4-byte (32b) Command Modifier that specifies the target address
3. a Latency period may be needed for operations where the device outputs data back to the host
4. one or more bytes of Data transferred between host and memory

The Command Code field is included in all transactions but the other fields are included depending upon the specific transaction requirements.

Table 134 — Mandatory SPI Commands

1S-1S-1S Commands	**Command Code** *(note 1)*	**Command Modifier** *(note 3)*	**Latency** *(note 1, 3)*	**Data Bytes** *(note 2, 3)*	**Transaction Format**	**Minimum Required Frequency** *(note 4)*
Read SFDP (3 byte add)	5Ah	3B	8 CK	1+	0.a	50MHz
Read Zero Latency (3 byte add)	03h	3B	0 CK	1+	0.b	
Read ID	9Fh	na	0 CK	1+	0.c	
Read Status Register	05h	na	0 CK	1	0.c	100MHz
Write Enable	06h	na	na	na	0.d	
Write Disable	04h	na	na	na	0.d	
Erase	SFDP	4B	na	na	0.e	
Read Any Register *(see NOTE 6)*	65h	4B	0 CK or SFDP	1	0.f	
Write Any Register	71h or SFDP	4B	na	1	0.g	
Program	12h	4B	na	1+	0.h	
1S-1S-4S Commands	**Command Code**	**Command Modifier**	**Latency** *(note 1, 3)*	**Data Bytes**	**Transaction Format**	**Minimum Requited Frequency** *(note 4)*
Read Fast (4 byte add, *see NOTE 5*)	6Ch	4B	READ-ID or SFDP	1+	1.a	100MHz
Program	34h	4B	na	1+	1.b	

NOTE 1 SFDP refers to the Serial Flash Discoverable Parameters per JESD216.

NOTE 2 The Data lengths that are not explicit (1+) are specified in the SFDP.

NOTE 3 “na” indicates that the field is not part of the transaction and does not consume clock cycles.

NOTE 4 Any clock rate below the Minimum Required Frequency is supported. Manufacturers may support clock rates higher than the Minimum Required Frequency.

NOTE 5 The latency clock requirement at 100MHz Read Fast is found in either the SFDP or byte 9 of the Read ID data base.

NOTE 6 0 CK latency for volatile register read latency and SFDP for non-volatile register read latency.

10.3.2 SPI Command Description

The mandatory SPI command functionality is described in the following sections.

10.3.2.1 Read SFDP

The Read Serial Flash Discoverable Parameters (SFDP) command reads from a database of standard parameters stored within the LPDDR4X-NVM device. The format and content of this database is described in the JESD216 standard. In the 1S-1S-1S protocol mode, there is a command, a 3-byte address followed by 8 cycles of initial access latency, before SFDP data is output. See Figure 100 — 1S-1S-1S Format 0.a Command, 3-Byte Address, 8 Latency Cycles and Read Data. The memory transfers 1 or more bytes of SFDP information to the controller. The first four bytes of the SFDP data stream (starting at address 0) is identified by the 4 ASCII characters for “S” “F” “D” “P”.

The 3-byte address selects the starting point for reading a sequence of bytes from the SFDP database.

10.3.2.2 Read Zero Latency

The Read with Zero Latency command provides a backward compatible SPI operation for reading array data. This command is generally used for reading initial boot code from an SPI non-volatile memory before the device is identified. This initial boot code may perform device identification and then select a different supported read command for higher performance. Because Read Zero Latency in legacy devices provides very little read latency time for accessing a memory array, the mandatory clock rate guarantees operation of at a minimum of 50MHz. The SPI port may optionally support higher clock rates.

In the 1S-1S-1S protocol mode, the Read Zero Latency command uses a 3-byte address followed by no initial access latency, before data bytes are read. See Figure 101 — 1S-1S-1S Format 0.b Command, 3-byte Address and Read Data.

10.3.2.3 Read Fast

The Read Fast command provides a backward compatible SPI operation for reading array data at higher clock frequencies.

In the 1S-1S-4S protocol mode, the controller transfers the one byte command,4 bytes of address, followed by a configurable number of initial access latency cycles and then the memory transfers 1 or more bytes of data to the controller. See Figure 108 — 1S-1S-4S Format 1.a: Command, Address, ‘x’ Latency Cycles and Read Data.

10.3.2.4 Write Enable

The Write Enable command provides a backward compatible SPI operation for enabling operations that alter data in the memory device. Following POR, commands that change data are prevented from executing. The Write Enable command must precede commands to perform write, program or erase operations. The Write Enable command serves to make any data changes a two or more command sequence to minimize the chance of an inadvertent alteration.

In the 1S-1S-1S protocol mode, the controller transfers the one byte command. There are no additional command modifier bytes, latency or data phases. See Figure 103 1S-1S-1S Format 0.d: Command.

10.3.2.5 Write Disable

The Write Disable command provides a backward compatible SPI operation for disabling commands that alter data in the memory device. Following POR, commands that alter data are prevented from executing. The Write Disable command may be used following the end of data changing operation to return to a state in which these operations are again prevented from executing.

In the 1S-1S-1S protocol mode, the controller transfers the one byte command. There are no additional command modifier bytes, latency or data phases. See Figure 103 1S-1S-1S Format 0.d: Command.

10.3.2.6 Read ID

The Read ID command allows the user to query the LPDDR4X-NVM device to find device specific information. In the 1S-1S-1S protocol mode the Read ID Command-Code is issued by the host, and then the memory outputs ID information on a byte by byte basis. The first byte output by the memory is the Manufacturer ID, the next three bytes describe the Device ID. The fourth byte indicates the number of remaining bytes in the Read ID database. Additional bytes of identification information may be supported at the discretion of the manufacturer. If no additional Read ID bytes are supported, the Read ID length field (byte 4) is set to 00h. See the memory device data sheet for additional details. The Read ID transaction follows the 1S-1S-1S Transaction Format 0.c (Figure 102).

Table 135 — READ-ID Contents

Byte Address	Function	Comment	Mandatory /Optional
0	Manufacturer ID	Manufacturer Identification (See JEDEC JEP166)	Mandatory
1	Device ID	Manufacturer Defined Device Identification	
2	Device Version 1	Manufacturer Defined Version (byte 1)	
3	Device Version 2	Manufacturer Defined Version (byte2)	
4	Read ID Length	Number of remaining bytes in READ-ID contents	

Table 135 — READ-ID Contents (cont'd)

5	Device Density	(Value + 1) x 32Mb, *for example: Value=7--> (1+7)x32Mb=256Mb*	Optional
6	LPDDR4X_NVM Row Size	0x01 - 32B Row 0x02 - 64B Row others - RESERVED	
7	LPDDR4X_NVM Burst Length (BL), ECC over ECCO, Temperature Sensor, Sub-Bank Architecture, LPDDR READ Protocol optional feature indication	0xxx xx01b - BL16 Supported 0xxx xx10b - BL32 Supported 0xxx xx11b - Both BL16 and BL32 Supported 0xxx x0xxb - ECC over ECCO not supported 0xxx x1xxb - ECC over ECCO supported 0xxx 0xxxb - Temperature Sensor not supported 0xxx 1xxxb - Temperature Sensor supported 0xx0 xxxxb - Sub-Bank Architecture not supported 0xx1 xxxxb - Sub-Bank Architecture supported 000x xxxxb - Legacy JEDEC READ 001x xxxxb - Modified JEDEC READ (without PRE-ACTIVATE) 010x xxxxb - Modified JEDEC READ (with PRE-ACTIVATE) 011x xxxxb - Non-Volatile READ others - RESERVED	
8	tRCD	Value in nanoseconds, (min=0, max=255ns)	
9	SPI- READ FAST Latency	Number of latency clocks at 100MHz	
10	tRC, tRCN	Value in nanoseconds, (min=0, max=255ns)	
11	tSPR	Value in microseconds [4:0] - 5 bit number (n= 0-31) [7:5] - 3 bit order of magnitude (10^m= 10^0 to 10^7) tSPR = n x 10^m (range= 0x10^0 to 31x10^7, 0 to 310s)	
12	Upper Clock Frequency Limit	0000 0000b - 266 MHz 0000 0001b - 533 MHz 0000 0010b - 800 MHz 0000 0011b - 1066 MHz 0000 0100b - 1333 MHz 0000 0101b - 1600 MHz 0000 0110b - 1866 MHz 0000 0111b - 2133 MHz others - RESERVED	
13 - 31	Reserved	values = 0xFF	
32-35	Bank Allocation Register Address	Specified by device manufacturer, MSB in lowest address	
36-39	Temperature Register Address	Specified by device manufacturer, MSB in lowest address optional - 0xFFFFFFFF if not supported	
40-43	Interleaved Operation Register Address	Specified by device manufacturer, MSB in lowest address optional - 0xFFFFFFFF if not supported	
44-47	Interrupt Configuration Register Address	Specified by device manufacturer, MSB in lowest address optional - 0xFFFFFFFF if not supported	
48-51	Interrupt Status Register Address	Specified by device manufacturer, MSB in lowest address optional - 0xFFFFFFFF if not supported	
52+	Reserved	values = 0xFF	

10.3.2.7 Memory Granularity

The writable memory array of an LPDDR4X-NVM memory is divided into two levels of granularity comprised of sectors, and pages. A Sector is the size and alignment (granularity) of an area that can be erased with a single erase operation. A Page is the maximal size and alignment (granularity) of an area that can be altered with a single program operation. The sizes of sectors and pages can be retrieved using the READ SFDP command.

10.3.2.8 Program

The Program command provides a mechanism for programming data into the nonvolatile memory array. The program transaction specifies an initial target address and transfers data bytes into a programming buffer within the memory device. The minimum amount of data to be programmed is a single byte. The maximum number of bytes that can be programmed is the size of the program buffer. Programming is performed by copying data from the program buffer into the corresponding (aligned) page addresses within the NVM array. For example, if the size of the program buffer is 256 bytes, a programming operation can occur between aligned addresses 0x0000 0100 and 0x0000 01FF but a single program operation can not be performed between unaligned addresses 0x0000 0110 and 0x0000 020F. The program buffer size is device specific and can be ascertained by using the READ SFDP operation. The target address selects the starting address within the program buffer for the data to be loaded. Loading data beyond the end of the program buffer has undefined results. Byte locations within the program buffer that are not specified do not alter the corresponding locations in the target NVM page.

The Program operation is supported in both the 1S-1S-1S and 1S-1S-4S protocol modes. The program operation starts with a transfer of a one byte command followed by 4 bytes of address and finally a variable number of data bytes loaded into the program buffer. See Figure 109 — 1S-1S-4S Format 1.c: Command, Address and Write Data. Also see Figure 106 - 1S-1S-1S format 0.g.

10.3.2.9 Erase

The Erase command provides a backward compatible SPI operation for erasing data in a non-volatile memory array. An erase size aligned group of bytes is called a sector. The sector to be erased is selected with an address pointing anywhere within the target sector. Erase sector size is indicated in the SFDP. Upon completion of the erase operation, the all data within the target sector will have transitioned to the 1 state.

In the 1S-1S-1S protocol mode, the controller transfers the one byte command followed and 4 bytes of address. There are no latency or data transfer phases. See Figure 104 — 1S-1S-1S Format 0.e: Command and Address.

10.3.2.10 Read Status Register

The Read status register command provides a backward compatible SPI operation for reading memory device status. This command implicitly selects the eight-bit Status Register to read. If the transaction continues clocking, each additional eight bits represents an updated (dynamic) Status Register value. The format of the status information is device specific. The location and polarity of the Ready/Busy bit within the status register is indicated in the SFDP.

In the 1S-1S-1S protocol mode, the controller transfers the one byte command. Then the memory outputs 1 byte of status data to the controller. The status register content is repeatedly output with additional clocking. See Figure 102 — 1S-1S-1S Format 0.c: Command, 0 Latency Cycles and Read Data.

10.3.2.11 Read Any Register

The Read Any Register command provides for reading an address selected register. The register address map and register formats are memory device specific. The supported address map and formats are indicated in the SFDP. Only a single byte register value is read. If the transaction reads more than one byte, the same (static/identical) register value is repeatedly output.

In the 1S-1S-1S protocol mode, the controller transfers the one byte command followed by 4 bytes of address followed by a configurable number of initial access latency cycles. The memory then transfers 1 or more bytes of register data to the controller. See Figure 105 — 1S-1S-1S Format 0.f: Command, Address, ‘x’ Latency Cycles and Read Data.

10.3.2.12 Write Any Register

The Write Any Register command provides for writing an address selected register. The register address map and register formats are memory device specific. Only a single (eight bit) register is written. If the transaction writes more than one byte, only the first byte received is used to write the target register. The Write Enable command must precede the Write Any Register command.

In the 1S-1S-1S protocol mode, the controller transfers the one byte command followed by 4 bytes of address followed by one byte of data that is written to the target register. See Figure 106 — 1S-1S-1S Format 0.g: Command, Address, and Write Data.

10.4 Transaction Formats

The SPI port on the LPDDR4X-NVM device supports the 1S-1S-1S and 1S-1S-4S transaction formats. The numbers in the format indicate the width of the “data” being transferred during a clock cycle and the “S” indicates that the “data” is being transferred in a single data rate manner. The three elements are indicative of the Command Code, Command Modifier and Data fields of the transaction. Note that in the supported formats, the Command Code and Command Modifier are sent from the host in a 1S-1S “or x1” mode using DQ[0]. Data is transferred between the host and memory in either a x1 (on DQ[1]) or a x4 (on DQ[3:0]) format.

10.4.1 1S-1S-1S Transaction Formats

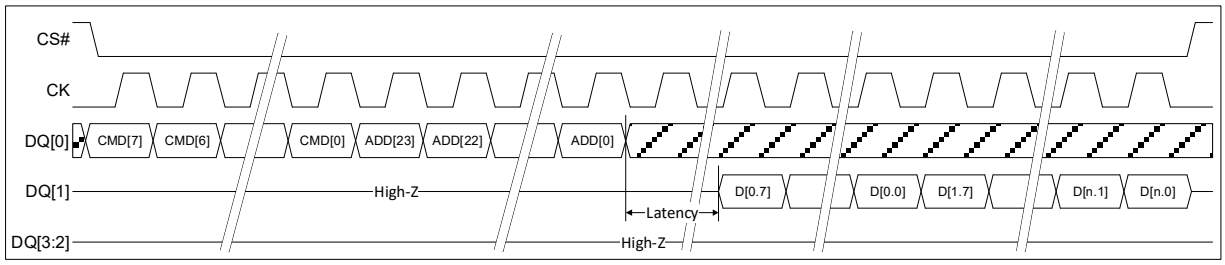

Figure 101 — Transaction Format 0.a (Command, 3-Byte Address, Latency, Data)

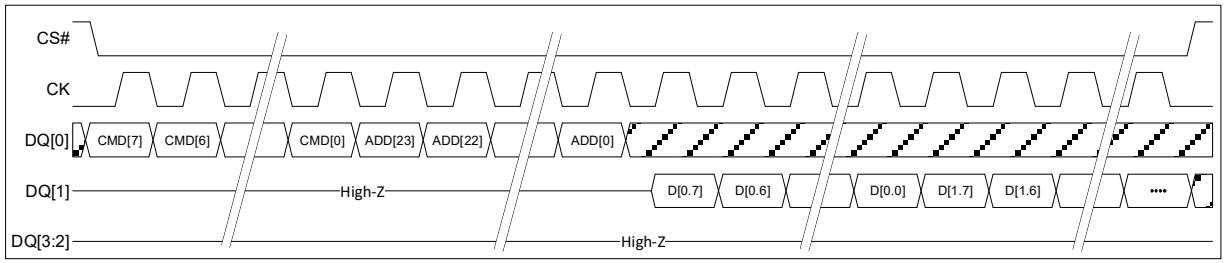

Figure 102 — Transaction Format 0.b (Command, 3-Byte Address, Data)

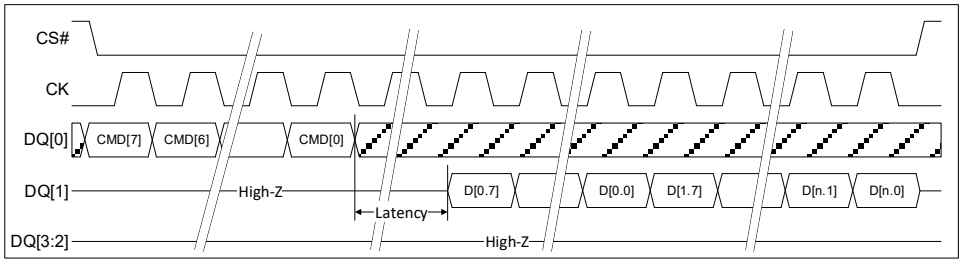

Figure 103 — Transaction Format 0.c (Command, Latency, Data)

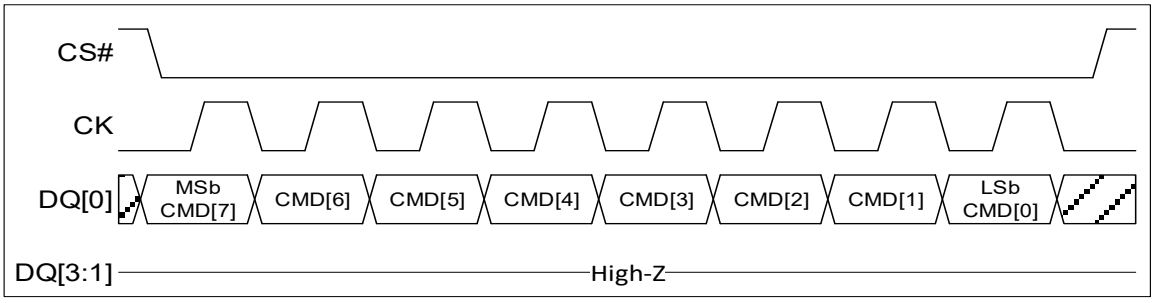

Figure 104 — Transaction Format 0.d (Command)

10.4.1 1S-1S-1S Transaction Formats (cont'd)

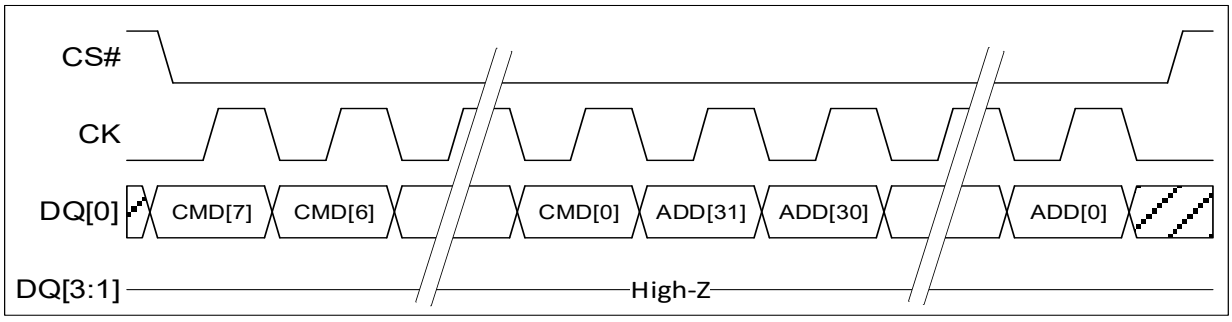

Figure 105 — Transaction Format 0.e (Command, 4-Byte Address)

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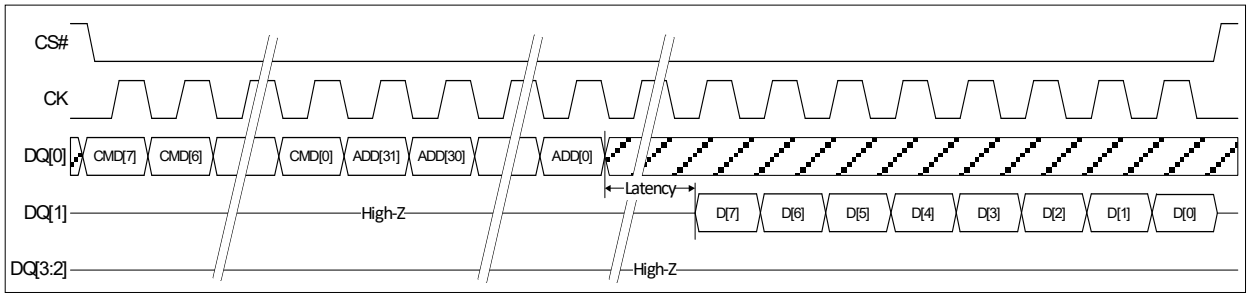

Figure 106 — Transaction Format 0.f (Command, 4-Byte Address, Latency, Data)

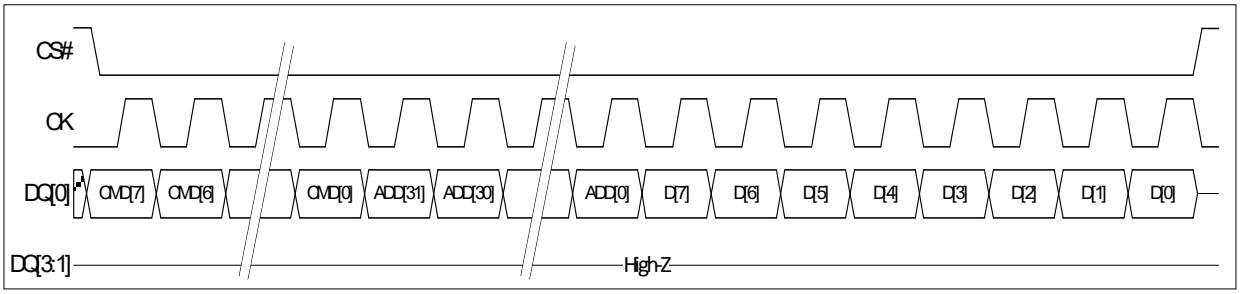

Figure 107 — Transaction Format 0.g (Command, 4-Byte Address, 1-Byte Data)

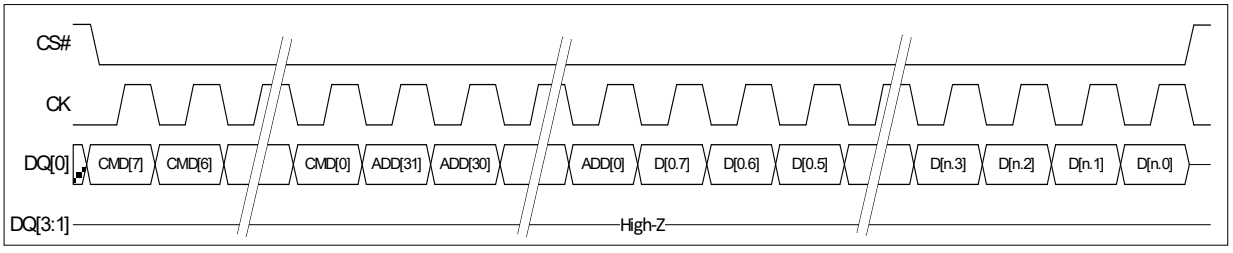

Figure 108 — Transaction Format 0.h (Command, 4-Byte Address, Latency, n-Byte Data)

10.4.2 1S-1S-4S Transaction Formats

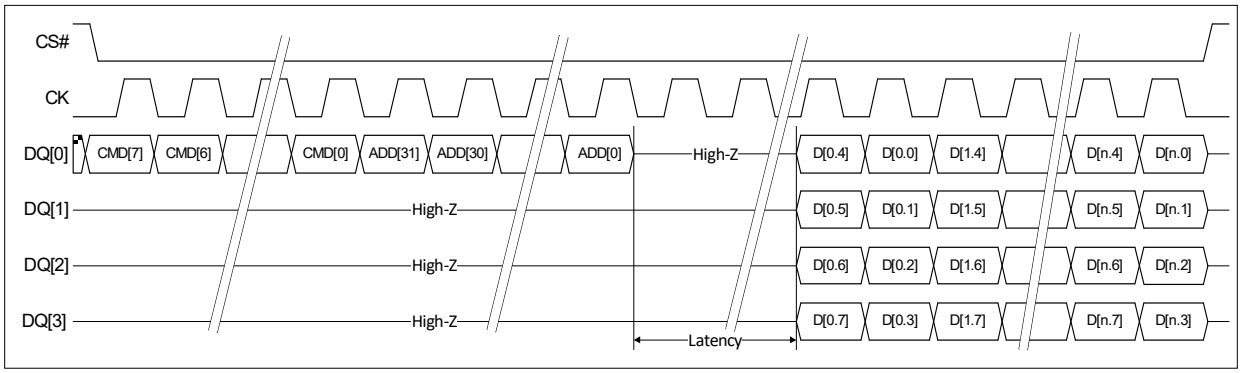

Figure 109 — Transaction Format 1.a (Command, 4-Byte Address, Latency, n-Byte Quad-Data)

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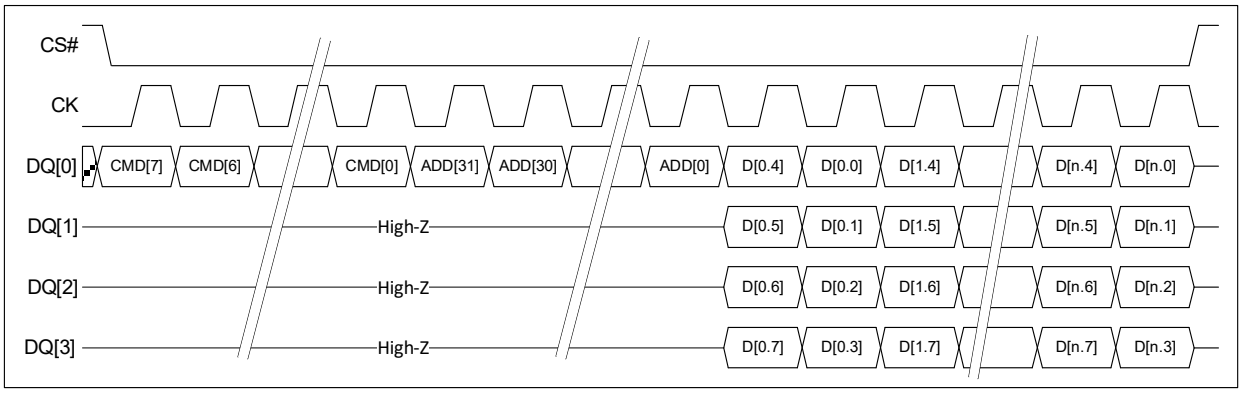

Figure 110 — Transaction Format 1.b (Command, 4-Byte Address, n-Byte Quad-Data)

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10.5 SPI to LPDDR4X User Array Address Translation

The SPI to LPDDR4X address translation assumes that row sizes are either 32B (BL16) or 64B (BL32) long. The intent is to strike a balance between minimal alternations on the host LPDDR controller and reducing the number of (clock) cycles required on the Command/Address bus. Three different LPDDR4X-NVM read sequences are supported and each are described. LPDDR4X-NVM devices must support at least one of the described read sequences.

10.5.1 Legacy JEDEC READ

The legacy JEDEC read transaction is able to be supported by NVM technologies with low latencies. The host controller sends the standard ACT1-ACT2-RD1-CAS2 sequence and data is retrieved from the user array and is ready to output within the RL period. The extended tRCD gap that normally separates the ACTIVE from the READ operations is not required.

Table 136 — Legacy JEDEC READ - SPI to LPDDR4X Address Translation

SPI Address	Legacy JEDEC Address				
	BL16	LPDDR4X CA Bus Command	BL32	LPDDR4X CA-Bus Command	Notes
A0	-		-		
A1	-		-		
A2	-		-		
A3	C2	CAS2	C2	CAS2	2
A4	C3		C3		
A5	R0		C4		
A6	R1		R0		
A7	R2		R1		
A8	R3		R2		
A9	R4		R3		
A10	R5	RD1	R4	RD1	
A11	R6	ACT2	R5	ACT2	
A12	R7		R6		
A13	R8		R7		
A14	R9		R8		
A15	R10		R9		
A16	R11		R10		
A17	R12		R11		
A18	R13		R12		
A19	R14		R13		
A20	R15		R14		
A21	R16	ACT1	R15	ACT1	
A22	R17		R16		
A23	R18		R17		
A24	R19		R18		
A25	R20		R19		
A26	R21		R20		
A27	R22		R21		
A28	R23	ACT2	R22	ACT2	
A29	BA0	ACT1/RD1	BA0	ACT1, RD1	3
A30	BA1		BA1		
A31	BA2		BA2		
Max Density	***32 Gb***		***32 Gb***		

NOTE 1 32 Gb (4 GB) is the highest density supported by the 32b SPI addressing.

NOTE 2 Larger row sizes would be accommodated by increasing the column bits and reducing the row bits. The maximum density supported will not change.

NOTE 3 The LPDDR4X BA bits are assigned to the three highest order SPI address bits for a given density. For example, if the device has a 256Mb density, the BA0, BA1 and BA2 bits would correspond to SPI addresses A22, A23 and A24 respectively.

10.5.2 Modified JEDEC READ

The Modified JEDEC READ moves all of the row addressing into the ACT1-ACT2 transactions and allows for the extended tRCD that is required to support longer latency NVM technologies. The LPDDR4X-NVM host controller will need to reduce the column addressing supported in the RD1-CAS2 cycles and move these bits into the ACT1-ACT2 cycles. This reduction of the addressing performed during the RD1-CAS2 limits the densities supported in this mode of operation. The PRE-ACTIVATE command (PRE) has been added as an optional feature to specify additional high-order ROW bits. These additional ROW address bits support densities up to 32 Gb.

Table 137 — Modified JEDEC READ - SPI to LPDDR4X Address Translation (64 Byte Row Size)

SPI Address	Modified JEDEC Address		
	BL16 and BL32 supported	LPDDR4X-NVM CA-Bus Command	Notes
A0	-		
A1	-		
A2	-		
A3	C2	CAS2	1
A4	C3		
A5	C4		
A6	R0	ACT2	
A7	R1		
A8	R2		
A9	R3		
A10	R4		
A11	R5		
A12	R6		
A13	R7		
A14	R8		
A15	R9		
A16	R10	ACT1	
A17	R11		
A18	R12		
A19	R13		
A20	R14		
A21	R15		
A22	R16		
A23	R17	ACT2	
A24	R18		
A25	R19	PRE	3
A26	R20		
A27	R21		
A28	R22		
A29	BA0	PRE, ACT1, RD1	2, 3
A30	BA1		
A31	BA2		
Max Density: 2 Gb (without PRE-ACTIVATE) or 32 Gb (with PRE-ACTIVATE)			

NOTE 1 Larger row sizes would be accommodated by increasing the column bits in the RD1 and CAS2 cycles. The maximum density supported would increase accordingly. However, the max density would be capped due to the 32 bit SPI addressing.

NOTE 2 The LPDDR4X BA bits are assigned to the three highest order SPI address bits for a given density. For example, if the device has a 256 Mb density, the BA0, BA1, and BA2 bits would correspond to SPI addresses A22, A23, and A24 respectively.

NOTE 3 Device densities of 2 Gb and below will ignore PRE-ACTIVATE commands.

10.5.2 Modified JEDEC READ (cont'd)

Table 138 — Modified JEDEC READ - SPI to LPDDR4X Address Translation (32 Byte Row Size)

SPI Address	Modified JEDEC Address		
	Only BL16 Supported	LPDDR4X-NVM CA-Bus Command	Notes
A0	-		
A1	-		
A2	-		
A3	C2	CAS2	1
A4	C3		
A5	R0	ACT2	
A6	R1		
A7	R2		
A8	R3		
A9	R4		
A10	R5		
A11	R6		
A12	R7		
A13	R8		
A14	R9		
A15	R10	ACT1	
A16	R11		
A17	R12		
A18	R13		
A19	R14		
A20	R15		
A21	R16		
A22	R17	ACT2	
A23	R18		
A24	R19	PRE	3
A25	R20		
A26	R21		
A27	R22		
A28	R23		
A29	BA0	PRE, ACT1, RD1	2, 3
A30	BA1		
A31	BA2		
Max Density: 1 Gb (without PRE-ACTIVATE), 32 Gb (with PRE-ACTIVATE)			

NOTE 1 Larger row sizes would be accommodated by increasing the column bits in the RD1 and CAS2 cycles. The maximum density supported would increase accordingly. However, the max density would be capped due to the 32 bit SPI addressing.

NOTE 2 The LPDDR4X BA bits are assigned to the three highest order SPI address bits for a given density. For example, if the device has a 256 Mb density, the BA0, BA1, and BA2 bits would correspond to SPI addresses A22, A23, and A24 respectively.

NOTE 3 Device densities of 1 Gb and below will ignore PRE-ACTIVATE commands.

10.5.3 Non-Volatile READ (NVR)

The NVR transactions were developed to reduce the read request footprint on the LPDDR4X Command/ Address bus. The legacy JEDEC READ consists of an ACT1-ACT2-RD1-CAS2 sequence that takes eight clock cycles. The NVR READ implements a shorter NVR1-NVR2 sequence taking only four clock cycles. The shorter NVR sequence has a significant impact on overall latency when performing a READ operation (especially from an idle state). The NVR sequence doesn't specify a starting column address and data is always output starting at the beginning of the burst length.

Table 139 — NVR READ - SPI to LPDDR4X Address Translation

SPI Address		Non-Volatile Read Address			
BL16	**BL32**	**BL16**	**BL32**	**LPDDR4X-NVM CA- Bus Command**	**Notes**
A0	A0	-	-		
A1	A1	-	-		
A2	A2	-	-		
A3	A3	-	-		
A4	A4	-	-		
A5	A5	R0	-	NVR2	
A6	A6	R1	R0		
A7	A7	R2	R1		
A8	A8	R3	R2		
A9	A9	R4	R3		
A10	A10	R5	R4		
A11	A11	R6	R5		
A12	A12	R7	R6		
A13	A13	R8	R7		
A14	A14	R9	R8		
A15	A15	R10	R9		
A16	A16	R11	R10		
A17	A17	R12	R11	NVR1	2
A18	A18	R13	R12		
A19	A19	R14	R13		
A20	A20	R15	R14		
A21	A21	R16	R15		
A22	A22	R17	R16		
A23	A23	R18	R17		
A24	A24	R19	R18		
A25	A25	R20	R19		
A26	A26	R21	R20		
A27	A27	R22	R21		
-	A28	-	R22		
Max Density		***2 Gb***	***4 Gb***		

NOTE 1 NVR transactions are limited to a 2 Gb (BL16) and 4 Gb (BL32) maximum density.
NOTE 2 The three highest order row bits for a given density are used as BA[2:0].

10.6 SPI Registers

Only two (byte wide) SPI registers are mandatory on an LPDDR4X-NVM device. Device manufacturers may add additional registers to support manufacturer specific operation. All registers are defined in this specification are readable and writable.

Table 140 — SPI Registers

Register Name	Register Address (32b)	
Status Register	Defined by Read ID	Mandatory
Bank Allocation Register	Defined by Read ID	
Temperature Register	Defined by Read ID	Optional
Interleaved Operation Register	Defined by Read ID	
Interrupt Infrastructure Register(s)	Defined by Read ID	

10.6.1 Status Register (SR)

The Status Register is mandatory and is required primarily to support Program and Erase operations with the Ready/Busy bit. Other information in the Status Register are manufacturer specific. The remainder of the Status Register bit functionality is at the discretion of the manufacturer.

10.6.2 Bank Allocation Register (BAR)

The Bank Allocation Register is mandatory and is used to determine whether a bank is accessible via the LPDDR4X port or over the SPI port. Each of the eight banks is controlled by the corresponding bit in the BAR (Bank 0 controlled by BAR.0). If a BAR bit is 0, the corresponding bank is accessible from the SPI port. If a BAR bit is 1, the corresponding bank is accessible from the LPDDR4X port.

10.6.3 Temperature Register

The Temperature Register is used to control the optional temperature sensor on the LPDDR4X-NVM device. The functionality is fully described in Section 4.19.

10.6.4 Interleaved Operation Register

The Interleaved Operation Register is used to enable or disable Interleaved Program and Interleaved Read operations that are required by the ECC over ECCO functionality. The ECC over ECCO functionality is described in Section 10.7.

10.6.5 Interrupt Infrastructure Register(s)

The Interrupt Infrastructure Registers are used to manage interrupt activities on the LPDDR4X-NVM device.

10.7 ECC over ECCO Set-Up Operations

The LPDDR4X-NVM device (optionally) implements an end-to-end ECC strategy. This feature is supported by programming a User ECC syndrome value while programming User Data over the SPI interface. During LPDDR4X-NVM READ transactions, both the (previously programmed) User Data and User ECC syndrome are retrieved by the host controller. The host controller then validates the User ECC syndrome given the retrieved User Data. The host controller determines the appropriate action if the ECC syndrome does not match expectations.

The SPI READ and PROGRAM operations can be performed in either a legacy or an “interleaved” fashion. The interleaved operations intersperse User Data and the User ECC metadata within the READ and PROGRAM operations. Interleaved operations are enabled or disabled with a control bit in a configuration register.

10.7.1 SPI Interleaved PROGRAM Operation

The Interleaved Program allows the user to specify the bits that are output on the LPDDR4X ECCO output during a READ operation. The Interleaved Program operation is performed over the SPI bus as a standard Program operation except that ECC bits are interleaved with the data to be programmed. For every eight bytes of data, a ninth byte of User ECC information is loaded into the Program Buffer. The User ECC value is generated by the host system and is intended to be used by the host LPDDR4X controller to determine whether an ECC error has occurred during an LPDDR4X READ transaction. Note that the Interleaved Program operation expects multiples of 32 bytes of User Data to be programmed aligned on 32 byte address boundaries. The Interleaved Program sequence is described in Figure 112.

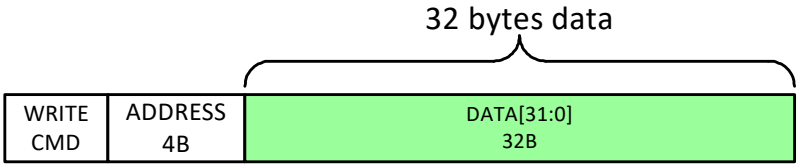

Figure 111 — Legacy Programming Sequence (Interleaved Operations Disabled)

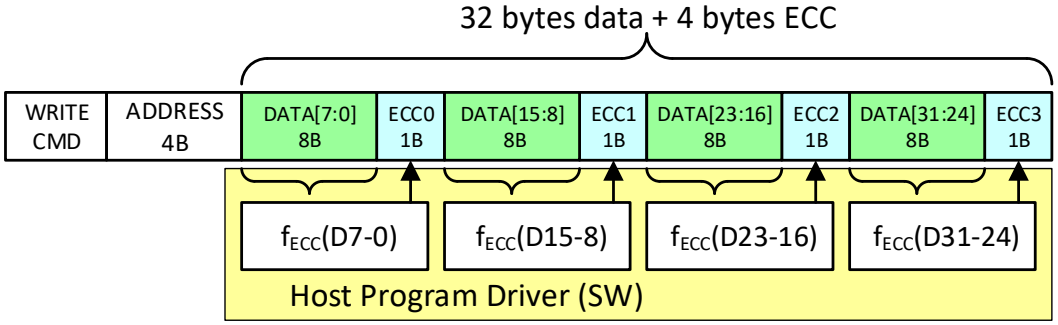

Figure 112 — Interleaved Programming Sequence (Interleaved Operations Enabled)

10.7.2 SPI Interleaved READ Operation

The Interleaved READ allows both User Data and the associated User ECC to be retrieved over the SPI port. The same eight byte User Data and one byte User ECC interleaving output during the Fast Read transactions when Interleaved Operations are enabled. The Interleaved Read sequence is described in Figure 113.

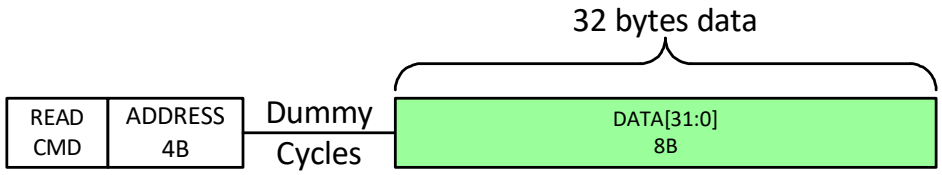

Figure 113 — Legacy Read Sequence (Interleaved Operations Disabled)

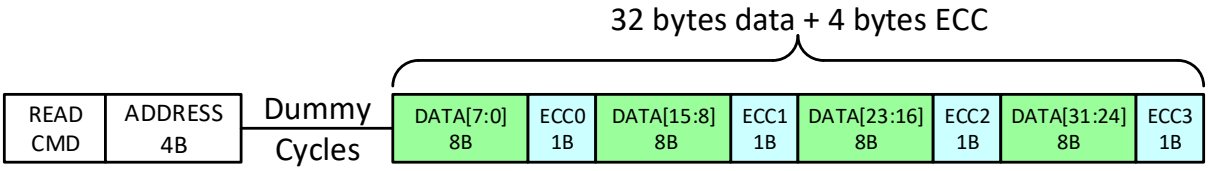

Figure 114 — Interleaved Read Sequence (Interleaved Operations Enabled)

10.7.3 ECC to ECCO Bit Mapping During LPDDR4X READ Transactions

Table 142 describes how the bits and bytes that were programmed on the SPI port are output on the LPDDR4X-NVM port during a READ transaction. The table assumes that ECC over ECCO is enabled. The table describes a BL16 (32B) read burst. Note how each 8-bit ECC value corresponds with each 8-byte User Data values that were previously programmed. There is a 1 to 1 correspondence between the Table 142 bits and bytes and the way User Data and User ECC is programmed as shown in Figure 112.

Table 141 — READ Transaction SPI to LPDDR4X Data Mapping (BL32)

LPDDR READ Beat	LPDDR4X Output Signals During READ			
	DQ[15:8]	ECCO[1]	DQ[7:0]	ECCO[0]
1	DATA 1	ECC 0.1	DATA 0	ECC 0.0
2	DATA 3	ECC 0.3	DATA 2	ECC 0.2
3	DATA 5	ECC 0.5	DATA 4	ECC 0.4
4	DATA 7	ECC 0.7	DATA 6	ECC 0.6
5	DATA 9	ECC 1.1	DATA 8	ECC 1.0
6	DATA 11	ECC 1.3	DATA 10	ECC 1.2
7	DATA 13	ECC 1.5	DATA 12	ECC 1.4
8	DATA 15	ECC 1.7	DATA 14	ECC 1.6
9	DATA 17	ECC 2.1	DATA 16	ECC 2.0
10	DATA 19	ECC 2.3	DATA 18	ECC 2.2
11	DATA 21	ECC 2.5	DATA 20	ECC 2.4
12	DATA 23	ECC 2.7	DATA 22	ECC 2.6
13	DATA 25	ECC 3.1	DATA 24	ECC 3.0
14	DATA 27	ECC 3.3	DATA 26	ECC 3.2
15	DATA 29	ECC 3.5	DATA 28	ECC 3.4
16	DATA 31	ECC 3.7	DATA 30	ECC 3.6
17	DATA 33	ECC 4.1	DATA 32	ECC 4.0
18	DATA 35	ECC 4.3	DATA 34	ECC 4.2
19	DATA 37	ECC 4.5	DATA 36	ECC 4.4
20	DATA 39	ECC 4.7	DATA 38	ECC 4.6
21	DATA 41	ECC 5.1	DATA 40	ECC 5.0
22	DATA 43	ECC 5.3	DATA 42	ECC 5.2
23	DATA 45	ECC 5.5	DATA 44	ECC 5.4
24	DATA 47	ECC 5.7	DATA 46	ECC 5.6
25	DATA 49	ECC 6.1	DATA 48	ECC 6.0
26	DATA 51	ECC 6.3	DATA 50	ECC 6.2
27	DATA 53	ECC 6.5	DATA 52	ECC 6.4
28	DATA 55	ECC 6.7	DATA 54	ECC 6.6
29	DATA 57	ECC 7.1	DATA 56	ECC 7.0
30	DATA 59	ECC 7.3	DATA 58	ECC 7.2
31	DATA 61	ECC 7.5	DATA 60	ECC 7.4
32	DATA 63	ECC 7.7	DATA 62	ECC 7.6

NOTE 1 With ECCO enabled.
NOTE 2 LPDDR4X DQ bit ordering ([15:8] and [7:0]) for each byte lane follows SPI bit ordering ([7:0]).

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10.7.3 ECC to ECCO Bit Mapping During LPDDR4X READ Transactions (cont'd)

Table 142 — READ Transaction SPI to LPDDR4X Data Mapping (BL16)

LPDDR READ Beat	LPDDR4X Output Signals During READ			
	DQ[15:8]	ECCO[1]	DQ[7:0]	ECCO[0]
1	DATA 1	ECC 0.1	DATA 0	ECC 0.0
2	DATA 3	ECC 0.3	DATA 2	ECC 0.2
3	DATA 5	ECC 0.5	DATA 4	ECC 0.4
4	DATA 7	ECC 0.7	DATA 6	ECC 0.6
5	DATA 9	ECC 1.1	DATA 8	ECC 1.0
6	DATA 11	ECC 1.3	DATA 10	ECC 1.2
7	DATA 13	ECC 1.5	DATA 12	ECC 1.4
8	DATA 15	ECC 1.7	DATA 14	ECC 1.6
9	DATA 17	ECC 2.1	DATA 16	ECC 2.0
10	DATA 19	ECC 2.3	DATA 18	ECC 2.2
11	DATA 21	ECC 2.5	DATA 20	ECC 2.4
12	DATA 23	ECC 2.7	DATA 22	ECC 2.6
13	DATA 25	ECC 3.1	DATA 24	ECC 3.0
14	DATA 27	ECC 3.3	DATA 26	ECC 3.2
15	DATA 29	ECC 3.5	DATA 28	ECC 3.4
16	DATA 31	ECC 3.7	DATA 30	ECC 3.6

NOTE 1 With ECCO enabled.
NOTE 2 LPDDR4X DQ bit ordering ([15:8] and [7:0]) for each byte lane follows SPI bit ordering ([7:0]).

11 Interrupt Output (INT_n)

The Interrupt signal (INT_n) is an open-drain output that is used by the memory to indicate to the host that an internal event has occurred. The memory manufacturer determines what internal events are able to cause the Interrupt Output to be driven to the active (LOW) state. The behavior of the INT_n output is controlled by the following configuration settings:

1. An Interrupt Configuration Register that is used to enable a particular interrupt source
2. An Interrupt Status Register (ISR) that will indicate what source caused an interrupt event. Note that these register bits are “sticky.” Initially in the “cleared” state, an ISR bit is “set” if the associated interrupt is enabled when the indicated event occurs. The set bits can only be cleared with an explicit Write Any Register operation to the ISR.

Any number of internal events can be used to trigger an interrupt. Historically, ECC failures are an example from the NVM world that trigger an interrupt. The LPDDR4X-NVM spec only requires a single interrupt event to be supported. An array access that violates the bank allocation indication in the Bank Allocation Register (BAR) is the only mandatory interrupt source that must be supported (see Table 143).

The time taken between an interrupt event and when the INT_n output is asserted is the Interrupt Output Time (t_IOT, see Figure 115).

The implementation details of the interrupt infrastructure is manufacturer specific.

Table 143 — LPDDR4X-NVM Interrupt Sources

Mandatory Interrupt Sources
Bank Allocation Register Violation
Optional Interrupt Sources
Single Error Correction During Array READ Access
Dual Error Detect During Array READ Access
Illegal LPDDR4X Bus Command
Illegal SPI Bus Command
.... others (manufacturer specific)

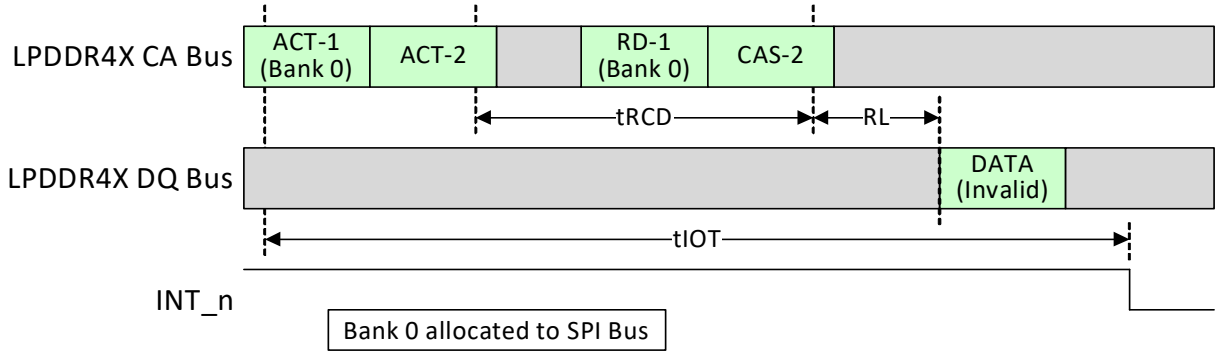

Figure 115 — Example Output Response Time (Bank Allocation Register READ Access Failure)

Table 144 — Interrupt Output Time

Parameter	Symbol	MIN	MAX	Unit
Interrupt Output Time	t_{IOT}	-	100	ns

Annex A — (Informative) Differences between Document Revisions

A.1 JESD326-4A compared to its Predecessor JESD326-4 (November 2024)

Page 16: TBD changed to MSV in Table 6, changed NOTE 1 as defined in Table 135

Page 41: TBD changed to MSV in Table 53, changed NOTE 3 as defined in Table 135

Page 52: Added Figure 29 - Rank to Rank Circuit Arrangement

Page 52: Added Table 61 - Rank to Rank Transaction Timings (with WRITE DQ_ODT off)

Page 52: Added Table 62 - Rank to Rank Transaction Timings (with WRITE DQ_ODT on)

Page 77: Removed the sentence "The component level characterization method is TBD" from Clause 4.13 above Table 69

Page 117: Added VDDQ_SPI option for 1.1V added to Table 98 - Recommended DC Operating Conditions

Page 155: Modified Table 135 READ-ID Contents

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Standard Improvement Form **JEDEC Standard JESD326-4A**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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