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PMIC5120 Power Management IC Standard

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(From JEDEC Board Ballot JCB-25-21, formulated under the cognizance of the JC-40.1 subcommittee on Digital Logic Families and Applications, item 336.18E).

1 PMIC5120 Power Management IC Standard

1.1 Scope

This standard defines the specification of interface parameters, signaling protocols, and features for PMIC devices used for memory module applications. The designation PMIC5120 refers to the device specified by this document.

The purpose is to provide a standard for the PMIC5120 device for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Unless otherwise noted in the document, any illegal operation is not allowed and device operation is not guaranteed.

NOTE: The designation PMIC5120 refers to a portion of the part number designation of a series of commercial logic devices common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

1.2 Device Standard

1.2.1 Description

The PMIC5120 is designed for typical DDR5 SODIMM, UDIMM, CSODIMM, and CUDIMM. The PMIC features three step down switching regulators and two LDO regulators.

The PMIC is designed to support approximately TBD Watts of power. The PMIC is powered from VIN_Bulk input for the entire PMIC including the switching regulators and LDO output regulators. The PMIC supports selectable interface (I^2C or I3C Basic) to fit various application environment. The PMIC device is intended to operate up to 12.5 MHz on a 1.0 V I3C Basic bus or up to 1 MHz on 1.0 V to 3.3 V I^2C bus.

1.2.2 Common Feature Summary

Table 1 — PMIC Device Type Current Capability per Phase

Device Type	SWA	SWB	SWC	Unit
PMIC5100[1]	4	4	1	A
PMIC5120	6	6	2	A

NOTE 1 For reference.

- VIN_Bulk input supply range: 4.25 V to 5.5 V
- Three step down switching regulators: SWA, SWB and SWC
- Programmable dual phase and single phase regulator for SWA and SWB
- 2 LDO regulators: VOUT_1.8V, VOUT_1.0V

1.2.2 Common Feature Summary (cont'd)

- Error injection capability
- Persistent error log registers
- Secure mode and programmable mode of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Output power good status reporting mechanism
- VIN_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection features: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable (MTP) Non-Volatile Memory
- Programmable and DIMM specific registers for customization
- General Status Interrupt (GSI) function
- Flexible Open Drain IO (I^2C) and Push Pull (I3C Basic) IO support
- Flexible mechanism to enable switch regulators (w/ VR_EN pin or VR Enable command on I^2C or I3C Basic interface)
- Quiescent Power State (P1 State)

2 PMIC Pin List and Package

2.1 Pin List

Table 2 — PMIC Pin Description

Pin Count	Pin Name	Type	Description
3	VIN_Bulk_A VIN_Bulk_B VIN_Bulk_C	I	5 V power input supply to the PMIC for SWA, SWB and SWC respectively. All three VIN_Bulk input pins must be connected to the 5 V input supply even if one or more output regulators are not intended to be used.
1	VIN	I	5 V power input supply to the PMIC for analog circuits.
2	PGND	PWR	Power Ground. Connects to DIMM ground plane.
1	AGND	PWR	Analog Ground. Connects to DIMM ground plane.
1	SWA	O	Switch node A output buck regulator. This pin connects to L1 power inductor. In single phase regulator mode of operation, the SWA output must not be connected to SWB output even if they are configured to same exact output voltage. In dual phase regulator mode of operation, the SWA and SWB outputs are connected.
1	SWB	O	Switch node B output buck regulator. This pin connects to L2 power inductor. In single phase regulator mode of operation, the SWA output must not be connected to either SWB output even if they are configured to same exact output voltage. In dual phase regulator mode of operation, the SWA and SWB outputs are connected.
1	SWC	O	Switch node C output buck regulator. This pin connects to L3 power inductor.
1	BOOT_SWA	PWR	Bootstrap node for SWA high side NMOS driver. This pin connects to SWA through a high quality capacitor.
1	BOOT_SWB	PWR	Bootstrap node for SWB high side NMOS driver. This pin connects to SWB through a high quality capacitor.
1	BOOT_SWC	PWR	Bootstrap node for SWC high side NMOS driver. This pin connects to SWC through a high quality capacitor.
1	SWA_FB_P	I	Switch node A output buck regulator positive feedback. In single phase or dual phase regulator mode of operation, this pin connects to DIMM power plane load.
1	SWB_FB_P	I	Switch node B output buck regulator positive feedback. In single phase regulator mode of operation, this pin connects to DIMM power plane load. In dual phase regulator mode of operation, this pin is connected to GND.
1	SWC_FB_P	I	Switch node C output buck regulator positive feedback. This pin connects to DIMM power plane load.
1	VOUT_1.8V	O	1.8V LDO Output
1	VOUT_1.0V	O	1.0V LDO Output

Table 2 — PMIC Pin Description (cont'd)

Pin Count	Pin Name	Type	Description
1	PWR_GOOD	IO	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceeds the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin transitions from high to low. The LDO outputs shall remain on.
1	VR_EN	I	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
1	SCL	I	Clock input for I^2C and I3C Basic bus management interface.
1	SDA	IO	Data input and output for I^2C and I3C Basic bus management interface.
1	GSI_n	O	General Status Interrupt. Open Drain Output. This PMIC asserts this pin low to communicate any or more events to host. This pin stays asserted until the appropriate registers are explicitly cleared and event is no longer present.
1	PID	I	PMIC ID pin for I^2C and I3C Basic bus.
4	TC/GND		Thermal connection to GND. This pin is connected to GND on the PCB and may be connected to GND on the die.

2.2 Package

2.2.1 Flip Chip QFN Package (3 mm x 4 mm)

- 28 pins (24 Functional pins; 4 dummy corner pins)
- 3 mm x 4 mm Maximum Package Outline

2.2.2 Mechanical Drawing

The drawing and dimensions for 28 pins FC QFN package are shown below as reference only. This package is defined in JEDEC standard MO-339A.

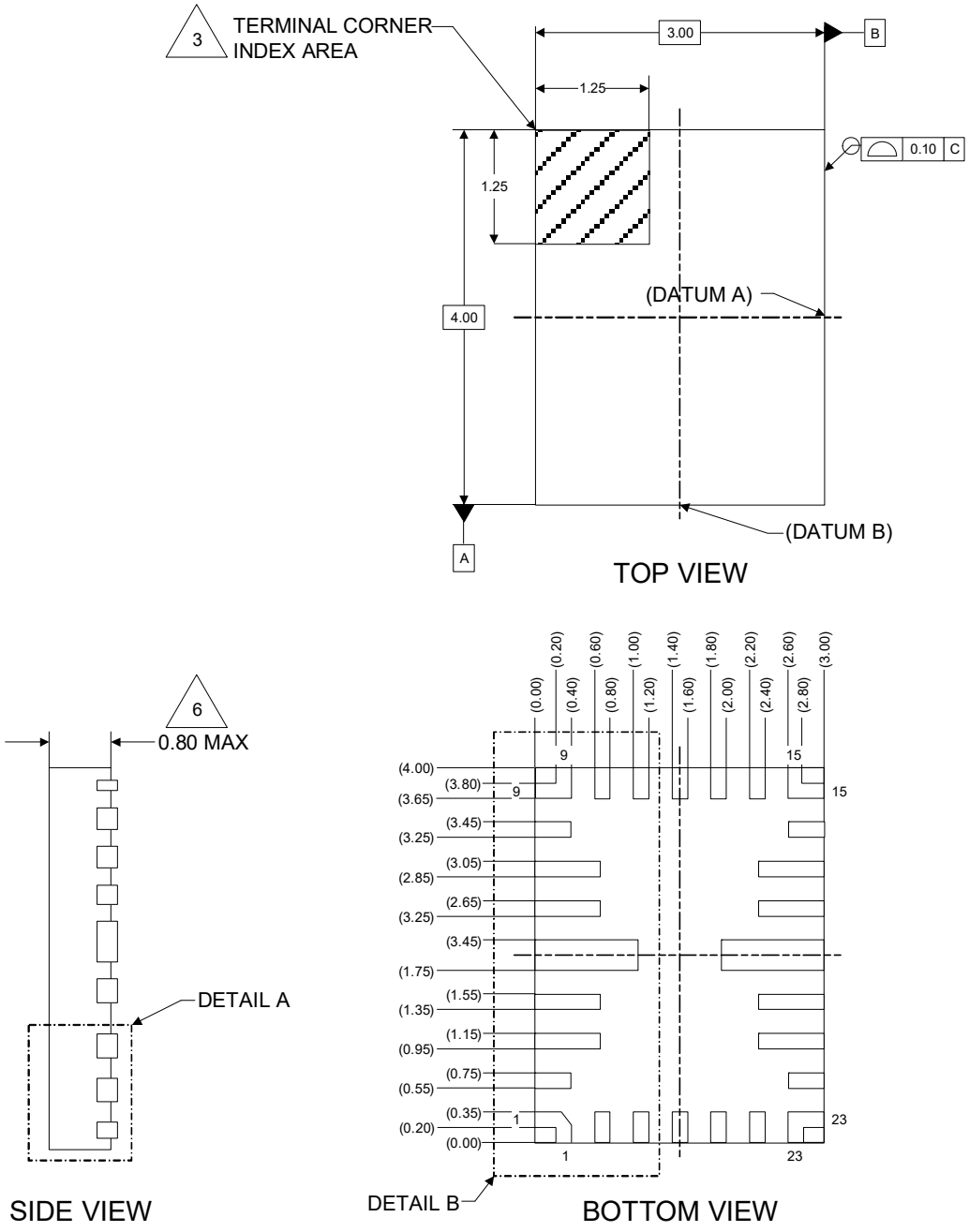


Figure 1 — QFN Package Mechanical Drawing

2.2.2 Mechanical Drawing (cont'd)

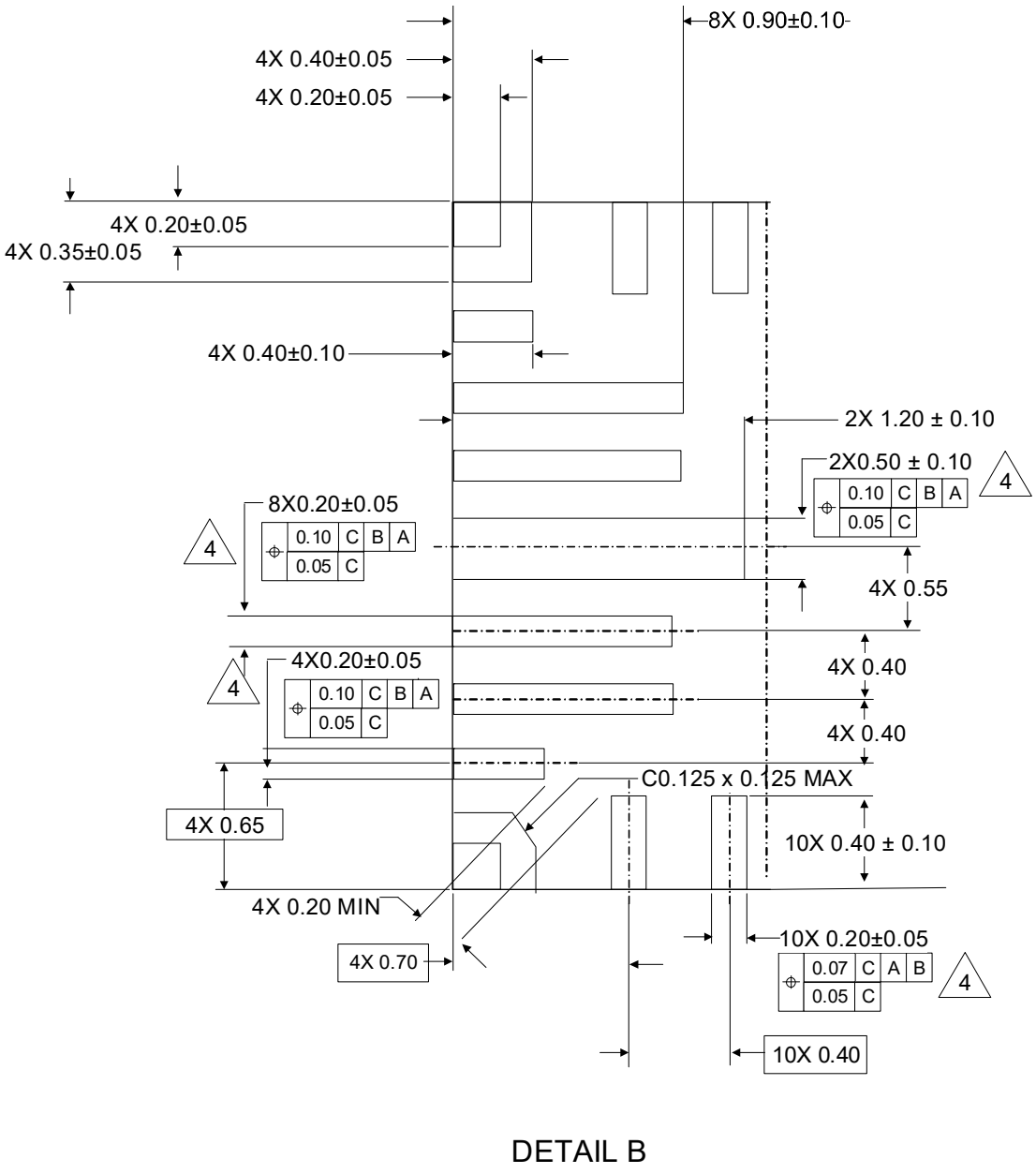


Figure 2 — QFN Package Mechanical Drawing - Detail Dimensions

2.2.2 Mechanical Drawing (cont'd)

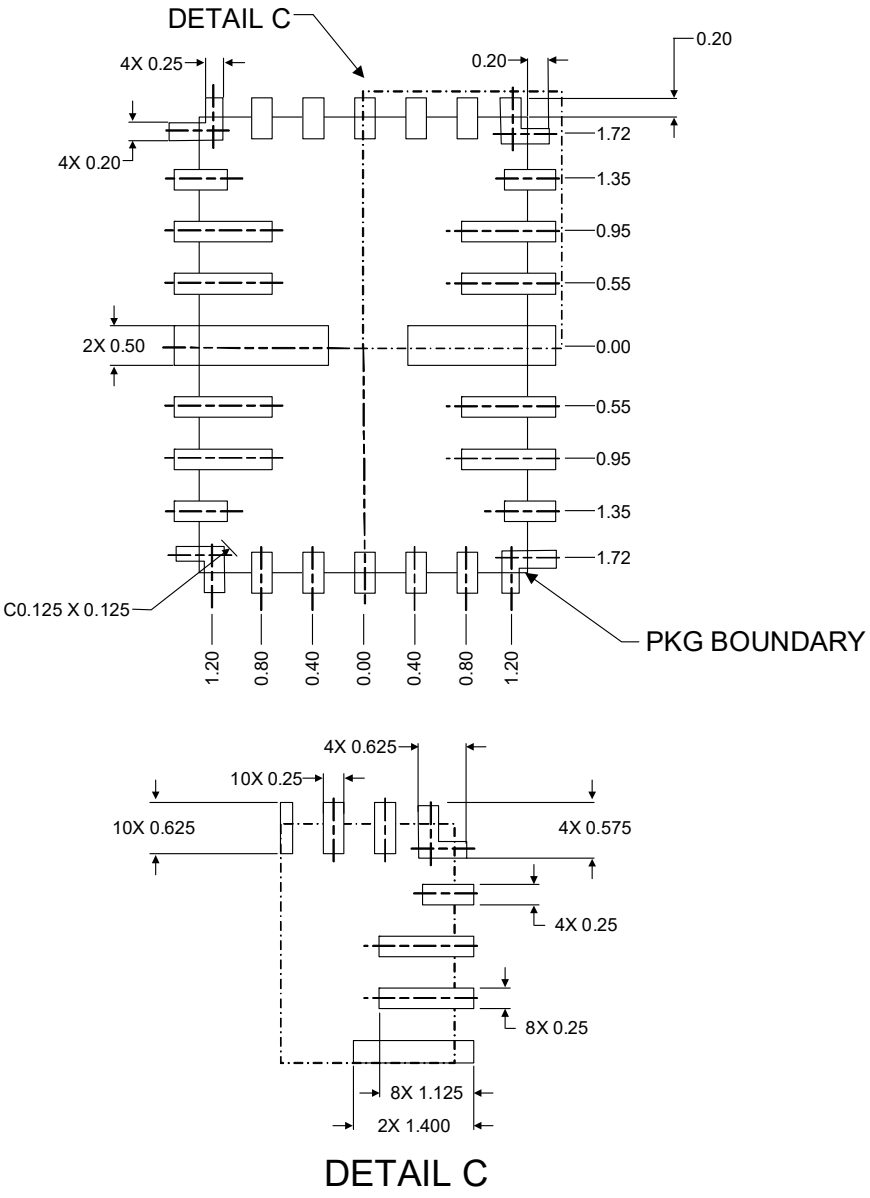


Figure 3 — Recommended PCB Pattern (Units: mm)

2.2.3 Pinout (FC QFN Package - 28 Pins)

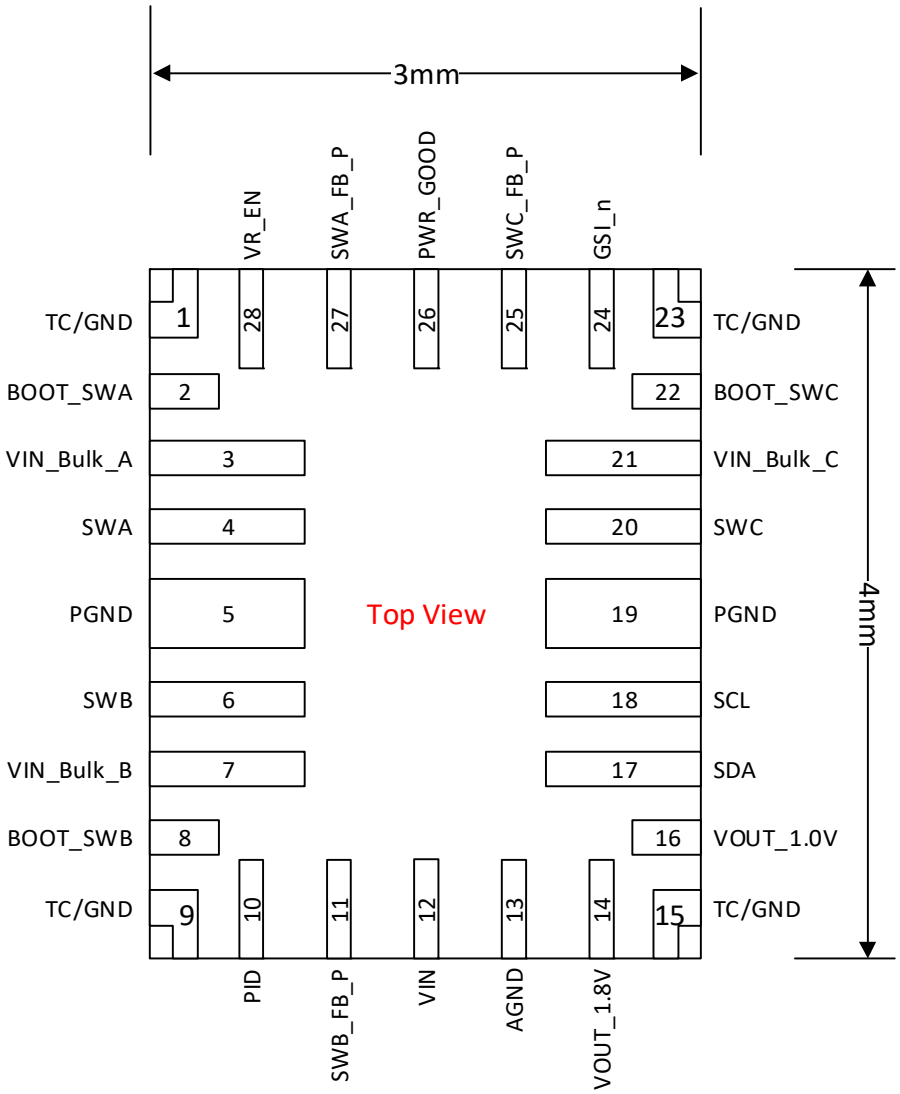


Figure 4 — FC QFN Package Pinout - 28 Pins; Top View

2.2.3 Pinout (FC QFN Package - 28 Pins) (cont'd)

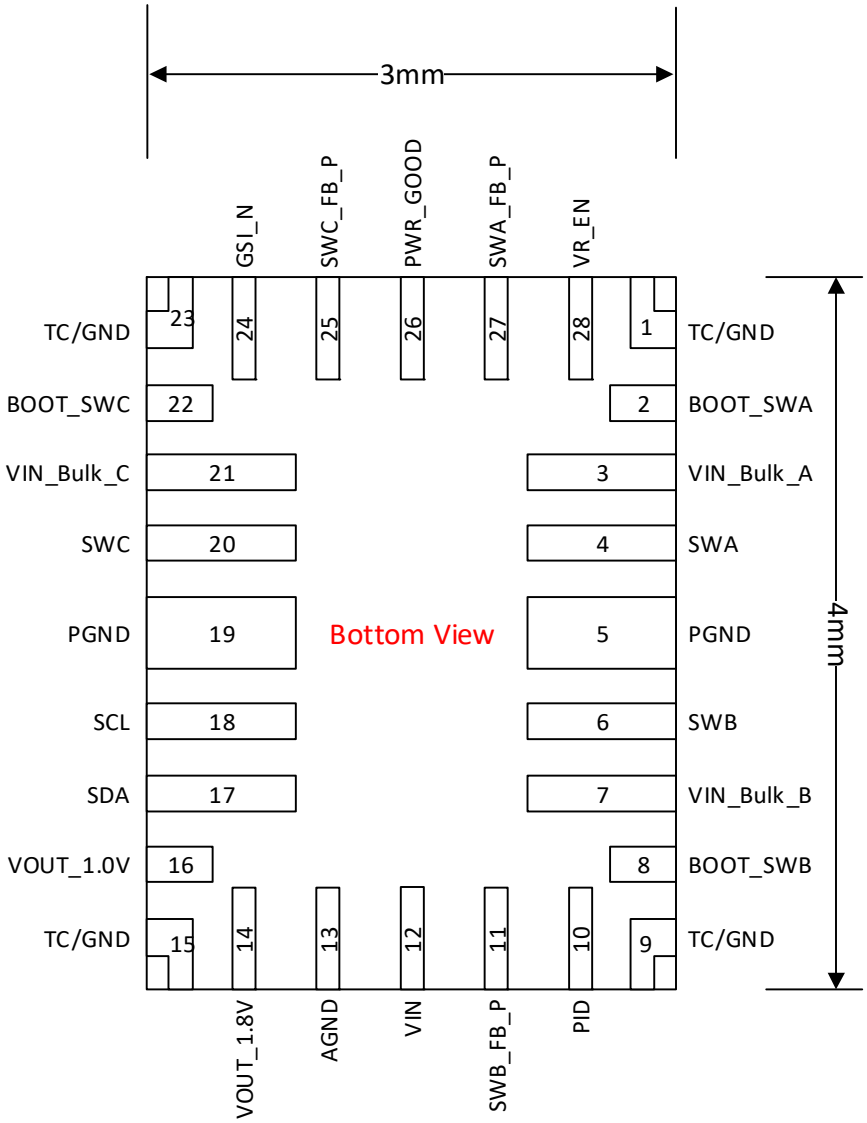


Figure 5 — FC QFN Package Pinout - 28 Pins; Bottom View

3 Electrical Characteristics

3.1 Input Supply Electrical Characteristics

Table 3 — Input Supply DC + AC Specification[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bulk Input Supply Voltage	VIN_Bulk	4.25	5.0	5.5	V	2
Bulk Input Supply Maximum AC Voltage	VIN_Bulk_AC	-	-	6.5	V	
Maximum voltage on VIN_Bulk during soft stop	VIN_Bulk_Soft_Stop_Max	-	-	5.55	V	3,4,5
Bulk Input Supply Voltage Ramp Up Rate	VIN_Bulk_Ramp_Up	0.1	-	3.0	V/ms	6
Bulk Input Supply Voltage Ramp Down Rate	VIN_Bulk_Ramp_Down	0.5	-	1.0	V/ms	7
Bulk Input Supply Voltage Start Up Overshoot	VIN_Bulk_OS_STARTUP	-	-	TBD	V*µs	8
Maximum Input Current for VIN_Bulk Input Supply Voltage	I_{VIN_Bulk}	-	-	3.5	A	9
VIN_Bulk Input Quiescent Current	$I_{VIN\_Bulk\_Quiescent}$	-	-	25	µA	10
VIN_Bulk Input Idle Current	$I_{VIN\_Bulk\_Idle}$	-	-	TBD	µA	11

NOTE 1 Input supply is referred in this table are VIN_Bulk and VIN.

NOTE 2 During first power on, the input voltage supply must reach minimum 4.25 V for PMIC to detect valid input supply.

NOTE 3 The maximum VIN_Bulk input supply voltage rise during soft stop for SWx soft stop operation.

NOTE 4 The maximum VIN_Bulk input supply voltage rise is tested with max VIN_Bulk = 5.5V, including DC or AC offset. SWA and SWB = 1.1V, SWC = 1.8V, and using the recommended setting from the "PMIC Register setting for the Soft Stop" table in JESD323 or JESD324, depending on the DIMM type. The test condition assumes input VIN_Bulk supply is not capable of sinking current. The maximum VIN_Bulk input supply voltage rise is tested with module VIN_Bulk and output rail decoupling from any relevant passed CSODIMM or CUDIMM RC ballot, and with bulk output capacitance for SWx listed in Section 5, "DDR5 DIMM Schematic".

NOTE 5 This specification defines the DC component of the voltage during soft stop. AC noise that is less than 1µs can be ignored when testing against this spec. The maximum voltage rise is measured under 1 MHz bandwidth limiting during soft stop shut down

NOTE 6 The ramp up rate between 300 mV and 4.0 V.

NOTE 7 The ramp down rate between 4.0 V and 300 mV.

NOTE 8 The area under the curve above VIN_Bulk = 5.5 V. VIN_Bulk_AC spec must also be satisfied.

NOTE 9 This is a platform spec, the maximum input current delivered by the platform through the DIMM gold finger.

NOTE 10 VIN_Bulk = 5.0 V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR_EN signal is static Low or High; GSI_n signal is pulled High. I^2C or I3C Basic interface access is not allowed and bus is pulled High. PID signal is pulled either High or Low.

NOTE 11 VIN_Bulk = 5.0 V. Measured at room temperature. All output regulators and LDOs are on with 0 A output load. VR_EN signal is static Low or High. GSI_n signal is pulled High. I^2C or I3C Basic interface access is allowed and bus is pulled High. PID signal is pulled either High or Low

3.2 Switch Regulator Output Electrical Characteristics

Table 4 — SWA, SWB[1] - Single Phase Regulator; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.1		V	2
Maximum Continuous DC Current Load	I_{tdc}	0	-	6	A	3
Maximum Peak Instantaneous Current	$I_{peakmax}$	-	-	8.5	A	4
Maximum Load Transient	dI/dt	-	-	7	A/µs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	5,6
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	7

NOTE 1 Only applicable if Table 173, Register 0x4F [0], = '0'.
NOTE 2 Typical voltage configured in the register Table 129, Register 0x21, [7:1] for SWA and Table 133, Register 0x25, [7:1] for SWB.
NOTE 3 Measured over long period of time. Typically 1 second.
NOTE 4 Measured over short period of time. Typically ≥ 20 µs but less than 50 µs.
NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 3, Input Supply DC + AC Specification. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and is not to exceed TBD mV.
NOTE 6 Applies across entire PMIC operating temperature range.
NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 5.0 V. The regulator output current load Itdc = 0 A.

Table 5 — SWA + SWB[1] - Dual Phase Regulator; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.1		V	2
Maximum Continuous DC Current Load	I_{tdc}	0	-	12	A	3
Maximum Peak Instantaneous Current	$I_{peakmax}$	-	-	17	A	4
Maximum Load Transient	dI/dt	-	-	14	A/µs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	5,6
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75		7

NOTE 1 Only applicable if Table 173, Register 0x4F [0], = '1'.
NOTE 2 Typical voltage configured in the register Table 129, Register 0x21, [7:1].
NOTE 3 Measured over long period of time. Typically 1 second.
NOTE 4 Measured over short period of time. Typically ≥ 20 µs but less than 50 µs.
NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 3, Input Supply DC + AC Specification. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and is not to exceed TBD mV.
NOTE 6 Applies across entire PMIC operating temperature range.
NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load I_{tdc} = 0 A.

3.2 Switch Regulator Output Electrical Characteristics (cont'd)

Table 6 — SWC[1] - Single Phase Regulator; DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.8		V	2
Maximum Continuous DC Current Load	I_{tdc}	0	-	2	A	3
Maximum Peak Instantaneous Current	$I_{peakmax}$	-	-	3	A	4
Maximum Load Transient	dI/dt	-	-	2.5	A/µs	
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	5,6
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	7

NOTE 1 There is no note. This is intentional.
NOTE 2 Typical voltage configured in the register Table 135, Register 0x27, [7:1].
NOTE 3 Measured over long period of time. Typically 1 second.
NOTE 4 Measured over short period of time. Typically ≥ 20 µs but less than 50 µs.
NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN_Bulk can vary from minimum to maximum value specified in Table 3, Input Supply DC + AC Specification. The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter and is not to exceed TBD mV.
NOTE 6 Applies across entire PMIC operating temperature range.
NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load Itdc = 0 A.

3.3 LDO Output Regulator Characteristics

Table 7 — LDO Output Regulator DC + AC Specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1.8 V LDO Output Voltage	VOUT_1.8V		1.8		V	1
1.8 V LDO Output - Maximum Output Current	$I_{tdc\_VOUT\_1.8V}$	-	-	25	mA	2
1.0 V LDO Output Voltage	VOUT_1.0V		1.0		V	3
1.0 V LDO Output - Maximum Output Current	$I_{tdc\_VOUT\_1.0V}$	-	-	20	mA	4

NOTE 1 Typical voltage is configured in register Table 139, Register 0x2B, [7:6]. The min and max values are guaranteed to be within ± 100 mV of programmed value.
NOTE 2 The maximum output current represents the external load only and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.8V LDO Power Good status is good (i.e., $t_{1.8V\_Ready}$ timing parameter is satisfied). Prior to PMIC's 1.8V LDO Power Good status (i.e., while PMIC is still ramping up the 1.8V LDO), the maximum output current shall be limited to maximum of 10 mA.
NOTE 3 Typical voltage is configured in register Table 139, Register 0x2B, [2:1]. The min and max values are guaranteed to be within ± 50 mV of programmed value.
NOTE 4 The maximum output current represents the external load only and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.0V LDO Power Good status is good (i.e., $t_{1.0V\_Ready}$ timing parameter is satisfied). Prior to PMIC's 1.0V LDO Power Good Status (i.e., while PMIC is still ramping up the 1.0V LDO), the maximum output current shall be limited to maximum of 5 mA.

3.4 I^2C or I3C Basic DC and AC Electrical Characteristics

Table 8 — I^2C, I3C Basic and Logic Interface DC Electrical Specification

Parameter	Symbol	Min	Max	Unit	Notes
Input Low Voltage (PWR_GOOD, SDA, SCL, VR_EN)	V_{IL}	-0.3	0.3	V	
Input High Voltage (SDA, SCL)	V_{IH}	0.7	3.6	V	
Input High Voltage (PWR_GOOD, VR_EN)		1.26	3.6	V	
Output Low Voltage (SDA)	V_{OL}	-	0.3	V	1
Output Low Voltage (PWR_GOOD, GSI_n)		-	0.3	V	1 2
Output High Voltage (SDA)	V_{OH}	0.75	-	V	3
Output Low Current (SDA)	I_{OL}	3	-	mA	4
Output Low Current (PWR_GOOD, GSI_n)		3	-	mA	4
Output High Current (SDA)	I_{OH}		-3	mA	5
Rising Output Slew Rate (SDA)	Slew_Rate	0.1	1	V/ns	6
Falling Output Slew Rate (SDA)		0.1	3	V/ns	
Input Leakage Current	I_{LI}	-	±5	µA	
Output Leakage Current	I_{LO}	-	±5	µA	

NOTE 1 3 mA sink current.
NOTE 2 PWR_GOOD, GSI_n output is Open Drain output. There is an external pullup resistor to 1.8 V or 3.3 V on the board or other device.
NOTE 3 3 mA source current.
NOTE 4 V_{OL} = 0.3 V.
NOTE 5 V_{OH} = VDDIO - 0.3 V.
NOTE 6 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 9 and Figure 10 shows the timing measurement points. For slew rate measurement, the V_{OH} level shown in Figure 10 is a function of R_{on} value; $V_{OH} = \{1.0/(R_{on} + 50)\} * 50$.

Table 9 — Input Capacitance Spec

Parameter	Symbol	Min	Max	Unit	Notes
Input Capacitance (PWR_GOOD, SCL, SDA, VR_EN)	C_{IN}	-	5	pF	

Table 10 — Input Spike Filter Spec

Parameter	Symbol	Test Condition	Min	Max	Unit	Notes
Pulse width of spikes which must be suppressed by the input filter in I^2C mode	t_{SP}	Single glitch, f ≤ 100 KHz	-	-	ns	
		Single glitch, f > 100 KHz	0	50	ns	1

NOTE 1 T_A = 25 °C; f = 400 KHz. Verified by design and characterization only.

Table 11 — Output Ron

Parameter	Symbol	Min	Max	Unit	Notes
SDA Output Pullup and Pulldown Driver Impedance	R_{ON}	20	100	Ω	1
GSI_n, PWR_GOOD Output Pulldown Driver Impedance		20	100	Ω	2

NOTE 1 Pulldown Ron = Vout/Iout. Pullup Ron = (VOUT_1.0V - Vout)/Iout.
NOTE 2 Pulldown Ron = Vout/Iout

3.4 I²C or I3C Basic DC and AC Electrical Characteristics (cont'd)

Table 12 — I²C and I3C Interface AC Characteristics

		I²C Mode - Open Drain		I3C Basic Mode Push-Pull[1]			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Clock Frequency	f_{SCL}	0.01	1	0.01	12.5	MHz	
Clock High Pulse Width Time	t_{High}	260		35		ns	
Clock Low Pulse Width Time	t_{Low}	500		35		ns	
Detect Clock Input Low Time	$t_{TIMEOUT}$	10	50	10	50	ms	
Rise Time	t_R	-	120	-	5	ns	2,3
Fall time	t_F	-	120	0	5	ns	2,3
Data in Setup Time	$t_{SU:DAT}$	50	-	8	-	ns	2,4
Data in Hold Time	$t_{HD:DI}$	0	-	3	-	ns	2,4
Start Condition Setup Time	$t_{SU:STA}$	260	-	12	-	ns	2
Start Condition Hold Time	$t_{HD:STA}$	260	-	30	-	ns	2
Stop Condition Setup Time	$t_{SU:STO}$	260	-	12	-	ns	2
Time between Stop Condition and next Start Condition	t_{BUF}	500	-	500	-	ns	2,5
SDA Data Out Hold Time	$t_{HD:DAT}$	0.5	350	N/A	N/A	ns	6
SCL Falling Clock In to Valid SDA Data Out Time	t_{DOUT}	N/A	N/A	0.5	12	ns	7,8
SCL Rising Clock In to Target SDA Output Off	t_{DOFFT}	N/A	N/A	0.5	12	ns	8,9
SCL Rising Clock In to Controller SDA Output Off	t_{DOFFC}	N/A	N/A	0.5	30	ns	8,10
SCL Rising Clock In to Controller Driving Data Signal Low	$t_{CL\_r\_DAT\_f}$	N/A	N/A	40	-	ns	11
Bus Available Time (no edges seen on SCL and SDA)	t_{AVAL}	N/A	N/A	1	-	µs	
Time to issue IBI after an event is detected when Bus is available	t_{IBI_ISSUE}	N/A	N/A	-	15	µs	
Time from Clear Register Status to any I3C Basic operation with Start condition to avoid false IBI generation; PEC disabled	$t_{CLR\_I3C\_CMD\_Delay}$	N/A	N/A	4	-	µs	
Time from Clear Register Status to any I3C Basic operation with Start condition to avoid false IBI generation; PEC enabled		N/A	N/A	15	-	µs	
DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay	$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	3	-	3	-	µs	12,13,14
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	$t_{WR\_RD\_DELAY\_PEC\_EN}$	N/A	N/A	8	-	µs	15,16,17
SETHID CCC or SETAASA CCC followed by any other CCC or Read/Write Command Delay	$t_{I2C\_CCC\_Update\_Delay}$	2.5	-	N/A	N/A	µs	
RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	$t_{I3C\_CCC\_Update\_Delay}$	-	-	2.5	-	µs	

Table 12 — I²C and I3C Interface AC Characteristics (cont'd)

		I²C Mode - Open Drain		I3C Basic Mode Push-Pull[1]			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Any CCC followed by RSTDAA CCC Delay	t_{CCC_Delay}	N/A	N/A	2.5	-	µs	

NOTE 1 I3C Basic mode with Open Drain operation follows timing values as shown in I²C Mode - Open Drain column.
NOTE 2 See Figure 6 for PMIC's input timing definition.
NOTE 3 See Figure 11 for voltage threshold definition for rise and fall times.
NOTE 4 The input setup time is referenced from SDA VIL or VIH threshold as shown in Figure 6 to SCL VIH threshold as shown in Figure 6. The input hold time is referenced from SCL VIL threshold as shown in Figure 6 to SDA VIL or VIH threshold as shown in Figure 6.
NOTE 5 If PEC is enabled, $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter applies.
NOTE 6 The PMIC device guarantees $t_{HD:DAT}$ value in I²C mode of operation. See Figure 8 for PMIC's output timing definitions as well as SCL clock input threshold level and SDA data output threshold levels.
NOTE 7 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOUT}value. See Figure 7 for PMIC's output timing definition as well as SCL clock input threshold level and SDA data output threshold levels.
NOTE 8 This timing parameter is guaranteed into output timing reference load as shown in Figure 9.
NOTE 9 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See Figure 34.
NOTE 10 The PMIC device must be configured in I3C Basic mode to guarantee t_{DOFFC} value. See Figure 35.
NOTE 11 See Figure 37.
NOTE 12 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.
NOTE 13 The PMIC sends NACK if Host does not satisfy $t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$ timing parameter.
NOTE 14 This timing parameter restriction is only applicable when PEC function is disabled in PMIC. If PEC is enabled, this timing parameter does not apply.
NOTE 15 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.
NOTE 16 This timing parameter restriction is only applicable when PEC function is enabled in PMIC. If PEC is disabled, this timing parameter does not apply.
NOTE 17 The PMIC sends NACK if Host does not satisfy $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter.

The PMIC device follows the I²C bus and I3C Basic bus input timing requirements as shown in Figure 6 and Table 12 and output timing requirement as shown in Figure 7.

3.4 I²C or I3C Basic DC and AC Electrical Characteristics (cont'd)

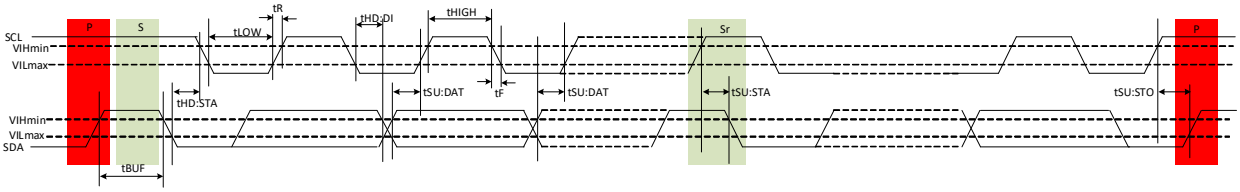


Figure 6 — I²C or I3C Basic Bus AC Input Timing Parameter Definition

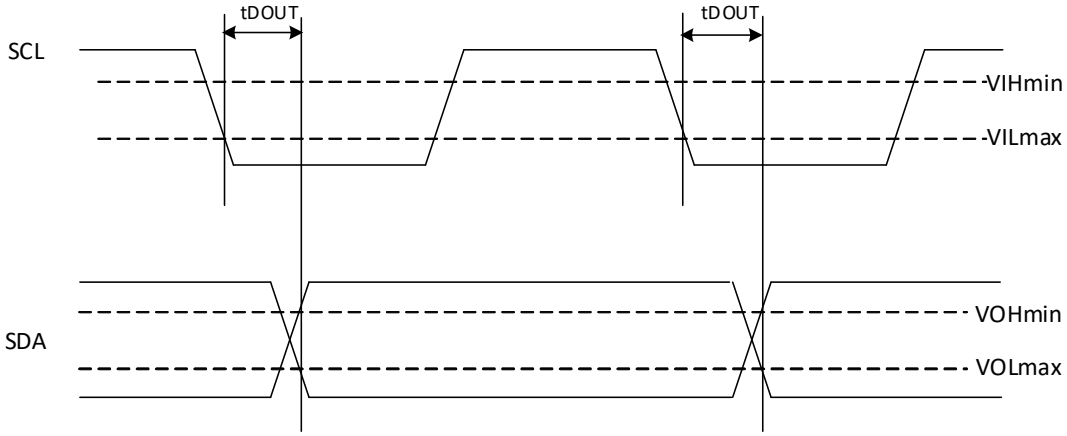


Figure 7 — I3C Basic Bus AC Data Output Timing Parameter Definition

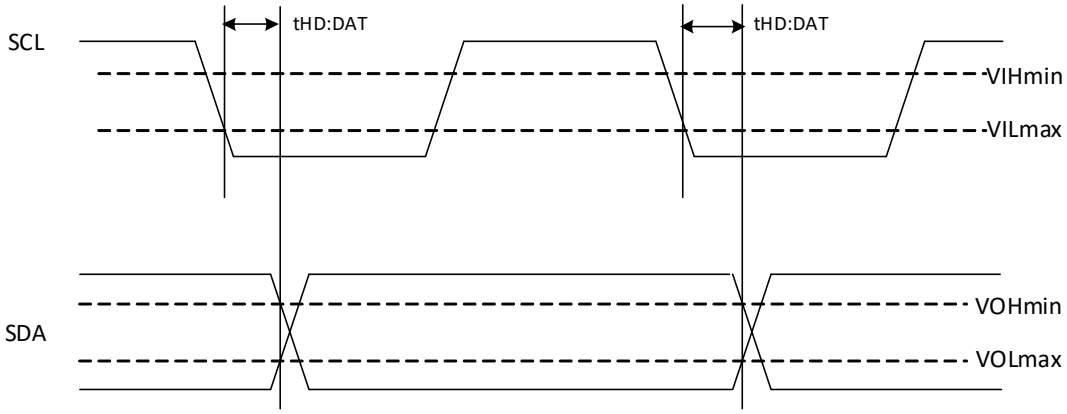


Figure 8 — I²C Bus AC Data Output Timing Parameter Definition

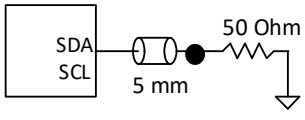


Figure 9 — Output Slew Rate and Output Timing Reference Load

3.4 I²C or I3C Basic DC and AC Electrical Characteristics (cont'd)

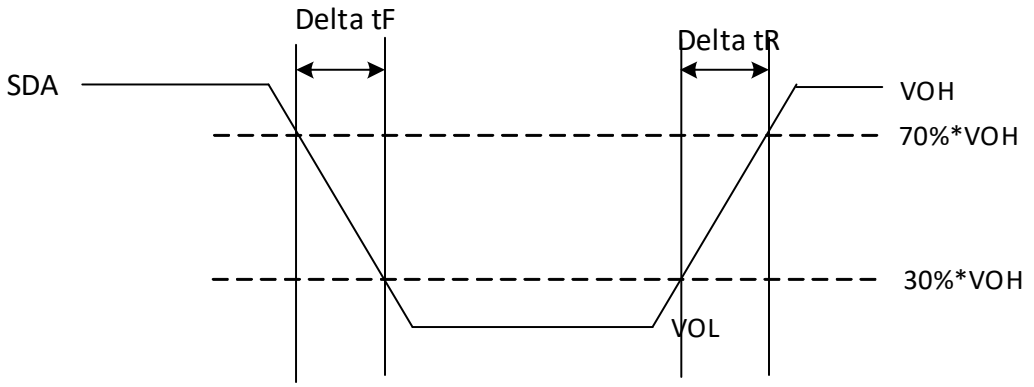


Figure 10 — Output Slew Rate Measurement Points

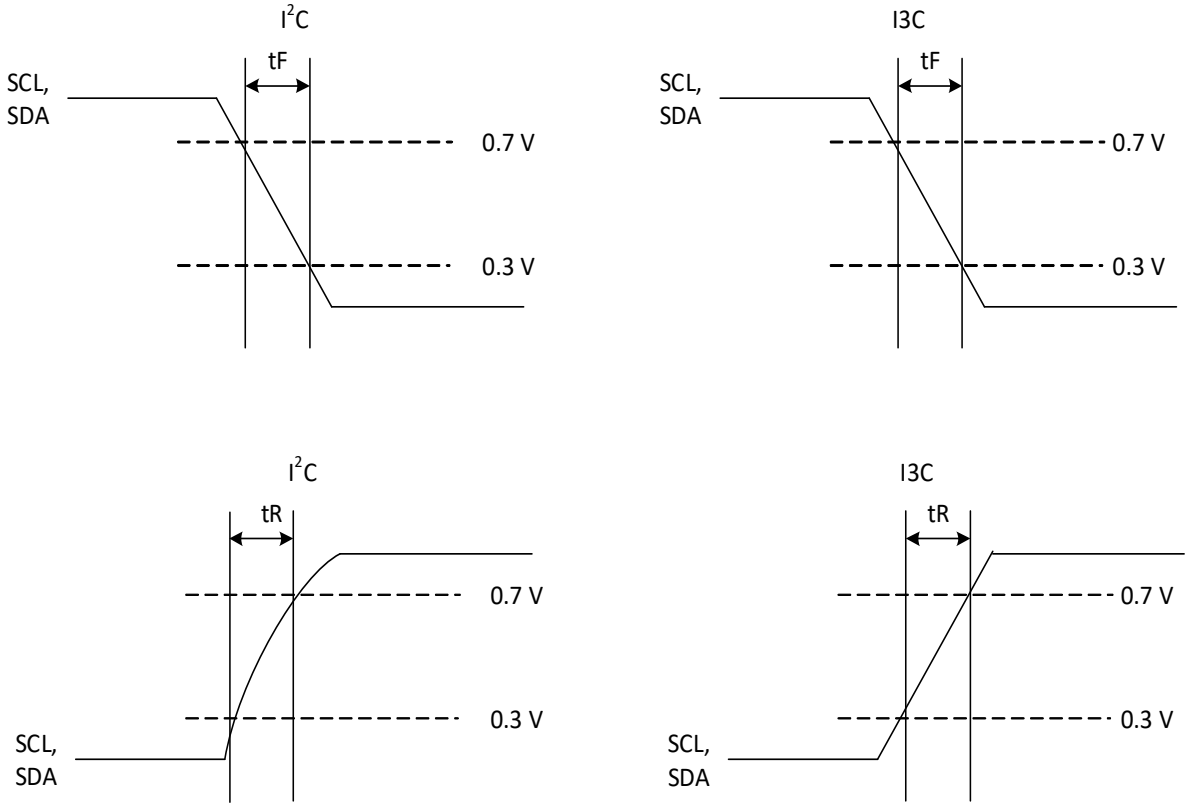


Figure 11 — Input Rise and Fall Timing Parameter Definition

3.5 Measurement Condition

Table 13 — AC Measurement Conditions[1]

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance		40	pF
	Input rise and Fall times - Open Drain	-	120	ns
	Input rise and fall times - Push Pull	-	5	ns
	Input signal swing levels	0.2 to 0.8		V
	Input levels for timing reference	0.3 to 0.7		V

NOTE 1 This AC measurement condition (Table 13 and Figure 12) is only for the test purpose in lab.

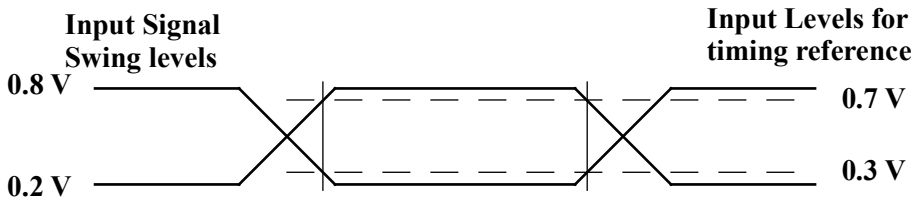


Figure 12 — AC Measurement Waveform

3.6 PMIC AC Timing Parameters

Table 14 — PMIC AC Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Supply to GSI_n assertion	tInput_PWR_GOOD_GSI_Assertion			10	µs	
Input over voltage condition to GSI_n assertion	tInput_OV_GSI_Assertion	-	-	10	µs	
Input over voltage condition to automatic PMIC VR Disable	tInput_OV_VR_Disable	-	-	20	µs	
Output Voltage Tolerance to GSI_n assertion	tOutput_PWR_GOOD_GSI_Assertion	-	-	10	µs	
Output over voltage condition to automatic PMIC VR Disable	tOutput_OV_VR_Disable	-	-	20	µs	
Output under voltage lockout condition to automatic PMIC VR Disable	tOutput_UV_VR_Disable	-	-	20	µs	
Output current limiter Warning to GSI_n assertion	tOutput_Current_Limiter	-	-	10	µs	
High Temperature Warning to GSI_n assertion	tHigh_Temp_Warning	-	-	10	µs	
Critical Temperature condition to automatic PMIC shut down	tShut_Down_Temp	-	-	10	µs	
VIN_Bulk input supply stable to VR Enable Command	tVIN_Bulk_to_VR_Enable	6.5	-	-	ms	
VIN_Bulk input supply stable to VOUT_1.8V output stable	t1.8V_Ready	-	-	2.5	ms	

Table 14 — PMIC AC Timing Parameters (cont'd)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
VOUT_1.8V output supply stable to VOUT_1.0V output stable	t1.0V_Ready	-	-	1.0	ms	1
VOUT_1.8V output supply to PMIC Management Ready	tManagement_Ready	-	-	3	ms	
VR Enable Command to PMIC output regulator ready	tPMIC_PWR_Good_Out	Figure 23			ms	
VR Disable Command to PMIC Output Regulators Off	tPMIC_Output_Off	Figure 25			ms	
PWR_GOOD Input Low Pulse Width	tPWR_GOOD_Low_Pulse_Width	2	0	0	µs	
PWR_GOOD Input Low Pulse Width Input Filter	tPWR_GOOD_Low_Pulse_Width_Filter	-	-	0.35	µs	
VR_EN_Input High Pulse Width	tVR_EN_High_Pulse_Width	2	0	0	µs	
VR_EN Input High Pulse Width Input Filter	tVR_EN_High_Pulse_Width_Filter	-	-	0.35	µs	
Output Voltage Adjustment in Programmable Mode	Δv/Δt	-	1	-	mV/µs	2

NOTE 1 This time is added to $t_{1.8V\_Ready}$ parameter to get total time from VIN_Bulk input supply.
NOTE 2 See footnote 4 for registers Table 129, Register 0x21, [7:1], Table 133, Register 0x25, [7:1] and Table 135, Register 0x27, [7:1]. The accuracy is ± 10%.

3.7 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 15, Absolute Maximum Rating, Table 16, ESD Requirement, and Table 17, EOS Requirement may cause permanent damage to the device. Functional operation of the DDR5 PMIC at absolute maximum ratings is not implied. Exposure to absolute maximum rating condition for extended periods may affect long term reliability.

Table 15 — Absolute Maximum Rating

Pin	Maximum Rating		Unit
	DC	AC	
VIN_BULK, VIN	-0.3 to 6	TBD (Duration ≤ 25 ns)	V
VOUT_1.8V, VOUT_1.0V	-0.3 to 2.2	-	V
SWA, SWB, SWC	-0.3 to 6	-3 to 9 (Duration < 25 ns)	V
BOOT_SWA, BOOT_SWB, BOOT_SWC (to GND)	-0.3 to 12	-0.3 to 15 (Duration < 25 ns)	V
BOOT_SWA, BOOT_SWB, BOOT_SWC (to SWx)	-0.3 to 6	TBD	V
SWA_FB_P, SWB_FB_P, SWC_FB_P (to AGND)	-0.3 to 2.2	-	V
PWR_GOOD, GSI_n, VR_EN	-0.3 to 5.0	-	V
SCL, SDA; I^2C Mode only	-0.3 to 5.0		V
SCL, SDA; I3C Mode only	-0.3 to 2.1		V
PID	-0.3 to 2.2	TBD	V
AGND, PGND	-0.3 to 0.3	-	V

3.8 ESD Requirements

Table 16 — ESD Requirement

Test Model	Pin	Maximum Rating	Unit
HBM	All	± 2000	V
CDM	All	± 500	V

Table 17 — EOS Requirement

Pin	Maximum Rating	Unit	Notes
VIN_BULK	10	V	1,2,3,4

NOTE 1 The test is performed on DDR5 DIMM module without any input capacitor on VIN_BULK
NOTE 2 The input source needs to follow the waveform and condition as shown in Figure 13 and Table 18.
NOTE 3 Probing is performed at the VIN_BULK pin of PMIC.
NOTE 4 Applies to VIN_Bulk and VIN pin.

Table 18 — Input Source Condition

Item	Value	Notes
T (rise from 30% to 90% of peak)	0.72 µs (+ 30%)	
T1 (rise time)	1.2 µs (+ 30%)	T1 = 1.67*T
T2 (duration time to half value)	50 µs (+ 20%)	
Output Impedance	2 Ω	
$V_{UNDERSHOOT}$ Voltage	30% Max	

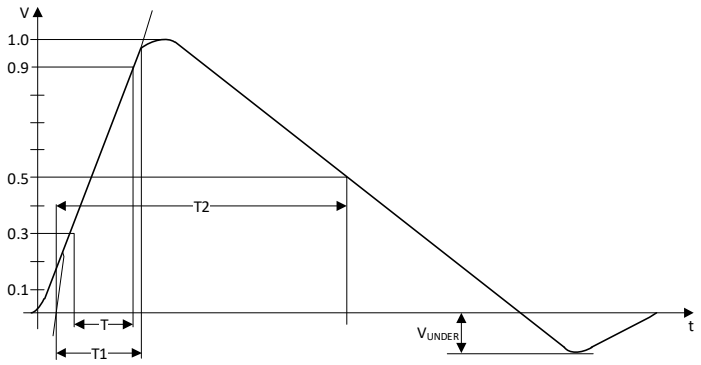


Figure 13 — Impulse Waveform for EOS Test (IEC 61000-4-5)

3.9 Thermal Characteristics

Table 19 — Thermal Characteristics

Parameter	Symbol	Maximum Rating	Unit	Notes
Thermal resistance junction to case	Θ_{JC}	TBD	°C/W	1,2,3
Junction operating temperature	T_J	-10 to 125	°C	
Case operating temperature	T_C	-10 to TBD	°C	3
Storage temperature	T_{STG3}	-55 to 150	°C	3
Lead temperature (soldering, 10s)	T_{LEAD}	260	°C	3

NOTE 1 The maximum power dissipation is $P_{D(MAX)} = (T_{JMAX} - T_C)/ \Theta_{JC}$. Exceeding the maximum allowable power dissipation results in excessive die temperature and the device will enter thermal shutdown.

NOTE 2 This thermal rating was calculated on JEDEC 51 standard 4 layer board with dimensions 3” x 4.5” in still air conditions. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude and other unlisted variables.

NOTE 3 This specification is compliant with JESD402-1 Temperature Grade and Measurement Specification for Components and Modules, operating temperature range MT, storage temperature range T_{STG3}. See JESD402-1 for details, including measurement point.

4 Performance Characteristics

4.1 Efficiency

The PMIC efficiency spec is defined for the reference test board only and it is not applicable for any DIMM application board which varies from the reference test board. The reference test board includes the inductor and the PCB characteristics which complies with the footnote 8 in Table 20. The efficiency spec is only measured for one switch regulator at a time; all other switch regulators must be disabled. The PMIC switching frequency must comply with the footnote 11 in Table 20. The typical DIMM application environment, which deviates from the reference test board in that all buck regulators are turned on simultaneously, external load is carried on the LDOs, and signal interface pins may not be held static, will have lower efficiency than defined in Table 20. The combination of all variation for application environment is not subject to the efficiency spec as defined in Table 20.

4.1.1 Efficiency with Inductor Footprint

Table 20 — Efficiency Characteristics[1]

Switch Node Output	Efficiency	Efficiency (% of Max Itdc Load)				Unit	Notes
	Light Load[2]	25%	50%	75%	100%		
SWA or SWB (Single Phase Regulator Mode)	83	≥ 90	≥ 88	≥ 85	≥ 82	%	3,4,5,6,7,8,9,10,11,12
SWA + SWB (Dual Phase Regulator Mode)	83	≥ 90	≥ 88	≥ 85	≥ 82	%	
SWC	85	≥ 90	≥ 89	≥ 87	≥ 85	%	

NOTE 1 The efficiency numbers assume the inductor specification as noted in Section 4.2.

NOTE 2 Light Load is defined as 100 mA for SWA and SWB for single phase regulator mode; 200 mA for SWA+SWB for dual phase regulator mode; 50 mA for SWC. Acoustic Noise prevention may be disabled in Table 150, Register 0x36 [3:1] when measuring Light Load Efficiency.

NOTE 3 VIN_Bulk = 5 V

NOTE 4 The maximum Itdc as specified in Table 4 through Table 6, appropriately.

NOTE 5 When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.

NOTE 6 No external load on VOUT_1.8V, VOUT_1.0V LDO is applied.

NOTE 7 I^2C/I3C Basic bus is pulled High and held static. PWR_GOOD and GSI_n signals are pulled High and held static.

NOTE 8 The efficiency includes the buck regulator loss, the PCB loss (< 4 mΩ or less). See Section 4.2 assumption for DCR and ACR.

NOTE 9 Efficiency calculation equation: $(V_{OUT} * I_{OUT}) / [(V_{IN\_Bulk} * I_{VIN\_Bulk})+(V_{IN} * I_{VIN})]$; where V_{OUT}, I_{OUT}, V_{IN_Bulk}, I_{VIN_Bulk}, V_{IN}, I_{VIN} parameters are actual measured values.

NOTE 10 Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature of 105 °C). The DCR characteristics noted above applies inductor temperature of 105 °C.

NOTE 11 The output buck regulator switching frequency can be set to 750 KHz.

NOTE 12 For input supply rail, probing is done at the input high frequency filter cap (0.1 uF) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.

4.2 Inductor Specification

4.2.1 Mechanical Specification

The inductor package dimensions and its recommended land patterns are defined in Table 21 and Table 22 for SWA and SWB, and Table 23 for SWC.

Table 21 — Inductor Mechanical Specifications for SWA and SWB

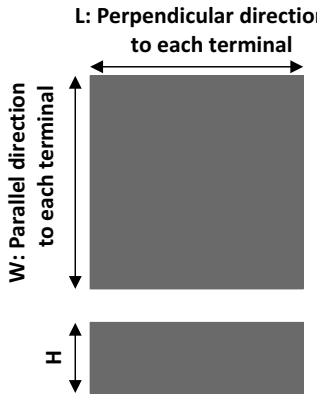
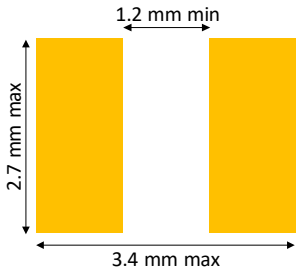
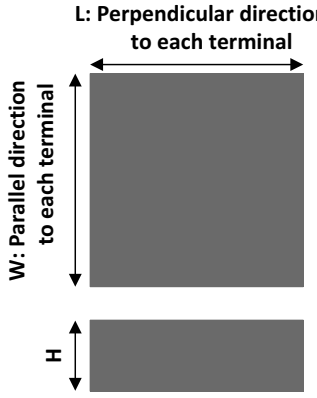
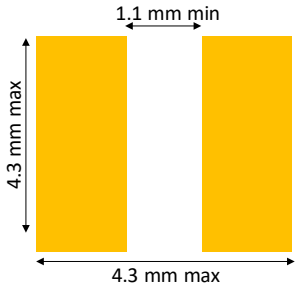
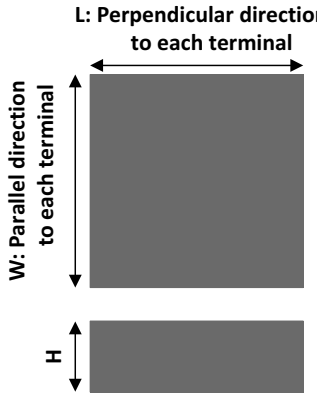
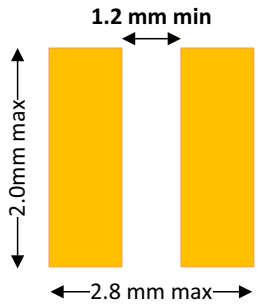
Package Size		Reference Drawing	Recommended Land Pattern
L [mm]	3.4 Max		
W [mm]	2.7 Max		
H [mm]	1.2 Max		

Table 22 — Selectable Optional Mechanical Specifications for SWA and SWB by the Implemented Acceptable DIMM (in UDIMM and SODIMM) Design

Package Size		Reference Drawing	Recommended Land Pattern
L [mm]	4.3 Max		
W [mm]	4.3 Max		
H [mm]	1.2 Max		

4.2.1 Mechanical Specification (cont'd)

Table 23 — Inductor Mechanical Specifications for SWC

Package Size		Reference Drawing	Recommended Land Pattern
L [mm]	2.7 Max		
W [mm]	2.2 Max		
H [mm]	1.2 Max		

4.2.2 Electrical Specifications

The inductor electrical specifications are defined in Table 24 for SWA and SWB (1.1V), and Table 25 for SWC (1.8V), respectively.

Table 24 — Inductor Electrical Specifications for SWA and SWB (1.1V)

Size Selection	L @ 0.5-1 MHz (0 Bias) [µH]	Max DCR [mΩ]	Max ACR @ 1 MHz[1,2] [mΩ]	Ipeakmax (A)[3]	Min L @Ipeakmax [µH]	Max L @Ipeakmax (uH)
3.4 x 2.7 x 1.2 mm max	0.47 ± 20%	11.0	93	8.5	0.2	0.38
4.3 x 4.3 x1.2 mm max	0.47 ± 20%	8.5	93	8.5	0.27	0.47

NOTE 1 ACR definition: ACR = Rs@1MHz – DCR Measured Current (1MHz/sinusoidal): 0.49Arms with No DC Bias for all cases.

NOTE 2 On the Rs measurement, it will be recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments, or other instruments which is guaranteed on the measurement accuracy by inductor vendors.

NOTE 3 Minimum and Maximum inductance is defined at DC bias current given by the definition of Ipeakmax.

➢ Test condition for all: Ambient Temperature=20±2 °C, Ambient Humidity=65±5%Rh.

4.2.2 Electrical Specifications (cont'd)

Table 25 — Inductor Electrical Specifications for SWC (1.8V)

L @ 0.5-1 MHz (0 Bias) [µH]	Max DCR [mΩ]	Max ACR @ 1 MHz[1,2] [mΩ]	Min L @Ipeakmax[3] [µH]
1.0 ± 20%	36	182	0.5

NOTE 1 ACR definition: ACR = Rs@1MHz – DCR Measured Current (1MHz/sinusoidal): 0.33 Arms with No DC Bias for all cases.

NOTE 2 On the Rs measurement, it will be recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments, or other instruments which is guaranteed on the measurement accuracy by inductor vendors.

NOTE 3 Minimum Inductance is defined at DC bias current given by definition of Ipeakmax in PMIC5120.

- Test condition for all: Ambient Temperature=20±2 °C, Ambient Humidity=65±5%Rh

5 DDR5 DIMM Schematic

Figure 14 shows an example schematic when PMIC is configured in dual phase regulator mode. Table 26, PMIC Schematic Values shows all component details shown in the schematics. Note that the distributed capacitance across the entire DIMM module is not shown in the schematic. The amount of distributed capacitance required is DIMM-specific and so is not part of the PMIC spec. The bulk and decoupling capacitance shown here is a fixed requirement.

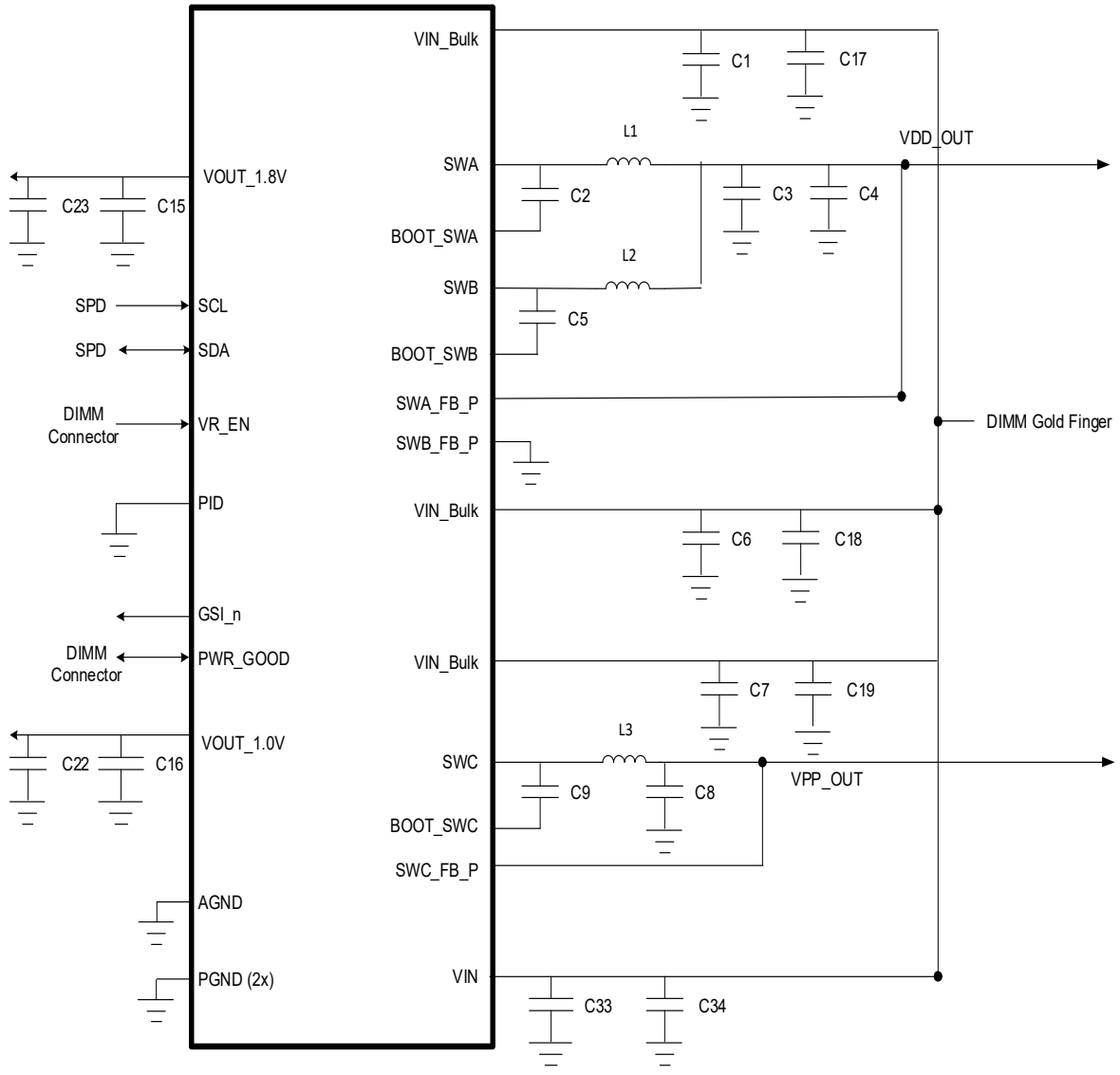


Figure 14 — Dual Phase Regulator - DDR5 DIMM Schematic

Figure 15 shows an example schematic when PMIC is configured in single phase regulator mode. Table 26, PMIC Schematic Values shows all component details shown in the schematics. Note that the distributed capacitance across the entire DIMM module is not shown in the schematic. The amount of distributed capacitance required is DIMM-specific and so is not part of the PMIC spec. The bulk and decoupling capacitance shown here is a fixed requirement.

5 DDR5 DIMM Schematic (cont'd)

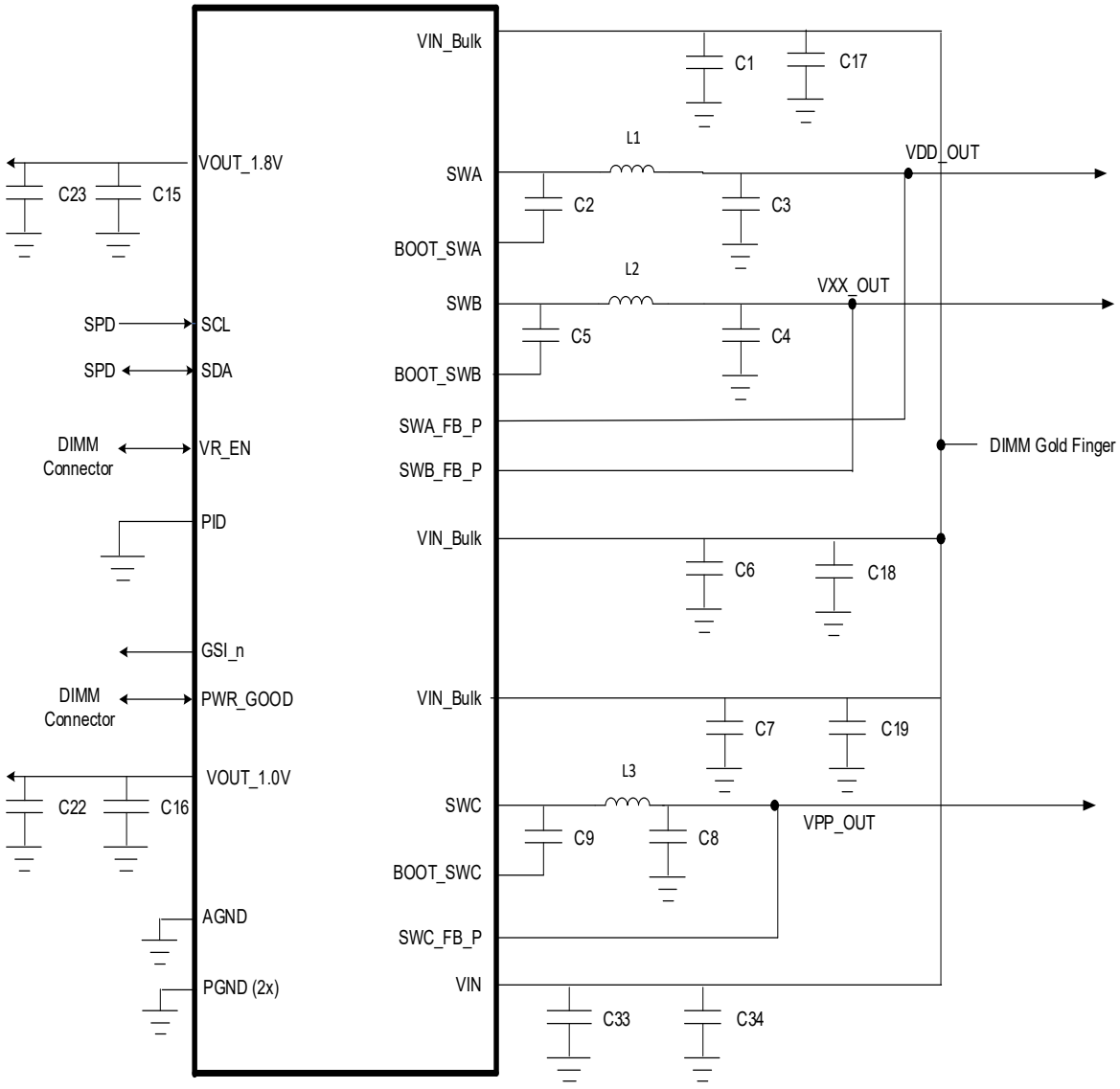


Figure 15 — Single Phase Regulator - DDR5 PMIC Schematic

5 DDR5 DIMM Schematic (cont'd)

Table 26 — PMIC Schematic Values

Component	Dual Phase Regulator Mode		Single Phase Regulator Mode		Unit	Comment
	Value	Physical Size	Value	Physical Size		
L1	0.47	3.4 x 2.7 x 1.2 mm or 4.3 x 4.3 x 1.2 mm	0.47	3.4 x 2.7 x 1.2 mm or 4.3 x 4.3 x 1.2 mm	µH	
L2	0.47	3.4 x 2.7 x 1.2 mm or 4.3 x 4.3 x 1.2 mm	0.47	3.4 x 2.7 x 1.2 mm or 4.3 x 4.3 x 1.2 mm	µH	
L3	1.0	2.7 mm x 2.2 mm x 1.2 mm	1.0	2.7 mm x 2.2 mm x 1.2 mm	µH	
C1	22 (2x)	10 V; 0603	22 (2x)	10 V 0603	µF	
C2	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C3	47 (3x)	6.3 V; 0603	47 (3x)	6.3 V; 0603	µF	
C4	47 (3x)	6.3 V; 0603	47 (3x)	6.3 V; 0603	µF	
C5	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C6	22 (2x)	10 V 0603	22 (2x)	10 V 0603	µF	
C7	22 (2x)	10 V 0603	22 (2x)	10 V 0603	µF	
C8	47 (3x)	6.3 V; 0603	47 (3x)	6.3 V; 0603	µF	
C9	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C15	4.7	6.3 V; 0402	4.7	6.3 V; 0402	µF	
C16	4.7	6.3 V; 0402	4.7	6.3 V; 0402	µF	
C17	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C18	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C19	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C22	0.1	6.3 V; 0201	0.1	6.3 V; 0201	µF	
C23	0.1	6.3 V; 0201	0.1	6.3 V; 0201	µF	
C33	0.1	10 V; 0201	0.1	10 V; 0201	µF	
C34	4.7	10 V; 0402	4.7	10 V; 0402	µF	

Figure 16 and Figure 17 show PMIC and passive component layout example for DDR5 SODIMM and DDR5 UDIMM. This layout is for reference and final layout may vary.

5 DDR5 DIMM Schematic (cont'd)

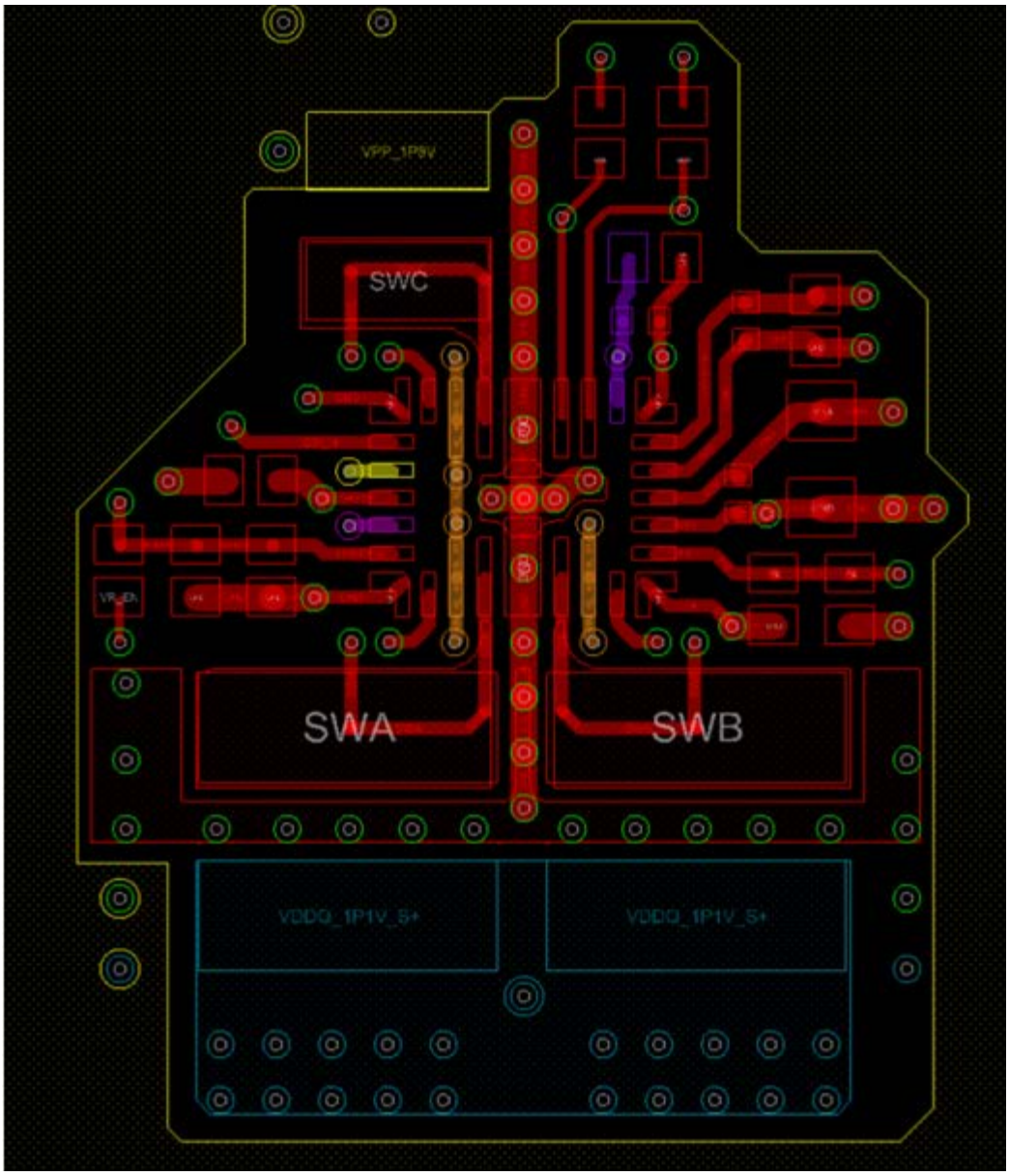


Figure 16 — DDR5 DIMM PMIC Layout Example - Top Layer

5 DDR5 DIMM Schematic (cont'd)

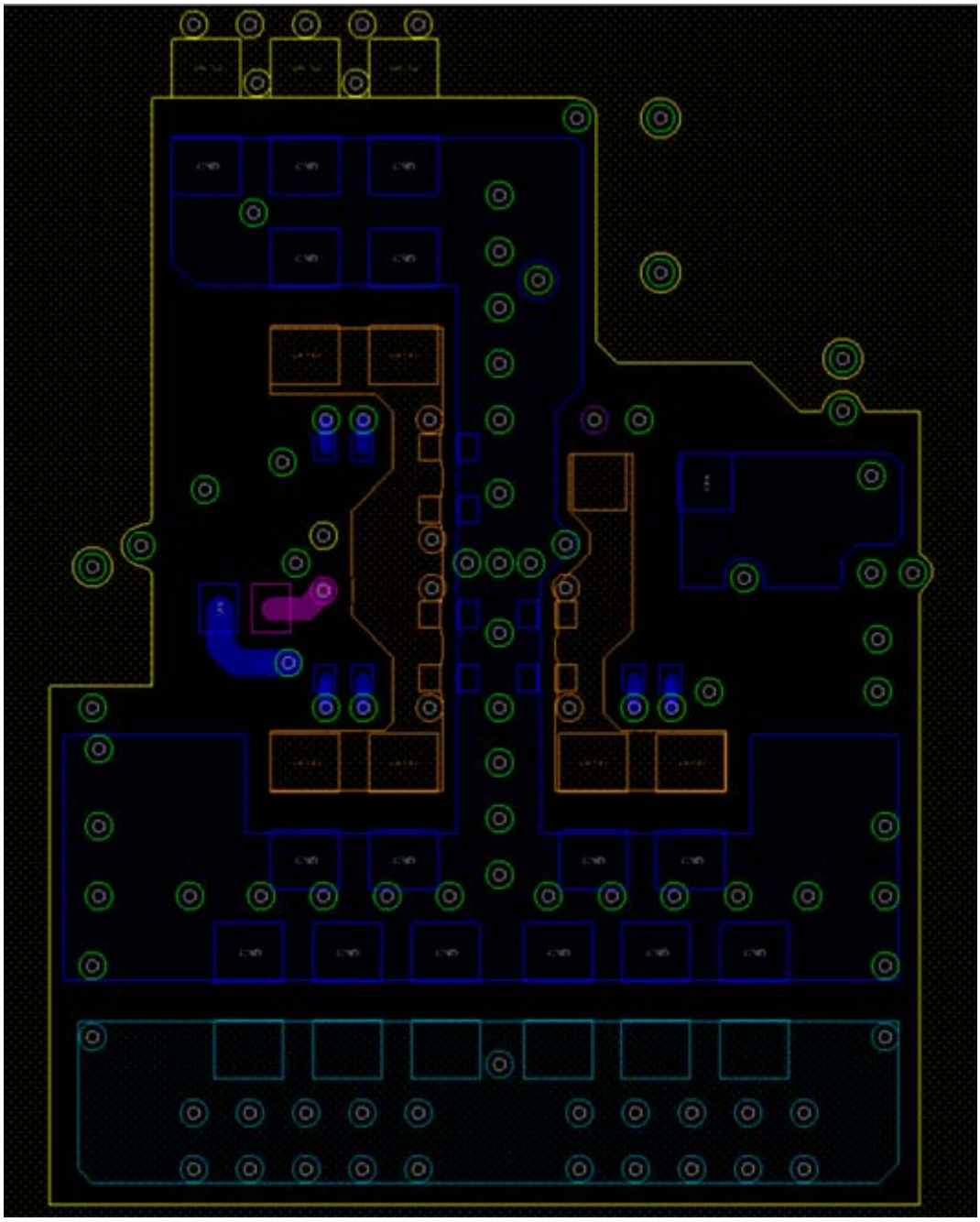


Figure 17 — DDR5 DIMM PMIC Layout Example - Bottom Layer

6 Functional Operation

6.1 PMIC Input Voltage Supply and Ramp Condition

The DDR5 PMIC has one input supply from the platform: VIN_Bulk.

The VIN_Bulk supply is used by the PMIC for all three switch (SWA, SWB, SWC) output regulators and two LDO outputs (VOUT_1.8V & VOUT_1.0V) regulators. Note that the VOUT_1.8V LDO output is separate and independent from SWC output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA or SWB.

At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage of 4.25 V before it can be detected as a valid input supply to the PMIC.

Once the VIN_Bulk supply is valid and stable, the PMIC shall assert PWR_GOOD output low, drive VOUT_1.8V and VOUT_1.0V supply within $t_{1.8V\_Ready}$ and $t_{1.0V\_Ready}$ time respectively. The PMIC drives PWR_GOOD output signal low only when VIN_Bulk input supply reaches minimum of 4.25 V. The PWR_GOOD output is pulled up to either 1.8 V or 3.3 V on the platform or on the host controller.

The PWR_GOOD pullup voltage (either 1.8 V or 3.3 V) can be available before or after VIN_Bulk is valid and stable. If PWR_GOOD pullup voltage is available before VIN_Bulk is applied, the PWR_GOOD signal is High and remains High with no leakage path or damage to the PMIC. When VIN_Bulk is applied to the PMIC, the PMIC asserts PWR_GOOD output low.

The PMIC shall enable I^2C/I3C Basic bus interface function within tManagement_Ready. The host shall not attempt to access the PMIC's memory registers until tManagement_Ready timing requirement is satisfied.

6.2 Power Up Initialization Sequence

During power on, the host shall:

1. Ramp up VIN_Bulk supply.
2. Hold VIN_Bulk supply stable for a minimum of tVIN_Bulk_to_VR_Enable time.
3. Hold VR_EN pin to static low or high. There is no timing relationship required on VR_EN pin with respect to VIN_Bulk input supply ramp up as long as VR_EN pin is held to static level to either low or high.
4. During VIN_Bulk ramp, if VR_EN signal is held low, it can transition to high only once. Once high, it shall remain high. The VR_EN signal is not allowed to transition to low during VIN_Bulk ramp up.
5. If VR_EN pin is held High during VIN_Bulk ramp up or transitions to High during VIN_Bulk ramp up, the PMIC turns on its output rails.
6. If VR_EN pin is held Low during VIN_Bulk Ramp, assert VR_EN signal High to turn on PMIC output rails. Alternatively, host can issue VR Enable command by setting register Table 146, Register 0x32 [7] = '1' via I^2C/I3C Basic bus or via DEVCTRL CCC to turn on PMIC output rails.

6.2.1 Power Up Sequence

Figure 18 to Figure 21 show examples of PMIC power up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB, SWC) is for example purpose only. The specific ramp up sequence is configurable through power on sequence configuration registers.

After VR Enable command is registered on the I^2C or I3C Basic bus or VR_EN pin is registered high, the PMIC shall complete the following steps within tPMIC_PWR_GOOD_OUT:

1. Check VIN_Bulk Power Good status is valid.
2. Power up itself - PMIC executes Power On Sequence Config 0 (Table 158, Register 0x40) to Power On Sequence Config 2 (Table 160, Register 0x42,) registers and configures PMIC internal registers as programmed in DIMM vendor memory space registers.
3. Power up all enabled output switch regulators and ready for normal operation
4. Update status registers Table 104, Register 0x08 [5,3:2] and floats PWR_GOOD signal within maximum of tPMIC_PWR_GOOD_OUT time.

If PMIC PWR_GOOD signal is not floated within tPMIC_PWR_GOOD_OUT time, the host can access the PMIC status registers for detailed information after tPMIC_PWR_GOOD_OUT time. The PMIC may NACK for any host request on I^2C or I3C Basic bus after VR Enable command (either with VR_EN pin high or on I^2C/I3C Basic Bus) until tPMIC_PWR_GOOD_OUT time expires.

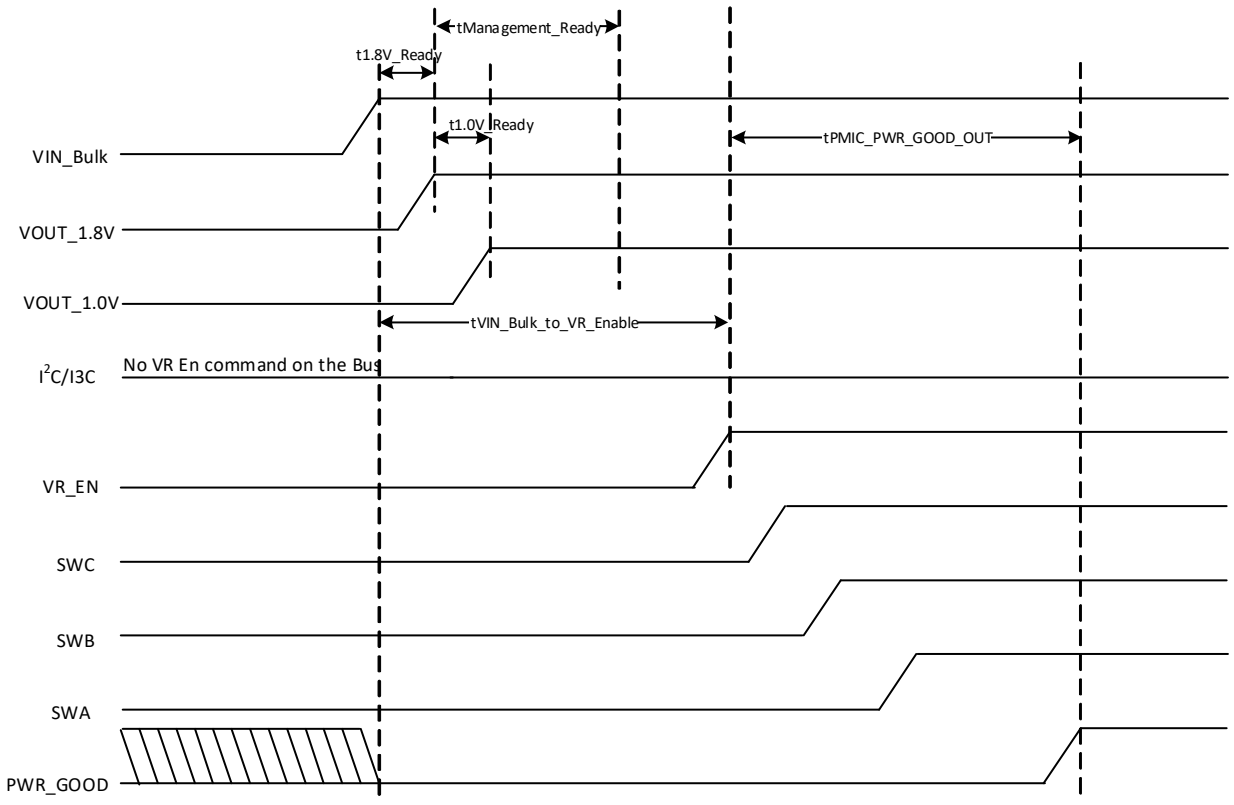


Figure 18 — Power Up Sequence; VR_EN Pin High after VIN_Bulk Ramp; No Bus Command

6.2.1 Power Up Sequence (cont'd)

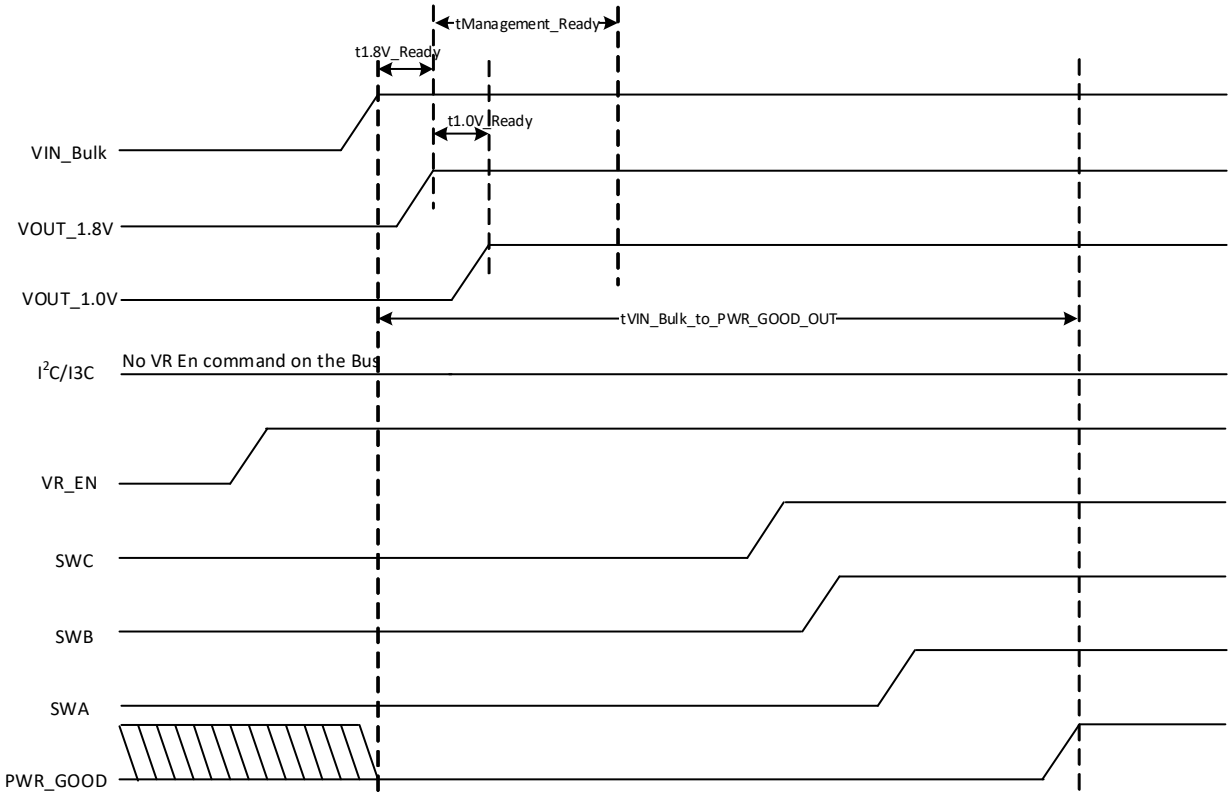


Figure 19 — Power Up Sequence; VR_EN pin High before VIN_Bulk Ramp; No Bus Command

6.2.1 Power Up Sequence (cont'd)

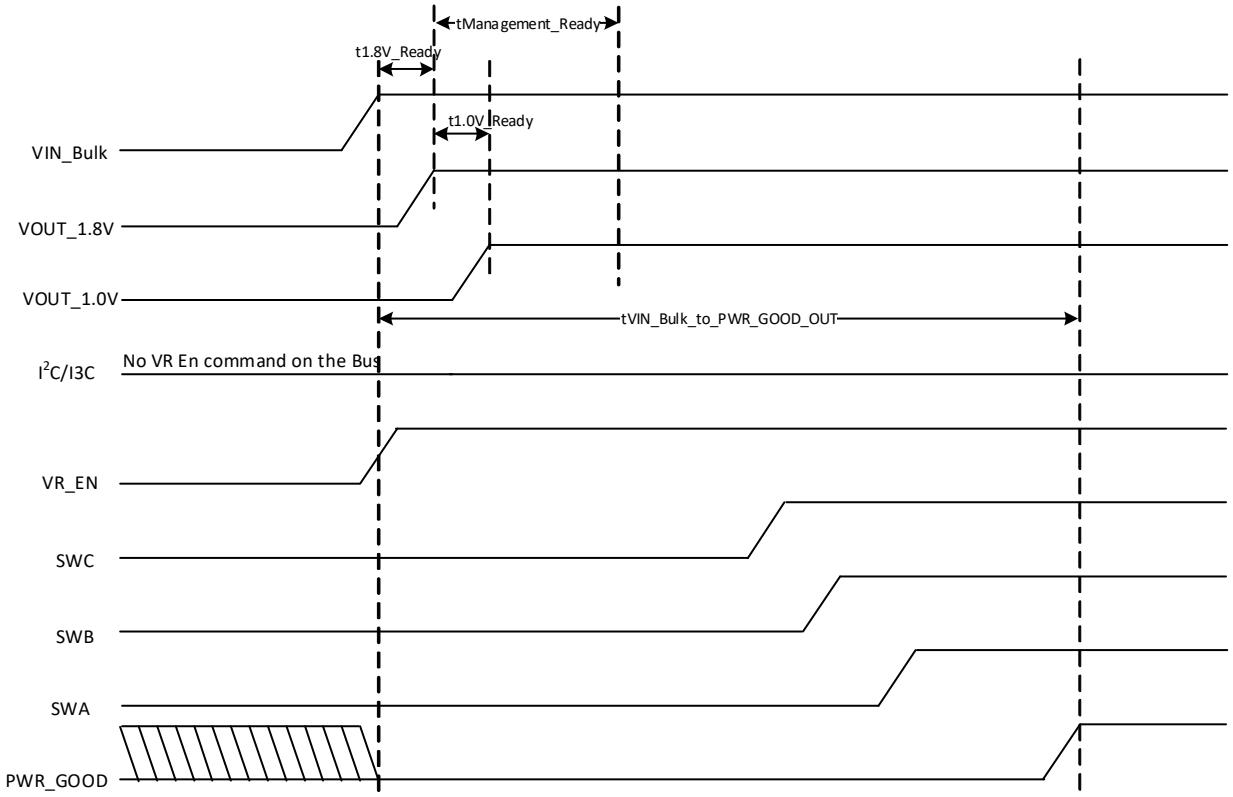


Figure 20 — Power Up Sequence; VR_EN pin High during VIN_Bulk Ramp; No Bus Command

6.2.1 Power Up Sequence (cont'd)

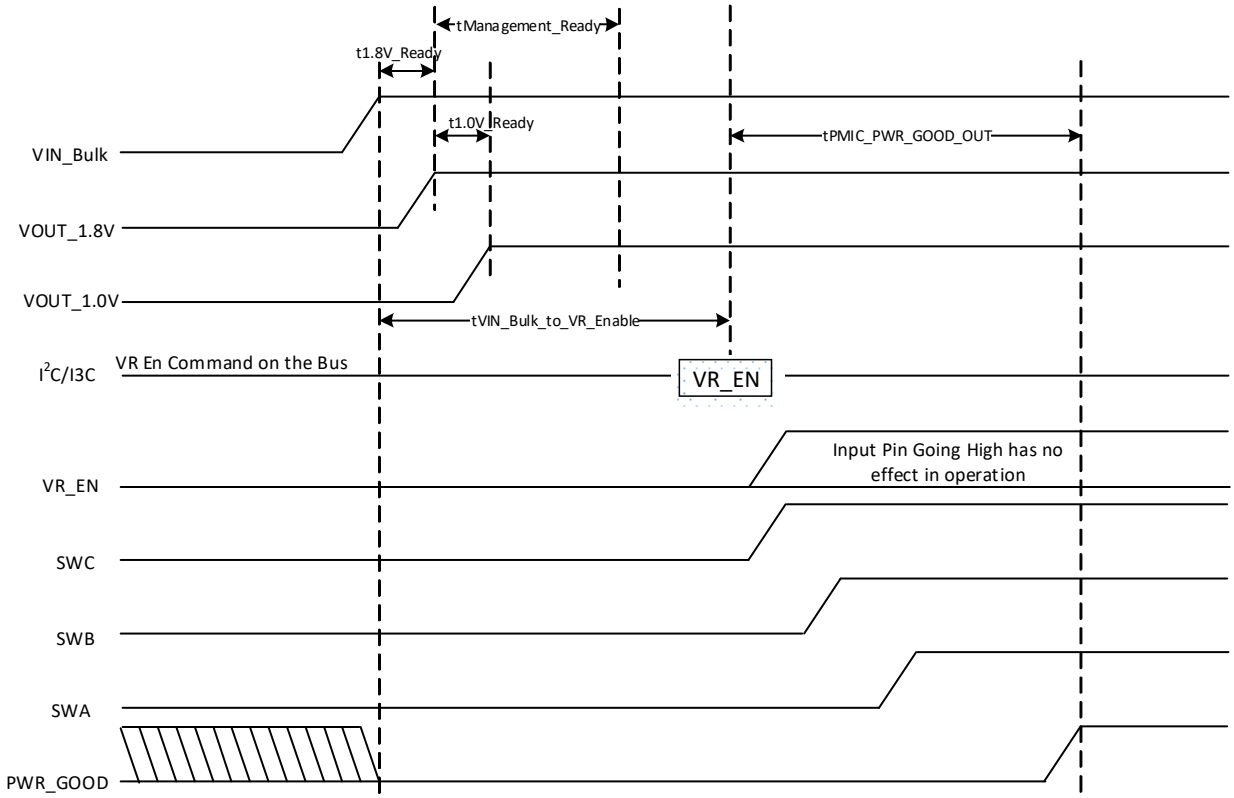


Figure 21 — PMIC Power Up Sequence; with Bus Command

6.2.1 Power Up Sequence (cont'd)

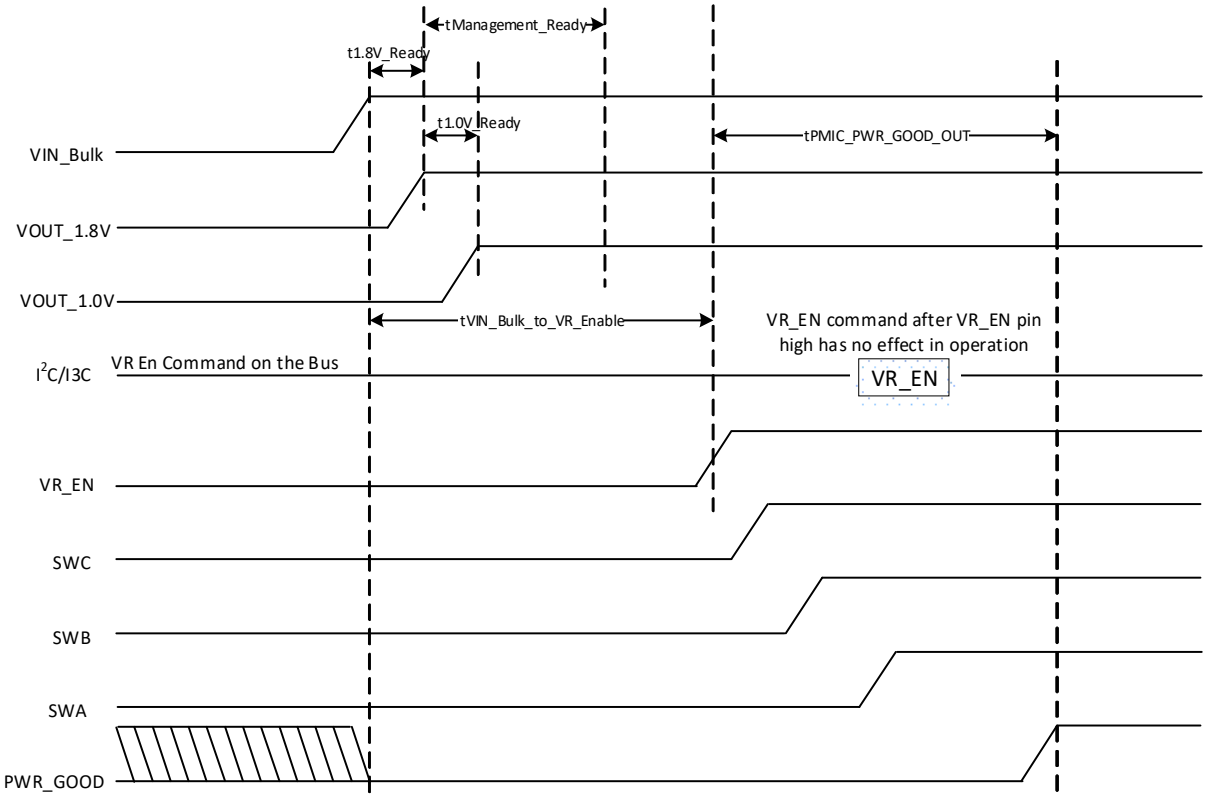


Figure 22 — PMIC Power Up Sequence; with VR_EN Pin followed by Bus Command

6.3 PMIC Output Rail Turn On Timing

Figure 23 shows the timing relationship once the PMIC receives VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) and when it floats PWR_GOOD output signal; timing parameter tPMIC_PWR_GOOD_OUT applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence configuration registers that are executed plus additional 5 ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config2 registers. Note that if more than one regulators are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 23 uses three power on sequence config0 to config2 registers and only one buck regulator is enabled in each power on sequence config 0 to config 2 registers.

6.3 PMIC Output Rail Turn On Timing (cont'd)

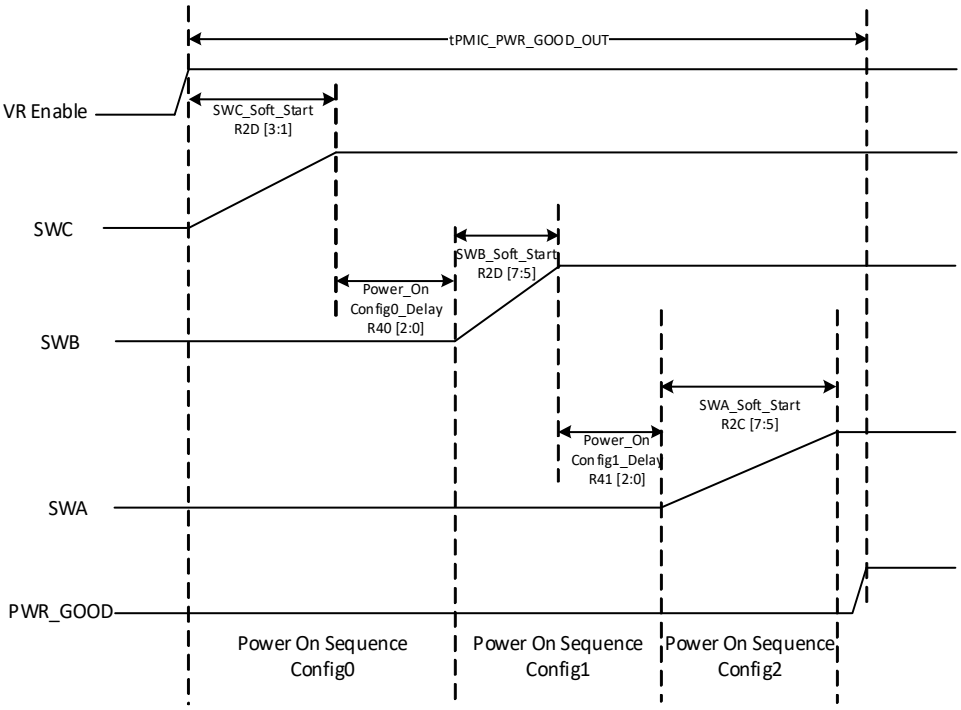


Figure 23 — PMIC Power On Timing

6.4 Secure Mode and Programmable Mode of Operation

Prior to issuing VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), the host must configure the register Table 143, Register 0x2F [2] appropriately as desired. The PMIC offers two modes of operation after VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) is registered.

1. Programmable Mode - In this mode, independent of when host issues VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), the PMIC allows modification to any register in the host region as desired by the host and PMIC responds appropriately.
2. Secure Mode - In this mode, after host issues VR Enable command (either with VR_EN pin or on I^2C/ I3C Basic bus), the PMIC does not allow modification to registers Table 117, Register 0x15 to Table 143, Register 0x2F, Table 146, Register 0x32 [7,5:0], Table 149, Register 0x35, or Table 150, Register 0x36 in the host region as well as Table 158, Register 0x40 to Register 0x6F in the DIMM vendor region and Register 0x70 through Register 0xFF in the PMIC vendor region.. These registers are write-protected marked with RED color cells in "Register" column in Table 94, Host Region - Register Map and in Table 95, DIMM Vendor Region - Register Map. The PMIC simply ignores the host request. Throughout this entire specification, when it refers to as PMIC allows access to the registers, it refers to write operation to the registers that are not write-protected in secure mode or programmable mode. There is no restriction for the read operation in secure mode or programmable mode. The host must power cycle the PMIC to make any modifications to the registers. The PMIC power cycle is defined as complete removal of VIN_Bulk input supply to the PMIC and this definition is applied to the entire specification.

6.4 Secure Mode and Programmable Mode of Operation (cont'd)

The PMIC does allow modification to any other remaining registers that are not marked in RED color cells in "Register" column in Table 94, Host Region - Register Map with I^2C or I3C Basic bus. The Secure Mode is only applicable once VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) is registered. This is important because by default Table 143, Register 0x2F [2] = '0' when PMIC is first powered up. Prior to VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus), PMIC allows modification to any registers in the host region.

Note that there is one exception in Secure mode of operation. The exception is for register Table 146, Register 0x32 [7]. This register can get updated with VR_EN pin assertion/de-assertion or PWR_GOOD signal input assertion to low or when PMIC internally generates its own VR Disable command due to some fault condition. This register cannot be updated with I^2C or I3C Basic bus command or with DEVCTRL CCC command.

6.5 Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on (with VR_EN pin or with VR Enable command on I^2C/ I3C Basic bus), the PMIC's output regulators are powered down as described below depending on PMIC's mode of operation.

6.5.1 Normal Power Down Sequence

Under normal operating condition with valid VIN_Bulk input supply, to disable the PMIC output regulators, the PMIC allows the following three methods for normal power down sequence.

- VR_EN pin de-assertion from High to Low
- VR Disable command on I^2C or I3C bus (if PMIC registers are not in secure mode)
- PWR_GOOD input from High to Low (if PWR_GOOD pin is configured as IO)

All three methods trigger the PMIC to generate an internal VR Disable command, after which the PMIC executes the normal power down sequence as programmed in Power Off Sequence Config0 to Power Off Sequence Config2 (Table 176, Register 0x58 to Table 178, Register 0x5A,), in DIMM vendor region MTP memory.

The PMIC requires a valid VIN_Bulk input supply (i.e., minimum of 4.25V) to execute the normal power down sequence. In a platform where the VIN_Bulk input supply ramp down rate is very slow (starting from VIN_Bulk nominal condition of 5V until it ramps down to 4.25V), the PMIC may be able to execute the normal power down sequence before the VIN_Bulk input supply is completely removed, depending on the ramp down rate, programmed soft stop time, and the delay time in the Power Off Sequence Config registers. If the VIN_Bulk ramp down is very fast (e.g. instantaneous with 0ns), the PMIC cannot execute the normal power down sequence to turn off all buck regulators.

Figure 24 shows one example of a normal power down sequence where PMIC regulators are turned off by de-asserting the VR_EN pin from high to low. The PMIC executes Power Off Sequence Config0 to Power Off Sequence Config2 (Table 176, Register 0x58 to Table 178, Register 0x5A,). The example shows the power down sequence spread out over all three Power Off Sequence Config (0 to 2) registers where only one buck regulator is turned off in each Power Off Sequence Config register. The sequence shows the order where SWA is turned off first followed by delay. Then SWB is turned off followed by delay. Lastly. SWC is turned off followed by delay. Each buck regulator follows its own timing for soft stop time, as configured.

The PMIC allows any combination where all three buck regulators can be turned off only in the first Power Off Sequence Config0 register, or one or more buck regulators can be turned off in any given Power Off Sequence Config register.

6.5.1 Normal Power Down Sequence (cont'd)

See additional details about PMIC register status, PWR_GOOD signal, as noted in Section 6.5.2 to Section 6.5.5, depending on how the PMIC is configured to operate in normal mode.

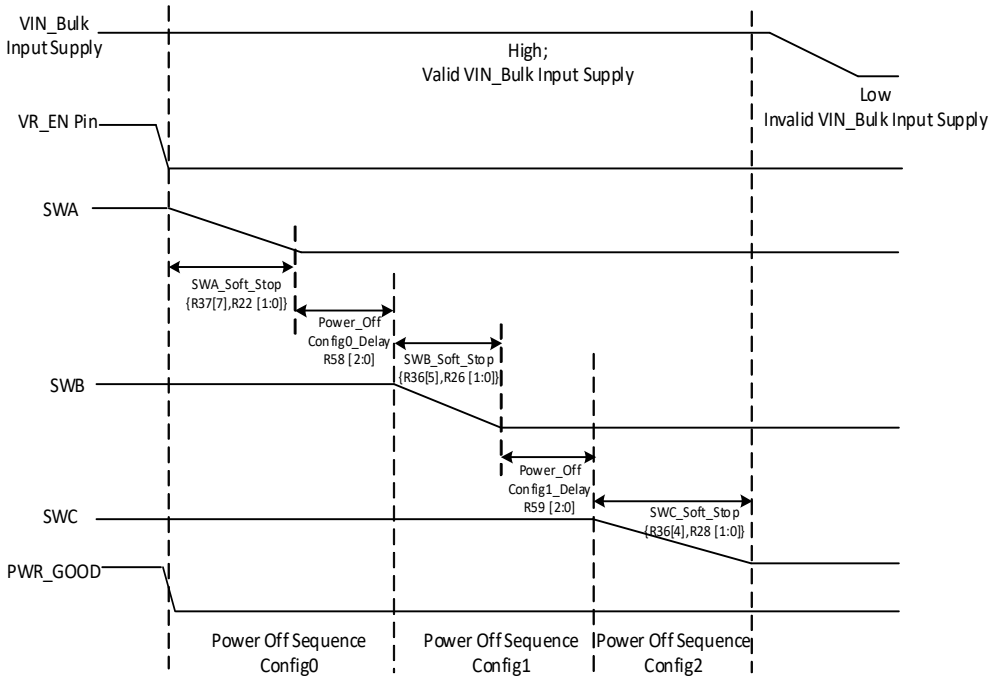


Figure 24 — Normal Power Down Sequence with VR Disable Command

6.5.2 Programmable Mode Operation; R1A[4] = '0'

The PMIC allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Table 146, Register 0x32 [7] = '0' or VR_EN pin transitions to low). The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:
   a. If VR Disable command with a pin (i.e., VR_EN pin transitions to Low), PMIC asserts PWR_-GOOD signal Low. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 25. The PMIC does not require power cycle.
   b. If VR Disable command on a I^2C/I3C Bus (i.e., Table 146, Register 0x32 [7] = '0'), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The host can re-enable the PMIC's output regulators by issuing VR_EN command on the I^2C/I3C bus (i.e., Table 146, Register 0x32 [7] = '1'). The PMIC executes power on sequence config 0 to power on sequence config 2 registers and continues to float the PWR_GOOD signal until tPMIC_PWR_GOOD_OUT time at which point, PMIC assumes normal control of PWR_GOOD signal. See Figure 26. The PMIC does not require power cycle.

6.5.2 Programmable Mode Operation; R1A[4] = '0' (cont'd)

c. The simultaneous usage of VR_EN pin and I^2C/I3C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet a and PWR_GOOD signal remains low even if there is a subsequent I^2C/I3C bus command as described in bullet b.

2. Configuring one or more bits in Table 143, Register 0x2F [6,4:3] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) on its own. The PMIC keeps the PWR_-GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Table 143, Register 0x2F [6,4:3] to '1' in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating. The PWR_GOOD signal behavior is same as in Figure 26.
3. If Table 146, Register 0x32 [5] = '1', driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_-GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. If host re-enables PMIC's output regulators by issuing VR_EN command on the I^2C/I3C Basic bus (i.e., Table 146, Register 0x32 [7] = '1'), the PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 30 under column "Trigger VR Disable". The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The PMIC asserts PWR_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either Table 146, Register 0x32 [7] = '1' or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

6.5.2 Programmable Mode Operation; R1A[4] = '0' (cont'd)

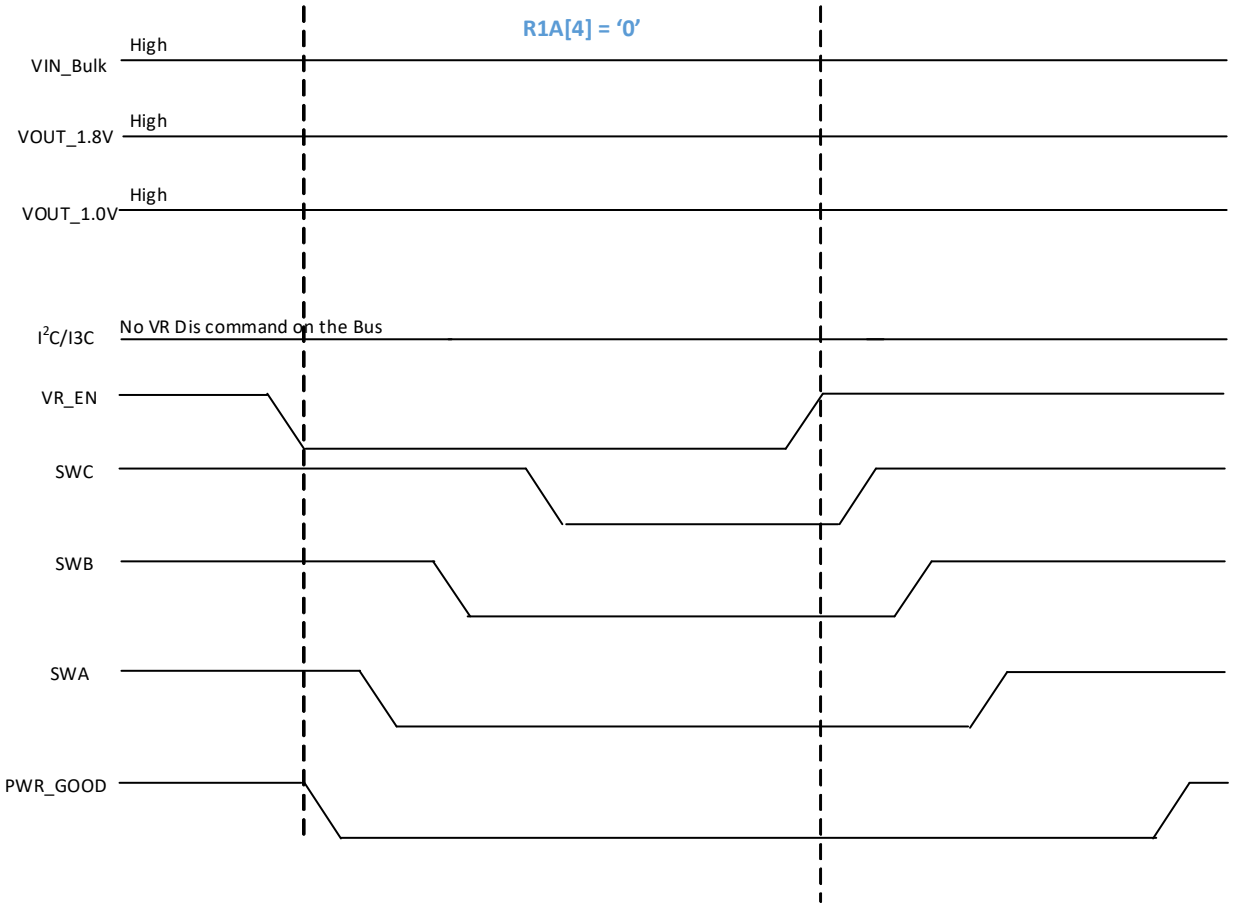


Figure 25 — Power Down with VR_EN Pin; R1A[4]=0; Programmable Mode; PWR_GOOD Signal

6.5.2 Programmable Mode Operation; R1A[4] = '0' (cont'd)

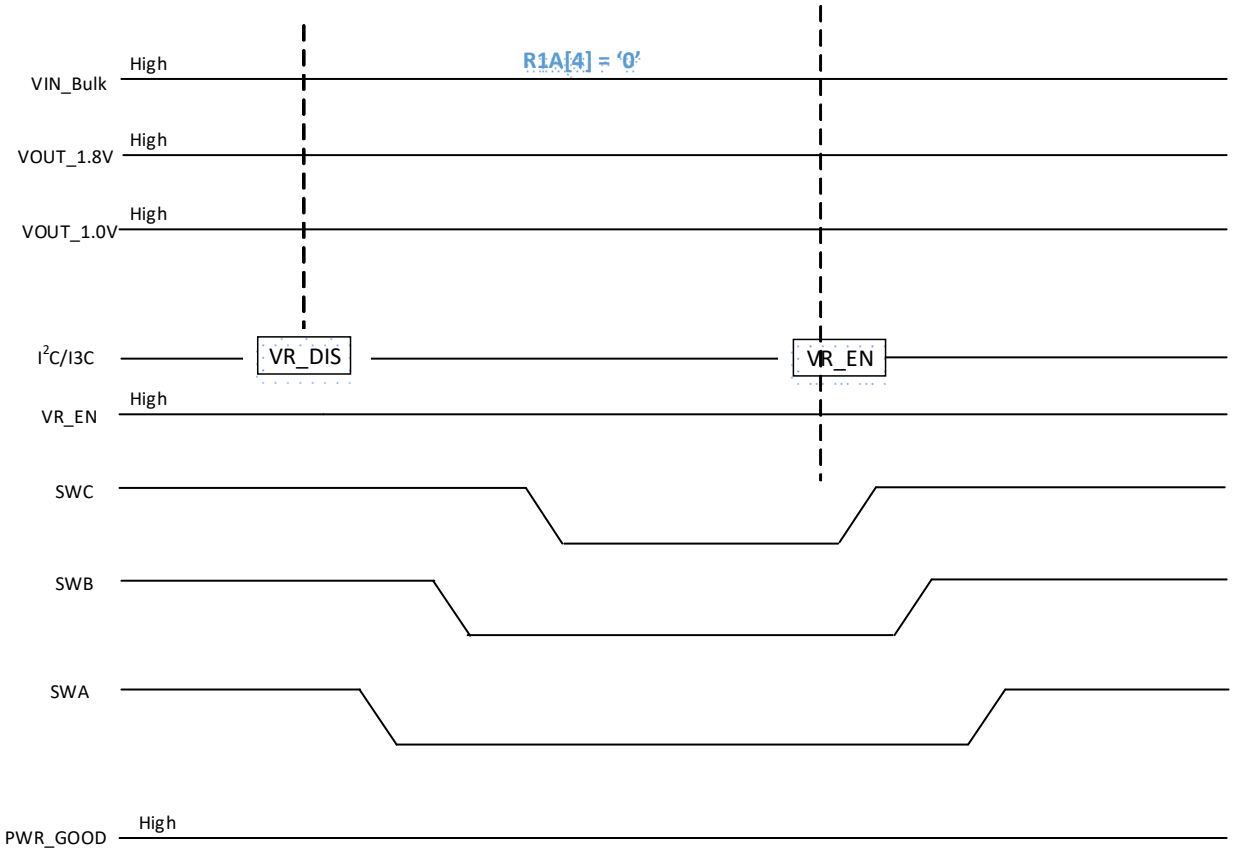


Figure 26 — Power Down with VR_DIS; R1A[4]=0; Programmable Mode; PWR_GOOD Signal

6.5.3 Programmable Mode Operation; R1A[4] = '1'

The PMIC allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Table 146, Register 0x32 [7] = '0' or VR_EN pin transitions to low). The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The PMIC controls the PWR_GOOD signal as following in bullet a and bullet b:
   a. If VR Disable command with a pin (i.e., VR_EN pin transitions to Low), PMIC asserts PWR_-GOOD signal Low. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 27. The PMIC does not require power cycle.

6.5.3 Programmable Mode Operation; R1A[4] = '1' (cont'd)

b. If VR Disable command on a I^2C/I3C Basic Bus (i.e., Table 146, Register 0x32 [7] = '0'), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The PMIC exits from P1 state with only VR_EN pin transition to High. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High and PMIC executes power on sequence config 0 to power on sequence config 2 registers. The PMIC continues to float PWR_GOOD signal until tPMIC_PWR_GOOD_OUT timing parameter is satisfied and at that point PMIC assumes normal control of PWR_GOOD signal. See Figure 28. The PMIC does not require power cycle.

c. The simultaneous usage of VR_EN pin and I^2C/I3C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in bullet a and PWR_GOOD signal remains low even if there is a subsequent I^2C/I3C bus command as described in bullet b.

2. Configuring one or more bits in Table 143, Register 0x2F [6,4:3] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in Table 143, Register 0x2F [6,4:3] to '1' in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating. The PWR_GOOD signal behavior is same as in Figure 28.
3. If Table 146, Register 0x32 [5] = '1', driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. The PMIC does not enter in P1 state. If host re-enables PMIC's output regulators by issuing VR_EN command on I^2C/I3C Basic bus (i.e., Table 146, Register 0x32 [7] = '1'), the PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 30 under column "Trigger VR Disable". The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either Table 146, Register 0x32 [7] = '1' or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

6.5.3 Programmable Mode Operation; R1A[4] = '1' (cont'd)

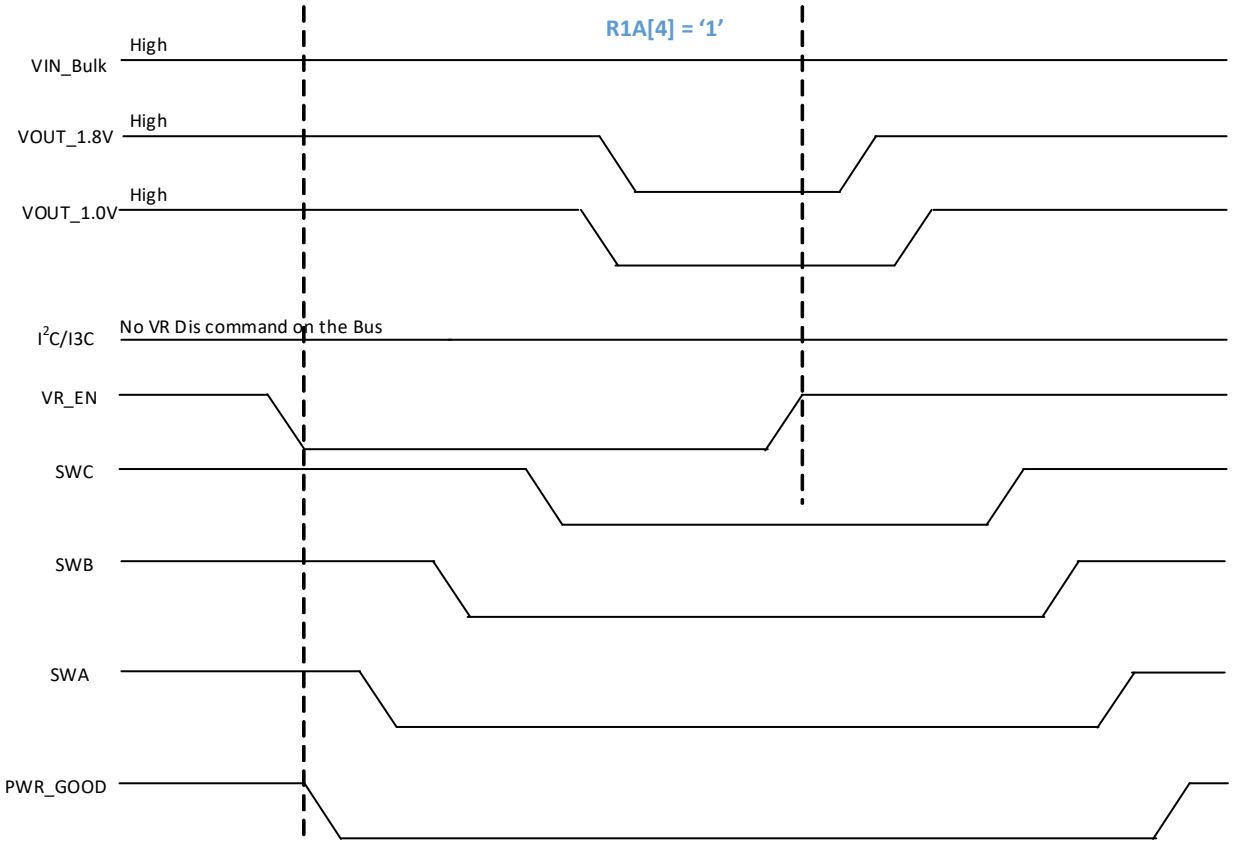


Figure 27 — Power Down with VR_EN Pin; R1A[4]=1; Programmable Mode; PWR_GOOD Signal

6.5.3 Programmable Mode Operation; R1A[4] = '1' (cont'd)

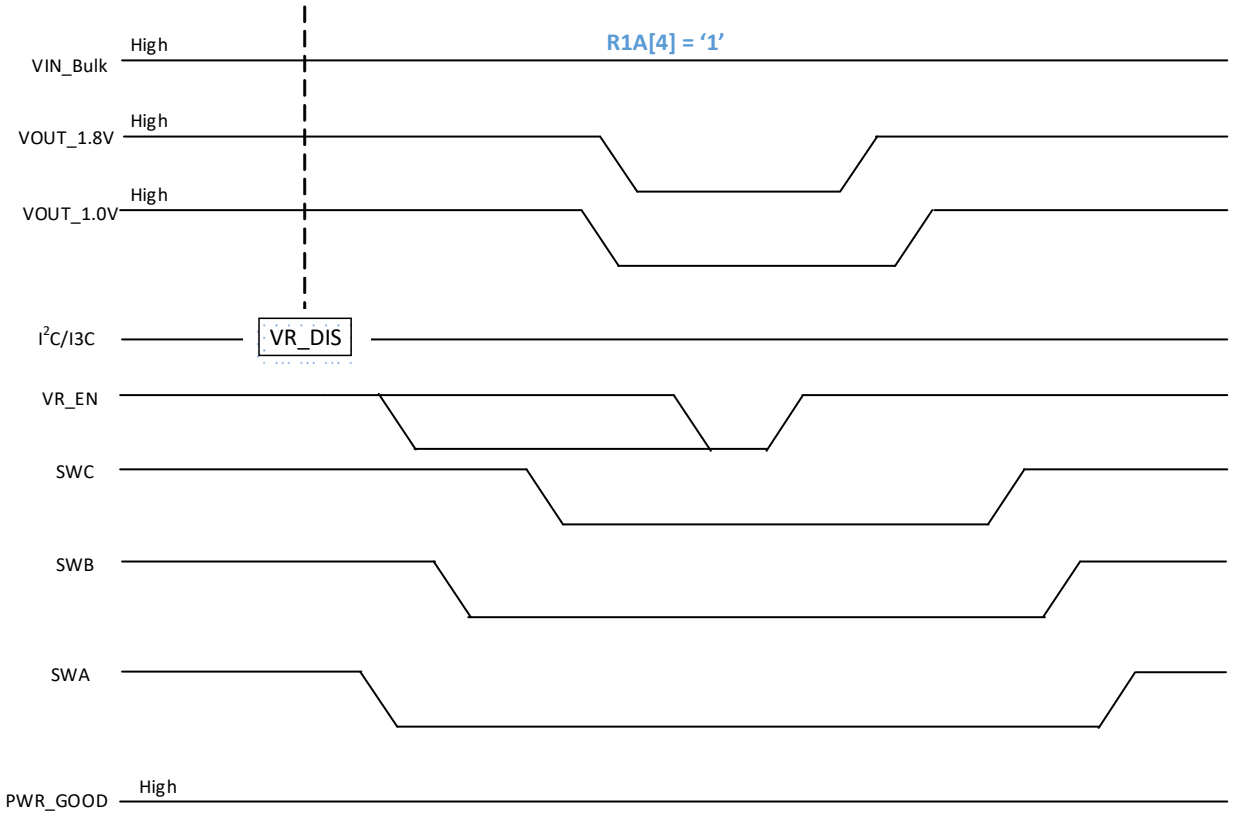


Figure 28 — Power Down with VR_DIS; R1A[4]=1; Programmable Mode; PWR_GOOD Signal

6.5.4 Secure Mode Operation; R1A[4] = '0'

The PMIC allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 29. The PMIC does not require power cycle.
    a. Note that VR Disable or Enable command on a I^2C/I3C Basic Bus (i.e., Table 146, Register 0x32 [7] = '0' or '1') has no effect on the PMIC. Also, configuring one or more bits in Table 143, Register 0x2F [6,4:3] to '0' has no effect on the PMIC. See Figure 30.

6.5.4 Secure Mode Operation; R1A[4] = '0' (cont'd)

2. If Table 146, Register 0x32 [5] = '1', driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_-GOOD signal low and unlocks only Table 146, Register 0x32 [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the Table 146, Register 0x32 [7]. When host issues VR Enable command by I^2C/I3C Basic bus, the PMIC executes Power on sequence config 0 to Power on sequence config 2 registers, floats PWR_-GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks register Table 146, Register 0x32 [7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 30 under column "Trigger VR Disable". The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either Table 146, Register 0x32 [7] = '1' or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

6.5.5 Secure Mode Operation; R1A[4] = '1'

The PMIC allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config 0 to config 2 registers and floats PWR_GOOD signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied. See Figure 29. The PMIC does not require power cycle.
   a. Note that VR Disable or Enable command on a I^2C/I3C Basic Bus (i.e., Table 146, Register 0x32 [7] = '0' or '1') has no effect on the PMIC. Also, configuring one or more bits in Table 143, Register 0x2F [6,4:3] to '0' has no effect on the PMIC. See Figure 30.
2. If Table 146, Register 0x32 [5] = '1', driving PWR_GOOD input low. The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers; drives PWR_-GOOD signal low and unlocks only Table 146, Register 0x32 [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the Table 146, Register 0x32 [7]. The PMIC does not enter in P1 state. When host issues VR Enable command by I^2C/I3C Basic bus, the PMIC executes Power on sequence config 0 to Power on sequence config 2 registers, floats PWR_GOOD output signal after tPMIC_PWR_GOOD_OUT timing parameter is satisfied and re-locks register Table 146, Register 0x32 [7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in Table 30 under column "Trigger VR Disable". The PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either Table 146, Register 0x32 [7] = '1' or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

6.5.5 Secure Mode Operation; R1A[4] = '1' (cont'd)

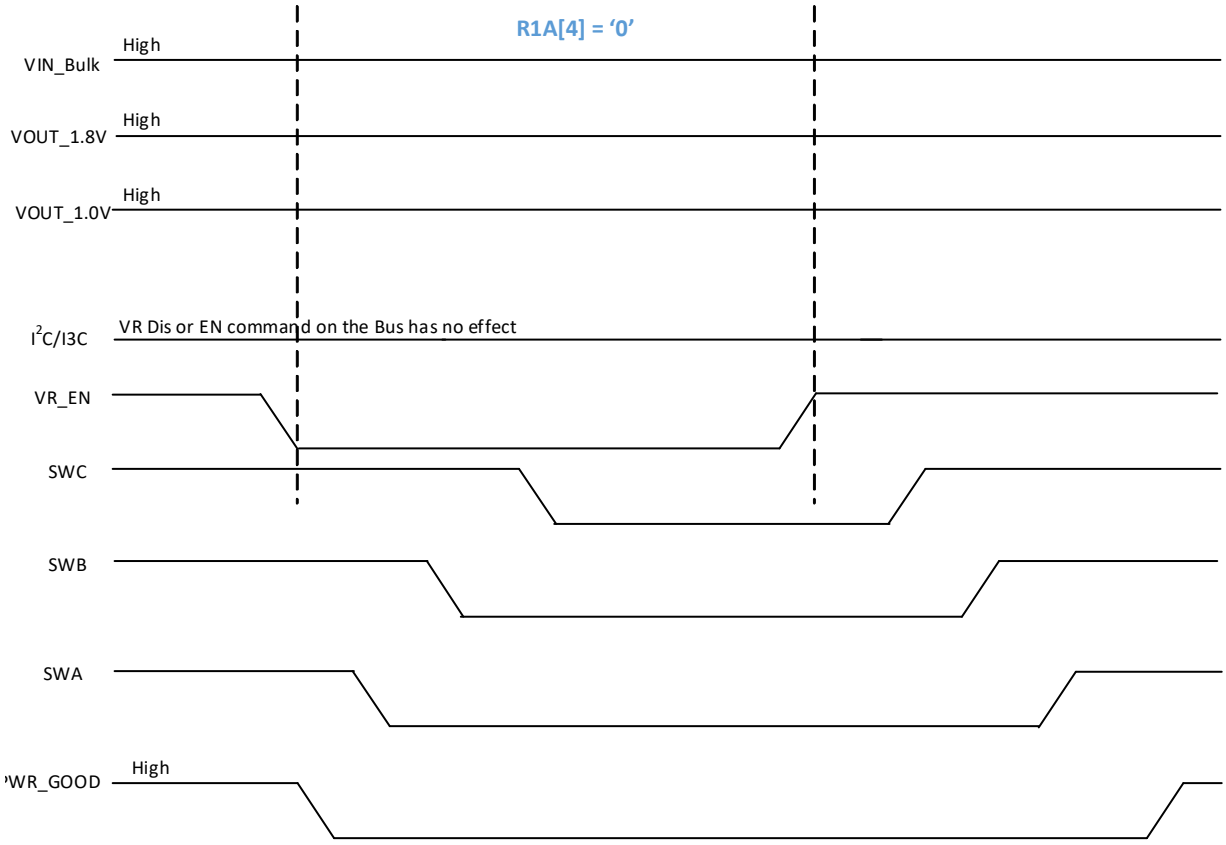


Figure 29 — Power Down with VR_EN Pin; R1A[4]=0; Secure Mode; PWR_GOOD Signal

6.5.5 Secure Mode Operation; R1A[4] = '1' (cont'd)

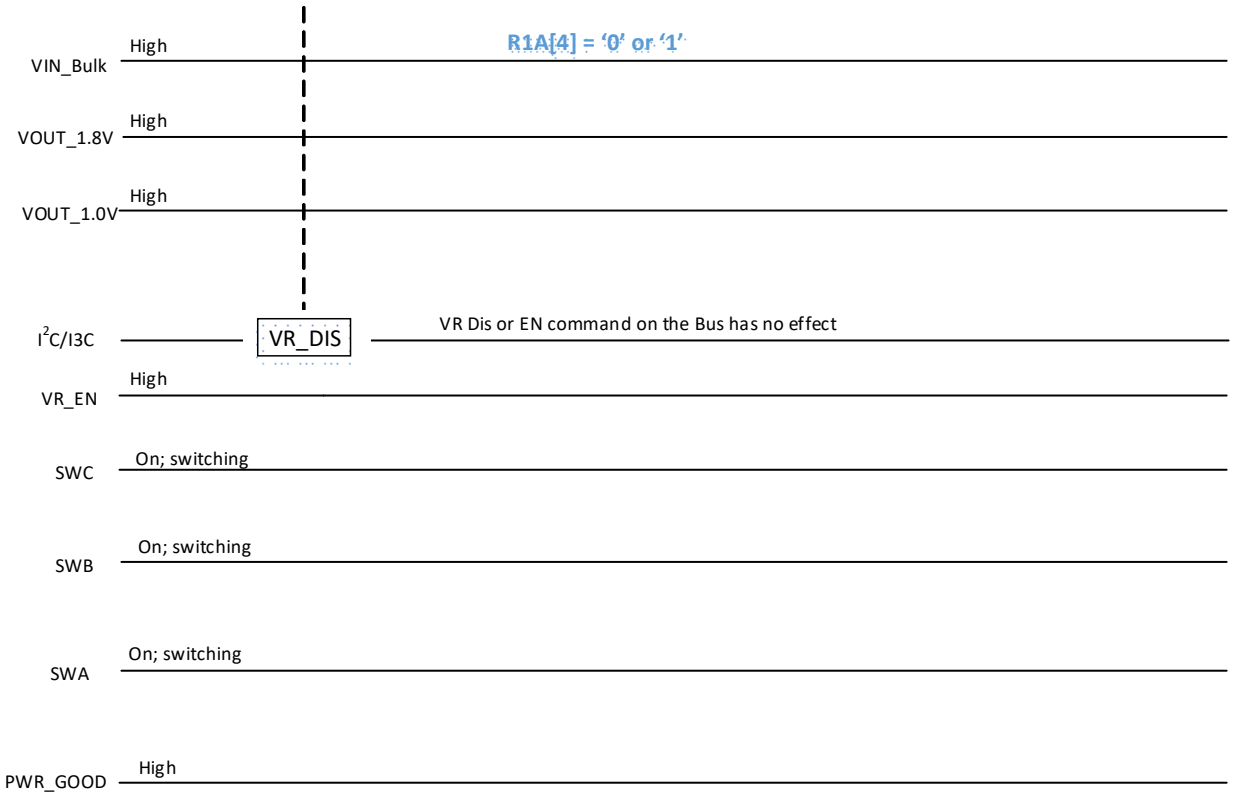


Figure 30 — VR_DIS or VR_EN CMD on Bus; R1A[4]=x; Secure Mode; PWR_GOOD Signal

6.5.5 Secure Mode Operation; R1A[4] = '1' (cont'd)

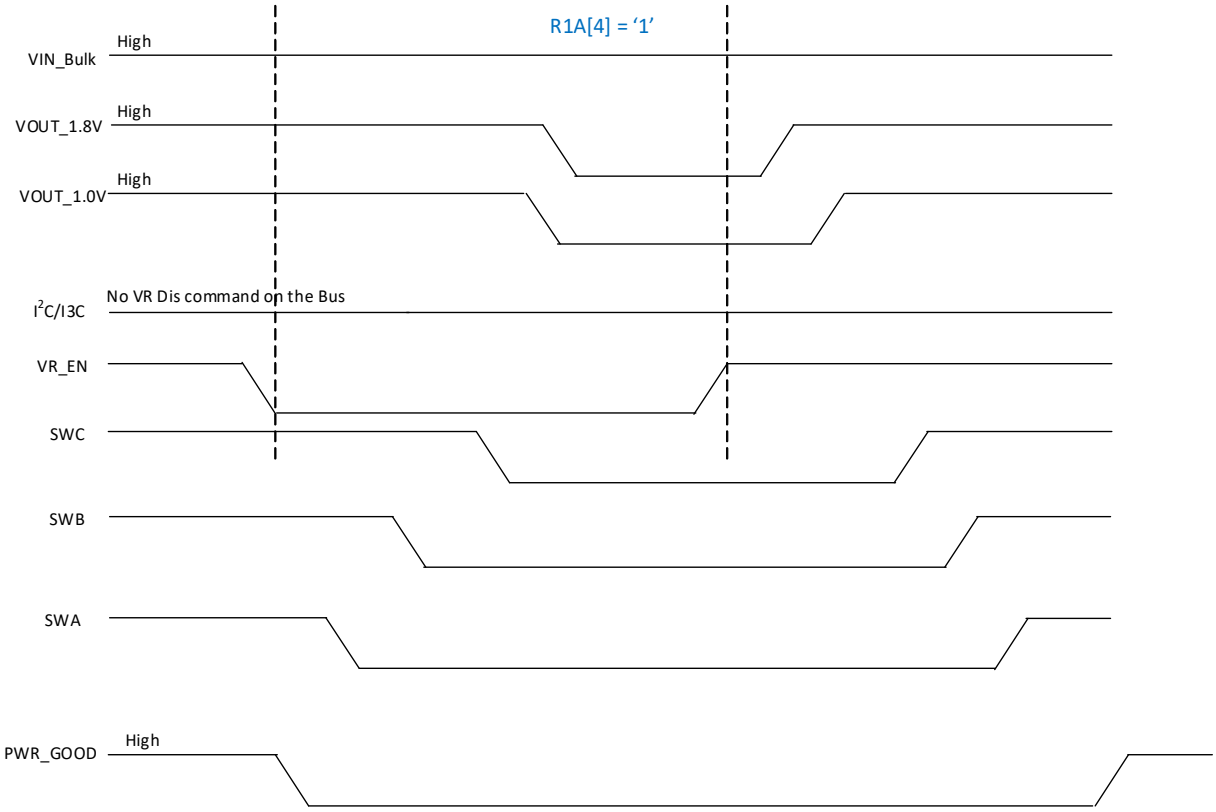


Figure 31 — Power Down with VR_EN Pin; R1A[4]=1; Secure Mode; PWR_GOOD Signal

6.6 PMIC Output Rail Off Timing

Figure 32 shows the timing relationship once the PMIC registers VR Disable command internally due to fault condition as listed in Table 30. The waveform shows each buck regulator output soft stop time and delay time once the soft stop time expires from each power off sequence config0 to power off sequence config2 registers. Note that if more than one regulators are disabled in a power off sequence config register and if those regulators have different soft stop time programmed, then the larger value of that soft stop time is used as a reference for delay timer to start. Each regulator will still follow different soft stop time to turn off the buck regulator.

The specific example in Figure 32 uses only three power off sequence config0 to config2 registers and only one buck regulator is disabled in power off sequence config 0, config 1 and config 2 registers.

6.6 PMIC Output Rail Off Timing (cont'd)

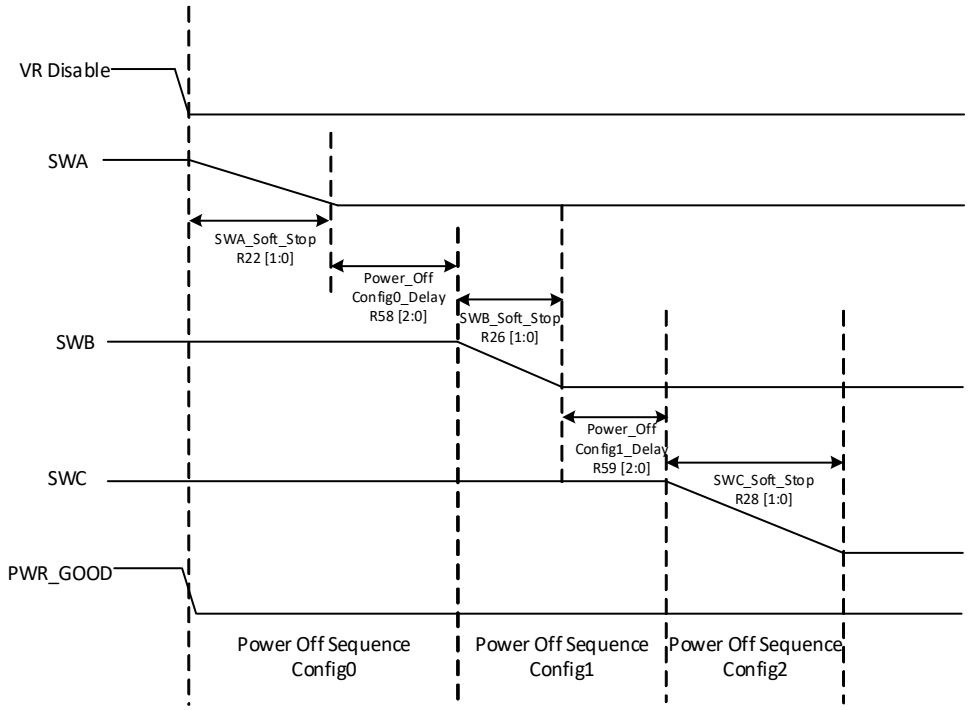


Figure 32 — PMIC Power Off Timing Due to Internal Fault Condition

6.6.1 Power Down Output Regulators During Power On Sequence

During power on as described in Section 6.2 it is possible that PMIC can trigger VR Disable command on its own as described in Table 30 when one or more regulators are already turned on even while other remaining output regulators are not yet turned on because PMIC has not completed the power on sequence config registers. For these type of cases, the PMIC will not execute the remaining power on sequence config registers and will immediately jump to executing the power off sequence config0 to power off sequence config2 registers. The PMIC will update the status registers and error log registers appropriately as normal because it generated VR Disable command on its own. The PWR_GOOD output signal would remain low.

6.7 Power Good (PWR_GOOD) Signal

The PWR_GOOD output signal type can be configured as either output only or input and output through register Table 146, Register 0x32 [5]. By default, PWR_GOOD is an output signal. The PWR_GOOD signal can only be configured once, at power on, before issuing VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus). The PWR_GOOD signal configuration applies to both secure mode or programmable mode of operation.

Section 6.7.1, Section 6.7.2, Table 27, and Table 28 describe PMIC's behavior.

6.7 Power Good (PWR_GOOD) Signal (cont'd)

Table 27 — PMIC Operation; PWR_GOOD Type: Input and Output

External PWR_GOOD Input	PMIC's Internal PWR_GOOD	PMIC Operation	Notes
High	High	High (Power Good); Normal Operation	
High	Low	Low (Power Not Good); PMIC Communicates its Status; See Section 6.7.1 for more information	1,2
Transition from High to Low	High	Low(Power Good); PMIC Executes VR Disable Command	3
Low	Low	Low (Power Not Good); PMIC Internally Generates VR Disable Command	

NOTE 1 The PMIC indicates its own internal status and it may shut down on its own by following Power Off Config0 to Power Off Config2 sequence.
NOTE 2 This is a transient state and the net results of the PWR_GOOD signal is Low.
NOTE 3 The PMIC shuts down based on external command by following Power Off Config0 to Power Off Config2 sequence.

Table 28 — PMIC Operation; PWR_GOOD Type: Output Only

External PWR_GOOD Input	PMIC's Internal PWR_GOOD	PMIC Operation	Notes
X (High or Low)	High	(Power Good); Normal Operation	
X (High or Low)	Low	(Power Not Good); PMIC communicates its status; See Section 6.7.1 for more information	1

NOTE 1 The PMIC indicates its own internal status and it may shut down on its own by following Power Off Config0 to Power Off Config2 sequence.

6.7.1 PWR_GOOD as Output Only Signal

When Table 146, Register 0x32 [5] = '0', the PWR_GOOD signal type is output only; the input of PWR_GOOD signal is ignored.

The PMIC PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V). The PMIC floats PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator's (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power up, when input supply VIN_Bulk is ramped up and stable, the PMIC keeps PWR_GOOD pin asserted to low; however PMIC updates corresponding status register. By default, the register Table 146, Register 0x32 [5] = '0'. Once PMIC receives VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus) from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters into operating state called as "Regulation". At this point, PMIC floats PWR_GOOD pin and the external board pullup resistor pulls the pin high as there may be other PMIC on different DIMM may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e., no other PMIC is driving the PWR_GOOD pin low), the PMIC remains in "Regulation" state.

6.7.1 PWR_GOOD as Output Only Signal (cont'd)

Once the PWR_GOOD pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) that causes the PMIC to update its status registers to indicate the power status is not good, then PMIC asserts PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR_GOOD pin float (i.e., get High) even if the condition that triggered the PMIC to assert the PWR_GOOD pin no longer exists. In other words, the PMIC's PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the host.

If PMIC is operating in Secure mode of operation, see Section 6.5.4 and Section 6.5.5 for additional information.

If PMIC is in Programmable mode of operation, see Section 6.5.2 and Section 6.5.3 for additional information.

6.7.2 PWR_GOOD as Input and Output Signal

When Table 146, Register 0x32 [5] = '1', the PWR_GOOD signal type is both input and output and is only applicable after host issues VR Enable command (either with VR_EN pin or on I^2C/I3C Basic bus). Also note that simultaneous usage of the PWR_GOOD pin as IO and the VR_EN pin is not allowed and considered an illegal configuration. In other words, if the VR_EN pin is intended to be used to turn on and turn off output rails, the PWR_GOOD pin must be configured as output only. If the PWR_GOOD pin is intended to be used as IO, the VR_EN pin must be connected to GND on the board.

The PMIC PWR_GOOD pin indicates status of VIN_Bulk input supply and all output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V). The PMIC floats the PWR_GOOD pin when VIN_Bulk input supply is valid and all enabled output regulator's (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power up, when input supply VIN_Bulk is ramped up and stable, the PMIC keeps the PWR_GOOD pin asserted to low; however PMIC updates corresponding status register. The host, prior to issuing VR Enable command on I^2C/I3C Basic bus, can configure the register Table 146, Register 0x32 [5] = '1'. When host issues VR Enable command on I^2C/I3C Basic bus, the PMIC turns on its output regulators and updates corresponding status registers and enters into operating state called "Regulation". At this point, the PMIC floats the PWR_GOOD pin and waits for the external board pullup resistor to pull the pin high as there may be other PMICs on different DIMMs that may be driving the PWR_GOOD pin low. Once the PWR_GOOD pin is pulled high (i.e., no other PMIC is driving the PWR_GOOD pin low), the PMIC automatically enters in to operating state called "Bulk Control Link Monitor".

Once the PWR_GOOD pin is high, if PMIC detects any condition either on VIN_Bulk input supply or any of the output regulators (VOUT_A, VOUT_B, VOUT_C, VOUT_1.8V, VOUT_1.0V) that causes the PMIC to update its status registers to indicate the power status is not good, then the PMIC asserts the PWR_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR_GOOD pin float (i.e., get High) even if the condition that triggered the PMIC to assert the PWR_GOOD pin no longer exists. In other words, the PMIC's PWR_GOOD pin is latched and once latched, it must be explicitly addressed by the host.

In this "Bulk Control Link Monitor" operating state, the PMIC's behavior is as follows:

If the PMIC is operating in Secure mode of operation, see Section 6.5.4 and Section 6.5.5 for additional information.

- The PMIC allows the PWR_GOOD input signal low at any time. The host must keep the PWR_GOOD signal low for a minimum of tPWR_GOOD_Low_Pulse_Width to issue a command to the PMIC to execute VR Disable. When the PMIC detects the PWR_GOOD signal low, the PMIC internally triggers a VR Disable command, shuts off all output regulators (the PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,)), drives the PWR_GOOD signal low, and unlocks only Table 146, Register 0x32 [7].

6.7.2 PWR_GOOD as Input and Output Signal (cont'd)

- The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the Table 146, Register 0x32 [7]. As long as there is a valid VIN_Bulk input supply, the PMIC allows read access to all its configuration registers. The PMIC allows write access to non-locked configuration registers and register Table 146, Register 0x32 [7]. If the host issues a VR Enable command on the I^2C/I3C bus, the PMIC executes the Power on sequence config0 to Power on sequence config2 registers, floats the PWR_GOOD signal and re-locks register Table 146, Register 0x32 [7].

If the PMIC is in Programmable mode of operation, see Section 6.5.4 and Section 6.5.5 for additional information.

- The PMIC allows the PWR_GOOD input signal low at any time. The host must keep the PWR_GOOD signal low for a minimum of tPWR_GOOD_Low_Pulse_Width to issue a command to the PMIC to execute VR Disable. When the PMIC detects the PWR_GOOD signal low, the PMIC internally triggers a VR Disable command, shuts off all output regulators (the PMIC executes power off sequence config0 (Table 176, Register 0x58) to power off sequence config2 (Table 178, Register 0x5A,)), and drives the PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. As long as there is a valid VIN_Bulk input supply, the PMIC allows read and write access to all its configuration registers. The host can issue a VR_EN command on the I^2C/I3C Basic bus (i.e., Table 146, Register 0x32 [7] = '1') again to turn on the PMIC's output regulator, and the PMIC will execute the Power On Config0 to Config2 registers and float the PWR_GOOD signal.

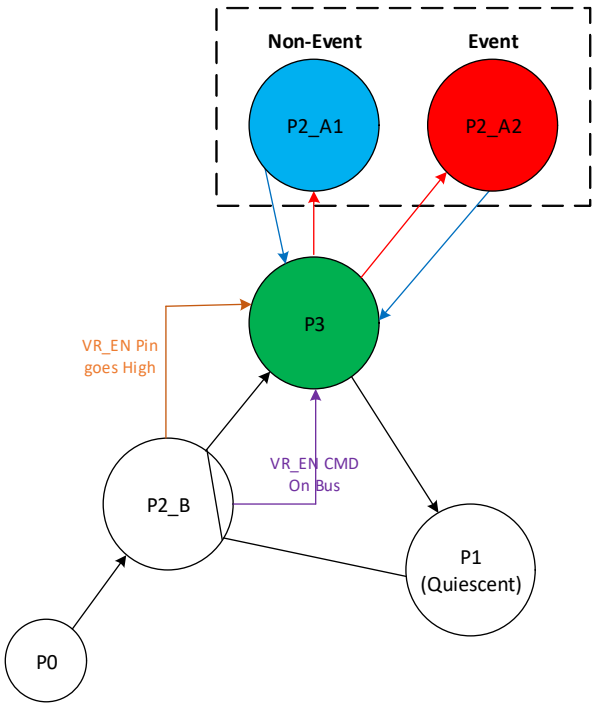
6.8 Idle Condition and Quiescent Power State

Quiescent Power State definition: All circuits including PMIC switch output and LDO output regulators are off. VR_EN signal is at static low or high level. I^2C or I3C Basic interface access is not allowed and is pulled high. PID signal is at static low or high level. This state is only applicable if Table 122, Register 0x1A [4] = '1'. This state is labeled as P1 state in Figure 33.

Idle Condition definition: All circuits including PMIC switch output and LDO output regulators are on with 0 A load. VR_EN signal is at static low or high level. I^2C or I3C Basic interface access is allowed but bus is pulled high. PID signal is at static low or high level.

Figure 33 shows high level PMIC states and its definition. The state transitions from each state is defined in Table 29.

6.8 Idle Condition and Quiescent Power State (cont'd)



P0 State:
-- VIN_Bulk invalid

P1 State:
-- R1A[4] = '1'
-- Entry from P3 State Only

P2_B State:
-- Transition from P0 or P1 State; Before VR Enable Command
-- All Switch Regulators are Off
-- All LDOs are on
-- PWR_GOOD Output = L
-- VR_EN Input = L
-- R32[7] = '0'

P2_A1 State (No Fault Event):
-- Transition from P3; After VR Enable Command
-- All Switch Regulators are Off
-- All LDOs are on
-- PWR_GOOD Output = L or H
-- VR_EN Input = L or H
-- R32[7] = '0'

P2_A2 State (Fault Event):
-- Transition from P3; After VR Enable Command
-- All Switch Regulators are Off
-- All LDOs are ON
-- PWR_GOOD Output = L
-- VR_EN Input = L or H
-- R32[7] = '0'

P3 State (Regulation Mode or Bulk Link Monitor Mode)
-- All Switch Regulators are On
-- R32[7] = '1'

Figure 33 — State Definition and Transitions

6.8 Idle Condition and Quiescent Power State (cont'd)

Table 29 — State Transitions

Start State	Activity	Register Setting			End State	PWR_GOOD Output[1]	Power Cycle Required?	Note
		R2F[2]	R32[5]	R1A[4]				
P0	Valid VIN_Bulk	N/A	N/A	N/A	P2_B	Low	N/A	
P1	VR_EN; High to Low	X	X	X	N/A			
	VR_EN Pin; Low to High	X	X	0	N/A			
		X	X	1	P3	Hi-Z	No	
	VR_DIS CMD on I2C/I3C Bus	X	X	1	P1	No Change	N/A	
	VR_EN CMD on I2C/I3C Bus	X	X	1	P1	No Change	N/A	
P2_B	VR_EN Pin Transition to High	X	0	X	P3	Hi-Z	N/A	
		X	1	X	Illegal Configuration			2
	VR_EN CMD on Bus	X	X	X	P3	Hi-Z	N/A	
P3	VR_EN Pin; High to Low	X	0	0	P2_A1	Low		
		X	0	1	P1	Low		
		X	1	X	Illegal Configuration			2
	VR_EN Pin; Low to High	X	X	X	P3	Hi-Z	N/A	3
	VR_DIS CMD on I2C/I3C Bus	1	X	0	P2_A1	Hi-Z		
		1	X	1	P1	Hi-Z		
		0	X	X	P3	Hi-Z	N/A	
	VR_EN CMD on I2C/I3C Bus	X	X	X	P3	Hi-Z	N/A	4
	PWR_GOOD Input Low	X	0	X	P3	Hi-Z	N/A	5,6
		1	1	X	P2_A1	Low		6
		0	1	X	P2_A1	Low		6
	Internal VR Disable Event	0	X	X	P2_A2	Low	Yes	
		1	X	X	P2_A2	Low	No	7
	VIN_Bulk Invalid	X	X	X	P0	N/A	N/A	
P2_A1	VR_EN Pin; High to Low	X	X	X	No Change	No Change	N/A	8
	VR_EN Pin; Low to High	X	1	X	Illegal Configuration			2
		X	0	0	P3	Hi-Z	No	
		X	0	1	N/A			9
	VR_DIS CMD on I2C/I3C Bus	X	X	X	No Change	No Change	N/A	10
	VR_EN CMD on I2C/I3C Bus	0	0	0	No Change	No Change	N/A	
		0	1	X	P3	Hi-Z	No	
		0	0	1	N/A	N/A	N/A	
		1	X	0	P3	Hi-Z	No	
		1	1	1	P3	Hi-Z	No	
		1	0	1	N/A			7
	Internal VR Disable Event	0	X	X	P2_A2	Low	Yes	
		1	X	X	P2_A2	Low	No	7,11
	VIN_Bulk Invalid	X	X	X	P0	N/A	N/A	

Table 29 — State Transitions (cont'd)

Start State	Activity	Register Setting			End State	PWR_GOOD Output[1]	Power Cycle Required?	Note
		R2F[2]	R32[5]	R1A[4]				
P2_A2	VR_EN Pin; High to Low	X	X	X	No Change	No Change	N/A	12
	VR_EN Pin; Low to High	0	X	X	P2_A2	Low	Yes	
		1	0	0	P3	Hi-Z	No	
		1	0	1	P3	Hi-Z	No	
		1	1	X	Illegal Configuration			2
	VR_EN CMD on I^2C/I3C Bus	0	X	X	P2_A2	Low	Yes	
		1	X	0	P3	Hi-Z	No	
		1	0	1	P3	Hi-Z	No	
		1	1	1	P3	Hi-Z	No	
	Internal VR Disable Event	0	X	X	No Change	No Change	Yes	
		1	X	X	No Change	No Change	No	7,11
	VIN_Bulk Invalid	X	X	X	P0	N/A	N/A	

NOTE 1 This represents PMIC's PWR_GOOD output signal; all power is good; no fault event.
NOTE 2 Simultaneous usage of VR_EN pin and PWR_GOOD IO type (Table 146, Register 0x32 [5] = '1') is not allowed and considered an illegal configuration. If VR_EN pin is intended to be used to turn on or off output rails, PWR_GOOD signal must be configured as O only (i.e., Table 146, Register 0x32 [5] = '0'). VR_EN pin must be tied to GND if PWR_GOOD signal is intended to be configured as IO (Table 146, Register 0x32 [5] = '1').
NOTE 3 PMIC is already in P3 state. It assumes PMIC entered in P3 state with VR_EN command on I^2C/I3C bus.
NOTE 4 PMIC is already in P3 state. It assumes PMIC entered in P3 state with VR_EN pin transition to High.
NOTE 5 PMIC PWR_GOOD IO Type is configured as Output Only.
NOTE 6 PMIC's input of PWR_GOOD is Low. But internally, PMIC's PWR_GOOD output signal is Hi-Z.
NOTE 7 PMIC allows to re-enable output regulators with VR Enable command (either with VR_EN pin or on I^2C/I3C bus) assuming that event is no longer present and status registers are cleared.
NOTE 8 PMIC is already in P2_A1 state and so VR_EN pin transition has no meaning.
NOTE 9 Since Table 122, Register 0x1A [4] = '1', the PMIC never enters into P2_A1 state if there is no event, PMIC always enters in P1 state.
NOTE 10 PMIC is already in P2_A1 state with VR_EN pin. So VR_DIS command on the bus has no effect.
NOTE 11 Power cycle is always required if there is a thermal shutdown regardless of the register Table 143, Register 0x2F [2] setting.
NOTE 12 PMIC is already in P2_A2 state and so VR_EN pin transition has no meaning.

6.9 GSI_n Signal

General Status Interrupt (GSI_n) is an Open Drain output signal. By default at power on, GSI_n output is disabled. The host can enable the GSI_n output by setting Table 123, Register 0x1B [3] = '1'. Typically, GSI_n output is pulled up to 1KΩ resistor to 1.8 V or 3.3 V. The PMIC asserts GSI_n output for the events as described in Table 30.

6.10 Function Interrupt - PWR_GOOD and GSI_n Output Signals

This section defined the output functionality of GSI_n pin and PWR_GOOD (Table 146, Register 0x32 [5] = '0') pin.

When mask register bits are not set, the PMIC asserts its GSI_n output and assert PWR_GOOD output signals as shown in Table 30 when any event occurs. The table also highlights 9 events that cause the PMIC to internally generate a VR Disable command. For remaining events that do not trigger internal VR Disable command, the PMIC continues to operate as normal.

6.10 Function Interrupt - PWR_GOOD and GSI_n Output Signals (cont'd)

Table 30 — Events Interrupt Summary

Event	Status Bit	Clear Bit	Mask Bit	Threshold Bits	Trigger VR Disable?	PWR_GOOD Output	GSI_n Output
VIN_Bulk Over Voltage	R08 [0]	R10 [0]	R15 [0]	R1B [7]	Yes	Low	Low
SWA Output Power Good	R08 [5]	R10 [5]	R15 [5]	R21 [1]; R22 [7:6]	No	Low	Low
SWB Output Power Good	R08 [3]	R10 [3]	R15 [3]	R25 [1]; R26 [7:6]	No	Low	Low
SWC Output Power Good	R08 [2]	R10 [2]	R15 [2]	R27 [1]; R28 [7:6]	No	Low	Low
1.8 V LDO Power Good	R09 [5]	R11 [5]	R16 [5]	R1A [2]	No	Low	Low
1.0 V LDO Power Good	R33 [2]	R14 [2]	R19 [2]	R1A [0]	No	Low	Low
SWA Output Over Voltage	R0A [7]	R12 [7]	R17 [7]	R22 [5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A [5]	R12 [5]	R17 [5]	R26 [5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A [4]	R12 [4]	R17 [4]	R28 [5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B [3]	R13 [3]	R18 [3]	R22 [3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B [1]	R13 [1]	R18 [1]	R26 [3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B [0]	R13 [0]	R18 [0]	R28 [3:2]	Yes	Low	Low
VIN_Bulk Input Under Voltage	R33[3]	R14[3]	R19[3]	Vendor Specific	Yes	Low	Low
SWA Output Current Limit	R0B [7]	R13 [7]	R18 [7]	R20 [7:6]	No	High	Low
SWB Output Current Limit	R0B [5]	R13 [5]	R18 [5]	R20 [3:2]	No	High	Low
SWC Output Current Limit	R0B [4]	R13 [4]	R18 [4]	R20 [1:0]	No	High	Low
SWA Output High Current/Power	R09 [3]	R11 [3]	R16 [3]	R1C [7:2]	No	High	Low
SWB Output High Current/Power	R09 [1]	R11 [1]	R16 [1]	R1E [7:2]	No	High	Low
SWC Output High Current/Power	R09 [0]	R11 [0]	R16 [0]	R1F [7:2]	No	High	Low
High Temperature Warning	R09 [7]	R11 [7]	R16 [7]	R1B [2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E [2:0]	Yes	Low	Low
PEC Error	R0A [3]	R12 [3]	R17 [3]	N/A	No	High	Low
Parity Error	R0A [2]	R12 [2]	R17 [2]	N/A	No	High	Low

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or PWR_GOOD signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or PWR_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 31 and Table 32 shows the PMIC's response of GSI_n signal and PWR_GOOD output signal for each event before and after host issues the Clear command. Table 31 and Table 32 assume that all mask bits are either '0' or '1' for simplicity.

6.10 Function Interrupt - PWR_GOOD and GSI_n Output Signals (cont'd)

Table 31 — PMIC Response for Clear Command by Host - 1

	Event Occurred; All Mask Bits = '0'		Clear Command; Event Not Present; All Mask Bits = '0'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
			R2F [1:0] = '00' or '01' or '10'		R2F [1:0] = '00'		R2F [1:0] = '00'	
Event	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
1.8 V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0 V LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_Bulk Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C	P/C	Low	Low	P/C	P/C
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 32 — PMIC Response for Clear Command by Host - 2

	Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
	R2F [1:0] = '01'		R2F [1:0] = '01'		R2F [1:0] = '10'		R2F [1:0] = '10'	
Event	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
1.8 V LDO Power Good	High	Low	High	High	High	High	High	High
1.0 V LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_Bulk Input Under Voltage	Low	Low	Low	High	Low	High	Low	High

Table 32 — PMIC Response for Clear Command by Host - 2 (cont'd)

	Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
	R2F [1:0] = '01'		R2F [1:0] = '01'		R2F [1:0] = '10'		R2F [1:0] = '10'	
Event	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**	**PWR_GOOD Output**	**GSI_n Output**
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C	P/C	Low	Low	P/C	P/C
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of PWR_GOOD output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of PWR_GOOD output signal.

The PMIC assumes that there is no fuse protection on VIN_Bulk input rail on the DDR5 DIMM module to prevent short circuit type event.

6.10.1 Input Over Voltage Protection

An input over voltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN_Bulk rail.

There is one possibility where PMIC recognizes the input over voltage event.

1. VIN_Bulk input goes above the threshold set in register Table 123, Register 0x1B [7].

When this event occurs for a period longer than tInput_OV_GSI_Assertion time then PMIC sets the register Table 104, Register 0x08 [0] accordingly and drives GSI_n output signal as shown in Table 30 at the same time. Note that at this point, the PMIC does not assert PWR_GOOD output signal. The PMIC allows access to all registers and PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN_Bulk input over voltage status register by writing '1' to register Table 112, Register 0x10 [0] appropriately or by writing '1' to global status clear register Table 116, Register 0x14 [0]. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 104, Register 0x08 [0] will remain at '1'.

In programmable mode (i.e., Table 143, Register 0x2F [2] = '1'), if VIN_Bulk input supply over voltage condition persists greater than tInput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the VIN_Bulk input over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted. If the input over voltage condition is still present then PMIC will continue to assert GSI_n output signal and the status register Table 104, Register 0x08 [0] will remain at '1'. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal and input over voltage condition is no longer present.

6.10.1 Input Over Voltage Protection (cont'd)

In secure mode (i.e., Table 143, Register 0x2F [2] = '0'), if VIN_Bulk input supply over voltage condition persists greater than tInput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR_GOOD signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

6.10.2 Output Power Good Status

The PMIC provides the voltage tolerance information to host that its output regulator may have crossed the desired dc+ac voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWB and SWC is programmed in register Table 129, Register 0x21, [7:1], Table 133, Register 0x25, [7:1] and Table 135, Register 0x27, [7:1] respectively. The PMIC offers the PWR_GOOD condition to be set independently for low side and high side.

In addition, PMIC has two LDO regulators: VOUT_1.8V and VOUT_1.0V

There are four possibilities where PMIC recognizes the output power good event for any output regulator.

1. Output voltage goes below the threshold set in register Table 129, Register 0x21, [0] for SWA or Table 133, Register 0x25, [0] for SWB or Table 135, Register 0x27, [0] for SWC.
2. Output voltage goes above the threshold set in register Table 130, Register 0x22, [7:6] for SWA or Table 134, Register 0x26, [7:6] for SWB or Table 136, Register 0x28, [7:6] for SWC.
3. LDO output VOUT_1.8V goes below the threshold set in register Table 122, Register 0x1A [2].
4. LDO output VOUT_1.0V goes below the threshold set in register Table 122, Register 0x1A [0].

When either event occurs for a period longer than tOutput_PWR_GOOD_GSI_Assertion time then PMIC sets the register Table 104, Register 0x08 [5,3:2] or Table 105, Register 0x09 [5] or Table 147, Register 0x33 [2] appropriately and drives PWR_GOOD and GSI_n output signal as shown in Table 30 at the same time. The PMIC may continue to operate but DDR5 DIMM functionality may not be guaranteed. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine and identify the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host may clear the appropriate status register individually or by writing '1' to global status clear register Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted and PWR_GOOD signal to be asserted. If the output power not good condition is still present then PMIC will continue to assert GSI_n output signal and assert PWR_GOOD signal and the appropriate status register Table 104, Register 0x08 [5,3:2] or Table 105, Register 0x09 [5] or Table 147, Register 0x33 [2] will remain at '1'. If the output power not good condition persists, the host may set the appropriate mask register to remove GSI_n or PWR_GOOD output signal as shown in Table 31 and Table 32.

6.10.3 Output Over Voltage Protection

An output over voltage protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulators.

There are three possibilities where PMIC recognizes the over voltage event.

1. SWA output regulator goes above the threshold set in register Table 130, Register 0x22, [5:4].
2. SWB output regulator goes above the threshold set in register Table 134, Register 0x26, [5:4].
3. SWC output regulator goes above the threshold set in register Table 136, Register 0x28, [5:4].

6.10.3 Output Over Voltage Protection (cont'd)

In programmable mode (i.e., Table 143, Register 0x2F [2] = '1'), if any output over voltage condition persists greater than tOutput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register Table 106, Register 0x0A [7,5:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the appropriate output over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR_GOOD signal is floated when all of its output regulators are normal.

In secure mode (i.e., Table 143, Register 0x2F [2] = '0'), if any output over voltage condition persists greater than tOutput_OV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register Table 106, Register 0x0A [7,5:4] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

6.10.4 Output Under Voltage and VIN_Bulk Under Voltage Lockout Protection

An output under voltage lockout protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulators.

There are four possibilities where PMIC recognizes the under voltage lockout event.

1. SWA output regulator goes below the threshold set in register Table 130, Register 0x22, [3:2].
2. SWB output regulator goes below the threshold set in register Table 134, Register 0x26, [3:2].
3. SWC output regulator goes below the threshold set in register Table 136, Register 0x28, [3:2].
4. VIN_Bulk input voltage goes below vendor specific voltage.

In programmable mode (i.e., Table 143, Register 0x2F [2] = '1'), if any output under voltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register Table 107, Register 0x0B [3,1:0], Table 147, Register 0x33 [3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR_GOOD signal assertion and GSI_n signal assertion. Once host determines the cause, the host must first clear the appropriate output under voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted. Once the status register is cleared and GSI_n output signal is de-asserted, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command assuming valid VIN_Bulk input voltage. The PMIC enables output switching regulators and floats PWR_GOOD signal High when all of its output regulators are normal.

In secure mode (i.e., Table 143, Register 0x2F [2] = '0'), if any output under voltage condition or VIN_Bulk input voltage condition as listed above persists greater than tOutput_UV_VR_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register Table 107, Register 0x0B [3,2:0], Table 147, Register 0x33 [3] appropriately, asserts PWR_GOOD and asserts GSI_n output signal. The PMIC keeps its VOUT_1.8V and VOUT_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

6.10.5 Output Current Limiter Warning Event

The PMIC has output current limiter mechanism to limit the current on the PMIC output voltage regulators.

There are three possibilities where PMIC recognizes the current limiter event.

1. SWA output regulator current goes above the threshold set in register Table 128, Register 0x20 [7:6].
2. SWB output regulator current goes above the threshold set in register Table 128, Register 0x20 [3:2].
3. SWC output regulator current goes above the threshold set in register Table 128, Register 0x20 [1:0].

When either event occurs for a period longer than tOutput_Current_Limiter time then PMIC sets the register Table 107, Register 0x0B [7,5:4] appropriately, drives GSI_n output signal as shown in Table 30 at the same time. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determine the cause, the host may clear the appropriate output current limiter status register as well as any other status registers individually or by writing '1' to global status clear register in Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted. If the output current limiter condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in Table 107, Register 0x0B [7,5:4] will remain at '1'. If the output current limiter condition persists, the host may set the appropriate mask register to remove the GSI_n output signal as shown in Table 31 and Table 32.

6.10.6 Output High Current Consumption Warning Event

The PMIC supports high output current consumption warning mechanism for each of its regulator output. If enabled, the PMIC actively monitors the average output current of the regulator.

There are three possibilities where PMIC recognizes the high output current consumption.

1. SWA output regulator average current goes above the threshold set in register Table 124, Register 0x1C [7:0].
2. SWB output regulator average current goes above the threshold set in register Table 126, Register 0x1E [7:0].
3. SWC output regulator average current goes above the threshold set in register Table 127, Register 0x1F [7:0].

When either event occurs then PMIC sets the register Table 105, Register 0x09 [3,1:0] appropriately, drives GSI_n output signal as shown in Table 30 at the same time. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing '1' to global status clear register in Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted. If the output current consumption warning condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in Table 105, Register 0x09 [3,1:0] will remain at '1'. If the output current consumption warning condition persists, the host may set the appropriate mask register to remove GSI_n output signal as shown in Table 31 and Table 32.

6.10.7 PMIC High Temperature Warning and Critical Temperature Protection

The PMIC provides a high temperature warning mechanism as well as critical temperature shutdown. There are two registers associated with PMIC temperature: The high temperature warning threshold register Table 123, Register 0x1B [2:0] and shutdown temperature threshold register Table 142, Register 0x2E [2:0]. The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

6.10.7 PMIC High Temperature Warning and Critical Temperature Protection (cont'd)

There is one possibility where PMIC recognizes the high temperature event.

1. The PMIC temperature goes above the threshold set in register Table 123, Register 0x1B [2:0].

When the above event occurs for a period longer than tHigh_Temp_Warning time, the PMIC sets the register Table 105, Register 0x09 [7] and drives GSI_n output signal as shown in Table 30 at the same time. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the temperature warning status register as well as any other status registers individually or by writing '1' to global status clear register in Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted. If the high temperature warning condition is still present then PMIC will continue to assert GSI_n output signal and the appropriate status register in Table 105, Register 0x09 [7] will remain at '1'. If the high temperature warning condition persists, the host may set the appropriate mask register to remove GSI_n output signal as shown in Table 31 and Table 32.

If the PMIC temperature goes above the threshold set in register Table 142, Register 0x2E [2:0] for a period longer than tShut_Down_Temp time, the PMIC internally generates VR Disable command and disables all of its switching output regulators, sets the code in register Table 101, Register 0x05 [2:0], updates Table 104, Register 0x08 [6], drives GSI_n and PWR_GOOD output signal as shown in Table 30 at the same time. The PMIC keeps its VOUT_1.8V LDO and VOUT_1.0V LDO output regulator active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host is expected to monitor the temperature status registers. When the temperature drops below the threshold, the host must re-start the PMIC by going through the power cycle of the VIN_Bulk input supply.

6.10.8 Packet Error Code (PEC) and Parity Error Event

In I3C mode, PEC function and parity function can be enabled. If enabled, when PMIC detects either PEC error or Parity Error, the PMIC sets the register Table 106, Register 0x0A [3:2] appropriately, drives GSI_n output signal as shown in Table 30 and it continues to operate as normal and allows access to all registers. See Section 6.18.6 to 6.18.9 for additional details. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in Table 116, Register 0x14 [0] which triggers the GSI_n signal to be de-asserted.

In I^2C mode, for supported CCC, the PMIC supports parity function. When PMIC detects parity error, the PMIC sets the register Table 106, Register 0x0A [2], drives GSI_n output signal as shown in Table 30 and it continues to operate as normal and allows access to all registers. See Section 6.18.6 to 6.18.9 for additional details. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the GSI_n signal assertion. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in Table 116, Register 0x14 [0] which triggers the GSI_n signal to be deasserted.

6.11 Analog to Digital Converter (ADC)

The PMIC supports analog to digital converter (ADC) to monitor input supply voltages (VIN_Bulk) as well as output voltage regulator voltage (SWA, SWB, SWC, VOUT_1.8V and VOUT_1.0V). Register 0x30 [7:3] allows to enable the ADC and select the desired input supply voltage or desired output supply voltage. Register 0x31 [7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is as following:

- Switch Output Voltage Regulator SWA, SWB (Output Voltage Range: 1050 mV to 1160 mV): ± 1 LSB
- Switch Output Voltage Regulator SWA, SWB (Output Voltage Range outside of 1050 mV to 1160 mV): ± 3 LSB

6.11 Analog to Digital Converter (ADC) (cont'd)

- Switch Output Voltage Regulator SWC (Output Voltage Range: 1750 mV to 1850 mV): ± 1 LSB
- Switch Output Voltage Regulator SWC (Output Voltage Range outside of 1750 mV to 1850 mV): ± 3 LSB
- VOUT_1.8V, VOUT_1.0V Output Voltage: ± 3 LSB
- VIN_Bulk Input Voltage: ± 6 LSB

The PMIC also monitors output voltage regulator current or power (SWA, SWB, and SWC) and updates Register 0x0C [7:0] for SWA, Register 0x0E [7:0] for SWB, and Register 0x0F [7:0] for SWC. Register 0x1B [6] allows the host to select whether the PMIC should report current measurements or power measurements. The current or power measurement reported in this registers are an average measurement over time period defined in Register 0x30 [1:0]. If Register 0x1B [6] = '1', Register 0x1A [1] allows host to select whether PMIC should report individual rail power or total power in Register 0x0C [7:0]. The register update frequency of this register is configured in Register 0x30 [1:0]. The internal sampling rate of the PMIC is vendor specific. Register 0x32 [1:0] allows the user to change the LSB step size for current or power measurements.

Table 33 — PMIC ADC Current and Power Accuracy; R32[1:0] = 00

Load Current	SWA to SWC Rails - Current Accuracy	SWA to SWC Rails - Corresponding Power Accuracy	Total Power Accuracy
Less than 0.5A	±4 LSB	±7 LSB	±12 LSB
Greater than or equal to 0.5A	±3 LSB	±6 LSB	

Table 34 — PMIC ADC Current and Power Accuracy; R32[1:0] = 01

Load Current	SWA to SWC Rails - Current Accuracy	SWA to SWC Rails - Corresponding Power Accuracy	Total Power Accuracy
Less than 0.5A	±9 LSB	±18 LSB	N/A[1]
Greater than or equal to 0.5A	±8 LSB	±16 LSB	

NOTE 1 Register 0x32 [1:0] must be set to 00 when Register 0x1A [1] = 1.

6.12 PMIC Address ID (PID)

The DDR5 PMIC has PID input pin which allows to assign up to three different unique ID for I^2C and I3C Basic protocol.

At first power on, when VIN_Bulk input is applied, the PMIC automatically determines its ID. The PMIC offers three different ID as shown in Table 35.

Table 35 — PMIC ID

PID Pin Connection on DIMM Board	PMIC ID	Comment
Short to GND	PID = 1001	PMIC can be configured
Floating	PID = 1000	
Short to 1.8	PID = 1100	Connected to PMIC's VOUT_1.8V Rail

6.13 Error Injection

The DDR5 PMIC offers error injection function for the purpose of debug, test and validation at various stages.

6.13.1 Error Injection Function Usage prior to VR Enable (either via VR_EN Pin or I²C/ I3C Bus)

Prior to VR Enable command, the Error injection function may be invoked by setting error injection enable bit Table 149, Register 0x35 [7] = '1' during the configuration state. If any of either VIN_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected prior to VR Enable command, the PMIC shall not execute power on sequence and shall not enable PMIC output regulators when PMIC receives VR Enable command. The PMIC shall not update error log registers (Table 100, Register 0x04 to Table 102, Register 0x06). The PMIC shall update appropriate status registers (Table 104, Register 0x08 to Table 107, Register 0x0B, Table 147, Register 0x33) accordingly. The PMIC shall enter in secure mode if Table 143, Register 0x2F [2] = '0' and programmable mode if Table 143, Register 0x2F [2] = '1'.

6.13.2 Error Injection Function Usage after VR Enable (either via VR_EN Pin or I²C/I3C Bus)

After PMIC output regulators are enabled with VR Enable command and PMIC is in programmable mode, the error injection function may be invoked by setting error injection enable bit Table 149, Register 0x35 [7] = '1'. If any of either VIN_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected the PMIC shall execute Power Off Sequence to disable PMIC output regulators and shall update the error log registers (Table 100, Register 0x04 to Table 102, Register 0x06) as well as status registers (Table 104, Register 0x08 to Table 107, Register 0x0B, Table 147, Register 0x33) accordingly. Note that if any of the output rails are not enabled through power on sequence configuration registers, the error injection on that output rail does not apply.

After PMIC output regulators are enabled with VR Enable command and PMIC is in secure mode, the error injection enabling Table 149, Register 0x35 [7] = '1' is disallowed. The PMIC shall ignore any attempts to inject any error and shall not execute Power Off Sequence to disable PMIC output regulators and shall not update any error log or status registers.

To exit the error injection function, the host shall power cycle VIN_Bulk input supply.

6.14 Acoustic Noise

The PMIC5120 buck regulators normally operates in DCM (Discontinuous Current Mode). The buck regulator's switching frequency is a function of a current load on its output regulator. At light load (typically < 50mA), the buck regulator's switching frequency may approach to less than 100 KHz.

The human ear audible frequency range is 20 Hz to 20 KHz. If buck regulator switching frequency falls within the human ear audible frequency range, then human ear can experience the acoustic noise.

To prevent the acoustic noise to human ear, the PMIC offers a feature which prevents the buck regulator switching frequency to go below the threshold frequency that is configured in register R36[3:1]. When the feature is enabled, the PMIC ensures that its switching frequency stays above the threshold frequency regardless of how low the output load current may be.

The acoustic noise prevention control feature is in Table 150, Register 0x36 [3:1]. The control register applies to all three buck regulators. This feature is not applicable to any buck regulator that is configured to operate as Forced CCM (Continuous Current Mode). If PMIC is configured such that one or more buck regulators is configured as DCM and other buck regulator is configured as Forced CCM, when this feature is enabled, it applies to any buck regulators that are configured as DCM.

At light load, when this feature is enabled, there may be a slight difference in efficiency. However, the difference in efficiency may be insignificant and may be within the measurement noise.

6.15 I²C and I3C Basic Operation

At power on, by default, the PMIC device comes up in legacy I²C mode of operation. Following applies in I²C mode:

1. The max operation speed is limited to 1 MHz
2. In-band interrupts are not supported
3. Bus reset is supported.
4. Parity check is not supported except for supported CCCs.
5. Packet Error check is not supported.

The PMIC device shall operate in the legacy I²C mode until put into I3C Basic mode via command.

The host may put the PMIC device in I3C Basic mode by issuing SETAASA CCC.

Following applies in I3C Basic mode.

1. The max operation speed is up to 12.5 MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

6.16 Device Interface - Protocol

6.16.1 Management Bus

The PMIC supports two different protocol on its management bus.

- I²C Target Protocol - Speed Up to 1 MHz
- I3C Basic Target Protocol - Speed Up to 12.5 MHz

The PMIC's 7-bit target address [7:1] is composed of 4-bit device address [7:4] and 3-bit HID address [3:1].

The PMIC's 4-bit device address [7:4] is:

- If PID pin is tied to GND on PCB: '1001'
- If PID pin is tied to 1.8 V on PCB: '1100'
- If PID pin floating on PCB: '1000'

The PMIC's 3-bit HID address [3:1] is per Table 148, Register 0x34 [3:1].

6.16.2 Switch from I²C Mode to I3C Basic Mode

By default when PMIC first powers on, it operates in I²C mode. The PMIC device shall operate in I²C mode until put into I3C Basic mode via command.

In I²C mode, the host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, SETAASA). All other CCC are not supported and the PMIC device simply ignores it. The host must issue DEVCTRL and SETHID CCC first (if required) followed by SETAASA CCC.

The host puts the PMIC device in I3C Basic mode by issuing SETAASA CCC. See also Section 6.18.10.4.

When SETHID CCC is registered by the PMIC, it updates the Table 148, Register 0x34 [3:1].

When SETAASA CCC is registered by the PMIC, it updates the Table 146, Register 0x32 [6] to '1'.

6.16.3 Switch from I3C Basic Mode to I²C Mode

The host can put the PMIC device back in I²C mode from I3C Basic mode at any time by issuing RSTDAA CCC.

When RSTDAA CCC is registered by the PMIC, it updates Table 146, Register 0x32 [6] to '0'. See also Section 6.18.10.3.

6.17 I²C Target Protocol

The PMIC device operate on a standard I²C serial interface. Transactions where the PMIC device is the targeted target device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The PMIC device host region registers that are write-protected in secure mode of operation, the PMIC ACKs the host request but the PMIC does not execute the operation internally.

Similarly, regardless of secure mode or programmable mode of operation, without the correct password, all DIMM vendor region and vendor specific region registers are write-protected and PMIC ACKs the host request but the PMIC does not execute the operation internally.

The PMIC device accepts 1 byte of address which covers 256 bytes of registers. The PMIC device register space does not require page selection process as all registers are within first 256 bytes.

6.17.1 Write Operation Data Packet

The PMIC supports Byte Write operation as shown in Table 36. For Byte Write, only data byte is transferred followed by Stop operation.

Table 36 — Write Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr[1]	1	X	0	X	HID			W=0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	...								A	
	Data								A	Sr or P

NOTE 1 In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered an illegal operation.

6.17.2 Read Operation Data Packet

The PMIC supports Byte Read or Block Read operation as shown in Table 38. For Byte Read, only data byte is transferred followed by Stop operation.

6.17.2 Read Operation Data Packet (cont'd)

Table 37 — Read Command Data Packet

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr[1]	1	X	0	X	HID			W=0	A	
	Address [7:0]								A	
Sr	1	X	0	X	HID			R=1	A[2]	
	Data								A	
	Data								A	
	...								A	
	Data								N[3]	Sr or P

NOTE 1 In I2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I2C mode. Any other operation including another Repeat Start is considered an illegal operation.

NOTE 2 If the PMIC NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The PMIC may eventually ACK.

NOTE 3 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

6.17.3 Default Read Address Pointer Mode

During normal operation of the DDR5 DIMM, the host periodically polls critical information from the PMIC. The host may poll all the status registers or current or power measurement registers or the temperature register or any combination of these different types of registers. To help improve the efficiency of the I2C bus protocol, the PMIC offers a default read pointer address mode so that whenever PMIC sees the STOP operation on SCL and SDA bus, its read address pointer is always set to default address. The default read pointer address mode is enabled through register Table 154, Register 0x3A [6] and default starting address for read operation is selectable through register Table 154, Register 0x3A[5:4]. This allows host to reduce the normal read command data packet length, as shown in Table 37, to the shorter length shown in Table 38 . The default read address pointer reduces the packet overhead by 2 bytes. The host typically enables this mode at last after VR Enable command when the normal operation begins of the DDR5 DIMM.

Table 38 — Read Command Data Packet with Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	1	X	0	X	HID			R=1	A	
	Data								A	
	Data								A	
	...								A	
	Data								N[1]	Sr or P

NOTE 1 When PMIC device reaches last byte within the region (either Host region or DIMM vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM vendor region or Vendor specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

6.18 I3C Basic Target Protocol

6.18.1 Write Operation Data Packet

The PMIC device operate on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 39. The “T” bit carries Parity information from the host for each byte.

The PMIC device host region registers that are write-protected in secure mode of operation, the PMIC does not execute the operation internally. Similarly, regardless of secure mode or programmable mode of operation, without the correct password, all DIMM vendor region and vendor specific region registers are write-protected and PMIC does not execute the operation internally.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. The host may optionally enable this function through Table 148, Register 0x34 [7] or DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Write operation.

Table 39 — Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	Sr[4] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7’h7E.

6.18.1 Write Operation Data Packet (cont'd)

Table 40 — Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			W=0	0000				T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[4] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If PMIC device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If PMIC device has no pending IBI, there is no action taken by PMIC. Table 41 and Table 42 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 42, PEC calculation does not include IBI header byte (7'h7E followed by W=0).

Table 41 — Write Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	Sr[5] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start)

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

6.18.1 Write Operation Data Packet (cont'd)

Table 42 — Write Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[5] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start)

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull peration (Address bit 7).

NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

6.18.2 Read Operation Data Packet

The PMIC device operate on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See Table 43. The "T" bit carries Parity information from the host for each byte prior to Repeat START. After Repeat START, "T" bit carries information from PMIC device to Host indicating Continuous ('1') or Stop ('0') whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. The host may optionally enable this function through Table 148, Register 0x34 [7] or DEVCTRL CCC. If enabled, the PEC is appended as shown in Table 44. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Read operation.

6.18.2 Read Operation Data Packet (cont'd)

Table 43 — Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6,7]	Sr[8] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 5 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 37 to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only host can perform STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

6.18.2 Read Operation Data Packet (cont'd)

Table 44 — Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[6]	Sr[7] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 38 to see how Host ends target device operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If PMIC device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If PMIC device has no pending IBI, there is no action taken by PMIC. Table 45 and Table 46 show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 46, PEC calculation (from Host to PMIC) does not include IBI header byte (7'h7E followed by W=0).

6.18.2 Read Operation Data Packet (cont'd)

Table 45 — Read Command Data Packet with IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N[5,6]	
	Data								T=1	
	...								T=1	
	Data								T=1[7,8]	Sr[9] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 7 See Figure 37 to see how Host ends target device operation.

NOTE 8 When PMIC device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform the STOP operation.

NOTE 9 Repeat Start or Repeat Start with 7'h7E.

6.18.2 Read Operation Data Packet (cont'd)

Table 46 — Read Command Data Packet with IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			W=0	A[2,3,4]	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[5,6]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[7]	Sr[8] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 5 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 7 See Figure 38 to see how Host ends target device operation followed by Host STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

6.18.3 Default Read Address Pointer Mode

This mode works same exact way as explained in Section 6.17.3. Table 47 and Table 48 show the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, Table 154, Register 0x3A [3:2] sets the number of bytes that PMIC sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in Table 154, Register 0x3A [3:2] register. In other words, the host must not interrupt the burst length pre-maturely for Default Address Pointer Read operation.

Table 47 — Read Command Data Packet with Address Pointer Mode; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			R=1	A/N[1]	
	Data								T=1	
	...								T=1	
	Data								T=1[2,3]	Sr[4] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 See Figure 37 to see how Host ends target device operation.
NOTE 3 When device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.
NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Table 48 — Read Command Data Packet with Address Pointer Mode; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			R=1	A/N[1]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[2]	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 See Figure 38 to see how Host ends target device operation followed by Host STOP operation.
NOTE 3 Repeat Start or Repeat Start with 7'h7E.

6.18.3 Default Read Address Pointer Mode (cont'd)

Table 49 — Read Command Data Packet with Address Pointer Mode and IBI Header; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			R=1	A/N[2,3]	
	Data								T=1	
	...								T=1	
	Data								T=1[4,5]	Sr[6] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).
NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
NOTE 4 See Figure 37 to see how Host ends target device operation.
NOTE 5 When device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.
NOTE 6 Repeat Start or Repeat Start with 7'h7E.

Table 50 — Read Command Data Packet with Address Pointer Mode and IBI Header; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1,2]	
Sr	1	X	0	X	HID			R=1	A/N[2,3]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[4]	Sr[5] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).
NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 3 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
NOTE 4 See Figure 38 to see how Host ends target device operation followed by Host STOP operation.
NOTE 5 Repeat Start or Repeat Start with 7'h7E.

6.18.3 Default Read Address Pointer Mode (cont'd)

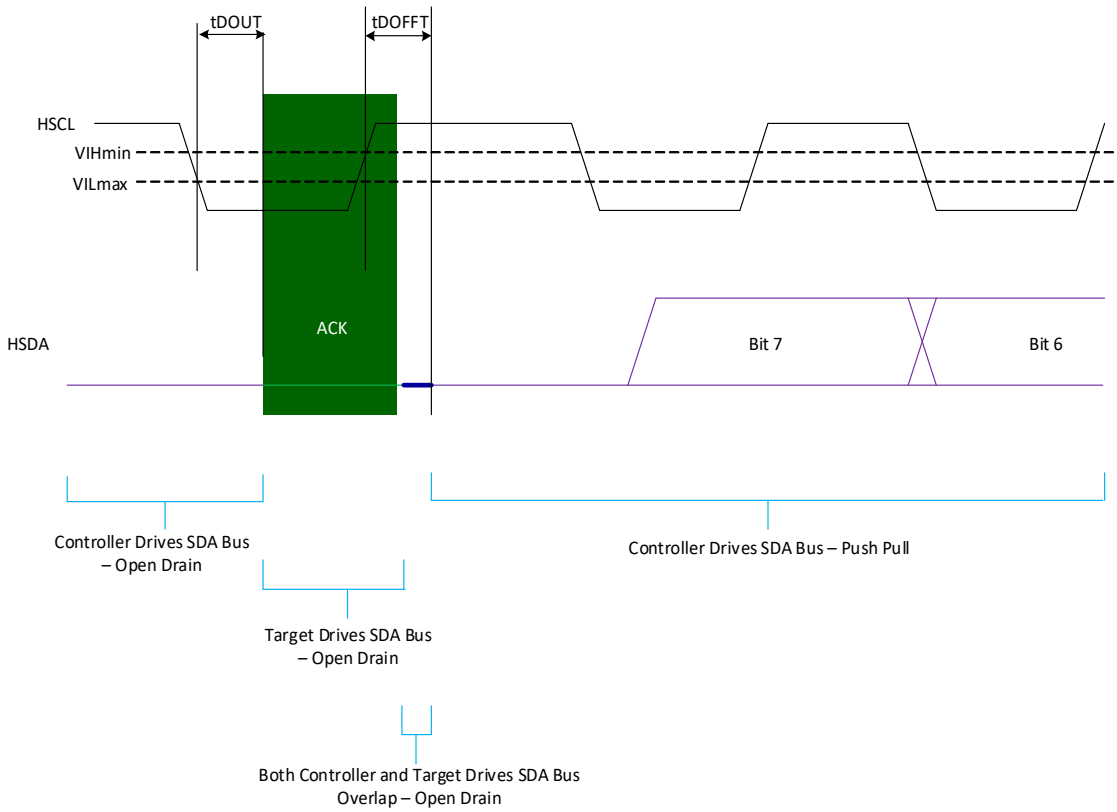


Figure 34 — Target Open Drain (ACK) to Controller Push Pull Hand Off Operation

6.18.3 Default Read Address Pointer Mode (cont'd)

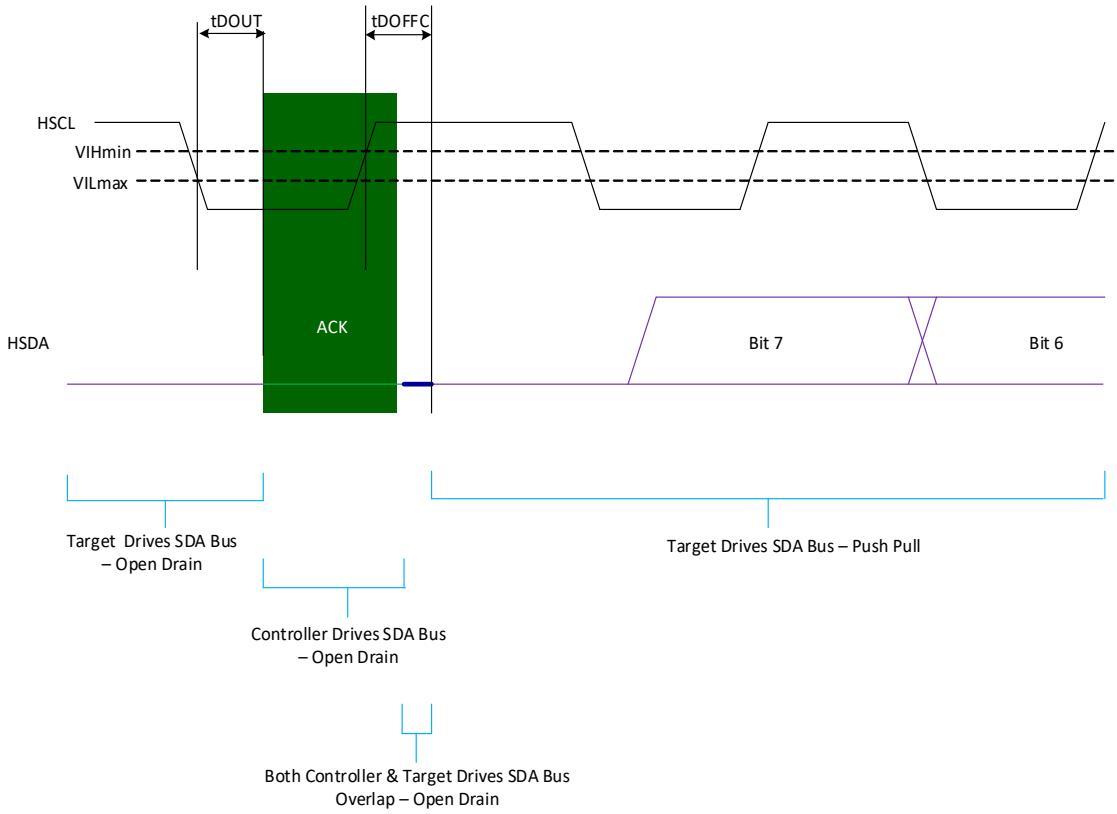


Figure 35 — Controller Open Drain (ACK) to Target Push Pull Hand Off Operation

6.18.3 Default Read Address Pointer Mode (cont'd)

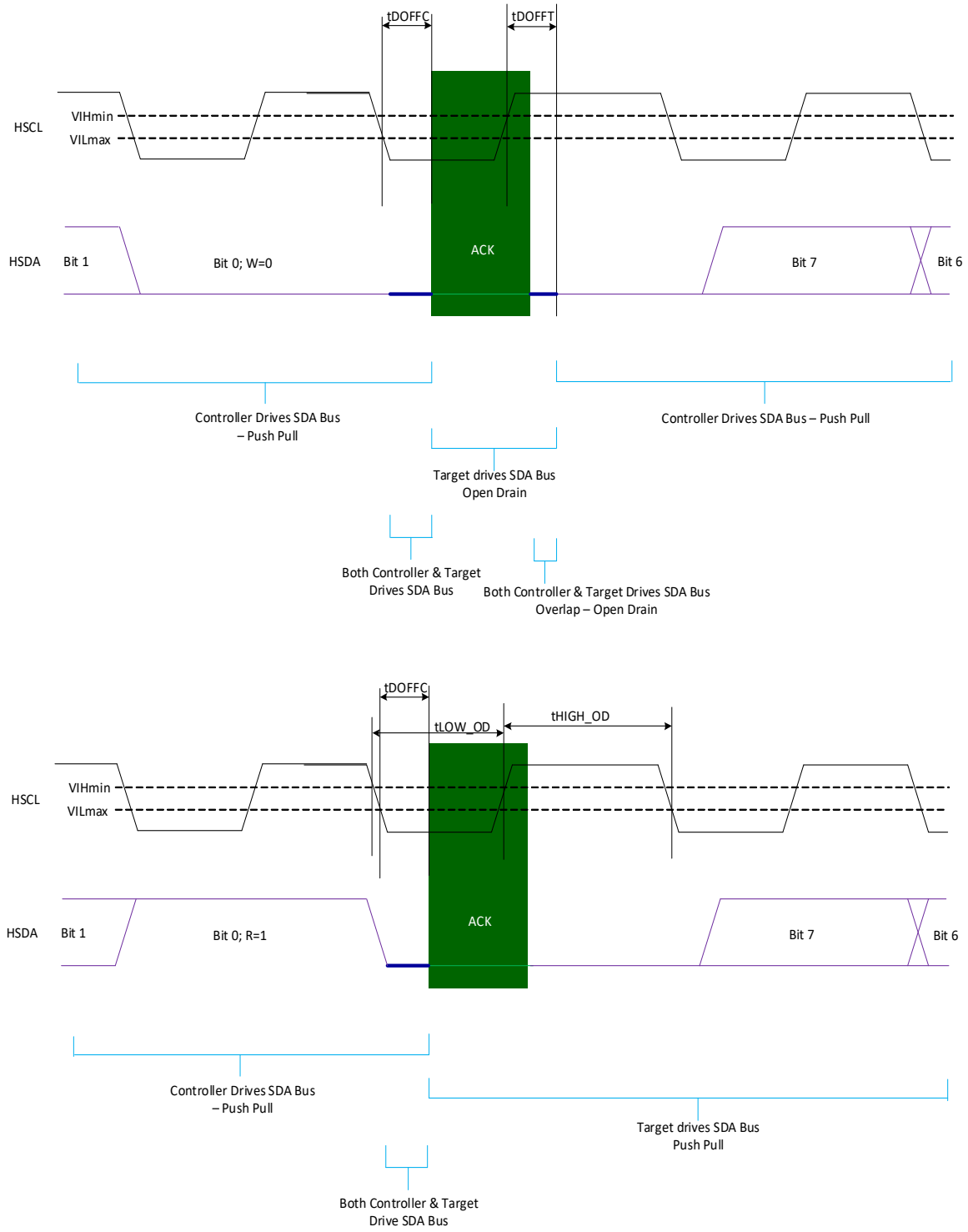


Figure 36 — Controller Push Pull to Target Open Drain Hand Off Operation

6.18.3 Default Read Address Pointer Mode (cont'd)

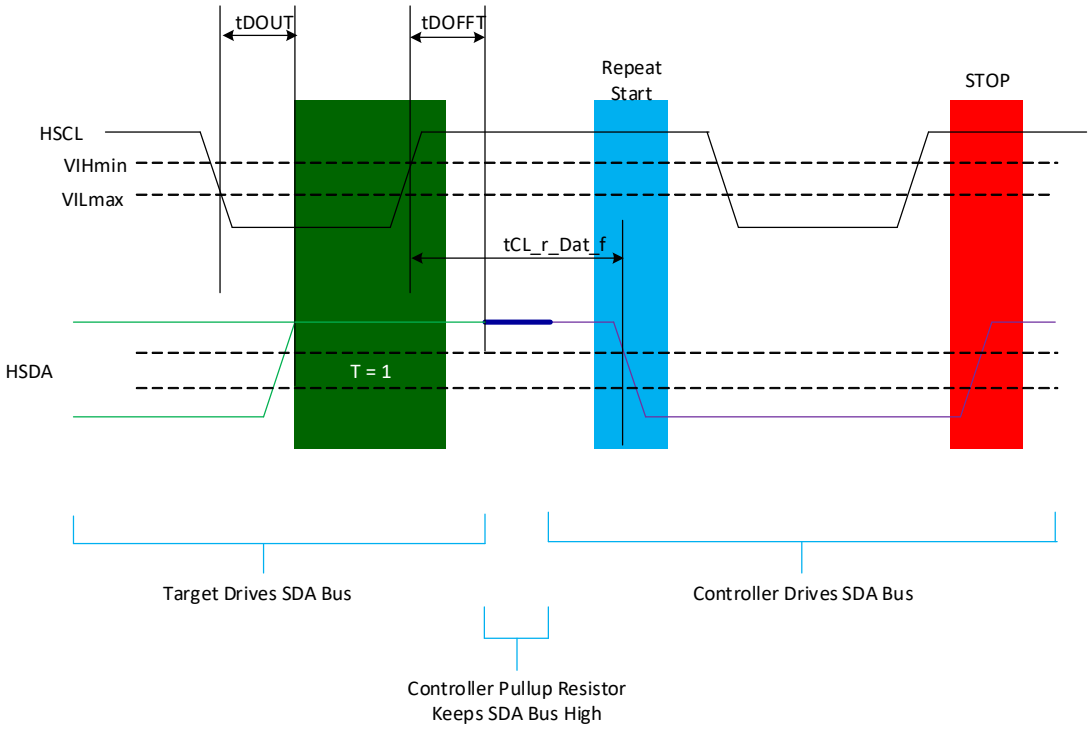


Figure 37 — T=1; Controller Ends Read with Repeated START and STOP Waveform

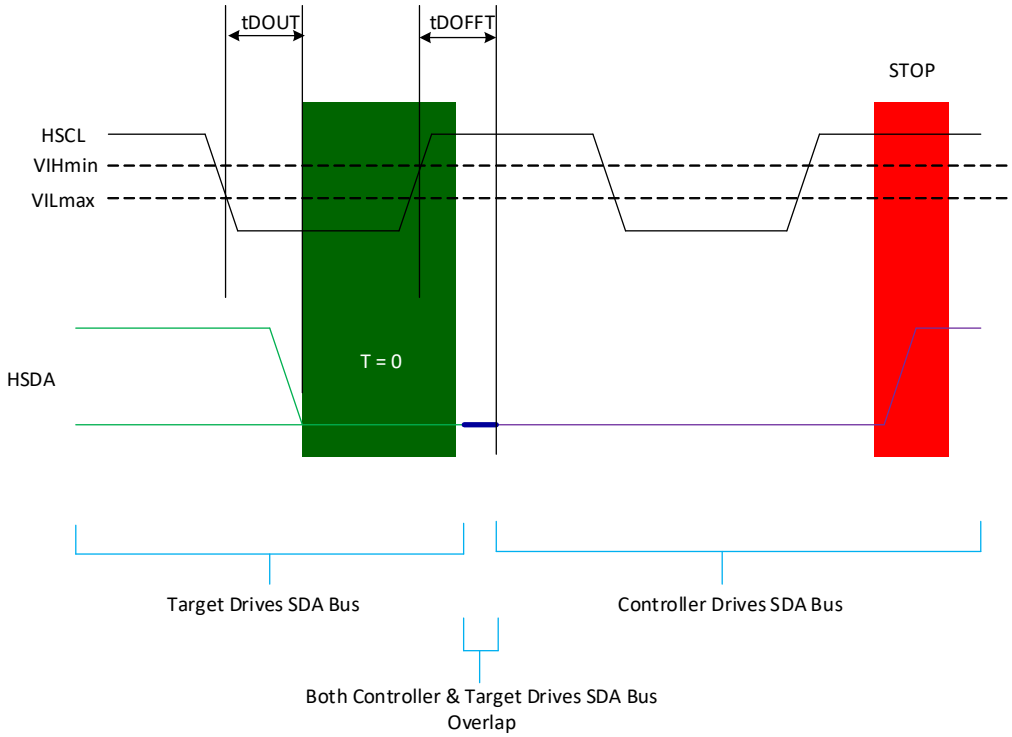


Figure 38 — T=0; Target Ends Read; Controller Generates STOP

6.18.4 In Band Interrupt (IBI)

In I^2C mode, in band interrupt function is not supported. Only I3C Basic mode supports in band interrupt function.

The PMIC device supports a feature to enable or disable the event interrupts.

- Interrupt Enable in register Table 148, Register 0x34 [6] - When Table 148, Register 0x34 [6] = '1', the device sends the interrupt at next available opportunity when any of the register bits in Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:2], Table 107, Register 0x0B [7,5:3,1:0], and Table 147, Register 0x33 [2] is set to '1'. The device also sets Table 106, Register 0x0A [1] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

- When Table 148, Register 0x34 [6] = '0', the device does not send the interrupt regardless of the register bits status in Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:2], Table 107, Register 0x0B [7,5:3,1:0], and Table 147, Register 0x33 [2]. However, the device does set Table 106, Register 0x0A [1] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

6.18.4.1 Mechanics of In Band Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt (i.e., Table 106, Register 0x0A [1] = '1') and Table 148, Register 0x34 [6] = '1') the PMIC device will request an interrupt after detecting a START condition by transmitting its 7-bit binary address (LID bits followed by HID bits) followed by R/W bit = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If the PMIC device detects no START condition but if the I3C Basic bus (SDA and SCL) has been inactive (no edges seen) for t_{AVAL} period, then PMIC device may assert SDA low by t_{IBI_ISSUE} time to request an interrupt. When the PMIC device requests an interrupt, the Host toggles the SCL. The PMIC device transmits its 7-bit binary address; '1001' (LID) followed by '111' (HID) followed by R/W bit = '1'.

When the PMIC device requests an interrupt, the host may take one of the two actions below:

- The Host sends ACK on 9^{th} bit to accept the interrupt request. At this point, if the PMIC confirms that it has won the arbitration, the PMIC transmits the IBI payload as shown in Table 51 and Table 52 for PEC disabled and PEC enabled configuration respectively. See Figure 39. Figure 39 just shows only first two data bits of the first payload byte (MDB Byte) to illustrate the timing. The interrupt payload contains MDB followed by PMIC error register contents Table 104, Register 0x08 to Table 107, Register 0x0B and Table 147, Register 0x33 in order. The host then issues the STOP command. Note the timing waveform in Figure 39. The host then accepts the IBI payload if it sends an ACK on 9^{th} bit to accept the interrupt request. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the PMIC Hub device retains the IBI Status flag Table 106, Register 0x0A [1] and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the PMIC device successfully transmits the entire IBI payload, it then clears the IBI Status flag Table 106, Register 0x0A [1] = '0' and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is an another different event occurs; for another same event, the device does not request for an IBI.

- The Host sends NACK on the 9^{th} bit as shown in Figure 40 followed by a STOP command. In this case, the PMIC device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which PMIC device sent the IBI request. The PMIC device retains the IBI Status flag Table 106, Register 0x0A [1] = '1' and Pending Interrupt Bits [3:0] = '0001'.

6.18.4.1 Mechanics of In Band Interrupt Generation (cont'd)

Table 51 — Target Device IBI Payload Packet; PEC is Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	X	0	X	HID			R=1	A[1]	
	MDB = 0x00								T=1	
	R08 [7:0]								T=1	
	R09 [7:0]								T=1	
	R0A [7:0]								T=1	
	R0B [7:0]								T=1	
	R33 [7:0]								T=0[2]	P

NOTE 1 See Figure 35 to see how the transition occurs from Controller Open Drain (ACK) to Target Push Pull operation (1st bit of MDB Byte bit [7]).
NOTE 2 See Figure 38 to see how Host device ends target device operation followed by Host STOP operation.

Table 52 — Target Device IBI Payload Packet; PEC is Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	X	0	X	HID			R=1	A[1]	
	MDB = 0x00								T=1	
	R08 [7:0]								T=1	
	R09 [7:0]								T=1	
	R0A [7:0]								T=1	
	R0B [7:0]								T=1	
	R33 [7:0]								T=1	
	PEC								T=0[2]	P

NOTE 1 See Figure 35 to see how the transition occurs from Controller Open Drain (ACK) to Target Push Pull operation (1st bit of MDB Byte bit [7]).
NOTE 2 See Figure 38 to see how Host ends target device operation followed by Host STOP operation.

6.18.4.1 Mechanics of In Band Interrupt Generation (cont'd)

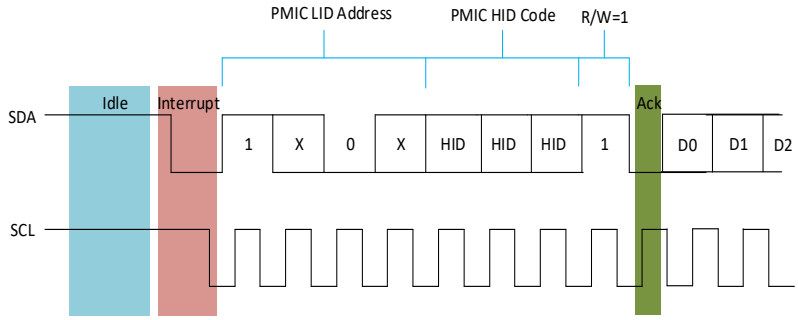


Figure 39 — PMIC Request Interrupt; Host Ack followed by PMIC Device IBI Payload

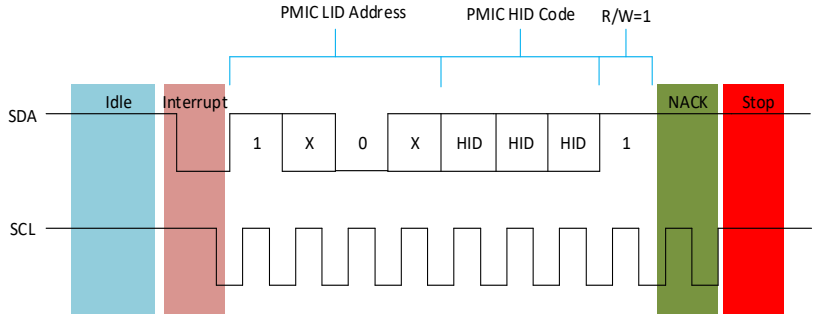


Figure 40 — PMIC Requests Interrupt; Host NACK followed by STOP

6.18.4.2 Interrupt Arbitration

As there are multiple devices I3C Basic bus, multiple device may request an interrupt when the Host I3C Basic bus is inactive for t_{AVAL} period. Arbitration process is required.

For DDR5 DIMM application environment, there could be up to total of 13 difference devices including the PMIC on I3C Basic bus.

On a typical DDR5 DIMM application environment, all devices have the same 3-bit HID code. Hence the arbitration is always won by the lowest 4-bit LID code. For example, if one local target device has LID code of '0010' and other device (PMIC) has a LID code of '1001', through the arbitration process, the LID code of '0010' wins. The other device (PMIC) with a LID code of '1001' must release the bus and wait for next opportunity to request an interrupt. Table 53 shows the arbitration priority based on the LID code for all devices. The Green colored cells in Table 53 are the likely devices that will be on a standard DDR5 RDIMM or DDR5 LRDIMM. The Olive colored cells in Table 53 do not apply.

6.18.4.2 Interrupt Arbitration (cont'd)

Table 53 — Interrupt Arbitration - Among All Devices

Device	LID Code	HID Code = '111'	Arbitration Priority
N/A	0000	N/A	N/A
RFU	0001	111	1
TS0	0010	111	2
RFU	0011	111	3
RFU	0100	111	4
RFU	0101	111	5
TS1	0110	111	6
RFU	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD Hub	1010	N/A	N/A
RCD	1011	111	10
PMIC2	1100	111	11
RFU	1101	111	12
RFU	1110	111	13
N/A	1111	N/A	N/A

In an uncommon but possible scenario would be that at the exact same time as when the Hub or local target devices (i.e., PMIC) are requesting an interrupt, the host is starting an operation to the hub or local target devices (i.e., PMIC). When this happens, Host also gets involved in the arbitration process along with the Hub or the local target devices (PMIC). During the arbitration phase, there will be always only one winning device and it could be either Hub or the local target device (i.e., PMIC) or the Host.

If the host wins during the arbitration phase, it continues with normal operation. The losing Hub or local target device (i.e., PMIC) waits for next opportunity to send an interrupt.

If the host loses during the arbitration phase, it must let go of the bus. When the host loses during the arbitration, the host must let the Hub or local target device (i.e., PMIC) finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9^{th} bit, the host has two options to take the action as noted below:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning Hub or local target device (i.e., PMIC). After the IBI payload, the host issues STOP operation.
- Host sends an NACK followed by STOP operation.

In a rare but still possible scenario would be that at the exact same time as when the PMIC is requesting an interrupt, the host is starting an operation to the same PMIC. When this happens, neither Host or nor the PMIC knows it is a winner until the 8^{th} bit and Host always wins. This is because, the PMIC sends R=1 (8^{th} bit) during the interrupt. The host sets W=0 (8^{th} bit) during the operation. As a result, the host wins and the PMIC must let go of the bus and wait for the next opportunity to send an interrupt.

6.18.4.2 Interrupt Arbitration (cont'd)

An extremely rare but still possible scenario would be that at the same exact time as when PMIC device is requesting an interrupt, the host is requesting a read operation with the default read address pointer mode to the PMIC device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the PMIC device sends R=1 (8^{th} bit) during the interrupt and Host also sends R=1 for read request with default read address pointer mode. As a result, there is no winner because Host is waiting for PMIC to ACK and PMIC is waiting for Host to ACK. In this case, neither Host nor PMIC will ACK. Since there is no ACK (i.e., NACK) by either device, the Host must time out and repeat the read request with Repeat Start. When Host repeats the read request with Repeat Start, the PMIC does not send an interrupt because of Repeat Start.

6.18.4.3 Clearing IBI Status and Device Status Registers

The PMIC device provides the IBI status in Table 106, Register 0x0A [1] by setting it to '1'. The PMIC device clears the IBI status register Table 106, Register 0x0A [1] to '0' automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits [3:0] to '0000'. Once IBI status register is cleared, the PMIC does not request for an IBI again unless an another event occurs.

The device status registers (Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:2], Table 107, Register 0x0B [7,5:3,1:0], and Table 147, Register 0x33 [2] are latched and remains set even after PMIC device sends IBI payload and clears the IBI status register Table 106, Register 0x0A[1] to '0'. The host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global clear command.

After host issues clear command, if the condition is no longer present the device clears the appropriate status register, clears the IBI status register Table 106, Register 0x0A [1] to '0' and Pending Interrupt Bits [3:0] to '0000' even if the device has not sent the IBI. After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register Table 106, Register 0x0A [1] to '1' and Pending Interrupt Bits [3:0] to '0001' even if the device has already sent the IBI and entire IBI payload.

6.18.5 Packet Error Check (PEC) Function

In I^2C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.

The PMIC device implement an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PECs is enabled through DEVCTRL CCC or by directly writing '1' to Table 148, Register 0x34 [7]. The PEC is a CRC-8 value calculated on all the messages bytes except for START, REPEAT START, STOP conditions or T-bits, ACK, NACK and IBI header (7'h7E followed by W=0) bits.

The polynomial for CRC-8 calculations is:

- $C(X) = X^8 + X^2 + X^1 + 1$

The seed value for PEC function is all zeros.

When Host calculates PEC for PMIC device, it includes LID and HID bits followed by R/W bit.

6.18.6 Parity Error Check Function

In I^2C mode, parity error checking is not supported except for supported CCCs. Only I3C Basic mode supports parity error checking.

By default, when PMIC device is put in I3C Basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. Host can also disable the parity function with DEVCTRL CCC or by directly writing '1' to Table 148, Register 0x34 [5]. When parity function is disabled, the PMIC device simply ignores the "T" bit information from the Host. The host may actually choose to compute the parity and send that information during "T" bit or simply drive static low or high in "T" bit.

6.18.6 Parity Error Check Function (cont'd)

The PMIC device implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'. If even number of bits in the byte are '1', the parity bit value is '1'. The host computes the parity and sends during "T" bit.

6.18.7 Packet Error Check and Parity Error Handling

There are two types of error checking done by the PMIC device. Parity error checking and Packet Error checking. By default, the parity error checking is always enabled and packet error checking is disabled. The host may enable the packet error checking at any time. The parity error is calculated for each byte. The host sends parity error information in "T" bit.

I3C basic defines TE0, TE1, TE2, TE3, TE4, TE5, TE6 error detection for target devices. Only TE1 and TE2 error detection is supported by the PMIC for parity checking. All other errors are not supported and not applicable.

6.18.7.1 Write Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for the parity error for each byte in a packet that it receives from the host except for the device select code byte that it receives from the host as shown in Table 54.

Table 54 — Write Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	Sr[4] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write Command - if no parity error:

- The PMIC device executes the command.

Write Command - if parity error:

- The PMIC device discards the one byte in the packet that had parity error.
- The PMIC device discards all sub-sequent bytes in that packet until STOP operation. The PMIC device may or may not check the parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the PMIC device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.

6.18.7.1 Write Command Data Packet Error Handling - PEC Disabled (cont'd)

- The PMIC device sets the register Table 106, Register 0x0A [2:1] to '11'; P_Err in GETSTATUS CCC to '1'; updates Pending Interrupts Bits [3:0] to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send in band interrupt if IBI is enabled.

6.18.7.2 Read Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in Table 55.

The PMIC device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes that PMIC device sends. The PMIC device sends Continuous ('1') or Stop ('0') information during "T" bit when PMIC device is sending the read data.

Table 55 — Read Command Data Packet; PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6,7]	Sr[8] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 5 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 37 to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or DIMM Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for DIMM Vendor region or Vendor Specific region. Once the address counter reaches 0xFF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform the STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

Read Command - If no parity error:

- The PMIC sends ACK back to the host when Host perform Start Repeat operation.
- The PMIC device executes the command and sends the data as shown in Table 55.

Read Command - If parity error:

- The PMIC device discards the one byte in the packet that had a parity error.

6.18.7.2 Read Command Data Packet Error Handling - PEC Disabled (cont'd)

- The PMIC device sends NACK back to the host when Host performs a Start Repeat operation. This is shown in the RED colored cell in Table 55. The NACK represents either a parity error in one byte that it receives from the host or that PMIC is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. If the PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start.
- The PMIC does not send the data shown in Table 55 and instead expects Host to perform STOP operation.
- The PMIC device sets Table 106, Register 0x0A [2:1] to '11'; P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

6.18.7.3 Write Command Data Packet Error Handling - PEC Enabled

The PMIC device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host as shown in Table 56. Further, the PMIC device checks for the packet error for the entire packet (from Start condition until last byte of Data) that is receives from the host in Table 56,

Table 56 — Write Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[4] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit [7]).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity in subsequent bytes when it determines the 7-bit device select code issues by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write Command - if no parity error:

- The PMIC device waits for the entire packet. If no error in packet, the PMIC device executes the command. If there is an error in the packet, the PMIC device discards the entire packet and does not execute that packet and waits for STOP; sets the register Table 106, Register 0x0A [3,1] to '11'; PEC_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

Write Command - if parity error:

- The PMIC device discards that byte and the entire packet until STOP operation.

6.18.7.3 Write Command Data Packet Error Handling - PEC Enabled (cont'd)

- The PMIC device sets the Table 106, Register 0x0A [2:1] to '11'; P_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.
- The PMIC device may or may not check the error for the packet. If the device checks for the packet error, likely it will detect an error in the packet and the device may also set the Table 106, Register 0x0A [3] and PEC_ERR in GETSTATUS CCC as well.

6.18.7.4 Read Command Data Packet Error Handling - PEC Enabled

The PMIC device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in Table 57.

The PMIC device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes shown in Table 57. The PMIC device sends Continuous ('1') or Stop ('0') information during "T" bit when PMIC device is sending the read data.

The PMIC device checks for the PEC error for a packet that it receives from the Host from Start condition to Repeat Start condition (from first device select code followed by the address offset and CMD byte).

The PMIC device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data PMIC device transmits back to Host).

Table 57 — Read Command Data Packet; PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1,2,3]	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[4,5]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[6]	Sr[7] or P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See Figure 36 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 38 to see how Host ends target device operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

6.18.7.4 Read Command Data Packet Error Handling - PEC Enabled (cont'd)

Read command - If no parity error and no PEC error:

- The PMIC device sends ACK back to the host when Host perform a Start Repeat operation.
- The PMIC device executes the command and sends the data as shown in Table 57.
- The PMIC computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in the cells in Table 57.

Read command - if parity error or PEC error:

- The PMIC device discards the byte in the packet that had a parity error.
- The PMIC device discards second byte in that packet if a parity error occurred in first byte. The PMIC device may or may not check parity for the second byte in that packet.
- The PMIC device discards the packet if there is a PEC error.
- The PMIC sends NACK back to the host when Host perform Start Repeat operation. This is shown in the RED colored cell in Table 57. The NACK represents either PEC error or a parity error in one of the two bytes or that PMIC is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. The PEC calculation by PMIC device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes the device select code of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the PMIC target device NACKs due to PEC error or a parity error in previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The PMIC device does not send any data shown in Table 57 and instead expects Host to perform STOP operation.
- The PMIC device sets Table 106, Register 0x0A [3:2] accordingly and Table 106, Register 0x0A [1] to '1'; P_Err, PEC_Err in GETSTATUS CCC to '1' accordingly; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

6.18.8 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/Write operations.

6.18.9 Error Reporting

All error conditions detected by the PMIC devices are captured in Table 104, Register 0x08 to Table 107, Register 0x0B, and Table 147, Register 0x33 registers.

There are four different possible ways error information can be communicated to the host.

1. The host makes the read request to Table 104, Register 0x08 to Table 107, Register 0x0B, and Table 147, Register 0x33 registers.
2. The host starts any transaction with Start condition followed by 7'h7E IBI header.
3. The PMIC device sends in band interrupt if enabled, when its SCL and SDA input has been idle for t_{AVAL} time.
4. The PMIC device asserts GSI_n pin if enabled.

6.18.10 I3C Basic Common Command Codes (CCC)

The I3C Basic spec lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The PMIC device NACKs for all unsupported CCC. The PMIC supports CCC as listed in Table 58.

The host shall not access any device specific registers or issue any CCC after VR Enable command (i.e., Table 146, Register 0x32 [6] = '1' or VR_EN pin asserted high) until tPMIC_PWR_GOOD_OUT timing parameter is satisfied.

The PMIC device requires STOP operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address Pointer mode operation must be followed by STOP operation before continuing to any CCC operation. The PMIC device also requires STOP operation between any direct CCC to broadcast CCC.

The PMIC device does allow Repeat Start operation between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

Table 58 — PMIC CCC Support Requirement

CCC	Mode	Code	Description	Note
ENEC	Broadcast	0x00	Enable Event Interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable Event Interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I^2C Mode (aka: Reset Dynamic Address Assignment)	
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)	
GETSTATUS	Direct	0x90	Get Device Status	
DEVCAP	Direct	0xE0	Get Device Capability	1
SETHID	Broadcast	0x61	PMIC updates its 3-bit HID Code register	1
DEVCTRL	Broadcast	0x62	Configure SPD Hub and all devices behind Hub	1

NOTE 1 JEDEC specific CCC.

6.18.10.1 ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. When ENEC CCC is registered by the PMIC, it updates Table 148, Register 0x34 [6] = '1' and it takes in effect at the next Start operation (i.e., after STOP operation). Table 59 to Table 62 show an example of a single ENEC CCC. Table 63 shows the encoding definition for ENEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

6.18.10.1 ENEC CCC (cont'd)

Table 59 — ENEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 60 — ENEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 61 — ENEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							ENINT	T	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.
NOTE 3 Repeat Start or Repeat Start with 7'h7E.

6.18.10.1 ENEC CCC (cont'd)

Table 62 — ENEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							ENINT	T	
	PEC								T	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the Host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 63 — ENEC CCC Byte Encoding

Bit	Encoding	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = '0'

6.18.10.2 DISEC CCC

The DISEC CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. When DISEC CCC is registered by the PMIC, it updates Table 148, Register 0x34 [6] = '0'and it takes in effect at the next Start operation (i.e., after STOP operation). Table 64 to Table 67 show an example of a single DISEC CCC. Table 68 shows the encoding definition for DISEC CCC.

If I3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 64 — DISEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

6.18.10.2 DISEC CCC (cont'd)

Table 65 — DISEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	
	PEC								T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 66 — DISEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							DISINT	T	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.
NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 67 — DISEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A[1,2]	
	0x00							DISINT	T	
	PEC								T	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.
NOTE 3 Repeat Start or Repeat Start with 7'h7E.

6.18.10.2 DISEC CCC (cont'd)

Table 68 — DISEC CCC Byte Encoding

Bit	Encoding	Notes
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = '0'

6.18.10.3 RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e., the RSTDAA command is not executed internally and any bytes arriving after the 0x06 RSTDAA Broadcast CCC are ignored for all purposes, including parity checking, until the next STOP operation or Repeat START with 7'h7E is received). When RSTDAA CCC is registered by the PMIC, it updates Table 146, Register 0x32 [6] = '0', it disables PEC and IBI function (Table 148, Register 0x34 [7:6] = '00') and clears parity function Table 148, Register 0x34 [5] = '0') and it takes in effect at the next Start operation (i.e., after STOP operation).

Table 69 and Table 70 show an example of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 69 — RSTDAA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x06 (Broadcast)								T	P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

Table 70 — RSTDAA CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x06 (Broadcast)								T	
	PEC								T	P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

6.18.10.4 SETAASA CCC

The SETAASA CCC is only supported when device is in I^2C mode. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any parity error, the host shall limit the maximum speed of operation for this CCC to 1 MHz. In I3C Basic mode, this CCC is ignored (i.e., the SETAASA CCC is not executed internally). When SETAASA CCC is registered by the PMIC, it updates Table 146, Register 0x32 [6] = '1' and it takes in effect at the next Start operation (i.e., after STOP operation). Table 71 shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as devices is in I^2C mode and there is no PEC function in I^2C mode.

Table 71 — SETAASA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

6.18.10.5 GETSTATUS CCC

The GETSTATUS CCC is supported in I3C Basic mode. In I^2C mode, this CCC is ignored (i.e., it is not executed internally and the Repeat Start byte arriving after the 0x90 GETSTATUS CCC code is not acknowledged and host must do STOP operation). Table 72 to Table 73 show an example of a single GETSTATUS CCC.

If I3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 72 — GETSTATUS CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R=1	A[1]	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

6.18.10.5 GETSTATUS CCC (cont'd)

Table 73 — GETSTATUS CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A[1]	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	
	PEC								T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 74 — GETSTATUS CCC Byte Encoding

Bit	Encoding	Notes
PEC_Err	0 = No Error 1 = PEC Error Occurred	This register is cleared when Host issues clear command to Table 114, Register 0x12 [3] for PEC error
P_Err	0 = No Error 1 = Protocol Error; Parity Error occurred	This register is cleared when Host issues clear command to Table 114, Register 0x12 [2].
Pending Interrupt	0000 = No Pending Interrupt or No New Global Status Event 0001 = Pending Interrupt or New Global Status Event All other encodings are reserved	This register is cleared when Host issues clear command to any appropriate device status register that causes IBI Status register to get cleared.

When the PMIC device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command by writing '1' to appropriate status or by issuing Global Clear command. Once the PMIC device clears the appropriate status register, only then PEC_Err, P_Err and Pending Interrupt Bits [3:0] gets cleared.

After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register Table 106, Register 0x0A [1] to '1' and Pending Interrupt Bits [3:0] to '0001'.

6.18.10.6 DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I^2C mode, it is illegal for host to issue this CCC. Table 75 to Table 76 show an example of a single DEVCAP CCC. Table 77 defines the encoding for DEVCAP CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

6.18.10.6 DEVCAP CCC (cont'd)

Table 75 — DEVCAP CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 76 — DEVCAP CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A[1]	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	
	PEC								T	Sr[2] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 77 — DEVCAP CCC Byte Encoding

Bit	Encoding	Notes
MSB [7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	PMIC hard codes this to '1'.
MSB[1:0]	RFU	Coded as '00'
LSB[7:0]	RFU	Coded as '0x00'

6.18.10.7 SETHID CCC

The SETHID CCC is supported only when device is in I^2C mode. In I^2C mode, when host issues this CCC to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed of operation for this CCC to 1 MHz. In I3C Basic mode, it is illegal for host to issue this CCC. When SETHID CCC is registered by the PMIC, it updates Table 148, Register 0x34 [3:1] with the HID code received by the PMIC and it takes in effect at the next Start operation (i.e., after STOP operation). Table 78 shows an example of a single SETHID CCC. As the device is in I^2C mode when SETHID CCC is issued, the PEC function is not supported.

Once PMIC receives SETHID CCC and updates its 3-bit HID code, after the Stop operation, PMIC device only responds to updated 7-bit address. The 4-bit LID code of the PMIC device remains as is.

The Host may issue SETHID CCC more than one time.

Table 78 — SETHID CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0000				HID			0	T	P

6.18.10.8 DEVCTRL CCC

On a typical I3C bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub devices, there are 4 local target devices totaling up to 40 or more devices on I3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e., Packet Error Check), the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I^2C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed of operation for this CCC to 1 MHz.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

The host must pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (e.g., RegMod = '1'), the host must still follow any device register restriction. For instance, if any device specific register such as IO timing parameter related register require STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

There are additional restrictions that host must pay attention to:

- DEVCTRL CCC must be followed by STOP operation before starting a device specific register access. In other words, host shall avoid DEVCTRL CCC followed by Repeat Start to do a device specific register operation. Note that host is allowed to do multiple DEVCTRL CCC with Repeat Start in between to the same device or across multiple devices.
- DEVCTRL CCC must be followed by STOP operation before starting Default Read Address Pointer Mode even across different devices.

6.18.10.8 DEVCTRL CCC (cont'd)

Table 79 — DEVCTRL CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T[2]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device select code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

Table 80 — DEVCTRL CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T[2]	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr[3] or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device select code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

6.18.10.8 DEVCTRL CCC (cont'd)

Table 81 — DEVCTRL CCC Command Definition

Parameter	Definition
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; PMIC device responds if DevID[6:0] field matches with PMIC device's own 7-bit address (4-bit LID + 3-bit HID) 011 = Multicast Command; PMIC device and possible other device responds if DevID[6:3] field matches with PMIC device's own 4-bit LID address 111 = Broadcast Command; All devices responds to this command All other encodings are reserved
StartOffset[1:0]	Only applicable if RegMod = '0' Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e., StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e., StartOffset[1:0] and PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

6.18.10.8 DEVCTRL CCC (cont'd)

Table 82 — DEVCTRL CCC Data Payload Definition

Byte #	Bit #	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable	Table 148, Register 0x34 [7] is updated
	[6]	Parity Disable	0 = Enable 1 = Disable	Table 148, Register 0x34 [5] is updated
	[5:2]	RFU	RFU	
	[1]	VR Enable	0 = VR Disable 1 = VR Enable	Table 146, Register 0x32 [7] is updated. Only PMIC device responds to this bit. All other devices ignore this bit.
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global and IBI Clear	0 = No Action 1 = Clear All Event and pending IBI[1]	Table 116, Register 0x14 [0] is updated.
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	

NOTE 1 After target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.

6.18.10.8.1 DEVCTRL CCC Examples - RegMod = '0'

Table 83 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of '1001' on I3C bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable parity function. The host sends AddrMask = '011' to indicate Multicast command with DevID[6:3] match; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices with DevID[6:3] that match to '1001' will do the VR Enable command and DevID[6:3] that matches to '0110' will disable the parity function.

6.18.10.8.1 DEVCTRL CCC Examples - RegMod = '0' (cont'd)

Table 83 — DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 84 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicates general register. Upon receiving this command, all devices will enable PEC function.

Table 84 — DEVCTRL CCC Example - Broadcast Command to all Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 85 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unitcast command to enable VR on DIMM5. The host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicates general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

6.18.10.8.1 DEVCTRL CCC Examples - RegMod = '0' (cont'd)

Table 85 — DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

6.18.10.8.2 DEVCTRL CCC Examples - RegMod = '1'

Table 86 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively followed by all devices with 4-bit LID of '1001' on the I3C Basic bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

6.18.10.8.2 DEVCTRL CCC Examples - RegMod = '1' (cont'd)

Table 86 — DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 87 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 87 — DEVCTRL CCC Example - Multicast Command to '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A[1]	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	P

NOTE 1 See Figure 34 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

6.18.11 IO Operation

At power on, by default, the PMIC device comes up in I^2C mode of operation with Open Drain IO for its management interface. The maximum speed is limited to 1 MHz and supported IO voltage levels are from 1.0 V to 3.3 V.

After power on, the host may put the interface of the PMIC device in I3C Basic mode of operation.

In I3C Basic mode, the host may drive the SCL clock input of the PMIC device using either Push-Pull output driver or using the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the host may always drive the SCL clock input using a Push-Pull output driver.

To support in band interrupt, the PMIC device supports dynamic switching between Open Drain mode and Push Pull mode on its SDA bus for various event. The Table 88 below describes the different mode of operation by the PMIC device for each cycle in I3C Basic mode.

Table 88 — PMIC Device Dynamic IO Operation Mode Switching; I3C Basic Mode

	Open Drain Mode	Push Pull Mode
START + Device Select Code	Yes	No
START + 7'h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Code	No	Yes
REPEAT START + 7'h7E Header Byte	No	Yes
CCC Byte (i.e., after 7'h7E+W=0+ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

6.18.12 Bus Clear

The device supports the following described Bus Clear feature in I^2C mode only. Any attempt by host to perform I^2C Bus clear on a target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the target device is in the middle of outputting data for read operation. For these type of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

6.18.13 Bus Reset

To prevent a malfunctioning device from locking up the I^2C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on SCL as shown in Figure 41 to force a device bus reset. All devices on a I^2C or I3C Basic bus reset simultaneously. Bus reset operation works same way regardless of whether device is operating in I^2C or I3C Basic mode.

To guarantee the PMIC resets I^2C bus or I3C Basic bus, the SCL clock input Low time has to be greater than or equal to $t_{TIMEOUT(Max)}$.

The PMIC device does not reset I^2C bus or I3C Basic bus if the SCL clock input Low time is less than $t_{TIMEOUT(Min)}$.

If the SCL clock input Low time is between $t_{TIMEOUT(Min)}$ and $t_{TIMEOUT(Max)}$, the PMIC device does not guarantee and it may or may not reset the I^2C bus or I3C Basic bus.

When RESET, the PMIC device takes following action.

1. Interface and any pending command or transactions are cleared
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Device returns to I^2C mode of operation; resets Table 106, Register 0x0A [3:2] = ‘00’; resets Table 146, Register 0x32 [6] = ‘0’; resets Table 148, Register 0x34 [7:5] = ‘000’; resets Table 148, Register 0x34 [3:1] = ‘111’.
4. Device does not re-sample PID pin.
5. Device floats the SDA pin such that it gets pulled High by the external or Hub device pullup resistor.
6. Device treats bus reset as STOP operation.

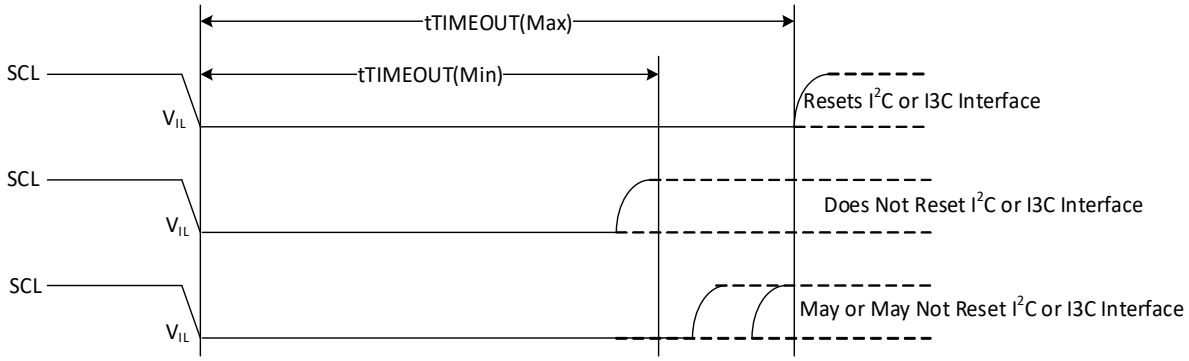


Figure 41 — I^2C or I3C Basic Bus Reset of PMIC

6.18.14 Command Truth Table

The command truth table only applies in I3C Basic mode with PEC enabled. In I^2C mode and in I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 89 — I3C Basic Mode Only with PEC Enabled Command Truth Table

PMIC Command (CMD Field)	Command Name	Command Code	RW	PMIC 8 bit Register Address [7:0]
		2nd Byte Bits [7:5]	2nd Byte Bit [4]	1st Byte Bits [7:0]
Write 1 Byte to Register	W1R	000	0	V
Read 1 Byte from Register	R1R		1	V
Write 2 Byte to Register	W2R	001	0	V
Read 2 Byte from Register	R2R		1	V
Write 4 Byte to Register	W4R	010	0	V
Read 4 Byte from Register	R4R		1	V
Write 16 Byte to Register	W16R	011	0	V
Read 16 Byte from Register	R16R		1	V
Reserved	RSVD	100	RSVD	RSVD
Reserved	RSVD	101	RSVD	RSVD
Reserved	RSVD	110	RSVD	RSVD
Reserved	RSVD	111	RSVD	RSVD

6.19 Application Notes

6.19.1 Error Injection Test Methodology

The PMIC error injection feature can be used many ways to test the PMIC at either component level or at the module level or at the system level. The error injection feature can be used to debug the PMIC component itself or to simulate the DIMM module behavior in a standalone ATE environment or in the system environment or to develop/simulate the system software to ensure PMIC and DIMM component hardware and system software works in a harmonious way if there is an actual fault event in the system.

The combination matrix to test each type of error injection is very large and it is the responsibility of the PMIC provider to ensure that all combinations are tested. The PMIC component specification does not provide the list in entirety but rather provides one possible general test method for error injection feature.

At all time, the PMIC specification must be followed. The test methodology does not alter or change the meaning of the PMIC specification. The test methodology may add, remove or modify steps in any sequence as long as the PMIC component specification is followed. The test results will vary depending on the starting condition and the sequence of steps. It is the responsibility of PMIC component provider to ensure results are checked against the specific condition and sequence while following the PMIC component specification.

6.19.1 Error Injection Test Methodology (cont'd)

One example of Error injection test after VR Enable command:

1. Power cycle the PMIC; Issue R39 = 0x74 command; observe PWR_GOOD and GSI_n signal.
2. Read the PMIC registers R04 to R0B & R33 (checks all memory and status registers are cleared).
3. Issue the VR Enable command; read the PMIC registers R04 to R0B & R33 (check PMIC successfully turned on the rails without any fault); observe PWR_GOOD and GSI_n signal.
4. Inject error via R35 and select desired error type.
5. Check PMIC regulators are turned off; read the PMIC registers R04 to R0B & R33 (Check appropriate error log and status registers are set); observe PWR_GOOD and GSI_n signal.
6. Power cycle the PMIC.
7. Read the PMIC registers R04 to R07 (checks all memory).
8. Issue R39 = 0x74 command.
9. Read the PMIC registers R04 to R0B & R33.
10. Repeat another error injection test starting step # 3.

7 Volatile Registers Space

7.1 Access Mechanism

7.1.1 Register Attribute Definition

All volatile registers have Base Attributes as defined in Table 90. Some register attributes are further modified with Attribute Modifiers, as defined in Table 91.

Table 90 — Register Base Attributes

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Writes have no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	WO	This bit can only be written by host. Read from this bit returns ‘0’.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return ‘0’ when read. Write has no effect.

Table 91 — Register Attribute Modifier

Attribute	Abbreviation	Description
Write ‘1’ Only	1O	This bit can only be set (i.e., write ‘1’) but not reset (i.e., write ‘0’). Write ‘0’ has no effect.
Protected	P	This bit is protected by the password. This bit cannot be written to unless the password code has been written into the password registers.
Persistent	E	This bit is persistent during power cycle.

7.2 Registers

7.2.1 Register Map Breakdown

Table 92 — Register Map Breakdown

Register Range	Region	Comments
0x00 - 0x3F	Host Region	Host Accessible Registers
0x40 - 0x6F	DIMM Vendor Region	DIMM Vendor Registers - Non Volatile Memory Allows DIMM vendors to program the PMIC for a given DRAM/ DIMM vendor designs. These are password protected registers and password is selected by DIMM vendor. Under normal operation, these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'. These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation.
0x70 - 0xFF	Vendor Specific Region	Vendor Specific Registers - Non Volatile Memory These are vendor specific password protected registers. Under normal operation these registers are not used by any host. These registers require password for read access. Access to these registers without correct password will return all data as '0'.

7.2.2 Memory Protection

The PMIC DIMM vendors registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to DIMM vendor registers are blocked unless it is unlocked by providing the correct password. The default password for DIMM vendor register is 0x9473. The PMIC offers each DIMM vendors to select their own password for DIMM vendor registers.

7.2.3 Steps to Access DIMM Vendor Registers

The steps to access the DIMM vendor registers are as following:

1. Write to register Table 151, Register 0x37 = 8 bit password LSB code.
2. Write to register Table 152, Register 0x38 = 8 bit password MSB code.
3. Write to register Table 153, Register 0x39 = 0x40.
4. Perform Read operations to DIMM vendor registers as desired.
5. Write to register Table 153, Register 0x39 = 0x00.

7.2.4 Steps to Change DIMM Vendor Region Password

By default, the DIMM vendor region register password is 0x9473. The steps to change the password from default password are as following:

1. Write to register Table 151, Register 0x37 = 0x73.
2. Write to register Table 152, Register 0x38 = 0x94.
3. Write to register Table 153, Register 0x39 = 0x40.
4. Write to register Table 151, Register 0x37 = New 8 bit password LSB code as desired by DIMM vendor.
5. Write to register Table 152, Register 0x38 = New 8 bit password MSB code as desired by DIMM vendor.

7.2.4 Steps to Change DIMM Vendor Region Password (cont'd)

6. Write to register Table 153, Register 0x39 = 0x80.
7. Wait 200 ms.
8. Write to register Table 153, Register 0x39 = 0x00.
9. Power cycle the PMIC. (Remove VIN_Bulk supply from the PMIC. The new password is in effect after the power cycle.

7.2.5 Steps to Burn or Program DIMM Vendor Region Registers

The steps to burn or to program the DIMM vendor registers are as following:

1. Write to register Table 151, Register 0x37 = 8 bit password LSB code.
2. Write to register Table 152, Register 0x38 = 8 bit password MSB code.
3. Write to register Table 153, Register 0x39 = 0x40.
4. Programming DIMM vendor registers are done at block level. Block 40 addresses: 0x40 - 0x4F; Block 50 addresses: 0x50 - 0x5F; Block 60 addresses: 0x60 - 0x6F. Perform write operation to each block as desired.
5. Burn each block one at a time: Block 40 addresses: Write register Table 153, Register 0x39 = 0x81. Block 50 addresses: Write register Table 153, Register 0x39 = 0x82. Block 60 addresses: Write register Table 153, Register 0x39 = 0x85.
6. Wait time 200 ms.
7. To check if programming is complete: Perform read from register Table 153, Register 0x39. The code 0x5A indicates it is complete. It takes approximately 200 ms per page to program.
8. To verify if programming is done correctly: Perform read operation from appropriate block addresses.
9. Write to register Table 153, Register 0x39 = 0x00.

7.2.6 Status Registers

The DDR5 PMIC offers status registers that are grouped into four different categories.

1. Global History of Error Log Register (Table 100, Register 0x04 [7:4])
2. Error Log Registers (Table 101, Register 0x05 [6,4:0], Table 102, Register 0x06[7,5:3,1:0], Table 103, Register 0x07 [7:0]; Table 103, Register 0x07 [7:0] is currently defined as Reserved)
3. Real time Status Registers (Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:1], Table 107, Register 0x0B [7,5:3,1:0], Table 147, Register 0x33 [2])
4. Periodic Status Registers (Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0], Table 111, Register 0x0F [7:0], Table 147, Register 0x33 [7:5])

Global History of Error Log Register (Table 100, Register 0x04 [7:4]) - This register records the PMIC state at each abnormal power down cycle. This register reports the cumulative error of each abnormal power down sequence. The PMIC writes this register on its own when it internally generates VR Disable command on its own due to failure. The host can erase this register in MTP memory and clear the status register by writing the code 0x74 in Table 153, Register 0x39.

Error Log Registers (Table 101, Register 0x05 [6,4:0], Table 102, Register 0x06 [7,5:3,1:0],Table 103, Register 0x07 [7:0]).

7.2.6 Status Registers (cont'd)

- These registers record the PMIC state at each power down sequence. The PMIC may report an abnormal power down sequence or a normal power down sequence. The PMIC writes these registers and updates MTP when it internally generates a VR Disable command on its own due to failure. At the next power up, the registers are restored from MTP to be read by the host, and MTP is cleared by the PMIC. A value of '0' in the register indicates that no fault event occurred prior to the previous power down cycle.
- The host can clear the status registers and MTP by writing the code 0x74 in Table 153, Register 0x39.
- See Figure 42 for illustration. The top waveform illustrates how PMIC captures Error Log Registers (R05 to R07) when there is a fault and how PMIC reports error log registers when PMIC goes through power cycle. The bottom waveform illustrates same as top waveform with one exception. It shows no fault condition when PWR_GOOD is asserted to turn off switch regulator outputs with power down sequence.
- The phrase "Power Cycle" is used interchangeably with "Power Down Cycle" as illustrated in both figures and it means the VIN_Bulk input supply is removed and re-applied. "Power Down Sequence" means execution of Power Off Sequence configuration registers (Table 176, Register 0x58 to Table 179, Register 0x5B).

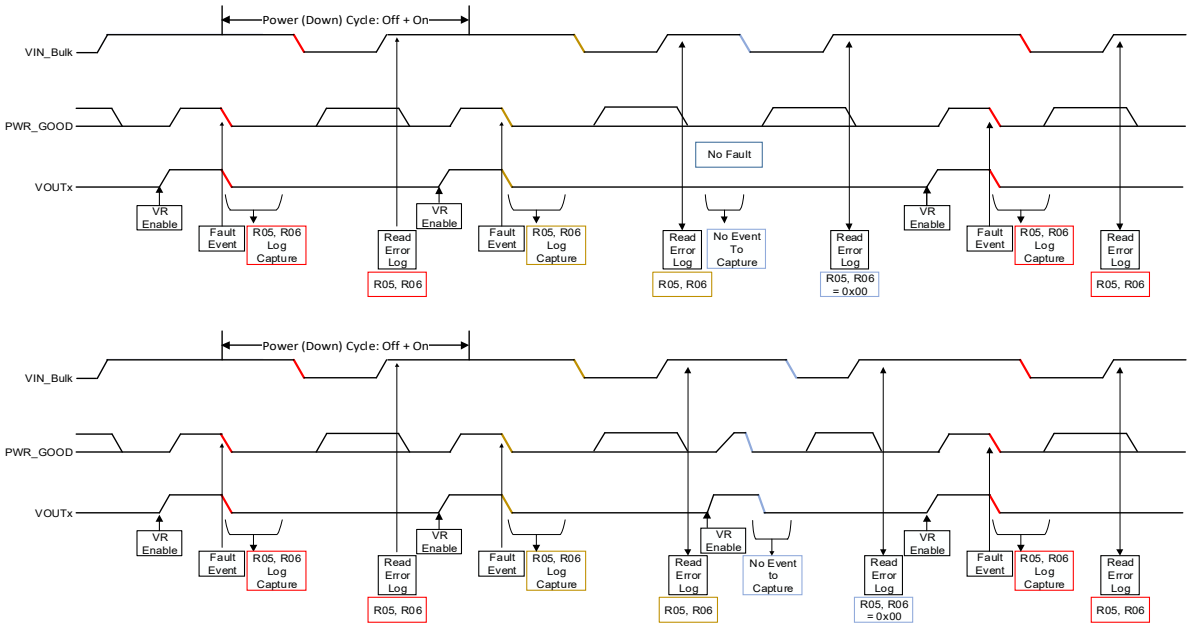


Figure 42 — Error Log (R05 to R07) Registers Behavior with Power Cycle

Real Time Status Registers (Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:1], to Table 107, Register 0x0B [7,5:3,1:0], Table 147, Register 0x33 [2]): These registers are updated to '1' any time based on any event that occurs. The status registers will remain at '1' even if the failing condition is no longer present until the Clear Register command is received by the PMIC. The GSI_n interrupt or PWR_GOOD interrupt may be generated by the PMIC at the same time depending on the type of event. The interrupts are only generated if they are not masked. The status registers Table 104, Register 0x08 [7], Table 105, Register 0x09 [5] and Table 147, Register 0x33 [2] is only valid once valid VIN_Bulk input supply is valid at the PMIC input pin. The remaining status registers are valid after VR Enable command is registered.

Periodic Status Registers (Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0], Table 111, Register 0x0F [7:0], Table 147, Register 0x33 [7:5]) - These registers are updated periodically. These registers are only valid after VR Enable command is registers.

7.2.6 Status Registers (cont'd)

All Read Only (RO) registers except for registers Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0] and Table 111, Register 0x0F [7:0] are one time latched registers. In other words, once PMIC sets those register flag, the host must explicitly clear those registers appropriately. The PMIC does not automatically update the registers on its own even if the event that triggered the status is no longer present. The registers Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0] and Table 111, Register 0x0F [7:0] are dynamically updated by the PMIC at certain frequency and they represent the status at that point.

7.2.7 Clear Registers

For each Real Time Status Registers (Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:1], Table 107, Register 0x0B [7,5:3,1:0], Table 147, Register 0x33 [2]), the DDR5 PMIC offers a way to clear the status of each event. The clear registers are Table 112, Register 0x10 [5,3:2,0], Table 113, Register 0x11 [7,5,3,1:0], Table 114, Register 0x12 [7,5:2], Table 115, Register 0x13 [7,5:3,1:0] and to Table 116, Register 0x14 [2] respectively. All clear registers are write '1' only registers. When '1' is written to any of the clear registers, the PMIC updates the status registers to default state and removes the interrupt condition on GSI_n and PWR_GOOD output signal assuming that event is no longer present. If the failing condition is still present, the status register will still remain at '1'. Note that GSI_n and PWR_GOOD interrupt is only applicable if that event is not masked. GSI_n output signal can be disabled.

When '1' is written to any of the clear registers, there are three categories of response by the PMIC.

1. PMIC removes GSI_n interrupt (PWR_GOOD interrupt is not applicable. Related status registers are: Table 113, Register 0x11 [7,3,1:0], Table 115, Register 0x13 [7,5:4].
2. PMIC removes GSI_n and PWR_GOOD interrupt. Related status registers are: Table 112, Register 0x10 [5,3:2], Table 113, Register 0x11 [5], Table 116, Register 0x14 [2].
3. PMIC only removes GSI_n interrupt and does not remove PWR_GOOD interrupt. Related status registers are: Table 112, Register 0x10 [0], Table 114, Register 0x12 [7,5:4], Table 115, Register 0x13 [3,1:0]. The host is expected to either power cycle the PMIC or re-issue the VR Enable command if PMIC is in programmable mode.

The PMIC offers a Global Clear command by writing '1' to registers Table 116, Register 0x14 [0]. This command works same way as individual clear command. This command can alternatively be used by the host if more than one clear command is required to different registers.

7.2.8 Mask Registers

For each Real Time Status Registers (Table 104, Register 0x08 [6:5,3:2,0], Table 105, Register 0x09 [7,5,3,1:0], Table 106, Register 0x0A [7,5:1], Table 107, Register 0x0B [7,5:3,1:0], Table 147, Register 0x33 [2]), the PMIC offers a way to mask the status of each event interrupt. The mask registers are Table 117, Register 0x15 [5,3:2,0], Table 118, Register 0x16 [7,5,3,1:0], Table 119, Register 0x17 [7,5:2], Table 120, Register 0x18 [7,5:3,1:0] and Table 121, Register 0x19 [2] respectively. The mask registers only masks the event interrupt on GSI_n and PWR_GOOD signal.

There is also a global mask register bits control Table 143, Register 0x2F [1:0] to control the GSI_n and PWR_GOOD output signal. When all mask registers are Table 117, Register 0x15 [5,3:2,0], Table 118, Register 0x16[7,5,3,1:0], Table 119, Register 0x17[7,5:2], Table 120, Register 0x18 [7,5:3,1:0], Table 121, Register 0x19 [2] configured as '0', the setting in Table 143, Register 0x2F [1:0] does not matter. The setting in Table 143, Register 0x2F [1:0] only matters when one or more mask registers Table 117, Register 0x15 [5,3:2,0], Table 118, Register 0x16 [7,5,3,1:0], Table 119, Register 0x17 [7,5:2], Table 120, Register 0x18 [7,5:3,1:0], Table 121, Register 0x19 [2] are configured to '1'.

7.2.8 Mask Registers (cont'd)

For any failure events that causes the PMIC to generate VR Disable command on its own, the mask register bits (Table 117, Register 0x15 [0], Table 119, Register 0x17 [7,5:4], Table 120, Register 0x18 [3,1:0] and Table 143, Register 0x2F [1:0]) do not apply and PMIC will assert PWR_GOOD output signal regardless of the setting in mask registers. The PMIC still updates the status registers appropriately when any event occurs. When masked, the host is expected to read the status registers periodically to learn if any of the event has occurred or not. The host can mask or un-mask each event individually. The host can mask or un-mask at any time in programmable mode. In secure mode of operation, the mask registers are locked.

7.2.9 Host Region Register Map

Table 93 — Host Region - Register Map - Color Coding Scheme

Region	Register Range	Restriction
Host Region + DIMM Vendor Region + Vendor specific Region	Table 117, Register 0x15 to Table 143, Register 0x2F Table 146, Register 0x32 [7,5:0] Table 149, Register 0x35 Table 150, Register 0x36 Table 158, Register 0x40 to Register 0x6F Register 0x70 to Register 0xFF	Register Modification is NOT allowed in Secure Mode
Host Region	Table 128, Register 0x20 to Table 141, Register 0x2D,	Registers are copied from DIMM Vendor Region Setting at power on

Table 94 — Host Region - Register Map

Register	Attribute	Description
Table 96, Register 0x00	ROE	R00 [7:0] Serial Number - Byte 0
Table 97, Register 0x01	ROE	R01 [7:0] Serial Number - Byte 1
Table 98, Register 0x02	ROE	R02 [7:0] Serial Number - Byte 2
Table 99, Register 0x03	ROE	R03 [7:0] Serial Number - Byte 3
Table 100, Register 0x04	ROE	R04 [7] Global Error Count R04 [6] Global Error Log - Buck OV or UV R04 [5] Global Error Log - VIN_Bulk OV R04 [4] Global Error Log - Critical Temperature R04 [3:0] Reserved
Table 101, Register 0x05	ROE	R05 [7] Reserved R05 [6] Power On Reset - SWA Power Not Good R05 [5] Reserved R05 [4:3] Power On Reset - SWB & SWC Power Not Good R05 [2:0] Power On Reset - High Level Error Log Code
Table 102, Register 0x06	ROE	R06 [7] Power On Reset - SWA Under Voltage Lockout R06 [6] Reserved R06 [5:4] Power On Reset - SWB & SWC Under Voltage Lockout R06 [3] Power On Reset - SWA Over Voltage R06 [2] Reserved R06 [1:0] Power On Reset - SWB & SWC Over Voltage
Table 103, Register 0x07	ROE	R07 [7:0] Reserved

Table 94 — Host Region - Register Map (cont'd)

Register	Attribute	Description
Table 104, Register 0x08	RO	R08 [7] Reserved R08 [6] Critical Temperature Shutdown Status R08 [5] SWA Output Power Good Status R08 [4] Reserved R08 [3:2] SWB, SWC Output Power Good Status R08 [1] Reserved R08 [0] VIN_Bulk Input Over Voltage Status
Table 105, Register 0x09	RO	R09 [7] PMIC High Temperature Warning Status R09 [6] Reserved R09 [5] VOUT_1.8V Output Power Good Status R09 [4] Reserved R09 [3] SWA High Output Current Consumption Warning Status R09 [2] Reserved R09 [1:0] SWB, SWC High Output Current Consumption Warning Status
Table 106, Register 0x0A	RO	R0A [7] SWA Output Over Voltage Status R0A [6] Reserved R0A [5:4] SWB, SWC Output Over Voltage Status R0A [3] PEC Error Status R0A [2] Parity Error Status R0A [1] IBI Status R0A [0] Reserved
Table 107, Register 0x0B	RO	R0B [7] SWA Output Current Limiter Warning Status R0B [6] Reserved R0B [5:4] SWB, SWC Output Current Limiter Warning Status R0B [3] SWA Output Under Voltage Lockout Status R0B [2] Reserved R0B [1:0] SWB, SWC Output Current Limiter Warning Status
Table 108, Register 0x0C	RO	R0C [7:0] SWA Output Current or Power or Total Output Power Measurement
Table 109, Register 0x0D	ROE	R0D [7:0] Serial Number - Byte 4
Table 110, Register 0x0E	RO	R0E [7:0] SWB Output Current or Power Measurement
Table 111, Register 0x0F	RO	R0F [7:0] SWC Output Current or Power Measurement
Table 112, Register 0x10	1O	R10 [7:6] Reserved R10 [5] Clear SWA Output Power Good Status R10 [4] Reserved R10 [3:2] Clear SWB, SWC Output Power Good Status R10 [1] Reserved R10 [0] Clear VIN_Bulk Input Over Voltage Status
Table 113, Register 0x11	1O	R11 [7] Clear PMIC High Temperature Warning Status R11 [6] Reserved R11 [5] Clear VOUT_1.8V Output Power Good Status R11 [4] Reserved R11 [3] Clear SWA High Output Current Consumption Warning Status R11 [2] Reserved R11 [1:0] Clear SWB, SWC High Output Current Consumption Warning Status

Table 94 — Host Region - Register Map (cont'd)

Register	Attribute	Description
Table 114, Register 0x12	1O	R12 [7] Clear SWA Output Over Voltage Status R12 [6] Reserved R12 [5:4] Clear SWB, SWC Output Over Voltage Status R12 [3] Clear PEC Error R12 [2] Clear Parity Error R12 [1:0] Reserved
Table 115, Register 0x13	1O	R13 [7:4] Clear SWA Output Current Limiter Warning Status R13 [6] Reserved R13 [5:4] Clear SWB, SWC Output Current Limiter Warning Status R13 [3] Clear SWA Output Under Voltage Lockout Status R13 [2] Reserved R12 [1:0] Clear SWB, SWC Output Under Voltage Lockout Status
Table 116, Register 0x14	1O	R14 [7:4] Reserved R14 [3] Clear VIN_Bulk Input Under Voltage Lockout Status R14 [2] Clear VOUT_1.0V Output Power Good Status R14 [1] Reserved R14 [0] Clear Global Status
Table 117, Register 0x15	RW	R15 [7:6] Reserved R15 [5] Mask SWA Output Power Good Status R15 [4] Reserved R15 [3:2] Mask SWB, SWC Output Power Good Status R15 [1] Reserved R15 [0] Mask VIN_Bulk Input Over Voltage Status
Table 118, Register 0x16	RW	R16 [7] Mask PMIC High Temperature Warning Status R16 [6] Reserved R16 [5] Mask VOUT_1.8V Output Power Good Status R16 [4] Reserved R16 [3] Mask SWA High Output Current Consumption Warning Status R16 [2] Reserved R16 [1:0] Mask SWB, SWC High Output Current Consumption Warning Status
Table 119, Register 0x17	RW	R17 [7] Mask SWA Output Over Voltage R17 [6] Reserved R17 [5:4] Mask SWB, SWC Output Over Voltage R17 [3] Mask PEC Error Status R17 [2] Mask Parity Error Status R17 [1:0] Reserved
Table 120, Register 0x18	RW	R18 [7] Mask SWA Output Current Limiter Warning Status R18 [6] Reserved R18 [5:4] Mask SWB, SWC Output Current Limiter Warning Status R18 [3] Mask SWA Output Under Voltage Lockout Status R18 [2] Reserved R18 [3:0] Mask SWB, SWC Output Under Voltage Lockout Status
Table 121, Register 0x19	RW	R19 [7:4] Reserved R19 [3] Mask VIN_Bulk Input Under Voltage Lockout Status R19 [2] Mask VOUT_1.0 V Output Power Good Status R19 [1:0] Reserved

Table 94 — Host Region - Register Map (cont'd)

Register	Attribute	Description
Table 122, Register 0x1A	RW	R1A [7:5] Reserved R1A [4] Quiescent Power State Entry Enable R1A [3] Reserved R1A [2] VOUT_1.8 V Power Good Threshold Voltage R1A [1] Output Power Select R1A [0] VOUT_1.0 V Power Good Threshold Voltage
Table 123, Register 0x1B	RW	R1B [7] VIN_Bulk Input Over Voltage Threshold R1B [6] Current or Power Meter Select R1B [5] Reserved R1B [4] Global Mask PWR_GOOD Output Pin R1B [3] GSI_n Pin Enable R1B [2:0] PMIC High Temperature Warning Threshold
Table 124, Register 0x1C	RW	R1C [7:0] SWA Output High Current Threshold
Table 125, Register 0x1D	RW	R1D [7:0] Reserved
Table 126, Register 0x1E	RW	R1E [7:0] SWB Output High Current Threshold
Table 127, Register 0x1F	RW	R1F [7:0] SWC Output High Current Threshold
Table 128, Register 0x20	RW	R20 [7:6] SWA Output Current Limiter Warning Threshold R20 [5:4] Reserved R20 [3:2] SWB Output Current Limiter Warning Threshold R20 [1:0] SWC Output Current Limiter Warning Threshold
Table 129, Register 0x21,	RW	R21 [7:1] SWA Voltage Setting R21 [0] SWA Power Good Low Side Threshold
Table 130, Register 0x22,	RW	R22 [7:6] SWA Power Good High Side Threshold R22 [5:4] SWA Over Voltage Threshold R22 [3:2] SWA Under Voltage Lockout Threshold R22 [1:0] SWA Soft Stop Time
Table 131, Register 0x23	RW	R23 [7:0] Reserved
Table 132, Register 0x24	RW	R24 [7:0] Reserved
Table 133, Register 0x25,	RW	R25 [7:1] SWB Voltage Setting R25 [0] SWB Power Good Low Side Threshold
Table 134, Register 0x26,	RW	R26 [7:6] SWB Power Good High Side Threshold R26 [5:4] SWB Over Voltage Threshold R26 [3:2] SWB Under Voltage Lockout Threshold R26 [1:0] SWB Soft Stop Time
Table 135, Register 0x27,	RW	R27 [7:1] SWC Voltage Setting R27 [0] SWC Power Good Low Side Threshold
Table 136, Register 0x28,	RW	R28 [7:6] SWC Power Good High Side Threshold R28 [5:4] SWC Over Voltage Threshold R28 [3:2] SWC Under Voltage Lockout Threshold R28 [1:0] SWC Soft Stop Time
Table 137, Register 0x29,	RW	R29 [7:6] SWA Mode Select R29 [5:4] SWA Switching Frequency R29 [3:0] Reserved
Table 138, Register 0x2A,	RW	R2A [7:6] SWB Mode Select R2A [5:4] SWB Switching Frequency R2A [3:2] SWC Mode Select R2A [1:0] SWC Switching Frequency
Table 139, Register 0x2B,	RW	R2B [7:6] VOUT_1.8 V LDO Setting R2B [5:3] Reserved R2B [2:1] VOUT_1.0 V LDO Setting R2B [0] Reserved

Table 94 — Host Region - Register Map (cont'd)

Register	Attribute	Description
Table 140, Register 0x2C,	RW	R2C [7:5] SWA Soft Start Time R2C [4:0] Reserved
Table 141, Register 0x2D,	RW	R2D [7:5] SWB Soft Start Time R2D [4] Reserved R2D [3:1] SWC Soft Start Time R2D [0] Reserved
Table 142, Register 0x2E	RW	R2E [7:3] Reserved R2E [2:0] PMIC Shutdown temperature threshold
Table 143, Register 0x2F	RW	R2F [7] Reserved R2F [6] SWA Enable R2F [5] Reserved R2F [4:3] SWB, SWC Enable R2F [2] Secure or Programmable Mode Select R2F [1:0] Mask Bits Register Control
Table 144, Register 0x30	RW	R30 [7] ADC Enable R30 [6:3] ADC Select R30 [2] Reserved R30 [1:0] ADC Register Update Frequency
Table 145, Register 0x31	RO	R31 [7:0] ADC Read Out
Table 146, Register 0x32	RW, RO	R32 [7] VR Enable R32 [6] Management Interface Selection R32 [5] PWR_GOOD Signal IO Type R32 [4:3] PMIC Power Good Output Signal Control R32 [2] Reserved R32 [1:0] ADC Accuracy Step Size
Table 147, Register 0x33	RO	R33 [7:5] Temperature Measurement R33 [4] Reserved R33 [3] VIN_Bulk Input Under Voltage Lockout Status R33 [2] VOUT_1.0V Output Power Good Status R33 [1:0] Reserved
Table 148, Register 0x34	RO	R34 [7] PEC Enable R34 [6] IBI Enable R34 [5] Parity Disable R34 [4] Reserved R34 [3:1] HID_CODE R34 [0] Reserved
Table 149, Register 0x35	RW	R35 [7] Error Injection Enable R35 [6:4] Rail Selection R35 [3] Over and Under Voltage Select R35 [2:0] Misc. Error Injection Type
Table 150, Register 0x36	RV	R36 [7:4] Soft Stop Time Extension
	RW	R36 [3:1] Acoustic Noise Prevention Control
	RV	R36 [0] Reserved
Table 151, Register 0x37	WO	R37 [7:0] Password Lower Byte 0
Table 152, Register 0x38	WO	R38 [7:0] Password Upper Byte 1
Table 153, Register 0x39	RW	R39 [7:0] Command Codes
Table 154, Register 0x3A	RW	R3A [7] Reserved R3A [6] Default Read Address Pointer Enable R3A [5:4] Default Read Address Pointer Selection R3A [3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A [1:0] Reserved

Table 94 — Host Region - Register Map (cont'd)

Register	Attribute	Description
Table 155, Register 0x3B	ROE	R3B [7] Reserved R3B [6] PMIC Part Capability R3B [5:4] Major Revision ID R3B [3:1] Minor Revision ID R3B [0] Reserved
Table 156, Register 0x3C	ROE	R3C [7:0] VENDOR_ID_BYTE0
Table 157, Register 0x3D	ROE	R3D [7:0] VENDOR_ID_BYTE1
0x3E	RV	R3E [7:0] Reserved
0x3F	RV	R3F [7:0] Reserved

7.2.10 DIMM Vendor Region Register Map

Table 95 — DIMM Vendor Region - Register Map

Register	Attribute	Description
Table 158, Register 0x40	RWPE	R40 [7:0] Power On Sequence - Configuration 0
Table 159, Register 0x41,	RWPE	R41 [7:0] Power On Sequence - Configuration 1
Table 160, Register 0x42,	RWPE	R42 [7:0] Power On Sequence - Configuration 2
Table 161, Register 0x43	RWPE	R43 [7:0] Reserved
Table 162, Register 0x44	RWPE	R44 [7:4] Soft Stop Time Extension R44 [3:0] Reserved
Table 163, Register 0x45	RWPE	R45 [7:1] SWA Voltage Setting R45 [0] SWA Power Good Low Side Threshold
Table 164, Register 0x46	RWPE	R46 [7:6] SWA Power Good High Side Threshold R46 [5:4] SWA Over Voltage Threshold R46 [3:2] SWA Under Voltage Lockout Threshold R46 [1:0] SWA Soft Stop Time
Table 165, Register 0x47	RWPE	R47 [7:0] Reserved
Table 166, Register 0x48	RWPE	R48 [7:0] Reserved
Table 167, Register 0x49	RWPE	R49 [7:1] SWB Voltage Setting R49 [0] SWB Power Good Low Side Threshold
Table 168, Register 0x4A	RWPE	R4A [7:6] SWB Power Good High Side Threshold R4A [5:4] SWB Over Voltage Threshold R4A [3:2] SWB Under Voltage Lockout Threshold R4A [1:0] SWB Soft Stop Time
Table 169, Register 0x4B	RWPE	R4B [7:1] SWC Voltage Setting R4B [0] SWC Power Good Low Side Threshold
Table 170, Register 0x4C	RWPE	R4C [7:6] SWC Power Good High Side Threshold R4C [5:4] SWC Over Voltage Threshold R4C [3:2] SWC Under Voltage Lockout Threshold R4C [1:0] SWC Soft Stop Time
Table 171, Register 0x4D	RWPE	R4D [7:6] SWA Mode Select R4D [5:4] SWA Switching Frequency R4D [3:0] Reserved
Table 172, Register 0x4E	RWPE	R4E [7:6] SWB Mode Select R4E [5:4] SWB Switching Frequency R4E [3:2] SWC Mode Select R4E [1:0] SWC Switching Frequency
Table 173, Register 0x4F	RWPE	R4F [7:1] Reserved R4F [0] SWA and SWB Single or Dual Phase Regulator Mode Select

Table 95 — DIMM Vendor Region - Register Map (cont'd)

Register	Attribute	Description
Table 174, Register 0x50	RWPE	R50 [7:6] SWA Output Current Limiter Warning Threshold R50 [5:4] Reserved R50 [3:2] SWB Output Current Limiter Warning Threshold R50 [1:0] SWC Output Current Limiter Warning Threshold
Table 175, Register 0x51	RWPE	R51 [7:6] VOUT_1.8V LDO Output Voltage Setting R51 [5:3] Reserved R51 [2:1] VOUT_1.0V LDO Voltage Setting R51 [0] Reserved
0x52 to 0x57	RV	R52 [7:0] to R57 [7:0] Reserved
Table 176, Register 0x58	RWPE	R58 [7:0] Power Off Sequence - Configuration 0
Table 177, Register 0x59,	RWPE	R59 [7:0] Power Off Sequence - Configuration 1
Table 178, Register 0x5A,	RWPE	R5A [7:0] Power Off Sequence - Configuration 2
Table 179, Register 0x5B	RWPE	R5B [7:0] Reserved
0x5C	RV	R5C [7:0] Reserved
Table 180, Register 0x5D	RWPE	R5D [7:5] SWA Soft Start Time R5D [4:0] Reserved
Table 181, Register 0x5E	RWPE	R5E [7:5] SWB Soft Start Time R5E [4] Reserved R5E [3:1] SWC Soft Start Time R5E [0] Reserved
0x5F to 0x6F	RV	R5F [7:0] to R6F [7:0] Reserved

7.2.11 Register Definition

Table 96 — Register 0x00

	R00		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R00 [7:0]: SERIAL_NUMBER_BYTE_0 Byte 0 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 97 — Register 0x01

	R01		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R01 [7:0]: SERIAL_NUMBER_BYTE_1 Byte 1 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 98 — Register 0x02

	R02		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R02 [7:0]: SERIAL_NUMBER_BYTE_2 Byte 2 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

Table 99 — Register 0x03

	R03		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R03 [7:0]: SERIAL_NUMBER_BYTE_3 Byte 3 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

7.2.11 Register Definition (cont'd)

Table 100 — Register 0x04

	R04		
Bits	**Attribute**	**Default**	**Description[1,2]**
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation[3] 0 = No Error or Only 1 Error since last Erase operation 1 = > 1 Error Count since last Erase operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Over or Under Voltage[4] 0 = No Error Occurred 1 = Error Occurred
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOLTAGE Global Error Log History for VIN_Bulk Over Voltage[4] 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature[4] 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	R04 [3:0]: Reserved

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0 V for VIN_Bulk voltage and 200 ms duration from PWR_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 Host must explicitly perform Erase operation to erase this entire register via command in Table 153, Register 0x39. The PMIC needs minimum of 200 ms for Erase operation.

NOTE 3 PMIC counts the error since last erase operation and if more than one error occurs, it sets this bit to '1'. Host must explicitly perform Erase operation to erase this entire register Table 100, Register 0x04 [7:0].

NOTE 4 PMIC sets the bit when error occurs.

7.2.11 Register Definition (cont'd)

Table 101 — Register 0x05

	R05		
Bits	**Attribute**	**Default**	**Description[1,2]**
7	RV	0	R05 [7]: Reserved
6	ROE	0	R05 [6]: SWA_POWER_GOOD PMIC Power On - SWA Power Not Good[3] 0 = Normal Power On 1 = Power On - SWA Power Not Good
5	RV	0	R05 [5]: Reserved
4	ROE	0	R05 [4]: SWB_POWER_GOOD PMIC Power On - SWB Power Not Good[3] 0 = Normal Power On 1 = Power On - SWB Power Not Good
3	ROE	0	R05 [3]: SWC_POWER_GOOD PMIC Power On - SWC Power Not Good[3] 0 = Normal Power On 1 = Power On - SWC Power Not Good
2:0	ROE	0	R05 [2:0]: PMIC_ERROR_LOG PMIC Power On - High Level Status Bit to Indicate Last Known Power Cycle or System Reset 000 = Normal Power On 001 = Reserved 010 = Buck Regulator Output Over or Under Voltage[4] 011 = Critical Temperature 100 = VIN_Bulk Input Over Voltage 101 = Reserved 110 = Reserved 111 = VIN_Bulk Under Voltage

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0 V for VIN_Bulk voltage and 200 ms duration from PWR_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via Table 153, Register 0x39. The PMIC needs minimum of 200 ms for Erase operation.

NOTE 3 This register is set only if PMIC generates internal VR Disable command due to fault condition.

NOTE 4 This code is a logical OR function of Table 102, Register 0x06 [7:0] register bits.

7.2.11 Register Definition (cont'd)

Table 102 — Register 0x06

	R06		
Bits	**Attribute**	**Default**	**Description[1,2]**
7	ROE	0	R06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWA Under Voltage Lockout 0 = Normal Power On 1 = Power On - SWA Under Voltage Lockout
6	RV	0	R06 [6]: Reserved
5	ROE	0	R06 [5]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWB Under Voltage Lockout[3] 0 = Normal Power On 1 = Power On - SWB Under Voltage Lockout
4	ROE	0	R06 [4]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWC Under Voltage Lockout 0 = Normal Power On 1 = Power On - SWC Under Voltage Lockout
3	ROE	0	R06 [3]: SWA_OVER_VOLTAGE PMIC Power On - SWA Over Voltage 0 = Normal Power On 1 = Power On - SWA Over Voltage
2	RV	0	R06 [2]: Reserved
1	ROE	0	R06 [1]: SWB_OVER_VOLTAGE PMIC Power On - SWB Over Voltage[3] 0 = Normal Power On 1 = Power On - SWB Over Voltage
0	ROE	0	R06 [0]: SWC_OVER_VOLTAGE PMIC Power On - SWC Over Voltage 0 = Normal Power On 1 = Power On - SWC Over Voltage

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0 V for VIN_Bulk voltage and 200 ms duration from PWR_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via Table 153, Register 0x39. The PMIC needs minimum of 200 ms for Erase operation.

NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11 Register Definition (cont'd)

Table 103 — Register 0x07

	R07		
Bits	**Attribute**	**Default**	**Description[1,2]**
7:0	ROE	0	R07 [7:0]: Reserved

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 4.0 V for VIN_Bulk voltage and 200 ms duration from PWR_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via Table 153, Register 0x39. The PMIC needs minimum of 200 ms for Erase operation.

Table 104 — Register 0x08

	R08		
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R08 [7]: Reserved
6	RO	0	R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status[1] 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	R08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status[2] 0 = Power Good 1 = Power Not Good
4	RV	0	R08 [4]: Reserved
3	RO	0	R08 [3]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status[3,4] 0 = Power Good 1 = Power Not Good
2	RO	0	R08 [2]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status[5] 0 = Power Good 1 = Power Not Good
1	RV	0	R08 [1]: Reserved
0	RO	0	R08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_Bulk Input Supply Over Voltage Status[6] 0 = No Over Voltage 1 = Over Voltage

NOTE 1 This register is set when PMIC temperature goes above the threshold setting in register Table 142, Register 0x2E [2:0].

NOTE 2 This register is set when SWA output voltage goes either below the threshold setting in register Table 129, Register 0x21,[0] or above the threshold setting in register Table 130, Register 0x22, [7:6].

NOTE 3 This register is set when SWB output goes either below the threshold setting in register Table 133, Register 0x25,[0] or above the threshold setting in register Table 134, Register 0x26, [7:6].

NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'.

NOTE 5 This register is set when SWC output goes either below the threshold setting in register Table 135, Register 0x27,[0] or above the threshold setting in register Table 136, Register 0x28, [7:6].

NOTE 6 This register is set when VIN_Bulk input voltage goes above the threshold setting in register Table 123, Register 0x1B [7].

7.2.11 Register Definition (cont'd)

Table 105 — Register 0x09

	R09		
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status[1] 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RV	0	R09 [6]: Reserved
5	RO	0	R09 [5]: VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS VOUT_1.8V LDO Output Power Good Status[2] 0 = Power Good 1 = Power Not Good
4	RV	0	R09 [4]: Reserved
3	RO	0	R09 [3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status[3] 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
2	RV	0	R09 [2]: Reserved
1	RO	0	R09 [1]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status[4,5] 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
0	RO	0	R09 [0]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status[6] 0 = No High Current Consumption Warning 1 = High Current Consumption Warning

NOTE 1 This register is set when PMIC temperature goes above the threshold setting in Table 123, Register 0x1B [2:0].
NOTE 2 This register is set when VOUT_1.8V output exceeds the threshold setting in register Table 122, Register 0x1A [2].
NOTE 3 This register is set when SWA output current consumption goes above the threshold setting in Table 124, Register 0x1C [7:0].
NOTE 4 This register is set when SWB output current consumption goes above the threshold setting in Table 126, Register 0x1E [7:0].
NOTE 5 This register is applicable regardless of the setting in Table 173, Register 0x4F [0].
NOTE 6 This register is set when SWC output current consumption goes above the threshold setting in Table 127, Register 0x1F [7:0].

7.2.11 Register Definition (cont'd)

Table 106 — Register 0x0A

	R0A		
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Over Voltage Status[1] 0 = No Over Voltage 1 = Over Voltage
6	RV	0	R0A [6]: Reserved
5	RO	0	R0A [5]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Over Voltage Status[2,3] 0 = No Over Voltage 1 = Over Voltage
4	RO	0	R0A [4]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Over Voltage Status[4] 0 = No Over Voltage 1 = Over Voltage
3	RO	0	R0A [3]: PEC_ERROR_STATUS Packet Error Code Status[5,6] 0 = No PEC Error 1 = PEC Error
2	RO	0	R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status[6,7] 0 = No Parity Error 1 = Parity Error
1	RO	0	R0A [1]: IBI_AND_GLOBAL_STATUS In Band Interrupt and Global Status[8] 0 = No Pending IBI or Outstanding Status 1 = Pending IBI or Outstanding Status
0	RV	0	R0A [0]: Reserved

NOTE 1 This register is set when SWA output voltage goes above the threshold setting in Table 130, Register 0x22, [5:4].
NOTE 2 This register is set when SWB output voltage goes above the threshold setting in Table 134, Register 0x26, [5:4].
NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.
NOTE 4 This register is set when SWC output voltage goes above the threshold setting in Table 136, Register 0x28, [5:4]
NOTE 5 Applicable in I3C Basic Mode Only and if enabled in register Table 148, Register 0x34 [7].
NOTE 6 This register is updated when PMIC device goes through bus reset as described in Section 6.18.13.
NOTE 7 Applicable in I3C Basic Mode and if enabled in register Table 148, Register 0x34 [5]. It is also applicable in I^2C mode for supported CCCs.
NOTE 8 This register can be used as Global Status in addition to IBI status. When IBI function is enabled, this register is automatically cleared when PMIC transmits IBI payload; however individual status registers still requires an explicit clear command from host.

7.2.11 Register Definition (cont'd)

Table 107 — Register 0x0B

	R0B		
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status[1] 0 = No Current Limiter Event 1 = Current Limiter Event
6	RV	0	R0B [6]: Reserved
5	RO	0	R0B [5]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status[2,3] 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	R0B [4]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status[4] 0 = No Current Limiter Event 1 = Current Limiter Event
3	RO	0	R0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Under Voltage Lockout Status[5] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
2	RV	0	R0B [2]: Reserved
1	RO	0	R0B [1]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Under Voltage Lockout Status[6,7] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
0	RO	0	R0B [0]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Under Voltage Lockout Status[8] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout

NOTE 1 This register is set when SWA output valley current goes above the threshold setting in Table 128, Register 0x20 [7:6].
NOTE 2 This register is set when SWB output valley current goes above the threshold setting in Table 128, Register 0x20 [3:2].
NOTE 3 This register is applicable regardless of the setting in Table 173, Register 0x4F [0].
NOTE 4 This register is set when SWC output valley current goes above the threshold setting in Table 128, Register 0x20 [1:0].
NOTE 5 This register is set when SWA output voltage goes below the threshold setting in Table 130, Register 0x22, [3:2].
NOTE 6 This register is set when SWB output voltage goes below the threshold setting in Table 134, Register 0x26, [3:2].
NOTE 7 Only applicable if Table 173, Register 0x4F [0] = '0'.
NOTE 8 This register is set when SWC output voltage goes below the threshold setting in Table 136, Register 0x28, [3:2].

7.2.11 Register Definition (cont'd)

Table 108 — Register 0x0C

	R0C		
Bits	**Attribute**	**Default**	**Description[1]**
7:0	RO	0	R0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT If Table 122, Register 0x1A[1] = '0': Switch Node A Output Current or Output Power[2] Measurement[3] 0000 0000 = Un-defined 0000 0001 = 125[4] or 31.25[5] mA/mW 0000 0010 = 250[4] or 62.5[5] mA/mW 0000 0011 = 375[4] or 93.75[5] mA/mW 0000 0100 = 500[4] or 125[5] mA/mW ... 1111 1111 ≥ 31.875[4] or 7.968[5] A/W If Table 122, Register 0x1A[1] = '1': Sum of SWA, SWB and SWC Output Power[6] 0000 0000 = Undefined 0000 0001 = 125 mW 0000 0010 = 250 mW 0000 0011 = 375 mW 0000 0100 = 500 mW ... 1111 1100 = 31500 mW 1111 1101 = 31625 mW 1111 1110 = 31750 mW 1111 1111 ≥ 31875 mW

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 If Table 123, Register 0x1B [6] = '0', the PMIC reports current measurement. If Table 123, Register 0x1B [6] = '1', the PMIC reports power measurement.

NOTE 3 If Table 173, Register 0x4F [0] = '1', host adds the current or power reported in Table 108, Register 0x0C [7:0] and Table 110, Register 0x0E [7:0] for total current or power consumption.

NOTE 4 If Table 146, Register 0x32 [1:0] = '00'.

NOTE 5 If Table 146, Register 0x32 [1:0] = '01'.

NOTE 6 Register Table 123, Register 0x1B [6] must be configured as '1' and Table 146, Register 0x32 [1:0] must be configured as '00'.

Table 109 — Register 0x0D

	R0D		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	0	R0D [7:0]: SERIAL_NUMBER_BYTE_4 Byte 4 of the unique 40-bit serial number stored in {[R00:R03],R0D} Serial Number is vendor-specific

7.2.11 Register Definition (cont'd)

Table 110 — Register 0x0E

	R0E		
Bits	**Attribute**	**Default**	**Description[1]**
7:0	RO	0	R0E [7:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power[2] Measurement[3] 000000 = Un-defined 0000 0001 = 125[4] or 31.25[5] mA/mW 0000 0010 = 250[4] or 62.5[5] mA/mW 0000 0011 = 375[4] or 93.75[5] mA/mW 0000 0100 = 500[4] or 125[5] mA/mW ... 1111 1111 ≥ 31.875[4] or 7.968[5] A/W

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.
NOTE 2 If Table 123, Register 0x1B [6] = '0', the PMIC reports current measurement. If Table 123, Register 0x1B [6] = '1', the PMIC reports power measurement.
NOTE 3 If Table 173, Register 0x4F [0] = '1', host adds the current or power reported in Table 108, Register 0x0C [7:0] and Table 110, Register 0x0E [7:0] for total current or power consumption.
NOTE 4 If Table 146, Register 0x32 [1:0] = '00'.
NOTE 5 If Table 146, Register 0x32 [1:0] = '01'.

Table 111 — Register 0x0F

	R0F		
Bits	**Attribute**	**Default**	**Description[1]**
7:0	RO	0	R0F [7:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power[2] Measurement 0000 0001 = 125[3] or 31.25[4] mA/mW 0000 0010 = 250[3] or 62.5[4] mA/mW 0000 0011 = 375[3] or 93.75[4] mA/mW 0000 0100 = 500[3] or 125[4] mA/mW ... 1111 1111 ≥ 31.875[3] or 7.968[4] A/W

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.
NOTE 2 If Table 123, Register 0x1B [6] = '0', the PMIC reports current measurement. If Table 123, Register 0x1B [6] = '1', the PMIC reports power measurement.
NOTE 3 If Table 146, Register 0x32 [1:0] = '00'.
NOTE 4 If Table 146, Register 0x32 [1:0] = '01'.

7.2.11 Register Definition (cont'd)

Table 112 — Register 0x10

	R10		
Bits	**Attribute**	**Default**	**Description[1]**
7:6	RV	0	R10 [7:6]: Reserved
5	1O	0	R10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear Register Table 104, Register 0x08 [5][2]
4	RV	0	R10 [4]: Reserved
3	1O	0	R10 [3]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power Good Status.[3] 1 = Clear Register Table 104, Register 0x08 [3][2]
2	1O	0	R10 [2]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear Register Table 104, Register 0x08 [2][2]
1	RV	0	R10 [1]: Reserved
0	1O	0	R10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear VIN_Bulk Input Supply Over Voltage Status. 1 = Clear Register Table 104, Register 0x08 [0][2]

NOTE 1 Table 112, Register 0x10 [5,3:2,0] are self clearing bits.
NOTE 2 See Table 31 and Table 32 for GSI_n and POWER_GOOD output signal status change.
NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11 Register Definition (cont'd)

Table 113 — Register 0x11

	R11		
Bits	**Attribute**	**Default**	**Description**[1]
7	1O	0	R11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status. 1 = Clear Register Table 105, Register 0x09 [7][2]
6	RV	0	R11 [6]: Reserved
5	1O	0	R11 [5]: CLEAR_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.8V Output Power Good Status. 1 = Clear Register Table 105, Register 0x09 [5][2]
4	RV	0	R11 [4]: Reserved
3	1O	0	R11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear Register Table 105, Register 0x09 [3][2]
2	RV	0	R11 [2]: Reserved
1	1O	0	R11 [1]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status.[3] 1 = Clear Register Table 105, Register 0x09 [1][2]
0	1O	0	R11 [0]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. 1 = Clear Register Table 105, Register 0x09 [0][2]

NOTE 1 Table 113, Register 0x11 [7,5,3,1:0] are self clearing bits.
NOTE 2 See Table 31 and Table 32 for GSI_n and POWER_GOOD output signal status change.
NOTE 3 This register is applicable regardless of the setting in Table 173, Register 0x4F [0].

7.2.11 Register Definition (cont'd)

Table 114 — Register 0x12

	R12		
Bits	**Attribute**	**Default**	**Description[1]**
7	1O	0	R12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Over Voltage Status. 1 = Clear Register Table 106, Register 0x0A [7][2]
6	RV	0	R12 [6]: Reserved
5	1O	0	R12 [5]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Over Voltage Status.[3] 1 = Clear Register Table 106, Register 0x0A [5][2]
4	1O	0	R12 [4]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Over Voltage Status. 1 = Clear Register Table 106, Register 0x0A [4][2]
3	1O	0	R12 [3]: CLEAR_PER_ERROR_STATUS Clear PEC Error Status. 1 = Clear Register Table 106, Register 0x0A [3]
2	1O	0	R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear Register Table 106, Register 0x0A [2]
1:0	RV	0	R12 [1:0]: Reserved

NOTE 1 Table 114, Register 0x12 [7,5:2] are self clearing bits.
NOTE 2 See Table 31 and Table 32 for GSI_n and POWER_GOOD output signal status change.
NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11 Register Definition (cont'd)

Table 115 — Register 0x13

	R13		
Bits	**Attribute**	**Default**	**Description[1]**
7	1O	0	R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear Register Table 107, Register 0x0B [7][2]
6	RV	0	R13 [6]: Reserved
5	1O	0	R13 [5]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status.[3] 1 = Clear Register Table 107, Register 0x0B [5][2]
4	1O	0	R13 [4]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. 1 = Clear Register Table 107, Register 0x0B [4][2]
3	1O	0	R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Under Voltage Lockout Status. 1 = Clear Register Table 107, Register 0x0B [3][2]
2	RV	0	R13 [2]: Reserved
1	1O	0	R13 [1]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Under Voltage Lockout Status.[4] 1 = Clear Register Table 107, Register 0x0B [1][2]
0	1O	0	R13 [0]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Under Voltage Lockout Status. 1 = Clear Register Table 107, Register 0x0B [0][2]

NOTE 1 Table 115, Register 0x13 [7,5:3,1:0] are self clearing bits.
NOTE 2 See Table 31 and Table 32 for GSI_n and POWER_GOOD output signal status change.
NOTE 3 This register is applicable regardless of the setting in Table 173, Register 0x4F [0].
NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11 Register Definition (cont'd)

Table 116 — Register 0x14

	R14		
Bits	**Attribute**	**Default**	**Description[1]**
7:4	RV	0	R14 [7:4]: Reserved
3	1O	0	R14 [3]: CLEAR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Clear VIN_Bulk Input Under Voltage Lockout Status 1 = Clear Register Table 147, Register 0x33 [3]
2	1O	0	R14 [2]: CLEAR_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.0V Output Power Good Status. 1 = Clear Register Table 147, Register 0x33 [2][2]
1	RV	0	R14 [1]: Reserved
0	1O	0	R14 [0]: GLOBAL_CLEAR_STATUS Clear all[2] status bits. 1 = Clear all status bits[3]

NOTE 1 Table 116, Register 0x14 [2, 0] are self clearing bits.
NOTE 2 All status bits in register Table 112, Register 0x10 [5,3:2,0], Table 113, Register 0x11 [7,5,3,1:0], Table 114, Register 0x12 [7,5:2], Table 115, Register 0x13 [7,5:3,1:0], and Table 116, Register 0x14 [2].
NOTE 3 See Table 31 and Table 32 for GSI_n and POWER_GOOD output signal status change.

Table 117 — Register 0x15

	R15		
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R15 [7:6]: Reserved
5	RW	1	R15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power Good Status Event. [1] 0 = Do Not Mask SWA Output Power Good Status Event 1 = Mask SWA Output Power Good Status Event
4	RV	0	R15 [4]: Reserved
3	RW	1	R15 [3]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power Good Status Event.[1,2] 0 = Do Not Mask SWB Output Power Good Status Event 1 = Mask SWB Output Power Good Status Event
2	RW	1	R15 [2]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power Good Status Event.[1] 0 = Do Not Mask SWC Output Power Good Status Event 1 = Mask SWC Output Power Good Status Event
1	RV	0	R15 [1]: Reserved
0	RW	0	R15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Over Voltage Status Event.[3] 0 = Do Not Mask VIN_Bulk Input Supply Over Voltage Status Event 1 = Mask VIN_Bulk Input Supply Over Voltage Status Event

NOTE 1 Not assert GSI_n or assert PWR_GOOD output signal.
NOTE 2 Only applicable if Table 173, Register 0x4F [0] = '0'.
NOTE 3 Not assert GSI_n output signal.

7.2.11 Register Definition (cont'd)

Table 118 — Register 0x16

	R16		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event. 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event[1]
6	RV	0	R16 [6]: Reserved
5	RW	1	R16 [5]: MASK_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.8V Output Power Good Status Event. 0 = Do Not Mask 1.8V Output Power Good Status Event 1 = Mask 1.8V Output Power Good Status Event[2]
4	RV	0	R16 [4]: Reserved
3	RW	0	R16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node A High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Consumption Warning Status Event 1 = Mask Switch Node A Output Current Consumption Warning Status Event[1]
2	RV	0	R16 [2]: Reserved
1	RW	0	R16 [1]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node B High Output Current Consumption Warning Status Event. [3] 0 = Do Not Mask Switch Node B Output Current Consumption Warning Status Event 1 = Mask Switch Node B Output Current Consumption Warning Status Event[1]
0	RW	0	R16 [0]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask Switch Node C High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Consumption Warning Status Event 1 = Mask Switch Node C Output Current Consumption Warning Status Event[1]

NOTE 1 Not assert GSI_n output signal.
NOTE 2 Not assert GSI_n or assert PWR_GOOD output signal.
NOTE 3 This register is applicable regardless of the setting in Table 173, Register 0x4F [0].

7.2.11 Register Definition (cont'd)

Table 119 — Register 0x17

	R17		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node A Output Over Voltage Status Event. 0 = Do Not Mask Switch Node A Output Over Voltage Status Event 1 = Mask Switch Node A Output Over Voltage Status Event[1]
6	RV	0	R17 [6]: Reserved
5	RW	0	R17 [5]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node B Output Over Voltage Status Event.[2] 0 = Do Not Mask Switch Node B Output Over Voltage Status Event 1 = Mask Switch Node B Output Over Voltage Status Event[1]
4	RW	0	R17 [4]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node C Output Over Voltage Status Event. 0 = Do Not Mask Switch Node C Output Over Voltage Status Event 1 = Mask Switch Node C Output Over Voltage Status Event[1]
3	RW	0	R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only[3] 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only[4] 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status
1:0	RV	0	R17 [1:0]: Reserved

NOTE 1 Not assert GSI_n output signal.
NOTE 2 Only applicable if Table 173, Register 0x4F [0] = '0'.
NOTE 3 Only applicable when PMIC is in I3C Basic Mode. This Mask register only masks the GSI_n output. Does not apply to IBI.
NOTE 4 Applicable when PMIC is in I3C Basic Mode or for supported CCC in I^2C mode. This Mask register only masks the GSI_n output. Does not apply to IBI.

7.2.11 Register Definition (cont'd)

Table 120 — Register 0x18

	R18		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node A Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Limiter Warning Status Event 1 = Mask Switch Node A Output Current Limiter Warning Status Event[1]
6	RV	0	R18 [6]: Reserved
5	RW	0	R18 [5]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node B Output Current Limiter Warning Status Event.[2] 0 = Do Not Mask Switch Node B Output Current Limiter Warning Status Event 1 = Mask Switch Node B Output Current Limiter Warning Status Event[1]
4	RW	0	R18 [4]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node C Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Limiter Warning Status Event 1 = Mask Switch Node C Output Current Limiter Warning Status Event[1]
3	RW	0	R18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node A Output Under Voltage Lockout Status Event. 0 = Do Not Mask Switch Node A Output Under Voltage Lockout Status Event 1 = Mask Switch Node A Output Under Voltage Lockout Status Event[1]
2	RV	0	R18 [2]: Reserved
1	RW	0	R18 [1]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node B Output Under Voltage Lockout Status Event.[3] 0 = Do Not Mask Switch Node B Output Under Voltage Lockout Status Event 1 = Mask Switch Node B Output Under Voltage Lockout Status Event[1]
0	RW	0	R18 [0]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node C Output Under Voltage Lockout Status Event. 0 = Do Not Mask Switch Node C Output Under Voltage Lockout Status Event 1 = Mask Switch Node C Output Under Voltage Lockout Status Event[1]

NOTE 1 Not assert GSI_n output signal.
NOTE 2 This register is applicable regardless of the setting in Table 173, Register 0x4F [0].
NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11 Register Definition (cont'd)

Table 121 — Register 0x19

	R19		
Bits	**Attribute**	**Default**	**Description**
7:4	RV	0	R19 [7:4]: Reserved
3	RW	0	R19 [3]: MASK_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Mask VIN_Bulk Input Under Voltage Lockout Event 0 = Do Not Mask VIN_Bulk Input Under Voltage Lockout 1 = Mask VIN_Bulk Input Under Voltage Lockout[1]
2	RW	1	R19 [2]: MASK_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.0V Output Power Good Status Event. 0 = Do Not Mask 1.0V Output Power Good Status Event 1 = Mask 1.0V Output Power Good Status Event[2]
1:0	RV	0	R19 [1:0]: Reserved

NOTE 1 Not assert GSI_n output signal.
NOTE 2 Not assert GSI_n or POWER_GOOD output signal.

7.2.11.1 Threshold Registers

Table 122 — Register 0x1A

	R1A		
Bits	**Attribute**	**Default**	**Description**
7:5	RV	0	R1A [7:5]: Reserved
4	RW	0	R1A [4]: QUIESCENT_STATE_EN PMIC Quiescent State Entry Enable[1] 0 = Disable 1 = Enable[2,3]
3	RW	0	R1A [3]: Reserved
2	RW	0	R1A [2]: VOUT_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6 V 1 = Reserved
1	RW	0	R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select[4] 0 = Report individual power for each rail in R0C, R0E and R0F 1 = Report total power of each rail in R0C[5]
0	RW	0	R1A [0]: VOUT_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = -10% from the setting in Table 139, Register 0x2B, [2:1] 1 = -15% from the setting in Table 139, Register 0x2B, [2:1]

NOTE 1 This bit must be configured before issuing VR Enable command.

NOTE 2 VR Disable command (VR_EN pin transition to low or Table 146, Register 0x32 [7] = '0' (in programmable mode only)) puts PMIC in Quiescent state.

NOTE 3 Simultaneous usage of programmable mode (i.e., Table 143, Register 0x2F [2] = '1'), PWR_GOOD as IO (i.e., Table 146, Register 0x32 [5] = '1') and P1 State Enable (i.e., Table 122, Register 0x1A [4] = '1') is considered an illegal configuration when VR_EN pin is intended to be used; otherwise it is a valid configuration if VR_EN command is used on I^2C/I3C Basic bus.

NOTE 4 This register is only applicable if Table 123, Register 0x1B [6] = '1'.

NOTE 5 Host should only read Table 108, Register 0x0C [7:0] for total power. The register contents of Table 110, Register 0x0E and Table 111, Register 0x0F may not be valid.

7.2.11.1 Threshold Registers (cont'd)

Table 123 — Register 0x1B

	R1B		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_Bulk Input Over Voltage Threshold Setting For GSI_n Assertion 0 = 5.8 V to 6 V (Varies across vendors) 1 = Reserved
6	RW	0	R1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers:[1] 1 = Report Power Measurements in registers[1]
5	RV	0	R1B [5]: Reserved
4	RW	0	R1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin[2] 0 = Not Masked 1 = Masked
3	RW	0	R1B [3]: GSI_N_PIN_ENABLE Enable GSI_n Pin[3] 0 = Disable GSI_n Pin 1 = Enable GSI_n Pin
2:0	RW	101	R1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold[4] 000 = Reserved 001 = PMIC temperature ≥ 85 °C 010 = PMIC temperature ≥ 95 °C 011 = PMIC temperature ≥ 105 °C 100 = PMIC temperature ≥ 115 °C 101 = PMIC temperature ≥ 125 °C 110 = PMIC temperature ≥ 135 °C 111 = Reserved

NOTE 1 Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0], Table 111, Register 0x0F[7:0].

NOTE 2 Mask POWER_GOOD output signal for all appropriate register bits in Table 117, Register 0x15 [5,3:2,0], Table 118, Register 0x16 [7,5,3,1:0], Table 119, Register 0x17 [7,5:4], Table 120, Register 0x18 [7,5:3,1:0] and Table 121, Register 0x19 [3:2]. Mask Register Control Table 143, Register 0x2F [1:0] still applies when Global PWR_GOOD output Mask register is set to '1'.

NOTE 3 This register can be used as Global Mask Function for GSI_n pin. If disabled, this masks GSI_n output signal for all register bits in Table 117, Register 0x15 [5,3,2:0], Table 118, Register 0x16 [7,5,3,1:0], Table 119, Register 0x17 [7,5:4], Table 120, Register 0x18 [7,5:3,1:0] and Table 121, Register 0x19 [3:2].

NOTE 4 The tolerance of the temperature warning threshold is ± 5 °C from the selected setting.

7.2.11.1 Threshold Registers (cont'd)

Table 124 — Register 0x1C

	R1C		
Bits	**Attribute**	**Default**	**Description**
7:0	RW	00110000	R1C [7:0]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold[1] If Table 146, Register 0x32 [1:0] = '01': 0000 0000 = Undefined 0000 0001 = 31.25 mA 0000 0010 = 62.5 mA 0000 0011 = 93.75 mA 0000 0100 = 125 mA ... 1100 0000 = 6.0 A ... 1111 1111 = 7.968 A If Table 146, Register 0x32 [1:0] = '00': 0000 0000 = Undefined 0000 0001 = 0.125 A 0000 0010 = 0.250 A ... 0011 0000 = 6.0 A (Default) ... 1111 1111 = 31.875 A

NOTE 1 The default value is set based on Table 146, Register 0x32 [1:0] = '00'

Table 125 — Register 0x1D

	R1D		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R1D [7:0]: Reserved

7.2.11.1 Threshold Registers (cont'd)

Table 126 — Register 0x1E

	R1E		
Bits	**Attribute**	**Default**	**Description**
7:0	RW	00110000	R1E [7:0]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_ THRESHOLD Switch Node B Output High Current Consumption Warning Threshold[12] If Table 146, Register 0x32 [1:0] = '01': 0000 0000 = Undefined 0000 0001 = 31.25 mA 0000 0010 = 62.5 mA 0000 0011 = 93.75 mA 0000 0100 = 125 mA ... 1100 0000 = 6.0 A ... 1111 1111 = 7.968 A If Table 146, Register 0x32 [1:0] = '00': 0000 0000 = Undefined 0000 0001 = 0.125 A 0000 0010 = 0.250 A ... 0011 0000 = 6.0 A (Default) ... 1111 1111 = 31.875 A

NOTE 1 This register is applicable regardless of the setting in Table 173, Register 0x4F [0]. For dual phase operation, this register should be configured identically as Table 124, Register 0x1C [7:0].

NOTE 2 The default value is set based on Table 146, Register 0x32 [1:0] = '00'

7.2.11.1 Threshold Registers (cont'd)

Table 127 — Register 0x1F

	R1F		
Bits	**Attribute**	**Default**	**Description**
7:0	RW	00010000	R1F [7:0]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_ WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold[1] If Table 146, Register 0x32 [1:0] = '01': 0000 0000 = Undefined 0000 0001 = 31.25 mA 0000 0010 = 62.5 mA 0000 0011 = 93.75 mA 0000 0100 = 125 mA ... 0100 0000 = 2.0 A ... 1111 1111 = 7.968 A If Table 146, Register 0x32 [1:0] = '00': 0000 0000 = Undefined 0000 0001 = 0.125 A 0000 0010 = 0.250 A ... 0001 0000 = 2.0 A (Default) ... 1111 1111 = 31.875 A

NOTE 1 The default value is set based on Table 146, Register 0x32 [1:0] = '00'

7.2.11.1 Threshold Registers (cont'd)

Table 128 — Register 0x20[1]

	R20		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 4.5 A 01 = 5.5 A 10 = 6.5 A 11 = Vendor-Specific
5:4	RV	0	R20 [5:4]: Reserved
3:2	RW	01	R20 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit[2] 00 = 4.5 A 01 = 5.5 A 10 = 6.5 A 11 = Vendor-Specific
1:0	RW	0	R20 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit: 00 = 1.5 A 01 = 2.0 A 10 = Reserved 11 = Vendor-Specific

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 174, Register 0x50.

NOTE 2 This register is applicable regardless of the setting in Table 173, Register 0x4F[0]. For dual phase operation, this register should be configured identically as Table 128, Register 0x20 [7:6].

7.2.11.1 Threshold Registers (cont'd)

Table 129 — Register 0x21[1,2]

	R21		
Bits	**Attribute**	**Default**	**Description**
7:1	RW	011 1100	R21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting[3,4] 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RW	0	R21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 129, Register 0x21, [7:1] 1 = -7.5% from the setting in Table 129, Register 0x21, [7:1]

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 163, Register 0x45.

NOTE 2 If required, the host must update the settings in register Table 129, Register 0x21, [0], Table 130, Register 0x22, [7:2] and Table 128, Register 0x20 [7:6] first prior to updating the settings in the register Table 129, Register 0x21, [7:1].

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050 mV to 1160 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWA output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 µs for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 µs before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there is any abnormal issues that triggers VR Disable command as described in Table 30. Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when Table 146, Register 0x32 [5] = '1'.

7.2.11.1 Threshold Registers (cont'd)

Table 130 — Register 0x22[1,2]

	R22		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 129, Register 0x21, [7:1] 01 = +7.5% from the setting in Table 129, Register 0x21, [7:1] 10 = +10% from the setting in Table 129, Register 0x21, [7:1] 11 = Reserved
5:4	RW	10	R22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over Voltage Status[3] 00 = +7.5% from the setting in Table 129, Register 0x21, [7:1] 01 = +10% from the setting in Table 129, Register 0x21, [7:1] 10 =+12.5% from the setting in Table 129, Register 0x21, [7:1] 11 = Reserved
3:2	RW	00	R22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 129, Register 0x21, [7:1] 01 = -12.5% from the setting in Table 129, Register 0x21, [7:1] 10 = Reserved 11 = Reserved
1:0	RW	11	R22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft Stop Time After VR Disable[4 5] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms (Default)

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 164, Register 0x46.

NOTE 2 If required, the host must update the setting in register Table 129, Register 0x21, [0], Table 130, Register 0x22, [7:2] and Table 128, Register 0x20 [7:6] first prior to updating the settings in the register Table 129, Register 0x21, [7:1].

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in Table 130, Register 0x22,[7:6].

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

NOTE 5 There is an extension to the SWA Soft Stop time in Table 150, Register 0x36 [7].

Table 131 — Register 0x23

	R23		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R23 [7:0]: Reserved

7.2.11.1 Threshold Registers (cont'd)

Table 132 — Register 0x24[1]

	R24		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R24 [7:0]: Reserved

NOTE 1 Only applicable if Table 173, Register 0x4F [0] = '0'.

Table 133 — Register 0x25[1,2]

	R25		
Bits	**Attribute**	**Default**	**Description**
7:1	RW	011 1100	R25 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting[3,4 5] 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RW	0	R25 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 133, Register 0x25, [7:1] 1 = -7.5% from the setting in Table 133, Register 0x25, [7:1]

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 167, Register 0x49.

NOTE 2 If required, the host must update the settings in register Table 133, Register 0x25, [0], Table 134, Register 0x26, [7:2] and Table 128, Register 0x20 [3:2] first prior to updating the settings in the register Table 133, Register 0x25, [7:1].

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050 mV to 1160 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWB output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 µs for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 µs before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there is any abnormal issues that triggers VR Disable command as described in Table 30. Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when Table 146, Register 0x32 [5] = '1'.

NOTE 5 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11.1 Threshold Registers (cont'd)

Table 134 — Register 0x26[1,2]

	R26		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R26 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 133, Register 0x25, [7:1] 01 = +7.5% from the setting in Table 133, Register 0x25, [7:1] 10 = +10% from the setting in Table 133, Register 0x25, [7:1] 11 = Reserved
5:4	RW	10	R26 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over Voltage Status[3] 00 = +7.5% from the setting in Table 133, Register 0x25, [7:1] 01 = +10% from the setting in Table 133, Register 0x25, [7:1] 10 =+12.5% from the setting in Table 133, Register 0x25, [7:1] 11 = Reserved
3:2	RW	00	R26 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 133, Register 0x25, [7:1] 01 = -12.5% from the setting in Table 133, Register 0x25, [7:1] 10 = Reserved 11 = Reserved
1:0	RW	11	R26 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft Stop Time After VR Disable[4 5] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms (Default)

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 168, Register 0x4A.

NOTE 2 If required, the host must update the settings in register Table 133, Register 0x25, [0], Table 134, Register 0x26, [7:2] and Table 128, Register 0x20 [3:2] first prior to updating the settings in the register Table 133, Register 0x25, [7:1].

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in Table 134, Register 0x26,[7:6].

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

NOTE 5 There is an extension to the SWB Soft Stop time in Table 150, Register 0x36 [5].

7.2.11.1 Threshold Registers (cont'd)

Table 135 — Register 0x27[1,2]

	R27		
Bits	**Attribute**	**Default**	**Description**
7:1	RW	011 1100	R27 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting[3,4] 000 0000 = 1500 mV 000 0001 = 1505 mV 000 0010 = 1510 mV ... 011 1100 = 1800 mV ... 111 1101 = 2125 mV 111 1110 = 2130 mV 111 1111 = 2135 mV
0	RW	0	R27 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 135, Register 0x27, [7:1] 1 = -7.5% from the setting in Table 135, Register 0x27, [7:1]

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 169, Register 0x4B.

NOTE 2 If required, the host must update the settings in register Table 135, Register 0x27, [0], Table 136, Register 0x28, [7:2] and Table 128, Register 0x20 [1:0] first prior to updating the settings in the register Table 135, Register 0x27, [7:1].

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1750 mV to 1850 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWC output voltage setting by 5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5 µs for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50 µs before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR_GOOD output signal if there is any abnormal issues that triggers VR Disable command as described in Table 30. Further, PMIC does monitor PWR_GOOD input signal and executes power off config sequence registers if it is registered low when Table 146, Register 0x32 [5] = '1'.

7.2.11.1 Threshold Registers (cont'd)

Table 136 — Register 0x28[1,2]

	R28		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R28 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 135, Register 0x27, [7:1] 01 = +7.5% from the setting in Table 135, Register 0x27, [7:1] 10 = +10% from the setting in Table 135, Register 0x27, [7:1] 11 = Reserved
5:4	RW	10	R28 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over Voltage Status[3] 00 = +7.5% from the setting in Table 135, Register 0x27, [7:1] 01 = +10% from the setting in Table 135, Register 0x27, [7:1] 10 = +12.5% from the setting in Table 135, Register 0x27, [7:1] 11 = Reserved
3:2	RW	00	R28 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 135, Register 0x27, [7:1] 01 = -12.5% from the setting in Table 135, Register 0x27, [7:1] 10 = Reserved 11 = Reserved
1:0	RW	11	R28 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft Stop Time After VR Disable[4 5] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 8 ms (Default)

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 170, Register 0x4C.

NOTE 2 If required, the host must update the settings in register Table 135, Register 0x27, [0], Table 136, Register 0x28, [7:2] and Table 128, Register 0x20 [1:0] first prior to updating the settings in the register Table 135, Register 0x27, [7:1].

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in Table 136, Register 0x28,[7:6].

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

NOTE 5 There is an extension to the SWC Soft Stop time in Table 150, Register 0x36 [4].

7.2.11.1 Threshold Registers (cont'd)

Table 137 — Register 0x29[1,2]

	R29		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R29 [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R29 [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific
3:0	RV	0	R29 [3:0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 171, Register 0x4D.

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in Table 146, Register 0x32 [7].

7.2.11.1 Threshold Registers (cont'd)

Table 138 — Register 0x2A[1,2]

	R2A		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R2A [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection[3] 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R2A [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency[3] 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific
3:2	RW	10	R2A [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	01	R2A [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 172, Register 0x4E.

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in Table 146, Register 0x32 [7].

NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

7.2.11.1 Threshold Registers (cont'd)

Table 139 — Register 0x2B[1,2]

	R2B		
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R2B [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting[3] 00 = 1.7 V 01 = 1.8 V 10 = 1.9 V 11 = 2.0 V
5:3	RV	0	R2B [5:3]: Reserved
2:1	RW	01	R2B [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting[4] 00 = 0.9 V 01 = 1.0 V 10 = 1.1 V 11 = 1.2 V
0	RV	0	R2B [0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 175, Register 0x51.

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in Table 146, Register 0x32 [7]. The host must also wait minimum of 5 µs after the adjustment before issuing VR Enable command.

NOTE 3 The VOUT_1.8V Power Good threshold in register Table 122, Register 0x1A [2] is always fixed regardless of the setting in this register.

NOTE 4 If required, the host must adjust this register one step at a time (0.1 V increment or decrement) to prevent false trigger of power good status and PWR_GOOD pin assertion. In other words, host should not increment or decrement 0.2 V or 0.3 V from its current setting.

Table 140 — Register 0x2C[1,2]

	R2C		
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft Start Time After VR Enable[3] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4:0	RV	0	R2C [4:0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 180, Register 0x5D.

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in Table 146, Register 0x32 [7].

NOTE 3 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

7.2.11.1 Threshold Registers (cont'd)

Table 141 — Register 0x2D[1,2]

	R2D		
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2D [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft Start Time After VR Enable[3,4] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4	RV	0	R2D [4]: Reserved
3:1	RW	001	R2D [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft Start Time After VR Enable[3] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
0	RV	0	R2D [0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as Table 181, Register 0x5E.

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in Table 146, Register 0x32 [7].

NOTE 3 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage)

NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'.

Table 142 — Register 0x2E

	R2E		
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R2E [7:3]: Reserved
2:0	RW	100	R2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature ≥ 105 °C 001 = PMIC Temperature ≥ 115 °C 010 = PMIC Temperature ≥ 125 °C 011 = PMIC Temperature ≥ 135 °C 100 = PMIC Temperature ≥ 145 °C 101 = Reserved 110 = Reserved 111 = Reserved

7.2.11.1 Threshold Registers (cont'd)

Table 143 — Register 0x2F

	R2F		
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R2F [7]: Reserved
6	RW	0	R2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output[1,2] 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R2F [5]: Reserved
4	RW	0	R2F [4]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output[1,2,3] 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RW	0	R2F [3]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output[1,2] 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2	RW	0	R2F [2]: SECURE_MODE PMIC Mode Operation 0 = Secure Mode Operation[4,5] 1 = Programmable Mode Operation
1:0	RW	10	R2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control[6] 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Signal Only (GSI_n Signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved

NOTE 1 This bit must be used only after power up sequence (after VR Enable command). At first power up, PMIC automatically updates the status of this register to '1' after VR Enable command. When VR Enable command is registered, the PMIC updates this register based on Power On Sequence Configuration (0 to 2) setting. If enabled in Power On Sequence Configuration 0 to 2 registers, only then, under programmable mode of operation, the PMIC's output regulator can be disabled by clearing this bit and they can be reenabled again by setting this bit. The PMIC does not alter its Power Good output signal and keeps it asserted High. If any regulator is not enabled in Power on Sequence Configuration 0 to 2, it cannot be enabled using this register. For example, if only SWA is enabled and SWB and SWC is not enabled in Table 158, Register 0x40 [7:0] to Table 160, Register 0x42, [7:0] then only SWA can be disabled and then re-enabled again but SWB and SWC cannot be enabled using Table 143, Register 0x2F [6,4:3].

NOTE 2 In programmable mode, after VR enable command, if any output regulators are disabled by clearing Table 143, Register 0x2F [6,4:3] and then if host issues VR Disable command or PMIC internally triggers VR Disable command, the PMIC keeps the disabled output regulator in Table 143, Register 0x2F [6,4:3] off and remaining output regulators are disabled by following the Power Off Sequence Configuration 0 to 2 settings.

NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

NOTE 4 This bit must be configured before issuing VR Enable command. If this bit is configured to '0', when PMIC registers VR Enable command, all registers bits starting Table 117, Register 0x15 to Table 143, Register 0x2F, Table 146, Register 0x32 [7,5:0], Table 149, Register 0x35, and Table 150, Register 0x36 in the host region as well as Table 158, Register 0x40 to Register 0x6F in the DIMM vendor region and Register 0x70 to Register 0xFF in the PMIC vendor region are secured and the host cannot change unless the PMIC goes through power cycle.

NOTE 5 Simultaneous usage of programmable mode (i.e., Table 143, Register 0x2F [2] = '1'), PWR_GOOD as IO (i.e., Table 146, Register 0x32 [5] = '1') and P1 State Enable (i.e., Table 122, Register 0x1A [4] = '1') is considered an illegal configuration when VR_EN pin is intended to be used; otherwise it is a valid configuration if VR_EN command is used on I^2C/I3C Basic bus.

NOTE 6 Applies to Mask Registers Table 117, Register 0x15 [5,3:2,0], Table 118, Register 0x16 [7,5,3,1:0], Table 119, Register 0x17 [7,5:2], Table 120, Register 0x18 [7,5:3,1:0], Table 121, Register 0x19 [2] when any one or more Mask registers are set to '1'. If all Mask registers are configured as '0', the setting in this register (Table 143, Register 0x2F [1:0]) does not matter.

Table 144 — Register 0x30

	R30		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable[1] 1 = Enable
6:3	RW	0	R30 [6:3]: ADC_SELECT Input Selection for ADC Readout[2] 0000 = SWA Output Voltage 0001 = Reserved 0010 = SWB Output Voltage[3] 0011 = SWC Output Voltage 0100 = Reserved 0101 = VIN_Bulk Input Voltage 0110 = Reserved 0111 = Reserved 1000 = VOUT_1.8V Output Voltage 1001 = VOUT_1.0V Output Voltage All other encodings are reserved.
2	RV	0	R30 [2]: Reserved
1:0	RW	0	R30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency[4,5] 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms

NOTE 1 Disables the ADC function completely. Applies to voltage readout in Table 145, Register 0x31 [7:0] as well as current or power readout in Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0] and Table 111, Register 0x0F [7:0]. Does not apply to thermal sensor temperature readout in Table 147, Register 0x33 [7:5] as well as high temperature warning and critical temperature shutdown.

NOTE 2 The host shall wait minimum of 9 ms delay after the input selection for ADC readout and the actual readout from Table 145, Register 0x31 to get the latest reading.

NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'.

NOTE 4 For average output current or power measurement in registers Table 108, Register 0x0C [7:0], Table 110, Register 0x0E [7:0] and Table 111, Register 0x0F [7:0].

NOTE 5 This register represents how often the registers are updated. The internal sampling rate is vendor specific.

7.2.11.1 Threshold Registers (cont'd)

Table 145 — Register 0x31

	R31		
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R31 [7:0]: ADC_READ ADC Output Voltage Reading[1](Applies to SW[A:C], VOUT_1.8V, VOUT_1.0V) 0000 0000 = Undefined 0000 0001 = 15 mV 0000 0010 = 30 mV ... 1111 1111 ≥ 3825 mV ADC Output Voltage Reading[2] (Applies to VIN_Bulk Input Voltage) 0000 0000 = Undefined 0000 0001 = 70 mV 0000 0010 = 140 mV ... 1111 1111 ≥ 17850 mV

NOTE 1 Only valid when Table 144, Register 0x30 [6:3] = '0000' or '0010' or '0011' or '0110' or '1000' or '1001'.
NOTE 2 Only valid when Table 144, Register 0x30 [6:3] = '0101'.

7.2.11.1 Threshold Registers (cont'd)

Table 146 — Register 0x32

	R32		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R32 [7]: VR_ENABLE PMIC Enable[1,2,3,4] 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection[5] 0 = I2C Protocol (Max speed 1 MHz) 1 = I3C Basic Protocol
5	RW	0	R32 [5]: PWR_GOOD_IO_TYPE PMIC PWR_GOOD Output Signal Type[6] 0 = Output Only 1 = Input and Output[7]
4:3	RW	0	R32 [4:3]: PWR_GOOD_OUTPUT_SIGNAL_CONTROL PMIC PWR_GOOD Output Signal Control 0x = PMIC controls PWR_GOOD on its own based on internal status 10 = PWR_GOOD Output Low 11 = PWR_GOOD Output Floats[8]
2	RV	0	R32 [2]: Reserved
1:0	RW	00	R32 [1:0]: ADC_ACCURACY_STEP_SIZE ADC Accuracy Step Size 00 = 125 mA or 125 mW 01 = 31.25 mA or 31.25 mW All other encodings are reserved

NOTE 1 The PMIC updates this bit when VR_EN signal transition to high or when host issues VR Enable command over I2C/I3C Basic bus; whichever comes first. PMIC also updates this bit when VR_EN signal transitions to low or when host issues VR Disable command over I2C/I3C Basic bus in programmable mode; whichever comes first. Further, PMIC updates this bit when PWR_GOOD input is low (if Table 146, Register 0x32 [5] = '1') or when PMIC internally generates VR Disable command due to fault condition regardless of PMIC's VR_EN signal input status.

NOTE 2 After this bit is set to '1', the PMIC executes Power On Sequence configuration 0 (Table 158, Register 0x40) to Power On Sequence configuration 2 (Table 160, Register 0x42,) registers. At least one bit in Table 158, Register 0x40 [6,4:3] must be set to '1' to issue VR Enable (either with VR_EN pin or over I2C/I3C Basic bus) command.

NOTE 3 The host shall ensure that prior to issuing VR Enable command, there is no pending IBI interrupt (i.e., Table 106, Register 0x0A [1] = '1'). After host issues VR Enable command (either with VR_EN pin or over I2C/I3C Basic bus), the PMIC may NACK any I2C or I3C Basic bus transactions by host until tPMIC_PWR_GOOD_OUT timing parameter is satisfied. The host shall not access any device specific registers or issue CCCs until tPMIC_PWR_-GOOD_Out parameter is satisfied. The PMIC device may request for an IBI during power up sequence (i.e., during tPMIC_PWR_GOOD_Out time) if there is any event.

NOTE 4 An exception to this register is applied. When PMIC is operating in secure mode of operation and PWR_GOOD input is low (if Table 146, Register 0x32 [5] = '1'), the PMIC unlocks this register. The PMIC allows host to issue VR Enable command. After host issues VR Enable command, the PMIC re-locks this register.

NOTE 5 This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in Section 6.18.13 regardless of whether PMIC is in secure mode or programmable mode of operation. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I2C mode or I3C Basic mode of operation. When this register is updated, it takes in effect when there is a next START operation (i.e., after STOP operation).

NOTE 6 This bit must be configured before issuing VR Enable command.

NOTE 7 Simultaneous usage of programmable mode (i.e., Table 143, Register 0x2F [2] = '1'), PWR_GOOD as IO (i.e., Table 146, Register 0x32 [5] = '1') and P1 State Enable (i.e., Table 122, Register 0x1A [4] = '1') is considered an illegal configuration when VR_EN pin is intended to be used; otherwise it is a valid configuration if VR_EN command is used on I^2C/I3C Basic bus.

NOTE 8 When this encoding is set, the PMIC always floats the PWR_GOOD output signal even when there is an internal VR Disable command due to fault condition.

Table 147 — Register 0x33

	R33		
Bits	**Attribute**	**Default**	**Description**
7:5	RO	0	R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature[1] 000 = ≤ 85 °C 001 = 85 °C 010 = 95 °C 011 = 105 °C 100 = 115 °C 101 = 125 °C 110 = 135 °C 111 = ≥ 140 °C
4	RV	0	R33 [4]: Reserved
3	RO	0	R33 [3]: VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS VIN_Bulk Under Voltage Lockout Status[2] 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
2	RO	0	R33 [2]: VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS VOUT_1.0V LDO Output Power Good Status[3] 0 = Power Good 1 = Power Not Good
1:0	RV	0	R33 [1:0]: Reserved

NOTE 1 The accuracy of the temperature readout code is ± 5 °C.

NOTE 2 This register is set when VIN_Bulk input voltage goes below a vendor specific threshold.

NOTE 3 This register is set when VOUT_1.0V output drops below the threshold setting in register Table 122, Register 0x1A [0].

7.2.11.1 Threshold Registers (cont'd)

Table 148 — Register 0x34

	R34		
Bits	**Attribute**	**Default**	**Description[1]**
7	RO	0	R34 [7]: PEC_ENABLE Packet Error Code Enable[2] (Applicable Only if Table 146, Register 0x32 [6] = '1') 0 = Disable 1 = Enable
6	RO	0	R34 [6]: IBI_ENABLE In Band Interrupt Enable[3] (Applicable Only if Table 146, Register 0x32 [6] = '1') 0 = Disable 1 = Enable
5	RO	0	R34 [5]: PARITY_DISABLE T Bit Parity Code Disable[2] (Applicable Only if Table 146, Register 0x32[6] = '1'.) 0 = Enable 1 = Disable[4]
4	RV	0	R34 [4]: Reserved
3:1	RO	111	R34 [3:1]: HID_CODE PMIC's 3-bit HID Code[5] 000 001 010 011 100 101 110 111
0	RV	0	R34 [0]: Reserved

NOTE 1 The write (or update) transaction to this register must be followed by STOP operation to allow the PMIC device to update the setting.

NOTE 2 This register is automatically updated when RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in Section 6.18.13. This register cannot be written by the Host through normal write operation either in I^2C mode or I3C mode of operation. This register is updated with DEVCTRL CCC with RegMod='0' only. This register cannot be written with DEVCTRL CCC with RegMod = '1'.

NOTE 3 This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in Section 6.18.13. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I^2C mode or I3C mode of operation. This register cannot be written with DEVCTRL CCC with RegMod = '1'.

NOTE 4 When Parity function is disabled, the PMIC simply ignores the "T" bit information from the Host. The host may actually choose to compute the parity and send that information in "T" bit or simply drive static low or high in "T" bit.

NOTE 5 This register is updated when PMIC device receives SETHID CCC or when PMIC device goes through bus reset as described in Section 6.18.13. This register cannot be written with DEVCTRL CCC with RegMod = '1'.

7.2.11.2 Error Injection Registers

Table 149 — Register 0x35

	R35		
Bits	**Attribute**	**Default**	**Description[1,2]**
7	RW	0	R35 [7]: ERROR_INJECTION_ENABLE Error Injection Enable[3] 0 = Disable 1 = Enable
6:4	RW	0	R35 [6:4]: ERROR_INJECTION_RAIL_SELECTION Error Injection - Input Rail and Output Rail Selection[4,5] 000 = Undefined 001 = SWA Output Only 010 = Reserved 011 = SWB Output Only 100 = SWC Output Only 101 = VIN_Bulk Input Only 110 = Reserved 111 = Do Not Use
3	RW	0	R35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT Over Voltage or Under Voltage Selection for Bits [6:4][6] 0 = Over Voltage 1 = Under Voltage[7]
2:0	RW	0	R35[2:0]: MISC_ERROR_INJECTION_TYPE Miscellaneous Error Injection Type[8] 000 = Undefined 001 = Reserved 010 = Critical Temperature Shutdown 011 = High Temperature Warning Threshold 100 = VOUT_1.8V LDO Power Good 101 = High Current Consumption Warning[9] 110 = Reserved 111 = Current Limiter Warning[9]

NOTE 1 Refer to Section 6.13 for error function usage model. The host can erase the error log registers (Table 100, Register 0x04 to Table 103, Register 0x07) by writing 0x74 to Table 153, Register 0x39.

NOTE 2 To exit from Error Injection Mode, the PMIC must go through power cycle of both VIN_Bulk input supply.

NOTE 3 When error injection function is invoked by setting bit [7] = '1', the setting of bits [6:4, 2:0] = '000 000' is considered an illegal setting.

NOTE 4 This register Table 149, Register 0x35 [6:4] is only applicable if Table 149, Register 0x35 [2:0] is '000'. Any value other than '000' in both Table 149, Register 0x35 [6:4] and Table 149, Register 0x35 [2:0] is considered an illegal setting and PMIC operation is not guaranteed.

NOTE 5 If dual phase regulator is selected, use SWA encoding to inject the error. Register bit [3] selects either over voltage or under voltage condition for the setting selected in this register.

NOTE 6 This register Table 149, Register 0x35 [3] is only applicable if bits [6:4] is anything other than '000'.

NOTE 7 The under voltage selection only applies to SWx output rails and VIN_Bulk input.

NOTE 8 This register Table 149, Register 0x35 [2:0] is only applicable if Table 149, Register 0x35 [6:3] is '0000'. Any value other than '000' in both Table 149, Register 0x35 [6:4] and Table 149, Register 0x35 [2:0] is considered an illegal setting and PMIC operation is not guaranteed.

NOTE 9 Applies to all enabled SWx output regulators at the same time.

7.2.11.2 Error Injection Registers (cont'd)

Table 150 — Register 0x36

	R36		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R36 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION SWA Output Regulator Soft Stop Time After VR Disable[1] [2] 3-bit encoding with {R36[7],R22[1:0]}: 0xx = Encoding determined by R22[1:0] (Default) 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms
6	RV	0	R36 [6]: Reserved
5	RW	0	R36 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION SWB Output Regulator Soft Stop Time After VR Disable[1] [2] 3-bit encoding with {R36[5],R26[1:0]}: 0xx = Encoding determined by R26[1:0] (Default) 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms
4	RW	0	R36 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION SWC Output Regulator Soft Stop Time After VR Disable[1] [2] 3-bit encoding with {R36[4],R28[1:0]}: 0xx = Encoding determined by R28[1:0] (Default) 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = Vendor-defined
3:1	RW	001	R36 [3:1]: ACOUSTIC_NOISE_PREVENTION_CONTROL Acoustic Noise Prevention Control Feature 000 = Feature is disabled 001 = Enable; Switching frequency threshold = 50 KHz 010 = Enable; Switching frequency threshold = 40 KHz 011 = Enable; Switching frequency threshold = 30 KHz 100 = Enable; Switching frequency threshold = 20 KHz
0	RV	0	R36 [0]: Reserved

NOTE 1 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

NOTE 2 At first power on, this register is automatically configured identically by PMIC on its own as Table 162, Register 0x44

7.2.11.3 Password Input and Command Code

Table 151 — Register 0x37

	R37		
Bits	**Attribute**	**Default**	**Description**
7:0	WO	-	R37 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (0x40 - 0x6F) Password - Lower Byte [7:0] = Code

Table 152 — Register 0x38

	R38		
Bits	**Attribute**	**Default**	**Description**
7:0	WO	-	R38 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (0x40 - 0x6F) Password - Upper Byte [7:0] = Code

Table 153 — Register 0x39

	R39		
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0x00	R39 Codes: Host Region Codes: 0x74: Clear Registers R04 to R07, Erase MTP memory for R04 to R07 Registers. DIMM Vendor Region (0x40 to 0x6F) Write Codes: 0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 and R38 registers. 0x00: Lock DIMM Vendor Region. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 and R38. 0x81: Burn DIMM Vendor Region - 0x40 to 0x4F 0x82: Burn DIMM Vendor Region - 0x50 to 0x5F 0x85: Burn DIMM Vendor Region - 0x60 to 0x6F DIMM Vendor Region (0x40 to 0x6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

7.2.11.3 Password Input and Command Code (cont'd)

Table 154 — Register 0x3A

	R3A		
Bits	**Attribute**	**Default**	**Description[1]**
7	RV	0	R3A [7]: Reserved
6	RW	0	R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host)[2] 1 = Enable Default Address Pointer; Address selected by register bits [5:4][3]
5:4	RW	0	R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation[4] 00 = R08 01 = R0C 10 = Reserved 11 = Reserved
3:2	RW	0	R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode[5] 00 = 2 Bytes 01 = 4 Bytes 10 = Reserved 11 = 16 Bytes
1:0	RV	0	R3A [1:0]: Reserved

NOTE 1 The write (or update) transaction to this register must be followed by STOP operation to allow the PMIC device to update the setting.
NOTE 2 The register setting in Table 154, Register 0x3A [5:4] is a don't care.
NOTE 3 This mode is only allowed when PEC function is disabled (i.e., Table 148, Register 0x34 [7] = '0').
NOTE 4 This register is only applicable if Table 154, Register 0x3A [6] = '1'.
NOTE 5 This register is only applicable if Table 154, Register 0x3A [6] = '1' and Table 148, Register 0x34 [7] = '1'.

7.2.11.3 Password Input and Command Code (cont'd)

Table 155 — Register 0x3B

	R3B		
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R3B [7]: Reserved
6	ROE	-	R3B [6]: PMIC_PART_CAPABILITY PMIC Current Capability. 0 = PMIC5100 (Low Current) 1 = PMIC5120 (High Current)
5:4	ROE	-	R3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	-	R3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved.
0	RV	-	R3B [0]: Reserved

Table 156 — Register 0x3C

	R3C		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	-	R3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0.

Table 157 — Register 0x3D

	R3D		
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	-	R3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1.

7.2.11.3 Password Input and Command Code (cont'd)

Table 158 — Register 0x40[1]

	R40		
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power On Sequence Config 0[2] 0 = Do Not Execute Config 0 1 = Execute Config 0
6	RWPE	0	R40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R40 [5]: Reserved
4	RWPE	0	R40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator.[3] 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power On Sequence Config 0[4] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms

NOTE 1 If more than one configuration register is used for power on sequence, first register must start at Table 158, Register 0x40 and it must go in sequential order to Table 160, Register 0x42, to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

NOTE 2 If bit [7] = '0', bits [6,4:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6,4:3] must be programmed as '1'.

NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] = '1'.

NOTE 4 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

7.2.11.3 Password Input and Command Code (cont'd)

Table 159 — Register 0x41[1,2]

	R41		
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power On Sequence Config 1 0 = Do Not Execute Config[3]1 1 = Execute Command 1
6	RWPE	0	R41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R41 [5]: Reserved
4	RWPE	0	R41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator.[4] 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power On Sequence Config 1[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms

NOTE 1 If any regulators are enabled in Table 158, Register 0x40 [6:3], those regulators must be configured as '1' in this sequence.

NOTE 2 If more than one configuration register is used for power on sequence, first register must start at Table 158, Register 0x40 and it must go in sequential order to Table 160, Register 0x42, to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

NOTE 3 If bit [7] = '0', bits [6,4:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6,4:3] must be programmed as '1'.

NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] = '1'.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

7.2.11.3 Password Input and Command Code (cont'd)

Table 160 — Register 0x42[1,2]

	R42		
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power On Sequence Config 2[3] 0 = Do Not Execute Config 2 1 = Execute Config 2
6	RWPE	0	R42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R42 [5]: Reserved
4	RWPE	0	R42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator.[4] 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power On Sequence Config 2[5] 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms

NOTE 1 If any regulators are enabled in Table 158, Register 0x40 [6,4:3] and Table 159, Register 0x41, [6,4:3], those regulators must be configured as '1' in this sequence.

NOTE 2 If more than one configuration register is used for power on sequence, first register must start at Table 158, Register 0x40 and it must go in sequential order to Table 160, Register 0x42, to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

NOTE 3 If bit [7] = '0', bits [6,4:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6,4:3] must be programmed as '1'.

NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] = '1'.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

Table 161 — Register 0x43

	R43		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R43 [7:0]: Reserved

7.2.11.3 Password Input and Command Code (cont'd)

Table 162 — Register 0x44

	R44		
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R44 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION SWA Output Regulator Soft Stop Time After VR Disable[1] 3-bit encoding with {R44[7],R46[1:0]}: 0xx = Encoding determined by R46[1:0] (Default) 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms
6	RV	0	R44 [6]: Reserved
5	RW	0	R44 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION SWB Output Regulator Soft Stop Time After VR Disable[1] 3-bit encoding with {R44[5],R4A[1:0]}: 0xx = Encoding determined by R4A[1:0] (Default) 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms
4	RW	0	R44 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION SWC Output Regulator Soft Stop Time After VR Disable[1] 3-bit encoding with {R44[4],R4C[1:0]}: 0xx = Encoding determined by R4C[1:0] (Default) 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = Vendor-defined
3:0	RV	0	R44 [3:0]: Reserved

NOTE 1 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

7.2.11.3 Password Input and Command Code (cont'd)

Table 163 — Register 0x45

	R45		
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	011 1100	R45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting[1] 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RWPE	0	R45 [1:0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low Side Voltage For Power Good Status 0 = - 5% from the setting in Table 163, Register 0x45 [7:1] 1 = - 7.5% from the setting in Table 163, Register 0x45 [7:1]

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050 mV to 1160 mV.

7.2.11.3 Password Input and Command Code (cont'd)

Table 164 — Register 0x46

	R46		
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 163, Register 0x45 [7:1] 01 = +7.5% from the setting in Table 163, Register 0x45 [7:1] 10 = +10% from the setting in Table 163, Register 0x45 [7:1] 11 = Reserved
5:4	RWPE	10	R46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over Voltage Status[1] 00 = +7.5% from the setting in Table 163, Register 0x45 [7:1] 01 = +10% from the setting in Table 163, Register 0x45 [7:1] 10 = +12.5% from the setting in Table 163, Register 0x45 [7:1] 11 = Reserved
3:2	RWPE	00	R46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 163, Register 0x45 [7:1] 01 = -12.5% from the setting in Table 163, Register 0x45 [7:1] 10 = Reserved 11 = Reserved
1:0	RWPE	11	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft Stop Time After VR Disable[2] [3] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms (Default)

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in Table 164, Register 0x46[7:6].
NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.
NOTE 3 There is an extension to the SWA Soft Stop time in Table 162, Register 0x44[7].

Table 165 — Register 0x47

	R47		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R47 [7:0]: Reserved

Table 166 — Register 0x48

	R48		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R48 [7:0]: Reserved

7.2.11.3 Password Input and Command Code (cont'd)

Table 167 — Register 0x49

	R49		
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	011 1100	R49 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting[1] 000 0000 = 800 mV 000 0001 = 805 mV 000 0010 = 810 mV ... 011 1100 = 1100 mV ... 111 1101 = 1425 mV 111 1110 = 1430 mV 111 1111 = 1435 mV
0	RWPE	0	R49 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 167, Register 0x49 [7:1] 1 = -7.5 from the setting in Table 167, Register 0x49 [7:1]

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1050 mV to 1160 mV.

7.2.11.3 Password Input and Command Code (cont'd)

Table 168 — Register 0x4A

	R4A		
Bits	**Attribute**	**Default**	**Description[1]**
7:6	RWPE	01	R4A [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 167, Register 0x49 [7:1] 01 = +7.5% from the setting in Table 167, Register 0x49 [7:1] 10 = +10% from the setting in Table 167, Register 0x49 [7:1] 11 = Reserved
5:4	RWPE	10	R4A [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over Voltage Status[2] 00 = +7.5% from the setting in Table 167, Register 0x49 [7:1] 01 = +10% from the setting in Table 167, Register 0x49 [7:1] 10 = +12.5% from the setting in Table 167, Register 0x49 [7:1] 11 = Reserved
3:2	RWPE	00	R4A [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 167, Register 0x49 [7:1] 01 = -12.5% from the setting in Table 167, Register 0x49 [7:1] 10 = Reserved 11 = Reserved
1:0	RWPE	11	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft Stop Time After VR Disable[3] [4] 00 = 0.5 ms 01 = 1 ms 10 = 2 ms 11 = 4 ms (Default)

NOTE 1 Only applicable if Table 173, Register 0x4F [0] = '0'.

NOTE 2 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in Table 168, Register 0x4A[7:6].

NOTE 3 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

NOTE 4 There is an extension to the SWB Soft Stop time in Table 162, Register 0x44[5].

7.2.11.3 Password Input and Command Code (cont'd)

Table 169 — Register 0x4B

	R4B		
Bits	**Attribute**	**Default**	**Description[1]**
7:1	RWPE	011 1100	R4B [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting[2] 000 0000 = 1500 mV 000 0001 = 1505 mV 000 0010 = 1510 mV ... 011 1100 = 1800 mV ... 111 1101 = 2125 mV 111 1110 = 2130 mV 111 1111 = 2135 mV
0	RWPE	0	R4B [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in Table 169, Register 0x4B [7:1] 1 = -7.5% from the setting in Table 169, Register 0x4B [7:1]

NOTE 1 Only applicable if Table 173, Register 0x4F [0] = '0'.
NOTE 2 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1750 mV to 1850 mV.

7.2.11.3 Password Input and Command Code (cont'd)

Table 170 — Register 0x4C

	R4C		
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4C [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in Table 169, Register 0x4B [7:1] 01 = +7.5% from the setting in Table 169, Register 0x4B [7:1] 10 = Reserved 11 = Reserved
5:4	RWPE	10	R4C [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over Voltage Status[1] 00 =+7.5% from the setting in Table 169, Register 0x4B [7:1] 01 = +10% from the setting in Table 169, Register 0x4B [7:1] 10 = +12.5% from the setting in Table 169, Register 0x4B [7:1] 11 = Reserved
3:2	RWPE	00	R4C [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in Table 169, Register 0x4B [7:1] 01 = -12.5% from the setting in Table 169, Register 0x4B [7:1] 10 = Reserved 11 = Reserved
1:0	RWPE	11	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft Stop Time After VR Disable[2] [3] 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms (Default)

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in Table 170, Register 0x4C[7:6].

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

NOTE 3 There is an extension to the SWC Soft Stop time in Table 162, Register 0x44[4].

7.2.11.3 Password Input and Command Code (cont'd)

Table 171 — Register 0x4D

	R4D		
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = Vendor specific
3:0	RV	0	R4D [3:0]: Reserved

Table 172 — Register 0x4E

	R4E		
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4E [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4E [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency[1] 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = Vendor specific
3:2	RWPE	10	R4E [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	R4E [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = Vendor specific

NOTE 1 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] = '1'.

7.2.11.3 Password Input and Command Code (cont'd)

Table 173 — Register 0x4F

	R4F		
Bits	**Attribute**	**Default**	**Description**
7:1	RV	0	R4F [7:1]: Reserved
0	RWPE	0	R4F [0]: SWA_SWB_PHASE_MODE_SELECT Switch Node A and Switch Node B Phase Regulator Mode Selection. 0 = Single Phase Regulator Mode 1 = Dual Phase Regulator Mode

Table 174 — Register 0x50

	R50		
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_ THRESHOLD_SETTING Switch Node A Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 4.5 A 01 = 5.5 A 10 = 6.5 A 11 = Vendor-Specific
5:4	RV	0	R50 [5:4]: Reserved
3:2	RWPE	01	R50 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_ THRESHOLD_SETTING Switch Node B Output Current Limiter Warning Threshold Setting[1] For COT Mode, Ivalley_limit: 00 = 4.5 A 01 = 5.5 A 10 = 6.5 A 11 = Vendor-Specific
1:0	RWPE	0	R50 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_ THRESHOLD_SETTING Switch Node C Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 1.5 A 01 = 2.0 A 10 = Reserved 11 = Vendor-Specific

NOTE 1 This register is applicable regardless of the setting in Table 173, Register 0x4F[0]. For dual phase operation, this register should be configured identically as Table 128, Register 0x20 [7:6].

7.2.11.3 Password Input and Command Code (cont'd)

Table 175 — Register 0x51

	R51		
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R51 [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting[1] 00 = 1.7 V 01 = 1.8 V 10 = 1.9 V 11 = 2.0 V
5:3	RV	0	R51 [5:3]: Reserved
2:1	RWPE	01	R51 [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting 00 = 0.9 V 01 = 1.0 V 10 = 1.1 V 11 = 1.2 V
0	RV	0	R51 [0]: Reserved

NOTE 1 The VOUT_1.8V Power Good threshold in register Table 122, Register 0x1A [2] is always fixed regardless of the setting in this register.

7.2.11.3 Password Input and Command Code (cont'd)

Table 176 — Register 0x58[1]

	R58		
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power Off Sequence Config 0 0 = Do Not Execute Config 0[2] 1 = Execute Config 0
6	RWPE	0	R58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R58 [5]: Reserved
4	RWPE	0	R58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Disable Switch Node B Output Regulator.[3] 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power Off Sequence Config 0[4] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms

NOTE 1 If more than one configuration register is used for power off sequence, first register must start at Table 176, Register 0x58 and it must go in sequential order to Table 178, Register 0x5A, to turn off all regulators. In other words, there must not be any gap of the register that is used for power off sequence.

NOTE 2 If bit [7] = '0', bits [6,4:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6,4:3] must be programmed as '1'.

NOTE 3 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] ='1'.

NOTE 4 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

7.2.11.3 Password Input and Command Code (cont'd)

Table 177 — Register 0x59[1,2]

	R59		
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power Off Sequence Config1[3] 0 = Do Not Execute Config 1 1 = Execute Config 1
6	RWPE	0	R59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R59 [5]: Reserved
4	RWPE	0	R59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator.[4] 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power Off Sequence Config 1[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms

NOTE 1 If any regulators are disabled in Table 176, Register 0x58 [6,4:3], those regulators must be configured as '1' in this sequence.

NOTE 2 If more than one configuration register is used for power off sequence, first register must start at Table 176, Register 0x58 and it must go in sequential order to Table 178, Register 0x5A, to turn off all regulators. In other words, there must not be any gap of the register that is used for power off sequence.

NOTE 3 If bit [7] = '0', bits [6,4:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6,4:3] must be programmed as '1'.

NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] ='1'.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

7.2.11.3 Password Input and Command Code (cont'd)

Table 178 — Register 0x5A[1,2]

	R5A		
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power Off Sequence Config 2[3] 0 = Do Not Execute Config 2 1 = Execute Config 2
6	RWPE	0	R5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R5A [5]: Reserved
4	RWPE	0	R5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator.[4] 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power Off Sequence Config 2[5] 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms

NOTE 1 If any regulators are disabled in Table 176, Register 0x58 [6,4:3], and Table 177, Register 0x59, [6,4:3] those regulators must be configured as '1' in this sequence.

NOTE 2 If more than one configuration register is used for power off sequence, first register must start at Table 176, Register 0x58 and it must go in sequential order to Table 178, Register 0x5A, to turn off all regulators. In other words, there must not be any gap of the register that is used for power off sequence.

NOTE 3 If bit [7] = '0', bits [6,4:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6,4:3] must be programmed as '1'.

NOTE 4 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] = '1'.

NOTE 5 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

7.2.11.3 Password Input and Command Code (cont'd)

Table 179 — Register 0x5B

	R5B		
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5B [7:0]: Reserved

Table 180 — Register 0x5D

	R5D		
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5D [7:5]: SWA_OUTPUT_SOFT_START_TIME Switch Node A Output Regulator Soft Start Time After VR Enable[1] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4:0	RV	0	R5D [4:0]: Reserved

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

Table 181 — Register 0x5E

	R5E		
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5E [7:5]: SWB_OUTPUT_SOFT_START_TIME Switch Node B Output Regulator Soft Start Time After VR Enable[1] [2] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4	RV	0	R5E [4]: Reserved
3:1	RWPE	001	R5E [3:1]: SWC_OUTPUT_SOFT_START_TIME Switch Node C Output Regulator Soft Start Time After VR Enable[1] 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
0	RV	0	R5E [0]: Reserved

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage)

NOTE 2 Only applicable if Table 173, Register 0x4F [0] = '0'. This bit is a don't care when Table 173, Register 0x4F [0] = '1'.

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Standard Improvement Form **JEDEC Standard JESD301-6**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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