EIA/JEDEC STANDARD

Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

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EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS

(From JEDEC Board Ballot JCB-98-93, formulated under the cognizance of the JC-15.1 Committee on Thermal Characterization.)

1 Background

Previous JEDEC standards [1-2] and other test board standards residing under the thermal measurement overview document [3] have described design specifications for construction of thermal test boards. These specifications were intended for conventional leaded and leadless packages. They did not address packages designed with the intention of direct thermal attachment to the test board such as deep downset packages or thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. The design detail is in addition to and not in replacement of the design specifications of those previous standards.

This specification should be used in conjunction with the electrical test procedures described in JESD51-1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)," [4], and JESD51-2, "Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)," [5].

1.1 References

JESD51-3, "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages."

JESD51-7, "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages."

JESD51, "Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device)."

JESD51-1, "Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device)."

JESD 51-2, "Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air)."

2 Scope

This specification provides for additional design geometries to be added to established thermal test board standards. The additions are only to allow testing of packages that need direct thermal contact with the thermal test board. Boards designed with this specification are not to be used on packages that do not require direct thermal attachment to the test board.

Following the intent of the previous test board specifications, this specification allows design of both universal test boards for a wide number of package geometries within a package family or for the design of unique boards for single packages.

3 Top Layer Trace Design

3.1 For single package test board designs

The thermal attach pad on the test board will be made on the top trace layer. The attach pad width and length dimensions are to be no more than 1 mm greater than the corresponding width and length dimensions of the thermal attachment structure. For example, if a thermal attachment area has an exposed area of 12 mm x 12 mm on the bottom of a 28 mm x 28 mm package, the thermal attach pad will be no larger than 13 mm x 13 mm. The array must not be smaller than the thermal attachment structure.

3.2 For universal or nested test board designs

The thermal attach area is to be made of an array of 1.0 mm x 1.0 mm (+/- 0.08 mm) trace squares separated by 0.2 mm (+/- 0.08 mm) clearances as shown in figure 1. The array is to be large enough to encompass the largest thermal attachment structure anticipated for use on the test board. The array must not be smaller than the thermal attachment structure. The array is to be positioned to maximize the number of trace squares that overlap the package's thermal attachment area.

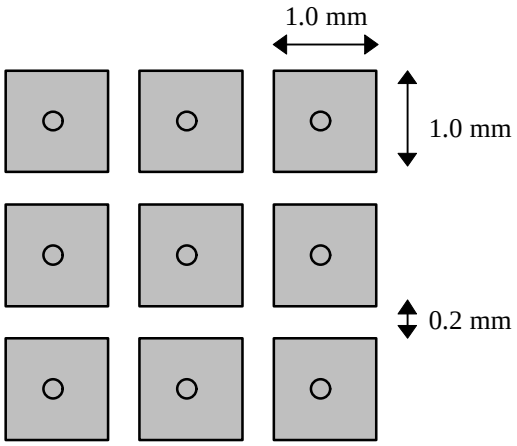
NOTES

1 The trace pattern used for the thermal attachment area must not contact any traces soldered to leads.

2 The Cu thickness of the thermal attach pad must be as specified by the general thermal test card specification documents.

4 Thermal Vias

- Thermal vias are only allowed on multi-layer test boards.
- Thermal vias for single package test board designs will be spaced on a 1.2 mm x 1.2 mm grid. This maintains the same thermal via spacing as allowed for universal test boards.
- One thermal via will exist for each trace square of a thermal attach area for a universal test board design. This thermal via will be centered within trace square.
- The thermal via diameter is 0.3 mm (+/- 0.08 mm).



NOTE — Dots represent 1 thermal via per trace area

Figure 1 — Trace array pattern for thermal attachment area showing 1.0 mm x 1.0 mm trace squares seperated by 0.2 mm spaces.

- The thermal via must provide thermal contact to the top buried plane in the multi-layer test board only.
- Thermal vias shall be plated to a minimum of 0.025 mm Cu thickness throughout the via barrel.
- Isolation Clearance Regions: Isolation clearance regions are required in the bottom buried plane for all thermal vias. An isolation clearance of no less than 0.6 mm in diameter shall be used. Isolation clearance regions are to be designed such that no isolation region merges with another. This will leave the bottom buried plane continuous from an electrical and thermal standpoint.

5 Solder Masks

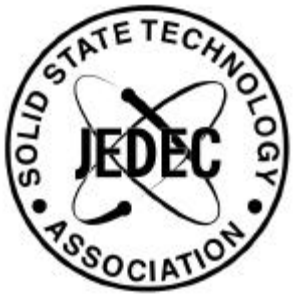
Solder masking is optional, but when used, shall be kept clear of the thermal attachment area or array.

6 Data Presentation

Table 1 lists parameters specified in this document. The "User" column allows the user to input actual measured values from his/her test boards. This table shall be appended to the table from the PCB description specification when used.

Table 1 — Specified Parameters and Values Used.

	Specified Geometry	Specification Value	User
1	Attachment Pad Size (single PCB)	attach geometry size or less than 1 mm larger	
2	Attachment Array Size (nested PCB)	size of largest attach geometry	
3	Array Trace Square Size	1.0 mm x 1.0 mm	
4	Array Trace Spacing	0.2 mm	
5	Via Diameter	0.3 mm	
6	Via Spacing	1.2 mm	
7	Via Plating Thickness (Minimum)	0.025 mm	
8	Isolation Clearance Diameter	≥ 0.6 mm	
9	Number of Vias to Top Buried Layer		
10	Via Attached to Bottom Trace Layer	optional	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