EIA/JEDEC STANDARD

High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

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JEDEC Solid State Technology Association

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HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES

(From JEDEC Board Ballot JCB-98-89, formulated under the cognizance of the JC-15.1 Committee on Thermal Characterization)

1 Background

The measurement of the junction-to-ambient ($R_{\theta JA}$) thermal characteristics of an integrated circuit (IC) package has historically been carried out using a number of test fixturing methods. The most prominent fixturing method is the soldering of the packaged devices to a printed circuit board (PCB). The characteristics of the test PCBs can have a dramatic (>60%) impact on the measured $R_{\theta JA}$. Due to this wide variability, it is desirable to have an industry-wide standard for the design of PCB test boards to minimize discrepancies in measured values between companies.

To obtain consistent measurements of $R_{\theta JA}$ from one company to the next, the test PCB geometry and trace layout must be completely specified for each package geometry tested. Such a complete specification would limit the flexibility of user companies who would like to design test boards for their individual needs. Thus, one characteristic of a test board specification is to allow some variability of PCB test board design while minimizing measurement variability.

Standard EIA/JESD 51-3, entitled “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages,” [1], details design criteria related to the design of a single layer (1s) test PCB. In contrast, this specification is dedicated to the design of a high effective thermal conductivity test PCB that embodies two signal layers, a power plane, and a ground plane (2s2p PCB).

This specification should be used in conjunction with the electrical test procedures described in JESD51-1, “Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device),” [2], and JESD51-2, “Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air),” [3].

1.1 References

EIA/JESD 51-3, “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.”

EIA/JESD 51-1, “Integrated Circuit Thermal Measurement Method - Electrical Test Method (Single Semiconductor Device).”

EIA/JESD 51-2, “Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).”

ANSI/IPC-SM-782-1987, Surface Mount Land Patterns (Configurations and Design Rules).

MIL standard MIL-W-5088B

2 Scope

This specification covers leaded surface mount components. It is not intended for through-hole, ball grid array, or socketed components. It does not cover packages with features (such as exposed die paddles) intended for direct thermal contact to multi-layer planes. See the appropriate test specifications for these package types.

3 Purpose

The purpose of this document is to describe parameterized guidelines for a thermal test board design with a "high" effective thermal conductivity compared to a single layer PCB. The resulting test PCBs are expected to show less than 10% PCB-related variation in measured $R_{\theta JA}$ for a given package geometry within the maximum and minimum range of all variable parameters. The specified parameters impact the area of the test board, the amount of copper (Cu) traces on the test board, and the resulting trace fan-out area, all of which are important parameters to the heat-sinking characteristics of the PCB.

The high effective thermal conductivity test PCB gives a near best case thermal performance value compared to the single layer low effective thermal conductivity PCB. It should be emphasized that values measured with these test boards cannot be used to directly predict any particular system application performance.

4 Stock Material

The test PCB shall be made of FR-4 material. The finished thickness of the PCB shall be 1.60 mm +/- 10%. For high-temperature applications, > 125 ºC, use of other test board material is acceptable as long as the thermal conductivity of the material is reported and measurement correlations have been established between the substitute material and FR-4.

Trace layers and layer thicknesses are defined in figure 1 along with relative dielectric thicknesses between the layers.

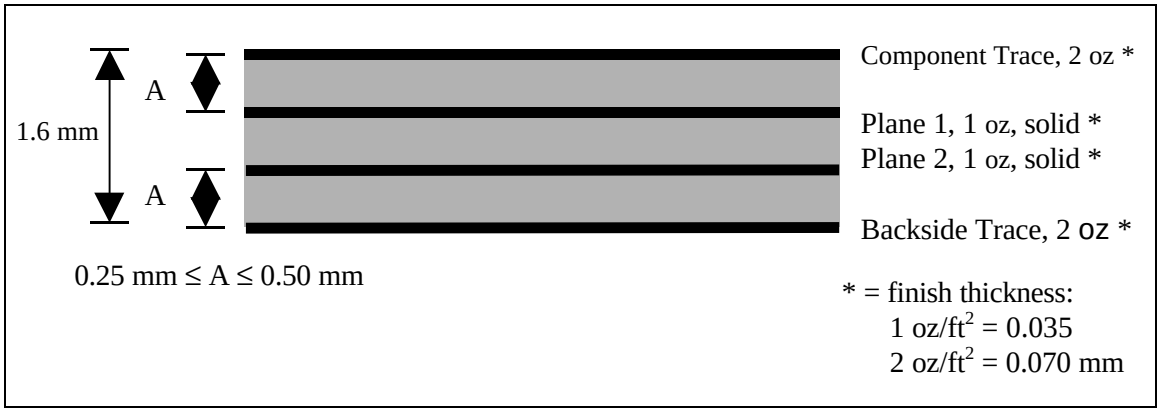


Figure 1 — Cross section of multi-layer PCB showing trace and dielectric thicknesses

5 Board Physical Geometries

The PCB shall be 76.20 mm x 114.30 mm +/- 0.25 mm in size for packages with a maximum body length less than 27.0 mm on a side (figure 2); or 101.60 mm x 114.30 mm +/- 0.25 mm in size for packages with a maximum body length from 27.0 mm to 48.0 mm (figure 3). A typical edge connector is depicted in figure 2. The edge connector may be pin-out and pitch modified for company specific needs. Width modification of dimension F is allowed.

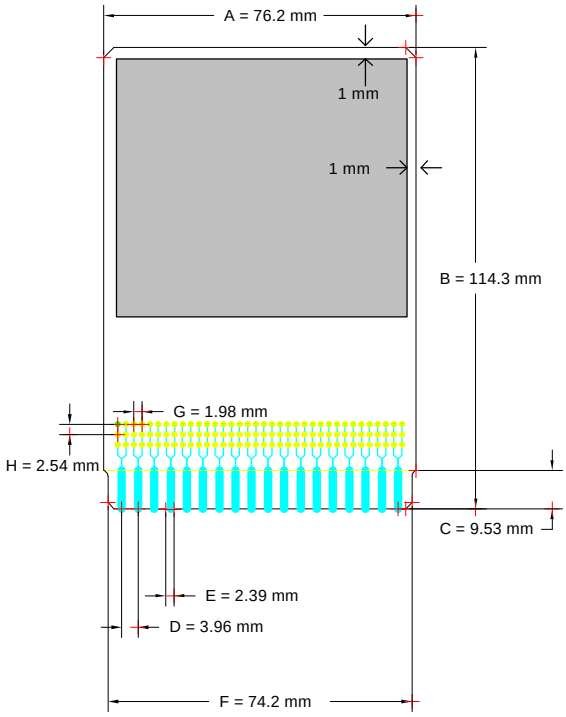


Figure 2 — PCB for packages <27.0 mm long 74.20 mm x 74.20 mm buried planes

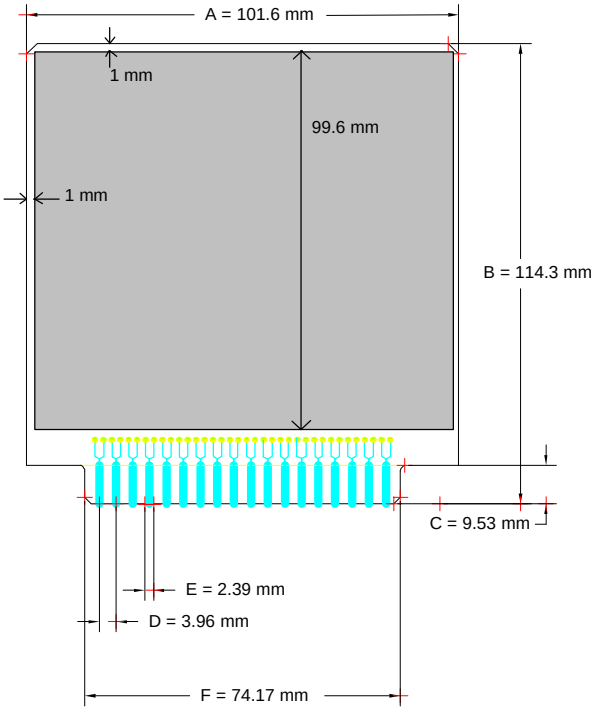


Figure 3 — PCB for Package ≥27.0 mm long 99.60 mm x 99.60 mm buried planes

6 Component Side Trace Design

6.1 Trace layout

Traces should be laid out such that the test device will be centered relative to a 76.20 mm x 76.20 mm square in the section of the test PCB furthest removed from the edge connector for packages <27.0 mm and centered in a 101.60 mm x 101.60 mm section for packages ≥27.0 mm. The traces connecting to the package must extend at least 25 mm out from the edge of the device body. Trace lengths longer than this amount are allowed and must be noted in table 2. For packages with leads on four sides, traces must be flared to meet the edges of a square such that the terminal via locations are equally spaced over 90% of the perimeter of the sides of this square adjacent to the leaded sides of the package (figure 4). For packages with leads on 2 sides, traces may be flared or straight to meet plated-through holes on 2.54 mm centers (figure 5). For inline packages (2-sided designs), the length axis of the package must align with the length axis of the test PCB. For 4-sided designs, staggering of trace terminal soldering positions inward from the trace termination square is allowed to 2.54 mm off the perimeter of the square (figure 6). For 2-sided designs, staggering of trace terminal soldering positions 2.54 mm inward from the 25 mm minimum trace length is allowed only when the number of pins per side multiplied by 2.54 mm is greater than 75 mm for the smaller PCB and greater than 100 mm for the larger PCB. A trace design that nests packages with equal pin pitches on the same PCB is allowed as long as the above conditions are met (figure 6).

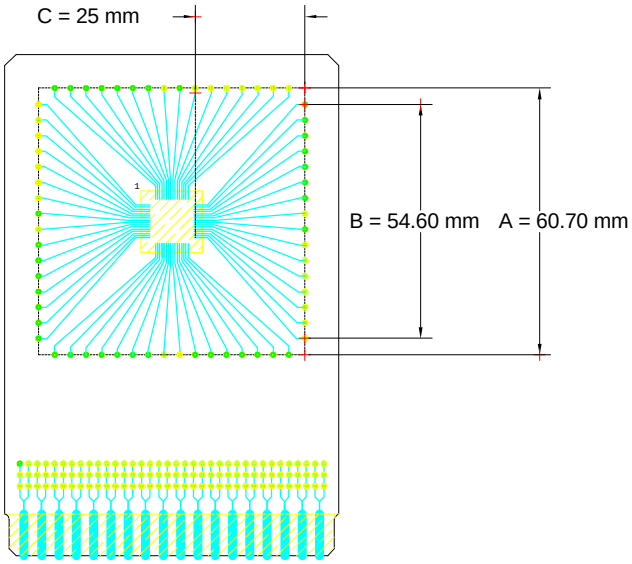


Figure 4 — Traces flared to square @ 25 mm from package body

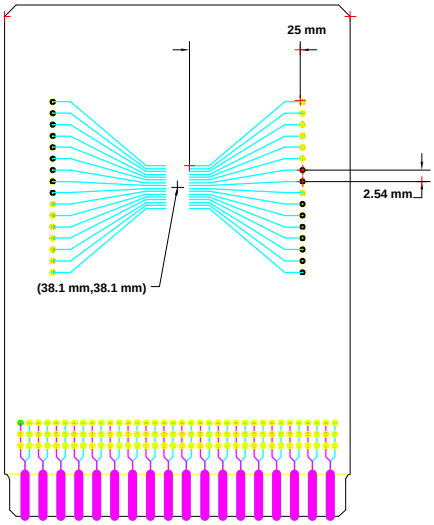


Figure 5 — Traces flared to 2.54 mm centered vias @25 mm from package body

6 Component Side Trace Design (cont'd)

6.2 Trace widths

Trace widths shall be 0.25 mm wide +/-10% at finish size for 0.5 mm or larger pin pitches. For finer pin pitches, the trace width shall be equal to the lead width. Achieving the finish size may require some oversize in design to compensate for over etching of the Cu traces during processing. Traces should terminate in a plated-through hole for soldering interconnect purposes. See 6.3 for a description of the plated-through hole vias. Solder land patterns should conform to the package lead outlines as described in ANSI/IPC publications [4]. No solder lands should be designed in the nested configuration; instead, the traces in the soldering region to the outer most lead tip of the largest package should be the same width as the lead before immediately necking down to 0.25 mm.

6.3 Plated-through hole vias

The plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter. A block-out area or isolation clearance with a diameter no greater than 0.70 mm larger than the drill hole diameter shall exist in the buried solid planes around each plated-through hole via. Other than this isolation clearance area, the buried planes shall be unbroken. Some buried-plane Cu must exist between via isolation clearance regions; the clearance regions must not merge into one another. No thermal vias shall be designed into the PCB.

6.4 Metallization characteristics

Metallization of the top and bottom trace layers on the PCB should be 2 oz (0.070 mm) finished thickness after final processing. This can be achieved by starting with a 1 oz Cu material and plating to 2 oz during PCB through-hole plating process. This process specification should be printed on all drawings to ensure proper processing. The thickness of the Cu tracks should be verified to +/- 20% after PCB fabrication since thickness variations greater than this can influence the performance of the PCB.

6 Component Side Trace Design (cont'd)

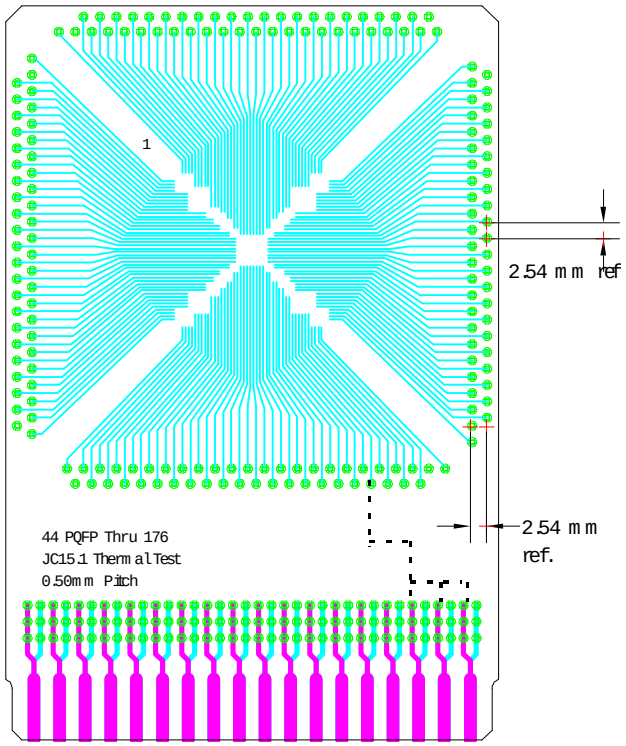


Figure 6 — Nested PCB design (44-176PQFP) (dotted line shows possible routing)

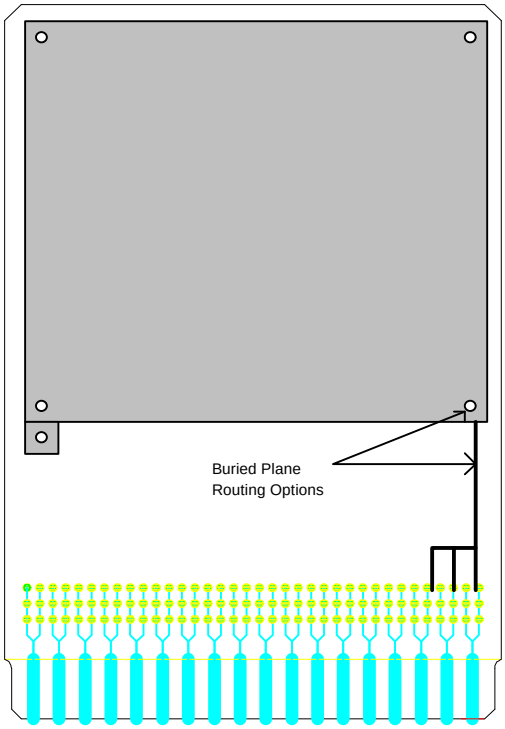


Figure 7 — Power and Ground plane termination and routing possibilities

7 Backside Trace Design

Routing connection between the through-hole vias described in 6.3 and the edge connector lands may be made using the top or backside traces. Top layer interconnection must remain outside the flared perimeter (fan-out area) of the through-holes. If hand wiring to the through-hole vias is selected instead, the backside trace design shall consist of only solder lands corresponding to the through-hole vias. Hand wiring should be made following the specification of 7.1. All power traces should be a minimum of 1 mm wide to handle possible high currents. Measurement force (power) and sense (measure) lines should be independent of each other when routed from the edge connector to the package pins.

7 Backside Trace Design (cont'd)

7.1 Wiring to the edge connector

Connection (wiring) from the through-holes to the edge connector can be made with 22AWG copper wire (0.65 mm diameter) or smaller if the connections are not designed as part of the trace pattern. Interconnect wiring to the edge connector shall be on the trailing edge of the board with respect to air flow direction and back side of the board with respect to the component placement. Connection from the edge connector to the fan-out perimeter and from the fan-out perimeter to the power dissipation structures must be made in a four-point method for force/power and sense/measure purposes. Wire and through-hole via diameters for heater force currents may need to be larger to accommodate high power tests. Use table 1 as a guide to determine the required wire diameter [5,6].

Table 1 — Wire Size Current Limits

AWG Wire Size	UL Current Capacity, (80 ºC), amperes	MIL-W-5088B amperes
30	0.4	na
28	0.6	na
26	1.0	na
24	1.6	na
22	2.5	5.0
20	4.0	8.3
18	6.0	15.4
16	10.0	19.4
14	16.0	31.2
12	26.0	40.0

8 Power and Ground Planes

The power and ground planes embedded in the board should be of 1 oz (0.035 mm thick) +0/- 20% Cu. They must be unbroken except for via isolation clearance patterns. The power and ground planes should terminate 1.0 mm from the edges of the PCB. The power and ground planes should not be present in the 9.5 mm edge connector pattern location shown in figures 2 and 3.

Power and ground connection for the heater device on the IC can be made using the buried power and ground planes. If so, ensure connection to the appropriate vias on the fan-out perimeter only.

A via connection at the corners of each buried power and ground plane is allowed for power and ground wiring to vias at the ends of the fan-out traces as shown in figure 7. In addition, designed in traces no wider than 1 mm are allowed from the edge connector to the buried planes on the buried plane layers.

9 Solder Masks

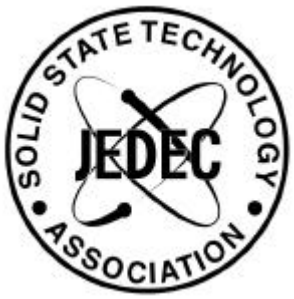
Solder masking is optional.

10 Data Presentation

Table 2 lists parameters specified in this document. The "user" column allows the user to input actual measured values from the test boards.

Table 2 — Specified parameters and values used

	Dimension	Specification	User
1	Board Finish Thickness	1.60 mm +/- 10%	
2	Dielectric Layer Thickness (to nearest surface)	0.25 mm ≤ thickness ≤ 0.50 mm	
3	Board Dimension (pkg length< 27 mm)	76.20 mm x 114.30 mm	
4	Board Dimension (27 mm ≤ pkg length ≤ 48 mm)	101.60 mm x 114.30 mm	
5	Board Material	FR-4	
6	Fan-out Trace Length (minimum)	25 mm	
7	Fan-out Trace Position	centered in 76.20 mm x 76.20 mm or 101.60 mm x101.60 mm section	
8	Trace Thickness	0.070 mm +/-20%	
9	Trace Width	0.25 mm +/-10% for ≥ 0.50 mm pin pitch; Lead width for < 0.50 mm pin pitch	
10	Trace Width in Nested Lands	Lead width	
11	Trace Coverage Area (total)		
12	Nested?	yes/no: package sizes nested	
13	Backside interconnect used?	yes/no: thickness 2 oz Cu (0.070 mm thick)	
14	Power/Ground thickness	1 oz each (0.035 mm) +0/-20%	
15	Power/Ground space to PCB edge	1 mm	
16	Power/Ground connected to fan-out vias?	yes/no: number of connections	
17	Solder Mask?	yes/no: type	
18	Via Spacing	2.54 mm ref.	
19	Via Land	1.25 mm	
20	Via Drill Hole	0.85 mm	
21	Via isolation clearance	≤0.70 mm oversize of via hole; buried plane continuity assured through via regions	
22	Wire Gauge (Sense)	≤ 22AWG (0.65 mm diameter)	
23	Wire Gauge (Heater Force)		
24	Drawings Available?	yes/no	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