JEDEC STANDARD

XFM Device
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XFM DEVICE

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Foreword

This standard has been prepared by JEDEC. The purpose of this standard is standardization of XFM form factor for embedded removable memory device including package dimensions, pin layout and electrical interface specification. This standard refers several other standard specifications that are provided by PCI-SIG® and NVM Express, Inc. organizations.

Introduction

The XFM Embedded Removable Memory Device (XFMD) is based on the PCI Express® (PCIe®) interface as a physical layer part and the NVM Express® (NVMe®) interface as a protocol layer part. Conformance to these standard interfaces will maximize connectivity between host and device.

The XFMD is a universal data storage and communication media with small and thin form factor. Its removability makes it suitable for applications that require an easy device exchange. It can be used in a variety of applications such as XR(AR, VR, MR), gaming, video recording (4K/8K movie, surveillance, EDR and drone), IOT, automotive, etc.

XFM Device

(From JEDEC Board Ballot JCB-21-22, formulated under the cognizance og the JC-64 Committee on Embedded Memory Storage and Removable Memory Cards. Item 140.01.)

1 Scope

This standard specifies the mechanical and electrical characteristics of the XFM Device. Such characteristics include, among others, package dimensions, pin layout, signal assignment, power supply voltages, currents, and electrical characteristics of the PCIe interface.

2 Normative Reference

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

Reference:

(1) PCI Express Base Specification Revision 4.0, Version 1.0 (September 27, 2017)

(2) NVM Express Base Specification Revision 1.4b (September 21, 2020)

(3) PCI Express M.2 Specification Revision 4.0, Version 1.0 (November 5, 2020)

3 Terms and Definitions

3.1 Terms and Definition

For the purposes of this standard, the terms and definitions given in the document included in clause 2, Normative Reference, and the following apply.

- "**AC Coupling Capacitor**" as defined by the PCIe Base Specification to isolate the differential data lanes between host and device.
- "**Device PCB**" is inside the device's package and used for forming pins and routing traces between pins, controller and memory chips.
- "**Host PCB**" is a part of XFM System model that mounts the Host LSI (including PCIe Root Complex), AC Coupling Capacitors and the XFM socket. Differential data lanes are connected by traces on the Host PCB having a specific characteristic impedance (Z_0).
- "**Thermal Interface Material**" is any material that has a high heat conductivity (small thermal resistance) and couples a heat-producing device with a heat-dissipating object (e.g., Host PCB) to improve heat dissipation.
- "**PHY**" in this document is physical layer of PCIe interface for serialization and deserialization of data.

3.2 Acronyms

AC	Alternating Current
ASPM	Active State Power Management (PCIe Base Specification)
AR	Augmented Reality
BER	Bit Error Rate
EDR	Event Data Recorder
ESD	Electro Static Discharge
GND	Ground
HBM	Human Body Model
IOT	Internet of Things
LSI	Large Scale Integrated Circuit
MR	Mixed Reality
NA	Not applicable
NU	Not used
PCB	Printed Circuit Board
PM	Power Management
PWR_1	Power Rail 1
PWR_2	Power Rail 2
RFU	Reserved for future use
SI	Signal Integrity
TIM	Thermal Interface Material
VR	Virtual Reality

3.3 Conventions

A binary number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Spaces may be included in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Spaces may be included in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h).

A decimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

A range of numeric values is represented in this standard in the form "a to z", where a is the first value included in the range, all values between a and z are included in the range, and z is the last value included in the range (e.g., the representation "0h to 3h" includes the values 0h, 1h, 2h, and 3h).

When the value of the bit or field is not relevant, x or xx appears in place of a specific value.

3.4 Keywords

Several keywords are used to differentiate levels of requirements and options, as follow:

Can - A keyword used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

Expected - A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

Ignored - A keyword that describes bits, bytes, quadlets, or fields whose values are not checked by the recipient.

Mandatory - A keyword that indicates items required to be implemented as defined by this standard.

May - A keyword that indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

Must - The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.

Obsolete - A keyword indicating that an item was defined in prior standards but has been removed from this standard.

Optional - A keyword that describes features which are not required to be implemented by this standard. However, if any optional feature defined by the standard is implemented, it shall be implemented as defined by the standard.

Reserved - A keyword used to describe objects—bits, bytes, and fields—or the code values assigned to these objects in cases where either the object or the code value is set aside for future standardization. Usage and interpretation may be specified by future extensions to this or other standards. A reserved object shall be zeroed or, upon development of a future standard, set to a value specified by such a standard. The recipient of a reserved object shall not check its value. The recipient of a defined object shall check its value and reject reserved code values.

Shall - A keyword that indicates a mandatory requirement strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). Designers are required to implement all such mandatory requirements to assure interoperability with other products conforming to this standard.

Should - A keyword used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).

3.4 Keywords (cont'd)

Will - The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.

3.5 Abbreviations

etc. - And so forth (Latin: et cetera)

e.g. - For example (Latin: exempli gratia)

i.e. - That is (Latin: id est)

4 Introduction

The features of the XFM Device are the following:

a) Form Factor

- Form Factor Size (Nominal)
  - surface: 14.0 mm x 18.0 mm
  - thickness: 1.4 mm

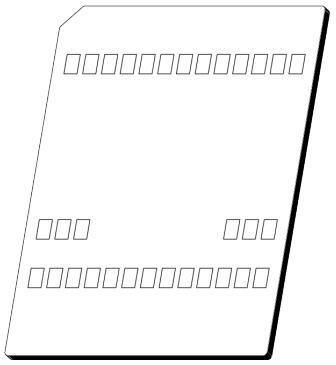

Figure 4-1 — XFM Form Factor Overview

b) Interface

- PCIe Physical Interface
  - PCIe Gen4 1-lane or 2-lane Interface
  - high reliability: PCIe interface BER under 10^{-12}
  - common clock architecture - REFCLK inputs
  - two 1.8 V sideband signals - PERST# and CLKREQ#
- NVMe Logical Interface
  - allows broad interoperability between hosts and devices
  - NVMe Revision 1.4

c) Two Power Supply Voltages

- power supply PWR_1: 2.5 V (nominal)
- power supply PWR_2: 1.2 V (nominal)

d) Power Management

- device power management functions of PCIe/NVMe for lower power consumption
  - PCIe Link power management - ASPM and L1 PM Substates
  - PCIe Slot Power Limit - host power supply capability
  - NVMe Power States

5 XFM Architecture Overview

5.1 XFM Device Concept

- Thin and small form factor
  - allows stacking of high capacity non-volatile memory (e.g. NAND Flash Memory)
  - small footprint
- Serviceability
  - replaceable with a socket system
    - embedded device replacement; e.g., malfunction, memory device lifetime, capacity extension, addition of secondary memory, etc.
    - hot insertion and removal not supported - device substitution only during host system shut down
  - device removal and disposal ensures absence of data leakage without need of long sanitize operations
  - removability solves data retention issues due to reflow stress for a pre-programmed device
- Heat dissipation
  - heat transfer to the Host PCB via 32 pins
  - additional heat transfer via bottom surface and optional use of TIM
- Connectivity and Interoperability
  - supported by PCIe/NVMe ecosystem
  - PCIe/NVMe drivers supported by most major Operating Systems
- Two Power Supply Voltages derived from NAND Flash power rails
  - 2.5 V for PWR_1 - lower side of wide range NAND Flash power supply voltage
  - 1.2 V for PWR_2 - NAND Flash interface voltage

5.2 XFM System Architecture

Figure 5-1 shows a conceptual model of the XFM system architecture, including components that are critical to the Signal Integrity (SI) of the system. Connectivity can be established whenever both host and device meet the Rx eye opening as defined by the PCIe Base Specification, therefore the XFM Device can be used with any host system that complies with the PCIe Base Specification. Compliance is out of the scope of this document.

The XFM device package includes the Device PCB, device LSI and ESD components. XFM Device doesn't mount AC coupling capacitors of Tx. The differential data lanes are connected between pins and device LSI pads via the traces on the Device PCB. ESD endurance is expected for soldering process during the device manufacturing and the device's insertion/removal by hand. It is recommended to use ESD protection components in the device package, because the pins are exposed and may accidentally be touched (ESD Testing Standards are shown in Annex D.3).

The XFM system module in Figure 5-1 shows a generic Host PCB with a Host LSI, AC coupling capacitors and XFM socket. The AC coupling capacitors are inserted in the PCB traces of the Tx and Rx pairs. The downstream AC coupling capacitors on Host PCB are placed as close as possible to the XFM socket. XFM Device is connected via XFM socket.

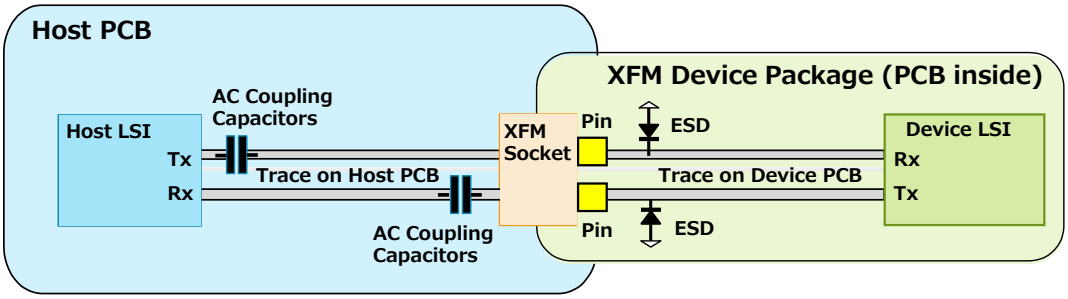

Figure 5-1 — XFM System Module High Speed Connectivity

6 XFM Device Specification

6.1 Device Package Specification

Form Factor Package Specification is defined by MO347 (by JC11). Figure 6-1 shows package schematic view. Dimensions of the form factor is indicated in nominal values.

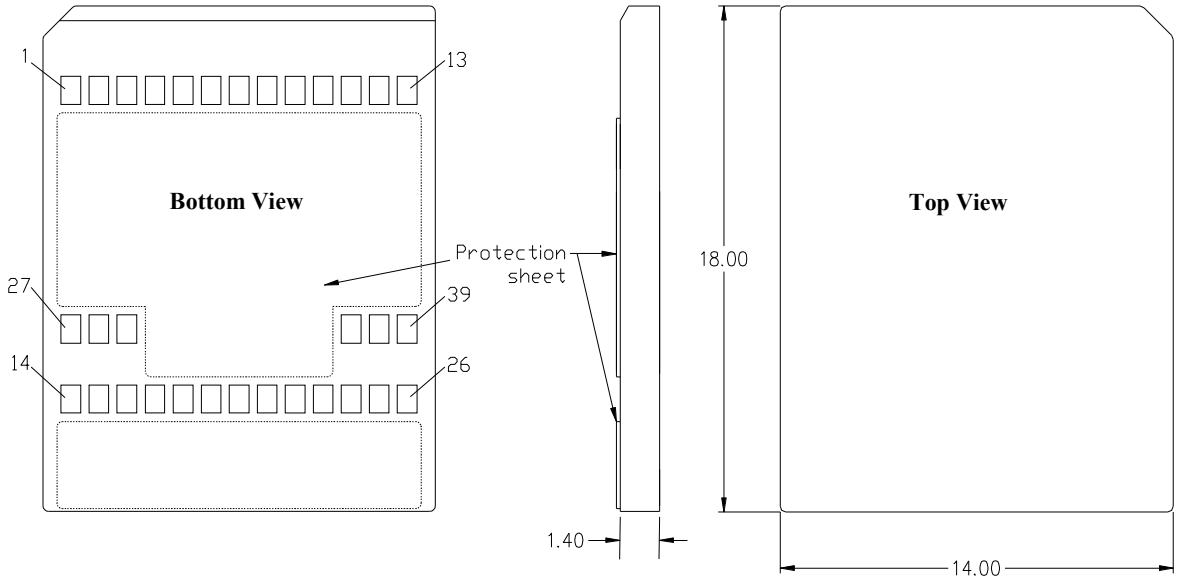

Figure 6-1 —Package Schematic View

As shown in Figure 6-1, this form factor has three rows:

(1) pin number 1 to 13 - first row
(2) pin number 27 to 39 - second row (pin number 30 to 36 are vacant)
(3) pin number 14 to 26 - third row

The device dissipates heat to host PCB mainly through socket contacts to its 32 pins. Heat dissipation via surface contact is another method to improve heat transfer away from XFM device. Therefore, pins 30 through 36 are not populated to allow the insertion of TIM, which allows a direct connection between the device and the Host PCB.

The device's surface inside of the area defined as protection sheet may be used for vendor specific purposes and covered with an appropriate material.

6.2 Signal Name Assignment

Table 6-1 shows signal names assignments, Figure 6-2 shows the placement of the pins on the device.

Table 6-1— Signal Name Assignment

Pin No.	Signal Name	Base configuration
1	GND	GND
2	PERp0	Receiver Differential Pair, Lane 0
3	PERn0	
4	GND	GND
5	PERp1	Receiver Differential Pair, Lane 1
6	PERn1	
7	GND	GND
8	PETp0	Transmitter Differential Pair, Lane 0
9	PETn0	
10	GND	GND
11	PETp1	Transmitter Differential Pair, Lane 1
12	PETn1	
13	GND	GND
27	GND	Power GND
28	GND	Power GND
29	Reserved	Reserved for Future Use
30-36		Missing Pin number
37	Reserved	Reserved for Future Use
38	GND	Power GND
39	GND	Power GND
14	GND	GND
15	REFCLKp	Reference Clock Differential Pair (100MHz)
16	REFCLKn	
17	GND	GND
18	GND	Power GND
19	PERST#	PCIe Reset Signal (Input)
20	PWR_2	Power Rail 2 (1.2V nominal)
21	PWR_2	
22	PWR_2	
23	CLKREQ#	Clock Request Signal (Open Drain)
24	PWR_1	Power Rail 1 (2.5V nominal)
25	PWR_1	
26	PWR_1	

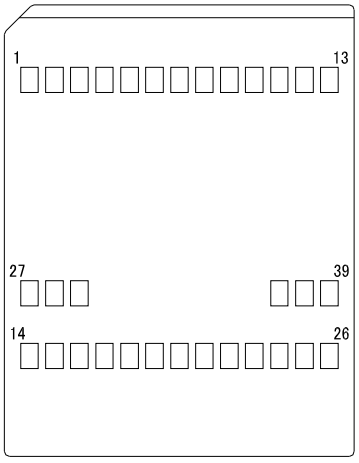

Figure 6-2 — PIN Number Assignment

The first row is assigned to two lanes of PCIe differential data.

The second row consists of four Power GNDs (27, 28, 38, and 39) and two reserved pins (29 and 37)

The third row consists of six power rails, one Power GND, differential REFCLK pair surrounded by two GNDs and 2 PCIe sideband signals (PERST#, CLKREQ#).

NOTE Reserved pins (29 and 37) shall be left open.

6.3 DC Electrical Specification

6.3.1 Power Supply Voltages

Table 6-2 defines the voltage range of the power supply at the device pins PWR_1 and PWR_2. The common power supply is supposed to provide nominal voltage according to the model explained in Annex A.4.

Table 6-2 — Power Supply Voltages

Power Rail	Voltage Range		
	Minimum [V]	Nominal [V]	Maximum [V]
PWR_1	2.40	2.50	2.70
PWR_2	1.14	1.20	1.26

6.3.2 Maximum Current of Power Rails and Power GNDs

Essential current requirement for each power rail is as follows:

Maximum DC current per pin: 1.2A

The XFM Device has three power pins for each power supply and five power GNDs pins. The maximum current of 3.6 A can be drawn for each power rail. Total current drawn for five power GNDs shall be lower than 6.0 A (See Figure A. 3).

AC current such as peak current is not defined in this document for design flexibility. For example, a decoupling capacitor value should be determined by a peak current of a specific device.

6.3.3 Current Ranges and Current Classes

6.3.3.1 Introduction

The XFM lineup can consist of different kind of devices with lower or higher performance and current consumption. In order to classify in which particular range a device falls, the definition of “Current Ranges” is added to ease the selection of a suitable devices according to the performance and power consumption needs of a given application (see see Table A. 4).

The current that can be actually drawn by a device is limited also by the voltage drop caused by the contact resistance with the socket. This means that the usable current is also restricted by components such as the power supply and the socket. The definition of “Current Class” is added in order to express the amount of usable current depending on the characteristics of such components.

Current Ranges and Current Classes can also be used as design guidelines for both the system integrator and the device manufacturer in order to achieve an optimal interoperability. In this way it is possible to design a new product even before all its parameters are known. A device may be selected to match a specific system after that the other components have been selected. A device may indicate a list of supported classes in the product specification.

6.3.3.2 Definition of Current Ranges

XFM defines four Current Ranges as shown in Table 6-3. The current is measured as RMS average over 100 ms. A device implementation may target a specific Current Range and may have the possibility to switch between different Current Ranges. A device indicates at least one of given Current Ranges according to a mode of the max (I_{PW1}, I_{PW2}) by product specification.

Table 6-3 — Current Ranges

Current Ranges	I_{PW1}, I_{PW2} [A]
CR-A	2.6 ~ 3.6
CR-B	2.0 ~ 2.6
CR-C	1.7 ~ 2.0
CR-D	~ 1.7

Typically, PWR_1 is used for NAND Memory and PHY and PWR_2 is used for NAND I/F. The logic circuits may be powered from either PWR_1 or PWR_2, according to the implementation. In order to accommodate any implementation, the current ranges are large enough to accommodate any combination. E.g. if CR-C is considered, it is possible to assume that 1.3 A are needed for the logic circuits and 0.7 A for NAND Flash and PHY, thus the upper limit is 2.0 A if the logic is on PWR_1. The minimum current of CR-C is assigned to 1.7 A considering there is 0.3 A gap. 1.7 A is assigned to the border current between CR-C and CR-D.

The current gap 0.6 A (twice of CR-C gap) is reserved for CR-B to make device design more flexible. 2.6 A is assigned to the border current between CR-A and CR-B.

These border currents are used as indices for intermediate currents of Current Ranges. Percentage of border currents against the maximum current 3.6 A are calculated as follows: 2.6 A is 72 %, 2.0 A is 56 % and 1.7 A is 47 %.

6.3.3.3 Permissible Current

The current drawn from a device will also characterize the voltage drop at the device's pin, according to the model as shown in Figure 6-3, which takes into account the fact that the resistance of the contact between socket and device will be higher than zero and affect the operation of the system. It is important to ensure that the voltage at the device's pin never goes below the minimum (V_D_min) defined by the voltage ranges.

A system using a common power supply is supposed to provide a nominal voltage (V_{PS}) in the device voltage range defined by Table 6-2. When the voltage drop brings the voltage V_D to V_D_min, the current per power pin is called "permissible current" (Ip). Ip shall not exceed the maximum pin current (I_{PW}_max) of 1.2 A. Ip is calculated with the two major host specific parameters; the socket contact resistance during the system's lifetime (Rc) and the power supply fluctuations (expressed by V_{PS}_min to V_{PS}_max) that will typically be < 1% or < 2%.

The Ip is calculated by following formula.

$Ip = \min (I_{PW}\_max,\ (V_{PS}\_min - V_D\_min) / Rc\_max)$

Refer to Annex A.3 for more details of permissible current.

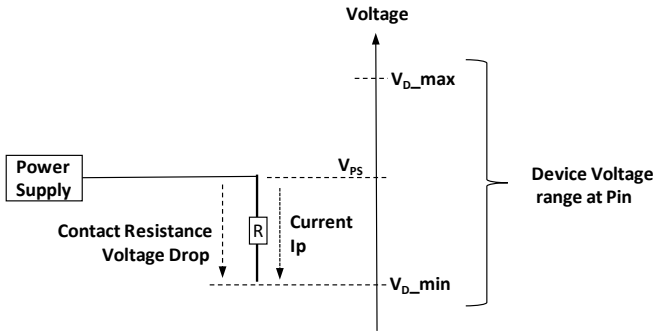

Figure 6-5 — Voltage Drop by Contact Resistance

In order to ensure a consistent calculation of the Current Classes and avoid rounding errors, 2 decimal places shall be used as shown shown in Table 6-4 and Table 6-5. The voltage min is rounded down and the voltage max is rounded up, both on the second decimal place.

Table 6-4 — Fluctuation of Power Supply Source Voltage V_{PS1}

Fluctuation	V_{PS1}_min	V_{PS1} Nominal	V_{PS1}_max
1 %	2.47 V	2.50 V	2.53 V
2 %	2.45 V	2.50 V	2.55 V

Table 6-5 — Fluctuation of Power Supply Source Voltage V_{PS2}

Fluctuation	V_{PS2}_min	V_{PS2} Nominal	V_{PS2}_max
1 %	1.18 V	1.20	1.22 V
2 %	1.17 V	1.20	1.23 V

6.3.3.4 Definition of Current Classes

There are four Current Classes, CC1 to CC4, that enable simple expression of a host system configuration, determined by host's parameters. Each class consist of a pair of usable currents for I_{PW1} and I_{PW2}.

CC1 is calculated by the permissible currents Ip1 and Ip2:

— CC1 (3 × Ip1, 3 × Ip2).

The rightmost suffix indicates the power rail number. Ip1 and Ip2 are calculated by the following formula:

Ip1= min (I_{PW}_max, (V_{PS1}_min – V_{D1}_min) / Rc_max)
Ip2= min (I_{PW}_max, (V_{PS2}_min – V_{D2}_min) / Rc_max)

CC2 to CC4 provide intermediate classes. Each of current is limited by the border currents (2.6 A, 2.0 A and 1.7 A respectively) that are defined in 6.3.3.2. For example, CC2 shall not exceed 2.6 A or the permissible current.

CC2 to CC4 are calculated as follows using min() function:

— CC2 (min(3 × Ip1, 2.6 A), min(3 × Ip2, 2.6 A));
— CC3 (min(3 × Ip1, 2.0 A), min(3 × Ip2, 2.0 A));
— CC4 (min(3 × Ip1, 1.7 A), min(3 × Ip2, 1.7 A)).

6.3.3.5 Notation of Current Classes

Variations of CC1 to CC4 with host components parameters are expressed by the format **CC#_$%**.

a) 'CC' denotes the Current Classes.
b) '#' denotes one digit to specify CC number:
   - 1; 2; 3; or 4.
c) '$' denotes one digit to specify contact resistance:
   - 3: 30 mΩ; 4: 40 mΩ; 5: 50 mΩ; 6: 60 mΩ; 7: 70 mΩ; 8: 80 mΩ.
d) '%' denotes one digit to specify power supply fluctuation:
   - 1: ±1%; 2: ±2%.

It is possible that the component parameters have values that fall between the values listed in this standard. In this case, the nearest larger values shall be selected.

See Annex A.4 about Current Classes implementation examples.

6.3.4 Electrical Characteristics of 1.8 V Logic Signaling

PERST# and CLKREQ# use 1.8 V signaling. 1.8 V signaling is defined in section "1.8 V Logic Signal Requirements" of the PCI-SIG M.2 Specification [PCI-SIG M.2]. M.2 expects a common I/O supply voltage (V_{DD18}) from 1.7 V to 1.9 V that determines V_{OH} and V_{IH} / V_{IL}. M.2 defines the wide range of pull-up resistor values, the system designer selects a pull-up resistor value considering voltage difference between host and device. See Annex A.5 for details about the calculation of the pull-up resistor value.

6.3.5 Power-up Timing

XFM conforms to the M.2 power-up timing. Refer to M.2 specification Figure 3-1 - CLKREQ# Clock Control Timings and Figure 3-2 - Power-up Timing Sequence for an Adapter Powered from System Power Rail.

6.4 AC Electrical Specification

PCIe differential data lane receiver and transmitter shall conform to the PCI Express Base Specification Revision 4.0.

ANNEX A - Device Design Guide (informative)

A.1 ESD Endurance for Removable Device

The device should implement a level of ESD tolerance of ±4 kV according to the HBM, more may be implemented according to the usage environment. The ESD tolerance of the PCIe differential lanes may be improved using ESD components.

A.2 Power Distribution

Power Supply voltages are derived from typical values used for the NAND Flash. PWR_1 is used to for the supply of NAND Flash, PWR_2 is used to for the controller as well as for the NAND Flash Interface. Other power supply voltages that are needed may be generated starting from PWR_1 or PWR_2. The core logic voltage (less than 0.9 V) may be generated from either PWR_1 or PWR_2. This option causes current imbalance between PWR_1 and PWR_2. Then power supply should be designed to provide the maximum current for both PWR_1 and PWR_2.

Figure A. 1 shows an example of possible power distribution. “Conv.” indicates a converter such as a DC-DC or an LDO, and may be inside or outside of Controller. The PCIe interface signal voltage and PCIe PHY source voltages are generated from PWR_1. This example shows the case the generation of the core logic voltage from PWR_2.

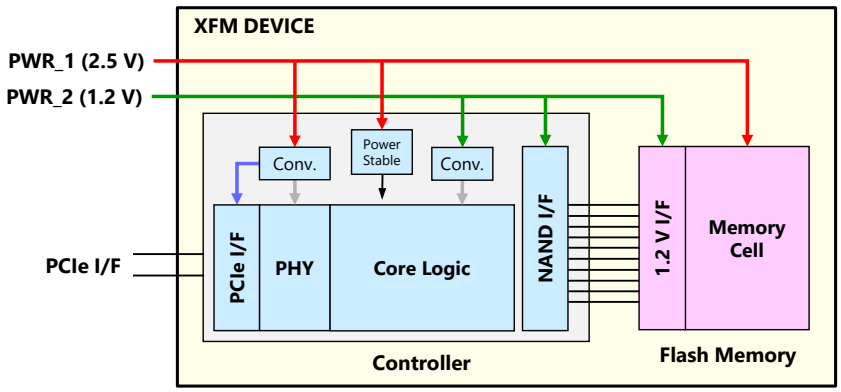

Figure A. 1 — Power Distribution Example

The PHY consists of an analog part (two Tx and two Rx) and a digital part (e.g., SERDES, digital filter, etc. - high speed parallel data circuits).

A.3 Contact Resistance and Permissible Current

The resistance of the contact between the socket and the XFM Device may cause a voltage drop that depends on the resistance and the current flowing through the contact. The current restricted by the contact resistance is called “Permissible Current” Ip and it is determined by several factors including host power supply voltage fluctuation, the minimum power supply voltage of the device, etc. This annex shows an example calculation of the permissible current:

Figure A. 2 shows the relation between voltages. Voltage drop is calculated as follows:

Voltage drop = Rc_max × Ip

The contact resistance (Rc) is sum of socket lead resistance and resistance at contact of socket lead and device pin. Rc_max stands for the maximum contact resistance considering fluctuation (e.g., contact resistance is indicated by an initial value and its variation).

The voltage supplied to the power pin shall not be higher than the maximum power supply voltage and lower than the minimum power supply voltage.

$V_{PS}\_max \leq V_{D}\_max$

$V_{PS}\_min - V_{D}\_min \geq$ Voltage drop $= Rc\_max \times Ip$

V_{PS} stands for power supply source voltage and fluctuation in plus and minus is assumed depending on the power supply circuit design. Those are expressed by V_{PS}_min and V_{PS}_max. V_{D}_max stands for the maximum value of the device's power supply voltage. V_{D}_min stands for the minimum value of device power supply voltage that is provided by Table 6-2.

Each power pin current is limited by the maximum current $I_{PW}\_max = 1.2$ A. The permissible current Ip which is saturated with I_{PW}_max is calculated by following formula by using min() function:

$Ip = \min(I_{PW}\_max,\ (V_{PS}\_min - V_{D}\_min) / Rc\_max)$

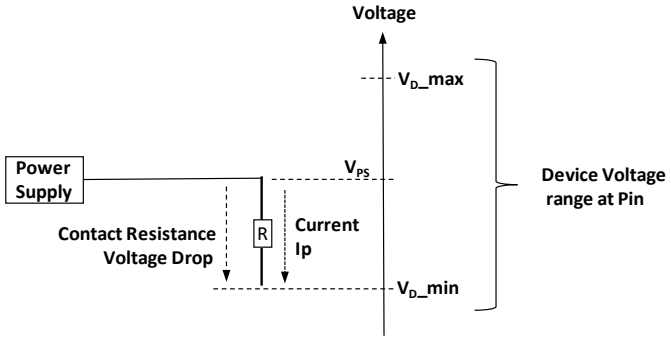

Figure A. 2 — Voltage Drop by Contact Resistance

The examples below show the case of ±1% and ±2% V_{PS} fluctuation.

Table A. 1 shows lists of permissible current Ip1 for PWR_1 (2.5 V range) in reference to contact resistances. Fluctuation of host power supply voltage is also included in the calculation for two cases; 1% drop and 2% drop
Table A. 2 shows lists of permissible current Ip2 for PWR_2 (1.2 V range) in reference to contact resistances. Fluctuation of host power supply voltage is also included in the calculation for two cases; 1% drop and 2% drop

Table A. 1 — Permissible Current of PWR_1

Rc_max [mΩ]	Ip1 [A] V_{PS} 1% drop	Ip1 [A] V_{PS} 2% drop
30	1.20	1.20
40	1.20	1.20
50	1.20	1.00
60	1.17	0.83
70	1.00	0.71
80	0.88	0.63

Conditions: Vps = 2.50 V, V_{D}_min = 2.40 V

Table A. 2 — Permissible Current of PWR_2

Rc_max [mΩ]	Ip2 [A] V_{PS} 1% drop	Ip2 [A] V_{PS} 2% drop
30	1.20	1.00
40	1.00	0.75
50	0.80	0.60
60	0.67	0.50
70	0.57	0.43
80	0.50	0.38

Conditions: Vps = 1.20 V, V_{D}_min = 1.14 V

EXAMPLE 1

In case of 60 mΩ contact resistance and 2% fluctuation

— Permissible current Ip1 = (2.45 V (V_{PS1}_min) – 2.40 V (V_D_min)) / 60 mΩ = 0.83 A
— Total permissible current for 3 pins of PWR_1 = 0.83 × 3 = 2.49 A

— Permissible current Ip2 = (1.17 V (V_{PS1}_min) – 1.14 V (V_D_min)) / 60 mΩ = 0.50 A
— Total permissible current for 3 pins of PWR_2 = 0.50 × 3 = 1.50 A

— Total current for 5 pins of power GND = 3.99 A

EXAMPLE 2

If V_{PS} is set to 200 mV higher in case of 2% fluctuation, permissible current can be improved:

— Permissible current PWR_2 = (1.22 V (V_{PS}) – 0.024 V (2% drop) – 1.14 V (V_D_min)) / 60 mΩ = 0.93 A

A.4 Current Classes Implementation Examples

These are some consideration points for Current Classes:

a) Finding design compromise between host and device
Usable current is determined by mutual design. A voltage drop at power supply pin is a major concern that is related to device current consumption and characteristics of host components (socket, power supply, etc.). This means that optimized current design is achieved by finding a mutually acceptable compromise. There are two scenarios A) device is customized to be able to use in a specified host system. and B) host system is designed by to be able to use a specified device.

b) Device current imbalance
Current Classes are intended to allow two cases of device implementation that supply voltage for logic circuit may be generated form either PWR_1 or PWR_2. As logic current is relatively large, it will cause large current imbalance between I_{PW1} for PWR_1 and I_{PW2} for PWR_2. This means that there are two cases of current imbalance, depending on devices; $I_{PW1} \leq I_{PW2}$ and $I_{PW1} \geq I_{PW2}$. There is the other option that both currents may be large. By supplying I_{PW1} and I_{PW2} with enough current, host can support multiple devices regardless of the device's implementation.

c) Providing 4 current levels selection
Current Ranges provides four current range selections below 3.6 A (1.2 A × 3 pins) for four levels of power and performance target. The four options enable optimized design for lower power applications.

Figure A. 3 shows a system current flow model that assumes existence of resistive elements between the power source and the device pin that cause voltage drop by current flow. Current flow of I_{PW1} and I_{PW2} is illustrated.

Following are consideration points for the implementation:

— Voltage drop by contact resistance at PWR_1 and PWR_2 pins
  - The voltage drop is proportional to the device's current consumption
  - 2.5 V has margin imbalance; 0.1 V lower side margin and 0.2 V upper side margin
  - 1.2 V margin is small 0.06 V - the lower the voltage, the smaller the margin
— Device Current Imbalance
  - $I_{PW1} \geq I_{PW2}$: Logic voltage is generated from PWR_1
  - $I_{PW1} \leq I_{PW2}$: Logic voltage is generated from PWR_2
— Power Rails and Power GND
  - 3 pins for each PWR_1 and PWR_2 that can provide up to 3.6 A assuming that impedance is balanced
  - 5 pins for common GND that limits total current to 6 A

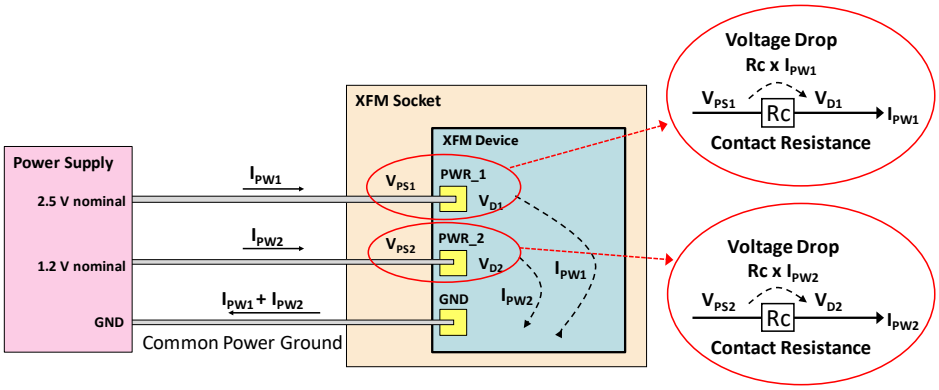

Figure A. 3 —System Current Flow Model

The following figures show two example flow charts; one is for the scenario A) and the other is for the scenario B) to determine current design using Current Classes.

Figure A. 4 shows an example flow chart for the scenario A):

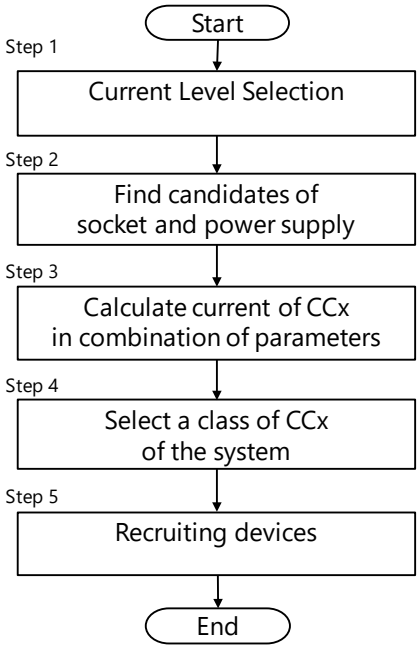

Figure A. 4 — Example Flow Chart of Scenario A)

- Step 1 : Host system selects one of specified currents from (3.6 A, 2.6 A, 2.0 A and 1.7 A).
  - This is a case host system selects 2.6 A as maximum current
- Step 2 : Find candidates of sockets and power supply
  - Sockets of 50 mΩ~70 mΩ contact resistance are available
  - PMIC of 1% fluctuation is available.
- Step 3 : Calculate classes of CC2 for less than 2.6 A. Three candidates of sockets 50 mΩ~70 mΩ reduces combination of calculation.
  - CC2_51: I_{PW1} = 2.6 A, I_{PW2} = 2.4 A
  - CC2_61: I_{PW1} = 2.6 A, I_{PW2} = 2.0 A
  - CC2_71: I_{PW1} = 2.6 A, I_{PW2} = 1.7 A
- Step 4 : Host system selects CC2_61 by following reasons:
  - CC2_71 is not selected because I_{PW2} = 1.7 A would make device design difficult.
  - To support multiple vendor's devices, balancing I_{PW1} and I_{PW2} is better for device implementation flexibility (CC2_51 is better) but a socket with 50 mΩ is rarely available.
  - PMIC is selected that can provide $I_{PW1} \geq$ 2.6 A and $I_{PW2} \geq$ 2.0 A
- Step 5 : Host vendor can select devices by indicating the current class of CC2_61
  - Device vendors knows the current requirements of device from CC2_61
  - A device is supposed to be usable on the system if I_{PW1} < 2.6 A and I_{PW2} < 2.0 A
  - In case of CR-B, it has 0.6 A margin (2.0 A to 2.6 A) to I_{PW1} but no margin to I_{PW2}

Figure A. 5 shows an example flow chart for the scenario B):

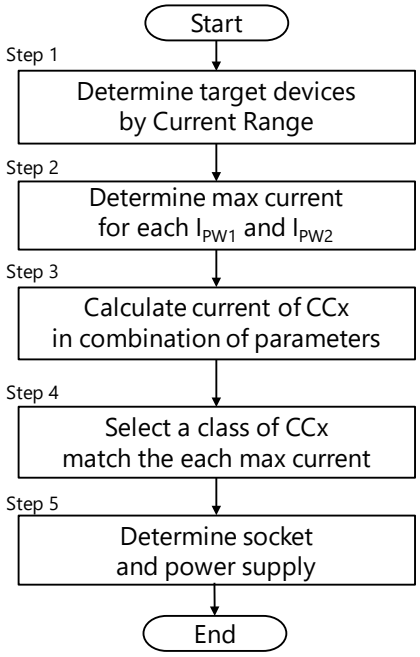

Figure A. 5 — Example Flow Chart of Scenario B)

— Step 1 : Host vendor collects candidates of XFM devices that can be used in a host system.
  - Current Ranges can be used as index to select device candidates.
  - This example collects devices of $I_{PW1} < 2.6$ A that will be included in CR-B or CR-C.
  - Also Current Classes can be used to select device candidates if device vendor provides a list of supported classes from CC1 to CC4.

— Step 2 : Determine the maximum current required
  - Power supply ability for I_{PW1} and I_{PW2} is determined by the highest of the actual maximum current of the device.
  - In a CR-B device, the actual maximum current may be lower than 2.6 A.

— Step 3 : Calculate classes of CC2 with host parameters combination.
  - CC2_51: $I_{PW1} = 2.6$ A, $I_{PW2} = 2.4$ A
  - CC2_61: $I_{PW1} = 2.6$ A, $I_{PW2} = 2.0$ A
  - CC2_71: $I_{PW1} = 2.6$ A, $I_{PW2} = 1.7$ A
  - CC2_52: $I_{PW1} = 2.6$ A, $I_{PW2} = 1.8$ A
  - CC2_62: $I_{PW1} = 2.5$ A, $I_{PW2} = 1.5$ A

— Step 4 : Select a class in CC2 that satisfy current requirements in Step 2
  - Candidates of classes that can realize current requirements
  - If any of the devices' $I_{PW2} > 2.0$ A, CC2_51 needs to be selected or devices of $I_{PW2} > 2.0$ A may be removed from the candidates.
  - If there is no device $I_{PW2} > 2.0$ A, CC2_61 (better socket availability) may be selected
  - If all devices are $I_{PW2} < 1.7$ A, CC2_71 or CC2_52 may be selected.

— Step 5 : Determine socket, power supply and devices
  - Availability and other factors are also considered
  - Determine devices form the candidates.
  - Host may simply indicate a specific system configuration by a class of CCx

Table A. 3 shows tables for CC1 to CC4 for all parameters combination that will save the labor for calculation. Voltage fluctuations V_{PS1}_min in Table 6-4 and V_{PS2}_min Table 6-5 are used in calculation. The rightmost column shows an example of device candidates that are selected by I_{PW1}. The candidates have the possibility to satisfy current requirements by tuning implementation if the device's minimum I_{PW1} is lower than the I_{PW1} of a given class.

Table A. 3 — Tables of CC1 to CC4 for All Parameters Combination

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC1_31	3.6	3.6	6.0	CR-A to -D
CC1_41	3.6	3.0	6.0	CR-A to -D
CC1_51	3.6	2.4	6.0	CR-A to -D
CC1_61	3.5	2.0	5.5	CR-A to -D
CC1_71	3.0	1.7	4.7	CR-A to -D
CC1_81	2.6	1.5	4.1	CR-B to -D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC2_31	2.6	2.6	5.2	CR-B to -D
CC2_41	2.6	2.6	5.2	CR-B to -D
CC2_51	2.6	2.4	5.0	CR-B to -D
CC2_61	2.6	2.0	4.6	CR-B to -D
CC2_71	2.6	1.7	4.3	CR-B to -D
CC2_81	2.6	1.5	4.1	CR-B to -D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC3_31	2.0	2.0	4.0	CR-C to -D
CC3_41	2.0	2.0	4.0	CR-C to -D
CC3_51	2.0	2.0	4.0	CR-C to -D
CC3_61	2.0	2.0	4.0	CR-C to -D
CC3_71	2.0	1.7	3.7	CR-C to -D
CC3_81	2.0	1.5	3.5	CR-C to -D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC4_31	1.7	1.7	3.4	CR-D
CC4_41	1.7	1.7	3.4	CR-D
CC4_51	1.7	1.7	3.4	CR-D
CC4_61	1.7	1.7	3.4	CR-D
CC4_71	1.7	1.7	3.4	CR-D
CC4_81	1.7	1.5	3.2	CR-D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC1_32	3.6	3.0	6.0	CR-A to -D
CC1_42	3.6	2.2	5.8	CR-A to -D
CC1_52	3.0	1.8	4.8	CR-A to -D
CC1_62	2.5	1.5	4.0	CR-B to -D
CC1_72	2.1	1.2	3.3	CR-B to -D
CC1_82	1.8	1.1	2.9	CR-C to -D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC2_32	2.6	2.6	5.2	CR-B to -D
CC2_42	2.6	2.2	4.8	CR-B to -D
CC2_52	2.6	1.8	4.4	CR-B to -D
CC2_62	2.5	1.5	4.0	CR-B to -D
CC2_72	2.1	1.2	3.3	CR-B to -D
CC2_82	1.8	1.1	2.9	CR-C to -D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC3_32	2.0	2.0	4.0	CR-C to -D
CC3_42	2.0	2.0	4.0	CR-C to -D
CC3_52	2.0	1.8	3.8	CR-C to -D
CC3_62	2.0	1.5	3.5	CR-C to -D
CC3_72	2.0	1.2	3.2	CR-C to -D
CC3_82	1.8	1.1	2.9	CR-C to -D

Current Class	I_{PW1} [A]	I_{PW2} [A]	Total [A]	Device Candidates
CC4_32	1.7	1.7	3.4	CR-D
CC4_42	1.7	1.7	3.4	CR-D
CC4_52	1.7	1.7	3.4	CR-D
CC4_62	1.7	1.5	3.2	CR-D
CC4_72	1.7	1.2	2.9	CR-D
CC4_82	1.7	1.1	2.8	CR-D

An example relation between Current Ranges of a device and its performance is shown in Table A. 4, but since this depends on the implementation and on the technology, this is only to give a guideline and not normative.

Table A. 4 — Example Relation between Current Ranges and Performance

Current Ranges	I_{PW1} , I_{PW2} [A]	Memory Performance Example
		PCIe Gen4 2-lane / PCIe Gen5 2-lane
CR-A	2.6~3.6	4GB/s~8GB/s
CR-B	2.0~2.6	2GB/s~5GB/s
CR-C	1.7~2.0	1GB/s~3GB/s
CR-D	~1.7	~2GB/s

A.5 Sideband Signaling

There may be an imbalance in 1.8 V power supply generation between host and device. The following guidelines help the system designer to take this imbalance into account under all possible operating conditions.

The voltage difference of V_{DD18} that is expressed by V_{DDIO} (device) and V_{PU} (host) is shown in Figure A. 6 as an example. V_{DDIO} is the voltage of the device's input cell that is internally generated. V_{PU} is the pull-up voltage (1.8 V) that is generated by the host. On/off timing of V_{PU} is correspondent to that of PWR_1. 'Conv.' stands for a generic voltage converter to generate the 1.8 V I/O supply voltage.

PERST# is an input. CLKREQ# is an open-drain I/O. Figure A. 6 shows an example implementation, when CLKREQ# is high, both open drain drivers are in the off state. V_{OH} is calculated by V_{PU} minus the voltage drop, which is determined by the value of the pull-up resistor and the total leakage current. The total leakage current (sum of host and device) that flows in the pull-up resistor at high voltage level limits the value of the resistor itself. The host needs to select the pull-up resistor value so that V_{OH} satisfies V_{IH} (min).

In this example, a 1.8 V supply is available on the Host PCB.

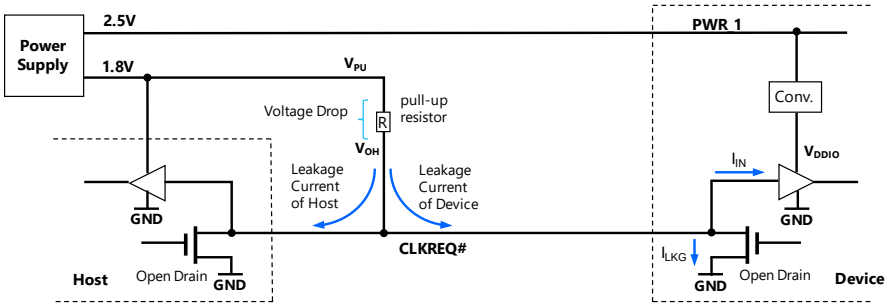

Figure A. 6 — Example Calculation of Output High Voltage and Pull-Up Resistor

EXAMPLE
If the device's supply reaches 1.90 V, the V_{IH}(min) will be 1.33 V. The host has to take into account that at the same time its supply may be 1.70 V, therefore the voltage drop allowed will be 0.37 V (1.70 V – 1.33 V). If the total leakage current is 30 µA, the pull-up resistor shall be less than 12.3 kΩ (0.37 V / 30 µA).

ANNEX B - Information for Socket Design (informative)

B.1 Power Pin Maximum Current

The maximum current of power per pin is 1.2 A of constant DC.

B.2 Contact Resistance Target

The contact resistance is determined by the characteristics of the socket contact and the device pin. The socket design has a considerable effect on the contact resistance. To reduce voltage drop, the socket should be designed to reduce the contact resistance as small as possible. The contact resistance may be defined by an initial value and its variation across time because of device aging. According to the result of A.3, the target contact resistance is less than 50 mΩ for the lifetime of the system.

B.3 Spacing for TIM

XFM form factor secures a space for heat dissipation on the bottom surface between the first row and the second row. The socket should be designed so that there is enough space for the TIM, so that the TIM can be directly connected between the device's surface and the Host PCB.

ANNEX C - Information for System Design (informative)

C.1 Connection between Host and Device

Figure C. 1 show signal connectivity between the host and the device. Symbol C denotes two AC coupling capacitors for the differential data pair. AC coupling capacitors for both upstream and downstream lanes are mounted on the host PCB. AC coupling capacitors for downstream are placed close to the socket. Symbol R denotes a pull-up resistor.

PWR_1 is connected to 2.5 V power supply. PWR_2 is connected to 1.2 V power supply.

The pull-up voltage V_{PU} for **CLKREQ#** is connected to 1.8V by host. An external level shifter may be used to support 3.3V signaling.

The two reserved pins on the second row are left open.

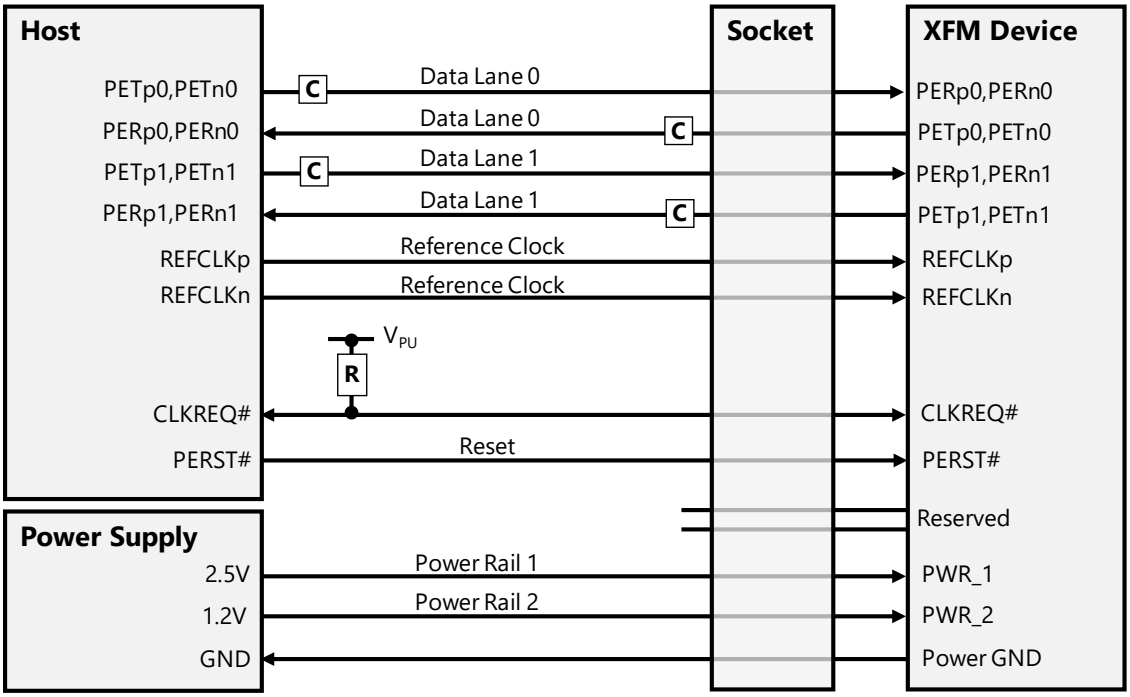

Figure C. 1 – Connection between Host and Device

C.2 Heat Dissipation Example Using TIM

Some space is secured between the first row and the second row of the XFM form factor. Figure C. 2 shows an example usage of this space for heat dissipation using TIM that improves heat transfer. A side of TIM surface is attached on Host PCB and the other side of surface is directly contacted to the device's surface when the device is in the socket.

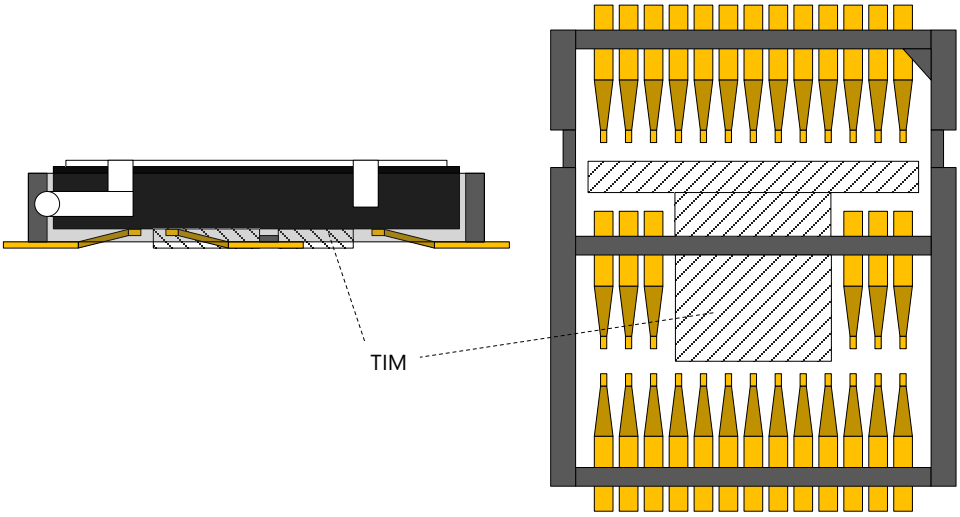

Figure C. 2 – An Example of Heat Dissipation Using TIM

ANNEX D - Reference of Device Test Standards (informative)

D.1 Environmental Testing

- Test Methods - JESD22 series, IEC 60068-2 series

Table D. 1 – Typical Reference of Environmental Testing Standards

JESD22		Correspondence to IEC 60068-2	
A103	High Temperature Storage life	60068-2-2	Dry Heat
A104	Temperature Cycling	60068-2-14	Change of temperature
A105	Power and Temperature Cycling	60068-2-30	Damp heat, cyclic
A107	Salt Atmosphere	60068-2-11	Salt mist
A119	Low Temperature Storage Life	60068-2-1	Cold
B103	Vibration, Variable Frequency	60068-2-6	Vibration(sinusoidal)
B104	Mechanical Shock	60068-2-31	Rough handling shocks
B110	Mechanical Shock - Component and Subassembly	60068-2-27	Shock

D.2 X-ray Testing

- X-Ray resistance requirement are specified in ISO/IEC 7816-1:(2011) for integrated circuit cards with contacts. Its test methods are specified in ISO/IEC 10373-1:(2006).

D.3 ESD Testing

- HBM - Electronic Product IEC61000-4-2
- CDM - Component Level ANSI/ESDA/JEDEC JS-002-2014

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