JEDEC PUBLICATION

FOUNDRY PROCESS QUALIFICATION GUIDELINES – TECHNOLOGY QUALIFICATION VEHICLE TESTING

(Wafer Fabrication Manufacturing Sites)

JEP001-3B

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FOUNDRY PROCESS QUALIFICATION GUIDELINES – TECHNOLOGY QUALIFICATION VEHICLE TESTING
(WAFER FABRICATION MANUFACTURING SITES)

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Foreword

This publication is part of a series of 3 documents providing methodologies for the minimum set of measurements to qualify a new semiconductor wafer process: back end of line (JEP001-1), transistor level (JEP001-2), and technology qualification vehicle testing (JEP001-3). The document provides methodologies for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to silicon-based technologies. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g., wide bandgap.

Any qualification requirements beyond the minimum set are to be developed for the specific performance expected of the technology. The minimum set of measurements and the requirements for the qualification based on those measurements are to be determined between the foundry and its customers on an individual basis. The process technology owner (foundry) will be required to document the details of specific testing unique to the process being qualified.

The guideline documents common best practices in the semiconductor industry and updated in accordance to advancement in the semiconductor industry and JEDEC bylaws of periodic reviews.

Introduction

This publication, was originally published as JP-001 entitled 'Foundry Process Qualification Guidelines', it was co-sponsored by JEDEC and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification methodologies. The JEDEC sponsoring committee is JC-14 through its JC-14.2 subcommittee on wafer level reliability.

This document encompasses and references a number of other standards and procedures, some of which are in a state of constant revision and update. While a case might be made for producing a lean, concise guideline that does not spell out specific procedures or requirements, the proposition of spelling out the essence of a comprehensive set of methodologies in one place has a practical value that outweighs the case for simplicity.

This publication is split into three parts: JEP001-1, JEP001-2, and JEP001-3 as described below. It is intended that each part references the appropriate tests. This standard should be read alongside reliability requirements established between the supplier and customer.

The structure of the JEDEC JEP001 series as currently conceived is as follows:

Part 1 – Backend of Line
Part 2 – Transistor-level
Part 3 – Technology Qualification Vehicle Testing

Acronyms

The following acronyms are used in this document.

ASIC	Application Specific Integrated Circuit
AF(T,V)	Acceleration Factor
AF(T)	Temperature Acceleration Factor
AF(V)	Voltage Acceleration Factor
BGA	Ball Grid Array
CDF	Cumulative Distribution Function
CDM	Charged Device Model
C.L.	Confidence Limit
DPPM	Defect Parts per Million
eNVM	Embedded Non-Volatile Memory
ESD	Electro-Static Discharge
FMEA	Failure Mode and Effects Analysis
GOX	Gate oxide (also used for gate dielectric)
HAST	Highly Accelerated Stress Test
HBM	Human Body Model
HD	High Density (SRAM, logic library)
HC	High Current (SRAM)
HP	High Performance (logic library)
HTOL	High Temperature Operating Life
I_{DDQ}	Quiescent Supply Current
MIM	Metal-Insulator-Metal
MSL	Moisture Sensitivity Level
NVM	Non-Volatile Memory
PLC	Programmable Logic Controller
PLL	Phase Locked Loop
SRAM	Static Random Access Memory
TC	Temperature Cycling
THB	Temperature Humidity Bias
T_{USE}	Temperature during use
T_{STRESS}	Temperature during stress
TQV	Technology Qualification Vehicle
V_{CC} / V_{DD}	Voltage applied to power supply pins
V_{CC_STRESS} / V_{DD_STRESS}	Vcc / VDD during stress
$V_{CC\_OPERATING}$ / $V_{DD\_OPERATING}$	Vcc / VDD during operation
V_{CC_NOM} / V_{DD_NOM}	Nominal Vcc / VDD during operation
V_{CC_MAX} / V_{DD_MAX}	Maximum Vcc / VDD during operation
xRAM	Alternative Random Access Memory

FOUNDRY PROCESS QUALIFICATION GUIDELINES – TECHNOLOGY QUALIFICATION VEHICLE TESTING (WAFER FABRICATION MANUFACTURING SITES)

(From JEDEC Board Ballot JCB-24-25, formulated under the co-sponsorship of the JC-14.2 Subcommittee on Wafer Level Reliability.)

1 Scope

This document describes test and data methods on technology qualification vehicles for the qualification of semiconductor technologies. It does not give pass or fail values or recommend specific test equipment, test structures or test algorithms. Wherever possible, it references applicable JEDEC, such as JESD47, or other widely accepted standards for requirements documentation.

There are two levels of qualification described. Level 1 is a pure process qualification intended to find reliability weaknesses. It primarily addresses technology wear-out mechanisms through package or wafer level reliability tests on specially designed test structures.

Level 2 demonstrates the reliability of the process that corresponds to the reliability demands from projected or known applications. Level 2 testing can be implemented via the testing of a relevant functional technology qualification vehicle (TQV), including life test.

Level 1 tests are described in JEP001-1 and JEP001-2, for back-end-of-line and transistor-level, respectively. This document describes Level 2 tests and requirements for a technology qualification vehicle.

2 Quality System

It is the responsibility of the foundry to have the appropriate quality system in place with special emphasis on issues relating to equipment capability, maintenance and calibration, continuous improvement and process control. In particular, a functioning SPC methodology should be demonstrated for all key processes (see EIA/JEDEC EIA-557A). As a minimum the foundry will have ISO9001 certification. The ISO9001 audit results by a third party and subsequent corrective actions on deficiencies shall be made available to the customer upon request. For those supplying to automotive applications, the foundry may also have to demonstrate requirements from the IATF TS 16949 standard to meet the needs of these products.

3 Responsibilities

3.1 Design and Implementation

In general, the foundry is responsible for the design and implementation of the Level 2 test vehicle (e.g., SRAM or pilot product) – see clause 8 for test vehicle requirements. For the special case of a foundry customer driving process development, or where the customer requires TQV data before such a vehicle becomes available, development of the Level 2 test vehicle may be shouldered in whole or in part by the customer. The foundry, customer or third party test vendor may execute the Level 2 (TQV) tests and requisite failure analysis. The foundry will be responsible for suggesting and implementing corrective action based on the failure analysis results. The qualification report shall adhere to the minimum reporting requirements and format described in this document.

While it is expected that a particular foundry methodology may differ from the methods outlined in this document, the wafer foundry should demonstrate to the customer that it has satisfactorily addressed all issues of interest. The wafer foundry should therefore provide a documented procedure and supporting data that provide an assessment of potential failure and wear-out mechanisms.

3.2 Reporting Requirements

Specific reporting requirements are included for the tests catalogued in this document. General reporting requirements include appropriate signoff, archiving and revision control, and the inclusion of supporting documents as appropriate.

The Level 2 qualification report shall include: (1) qualification plan, (2) description of the technology qualification vehicle (TQV), (3) test description and specification, (4) pass/fail criteria (5) test results and analysis including failure rates and (6) FA results.

4 Qualification Material

Qualification material should be sampled from a minimum of 3 non-consecutive wafers lots processed using the baseline process with adequate staggering through critical process steps, such that it is representative for production. A wafer lot is a quantity of wafers that are processed together as a batch under nominally controlled process conditions and within normal process operating parameters and control monitors. The batch is processed through matched equipment using the same or matched conditions, materials and methods. Typical sample sizes per lot are given in the individual test descriptions. Where applicable, confidence limits for each test population should be calculated. A conservative estimate of 40 die per wafer was made in determining sample size for tests that required the usage of all dies on the wafer.

Note 1 If more than a single set of equipment is used for qualification, then lots should represent various process tools and times.

Note 2 Lots should be sampled and verified to represent normal process variation for qualification. Skewed lots are not to be used for qualification and are used to set the process control parameters and limits.

5 Use of Packages

Packages with a wire-bonded die that are capable of higher temperatures are generally used for testing of the technology qualification vehicle (TQV) or pilot product. A qualification report for the standard wire-bonding process should be included. Advanced packaging (e.g., BGA, flip-chip or chip-scale) may be substituted where applicable. This, in combination with TC and THB tests, will demonstrate the assembly capability of this wafer fab process.

All references to temperature in the following sections imply junction temperature unless otherwise specified.

6 Reference Documents

6.1 Industry Standard Documents

The following reference documents contain provisions that, through reference in this text, constitute provisions of this document. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based in this publication are encouraged to investigate the possibility of applying the most recent editions of the reference documents indicated below. For undated references, the latest editions of the reference document referred to applies. Check the JEDEC website at http://www.jedec.org.

6.1.1 Reliability Assessment Methodology

JEDEC JEP70, *Quality and Reliability Standards and Publications.*
JEDEC JEP132, *Process Characterization Guidelines.*
JEDEC JEP143, *Solid State Reliability Assessment and Qualification Methodologies.*
JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.*
JEDEC JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms.*
JEDEC JESD94 *Application Specific Qualification Using Knowledge Based Test Methodology*
JEDEC JESD659, *Failure-Mechanism-Driven Reliability Monitoring.*
JEDEC JEP131, *Process Failure Mode and Effects Analysis (FMEA).*
AEC Q100, *Failure Mechanisms Based Stress Test Qualification for Integrated Circuits.*

6.1.2 Endurance Tests

IPC/JEDEC J-STD-020, *Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices.*
JEDEC JESD22-A101, *Steady State Temperature Humidity Bias.*
JEDEC JESD22-A104, *Temperature Cycling.*
JEDEC JESD22-A108, *Temperature, Bias and Operating Life.*
JEDEC JESD22-A110, *Highly Accelerated Stress Test (HAST).*
JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices prior to Reliability Testing.*
JEDEC JESD47, *Stress-Test Driven Qualification of Integrated Circuits.*
JEDEC JESD50, *Special Requirements for Maverick Product Elimination.*
JEDEC JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.*
JEDEC JESD85, *Methods for Calculating Failure Rates in Units of FITs.*

6.1.3 Electronic Discharge Tests

ANSI/ESDA/JEDEC JS-002-2018, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components*.
ANSI/ESDA/JEDEC JS-001-2017, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM).*

6.1.4 Latch-up Test

JEDEC JESD78, *IC Latch-Up Test.*

6.1.5 Quality Standards

EIA-557, *Statistical Process Control Systems.*
EIA-670, *Quality System Assessment*.
ISO 9001:2000, *Quality Management Systems – Requirements.*
JEDEC JESD671, *Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems).*

6.2 Selected References

Meeker, Q.A. and L.A. Escobar, *Statistical Methods for Reliability Data,* John Wiley, 1998.

Tobias, P.A. and D.C. Trindade, *Applied Reliability,* 2nd Ed., CRC Press, 1995.

Nelson, Wayne, "Accelerated Testing: Statistical Models, Test Plans, and Data Analyses", in *Wiley Series in Probability and Mathematical Statistics-Applied Probability,* John Wiley, 1990.

Amerasekera, E.A. and F.N. Najm, *Failure Mechanisms in Semiconductor Devices,* 2nd Ed., John Wiley, 1997.

Ohring, Milton, *Reliability and Failure of Electronic Materials and Devices,* Academic Press, 1998.

Yue, John, "Reliability", in C.Y. Chang and S.M. Sze (eds.), *ULSI Technology,* McGraw-Hill, 1996, Chapter 12.

Amerasekera, E.A. and Charvaka Duvvury, *ESD in Silicon Integrated Circuits,* John Wiley, 1996.

IRPS Conference Proceedings and Tutorials are an excellent source of information on current test methodologies and reliability models. (Web site www.irps.org)

Microelectronics Reliability, Pergamon Press. This journal publishes the proceedings of ESREF, the European equivalent of IRPS, along with frequent review papers.

7 Qualification Test Summary

Clause	Procedure	JEDEC Reference Standard(s)	Other Standards	Q or E (see NOTE)
9	Long Term Life Tests (HTOL)	JESD47, JESD22-A108, JESD85, JEP122	AEC Q100	Q
10	Early Life Test	JESD47, JESD22-A108, JESD74, JEP122	AEC Q100	Q
11	Temperature Cycling (TC)	JESD47, J-STD-020, JESD22-A113, JESD22- A104, JEP122	AEC Q100	Q
12	Temperature Humidity Bias (THB) or Highly Accelerated Stress Test (HAST)	JESD47, J-STD-020, JESD22-A113, JESD22- A101, JESD22-A110, JEP122	AEC Q100	Q
13	ESD Characterization	JESD47, JS-001, JS-002	ANSI/ESD: STM5.1, STM5.2, AEC Q100	Q
14	Latch-up Characterization	JESD47, JESD78	AEC Q100	Q

NOTE Q means qualification; E means engineering. The difference between qualification tests and engineering tests are that engineering tests are done for information only; engineering tests, therefore, do not have a pass/fail criterion.

8 Technology Qualification Vehicle (TQV) Requirements

An appropriate technology qualification vehicle is used to evaluate the expected early-life and long-term failure rate of the process. For defect density-based evaluations, both overall die area and representative circuit design density/complexity at the respective lithographic node are needed to demonstrate the process reliability.

For general applications, an overall TQV area requirement is a recommended starting point and alternate areas may be justified by technology envelope and application. See Table 1 for recommended area requirements, based on industry best practice. Additionally, different sample sizes may be required to achieve equivalent process and multiple TQV's may be pooled to obtain an overall area coverage.

SRAM arrays are an excellent basis for a TQV but do not exercise all design rules or parametric and circuit cases. Therefore, a TQV consisting of SRAM only may miss specific reliability concerns. Test chip content with alternate circuits, layout, density, and sensitivity representative of product usage or targeted to specific reliability risks may be required, either monolithically or through additional distinct TQVs. Additional components to consider for addressing these specific risks are listed in Table 2.

Table 1 – Recommended TQV Area

Device	Cell type	Device area	Qualification / Engineering	Notes
SRAM	High density (HD) + High current (HC)	~12 mm^2	Q	• HC area combined with HD. • Bit-cell footprint area only. • Device area recommendation is based on industry best practice. • Device area should match intended use in products.

Table 2 – Additional TQV Components to Consider

Device	Cell type
Logic	HP (high-performance) library HD (high-density) library
Alternative memories	eNVM, xRAM
Analog	Relevant analog, e.g., PLL, PLC
Passives	MIM capacitor, thin film resistor, etc.
Register file	Two port SRAM

9 Long Term Life Tests

The usefulness of a life test is dependent on an assessment of the dominant failure modes, as determined from a prior thorough analysis of failure modes (FMEA). See JEDEC publication JEP131.

9.1 Operating Life Test Requirements

Reference procedures	JEDEC JESD47, *Qualification Methods.* JEDEC JESD22-A108, *Temperature, Bias, and Operating Life.* JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.* JEDEC JESD85, *Methods for Calculating Failure Rates in Units of FITs.* JEDEC JEP148B, *Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment.*
Vehicle	Appropriate technology qualification vehicle (TQV) in component form.
Method	Per JESD22-A108, with: **Stress:** • Bias Life with 125 ºC < T_J < 175 ºC. • Full functional burn-in with f > 100 kHz • Voltage; see discussion under per circuit bias configuration • Total stress hours: use either; a) 1000 -0/+8 hrs at minimum V_{CC_STRESS}, or b) Scaled from 1000 hrs. based on acceleration for $V_{CC\_STRESS} > V_{CC\_OPERATING}$ and 500 -0/+8 hrs at minimum under any V_{CC_STRESS} • Test points at 0, 48, 168, 500 and 1000 hrs (or appropriately scaled to the end of stress). A higher ambient temperature may be used to reduce the required total stress hours. Care should be taken to ensure that the case and junction temperatures are within the applicable range for the process and package. **Drift Analysis (optional):** For a statistically significant sample of devices per lot, serialize devices. • Option #1: Take read and record data of key parameters drift (most sensitive to drift) at 0, 48, 168 and 500 hrs. • Option #2: Take read and record data of key parameters drift at suitable intervals. Analyze data to determine potential drift and report in tabular or graphical form for each parameter. Always compare drifts to estimates from reliability aging simulations.
Circuit bias configuration	$V_{CC\_STRESS} = \lambda V_{CC\_OPERATING}$, where V_{CC_STRESS} must not exceed the device functional limits The minimum λ allowed is 1, but may range up to that tolerated for a stress period without artificially damaging the devices under test. λ typically ranges up to 1.4. NOTE 1 Unless otherwise specified, the operating voltage is the maximum operating voltage specified for the device. NOTE 2 The voltage acceleration model should be obtained from specific failure data for the product under test. NOTE 3 The nomenclature V_{CC}, or alternatively V_{DD}, refers to the voltage(s) applied to the power supply pins.

9.1 Operating Life Test Requirements (cont'd)

Criteria for failure	Full functional test and, where appropriate, I_{DDQ} and leakage tests.
Failure analysis	Root cause analysis should be pursued for all failure types to substantiate models applied and as an opportunity for improvement actions.
Model to be used	Per JESD74 and JESD85: **Acceleration factor:** Total acceleration factor $AF(T,V) = AF(T) * AF(V)$ a) Temperature Acceleration, AF(T) - Arrhenius model for temperature acceleration factor (AF(T)): $AF(T) = exp(E_A/k[(1/T_{USE})-(1/T_{STRESS})])$ - T_{USE} and T_{STRESS} are junction temperatures in degrees kelvin. - k = Boltzmann's constant = 8.62×10^{-05} eV/K - Activation energy E_A is to be determined by failure mechanism. (see JEP122 as one reference) or as a composite behavior for the population (with justification). b) Voltage Acceleration, AF(V) - The correct voltage acceleration factor is to be derived for the product being stressed. The following models may be used: $AF(V) = exp(\alpha (V_{CC\_STRESS} - V_{CC\_OPERATING})$ **or** $AF(V) = exp (V_{CC\_STRESS} - V_{CC\_OPERATING})^n$ **Failure rate:** <u>Decreasing or generalized distribution of failures</u>: Use a Weibull model; other models may apply with justification. This can often mean normalizing end of stress data to an equivalent use condition and lifetime to arrive at the appropriate device failure rate. <u>Constant distribution of failures</u>: The FIT rate should be calculated using Chi-Square statistics at 60% confidence limits. $\lambda = \chi^2(x,\nu) / (2N * AF * t_{STRESS})$ where: $\chi^2(x, \nu)$ = Chi Square at (x, ν), from Chi Square tables x = (1-C.L.) and ν = (2r+2) C.L. = Confidence limit r = # of rejects N = Total sample size AF = Acceleration factor t_{STRESS} = Total stress time NOTE 1 For the purpose of calculating the temperature acceleration factor, T_{USE} is typically NOT the maximum operating temperature. Rather, it represents an average junction temperature over the life of the product. Typical values of T_{USE} are 55 °C (consumer), 70 °C (commercial), and 85 °C (industrial). NOTE 2 There is no universally agreed value of E_A to be used for temperature acceleration of product failures. In the absence of a reliable model, a value of E_A = 0.7 eV has historically been used. It is the responsibility of the technology owner to demonstrate that a conservative model is used.

9.1 Operating Life Test Requirements (cont'd)

Sample size	Follow option (a) or option (b): a) A minimum of 231 DUTs from 3 lots with no more than 90 DUTs from any one lot. b) In case a minimum failure rate needs to be proven, the sample size shall be increased. Approximately equal numbers of samples shall be selected from each of (at least) 3 lots. The target failure rate depends on application area.
Merit number	1. 0 failure tolerance is the standard per JESD47. 2. Report % failures for each lot at each read-out point and failure rate with an appropriate failure distribution model enabling extrapolation to use conditions.
Other data required	Standard Lot Data.

9.2 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. % failures for each lot at each read-out point.
5. Target defect density and failure rate requirements.
6. Calculated failure rates at the specified read-points.

NOTE The earliest part of the failure distribution (< 48 hrs if no voltage acceleration or equivalent at higher voltages) is excluded in the calculation of long term operating life. Specify the criteria and method of calculating failure rate.

7. Appropriate failure analysis reports.
8. Corrective actions taken.
9. Drift analysis results (optional).

10 Early Life Test

An appropriate technology qualification vehicle (TQV) is to be used to get a first view on the expected infant mortality rate of the process. The life period of interest is typically the first year or less.

NOTE It may be possible to utilize early data from the long term life test to fulfill the objective of this section.

10.1 Early Life Test Requirements

Reference procedure	JEDEC JESD47, *Qualification Methods.* JEDEC JESD22-A108, *Temperature, Bias, and Operating Life.* JEDEC JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components.* JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.* AEC Q100, *Failure Mechanisms Based Stress Test Qualification for Integrated Circuits.*
Vehicle	Appropriate technology qualification vehicle (TQV) in component form.
Method	Per JESD22- A108 with: • 125 ºC < Tj < 150 ºC, 48 hrs • Dynamic Burn-in with f > 100 kHz • Voltage; see discussion under per circuit bias configuration • Test Points: 0 hrs and 48 hrs. Intermediate readout points may be added as required. A higher ambient temperature may be used to reduce the required total stress hours. Care should be taken to ensure that the case and junction temperatures are within the applicable range for the process and package.
Circuit bias configuration	$V_{CC\_STRESS} = \lambda V_{CC\_OPERATING}$, where • V_{CC_STRESS} is at least V_{CCMAX} (V_{CCMAX} is often 1.1 x $V_{CC\_NOMINAL}$) • V_{CC_STRESS} must not exceed the device functional limits The minimum λ allowed is 1, but may range up to that tolerated for a stress period without artificially damaging the devices under test. NOTE 1 Unless otherwise specified, the operating voltage is the maximum operating voltage specified for the device. NOTE 2 The voltage acceleration model should be obtained from specific failure data for the product under test. NOTE 3 The nomenclature V_{CC}, or alternatively V_{DD}, refers to the voltage(s) applied to the power supply pins.
Criteria for failure	Full functional test and, where appropriate, I_{DDQ} and leakage tests.

10.1 Early Life Test Requirements (cont'd)

Model to be used	**Method 1: DPPM calculation** (from JESD74): $CDF = \chi^2 (x, \nu)/(2 \times N)$ where N = sample size χ^2 = Chi-squared statistic x = (1-C.L.) and ν = (2r + 2) C.L. – Confidence limit, typically 60% R = # of rejects N = Total sample size **Method 2: Failure rate calculation** (from JESD74 and JESD85): **Acceleration factor:** Total acceleration factor $AF(T,V) = AF(T) * AF(V)$ a) Temperature Acceleration, AF(T) - Arrhenius model for temperature acceleration factor (AF(T)): $AF(T) = exp(E_A/k[(1/T_{USE})-(1/T_{STRESS})])$ - T_{USE} and T_{STRESS} are junction temperatures in degrees kelvin. - k = Boltzmann's constant = 8.62×10^{-05} eV/K - Activation energy is to be determined by failure mechanism. (see JEP122 as one reference) or as a composite behavior for the population (with justification). b) Voltage Acceleration, AF(V) - If an experimentally validated alternative is absent, the following model is recommended: $AF(V) = exp[\gamma_v * (V_{STRESS} - V_{USE})]$ - γ_v is a voltage acceleration parameter - The value of γ_v is determined experimentally and may vary by failure mechanism. - If $V_{CC\_STRESS} = V_{CCMAX}$, then AF(V) = 1 **Failure rate:** <u>Decreasing or generalized distribution of failures</u>: Use a Weibull model; other models may apply with justification. This can often mean normalizing end of stress data to an equivalent use condition and lifetime to arrive at the appropriate device failure rate. <u>Constant distribution of failures</u>: The FIT rate should be calculated using Chi-Square statistics at 60% confidence limits. $\lambda = \chi^2(x,\nu) / (2N * AF * t_{STRESS})$ where: $\chi^2(x, \nu)$ = Chi Square at (x, ν), from Chi Square tables x = (1-C.L.) and ν = (2r+2) C.L. = Confidence limit r = # of rejects N = Total sample size AF = Acceleration factor t_{STRESS} = Total stress time

10.1 Early Life Test Requirements (cont'd)

Sample size	Approximately equal numbers of samples shall be selected from each of 3 lots (minimum). The sample size shall be sufficient to demonstrate the required early failure rate. For automotive applications the minimum required sample size is 800 per lot from 3 lots, per AEC Q100. JESD47K, table 5-2 contains minimum sample sizes to demonstrate various failure rate targets.
Merit number	Demonstration that the required early failure rate is met. For automotive applications, this is 0 fails out of 800 samples per lot, over 3 lots, per AEC Q100. Report: 1. Fraction failure for each lot at each readout point. 2. Total failures in DPPM (defective parts per million, Method 1 above) or the early failure rate derived from accelerated stress and quoted at a normalized use condition and early life point (Method 2 above).
Other data required	Standard lot data.

10.2 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. % failures for each lot at every readout point.
5. Total failures in DPPM (defective parts per million) at a projected number of use hours (e.g., 3000 hrs) under a stated use conditions of temperature, voltage, and any other primary variables
6. JESD74 describes appropriate interpretation of data to assess the early life failure rate. Included are descriptions for interpreting data when
   - the failure rate is decreasing (This is often the case for early life), or
   - the failure rate is constant (this can be rare where defects are a factor in early reliability).

Where the stress readout and the early life point of interest are not equivalent, proper interpretation methodology is especially critical.

11 Temperature Cycling Test

11.1 Temperature Cycling Test Requirements

Reference procedures	JEDEC JESD47, *Qualification Methods.* JEDEC JESD22-A104, *Temperature Cycling.* IPC/JEDEC J-STD-020, *Moisture level preconditioning.* JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices Prior to Preconditioning*. JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices*.
Test structures	Appropriate technology qualification vehicle.
Vehicle	Appropriate package.
Method	Preconditioning per appropriate MSL Level per J-STD-020 and JESD22-A113. Temperature Cycle per JESD47.
Circuit bias configuration	None (This test is unbiased.).
Criteria for failure	Per JESD47.
Model to be used	See JEP122.
Sample size	A minimum of 231 DUTs from 3 lots with no more than 90 DUTs from any one lot.
Merit number	0 failure tolerance is the standard per JESD47. If failures are observed, report distribution analysis and demonstrate the required failure rate is met.
Other data required	Standard Lot Data.

11.2 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. Sample size for each lot and the number of failures at each readout point
5. % failure.
6. Description of the plastic package (type, # pins, dimensions, lead-frame).

12 Temperature-humidity-bias (THB) / Highly Accelerated Stress Test (HAST)

Either THB or HAST is required.

12.1 THB / HAST Test Requirements

Reference procedures	JEDEC JESD47, *Qualification Methods.* IPC/JEDEC J-STD-020, *Moisture level preconditioning.* JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices Prior to Preconditioning.* JEDEC JESD22-A101, *Steady State Temperature Humidity Bias Life Test.* JEDEC JESD22-A110, *Highly Accelerated Stress Test (HAST).* JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices.*
Test conditions	Static bias = V_{CCMAX} (typically 1.1 x V_{CCNOM}) Biasing guidelines: See JESD22-A101 (THB) or JESD-A110 (HAST). • THB: 85 ºC/85% RH, 1000 hrs • HAST: 130 ºC, 85% RH, 96 hrs. For interim readouts, devices should be returned to stress within the time specified in JESD22-A101 or JESD22-A110.
Test structures	Appropriate technology qualification vehicle. If a dc test structure is designed it should be set up for minimum power dissipation under bias and maximum rated voltage for the technology (functional test structures will have transistor leakage).
Vehicle	Appropriate package.
Method	Preconditioning per appropriate MSL Level per JESD22_A113. Stress in either THB or HAST per JESD47.
Model to be used	See JEP122.
Sample size	A minimum of 231 DUTs from 3 lots with no more than 90 DUTs from any one lot.
Merit number	0 failure tolerance is the standard per JESD47. If failures are observed, report distribution analysis and demonstrate the required failure rate is met.
Other data required	Standard lot data.

12.2 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. Sample size for each lot and the number of failures at each readout point
5. Total failures in DPPM (defective parts per million).

13 Detailed Yield Results

Reference procedure	None.
Test parameters	Full functional test and I_{DDQ} and leakage tests.
Test structures	Appropriate technology qualification vehicle.
Vehicle	Wafer Probe.
Method	NA
Model to be used	Foundry will specify Yield Model.
Sample size	12 wafers from each of 6 lots.
Defect density	Defects per square centimeter.
Other data required	1. Area of SRAM or other qualification vehicle. 2. # of Critical Layers Used. 3. Site location information relative to edge exclusion zone.

13.1 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. Number of devices tested, devices passed and percent yield for each wafer tested.
5. Defect density per square cm.

14 ESD Characterization

The technology qualification vehicle (TQV) is used to get a first look at the ESD robustness of the process and product (especially I/O) design. As a minimum, human body model (HBM) test data should be collected. The inclusion of charged device model (CDM) data is highly recommended.

14.1 ESD Tests

Reference procedure	JEDEC JESD47 *Stress-Test Driven Qualification of Integrated Circuits.* ESDA/JEDEC JS-001 *Human Body Model ESD Test Method*. ESDA/JEDEC JS-002, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components*.
Test parameters	Full functional test and parametric (e.g., I_{DDQ} and leakage) tests.
Test structures	I/O and power pins of appropriate technology qualification vehicle.
Vehicle	Packaged TQV.
Method	Per JESD47.
Model to be used	None.
Sample size	Per JESD47.
Failure criteria	Per JESD47.
Merit number	Voltage level or classification per respective test method.
Other data required	Tester waveforms.

14.2 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. HBM ESD classification.

15 Latch-up Characterization

The technology qualification vehicle (TQV) is used to get a first look at the latch-up immunity of the process and ruggedness of the product design. This is a package level test.

15.1 Latchup Test

Reference procedure	JEDEC JESD47, *Qualification Methods.* JEDEC JESD78, *IC Latch-Up Test.*
Test parameters	Full functional test and parametric (e.g., I_{DDQ} and leakage) tests.
Test structures	I/O and power pins of appropriate technology qualification vehicle.
Vehicle	Packaged TQV.
Method	Method per specification. Per JESD78 and JESD47 if appropriate per technology or device under consideration.
Model to be used	None.
Sample size	Per JESD78 and JESD47 if appropriate per technology or device under consideration.
Failure criteria	Per JESD78 and JESD47 if appropriate per technology or device under consideration.
Merit number	Class (room and max temperature). Maximum passing current trigger and voltage trigger levels.
Other data required	Tester waveforms.

15.2 Report Requirements

These guidelines should not replace any existing agreements between customers and suppliers regarding specific information for reporting purposes.

1. Fab name and location; process name, lot #, wafer # and date code, and certification that material tested represents the current process being qualified.
2. Brief description of technology qualification vehicle: chip area, GOX area, circuit type (e.g., SRAM, ASIC), etc.
3. Test methodology and test coverage, test speed (frequency), I_{DDQ} limits.
4. Latch-up test conditions: Trigger test conditions, test temperature, failure criteria, functional test across datasheet limits.

Annex A (Informative) Differences between Revisions

A.1 Differences between JEP001-3B and JEP001-3A

The following list briefly describes most of the changes made to entries that appear in this publication, JEP001-3B, compared to its predecessor, JEP001-3A (September 2018).

Clause	Description of Change
Title	Title changed from "Product Level" to "Technology Qualification Vehicle Testing".
Forword	Updated the wording.
Introduction	Updated the wording.
Acronyms	Updated the list of acronyms.
Scope	Updated the wording in paragraph 4.
3	Subclause 3.1 deleted, 3.2 heading changed and 2nd paragraph deleted, 3.3 changed to 3.2.
4	Re-naming of clause 4 heading. Updated the requirements for qualification material, and the definition of a wafer lot. NOTE 1 and NOTE 2 added.
5	Removal of the paragraph on side brazed ceramic packages.
6	Updated the reference procedures and other references, keeping only those that are applicable to JEP001-3B. Subclause 6.1.5 removed. 6.1.6 renamed to 6.1.5.
7	Updated the table and added the NOTE.
8	Re-naming of clause 8 heading, clause 8 re-written, Table 1 and Table 2 added.
9 – 15	Subclauses 8.1 through 8.7 sequentially renamed clauses 9 through 15.
9	Updated the sample size / failure rate requirements, extrapolation model, and drift analysis requirements.
10	Updated the sample size / failure rate requirements.
11	Updated the failure rate requirements.
12	Updated the failure rate requirements.
14	Removed the reference to machine model (MM).
15	Update the report requirements item #4.

A.2 Differences between JEP001-3A and JEP001A

The following list briefly describes most of the changes made to entries that appear in, JEP001-3A (September 2018), compared to its predecessor, JEP001A (February 2014).

Clause	Description of Change
All	JEP001A split into 3 parts; JEP001-1A, Backend of Line, JEP001-2A, FEOL END Transistor Level, and JEP001-3A, Product Level.

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Standard Improvement Form **JEDEC** **JEP001-3B**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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2. Recommendations for correction:

_____

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3. Other suggestions for document improvement:

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