JEDEC PUBLICATION

Guidelines for Representing Threshold Voltage of SiC MOSFETs in Datasheets

Version 1.0

JEP202

JANUARY 2025

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by
©JEDEC Solid State Technology Association 2025
3103 10th Street North
Suite 240S
Arlington, VA 22201

PRICE: Contact JEDEC

Printed in the U.S.A.

For information, contact:

JEDEC Solid State Technology Association
3103 10th Street North
Suite 240S
Arlington, VA 22201
https://www.jedec.org/contact

This page intentionally left blank.

GUIDELINES FOR REPRESENTING THRESHOLD VOLTAGE OF SIC MOSFETS IN DATASHEETS, VERSION 1.0

Contents

Figures

Foreword

This document was drafted by JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use in the SiC power semiconductor and related power electronic industries, and provides guidelines for representation of threshold voltage and transfer characteristic of SiC MOS device in datasheets.

Introduction

Threshold voltage is the key parameter defining operation of Field Effect Transistors. Measurement and/or definition of the threshold voltage in the datasheet can have a significant influence on the interpretation of the device characteristics by user. Clear parameter definition and the standardization of the test methodology would greatly simplify comparison of different SiC products available on the market, as well as evaluation of such devices in different application topologies utilizing numerical simulations.

The purpose of this document is to list the factors that can influence threshold voltage and associated with it transfer characteristic of silicon carbide (SiC) Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) or any other Metal-Oxide-Semiconductor (MOS) gated devices, such as and Insulated Gate Bipolar Transistors (IGBTs), as well as to provide guidelines for a clean representation of such characteristics in datasheets.

GUIDELINES FOR REPRESENTING THRESHOLD VOLTAGE OF SIC MOSFETS IN DATASHEETS, VERSION 1.0

(From JEDEC Board ballot JCB-24-51, formulated under the cognizance of the JC-70.2 Subcommittee on SiC Power Electronic Conversion Semiconductor Standards.)

1 Scope

Threshold voltage V_T is the one of most important parameters of MOS device. V_T knowledge is vital for system designers, since it defines switching behavior of the device. Typically, in the datasheets it is defined as the gate voltage at which the drain current crosses certain threshold value. Often V_T is also measured under conditions that do not occur in real-world applications. In some cases, a fixed low V_{DS} is used as the test condition, but usually measured with gate and drain shorted together. Such definition of threshold voltage has not much use for system designers. In addition, and with focus on SiC-based MOS devices, threshold voltage depends strongly on measurement setup and pre-conditions as well which needs be considered during evaluating and comparing switching behavior of devices.

This document focuses on the features of silicon carbide MOS gated devices and their implications on device threshold voltage. To maximize the quality and especially practical worth of the data sheet data, the guidance for threshold voltage representation in such documents is provided.

2 Normative References

The following normative documents contain provisions that, through reference in this text, constitute provisions of this standard. For dated references, subsequent amendments to or revisions of any of these publications do not apply. However, parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated. For undated references, the latest edition of the normative document referred to applies.

[1] JEP183 “Guidelines for Measuring the Threshold Voltage (V_T) of SiC MOSFETs”, January 2021.

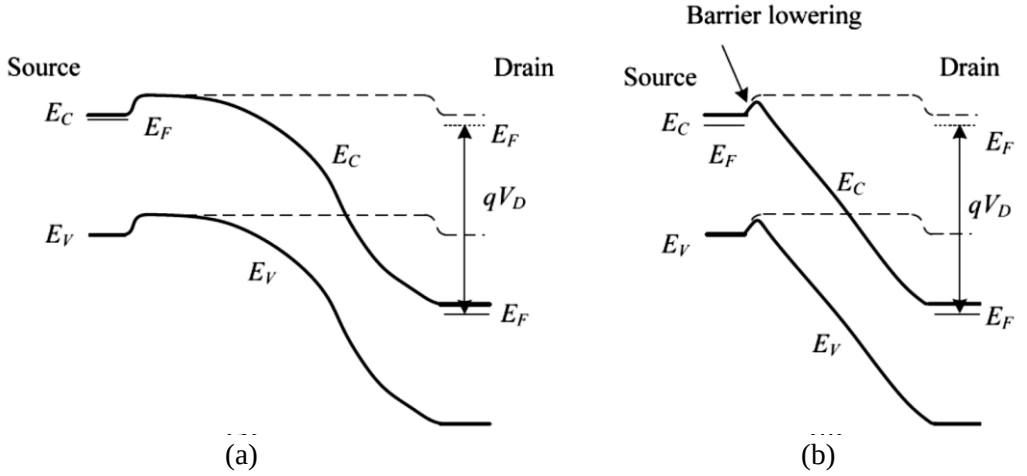
3 Terms, Definitions and Letter Symbols

DUT	Device Under Test
V_{GS}	Gate-source voltage applied to the DUT
V_{DS}	Drain-source voltage applied to the DUT
V_T	Threshold voltage
I_D	Drain current
T_{JM}	Maximum rated temperature of the DUT
DIBL	Drain Induced Barrier Lowering
SCE	Short Channel Effect

4 Description of DIBL Effect in SiC MOSFETs

Threshold voltage (V_T) is a fundamental parameter of FET transistors defined as the gate voltage at which significant drain current (I_D) begins to flow. In SiC MOSFET datasheets this value is typically defined as the gate voltage needed to achieve drain current of several mA when drain to source voltage (V_{DS}) is kept at relatively small (e.g., 0.1 V – 10 V) [1].

Due to low inversion channel mobility, commercial SiC MOSFETs are designed with a relatively short channels to minimize channel resistance. As the channel length of SiC MOSFETs is reduced to sub micrometer level, the decrease of threshold voltage is observed. This is due to the charge sharing between the drain/source region and the channel, and also due to high electric fields in the channel region. This effect is known as short channel effect (SCE). SCE includes the threshold voltage lowering due to high drain bias, so-called drain induced barrier lowering (DIBL) effect, and can be severe in power devices. DIBL effect arises as a result of two-dimensional potential distribution and high electric fields in the channel region. When the source and drain depletion regions are a substantial fraction of the channel length, short-channel effects start to occur. Once the sum of these depletion widths approaches the channel length, a condition called punch-through occurs. This is due to the lowering of the barrier near the source which results in the leakage drain current increase. This current is a strong function of the drain bias. For a long channel device, a drain bias can change the effective channel length, but the barrier at the source end remains unaffected as shown in Figure 1(a).



NOTE Dashed line is for $V_{DS} = 0$ and solid line is for $V_{DS} > 0$ [2].

Figure 1 — Energy-band Diagram at the Semiconductor Surface from Source to Drain, for (a) Long-channel MOSFET and (b) Short-channel MOSFET showing DIBL Effect

But in a shorter channel device (like SiC MOSFET), the drain bias can influence the barrier at the source end in Figure 1(b), such that the channel carrier concentration at that location is no longer fixed. This lowering of the source barrier causes an injection of extra carriers, which can result in a substantial increase in drain current. High leakage current potentially can limit the device operation for short channel MOSFETs during operation at high V_{DS}. In addition, DIBL effect reduces threshold voltage of the MOSFET, which, in turn, impacts switching behavior of the device. Depending on V_{DS} such V_T reduction can alter device switching performance, as well as lead to unwanted effects such as dynamic shoot-through.

4 Description of DIBL Effect in SiC MOSFETs (cont'd)

DIBL effect might vary for different design/technologies. Example of V_T vs. V_{DS} dependence is shown in Figure 2 [3], clearly indicating different dependence for different commercial products.

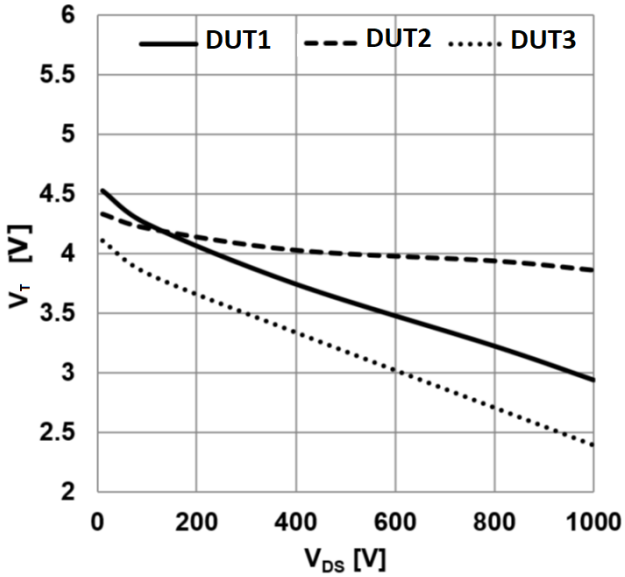


Figure 2 — V_T at 10 mA over Drain-source Voltage for Different SiC MOSFET Manufacturers, 1200 V Device Class

Thus, it is crucial to correctly depict V_T dependence on DIBL effect in the datasheets of SiC MOSFET devices. As mentioned above, MOSFET's threshold voltage value depends on current this parameter is tested at, so having one V_T value in the datasheet might be insufficient for fair comparison of different products.

4 Description of DIBL Effect in SiC MOSFETs (cont'd)

Figure 3 [4] shows an example of SiC MOSFET's transfer characteristics obtained at different V_{DS}.

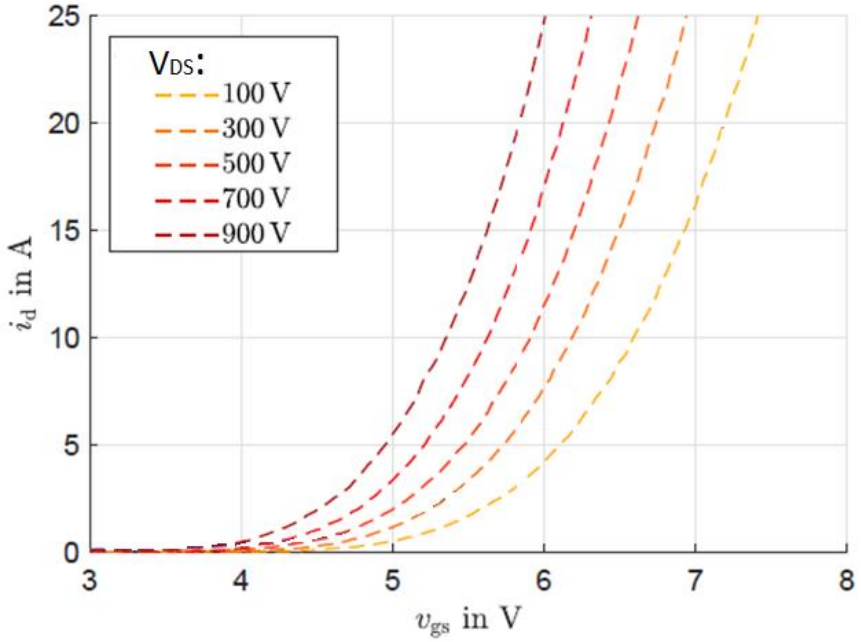


Figure 3 — Transfer Characteristics of SiC MOSFET for Different V_{DS} Voltages

As depicted above, increase of the drain voltage alters the whole transfer characteristic of the MOSFET. Also, it is obvious that V_T value and it is change strongly depends on I_D. To mitigate foreseen discrepancies in V_T representation and simplify comparison of different commercial products, it is recommended to depict the whole transfer characteristics at different drain voltages in SiC MOSFET datasheets.

5 Representation Guide

As outlined above, threshold voltage of a SiC MOSFET is strongly influenced by the choice of test condition, such as drain current and drain voltage. V_T of SiC IGBTs is expected to behave similarly. Therefore, it is important that different set of these test conditions was documented in a device datasheet. As the test conditions impact V_T value as typically defined, e.g., as the gate voltage needed to achieve drain current of several mA when drain to source voltage (V_{DS}) is kept at relatively small (e.g., 0.1 V – 10 V), as well as transfer characteristics shown in Figure 3, the measurement has to be performed in accordance with JEP183 "Guidelines for Measuring the Threshold Voltage (V_T) of SiC MOSFETs" [1]. Therefore, a device datasheet needs to document the following test conditions:

- Applied V_{GS} value used for conditioning
- Pulse length used for applying the conditioning V_{GS} value
- Device temperature at which V_T is determined

If a typical measurement of V_T at low V_{DS} values is used, the following parameters shall be specified:

- Threshold current I_D that was used to determine V_T

As in this case, V_T is given for a single specific measurement point, the above mentioned V_T value and test conditions might be shown in a table.

In addition to V_T at low V_{DS}, the interaction of V_T and V_{DS} should be visualized in datasheet. For this purpose, three approaches are exemplarily described.

1st approach - Threshold voltage as part of transfer characteristics:
An example of the transfer characteristics representation is shown in Figure 4.

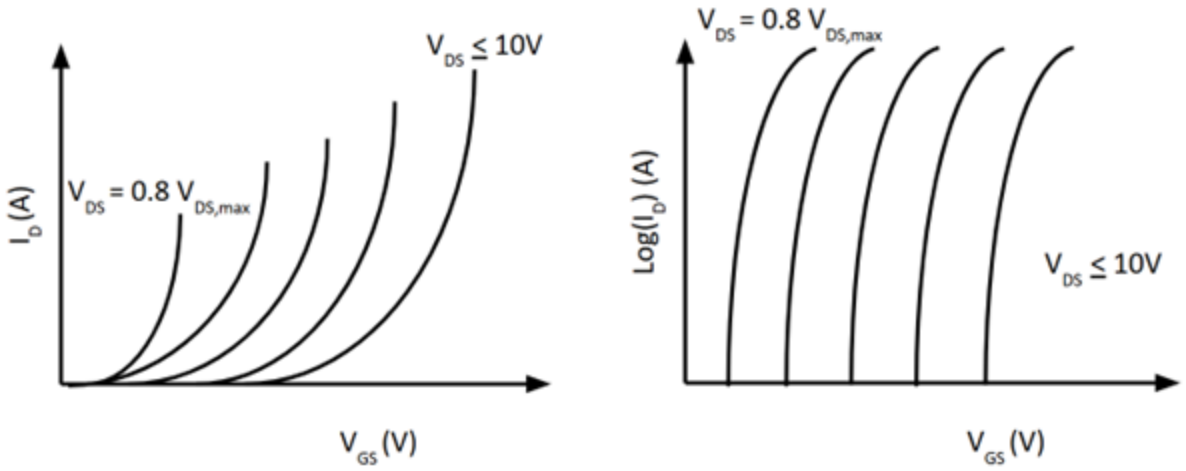


Figure 4 — Exemplary Drawing of the Transfer Characteristics Obtained at Different V_{DS}

It is recommended to measure such characteristics at different drain-source voltages ranging from very small (e.g., 0.1 V – 10 V) to at least 80% of maximum rated voltage. The characteristics in between should correspond to intermediate V_{DS} values increasing from the smallest V_{DS} in some discrete steps.

5 Representation Guide (cont'd)

While it is recommended, for user's sake, to measure such characteristics up to typical drain currents, the applied conditions definitely should not exceed maximum rating of the device. As a minimum room temperature drain characteristics should be presented in the datasheet. Inclusion of the same characteristics tested at elevated temperatures as well as representation of the drain current in logarithmic scale (Figure 4(b)) is also encouraged.

2nd approach - Threshold voltage versus applied drain-source voltage:
An example of the threshold voltage dependence on the drain voltage depicted in Figure 5.

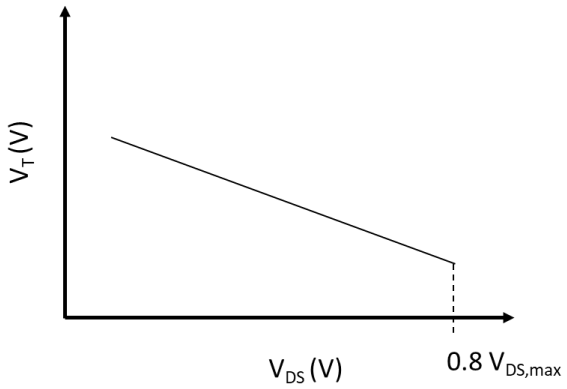


Figure 5 — Exemplary Drawing of the Threshold Voltage vs. Different V_{DS} (Constant I_D)

Similar to transfer characteristic, it is recommended to measure threshold voltage at different drain-source voltages ranging from very small (e.g., 0.1 V – 10 V) to at least 80% of maximum rated voltage. The V_T values have to be obtained at the same drain current I_D. Depiction of V_T tested at elevated temperatures in the same or separate plots (Figure 4(b)) is also encouraged.

3rd approach - Threshold voltage versus applied drain-source voltage at discrete voltage values:
Alternatively, to the 1st and 2nd approach, the interaction of V_T and V_{DS} might be given as tabular values. In this case, V_T shall be specified at the follow V_{DS} values:

- Very small V_{DS} value, e.g., 0.1 V – 10 V
- V_{DS} value used for the characterization of dynamic device properties
- V_{DS} value corresponding to a least 80% of maximum rated voltage

Statement on V_T at elevated temperatures in the same way is also encouraged.

In some cases, testing up 80% of maximum rated voltage and typical drain currents might be limited by used equipment. In this situation it is recommended to provide sufficient data, so extrapolation can be used to estimate V_T beyond values specified in a datasheet.

Annex A (Informative) References

[2] K. N. Ratnakumar and J. D. Meindl, “Short-Channel MOST Threshold Voltage Model,” IEEE Journal of Solid State Circuits, vol. 17, pp. 937-948, October 1982.

[3] T. Basler et al, “Practical Aspects and Body Diode Robustness of a 1200 V SiC Trench MOSFET”, PCIM Europe 2018, Nuremberg, Germany, June 2018.

[4] P. Hofstetter et al, “Influence of the Threshold Voltage Hysteresis and the Drain Induced Barrier Lowering on the Dynamic Transfer Characteristic of SiC Power MOSFETs”, Proc. APEC 2019, pp. 944-950, March 2019.

This page intentionally left blank.

Standard Improvement Form **JEDEC JEP202**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 10th Street North
Suite 240S
Arlington, VA 22201

Email: angies@jedec.org

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC®