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Guidelines for Reverse Recovery Time and Charge Measurement of SiC MOSFET

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GUIDELINES FOR REVERSE RECOVERY TIME AND CHARGE MEASUREMENT OF SIC MOSFET

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Foreword

This document was drafted by JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document is intended for use in the SiC power semiconductor and related power electronic industries and provides guidelines for test methods and circuits to be used for reverse recovery measurements for SiC power conversion devices.

Introduction

In 1994, JEDEC introduced the JESD24-10 standard [1], which describes a test method for measurement of reverse recovery time for power MOSFET drain source diodes. However, this standard proposes a test circuit using a p-channel MOSFET, even though the DUT itself is an n-channel transistor. This makes it difficult to apply this standard to a wide range of SiC power transistors, since p-channel types are not common.

IEC 60747-8 [2] proposes two different test circuits, neither of which requires a p-channel transistor. One of them is the clamped inductive load configuration, as widely used in double pulse test systems. However, when it comes to defining the boundaries for extracting the reverse recovery charge, this standard uses drain leakage current (IDSS) to define the corresponding threshold. This is in the range of micro amperes for power transistors. In contrast, the rated forward current of these transistors is in the tens, if not hundreds, of amperes. The dynamic range of the measurement setup shall cover this entire range. Due to the noise and a limited resolution, it is therefore not possible to determine the crossing of the drain current reliably and repeatedly through such a small threshold.

The objective of this guideline is to overcome the limitations of these standards and provide a test circuit and method that provides both reliable and repeatable results.

GUIDELINES FOR REVERSE RECOVERY TIME AND CHARGE MEASUREMENT OF SIC MOSFET

(From JEDEC BoD Ballot JCB-24-26, formulated under the cognizance of the JC-70.2 Subcommittee on SiC Power Electronic Conversion Semiconductor Standards.)

1 Scope

The purpose of this test is to determine the time required for the device under test (DUT) to switch off when a reverse bias is applied after the DUT has been forward biased and to determine the charge recovered under the same conditions. In addition, a distinction is made between capacitive and bipolar charge.

2 Terms, Definitions and Letter Symbols

C_{oss}	output capacitance
DUT	Device Under Test
di/dt	slope of current when diode is switching from forward to reverse conduction
di_r/dt	slope of current when diode is switching from reverse conduction to blocking
I_{FM}	maximum forward current through body diode
$I_{FM(Qoss)}$	maximum forward current through body diode if Q_{oss} is determined by measuring Q_{RR} at low currents
I_{RM}	reverse recovery peak current
i_F	forward current of DUT's body diode (inverted i_S), time-varying
i_L	current through inductor, time-varying
i_S	source current of DUT, time-varying
L_{par}	parasitic inductance of the switching circuit
Q_{BIP}	bipolar charge contribution to Q_{RR}
Q_{oss}	capacitive charge contribution to Q_{RR}
Q_{RR}	reverse recovery charge
R_G	gate resistor
T	DUT temperature
t_a	time from t_1 until I_{RM} is reached
t_b	time from I_{RM} until t_2
t_{c1}	beginning of integration period for Q_{oss}
t_{c2}	end of integration period for Q_{oss}
t_{dead}	time between the two pulses. This is the time in which the current flows in forward direction through the body diode. This time affects the reverse recovery behavior.
t_{rr}	reverse recovery time (the sum of t_a and t_b)
t_w	time at which the pn junction is free of charge carriers and the diode starts to pick up voltage
t_1	beginning of integration period for Q_{RR}
t_2	end of integration period for Q_{RR}
V_{DD}	supply voltage
$V_{GS(OFF)}$	gate to source voltage of DUT in OFF-state, dc component
$V_{GS(OFF,HS)}$	gate to source voltage of high-side device in OFF-state, dc component

2 Terms, Definitions and Letter Symbols (cont'd)

$V_{GS(ON,HS)}$	gate to source voltage of high-side device in ON-state, dc component
$V_{GS(th)}$	gate to source threshold voltage, dc component
v_{DS}	drain to source voltage of DUT, time-varying
$v_{DS(HS)}$	drain to source voltage of high side device, time-varying
v_{GS}	gate to source voltage of DUT, time-varying
$v_{GS(HS)}$	gate to source voltage of high side device, time-varying

3 Description

The body diode of SiC MOSFETs is in principle a classical PIN diode, if the channel is closed, see Figure 1. In power/PIN diodes, during forward conduction, the drift region is flooded with electron-hole pairs, also called plasma or stored charge Q_F, see Figure 2. In the same way a charge builds up during forward conduction of a SiC MOSFETs body diode. During diode turn-off, the stored charge must be removed to pick up the applied voltage and the electric field. In the process, a space charge region forms in the diode, see Figure 3. The removal process of the stored carriers is defined as reverse recovery process and is visible as measured reverse current.

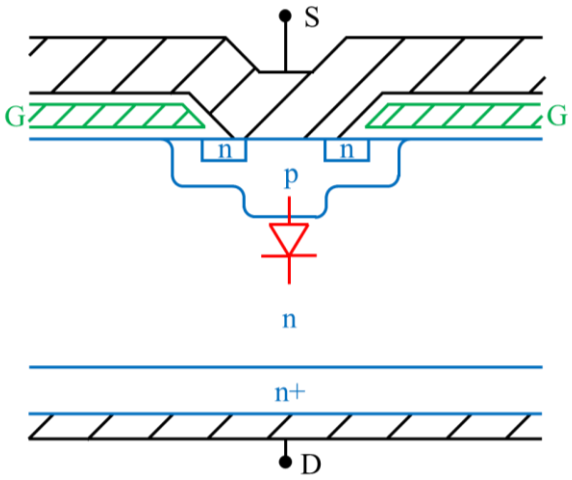


Figure 1 – Body Diode (Red) within the (SiC) MOSFET

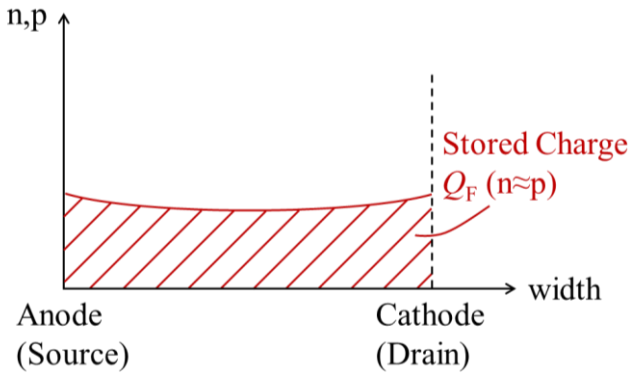


Figure 2 – Stored Charge QF of a PIN Diode or Body Diode during Forward Conduction

3 Description (cont'd)

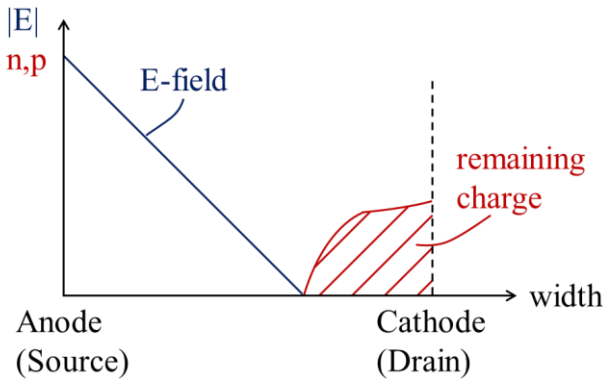


Figure 3 – Charge Removal Process during Turn-off of a SiC MOSFET Body Diode (Channel Closed), Recorded at a Certain Time during Turn-off; the Diode Already Picked up a Certain Voltage

First, a certain charge must be removed before the diode can pick up the voltage. The switching speed (d*i*/d*t*) in this interval is determined by the switch and/or the parasitic inductance of the commutation circuit, see Figure 4. At t_w, the pn junction of the diode is free of charge carriers and the diode starts to pick up the voltage. At a certain point, the reverse current reaches its maximum, which is visible at I_{RM}. Then d*i*/d*t* changes sign and the current drops towards the leakage current of the MOSFET. This falling di_r/d*t* induces an additional rise of the diode voltage (due to the parasitic inductance of the circuit). At the end of the reverse recovery process, the MOSFET blocks the applied voltage (DC link voltage) and only the leakage current flows.

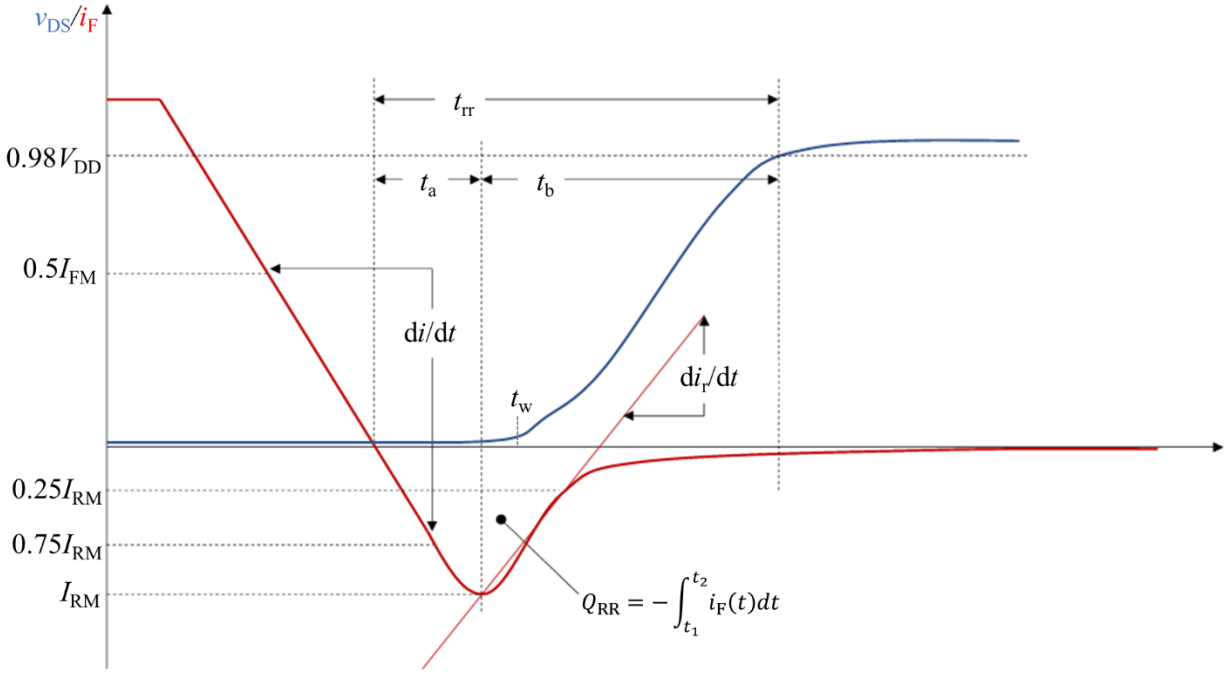


Figure 4 – Current/Voltage Characteristics at PIN Diode during Reverse Recovery

3 Description (cont'd)

The area below the current waveform (integral) is defined as Q_{RR} – the charge, which is visible during the reverse recovery behavior, see Figure 4 and description of the measurement circuit below. Characteristic times such as t_{rr} – reverse recovery time – are typically defined. These times are usually determined by the switching speed of the switching device. Q_{RR} is an important switching parameter. The higher the Q_{RR}, the higher the switching losses.

3.1 Two Components of Q_{RR}: Junction Capacitance Discharge and Stored Carrier Charge

If a voltage slope (dv/dt) is visible during reverse recovery, the junction capacitance of the pn junction must be charged. Therefore, the measured Q_{RR} is combined from this capacitive charge Q_{oss} and the carrier-stored charge Q_{BIP}:

$$Q_{RR} = Q_{oss} + Q_{BIP}.$$

Q_{oss} can be calculated from the $C_{oss}(V)$ curve of the SiC MOSFET with

$$Q_{oss} = \int_0^{V_{DD}} C_{oss}(V)\mathrm{d}V.$$

Especially for SiC MOSFETs, Q_{BIP} is much smaller compared to Silicon devices due to the short lifetimes and lower emitter efficiencies. Q_{oss} can be the dominant term in the measured Q_{RR}, especially at lower temperatures and forward currents.

3.2 Influence of v_{GS} on Reverse Recovery Behavior

To evaluate the pure Q_{RR} of the body diode, it is important to prevent a channel contribution which is visible as a parasitic turn-on during the reverse recovery process. If the electron channel turns on at the commutating diode, a second peak can be visible in the measured Q_{RR}, see [3] and Figure 5. Q_{RR} will be measured larger than the body diode itself specifies. Therefore, the gate voltage and external gate impedance at the DUT should be selected small enough to prevent channel contribution. In addition to the effect of parasitic turn-on, there is a v_{GS}-dependent third quadrant channel conduction which contributes to the measured reverse recovery charge even at normal off-state operating conditions for v_{GS}, see [4].

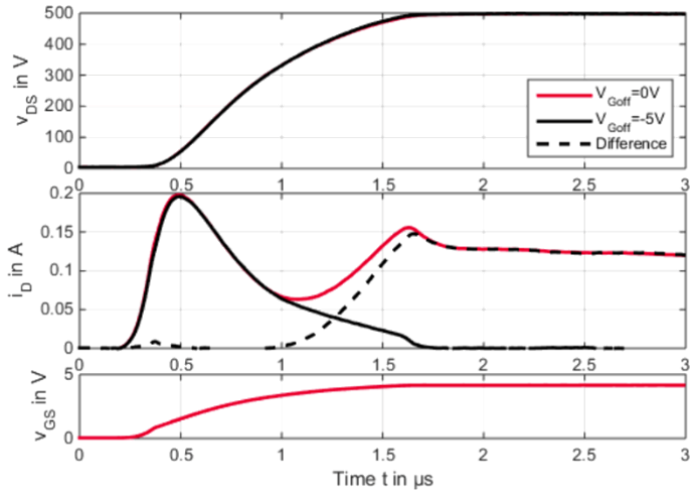


Figure 5 – A Second Peak in the Current Waveform (Red Waveform) due to Parasitic Turn-on Effect [3]

3.3 Influence of DUT Temperature

Electron and hole lifetimes and typically emitter efficiencies increase with higher temperatures during switching and consequently Q_{BIP} increases. The measured Q_{RR} can therefore be dominated by the stored carriers. This also strongly depends on the respective MOSFET technology.

4 Test Circuit

A half-bridge circuit consisting of the DUT and another transistor – preferably of the same type – serves as the test circuit, see Figure 6. The DUT is placed at the low side. An inductor L_{LOAD} is connected in parallel to the DUT as a load. The gate of the DUT is driven to a static DC level with low impedance, which ensures that the transistor is reliably turned off, v_{GS} is always kept below $V_{GS(th)}$. This may require using a negative voltage. The high-side transistor is driven by a floating gate driver and a suitable gate resistor R_G. The resistor can be used to adjust the switching speed and therefore the di/dt for the test.

A capacitor C is charged to the desired test voltage by a DC power supply before the test is started. The power supply can be decoupled from the test circuit after charging. The capacitance shall be sufficiently large so that the supply voltage drops less than 5 % throughout the test.

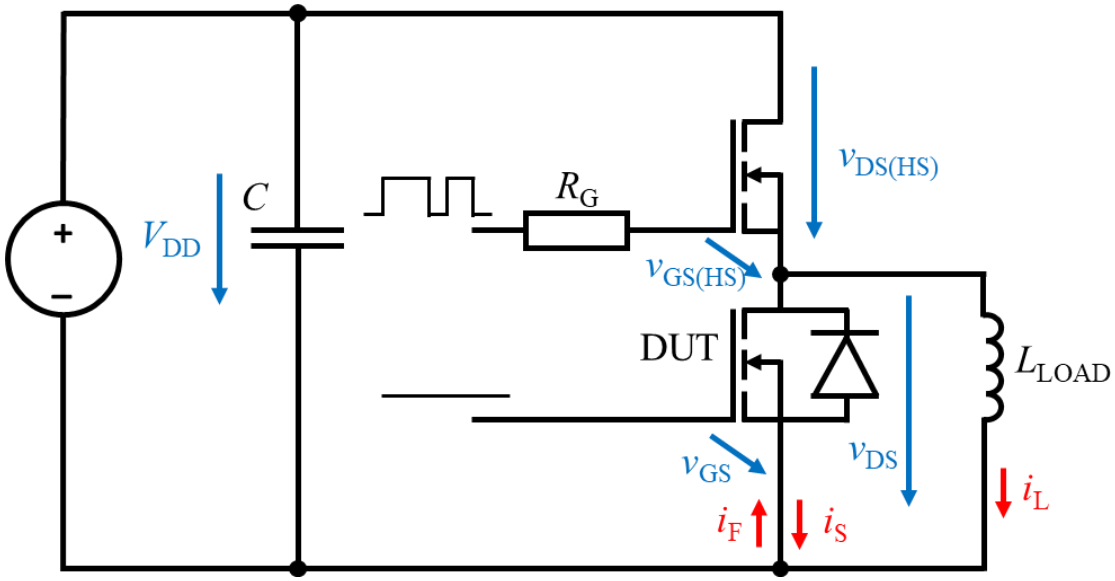


Figure 6 – Test Circuit for Measuring Reverse Recovery

When setting up the test circuit, the following parasitic elements should be considered.

- The power loop inductance, which is composed of the traces between the transistors, the traces between the transistors and the tank capacitor C, and the respective inductances of the transistors and capacitor should be minimized.
- The parasitic capacitance across the DUT should be minimized. The parasitic capacitance of the inductor is the main contributor to this.

4 Test Circuit (cont'd)

The parasitic characteristics of the transistors shall also be considered. In particular, the parasitic coupling from the drain to the gate can induce a voltage spike at the gate which can cause false turn-on as mentioned in the section above. To prevent this from happening the gate of the DUT shall be driven to a sufficiently low value with sufficiently low impedance.

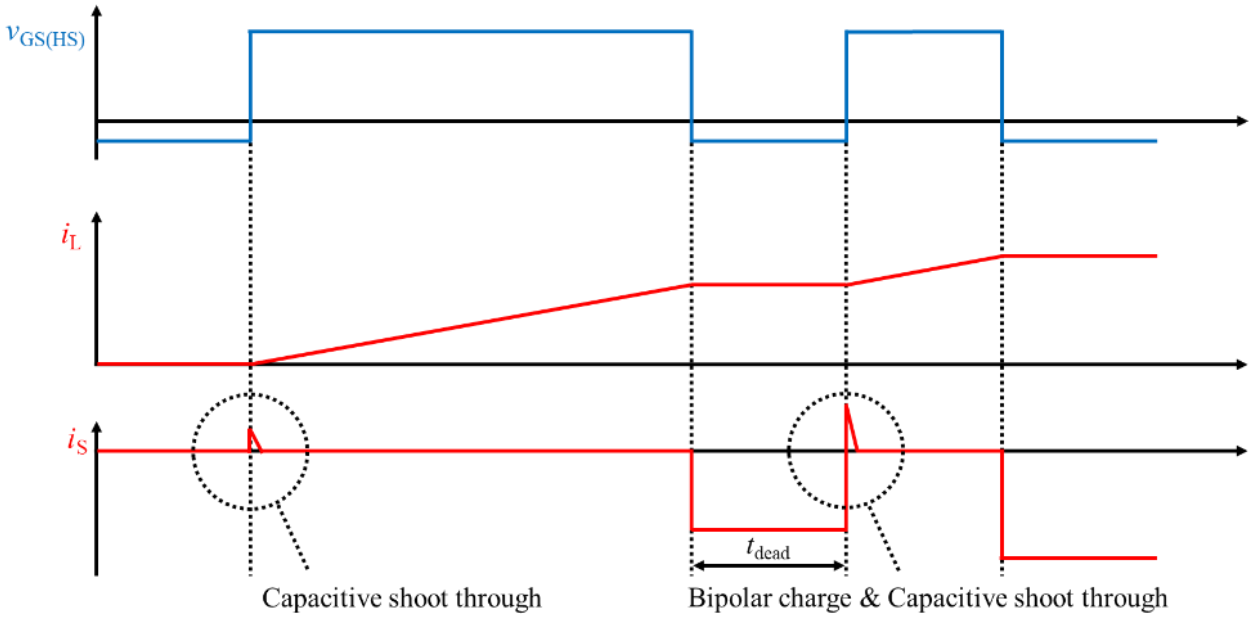


Figure 7 – Test Waveform

For testing, two gate pulses are applied to the high-side transistor. During the first pulse, the inductor is charged to the desired current at which the test is to be performed. Note that a current peak can already be observed at the beginning of this pulse. This is a capacitive shoot through caused by the voltage change on the DUT output capacitance C_{oss}, the parasitic capacitance of the load inductor and parasitic capacitances of the test circuit in general like the PCB. Between pulses, the DUT is reverse biased and the inductor current flows through the body diode of the DUT. At the beginning of the second pulse, when the high-side transistor is turned on for the second time, a combination of bipolar charge and capacitive shoot through is observed, see Figure 7.

5 Measurement Considerations

The measurement conditions which shall be documented are given in Table 1.

Table 1 – Measurement Condition Parameters to be Documented

Symbol	Description
I_{FM}	maximum forward current through body diode
$I_{FM(Qoss)}$	maximum forward current through body diode if Q_{oss} is determined by measuring Q_{RR} at low currents
L_{par}	parasitic inductance of the switching circuit
R_G	gate resistor
T	DUT temperature
t_{dead}	time between the two pulses. This is the time in which the current flows in forward direction through the body diode. This time affects the reverse recovery behavior.
V_{DD}	supply voltage
$V_{GS(OFF)}$	gate to source voltage of DUT in OFF-state, dc component
$V_{GS(OFF,HS)}$	gate to source voltage of high-side device in OFF-state, dc component
$V_{GS(ON,HS)}$	gate to source voltage of high-side device in ON-state, dc component

The reverse recovery behavior is not directly determined by the gate voltages ($V_{GS(OFF,HS)}$ and $V_{GS(ON,HS)}$) and the value of the gate resistor R_G of the high side transistor. However, these parameters determine how fast this transistor switches and thus the steepness during the body diode turn-off. The reverse recovery behavior depends on this steepness. Therefore, it is also acceptable to specify this steepness di/dt as one of the parameters describing the measurement conditions. However, in this case, the gate voltages and gate resistor should still be documented to improve the reproducibility of the measurements results.

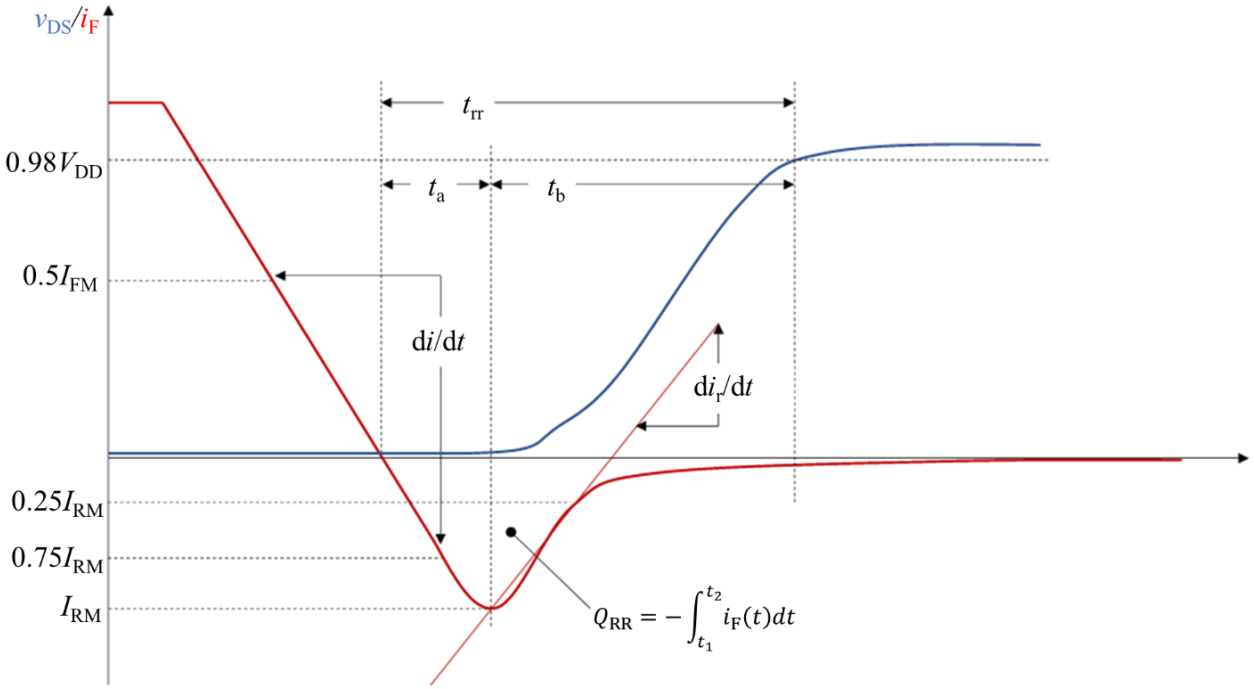
In contrast to t_{dead}, the length of both pulses and the inductance of the inductor have no direct influence on the reverse recovery behavior. However, those should be selected so that the pulses are long enough for the transistors to fully turn on and off.

The quantities given in Table 2 shall be extracted by measurement and documented. All quantities but Q_{oss} and Q_{BIP} can be directly extracted from current and voltage waveforms at the beginning of the second pulse as shown in Figure 8.

Table 2 – Measurement Result Parameters to be Documented

Symbol	Description
di/dt	slope of current when diode is switching from forward to reverse conduction
di_r/dt	slope of current when diode is switching from reverse conduction to blocking
I_{RM}	reverse recovery peak current
Q_{BIP}	bipolar charge contribution to Q_{RR}
Q_{oss}	capacitive charge contribution to Q_{RR}
Q_{RR}	reverse recovery charge
t_a	time from t_1 until I_{RM} is reached
t_b	time from I_{RM} until t_2
t_{rr}	reverse recovery time (the sum of t_a and t_b)

5 Measurement Considerations (cont'd)



NOTE This plot is showing i_F which is the inverted version of i_S.

Figure 8 – Extraction of Reverse Recovery Parameters

The following definitions apply for the extractions shown in Figure 8:

- t_1: the time when i_F is crossing the x-axis (i.e. 0 A);
- t_2: the time when v_{DS} reaches 98 % of V_{DD};
- di/dt: the slope of the straight line through $0.5I_{FM}$ and $0.75I_{RM}$;
- di_r/dt: the slope of the straight line through I_{RM} and $0.25I_{RM}$.

Defining the second boundary of the integral using a voltage threshold works under the assumption that all plasma charge in the drift region has effectively been swept out by this time. This can be verified by ensuring that i_F has approached 0 A at this time ($i_F < 0.1I_{RM}$). This is shown in Figure 9. In this example, the voltages of 600 V and 900 V are sufficiently high. This is not the case for 300 V.

5 Measurement Considerations (cont'd)

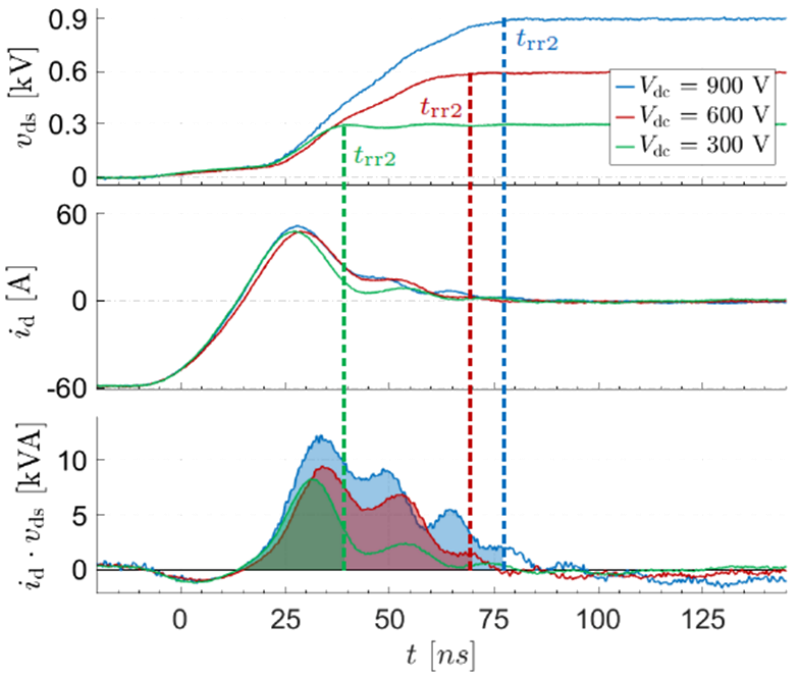


Figure 9 – Waveforms of Reverse Recovery Behavior at Various Values of V_{DD} [5]

As described in the previous sections, the extracted overall reverse recovery charge Q_{RR} is the sum of a capacitive charge Q_{oss} and a carrier stored charge Q_{BIP}. Only the latter contributes to the self-heating of the device, so a separation of these quantities should be performed. As described in the previous sections, the capacitive charge Q_{oss} results not only from the output capacitance of the DUT, but also from the parasitic capacitance of the load inductor and the parasitic capacitances of the test circuit in general.

There are two approaches to separate Q_{oss} from Q_{BIP} which are described below:

In the first approach the capacitive shoot through is measured at the beginning of the first pulse, see Figure 10. Since no current i_F flows through the diode at the beginning of the first pulse, no Q_{BIP} component is present, and the total measured charge is capacitive. Both Q_{oss} and Q_{BIP} can therefore be measured simultaneously within the same test. The definitions for the integration boundaries t_{c1} and t_{c2} are like t_1 and t_2 and are as follows:

- t_{c1} the time before start of first pulse;
- t_{c2} the time when v_{DS} reaches 98 % of V_{DD}.

In the second approach Q_{oss} is extracted in the second pulse as shown in Figure 8 with sufficiently low diode current $I_{FM(Qoss)}$ by changing the first pulse width. This is possible because Q_{BIP} decreases with decreasing diode current I_{FM} and Q_{oss} is independent of the diode current, see Figure 11. A sufficiently low current is reached, when there is no significant difference in the extracted charge between tests at room temperature and maximum junction temperature. Alternatively, the Q_{oss} can be measured using a LCR or capacitance meter.

5 Measurement Considerations (cont'd)

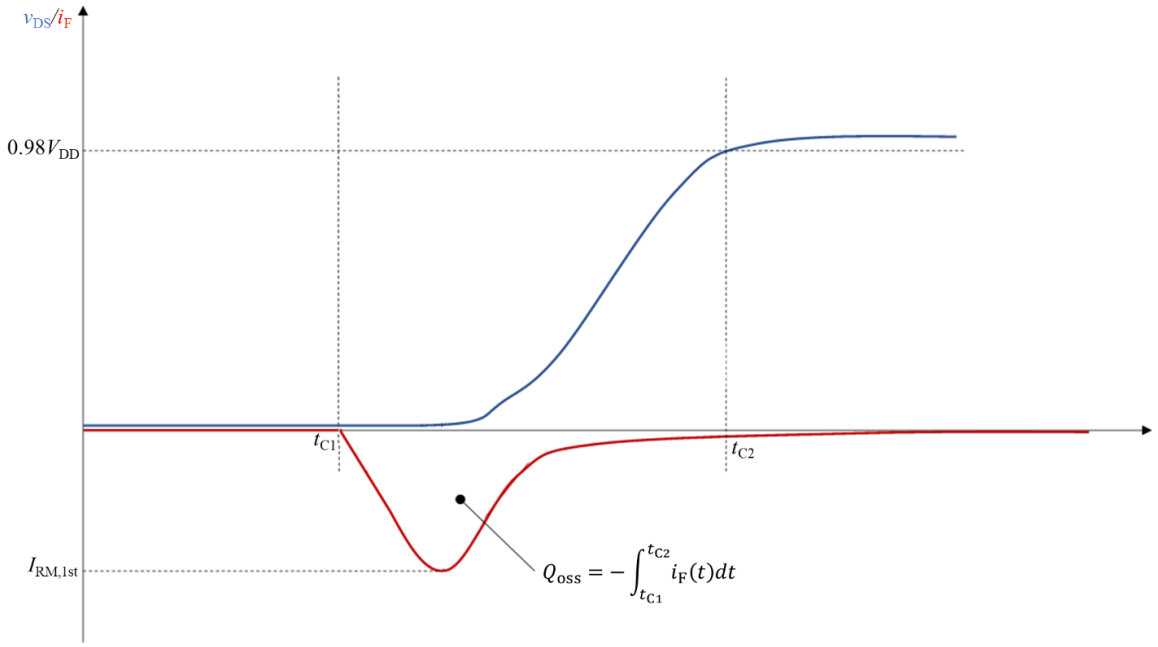


Figure 10 – Extraction of Q_{oss} at the First Pulse

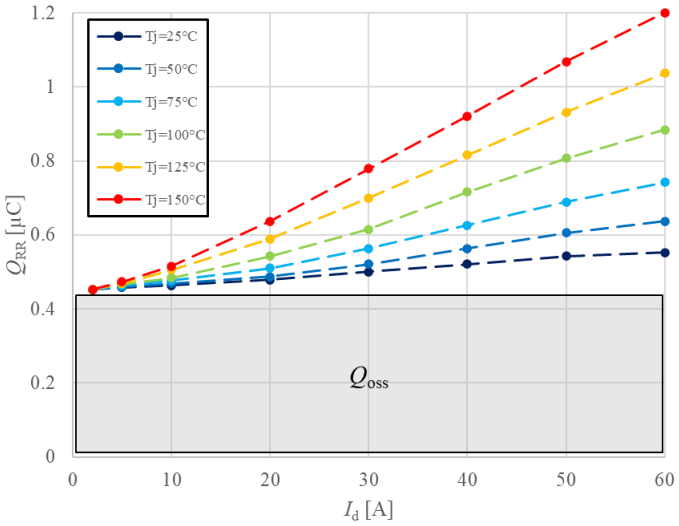


Figure 11 – Extraction of Q_{oss} by Measuring Q_{RR} for Low Currents

Whenever a charge is extracted at the first or second pulse, it is crucial that the current stays negative or does not take on a significant positive value over the entire integration interval. This means that there shall not be too much ringing through which the current becomes positive. If the current approaches zero at the end of the integration interval, it is permissible that the current occasionally slightly exceeds the zero-line due to the occurring noise.

5 Measurement Considerations (cont'd)

When selecting the measurement equipment, care shall be taken to ensure that a sufficiently high measurement bandwidth is available. This is dictated by the transition times, but also by the frequency of the ringing, if this should be faithfully captured as well. As a rule of thumb, the bandwidth up to which a significant amount of energy is carried in a signal can be estimated by dividing 0.5 by the transition time (10 % to 90 %). For an accurate measurement, an additional margin should be added [4].

From a measurement perspective the forward current though the transistor I_{FM} should be in a similar order of magnitude than the expected reverse recover peak current I_{RM}. Note that the oscilloscope shall be set to detect both currents without clipping the signal. If both share a similar size, the sensitivity of the current probe can be selected so that both can be measured with similar accuracy.

6 References

[1] JESD24-10 (1994): Test Method for Measurement of Reverse Recovery Time t_{rr} for Power MOSFET Drain-Source Diodes.

[2] IEC 60747-8 (2010): Semiconductor Devices – Discrete Devices – Part 8: Field-effect Transistors.

[3] K. Sobe, T. Basler and B. Klobucar, "Characterization of the Parasitic Turn-on Behavior of Discrete CoolSiC™ MOSFETs", *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1-7, 2019.

[4] L. Tang, H. Jiang, X. Zhong, G. Qiu, H. Mao, X. Jiang, X. Qi, C. Du, Q. Peng, L. Liu and L. Ran, "Investigation Into the Third Quadrant Characteristics of Silicon Carbide MOSFET", *IEEE Transactions on Power Electronics*, vol. 38(1), pp. 1155-1165, 2022.

[5] P. Sochor, A. Huerner, M. Hell and R. Elpelt, "Understanding the Turn-off Behavior of SiC MOSFET Body Diodes in Fast Switching Applications", *PCIM Europe digital days* 2021.

[6] B. Holzinger, M. Zimmermann, R. Takeda and M. Hawes, "Understanding Bandwidth Requirements When Measuring Switching Characteristics in Power Electronic Applications", *Bodo's Power System*, May 2021.

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