JEDEC PUBLICATION

Common Flash Interface (CFI) ID Codes

JEP137B

(Revision of JEP137-A)

MAY 2004

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Published by
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COMMON FLASH INTERFACE ID CODE ASSIGNMENTS

Introduction

This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and host system software interrogation handshake. JEP137 documents ID Code assignments for: 1) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes.

Additions to Table 1

The Algorithm Command Set and Control Interface ID codes list is not a fixed listing. Any company can be added to the list by making a request to the JEDEC Office at 703.907.7558. The present list is complete as of September 26, 2001. Updates to the list will be made periodically and Table 1 will be modified accordingly.

COMMON FLASH INTERFACE ID CODE ASSIGNMENTS

(From JEDEC Board Ballot JCB-98-81 and JCB-00-101, formulated under the cognizance of the JC-42.4 Subcommittee on Nonvolatile Memories.)

1 Scope

The Algorithm Command Set and Control Interface ID codes listed in this publication are assigned to each unique algorithm upon request to the JEDEC Office. Any number of different interfaces may be thus identified by a single vendor or association of vendors. It is up to those manufacturers to provide the detailed specifications for each identified interface. Similarly, new device interface codes will be assigned as needed as new devices employing the Common Flash Interface Query scheme are identified. This publication also provides examples of Query data output for pre-CFI devices as provided by participating vendors; these represent the appropriate data for the specifications and geometry of these devices as they would appear in the Query structure if the Query mode were available for them.

2 Algorithm command set & control interface ID code assignments

Table 1 — Command set and control assignments

Hex Value	Integer Value	Initial Sponsor(s)	Interface Name
0000	0	Null	e.g. when no Alternative Algorithm Command Set and Control Interface is specified
0001	1	Intel/Sharp	Intel/Sharp Extended Command Set
0002	2	AMD/Fujitsu	AMD/Fujitsu Standard Command Set
0003	3	Intel	Intel Standard Command Set
0004	4	AMD/Fujitsu	AMD/Fujitsu Extended Command Set
0006	6	Windbond	Winbond Standard Command Set
0100	256	Mitsubishi	Mitsubishi Standard Command Set
0101	257	Mitsubishi	Mitsubishi Extended Command Set
0102	258	SST	Page Write Command Set
0200	512	Intel	Intel Performance Code Command
0210	528	Intel	Intel Data Command Set
FFFF	65,535	N/A	Not Allowed / Reserved for Future Use

3 Device interface code assignments

Table 2 — Device assignments

Hex Value	Integer Value	Interface Name
0000	0	x8-only asynchronous interface
0001	1	x16-only asynchronous interface
0002	2	supports x8 and x16 via BYTE# with asynchronous interface
0003	3	x32-only asynchronous interface
0004	4	supports x16 and x32 via WORD# with asynchronous interface
FFFF	65,535	Not Allowed / Reserved for Future Use

Annex A Query structure examples

The following tables represent example data for Query structures of existing devices that were in volume production prior to publication of the CFI specification. Thus these data would be the correct CFI parameters if the CFI Query mode were present today or if this mode were added to future versions of such devices. Lacking Query output from the devices, the current system software may embed these data to support both future CFI-compliant devices and current pre-CFI devices.

Table A.1 — CFI query identification string

Offset	Length (bytes)	Description	Example Data **Intel 28F008SC** x8-only device	Example Data **AMD/Fujitsu 29F016** x8-only device	Example Data **Intel 28F800BVT** x16 device/mode	Example Data **AMD/Fujitsu 29LV008** x16 device/mode	Example Data **Intel 28F016SV** x16 device/mode
10h	03h	Query-unique ASCII string "QRY"	10: 51h 11: 52h 12: 59h	10: 51h 11: 52h 12: 59h	10: 0051h 11: 0052h 12: 0059h	10: 0051h 11: 0052h 12: 0059h	10: 0051h 11: 0052h 12: 0059h
13h	02h	Primary Algorithm Command Set and Control Interface ID Code 16-bit ID code for specific algorithm	13: 03h 14: 00h	13: 02h 14: 00h	13: 0003h 14: 0000h	13: 0002h 14: 0000h	13: 0003h 14: 0000h
15h	02h	Address for Primary Algorithm extended Query table Offset value = ***P*** ≥ 31h	15: 32h 16: 00h	15: 40h 16: 00h	15: 003Eh 16: 0000h	15: 0040h 16: 0000h	15: 0032h 16: 0000h
17h	02h	Alternate Algorithm Command Set and Control Interface ID Code second specific algorithm supported Note: ID Code = 0000h means none exists	17: 00h 18: 00h	17: 00h 18: 00h	17: 0000h 18: 0000h	17: 0000h 18: 0000h	17: 0000h 18: 0000h
19h	02h	Address for Secondary Algorithm extended Query table Note: Address 0000h means none exists	19: 00h 20: 00h	19: 00h 20: 00h	19: 0000h 20: 0000h	19: 0000h 20: 0000h	19: 0000h 20: 0000h

Annex A (cont'd)

Table A.2 — System interface string

Offset	Length (bytes)	Description	Example Data **Intel 28F008SC** x8-only device	Example Data **AMD/Fujitsu 29F016** x8-only device	Example Data **Intel 28F800BVT** x16 device/mode	Example Data **AMD/Fujitsu 29LV008** x16 device/mode	Example Data **Intel 28F016SV** x16 device/mode
1Bh	01h	Vcc Logic Supply Minimum Program/Erase voltage bits 7- 4 BCD volts bits 3-0 BCD 100 mV	1B: 30h	1B: 45h	1B: 0030h	1B: 0027h	1B: 0030h
1Ch	01h	Vcc Logic Supply Maximum Program/Erase voltage bits 7- 4 BCD volts bits 3-0 BCD 100 mV	1C: 55h	1C: 55h	1C: 0055h	1C: 0036h	1C: 0055h
1Dh	01h	Vpp [Programming] Supply Minimum Program/Erase voltage bits 7- 4 HEX volts bits 3-0 BCD 100 mV	1D: 30h	1D: 00h (No Vpp)	1D: 0045h	1D: 0000h (No Vpp)	1D: 0045h
1Eh	01h	Vpp [Programming] Supply Maximum Program/Erase voltage bits 7- 4 HEX volts bits 3-0 BCD 100 mV	1E: C6h	1E: 00h (No Vpp)	1E: 00C6h	1E: 0000h (No Vpp)	1E: 00C6h
1Fh	01h	Typical timeout per single byte/word program, 2^N µs (00h = not supported)	1F: 03h	1F: 03h	1F: 0003h	1F: 0003h	1F: 0003h
20h	01h	Typical timeout for max multi-byte program , 2^N µs (00h = not supported)	20: 00h	20: 00h	20: 0000h	20: 0000h	20: 000Ah
21h	01h	Typical timeout per individual block erase, 2^N ms (00h = not supported)	21: 0Ah	21: 0Ah	21: 000Ah	21: 000Ah	21: 000Ah
22h	01h	Typical timeout for full chip erase, 2^N ms (00h = not supported)	22: 00h	22: 00h	22: 0000h	22: 000Eh	22: 000Eh
23h	01h	Maximum timeout for byte/word program, 2^N times typical (00h = N/A)	23: 04h	23: 04h	23: 0004h	23: 0004h	23: 0004h
24h	01h	Maximum timeout for multi-byte program, 2^N times typical (00h = N/A)	24: 00h	24: 00h	24: 0000h	24: 0000h	24: 0004h
25h	01h	Maximum timeout per individual block erase, 2^N times typical (00h = N/A)	25: 04h	25: 04h	25: 0004h	25: 0004h	25: 0004h
26h	01h	Maximum timeout for chip erase, 2^N times typical (00h = N/A)	26: 00h	26: 00h	26: 0000h	26: 0004h	26: 0004h

Annex A (cont'd)

Table A.3 — Device geometry definition

Offset	Length (bytes)	Description	Example Data Intel 28F008SC x8-only device	Example Data AMD/Fujitsu 29F016 x8-only device	Example Data Intel 28F800BVT x16 device/mode	Example Data AMD/Fujitsu 29LV008 x16 device/mode	Example Data Intel 28F016SV x16 device/mode
27h	01h	Device Size = 2^n in number of bytes.	27: 14h	27: 15h	27: 0014h	27: 0014h	27: 0015h
28h	02h	Flash Device Interface description value meaning 0000h x8 asynchronous 0002h x8/x16 asynchronous	28: 00h 29: 00h	28: 00h 29: 00h	28: 0002h 29: 0000h	28: 0002h 29: 0000h	28: 0002h 29: 0000h
2Ah	02h	Maximum number of bytes in multi-byte program = 2^N (0000h = not supported)	2A: 00h 2B: 00h	2A: 00h 2B: 00h	2A: 0000h 2B: 0000h	2A: 0000h 2B: 0000h	2A: 0008h 2B: 0000h
2Ch	01h	Number of Erase Block Regions within device: **bits 7-0 = x** = # of Erase Block Regions	2C: 01h	2C: 01h	2C: 0004h	2C: 0004h	2C: 0001h
2Dh	04h	Erase Block Region 1 Information **bits 31- 16 = z**, where the Erase Block(s) within this Region are (z) times 256 bytes **bits 15 - 0 = y**, where y+1 = Number of Erase Blocks of identical size within region	y: (16 BLKs) 2D: 0Fh 2E: 00h z: (64 KB size) 2F: 00h 30: 01h	y: (32 BLKs) 2D: 1Fh 2E: 00h z: (64 KB size) 2F: 00h 30: 01h	y: (7 BLKs) 2D: 0006h 2E: 0000h z: (128 KB size) 2F: 0000h 30: 0002h	y: (1 BLK) 2D: 0000h 2E: 0000h z: (16 KB size) 2F: 0040h 30: 0000h	y: (32 BLKs) 2D: 001Fh 2E: 0000h z: (64 KB size) 2F: 0000h 30: 0001h
31h	04h	Erase Block Region 2 Information			y: (1 BLK) 31: 0000h 32: 0000h z: (96 KB size) 33: 0080h 34: 0001h	y: (2 BLKs) 31: 0001h 32: 0000h z: (8 KB size) 33: 0020h 34: 0000h	
35h	04h	Erase Block Region 3 Information			y: (2 BLKs) 35: 0001h 36: 0000h z: (8 KB size) 37: 0020h 38: 0000h	y: (1 BLK) 35: 0000h 36: 0000h z: (32 KB size) 37: 0080h 38: 0000h	
39h	04h	Erase Block Region 4 Information			y: (1 BLK) 39: 0000h 3A: 0000h z: (16 KB size) 3B: 0040h 3C: 0000h	y: (15 BLKs) 39: 000Eh 3A: 0000h z: (64 KB size) 3B: 0000h 3C: 0001h	

Annex B Algorithm-specific extended query tables

Table B.1 — Primary algorithm-specific extended query table

Offset	Length (bytes)	Description	Data
(P)h	03h	Primary extended Query table unique ASCII string “PRI“	P: 50h P+1: 52h P+2: 49h
(P+3)h	01h	Major version number, ASCII	P+3: VV_P
(P+4)h	01h	Minor version number, ASCII	P+4: vv_P
(P+5)h	*variable*	*Algorithm-specific extended Query table contents*	*TBD*

Table B.2 — Alternative algorithm-specific extended query table

Offset	Length (bytes)	Description	Data
(A)h	03h	Alternative extended Query table unique ASCII string “ALT“	2E: 41h 2F: 4Ch 30: 54h
(A+3)h	01h	Major version number, ASCII	31: VV_A
(A+4)h	01h	Minor version number, ASCII	32: vv_A
(A+5)h	*variable*	*Algorithm-specific extended Query table contents*	*TBD*


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