DECEMBER 1967

TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS

JEDEC PUBLICATION No. 65

Formulated by

JEDEC

JOINT ELECTRON DEVICE ENGINEERING COUNCIL

Published by

ELECTRONIC INDUSTRIES ASSOCIATION
Engineering Department

2001 Eye Street, N.W. Washington, D.C. 20006

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FOREWORD

This publication describes tests which are intended to represent only the verification of maximum ratings; they are not tests for performance or quality level. It is proposed that this material be used in conjunction with formats developed for device registration and defining data.

All values specified are nominal and should be maintained within equipment capabilities and good engineering practice.

The procedures in this document were prepared by the JS-6 Committee on Power Transistors and approved for publication by the JEDEC Semiconductor Device Council.

JS-6 - T1.1

Minimum Storage Temperature, Maximum Ratings T_{stg} min.

1. General

The minimum storage temperature shall be based on the capability of any individual transistor to meet the test described below.

2. Test Conditions

a. T_{stg} as specified.

b. Duration of the test to be one cycle, 6 hours at minimum specified storage temperature

3. Procedure

a. Adjust the temperature in a temperature-controlled enclosure to the specified storage temperature.

b. Place test transistors in the enclosure.

c. The order of the procedure may be reversed.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics of the Registration.

Maximum Storage Temperature, Maximum Ratings, $T_{stg\ max}$.

1. General

The maximum storage temperature shall be based on the capability of any individual transistor to meet the test described below.

2. Test Conditions

a. T_{stg} as specified.

b. Duration of the test to be one cycle, six hours at the maximum specified storage temperature.

3. Procedure

a. Adjust the temperature in a temperature-controlled enclosure to the specified storage temperature.

b. Place test transistors in the enclosure.

c. The order of the procedure may be reversed.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics of the Registration.

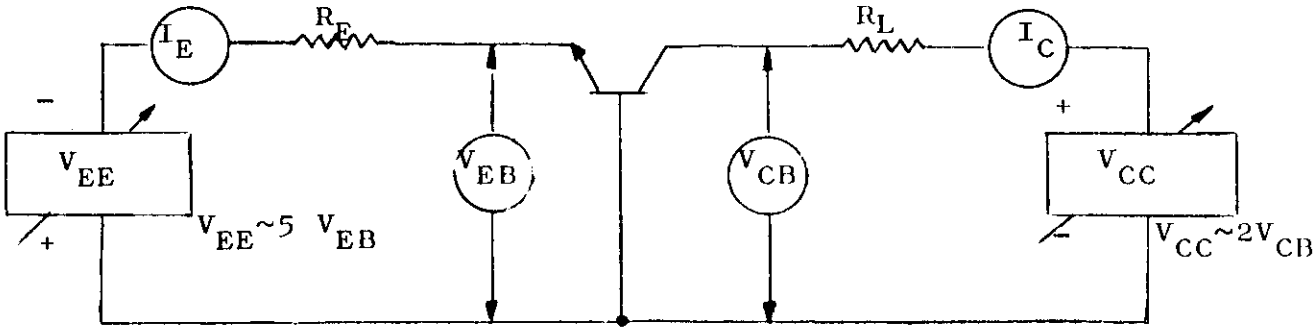
JS-6 - T2

Maximum Operating Junction Temperature Rating, $T_{j\ max}$.

1. General

The maximum operating junction temperature shall be based on the capability of any individual transistor to operate in the test circuit illustrated below:

2. Test Circuit and Conditions: (Polarity of transistor - PNP, NPN - must be observed)



a. V_{CB} and I_C must be specified.

b. The case temperature must be within 75 to 90 percent of the registered operating junction temperature, T_j.

c. The duration of the test shall be one hour.

3. Procedure

a. Adjust the bias conditions to achieve the specified I_C and V_{CB}. The temperature and power dissipation must be such that the junction temperature is equal to the maximum operating junction temperature calculated by:

$$T_J = T_C + \frac{Pd}{\text{Derating Factor } (W/^{o}C)}$$

T_C = Case temperature

P_d = Total Power Dissipation = $V_{CB}\ I_C + V_{EB}\ I_E$

b. Suitable precautions should be taken against transient spikes and oscillations.

Maximum Operating Junction Temperature Rating, $T_{j\ max.}$ (continued)

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

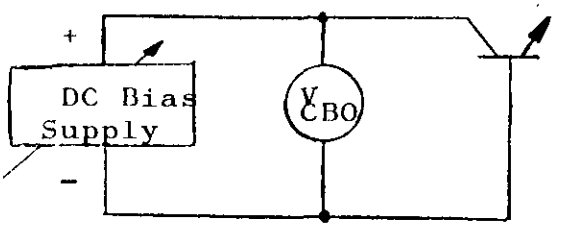
JS-6 - T3

Collector-Base Voltage, Maximum Ratings, V_{CBO}

1. General

The maximum collector-base voltage shall be based on the capability of any individual transistor to meet the test described below:

2. Test Circuit and Conditions: (Polarity of transistor - PNP, NPN - must be observed)



a. The transistor case temperature must be + 25°C.

b. Duration of the test to be one minute.

3. Procedure

a. Adjust the bias supply to obtain the specified V_{CBO}.

b. Suitable precautions should be taken against transient spikes and oscillations.

Collector-Base Voltage, Maximum Ratings, V_{CBO} (continued)

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

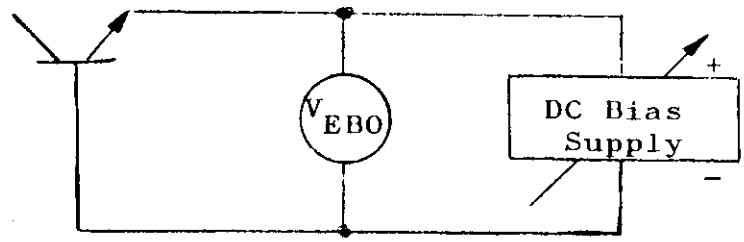
JS-6 - T4

Emitter-Base Voltage, Maximum Rating

1. General

The maximum emitter-base voltage shall be based on the capability of any individual transistor to meet the test described below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. The transistor case temperature must be + 25°C.

b. Duration of the test to be one minute.

3. Procedure

a. Adjust bias supply to obtain the specified V_{EBO}.

b. Suitable precautions should be taken against transient spikes and oscillations.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

JS-6 - T5

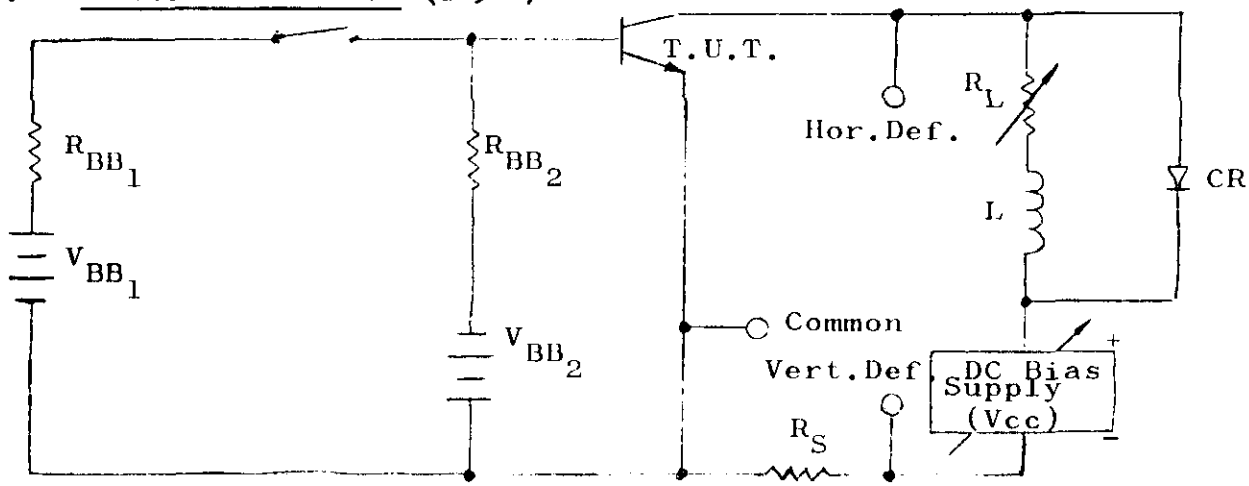
Collector-Emitter Voltage, Maximum Ratings

1. General

The maximum collector-emitter voltage shall be based on the capability of any individual transistor to meet one of the tests described below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)

2.1 Inductive Method (T 5.1)



a. All circuit values must be specified: V_{BB2} may be "0", $R_S \leq \frac{VCC}{20\ I_C}$, R_{BB2} may be infinite. The characteristics or the registered type number of CR if used must be specified.

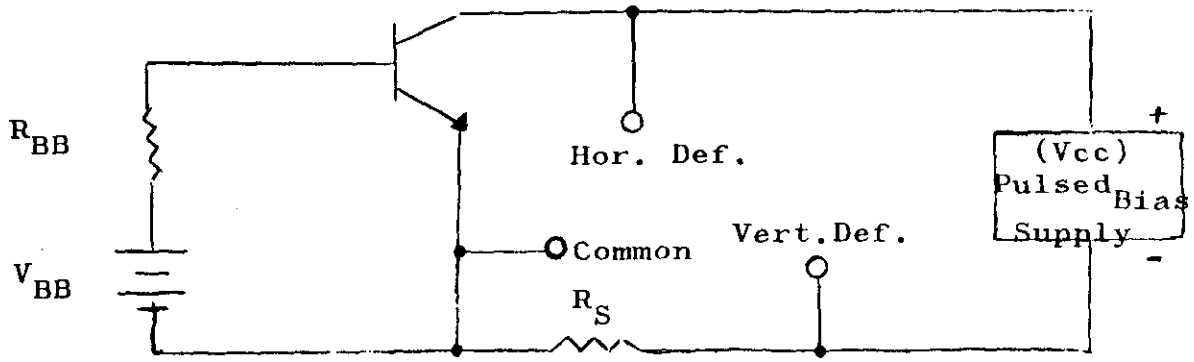
b. The transistor case temperature must be + 25°C.

c. The collector current at the maximum rating of V_{CE} must be as specified. If this is a sustaining test, this current should be high enough to insure that the transistor is in the sustaining region where the collector voltage is relatively insensitive to collector current over a large range of currents.

d. Duration of the test shall be that time adequate to make the reading.

e. The pulse repetition rate should be specified.

2.2 Pulsed Collector Method (T 5.2)



a. All circuit values must be specified; R_{BB} may be from "0" to infinity, V_{BB} may be "0".

b. The transistor case temperature must be +25°C.

c. The collector current at the maximum rating of V_{CE} must be as specified. If this is a sustaining test, this current should be high enough to ensure that the transistor is in the sustaining region where the collector voltage is relatively insensitive to collector current over a large range of currents.

d. Duration of the test shall be that time adequate to make the reading.

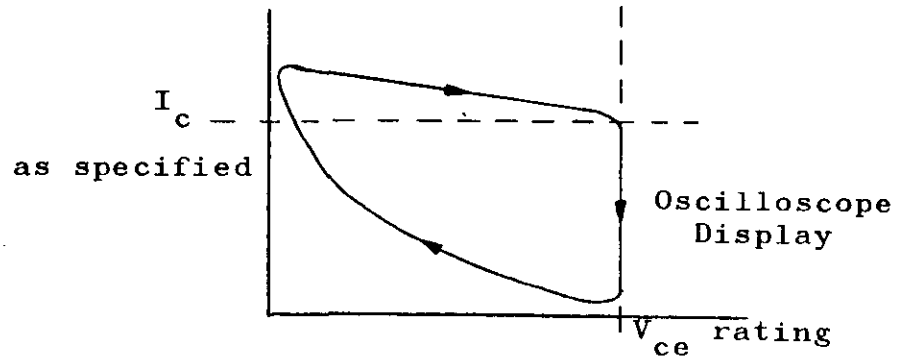
e. The pulse repetition rate and duty cycle should be specified.

3. Procedure

3.1 Inductive Method (T 5.1)

a. Adjust the bias supplies to the specified test conditions.

b. Decrease R_L until the intersection of the specified collector current and V_{CE} rating is reached. See following illustration.



c. Suitable precautions should be taken against transient spikes and oscillations.

3.2 Pulsed Collector Method (T 5.2)

a. Adjust V_{BB} to the specified value.

b. Increase V_{CC} until the specified collector current is obtained.

4. Evaluation (T 5.1 and T 5.2)

a. The device shall be allowed to reach thermal equilibrium at + 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

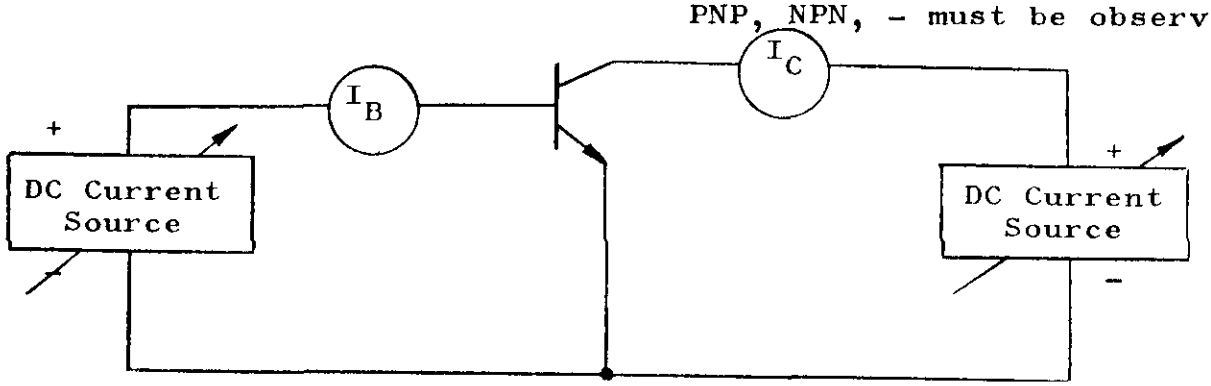
JS-6 - T6

Continuous Collector Current, Maximum Rating

1. General

The maximum continuous collector current rating shall be based on the capability of any individual transistor to operating in the test circuit illustrated below:

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN, - must be observed)



a. The base current must be specified.

b. The transistor case temperature which must not be exceeded shall be specified.

c. Duration of the test to be five minutes.

3. Procedure

a. Increase the base drive to obtain the specified base current, I_B.

b. Increase the collector drive to obtain the rated collector current, I_C.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

JS-6 - T7

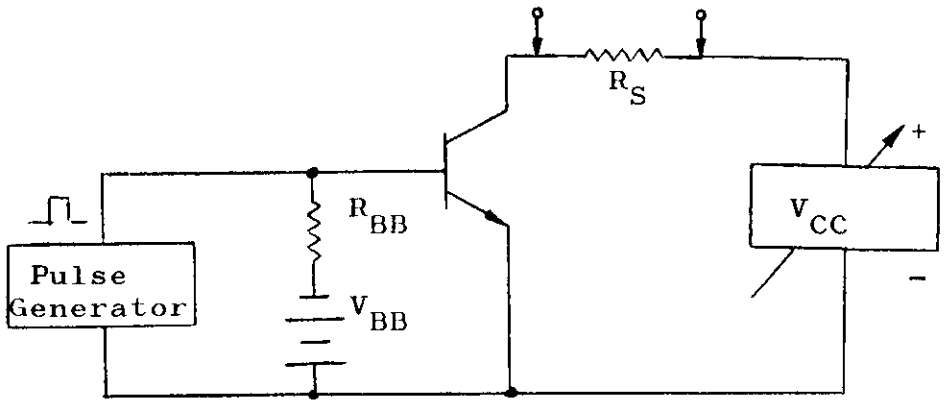
Pulsed Collector Current, Maximum Rating

1. General

The maximum pulsed collector current rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below.

2. Test Circuit and Conditions

(Polarity of transistor - PNP, NPN, must be observed.)



a. The transistor case temperature must be +25° C.

b. The amplitude, wave-shape (rise time, fall time, and pulse width), and duty cycle of the base drive pulse shall be specified.

c. V_{BB}, R_{BB} and R_S must be specified.

d. Duration of the test shall be that time adequate to make the reading.

3. Procedure

a. Adjust the pulse generator to obtain the specified drive pulse.

b. Adjust V_{CC} to obtain the rated pulsed collector current, I_{CM}.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurement.

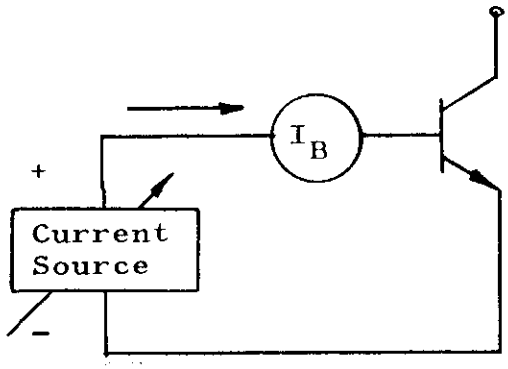
b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

JS-6 - T8
Continuous Base Current, Maximum Rating

1. General

The maximum continuous base current rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN, - must be observed)



a. The transistor case temperature which must not be exceeded shall be specified.

b. Duration of the test to be five minutes.

3. Procedure

Adjust the current source to obtain the rated base current, I_B.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

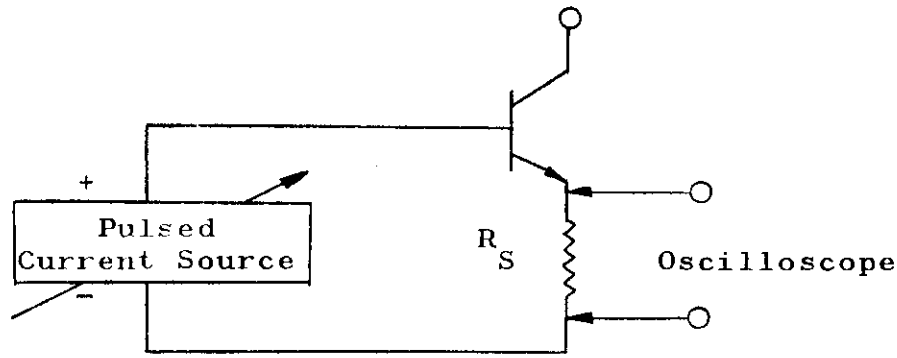
JS-6 - T9

Pulsed Base Current, Maximum Rating

1. General

The maximum pulsed base current rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. The transistor case temperature must be +25°C.

b. The amplitude, wave-shape (rise, time, fall time, and pulse width), and duty cycle shall be specified.

c. Duration of the test shall be that time adequate to make the reading.

3. Procedure

Adjust the pulsed current source to obtain the rated pulsed base current, I_{BM}.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

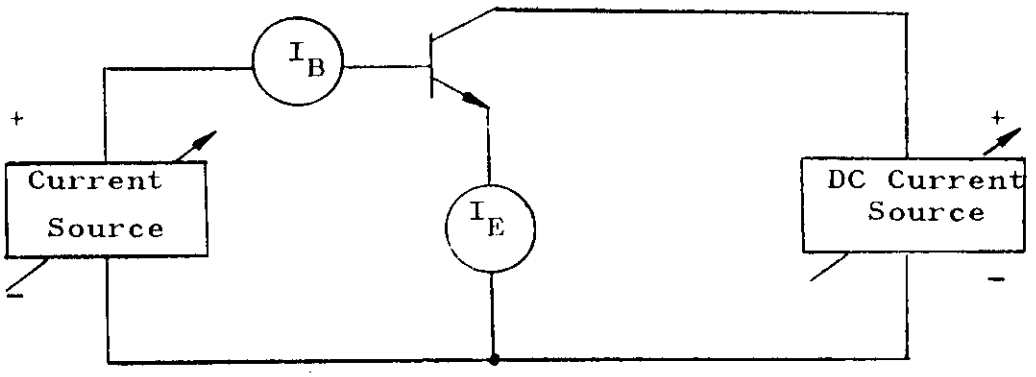
JS-6 - T10

Continuous Emitter Current, Maximum Rating

1. General

The maximum continuous emitter current rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. The base current must be specified.

b. The maximum transistor case temperature must be specified.

c. Duration of the test to be five minutes.

3. Procedure

a. Increase the base drive to obtain the specified base current, I_B.

b. Increase the collector drive to obtain the rated emitter current, I_E.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

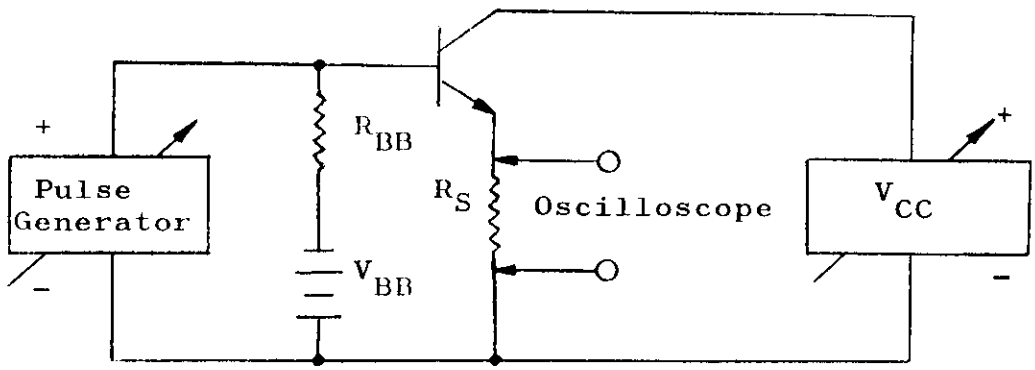
JS-6 - T11

Pulsed Emitter Current, Maximum Rating

1. General

The maximum pulsed emitter current rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. The transistor case temperature must be + 25°C.

b. The amplitude, wave-shape (rise time, fall time, and pulse width), and duty cycle of the base drive pulse shall be specified.

c. R_S, V_{BB} and R_{BB} must be specified.

d. Duration of test shall be that time adequate to make the reading.

3. Procedure

a. Adjust the pulse generator to obtain the specified drive pulse.

b. Adjust V_{CC} to obtain the rated pulsed emitter current, I_{EM}.

Pulsed Emitter Current, Maximum Rating (continued)

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

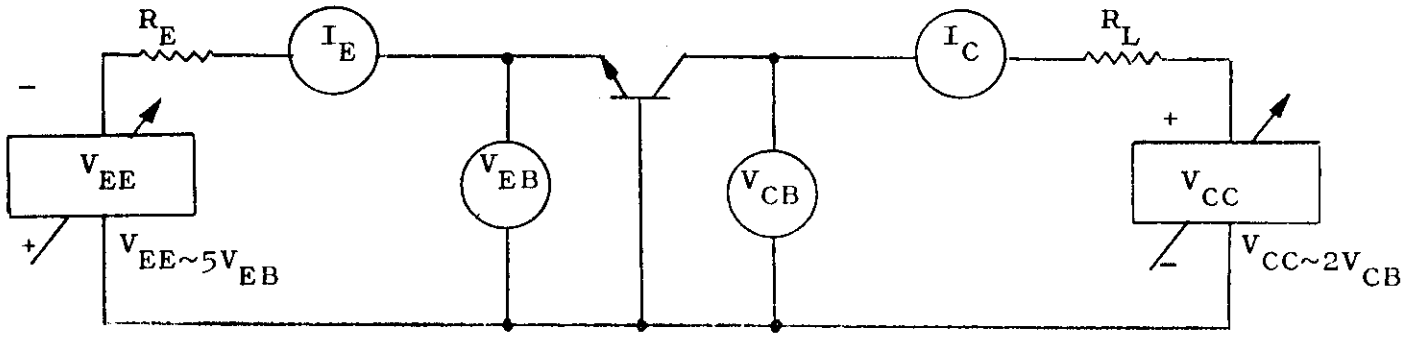
b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

Maximum Continuous Power Dissipation Rating

1. General

The maximum continuous power dissipation rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below:

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. V_{CB} must be specified.

b. The case temperature must be +55°C for all devices rated for operating junction temperatures of 125°C or less , and +100°C for all devices rated for operating junction temperatures about 125°C.

c. The duration of the test shall be one hour.

3. Procedure

a. Adjust the bias conditions to achieve the specified I_C and V_{CB}. The temperature and power dissipation must be such that the junction temperature is equal to the maximum operating junction temperature calculated by:

$$T_j = T_C + \frac{P_d}{\text{Derating factor (W/°C)}}$$

T_C = Case Temperature

P_d = Total Power Dissipation = $V_{CB}\ I_C + V_{EB}\ I_E$

b. Suitable precautions should be taken against transient spikes and oscillation.

Maximum Continuous Power Dissipation Rating (continued)

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.

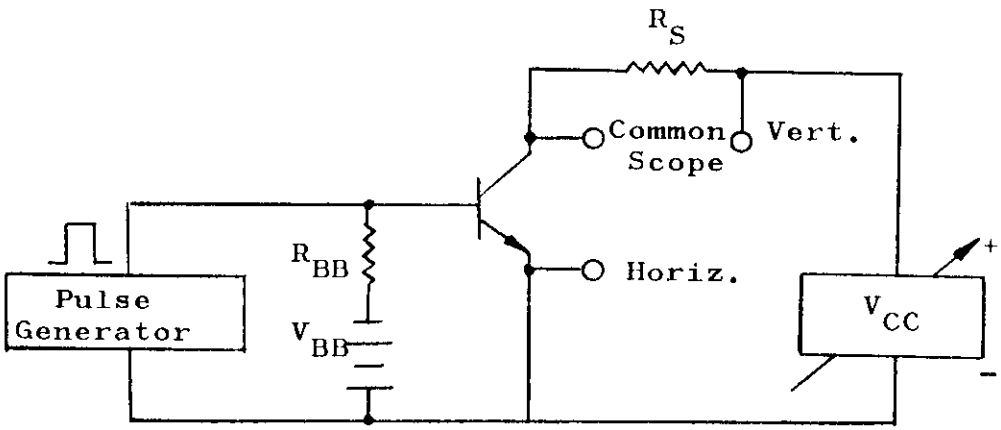
JS-6 - T13

Maximum Peak Power Dissipation Rating

1. General

The maximum peak power dissipation rating shall be based on the capability of any individual transistor to operate in the test circuit illustrated below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. All circuit values must be specified. Peak power shall be considered as the product of the collector current and supply voltage ($P_P = I_C V_{CC}$).

b. The transistor case temperature must be +25°C.

c. The wave-shape (rise time, fall time, and pulse width) and duty cycle of the pulse generator shall be specified.

d. Duration of test shall be that time adequate to make the reading.

3. Procedure

Increase the amplitude of the pulse generator to obtain the specified pulsed collector current, I_{CM}.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics of the Registration.

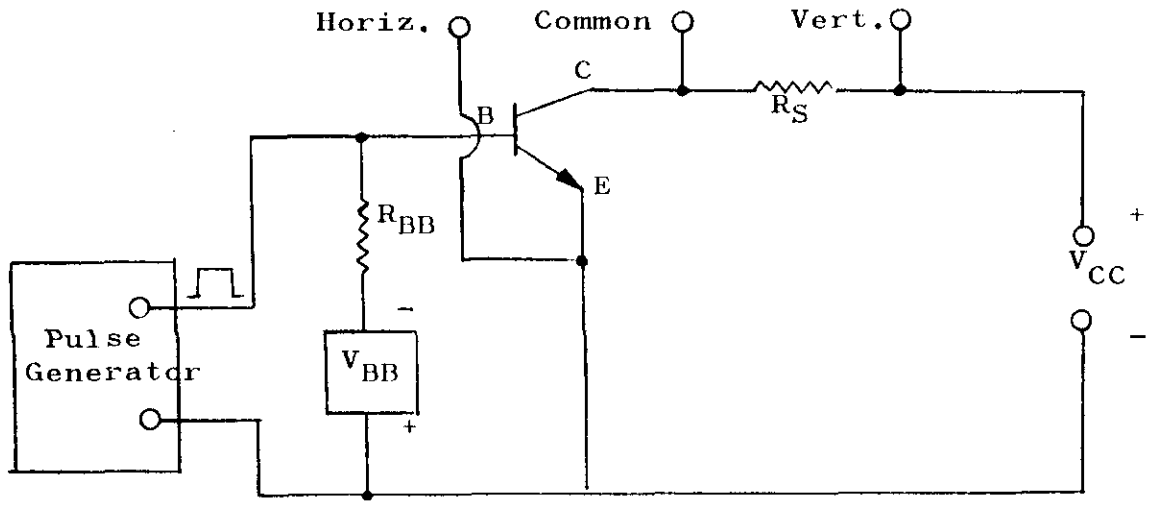
JS-6 - T14

Forward Bias, Maximum Operating Conditions

1. General

The forward bias, maximum operating conditions shall be based on the capability of any individual transistor to meet the test described below.

2. Test Circuit and Conditions (Polarity of transistor - PNP, NPN - must be observed)



a. All circuit values must be specified; R_S must be non-inductive and small such that $R_S \leq \frac{V_{CC}}{20\ I_C}$. V_{BB} and R_{BB} are selected to enhance switching by cutting off transistor when pulse is in "off" condition. BV_{EBO} and I_{EBO} limits must be observed.

b. The transistor case temperature must be specified.

c. Pulse width and duty cycle must be stated. Pulse generator rise and fall times must be specified.

d. Good engineering practice must be used to eliminate effects of lead inductance and power supply characteristics.

Forward Bias, Maximum Operating Conditions (continued)

3. Procedure

a. Adjust the bias supplies to the specified test condition.

b. Increase the pulse amplitude of the pulse generator to obtain the specified collector current, as defined by the voltage, current, and time relationship of the point to be verified.

4. Evaluation

a. The device shall be allowed to reach thermal equilibrium at + 25°C prior to the evaluation measurements.

b. The device shall still be capable of meeting all the Electrical Characteristics specified in the Registration.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