JEDEC STANDARD

Power Cycling

JESD22-A122B

(Minor revision of JESD22-A122A, June 2016)

NOVEMBER 2023

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A122B
POWER CYCLING

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Foreword

This document provides an industry standard test method for power cycling of solid state device packages where on and off cycles of a device create a non-uniform temperature distribution within the package and the next level of assembly. Both sleep and full power modes can be simulated and are used as the basis of life cycle testing of the solid state device and/or associated interconnections.

Introduction

In typical use, the on and off power cycles of functional devices will produce non-uniform temperature distributions within package components as well as between the package and interconnected hardware such as printed wiring boards (PWB), sockets, or heat sinks. The stresses that result from the temperature gradients found in actual product may or may not be accurately simulated by use of isothermal temperature cycling. This test method is a characterization tool which can augment and supplement results obtained with the isothermal chamber-based temperature cycling described in both JESD22-A104 and JESD22-A105. It should be used as an alternative to JESD22-A104 or JESD22-A105 only if such substitution can be technically justified. The test method uses a powered device, a thermal chip or an external heat source to simulate temperature cycling effects on the solid state device package and its materials, including solder joints in free-standing and assembled configurations.

Unlike either JESD22-A104 or JESD22-A105, the power cycles described in this test method are intended to simulate the range of usage conditions found from the vicinity of room ambient up to the maximum junction temperature for the device.

TEST METHOD A122B
POWER CYCLING

(From JEDEC Board Ballot JCB-23-54, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test methods for packaged Devices.)

1 Scope

This Test Method establishes a uniform method for performing solid state device package power cycling stress test. This specification covers power induced temperature cycling of a packaged component, simulating the non-uniform temperature distribution resulting from a device powering on and off in the application.

This test is conducted to determine the ability of solid state device to withstand thermal-mechanical stresses induced by cyclic, non-isothermal high and low temperatures induced by the device operation, including options like standby, hibernate or mini cycles found in some applications. It is used to verify the performance of various component materials and interfaces, especially solder interconnects and thermal interface materials (TIM). Both engineering samples with internal or external thermal heaters and actual power driven product can be used in this test method. Permanent changes in electrical and/or physical characteristics can result from these mechanical stresses and as such should be considered a destructive test.

2 Terms and Definitions

Tj (test)

The junction temperature of the powered device under test during the heating cycle.

Temperature distribution characterization

The range of temperature measured at key points of interest on the solid state device or its associated hardware and signified by T_1, T_2, etc., see Figure A.1.

Maximum cycle temperature: $T_{cycle(max)}$

The maximum cycle temperature of the test, see Table 2.

Minimum cycle temperature: $T_{cycle(min)}$

The minimum temperature of the test.

T (ambient)

The temperature of the local ambient around the test hardware. See Figure A.3 for examples.

2 Terms and Definitions (cont'd)

Nominal ΔT

The difference between nominal $T_{cycle(\max)}$ and nominal $T_{cycle(\min)}$ for the Power Cycling Test Condition, see Figure A.1.

Soak time

The total time the temperature of the sample is within a specified range of each nominal $\boldsymbol{T_{cycle(max)}}$ and nominal $\boldsymbol{T_{cycle(min)}}$. This range is defined as the time $\boldsymbol{T_j}$ is at –5 °C to +10 °C of $\boldsymbol{T_{cycle(max)}}$ nominal for the upper end of the cycle and the time $\boldsymbol{T_j}$ is +5 °C to –10 °C of $\boldsymbol{T_{cycle(min)}}$ nominal for the lower end of the cycle.

Cycle time

Time between one high temperature extreme to the next, or from one low temperature extreme to the next, for a given sample, see Figure A.1.

3 Apparatus

The apparatus used shall be capable of providing and controlling the specified temperatures and cycle timing. While the objective, test samples, and general procedures are similar to accelerated thermal cycling in a chamber, there are also important differences. Key elements of a power cycle apparatus include the following and are illustrated in Figure A.2.

a) A heating element for each tested sample. The heating method and location of heat source will be dependent on the test objective, and can include, but is not limited to, a powered device in the actual product, a serpentine line in the package, a thermal test chip, or an attached external heater mounted on or within the module.

NOTE Dependent on the test point of interest for the solid state device or its associated hardware, the appropriate heating method and location should be used such that the results are representative of the application.

b) Power supplies and connections for powering the heater elements or other heat source.

c) A housing or fixture for each sample or group of samples to provide electrical connections for powering and/or monitoring, and to facilitate cooling.

d) Computer, relay box, or other method of controlling heating and cooling to specified heat and cool parameters.

e) Ambient condition, controlled to the specified temperature range and/or air flow, which can consist of either the surrounding room or a local test enclosure.

f) Cooling system, including forced air or other means, dependent on the application and/ or test requirements.

g) Data collection system capable of recording pertinent test data, including temperature and electrical test information and results.

4 Procedure

The procedure for power cycle testing of solid state device packages generically consists of running the device under test (DUT) through a prescribed temperature range, for a given number of cycles, with appropriate data collection during the test. This cycling period usually starts with a setup step where the device is powered and the cycle temperatures are adjusted and verified. Some typical temperature ranges are shown in Table 2, though other temperatures ranges can be used, based on the specific application requirements. Key elements to an effective procedure include, but are not limited to, test controls, temperature measurement methodology, data collection requirements and heating/ cooling methods. These will be discussed in greater detail in the following clauses.

4.1 Test Samples, Fixtures, And Associated Hardware

The entire power cycle test configuration, including device, package, heat sink, printed circuit board thickness, and fixturing will have a significant effect on results. The test can be done with either actual product or a development test vehicle designed to simulate product. For application specific qualifications, the power cycling setup should reflect the actual product situation as close as possible.

4.2 Power Cycling Methods

There are a number of ways that power cycling can be performed. This includes use of constant or variable prescribed power and constant or variable heat removal or cooling, or combinations of these.

a) Constant power: For any single heater/ device, power is either ON (to a preset value, during heat up) or OFF (during cooling). This usually involves open loop control. The preset value may be varied among DUT to compensate for heater differences and improve temperature uniformity.
b) Variable power: Power varies during the heating and/ or cooling cycle to allow faster heat ramps, mini-cycles and/ or standby modes. Closed loop control is recommended.
c) Constant cooling: As with constant power, cooling is either ON (to a preset value during cooling or throughout the entire cycle) or OFF (during heating, as prescribed). This option involves open loop control.
d) Variable cooling: Cooling varies during the heating and/ or cooling cycle to allow mini-cycles, standby mode options or to mimic other system conditions. Use of this option can also enable increasing the cycle rate.

Figure 1 illustrates the example of constant versus variable power with constant cooling. Table 1 discusses the advantages and disadvantages of each combination. The specific combination used should be selected on product requirements and should be noted as part of the test summary.

4.2 Power Cycling Methods (cont'd)

There are a number of methods to apply heat to the device under test (DUT). The most common are either a powered device in the actual product, a serpentine line in the package, or an attached external heater mounted on or within the module.

Similarly cooling can be through forced convection (air, water or liquid nitrogen under controlled meter), natural convection or by means of attached cooling devices such as, but not limited to, thermoelectric coolers, Peltier cooling plates, or heat pipes. It should be noted that air cooling with a heat sink may be slow and affect test duration and test cycle frequency.

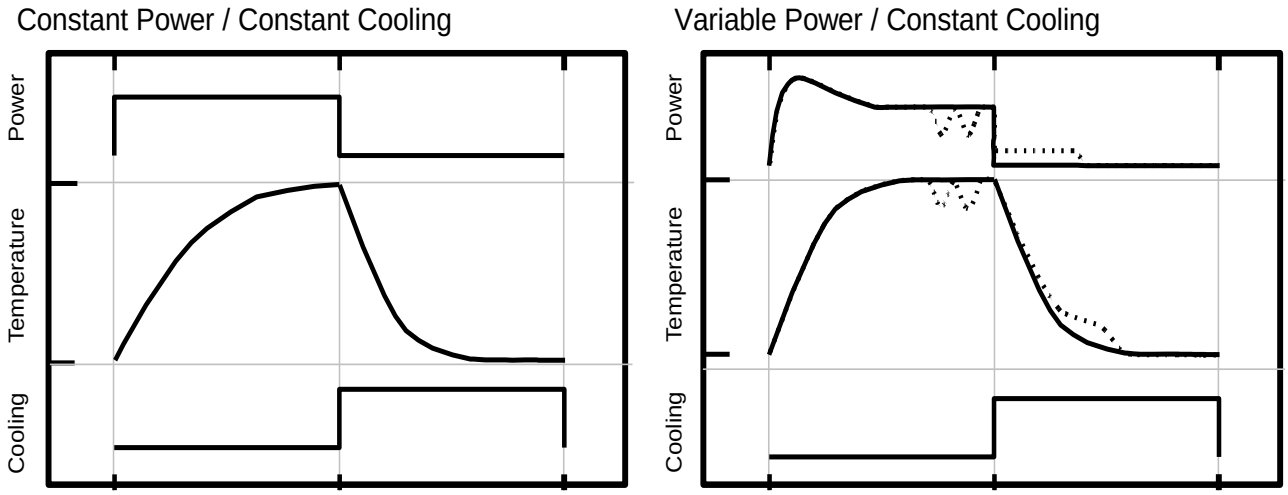


Figure 1 — Comparison of Constant versus Variable Power Testing

4.2 Power cycling methods (cont'd)

Table 1 — Power Cycling Methods

Test Setup Options	Constant Heat Removal/ Cooling	Variable heat Removal/ Cooling
Constant Power	• Easiest to implement • Requires attention to test detail	• Best suited for functional device testing • Best suited for test vehicles with tightly controlled heater resistances • If power must be held constant, variable cooling can allow Tj variation and acceleration modeling • Vary ambient temperatures to simulate different environments • Could be used for mini-cycle evaluation
Variable Power	• Ramping power to test site closely matches actual product profile • Need control to prevent unrealistic power surge • Could be used for mini-cycle evaluations • Different heating patterns, such as, multiple heaters with different resistances can be turned on at different intervals to match thermal profile found in actual product	• Most difficult to implement since it requires significant software control capability • Most appropriate for power cycling of products with complex chip power maps and cooling requirements • Can be used extensively in power cycle set-up and debug, while honing in on desired power/ temperature profile

4.3 Test Hardware

The DUT can consist of either functional product or simulated product through use of test vehicles. Selection should be made based on test hardware availability and the specific test point of interest; e.g. interconnections, thermal interface, etc.

If test vehicles are used they should be designed such that all relevant package and chip to package interaction failure mechanisms can be evaluated during the testing. Heaters should be positioned in the device such that the test site heating is similar to that seen in the product. Dependent on the test site of interest, the temperature variation across the test or functional die can be very important in assessing the product performance in the field.

Temperature sensors should be located across the DUT, either functional or test vehicle, to measure temperature variations on test hardware, see JEP 140 "Beaded Thermocouple Measurement of Semiconductor Packages" for one method of temperature measurement. Other industry recognized methods can also be used.

4.4 Test Conditions

Table 2 lists several typical test conditions. Boundary values are +5 °C and -10 °C for $T_{cycle(\min)}$ and + 10 °C and -5 °C for $T_{cycle(\max)}$. Other test conditions are acceptable based on product requirements and these conditions should be noted in the test summary.

Table 2 — Typical Power Cycling Evaluation Test Conditions

Test Condition	Nominal $T_{cycle(\min)}$, (°C)	Nominal $T_{cycle(\max)}$, (°C)
A	25	+100
B	25	+125
C	10	+100
D	10	+125
E	40	+100

NOTE 1 To simulate specific ambient temperatures, heating or cooling of the part under test may be required.

NOTE 2 Though 2 to 6 cycles per hour is typical, other rates may be used for evaluation of certain failure mechanisms, such as mini-cycle simulation.

NOTE 3 Other test conditions can be selected and should be based on product requirements.

NOTE 4 $T_{cycle(\max)}$ and $T_{cycle(\min)}$ should be selected and documented such that the stress temperatures are met during testing.

4.5 Test setup and Verification

Prior to testing the temperature cycle profile needs to be verified. Setup may include measuring the temperature coefficient of resistance (TCR) to calibrate the power level needed to achieve the desired test temperature settings, see JESD33 for details for this procedure. Thermocouple(s) or other temperature measuring device(s) need to be located at all key points of interest on the component or its associated hardware. The setup period may be used to get to the prescribed temperatures and cycle times. If a functional die is used, it is recommended that a series of runs be performed to characterize the actual solid state device and package temperatures versus time prior to the start of the power cycling test.

4.6 Test Controls and Measurement

Temperature and/or power should be monitored during power cycle testing through the use of temperature and heater sensors to ensure that the test temperatures are within the test condition tolerances. This is done to ensure that the required temperature profile is being maintained throughout the test sequence. Since heaters can vary from part to part, it is recommended that there be separate power control systems for multiple heaters running in parallel. Also if external heaters or coolers are being used, their flatness and parallelism to the test device is very important. It is important to have a consistent bond line thickness across the heater adhesive with respect to any thermal interface material (TIM).

Electrical readouts can be performed in-situ or at intervals to evaluate thermal interface degradation, interconnect fatigue, chip to package interaction failures and package substrate integrity.

4.7 Test Precautions

Power measurement should not be based on values shown on the power supply. Voltage and current sense measurements should be taken across the heaters for power calculations.

Some form of continuous temperature measurement and appropriate shut down controls are also recommended to prevent temperature from exceeding the upper control limit.

4.8 Data Collection

Data collection should include at a minimum the appropriate electrical readouts, temperature profiles as measured by temperature sensors, voltage sense across the heaters, the temperature of test points of interest; e.g., test card and heat sink or package lid. Temperature data at different key points of interest (e.g., T_1 and T_2 of Figure A.1) should be used to characterize the spatial temperature distribution.

4.9 Visual and Electrical Measurements

Visual examination and electrical measurements, which consist of parametric and functional test, shall be performed as specified in the applicable procurement document or data sheet. Electrical test may be performed either in-situ or at an ambient or extreme temperature. Failure resistance criteria must be adjusted based on the temperature of the sample at point of readout.

5 Failure Criteria

Failure criteria shall include, but not be limited to, hermeticity for hermetic devices, parametric limits, functional limits and mechanical damage resulting in failure of the test point of interest. Parametric and functional limits shall be defined by the applicable procurement document. Mechanical damage failure shall not include damage induced by fixturing or handling or if the damage is not critical to the package performance in the specific application.

6 Summary

The following details shall be specified in the applicable procurement documents:

a) Means of heating for test and location of the heat source.

b) Brief description of sample fixturing.

c) Temperature extremes and associated tolerances, sample cooling and heating ramp rate and number of cycles, cycles per hour, soak time, or specific solid state device requirements.

d) Location of temperature measurements, temperature recording intervals and temperature profiles versus time for the test points of interest.

e) Specify power versus time for the test.

f) Interim measurement intervals, when required.

g) Special acceptance criteria for examinations, seal tests (for hermetic packages), internal bond integrity tests and electrical tests if other than those specified in the device specification.

h) For qualification testing, sample size and quality level.

i) Test hardware description.

j) Failure criteria.

Annex A (informative) Temperature Profile, Apparatus, and DUT Cooling

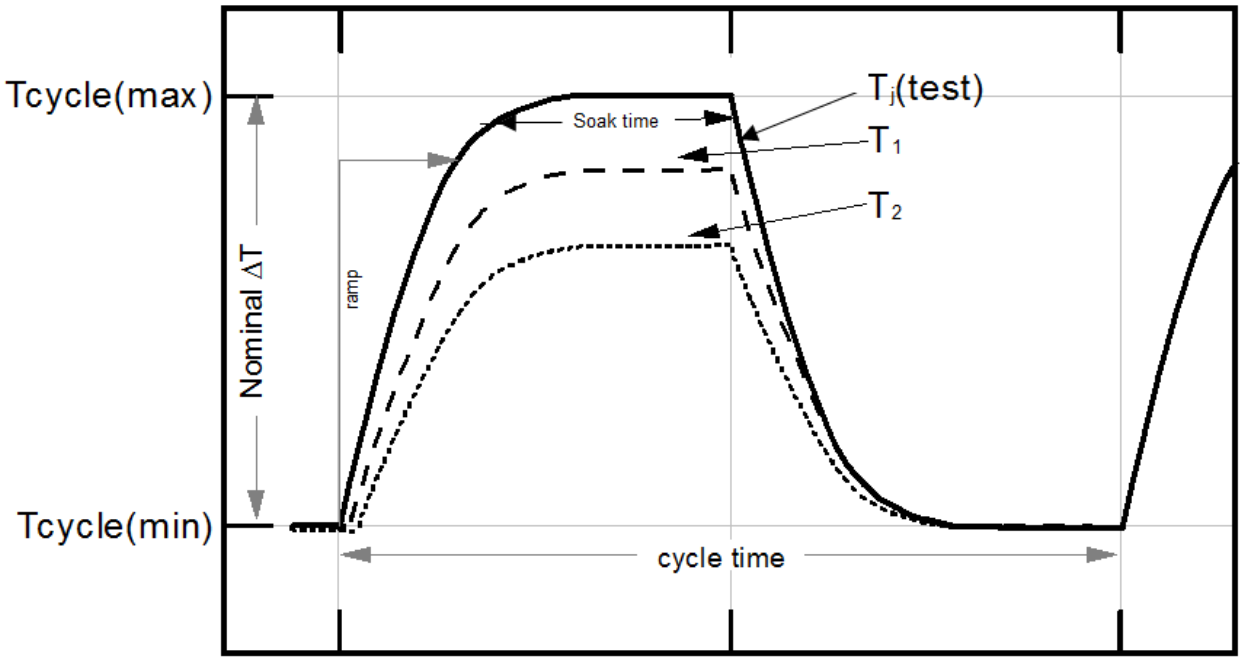


Figure A.1 — Representative Temperature Profile for Power Cycle Test Conditions

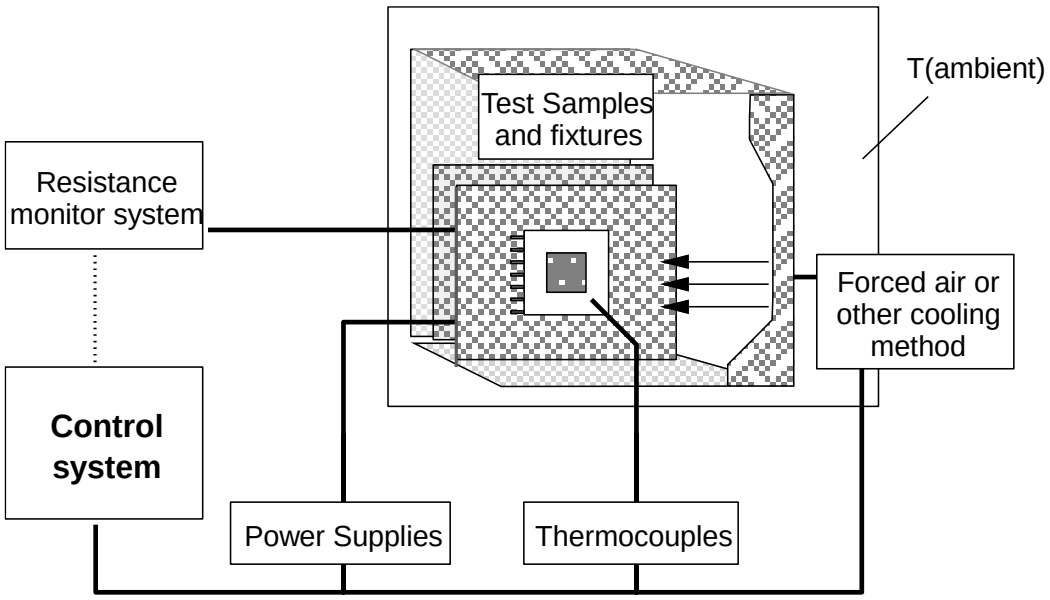
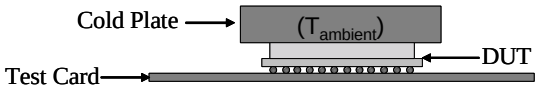
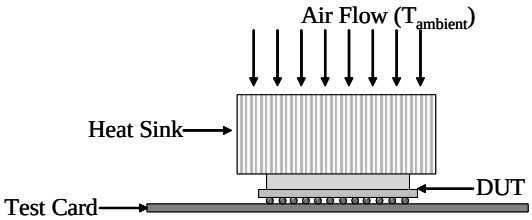
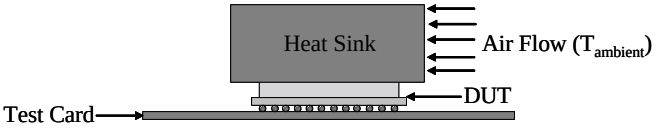


Figure A.2 — Typical Elements of a Power Cycle Test Apparatus

Annex A (informative) Temperature Profile, Apparatus, and DUT Cooling (cont'd)

Cooling Method	Sketch of Cooling Options
Water Cooled	
Air Cooled via impingement air flow	
Air Cooled via cross air flow	

NOTE The DUT should be oriented to represent the specific application and its associated air flow.

Figure A.3 — Examples of Cooling Options in Power Cycling

Annex B (informative) Differences between JESD22 A122B and its Predecessors

This annex describes most of the changes made to entries that appear in this standard, JESD22-A122B, compared to prior revisions. If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included in the list below. Some punctuation changes are not included in the list below.

B.1 Differences between JESD22-A122B and JESD22-A122A (June 2016)

Clause	Description of change
Introduction	Replaced the sentence: "Unlike either JESD22- A104 or JESD22-A105, the power cycles described in this test method are intended to simulate the range of usage conditions found from the vicinity of room ambient up to Tj maximum for the device, and are not specifically intended as a highly accelerated test or to apply to harsh application conditions such as those used to simulate some under-hood or aerospace environments." Shortened modified sentence: "Unlike either JESD22-A104 or JESD22-A105, the power cycles described in this test method are intended to simulate the range of usage conditions found from the vicinity of room ambient up to the maximum junction temperature for the device".
TOC	Added a Table of Contents.
Various	Fully justified text used throughout for consistency. Added margin in Table cells to improve readability. Headings changed to all caps format. Removed superfluous (cont'd) headings. Assigned heading Styles so that a Table of Contents could be automatically created. Removed clause heading numbers associated with "Terms" in section 2.
4.4	Inserted a border around Table 2 to contain the NOTEs, per JM7 formatting standard.
Annex A	Gave Annex A a title: "Temperature Profile, Apparatus, and DUT Cooling".

B.2 Differences between JESD22-A122A and JESD22-A122

Clause	Description of change
Several	The term "component" replaced by "solid state device"
2	Figure A.2, clear definition of Tj (test), $T_{cycle(\min)}$, T (ambient) Nominal ΔT Dwell time replaced by soak time
4.3	Tolerances aligned with other JEDEC standards
4.4	Additional explanation Table 2 and text boundary values aligned with JESD22-A104

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