JEDEC STANDARD

Power MOSFETs

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JULY 1985

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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POWER MOSFET's

(From JEDEC Council Ballot JCB-85-1, formulated under the cognizance of JC-25 Committee on Transistors.)

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CHAPTER 1

TERMS AND DEFINITIONS

1.1 INTRODUCTION

This chapter consists of a listing of terms and definitions and letter symbols that are used in other parts of this document and some are included for general information. Omitted from the list, however, are some special letter symbols of limited application whose use and definition are sufficiently close to those in this document to avoid the necessity of being included.

While the primary source for this listing is JEDEC Standard No. 77, the listing and the JC-25 JEDEC registration formats are recommended as more specialized reference material and have overriding authority where any conflicts may occur.

1.2 GENERAL TERMS AND DEFINITIONS

Term	Definition
breakdown	A phenomenon occurring in a reverse-biased semiconductor junction, the initiation of which is observed as a transition from a region of high small-signal resistance to a region of substantially lower small-signal resistance for an increasing magnitude of reverse current.
breakdown region	A region of the volt-ampere characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current.
breakdown voltage	The voltage measured at a specified current in a breakdown region.
channel	A thin semiconductor layer, between the source region and the drain region, in which the current is controlled by the gate potential.
depletion-mode operation	The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value decreases the magnitude of the drain current.
depletion-type transistor	A field-effect transistor having appreciable field-channel conductance for zero gate-source voltage; the channel conductance may be increased or decreased according to the polarity of the applied gate-source voltage.
drain	A region into which majority carriers flow from the channel. Note: Letter symbol is D or d.
dual-gate field-effect transistor	Alternate term for tetrode field-effect transistor.
electrode	An element that performs one or more of the functions of emitting or collecting electrons or holes, or of controlling their movement by an electric field.
enhancement-mode operation	The operation of a field-effect transistor such that changing the gate-source voltage from zero to a finite value increases the magnitude of the drain current.
enhancement-type field-effect transistor	A field-effect transistor having substantially zero channel conductance for zero gate-source voltage; the channel conductance may be increased by the application of a gate-source voltage of appropriate polarity.
field-effect transistor	A transistor in which the conduction is due entirely to the flow of majority carriers through a conduction channel controlled by an electric field arising from a voltage applied between the gate and source electrodes.
gate	The electrode associated with the region in which the electric field due to the control voltage is effective. Note: Letter symbol is G or g.
insulated-gate field-effect transistor	A field-effect transistor having one or more gate electrodes that are electrically insulated from the channel.

Term	Definition
junction (in a semiconductor device)	A region of transition between semiconductor regions of different electrical properties (e.g., n-n^+, p-n, p-p^+ semiconductors), or between a metal and a semiconductor.
junction-gate field-effect transistor	A field-effect transistor whose gate regions form p-n junctions with the channel. Usual abbreviation is "JFET".
metal-oxide-semiconductor field-effect transistor	An insulated field-effect transistor in which the insulating layer between each gate electrode and the channel is oxide material; the gate is metal or another highly conductive material. Usual abbreviation is "MOSFET".
n-channel field-effect transistor	A field-effect transistor that has an n-type conduction channel.
ohmic region	The region of the drain voltage-current characteristic curve in which a change in drain source voltage causes a proportional change in drain current.
open circuit	A circuit in which halving the magnitude of the terminating impedance does not produce a change in the parameter being measured greater than the required accuracy of the measurement.
p-channel field-effect transistor	A field-effect transistor that has a p-type conduction channel.
saturation region	The region of the drain voltage-current characteristic curve in which a change in drain-source voltage causes a relatively small change in drain current.
semiconductor device	A device whose essential characteristics are governed by the flow of charge carriers within a semiconductor.
short circuit	A circuit in which doubling the magnitude of the terminating impedance does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.
small signal	A signal that when doubled in magnitude does not produce a change in the parameter being measured that is greater than the required accuracy of the measurement.
source	A region from which majority carriers flow into the channel. Note: Letter symbol is S or s.
static value	A nonvarying value or quantity of measurement at a specified fixed point, or the slope of the line from the origin to the operating point of the appropriate characteristic curve.
substrate (of a semiconductor device)	The supporting material upon which or within which the elements of a semiconductor device are fabricated or attached.
terminal	An externally available point of connection.

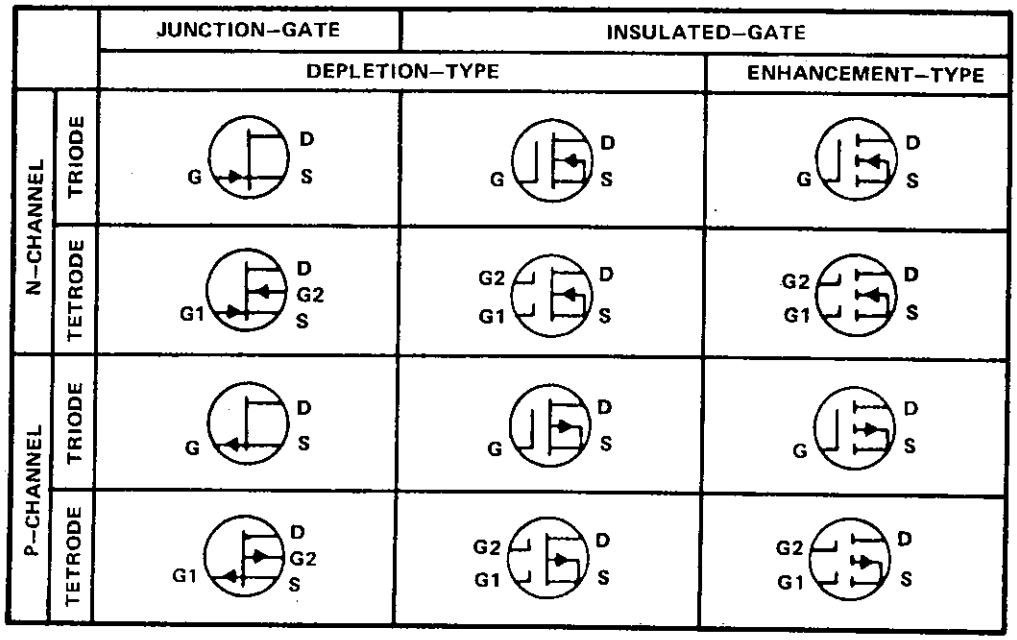


Figure A. Graphic Symbols for Field-Effect Transistors.

Term	Definition
tetrode field-effect transistor	A field-effect transistor having two independent gates, a source, and a drain. A substrate terminated externally and independently of other elements is considered a gate for the purposes of this definition. Note: Where no confusion is possible, the term may be abbreviated to "field-effect tetrode".
thermal resistance	The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium.
transient thermal impedance	The change in temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning the time interval and causing the change in temperature difference.
transistor	A semiconductor device capable of providing power amplification and having three or more electrodes. (Ref. IEC No. 147-0).
triode field-effect transistor	A field-effect transistor having a gate, a transistor source, and a drain. Note: Where no confusion is possible, the term may be abbreviated to "field-effect triode".
vertical field-effect transistor	A field-effect transistor in which the current between the drain and source electrodes is primarily normal to the top surface of the die. Note: The usual abbreviation is "VFET". If the device has an MOS structure, the usual abbreviation is "VMOS".

1.3 LETTER SYMBOLS, TERMS, AND DEFINITIONS

Symbol	Term	Definition
C_{ds}	drain-source capacitance	The capacitance between the drain and source terminals with the gate terminal connected to the guard terminal of a three-terminal bridge.
C_{dg}	drain-gate capacitance	See C_{rss}.
C_{gs}	gate-source capacitance	The capacitance between the gate and source terminals with the drain terminal connected to the guard terminal of a three-terminal bridge.
C_{iss}	short-circuit input capacitance, common-source	The capacitance between the input terminals (gate and source) with the drain short-circuited to the source for alternating current.
C_{oss}	short-circuit output capacitance, common-source	The capacitance between the output terminals (drain and source) with the gate short-circuited to the source for alternating current.
C_{rss}	short-circuit reverse transfer capacitance, common-source	The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three-terminal bridge.
g_{fs}, g_{is}, g_{os}, g_{rs}	common-source small-signal (forward transfer, input, output, reverse transfer) conductance	The real part of the corresponding admittance. See y_{fs}, y_{is}, y_{os}, and y_{rs}. Symbols in the forms of g_{xx} and $y_{xx(real)}$ are equivalent.
I_D	drain current, dc	The direct current into the drain terminal.
$I_{D(off)}$	drain cutofff current	The direct current into the drain terminal of a depletion-type transistor with a specified reverse gate-source voltage applied to bias the device to the off-state.
$I_{D(on)}$	on-state drain current	The direct current into the drain terminal with a specified forward gate-source voltage applied to bias the device to the on-state.
I_{DSS}	zero-gate-voltage drain current	The direct current into the drain terminal when the gate-source voltage is zero. Note: This is an on-state current in a depletion-type device, an off-state in an enhancement-type device.

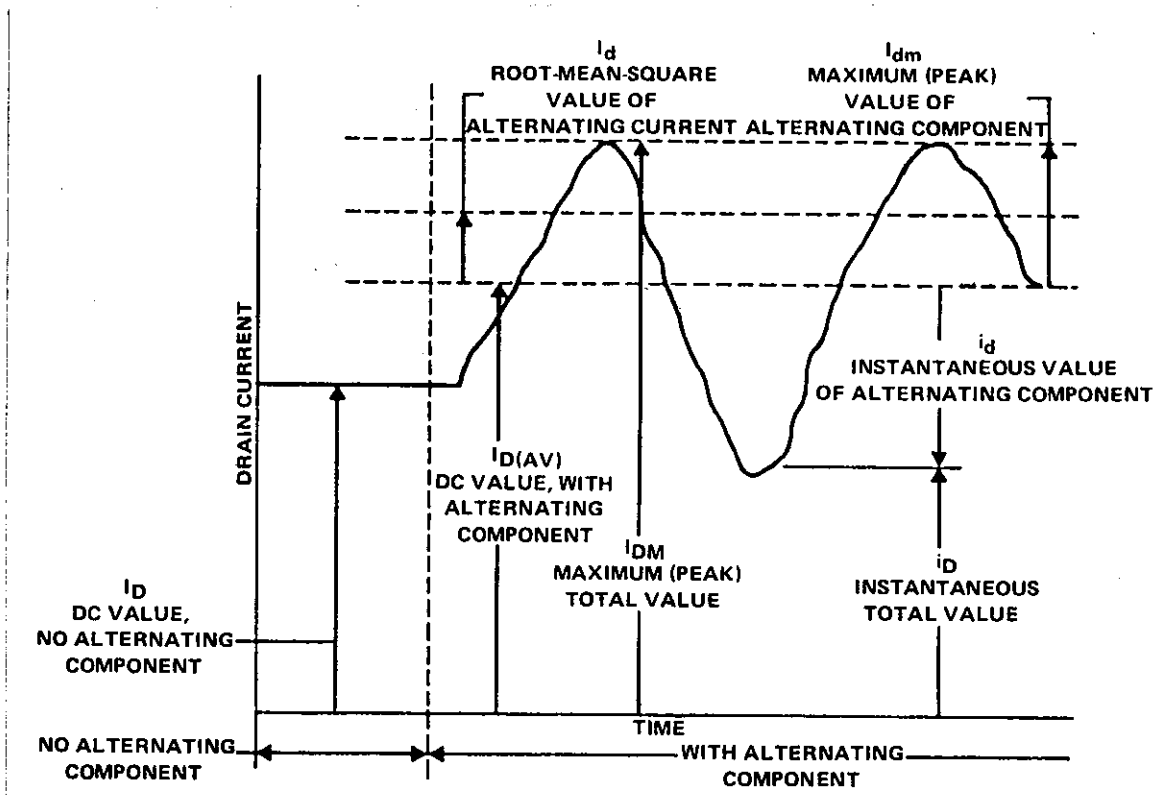


Figure B. Use of Letter Symbols (applies to any voltage or current terms).

Symbol	Term	Definition
I_G	gate current, dc	The direct current into the gate terminal.
I_{GF}	forward gate current	The direct current into the gate terminal with a forward gate-source voltage applied.
I_{GR}	reverse gate current	The direct current into the gate terminal with a reverse gate-source voltage applied.
I_{GSS}	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of a junction-gate field-effect transistor when the gate terminal is reverse biased with respect to the source terminal and the drain terminal is short-circuited to source terminal.
I_{GSSF}	forward gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated-gate field-effect transistor with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
I_{GSSR}	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated-gate field-effect transistor with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.
I_S	source current, dc	The direct current into the source terminal.

Symbol	Term	Definition
$I_{S(off)}$	source cutoff current	The direct current into the source terminal of a depletion-type transistor with a specified gate-drain voltage applied to bias the device to the off-state.
I_{SDS}	zero-gate-voltage source current	The direct current into the source terminal when the gate-drain voltage is zero. Note: This an an on-state current in a depletion-type device, an off-state current in an enhancement-type device.
P_T	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages.
p_T	nonreactive power input, instantaneous total, to all terminals	The sum of the products of the instantaneous input currents and voltages.
$r_{ds(on)}$	small-signal drain-source on-state resistance	The small-signal resistance between drain and source terminals with a specified gate-source voltage applied to bias the device to the on-state. Note: For a depletion-type device, the gate-source voltage may be zero.
$r_{DS(on)}$	static drain-source on-state resistance	The dc resistance between the drain source terminals with a specified gate-source voltage applied to bias the device to the on-state. Note: For a depletion-type device, the gate-source voltage may be zero.
R_θ	thermal resistance	(Refer to thermal resistance definition in Section 1.2).
$R_{\theta CA}$	thermal resistance, case-to-ambient	The thermal resistance (steady state) from the device case to the ambient.
$R_{\theta JA}$	thermal resistance, junction-to-ambient	The thermal resistance (steady state) from the semiconductor junction(s) to the ambient.
$R_{\theta JC}$	thermal resistance, junction-to-case	The thermal resistance (steady state) from the semiconductor junction(s) to a stated location on the case.
$R_{\theta JM}$	thermal resistance, junction-to-mounting surface	The thermal resistance (steady state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	ambient temperature or free-air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.

Symbol	Term	Definition
T_C	case temperature	The temperature measured at a specified location on the case of a device.
T_J	channel temperature	The temperature of the channel of a field-effect transistor.
T_{stg}	storage temperature	The temperature at which the device without any power applied, is stored.
t_c	turn-off crossover time (for reserve symbol, see t_{xo})	The time interval during which drain voltage rises from 10% of its peak off-state value and drain current falls 10% of its peak on-state value, in both cases ignoring spikes that are not charge-carrier-induced.
$t_{d(off)}$	turn-off delay time	Synonym for current turn-off delay time (see Note 1).
$t_{d(off)i}$	current turn-off delay time	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain current waveform falls to 90% of its on-state amplitude, ignoring spikes that are not charge-carrier-induced.
$t_{d(off)v}$	voltage turn-off delay time	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain voltage waveform rises to 10% of its off-state amplitude, ignoring spikes that are not charge-carrier-induced.
$t_{d(on)}$	turn-on delay time	Synonym for current turn-on delay time (see Note 1).
$t_{d(on)i}$	current turn-on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain current waveform rises to 10% of its on-state amplitude, ignoring spikes that are not charge-carrier-induced.
$t_{d(on)v}$	voltage turn-on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain voltage waveform falls to 90% of its off-state amplitude, ignoring spikes that are not charge-carrier-induced.
t_f	fall time	Synonym for current fall time (see Note 1).
t_{fi}	current fall time	The time interval during which the drain current changes from 90% to 10% of its peak on-state value, ignoring spikes that are not charge-carrier-induced.

Symbol	Term	Definition
t_{fv}	voltage fall time	The time interval during which the drain voltage changes from 90% to 10% of its peak off-state value, ignoring spikes that are not charge-carrier-induced.
t_{off}	turn-off time	Synonym for current turn-off time (see Note 1).
$t_{off(i)}$	current turn-off time	The sum of current turn-off delay time and current fall time, i.e., $t_{d(off)i} + t_{fi}$.
$t_{off(v)}$	voltage turn-off time	The sum of voltage turn-off delay time and voltage rise time, i.e., $t_{d(off)v} + t_{rv}$.
t_{on}	turn-on time	Synonym for current turn-on time (see Note 1).
$t_{on(i)}$	current turn-on time	The sum of current turn-on delay time and current rise time, i.e., $t_{d(on)i} + t_{ri}$.
$t_{on(v)}$	voltage turn-on time	The sum of voltage turn-on delay time and voltage fall time, i.e., $t_{d(on)v} + t_{fv}$.
t_p	pulse duration (formerly pulse time)	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform. Note: The two reference points are usually 90% of the steady-state amplitude existing before the leading edge. If the reference points are 50% points, the symbol t_w and term average pulse duration should be used.
t_r	rise time	Synonym for current rise time (see Note 1).
t_{ri}	current rise time	The time interval during which the drain current changes from 10% to 90% of its peak on-state value, ignoring spikes that are not charge-carrier-induced.
t_{rv}	voltage rise time	The time interval during which the drain voltage changes from 10% to 90% of its peak off-state value, ignoring spikes that are not charge-carrier-induced.
t_{ti}	current tail time	The time interval following current fall time during which the drain current changes from 10% to 2% of its peak on-state value, ignoring spikes that are not charge-carrier-induced.
t_w	average pulse duration (formerly pulse average time)	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge.

Symbol	Term	Definition
		Note: If the reference points are not 50% points, the symbol t_p and term pulse duration should be used.
t_{xo}	turn-off crossover time. (This is a reserve symbol to be used if use of t_c will cause confusion.)	For definition, see t_c.

Note 1: As names of time intervals for characterizing transistors, the terms "fall time" and "rise time" always refer to the change that is taking place in the magnitude of the output current even though measurements may be made using voltage waveforms. In a purely resistive circuit, the (current) rise time may be considered equal and coincident to the voltage fall time and the (current) fall time may be considered equal and coincident to the voltage rise time. The delay times for current and voltage will be equal and coincident. When significant amounts of inductance are present in a circuit, these equalities and coincidences no longer exist, and use of the unmodified terms delay time, fall time, and rise time must be avoided.

$V_{(BR)DSR}$	drain-source breakdown voltage with (resistance between gate and source,	The breakdown voltage between the drain terminal and the source terminal when the gate terminal is (as indicated by the last subscript letter) as follows:
$V_{(BR)DSS}$	gate short-circuited to source,	R = returned to the source terminal through a specified resistance
$V_{(BR)DSV}$	voltage between gate and source,	S = short-circuited to the source terminal
$V_{(BR)DSX}$	circuit between gate and source)	V = returned to the source terminal through a specified voltage X = returned to the source terminal through a specified circuit.
$V_{(BR)GSS}$	gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with the drain terminal short-circuited to the source terminal. Note: The symbol $V_{(BR)GSS}$ is primarily used with junction-gate field-effect transistors. The symbols $V_{(BR)GSSR}$ or $V_{(BR)GSSF}$ should be used with insulated-gate transistors having shunting diodes or similar voltage-limiting devices.
$V_{(BR)GSSF}$	forward gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
$V_{(BR)GSSR}$	reverse gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.

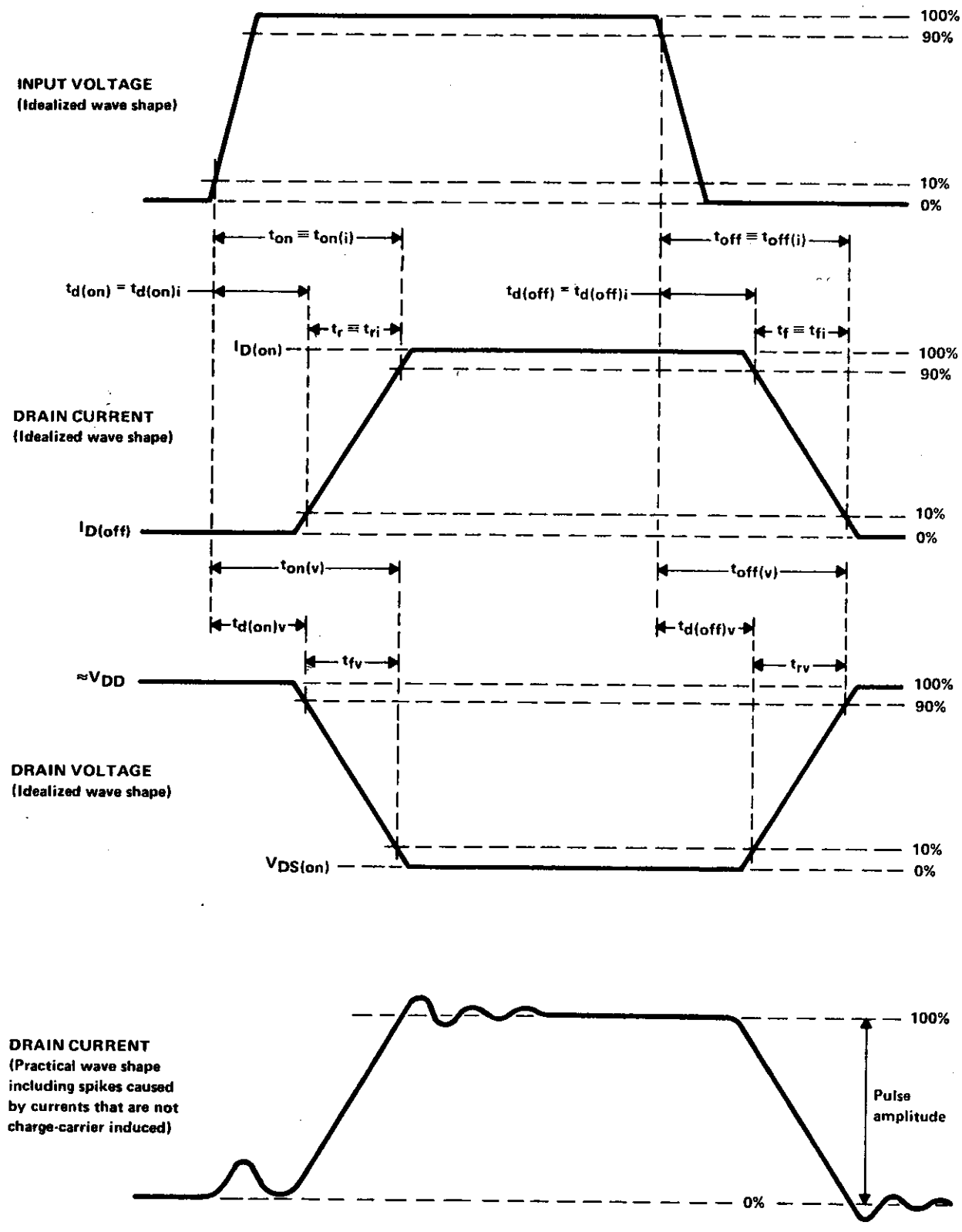
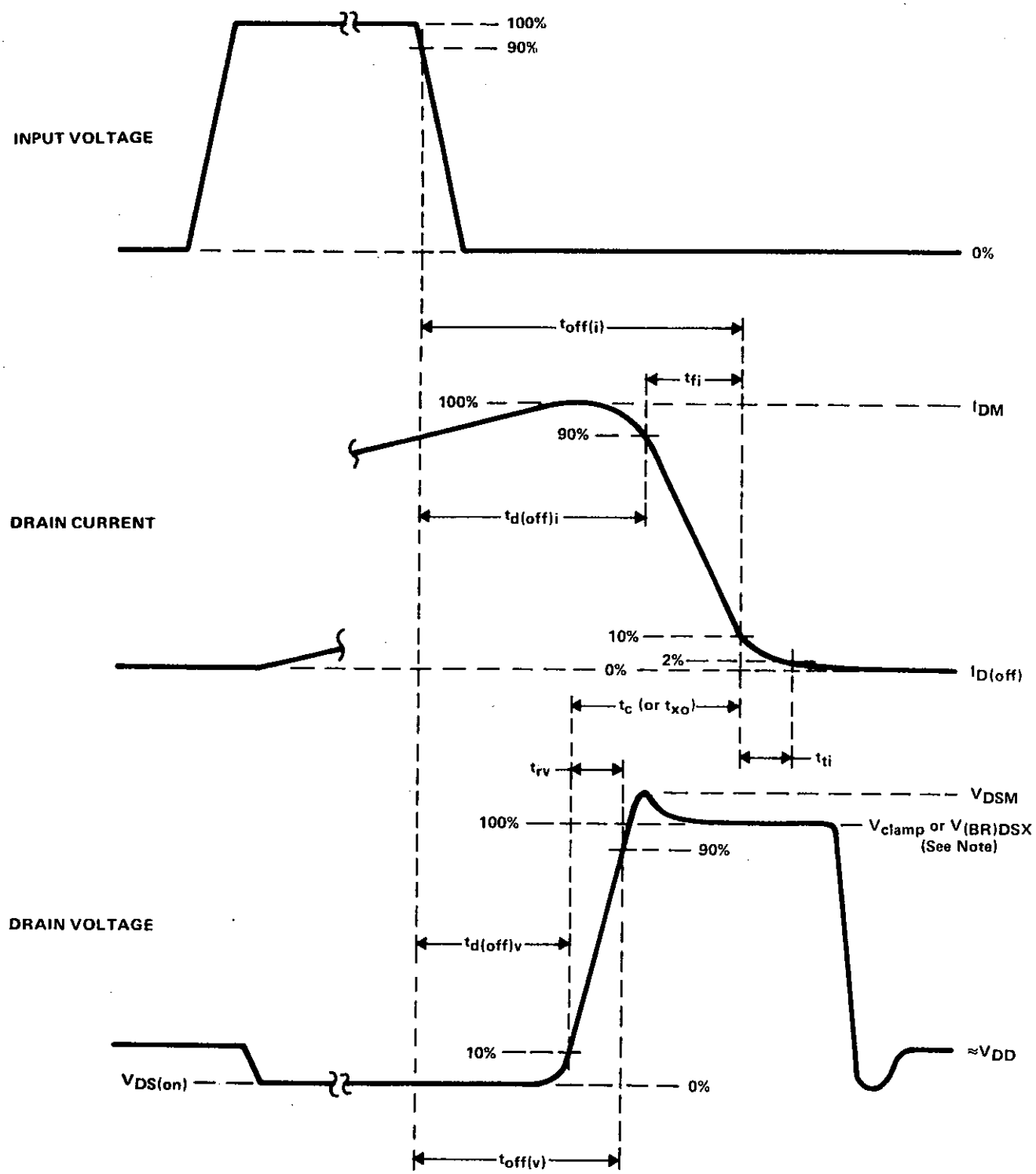


Figure C. Waveforms for Resistive-Load Switching.



NOTE: V_{clamp} (in a clamped inductive-load switching circuit) or $V_{(BR)DSX}$ (in an unclamped circuit) is the peak off-state voltage excluding spikes.

Figure D. Waveforms for Inductive-Load Switching, Turn-Off

Symbol	Term	Definition
V_{DD}, V_{GG}, V_{SS}	supply voltage, dc (drain, gate, or source)	The dc supply voltage applied to a circuit connected to the reference terminal.
V_{DG}, V_{DS}, V_{GD}, V_{GS}, V_{SD}, V_{SG}	voltage, dc drain-to-gate, drain-to-source, gate-to-drain, gate-to-source, source-to-drain, source-to-gate	The dc voltage between the terminal indicated by the first subscript and the reference terminal indicated by the second subscript (stated in terms of the polarity at the terminal indicated by the first subscript).
$V_{DS(on)}$	drain-source on-state voltage	The voltage between the drain and source terminals with a specified forward gate-source voltage applied to bias the device to the on-state.
V_{GSF}	forward gate-source voltage, dc	The voltage between the gate and source terminals of such polarity that an increase in its magnitude causes the channel resistance to decrease.
V_{GSR}	reverse gate-source voltage	The voltage between the gate and source terminals of such polarity that an increase in its magnitude causes the channel resistance to increase.
$V_{GS(off)}$	gate-source cutoff voltage (of a depletion-type FET)	The gate-source voltage at which the magnitude of the drain current reaches a specified low value.
$V_{GS(th)}$	gate-source threshold voltage (of an enhancement-type FET)	The gate-source voltage at which the magnitude of the drain current reaches a specified low value.
y_{fs}	common-source small-signal short-circuit forward transfer admittance	The ratio of rms drain current to rms gate-source voltage with the drain terminal ac short-circuited to the source terminal.
y_{is}	common-source small-signal short-circuit input admittance	The ratio of rms gate current to rms gate-source voltage with the drain terminal ac short-circuited to the source terminal.
y_{os}	common-source small-signal short-circuit output admittance	The ratio of rms drain current to rms drain-source voltage with the gate terminal ac short-circuited to the source terminal.
y_{rs}	common-source small-signal short-circuit reverse transfer admittance	The ratio of rms gate current to rms drain-source voltage with the gate terminal ac short-circuited to the source terminal.

Symbol	Term	Definition
$Z_{\theta(t)}$	transient thermal impedance	(Refer to transient thermal impedance definition in Section 1.2).
$Z_{\theta JA(t)}$	transient thermal impedance, junction-to-ambient	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\theta JC(t)}$	transient thermal impedance, junction-to-case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

CHAPTER 2

REGISTRATION

2.1 INTRODUCTION

This chapter briefly describes established procedures that are followed in the assignment of semiconductor-industry-type designations to power transistors. These procedures are discussed from the standpoints of both administration by JEDEC and compliance by the device manufacturer.

The material in Section 2.2 on type assignments is based upon JEDEC Publication No. 15C where the procedures are discussed in detail. The material in Sections 2.3 and 2.4 is adopted from JEDEC Publication No. 74.

2.2 TYPE ASSIGNMENT

2.2.1 Purpose and Intent

The purpose of the type designation and registration system is to facilitate the purchase and distribution of solid state devices by nontechnical individuals. The registration procedures are designed to ensure that devices registered with the Council differ from each other in performance characteristics or physical dimensions.

The following is a partial list of the many ways in which the JEDEC registration system is useful to many segments of the electronics industry:

(1) A single number replaces the multiple house numbers that would be used where there are two or more manufacturers of a particular device. This advantage is of particular value to the larger consumer such as the government, because it means in most cases the procurement and supply of a single item, instead of multiple items.

(2) The existence of a nationally recognized designation encourages other manufacturers to make similar devices, thereby increasing and promoting competition.

(3) Types registered under the JEDEC system differ from each other in a significant manner in terms of performance characteristics or physical dimensions.

(4) Types registered under the JEDEC system can be more easily compared because defining characteristics of the specification must be based upon standard test conditions and registered according to standard formats.

(5) The publication of registration information through trade channels makes it easier for consumers to obtain second sources of supply.

(6) The specifications of registered devices carrying the authorized designations cannot be changed at will by the first or any subsequent manufacturer, thus promoting standardization and interchangeability.

(7) In many cases it provides for nontechnical personnel of user procurement, and stock and maintenance operations to obtain the equivalent replacement parts.

(8) It provides a permanent record for future procurement in those cases where the original manufacturers no longer exist or make the type.

(9) It provides an identification system of parts which is of large benefit to the distributors and users of electronic parts. The JEDEC system permits reduction in the required number of parts in inventory.

Registration consists of the assignment of type designations to solid state devices in accordance with established rules, recording of the assignment and defining data, and the full dissemination of the information to the electronics industry. Registration procedures and rules are established by JEDEC, which is sponsored jointly by EIA and NEMA. In any event, JEDEC neither assumes liability for, nor endorses, the use of any products which bear its authorized registration number. The Council has as its primary objective the development of recommended standards in the field of solid-state devices. An effective registration procedure is considered basic to the achievement of that objective.

2.2.2 Brief Outline of Registration Procedures

(1) Request

The manufacturer furnishes to the Type Administrator defining data for a device in accordance with the applicable registration format and requests assignment of a type designation.

(2) Assignment

The Type Administrator assigns a type designation and notifies the manufacturer of the assignment.

(3) Release (Public Announcement)

Within one hundred and twenty (120) days after date of assignment, the Type Administrator announces the registration of the type by distributing the data to the manufacturers of solid state devices and to users.

(4) Correction Notice and Registration

Once data on a type have been released, it is possible to change the defining data for that type only by either of two methods: a correction notice or a reregistration. In those cases where an error has been discovered in the data submitted, a correction notice may be filed only by the original sponsor or the Type Administrator within sixty (60) days after registration. Any device manufacturer may, at any time, propose a reregistration to change the registered values for a device. In order for a change to be adopted, however, there must be no opposition to the proposal from any other manufacturer of the device.

2.2.3 Description of Registration Format

A format is intended to provide a uniform method of presentation of definition and performance of a JEDEC registered device. The Type Administrator uses the completed format to assure the uniqueness of the device for type assignment purposes. The registrant manufacturer uses the format to completely define a device to the degree which the formulating Committee and Council believe necessary to assure device interchangeability. Other potential manufacturers use the completed format and registration data to facilitate and assure device interchangeability. Solid-state device users employ the completed registration data to select, compare, and define devices to achieve intended circuit performance. The format provides for a common language of understanding between supplier and user.

Each format provides for specific values of mechanical and electrical parameters in two categories. One is for mandatory parameters, and the Type Administrator will not accept a proposed registration unless every such parameter is provided. The other is for additional parameters which the formulating Committee believes desirable for the further definition of a device intended for a normal application. Additional data not listed in a format is permissible if the registrant manufacturer believes it is necessary to further define the device and to assure interchangeability.

The Type Administrator must receive a properly completed registration format in order to issue a JEDEC-type number assignment. In the event an appropriate format has not been prepared by the JEDEC Committees, the Type Administrator, with advice from Council or Committee Chairmen, will determine what shall constitute an interim substitute format. A completed format characterizes a device by listing or referencing all mechanical outline dimensions and terminal identification, all essential electrical performance data and maximum ratings, all necessary test methods, and all appropriate parameter symbols which are believed necessary to assure device interchangeability. Each JEDEC product committee originates formats for each device category over which it has been assigned responsibility. Each format is approved for circulation and use by the JEDEC Council. JEDEC Committees have the responsibility for maintaining and upgrading the technical content of formats such that they reflect the advancement of the technology of both design and manufacture. Mechanical and electrical parameters are to be listed as minimum, maximum, or rated values required to assure device interchangeability.

2.2.4 Use of a Format and JEDEC Registered Data

The solid-state device manufacturer should use the JEDEC data for a registered device as the basis for his commercial data. Since the JEDEC registration data are industry property, each manufacturer who desires to produce and market that device must comply in every respect with the registered data. Commercial data describing that device must identify by asterisks all parameters which appear on the JEDEC registration. If a manufacturer believes it desirable, he may list additional defining data, such as performance curves or quality items, provided such additions do not affect interchangeability.

JEDEC Council reserves all rights to the use of its symbols. The Armed Services make use of JEDEC designations and are permitted to modify these designations by means of prefixes to indicate conformance with military specifications.

2.2.5 Test and Rating Methods Applied to JEDEC Data

Defining data on a format must be supported by sufficient reference or included information to assure an understanding of the test methods used in the mea-

surement and interpretation of data and ratings. It is the responsibility of the formulating JEDEC Committee and Council to define as many of the following test methods, conditions, and other information, as appropriate for the device or format under consideration:

(1) Standard circuits for the measurement of electrical characteristics

(2) Standard circuits for life testing of semiconductor devices

(3) Standard mechanical tests (shock, vibration, etc.)

(4) Standard fixtures and gauges

(5) Standard failure defining criteria

(6) Standard time duration of test when applicable (hours, cycles, pulses, etc.)

(7) Standard definition of allowable number of defective units, when absolutely necessary, in the establishment of a rating.

There should be no question as to the intention behind, or interpretation of, any parameter or test listed on a format.

2.3 STANDARD VALUES FOR USE IN REGISTRATION

2.3.1 Introduction

This section contains lists of standard values which are recommended for use in power transistor device specifications and JEDEC Registration to JC-25 Formats. Reasons for deviations should be sent to the Type Administrator in those cases where values are used which are not included in these lists.

2.3.2 Standard Values for Ratings

(1) Voltage

(a) for $\leq$ 300 V: Rounded 13 series*

(b) for $>$ 300 V: Increments of 50 V.

(2) Current: Rounded 13 series*

(3) Temperature (storage and operating): -65, -55, -40, -25, $+100$, $+125$, $+150$, $+175$, $+200$, $+250°$(C)

(4) Power: Rounded 13 series*

Case temperatures are selected from item 2.3.3.

2.3.3 Standard Values for Characteristics

(1) Specified limits: Rounded 13 series*

(2) Test Voltages and Currents: Rounded 13 series*

(3) Case Temperature: -65, -55, -40, -25, 0, $+25$, $+70$, $+85$, $+100$, $+125$, $+150$, $+175$, $+200°$(C)

2.4 MINIMUM DIFFERENCE STANDARD VALUES FOR DISCRETENESS OF REGISTRATION

2.4.1 Introduction

This section provides lists of minimum differences in ratings and characteristics that are recommended for use in determining if a transistor proposed for registration is sufficiently different from those already registered.

Discreteness of any one rating or characteristic listed below on the basis of the minimum difference indicated is sufficient for transistor discreteness, provided that rating or characteristic is required by the registration format. Changes in ratings and characteristics not required in the registration format are not criteria for discreteness.

Most of the minimum differences indicated are given in terms of standard steps. A standard step refers to the steps in the series of standard values listed in Section 2.3.

2.4.2 Minimum Difference for Ratings

(1) Voltage, drain-to-source (V_{DS}): one standard step.

(2) Current, continuous drain (I_D): two standard steps.

(3) Power, continuous (P_T):

(a) for $\leq$ 150 W: two standard steps

(b) for $>$ 150 W: one standard step

(4) Temperature, operating junction (T_j), and storage (T_{stg}):

two standard steps.

2.4.3 Minimum Differences for Characteristics

(1) Transconductance (g_{fe}):

* 1.0, 1.2, 1.5, 1.7, 2.0, 2.5, 3.0, 3.5, 4.0, 5.0, 6.0, 7.0, 8.0, $\times 10^n$; where n is an integral number.

(a) for increase or decrease of both upper and lower limits: one standard step

(b) for change in only lower limit: two standard steps. (change in upper limit alone is not a criteria).

(2) Input capacitance (C_{iss}), Reverse transfer capacitance (C_{rss}), and output capacitance (C_{oss}): two standard steps.

(a) as above, under item 1

(b) for change in only upper limit: two standard steps (change in lower limit alone is not a criteria).

(3) Drain-source resistance $r_{DS(on)}$: two standard steps.

(4) Drain cut-off current (I_{DSS} for MOSFET, $I_{D(off)}$ for JFET): two orders of magnitude.

(5) Threshold voltage $V_{GS(th)}$: two standard steps

(a) as above, under item 1

(b) for change in only upper limit: two standard steps (change in lower limit alone is not a criteria).

CHAPTER 3

ELECTRICAL VERIFICATION TESTS

3.1 INTRODUCTION

All measurements should be made at thermal equilibrium. A condition of thermal equilibrium is achieved if halving the time between application of power and measurement causes no change in the result within the required accuracy. Unless specified otherwise, the transistor case temperature should be maintained at approximately 25°C by use of an appropriate heat sink, when necessary.

The connecting lines shown in the circuit diagrams have negligible resistance compared to their lowest terminating impedance. Shown are resistors, inductors, and capacitors having an ideal characteristic at the used frequency range. The battery symbol indicates voltage sources having zero impedance, which in practice requires use of generous by-passing, and current sources approximate an infinite resistance. In practice, power supplies having current limiting should be used for voltage sources. All voltmeters and scopes have infinite input resistance and all ammeters have zero resistance, unless otherwise noted; a practical approximation to these ideals is achieved if doubling or halving does not produce a change in the measured values that exceeds the accuracy of the test. All circuit values are nominal and should be achieved within limits of a few percent or as dictated by equipment capabilities consistent with good engineering practice.

The listing of the following tests does not imply that all must be performed by either the manufacturer or the user. It is the responsibility of the user and manufacturer to agree to any series of specific tests or test conditions, and the further responsibility of the user to establish meaningful relationships between these tests and the performance of the power MOSFET in a particular application.

Except when not applicable, the MOSFET connections are shown for a "dc" technique; the same general configuration applies when a pulse technique or a curve tracer is used to perform the test.

An n-channel enhancement type transistor is shown as the transistor under test in the test circuits. These test methods will also apply to p–channel devices by appropriate polarity changes in the test circuit elements.

As many power MOSFETs have cut-off frequencies on the order of a gigahertz, parasitic oscillations may be troublesome unless certain precautions are observed. Usually oscillations are prevented by observing the following guidelines:

(1) Keep lead and trace lengths short.

(2) Place ferrite beads on the gate lead close to the gate terminal or use a resistor of 100 to 1000 Ω in series with the gate.

(3) Avoid a layout which may couple output signal to the input.

(4) Surround the MOSFET with a ground plane and shield output from input.

(5) Use noninductive resistors.

Except where specifically noted, the tests apply whether or not gate protection elements are included in the MOSFET. Protection elements are shown as zener diodes, although they need not necessarily be of this type. Depletion-mode transistors are not specifically covered in the material which follows.

3.2 MAXIMUM RATINGS

3.2.1 Introduction

This section describes tests which are intended to verify the maximum ratings given in transistor registration formats; they are not tests used for developing the maximum ratings nor are they intended for establishing performance or quality levels.

3.2.2 Verification Criteria

To verify a given maximum rating for a transistor, the transistor shall be tested as described in the applicable subsection. The transistor shall be capable of meeting all the electrical characteristics of the registration at the conclusion of the test procedure, after the transistor has been allowed to reach thermal equilibrium at 25°C or other specified temperature.

3.2.3 Storage Temperature, Minimum

3.2.3.1 Test Conditions

(1) Storage temperature at rated T_{stg} (min.)

(2) Test duration of six (6) hours at the rated T_{stg} (min.)

3.2.3.2 Procedure

A temperature-controlled enclosure shall be used.

3.2.4 Storage Temperature, Maximum – T_{stg} (max.)

3.2.4.1 Test Conditions

(1) Storage temperature at rated T_{stg} (max.)

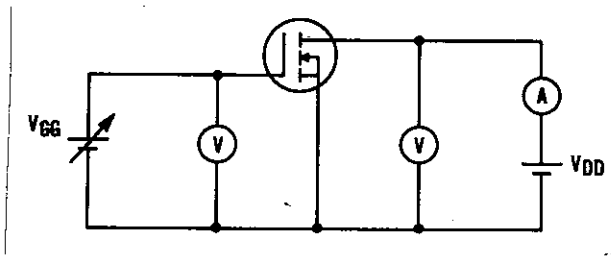
(2) Test duration of six (6) hours at the rated T_{stg} (max.)

3.2.4.2 Procedure

A temperature-controlled enclosure shall be used.

3.2.5 Junction Temperature, Maximum Operating – T_j (max.)

3.2.5.1 Test Circuit and Conditions



(1) $V_{DS} = V_{DS2}$ as specified on the device registration.

(2) P_T = 10% of maximum rated P_{T2} on the device registration.

(3) $T_C = T_{j(max)} - (0.1)R_{\theta JC}\ P_{T2}$.

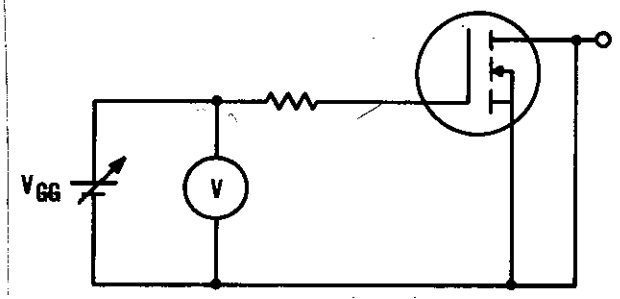
(4) The duration of the test shall be five (5) minutes, measured after a steady-state condition is reached.

3.2.5.2 Procedure

Adjust the bias conditions to achieve the specified V_{DS} and P_T. In doing so, do not exceed the rated maximum values for V_{GS} and V_{DS} of the device.

3.2.6 Forward and Reverse Gate–Source Voltage, Maximum – V_{GSF} and V_{GSR}

3.2.6.1 Test Circuit and Conditions



(1) V_{GG} = Rated V_{GSF} or V_{GSR} on the device registration.

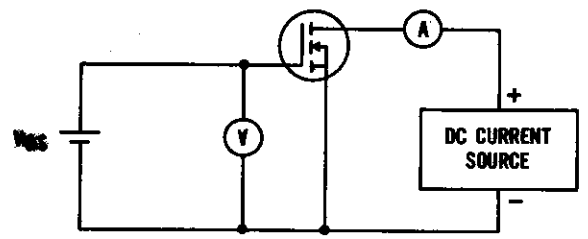
(2) The duration of the test shall be one (1) minute.

3.2.6.2 Procedure

Adjust the bias supply to attain the specified V_{GS}.

3.2.7 Drain Current, Maximum Continuous – I_D

3.2.7.1 Test Circuit and Conditions



(1) The gate voltage, V_{GS}, is that specified for $r_{DS(on)}$ at rated I_D.

(2) Duration of the test at the rated value for I_D shall be one (1) minute.

3.2.7.2 Procedure

(1) Increase the gate voltage to obtain the specified V_{GS}.

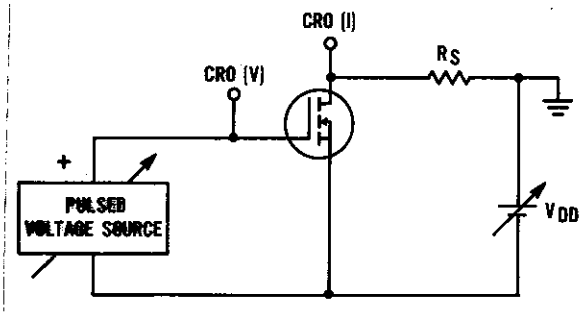
(2) Increase the drain current until the rated I_D is reached.

(3) Measure V_{DS}.

(4) $V_{DS} \times I_D \leq P_T$ rated V_{TC} = 25°C or as registered.

3.2.8 Drain Current, Maximum Pulsed – I_{DM}

3.2.8.1 Test Circuit and Conditions



(1) The amplitude, pulse width, and duty cycle of the pulsed voltage source shall be as specified for $r_{DS(on)}$ at rated I_{DM}.

(2) $R_S \simeq 10 r_{DS(on)}$.

(3) The duration of the test shall be that time adequate to make the reading.

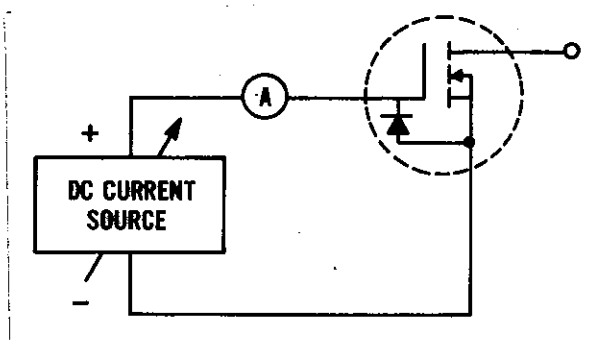
3.2.8.2 Procedure

(1) Adjust the pulse generator to obtain the specified drive pulse amplitude, width, and duty cycle.

(2) Adjust V_{DD} to obtain the rated I_{DM}.

3.2.9 Forward and Reverse Gate Current, Maximum Continuous – I_{GF} and I_{GR} (for MOS devices with a gate protection element)

3.2.9.1 Test Circuit and Condition



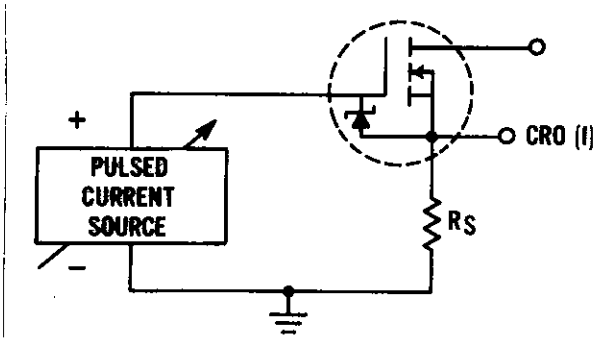
Duration of the test at the rated value for I_{GF} shall be one (1) minute.

3.2.9.2 Procedure

Adjust the current source to obtain the rated I_{GF} or I_{GR}.

3.2.10 Forward and Reverse Gate Current, Maximum Pulsed – I_{GFM} and I_{GRM}

3.2.10.1 Test Circuit and Conditions



(1) R_S is a small current viewing resistor.

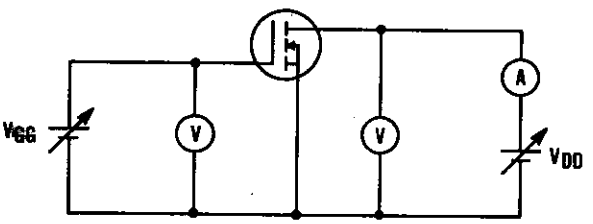
(2) The duration of the test shall be that time adequate to make the reading.

3.2.10.2 Procedure

Adjust the pulsed current source amplitude, pulse width, and duty cycle to obtain the rated I_{GFM} or I_{GRM}.

3.2.11 Power Dissipation, Maximum Continuous – P_D

3.2.11.1 Test Circuit and Conditions



(1) The case temperature, T_C, must be 55°C for all devices rated for operating junction temperatures of 125°C or less, or 100°C for all devices rated for operating junction temperatures above 125°C.

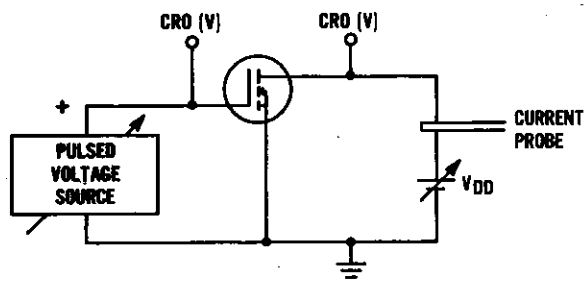
(2) The duration of the test shall be five (5) minutes, measured after thermal equilibrium at the required case temperature is reached.

3.2.11.2 Procedure

Adjust the bias conditions to achieve the specified V_{DS2} and P_{T2} on the device registration.

3.2.12 Power Dissipation, Maximum Peak – P_{DM}

3.2.12.1 Test Circuit and Conditions



(1) T_C = 25°C or as specified.

(2) The pulse width and duty cycle of the pulse voltage source shall be as specified in the device specification.

(3) The duration of test shall be that time adequate to make the reading.

3.2.12.2 Procedure

Increase the amplitude of the pulsed voltage source to obtain the rated P_{DM} at the specified V_{DS}.

3.3 ELECTRICAL CHARACTERISTIC TESTS

These tests are normally performed on production runs, at outgoing quality control, incoming inspection, or when characterizing devices.

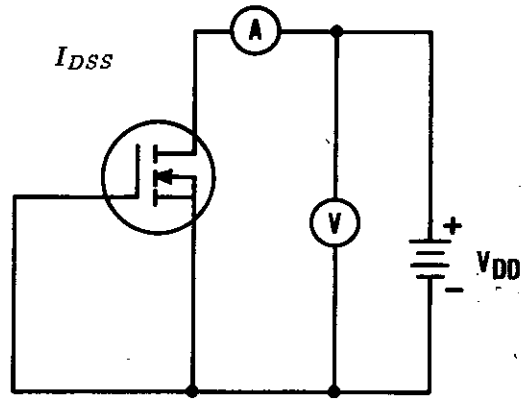
3.3.1 Cut–Off Currents – I_{DSS}, I_{GSS}, I_{GSSF}, I_{GSSR}

3.3.1.1 Description

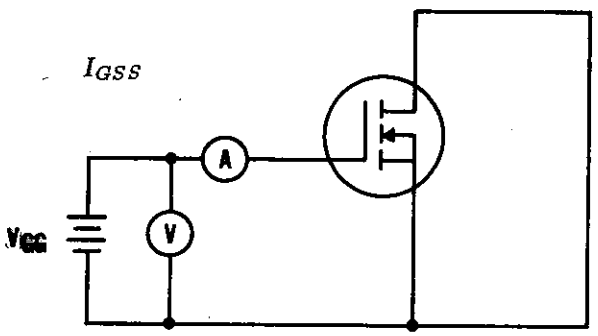
The cut-off currents are the residual currents which flow when the bias is such that the transistor is in the off-state.

The cut-off current is temperature sensitive. If testing is done at elevated temperature, a heat sink may be necessary to ensure a stable case temperature especially if continuous voltages are used.

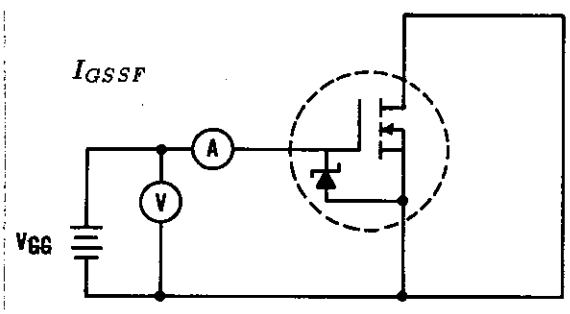
3.3.1.2 Test Circuits



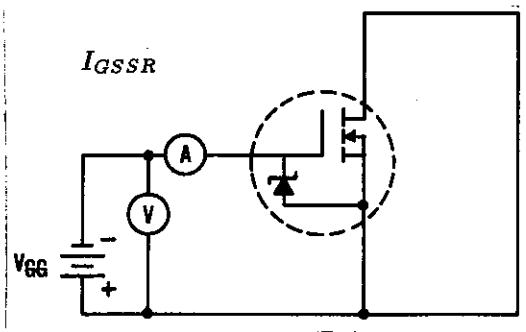
Circuit A



Circuit B



Circuit C



Circuit D

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3.3.1.3 Test Conditions to be Specified

(1) Zero Gate Voltage Drain Current – I_{DSS}. See circuit A.

(a) Case Temperature: T_C (only if $T_C \neq 25°C$)

(b) Drain-Source Voltage: V_{DS}

(c) Gate-Source Voltage: $V_{GS} = 0$

(2) Gate Current, Drain Short-Circuited to Source – I_{GSS}. See circuit B. (Applies for parts without gate protection elements and for either polarity of V_{GG}.)

(a) Case Temperature: T_C (only if $T_C \neq 25°C$)

(b) Drain-Source Voltage: $V_{DS} = 0$

(c) Gate-Source Voltage: V_{GS}

(3) Forward Gate Current, Drain Short-Circuited to Source – I_{GSSF}. See circuit C. (Applies for parts with gate protection elements.)

See (2) above.

(4) Reverse Gate Current, Drain Short-Circuited to Source – I_{GSSR}. See circuit D. (Applies for parts with gate protection elements.)

See (2) above.

3.3.1.4 Procedure

(1) I_{DSS}: Drain voltage is applied and the current is measured after a stable value is observed.

(2) I_{GSS}:
(3) I_{GSSF}:
(4) I_{GSSR}:

Gate voltage is applied and the gate current is measured after a stable value is observed.

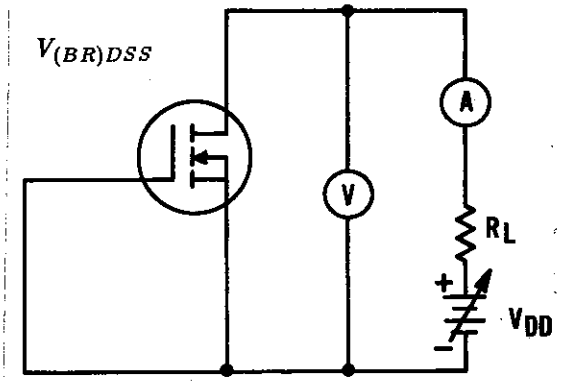
3.3.2 Breakdown Voltage – $V_{(BR)DSS}$, $V_{(BR)DSX}$, $V_{(BR)GSS}$

3.3.2.1 Description

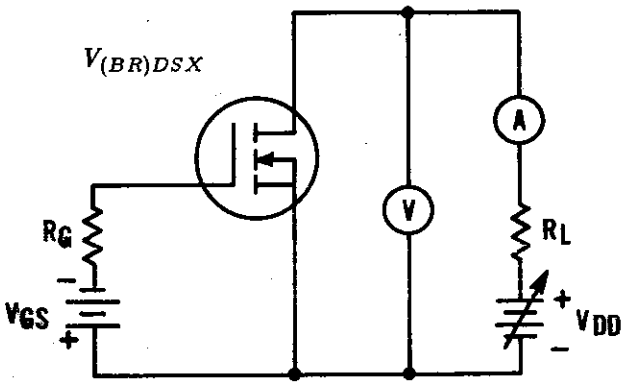
Breakdown voltage tests are necessary when characterizing parts. Breakdown tests are not used to verify voltage ratings, as measuring the breakdown voltage will, of necessity, cause the voltage rating to be exceeded and may damage the transistor.

To yield meaningful results, the current used for this test should be as low as possible, but must be sufficient to ensure that the breakdown voltage is relatively insensitive to current changes.

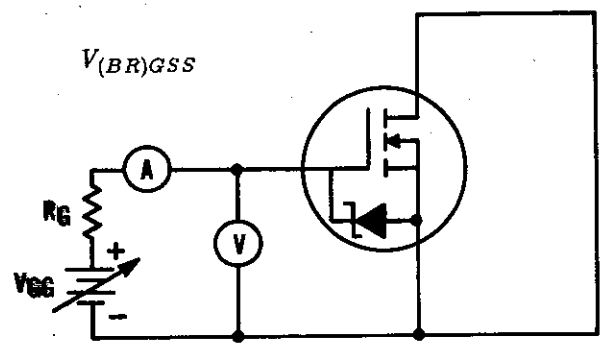
3.3.2.2 Test Circuits



Circuit A



Circuit B



Circuit C

3.3.2.3 Test Conditions to be Specified

(1) Drain-Source Breakdown Voltage – $V_{(BR)DSS}$. See circuit A.

(a) Case Temperature: T_C (if $T_C \neq 25°C$)

(b) Drain Current: I_D

(2) Drain-Source Breakdown Voltage – $V_{(BR)DSX}$. See circuit B.

(a) Case Temperature: T_C (if $T_C \neq 25°C$)

(b) Gate Supply Voltage: V_{GG}

(c) Gate Resistance: R_G

(d) Drain Current: I_D

(3) Gate-Source Breakdown Voltage – $V_{(BR)GSS}$. See circuit C (for gate protected parts only)

(a) Case Temperature: T_C (if $T_C \neq 25°C$)

(b) Gate Current: I_G

3.3.2.4 Procedure

(1) $V_{(BR)DSS}$

The drain supply V_{DD} is increased to achieve the required drain current. After a stable level is achieved, the drain-source voltage is measured.

(2) $V_{(BR)DSX}$

The gate supply voltage V_{GG}, is applied first. The drain supply V_{DD} is then increased to achieve the required drain current. After a stable level is achieved, the drain-source voltage is measured.

(3) $V_{(BR)GSS}$

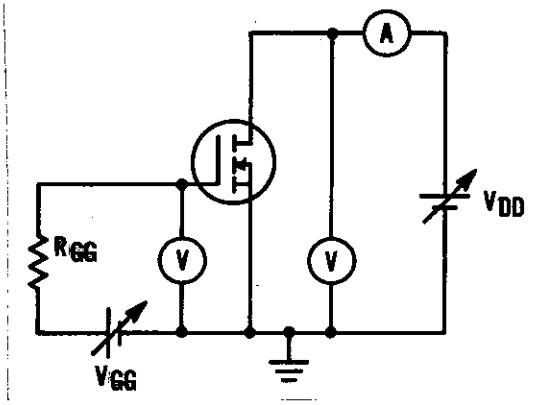
The gate supply voltage, V_{GG}, is increased to achieve the required gate current. After a stable level is achieved, the gate-source voltage is measured. Forward breakdown, $V_{(BR)GSSF}$, and reverse breakdown, $V_{(BR)GSSR}$, are measured identically except for the polarity of V_{GG}.

3.3.3 On–State Drain Current – $I_{D(on)}$

3.3.3.1 Description

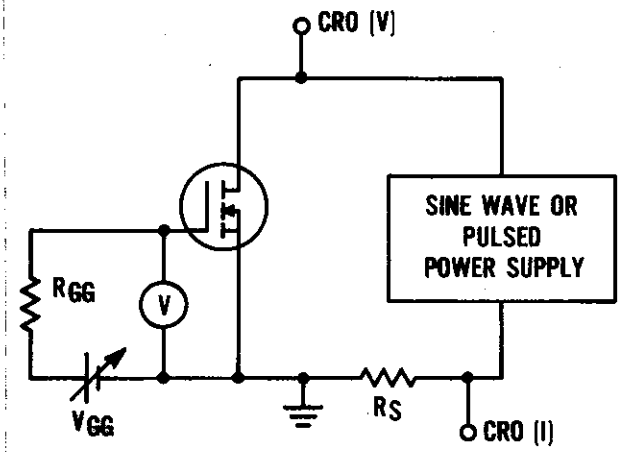
On-state drain current is a measure of the gain of the device. Together with the threshold voltage, it permits the transfer curve to be approximated.

3.3.3.2 Test Circuits



Continuous dc

Circuit A



Curve Tracer (C.T.) or Pulse (P)

Circuit B

(NOTE: Should not be used at any power level which will significantly affect the junction temperature of the DUT.)

3.3.3.3 Test Conditions to be Specified

(1) Case Temperature: T_C (if $T_C \neq 25°C$)

(2) Gate Source Voltage: V_{GS}

(3) Drain Source Voltage: V_{DS}

(4) Technique: dc (circuit A); C.T. or P (circuit B)

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3.3.3.4 Procedure

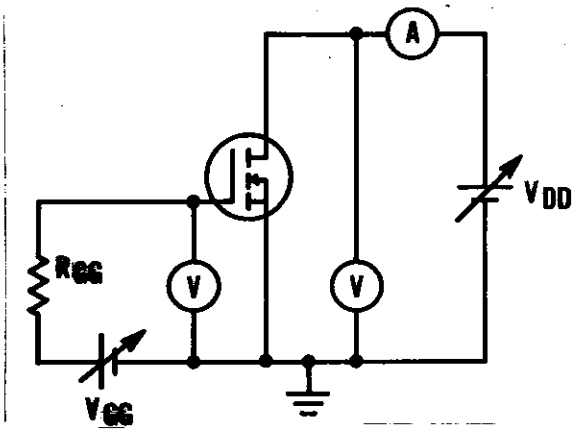
The supply, V_{GG}, is increased from zero until the specified gate voltage is achieved. I_D is then measured.

3.3.4 Static Drain–Source On–State Resistance – $r_{DS(on)}$

3.3.4.1 Description

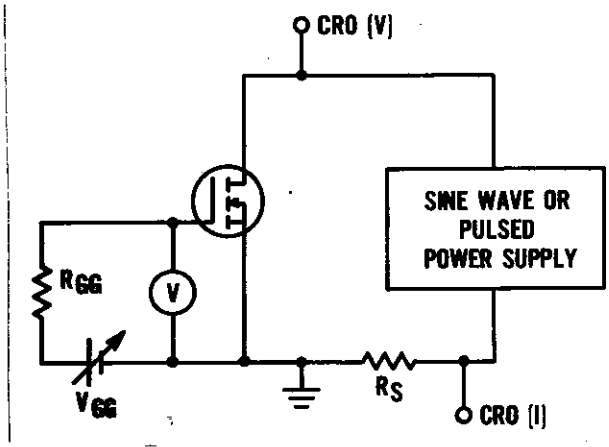
This parameter specifies the device's resistance between Drain and Source with the Gate at a specified forward-bias voltage. Gate voltage must be high enough so that changes in V_{DS} are roughly proportional to changes in I_D.

3.3.4.2 Test Circuit



Continuous dc

Circuit A



Curve Tracer (C.T.) or Pulse (P)

Circuit B

3.3.4.3 Test Conditions to be Specified

(1) Case Temperature: T_C (if $T_C \neq 25°C$)

(2) Gate Source Voltage: V_{GS}

(3) Drain Current: I_D

(4) Technique: dc (circuit A); C.T. or P (circuit B)

3.3.4.4 Procedure

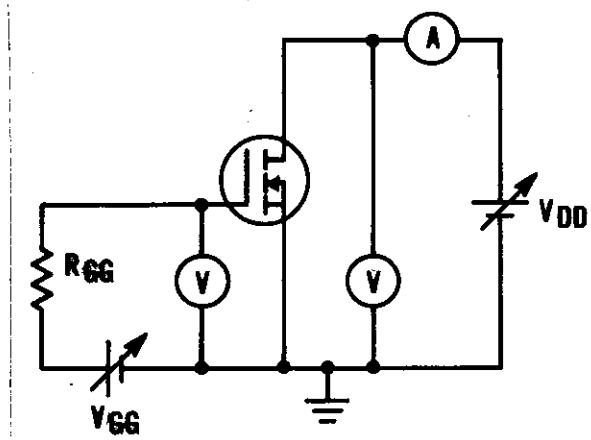
V_{DS} is measured and $r_{DS(on)}$ is calculated as V_{DS}/I_D.

3.3.5 Gate–Source Threshold Voltage – $V_{GS(th)}$

3.3.5.1 Description

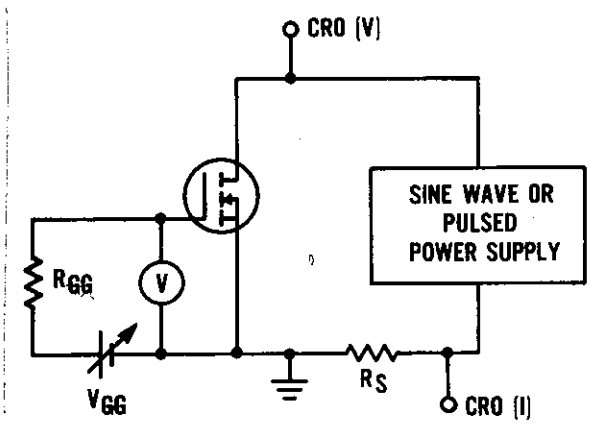
The threshold voltage specification defines a range of forward gate voltage for an enhancement type transistor at a drain current slightly above the cut-off level, I_{DSS}. The threshold voltage is considered a boundary between the off-state and on-state.

3.3.5.2 Test Circuit



Continuous dc

circuit A



Curve Tracer (C.T.) or Pulse (P)

circuit B

3.3.5.3 Test Conditions to be Specified

(1) Case Temperature: T_C (if $T_C \neq 25°C$)

(2) Drain Source Voltage: V_{DS}

(3) Drain Current: I_D

(4) Technique: dc (circuit A); C.T. or P (circuit B)

3.3.5.4 Procedure

V_{GG} is increased until I_D reaches the specified value at the specified V_{DS}.

3.3.6 Capacitance – C_{iss}, C_{oss}, C_{rss}

3.3.6.1 Description

Capacitances are the primary device characteristics determining switching speeds and frequency response. The ac test voltage must be small, on the order of 10-20 mV. Supply bypass capacitors must be much larger than device capacitance and supply isolation inductors must have very high impedance compared to device capacitance reactance.

3.3.6.2 Test Conditions to be Specified

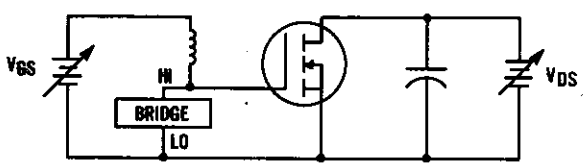
(1) Frequency: f

(2) Drain-Source Voltage: V_{DS}

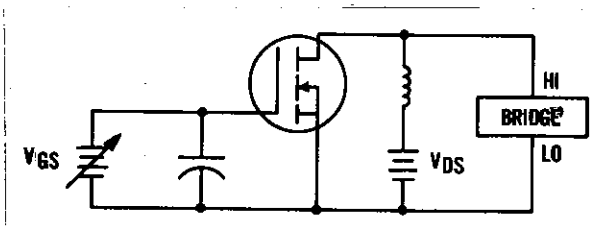
(3) Gate-Source Voltage: V_{GS} ($V_{GS} \leq V_{GS(th)}$)

(4) Case Temperature: T_C (if $T_C \neq 25°C$)

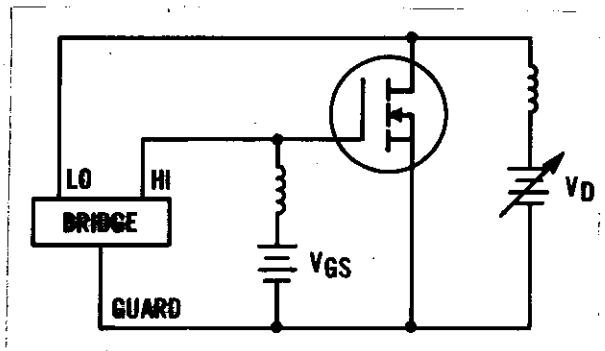
3.3.6.3 Test Circuit for Input Capacitance, C_{iss}



3.3.6.4 Test Circuit for Common-Source Output Capacitance, C_{oss}



3.3.6.5 Test Circuit for Reverse Transfer Capacitance, C_{rss}



3.3.6.6 Procedure

The specified bias is applied and the capacitance is measured.

3.3.7 Switching Time Measurements

3.3.7.1 Description

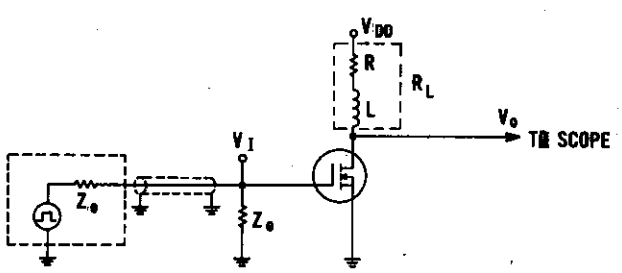
The circuit shown is suggested for measurement of switching times.

The input pulse duration and duty cycle should be chosen such that doubling or halving their values do not affect the measurement. The rise and fall time of the input pulse with the transistor removed from the circuit should be less than 25% of the respective output pulse being measured. If a pulse generator that generates fast enough rise and fall times is not available, the switching times of the device under test can be calculated knowing the input waveform rise and fall times and output waveform rise and fall times using the following:

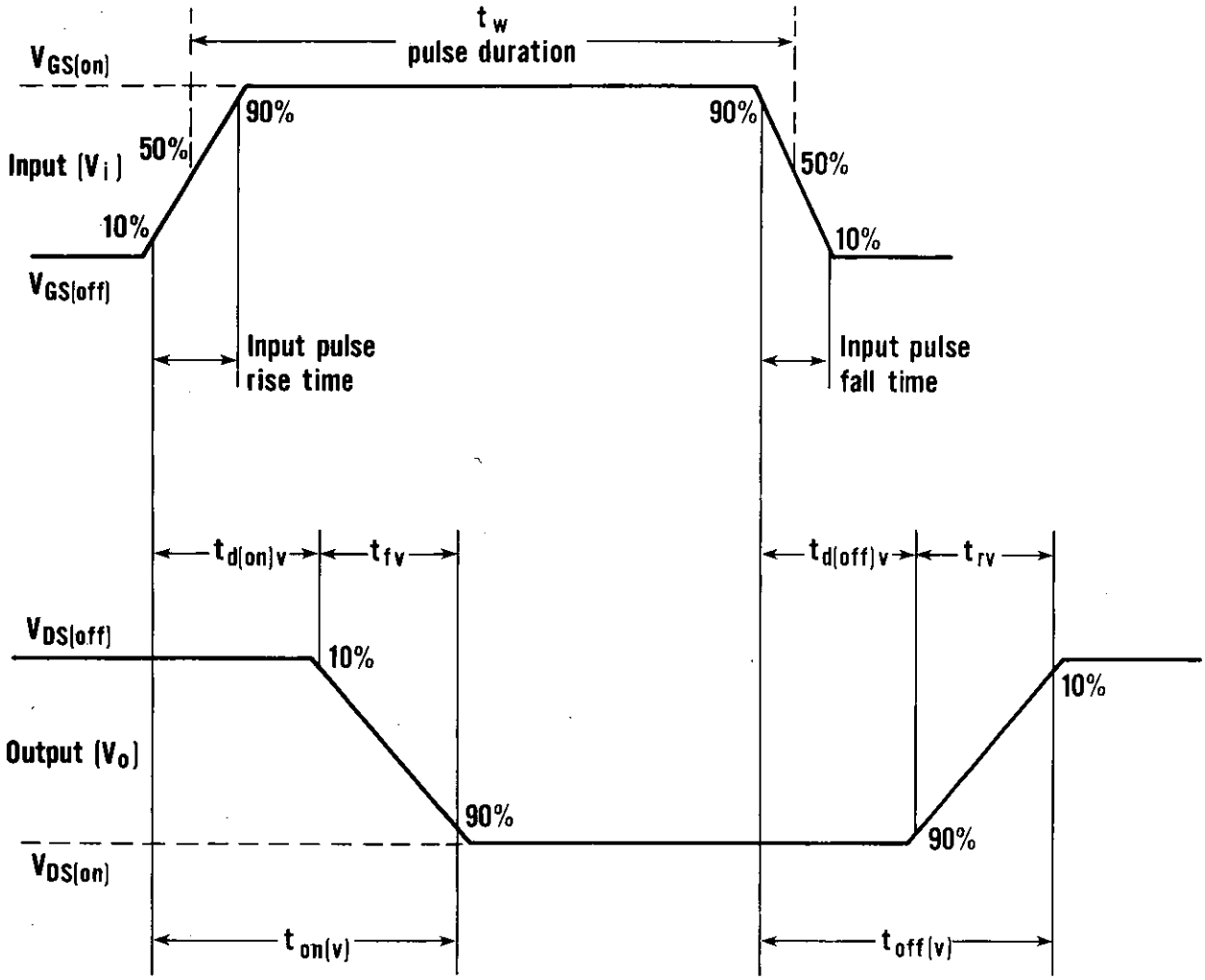
$$t_r = \sqrt{t_{r2}^2 - t_{r1}^2},$$

where t_r is the actual rise (or fall) time of device, t_{r1} is the input rise (or fall) time, and t_{r2} is the output rise (or fall) time.

3.3.7.2 Test Circuit



3.3.7.3 Waveforms



3.3.7.4 Test Conditions to be Specified

(1) Case temperature: T_C (if $T_C \neq 25°C$)

(2) Amplitude and rise time of V_i

(3) On-state drain current: I_D

(4) Off-state drain voltage: V_{DD}

(5) Generator and terminating impedance: Z_o

(6) Load circuit if not essentially resistive

3.3.7.5 Procedure

Apply the supply voltage and pulse input. Measurements may be taken immediately; however, an initial check of the circuit is necessary to ensure that the criteria of 3.3.7.1 are met.

CHAPTER 4

THERMAL CHARACTERISTICS

4.1 INTRODUCTION

The operating temperature of any semiconductor device is important in determining its reliability and operating life and has a strong influence on many of the electrical parameters. The thermal resistance of a device, $R_\theta(°C/W)$, is given by:

$$R_\theta = \frac{\Delta T_R}{P},$$

where $\Delta T_R(°C)$ is the rise in device chip temperature with respect to the temperature of a specified external reference point and $P(W)$ is the power dissipated by the device. Ideally, thermal resistance is a device specification that permits the user to establish the chip temperature for any power level. In order to specify and to verify the device thermal resistance, an accurate, reliable, and preferably nondestructive method for measuring the device chip temperature is required.

4.2 TEMPERATURE-SENSITIVE ELECTRICAL PARAMETERS

4.2.1 General

A temperature-sensitive electrical parameter (TSEP) is usually used as a thermometer to measure nondestructively the temperature of a semiconductor device chip. Many device electrical parameters are temperature sensitive, but the TSEP must satisfy several criteria if it is to be considered as a practical device thermometer. First, its variation with temperature must be large enough to be easily measured and to provide sufficient temperature resolution for the application at hand. Most practical TSEPs vary by several mV/°C (or equivalent). Second, the TSEP must be monotonic and preferably vary linearly with temperature. This allows easy calibration of the TSEP. Third, the TSEP should be stable and repeatable for at least as long as it takes to perform the measurement. Fourth, the TSEP should indicate a temperature that is representative of that of the device being measured. For device reliability and operating life considerations, this temperature would be the maximum device chip temperature (the device chip temperature is nearly always nonuniform). Finally, the TSEP should be a device parameter that is easily and quickly measured with a minimum of interference from other device parameters.

A cross-sectional view of a typical n-channel, vertical, double-diffused power MOSFET (VDMOS) showing the charge flow when the transistor is conducting and the critical device elements pertinent to the following discussion is given in figure 1. A practical power MOSFET will contain several thousand of the "cells" shown in the figure. Each of the TSEPs examined in this study will be discussed with reference to this figure.

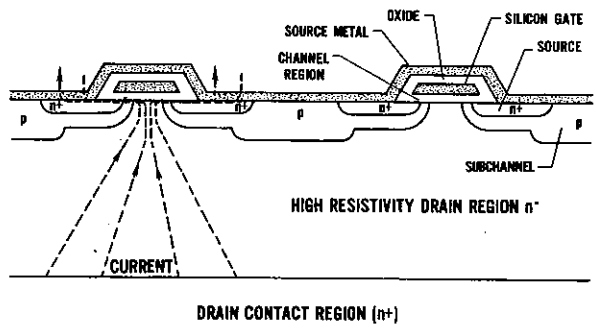


Figure 1. A Cross-Sectional View of a Typical Power MOSFET.

4.2.2 Source-Drain Diode Forward Voltage, V_{SD}

The source-drain diode is formed at the junction of the opposite conductivity type drain and subchannel regions (p-type subchannel and n-type drain for the n-channel device of fig. 1). The forward voltage of the diode can be directly sensed at the source-drain terminals because the source metallization overlaps and makes electrical contact to the subchannel region. The source-metal contact to the subchannel provides a low resistance path for "stray" minority carriers that may enter the subchannel region (such as due to leakage or avalanche current generated at the drain-subchannel junction) and thus inhibits their injection into the source. Injection of minority carriers into the source could turn on the parasitic bipolar transistor comprised of the source-subchannel-drain, causing the gate to "lose control" of the MOSFET. The metal contacting both subchannel and source thus enhances the safe operating limits of the MOSFET.

A substantial body of knowledge exists concerning the temperature sensitivity of a forward-biased diode [1]. For constant current:

$$\left.\frac{\partial V_{SD}}{\partial T}\right|_{I_{SD}} = -\frac{\frac{E_{go}}{q} - V_{SD}}{T},$$

where V_{SD}(V) is the forward voltage of the source-drain diode, T(K) is the diode temperature, E_{go}(eV) is the 0 K band gap energy, and q(C), the electron charge. It is found that typically $(\partial V_{SD}/\partial T)|_{ISD} \sim -2mV/K$. For the power MOSFET of figure 1, the source-drain diode forward voltage senses the temperature in the immediate vicinity of the diode.

4.2.3 Drain-Source On-Resistance, $r_{DS(on)}$

The drain-source on-resistance of a power MOSFET is comprised primarily of the channel resistance plus the drain resistance and is given by [2]:

$$r_{DS(on)} = r_{Ch} + r_D = \frac{1}{\beta(V_G - V_{GS(th)})} + k\rho_D,$$

where $r_{Ch}(\Omega)$ is the channel resistance and $r_D(\Omega)$ is the drain resistance, and V_G(V) is the gate-source voltage, $V_{GS(th)}$(V) is the threshold voltage, ρ_D(cm) is the drain region material resistivity, k (cm^{-1}) is a geometrical factor depending upon the relative dimensions of the device structure, and β is given by:

$$\beta = (W/L) \cdot C_o \cdot \mu_e,$$

where W(cm) is the channel width, L(cm) is the channel length, $C_o(f \cdot cm^{-2})$ is the gate oxide capacitance per unit area, and $\mu_e(cm^2 \cdot V^{-1} \cdot S^{-1})$ is the electron mobility in the channel inversion layer.

Both r_{Ch} and r_D are temperature sensitive. The channel resistance varies with temperature because both $V_{GS(th)}$ and μ_e are temperature sensitive.

The drain resistance varies with temperature because ρ_D is temperature sensitive. When the device is turned on with a large gate voltage $(V_G \gg V_{GS(th)})$, the channel resistance contributes very little to $r_{DS(on)}$. For this condition, both r_{DS} and $(\partial r_{DS(on)}/\partial T)|_{ID}$ are dominated by the drain resistance, r_D.

Over the temperature range of interest, the drain resistivity temperature variation is dominated by the temperature dependence of the bulk mobility which is dominated by lattice scattering. Computed values of the temperature coefficient of resistance $(1/\rho) \cdot (d\rho/dT)$ vary from about +0.007/K for 1 $\Omega \cdot cm$ n-type material to about +0.008/K for 100 $\Omega \cdot cm$ n-type material at room temperature [3]. A less than 1-percent change in drain region resistance (and thus $r_{DS(on)}$) occurs for a 1 K change in temperature. For a "typical" device with $r_{DS(on)} = 1\Omega$, the variation of $r_{DS(on)}$ with temperature is about $+7m\Omega/K$. The drain-source on-resistance primarily senses the temperature in the active drain region of the device.

4.2.4 Gate-Source Voltage, V_{GS}

The gate-source voltage controls the on/off state of the MOSFET. The threshold voltage, $V_{GS(th)}$, is approximately equal to the value of V_{SG} required to begin to turn on the MOSFET. When V_{GS} is used as a thermometer, the device is barely "turned on" and $V_{GS} \approx V_{GS(th)}$.

The drain current, I_D, is related to V_{GS} by:

$$I_D = \frac{\beta}{2}\left(V_{GS} - V_{GS(th)}\right)^2. \qquad (1)$$

Equation (1) is valid when the MOSFET is operating in the current saturation mode (constant current region), i.e., when the drain-source voltage, $V_{DS} \geq V_{GS}$. When V_{GS} is used as a thermometer, $V_{DS} \gg V_{GS}$.

From equation (1):

$$\left.\frac{\partial V_{GS}}{\partial T}\right|_{I_D} = \left(\frac{2I_D}{\beta^3}\right)^{1/2} \cdot \frac{d\beta}{dT} + \frac{dV_{GS(th)}}{dT}. \qquad (2)$$

For small values of I_D ($\sim$ 10 mA), $V_{GS} \sim V_{GS(th)}$ and the magnitude of the first term on the right of equation (2) is small compared to the second term $(dV_{GS(th)}/dT)$. The temperature variation of $V_{GS(th)}$ results from the temperature variation of the Fermi level in the channel region. Thus, the source-gate voltage senses the temperature of the channel region of the device. For practical devices, $dV_{GS(th)}/dT \sim -2$ to -6 mV/K.

4.3 APPARATUS, CIRCUITS, AND PROCEDURES

4.3.1 General

The apparatus for making a measurement of the device temperature for each of the techniques consists of a temperature-controlled heat sink for the device, a temperature control system, and the respective electronic switching and measurement circuitry.

4.3.2 Measurement Procedure

The measurement procedure is essentially the same for each of the TSEPs. Only steady-state measure-

ments will be discussed, but most of what follows also applies to transient measurements. The general procedure used is to repetitively power the device under test (DUT) with "normal" (heating) operating conditions and to then rapidly switch to a "measurement" (cooling) condition. The duty ratio (heating power time/measurement time) is typically 100:1. The case temperature of the device is held constant by the temperature-controlled heat sink and is continuously monitored.

During the measurement time, the TSEP is monitored. An oscilloscope may be used to enable the entire TSEP waveform to be measured as a function of time. The ability to monitor the TSEP during the entire measurement time permits one to determine the rate at which the device is cooling. This is important for determining the actual temperature at the instant the device is switched from the heating to the measurement condition as well as for determining when extraneous, nonthermal effects are interfering with the measurement. These concepts will be discussed in more detail in a later section.

The required calibration of the TSEP is accomplished by monitoring the TSEP as the heat-sink temperature (and thus the DUT temperature) is varied with only measurement conditions applied and no heating power applied to the DUT (0-percent duty cycle). Examples of a calibration curve for each of the TSEPs are shown in figure 2. To determine the device temperature for the actual measurement, the value of the TSEP obtained during the measurement is matched with the calibration curve. It is assumed that the same device temperatures give the same value for the TSEP during measurement and calibration.

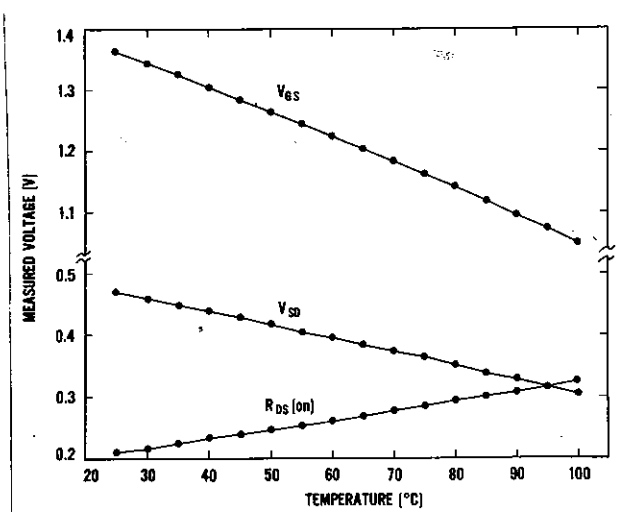


Figure 2. Examples of Calibration Curves for Each of the TSEPs.

4.3.3 Temperature-Controlled Heat Sink

In order for the measured temperature to be a meaningful parameter, some well-defined reference point associated with the device must be maintained at a constant temperature during measurement. The reference point usually chosen is on the bottom outside of the transistor case directly below the semiconductor chip. This is typically the hottest point on the case. The temperature may be monitored by either a glass bead thermistor or a thermocouple using the washer technique [4]. The DUT is firmly clasped to a temperature-controlled heat sink to maintain a constant reference point temperature. A typical heat sink is made of a copper block which contains water channels for the flow of chilled water as well as several "heating" resistors. The heat-sink temperature control is achieved by electronically controlling the power supplied to the heating resistors. The flow rate of chilled water is manually controlled. The electronic temperature controller uses the glass bead thermistor or thermocouple to sense the temperature for control purposes. Care must be taken to assure that the heat sink surface is flat and "burr free". The DUT attaching screws are screwed down with the same torque, and a thermal grease is used between the device and heat sink for all measurements.

4.3.4 Measurement Circuits

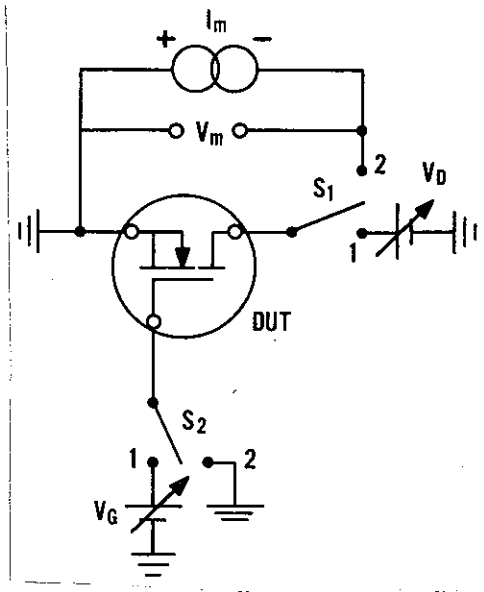
Simplified schematics of the measurement circuits used for each of the TSEPs are shown in figure 3.

A brief description of the operation of each circuit follows.

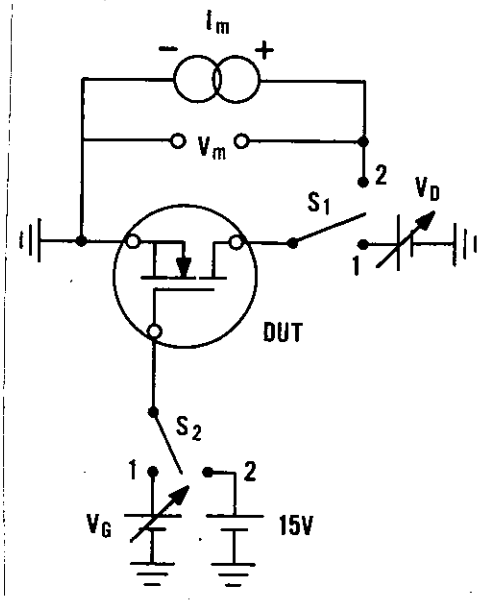
4.3.4.1 Source-Drain Forward Voltage Measurement Circuit

The circuit used to control the device and to measure the temperature using the forward voltage of the source-drain diode as a TSEP is shown in figure 3a. The circuit consists of the DUT, two power supplies, a current source, and two electronic switches. During the heating phase of the measurement, switches S_1 and S_2 are in position 1. The values of V_G and V_D are adjusted to achieve the desired values of I_D and V_{DS} for the "heating" conditions.

To measure the temperature, switches S_1 and S_2 are each switched to position 2. Thus, the gate is grounded and current source I_m supplies a forward measure-

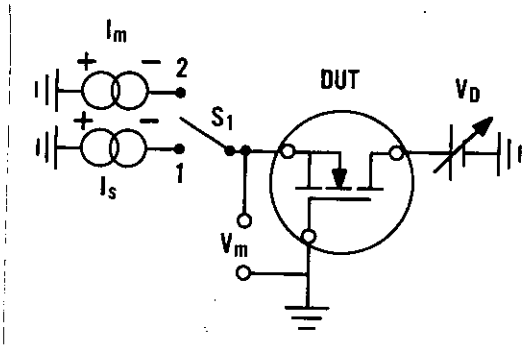


(a) Source-Drain Voltage



(b) Drain-Source On-Resistance

ment current to the source-drain diode. The polarity of the current source is such that the voltages applied to the MOSFET source and drain are opposite to those employed during normal MOSFET operation; i.e., for the measurement for an n-channel device, the drain is biased negative with respect to the source. The magnitude of I_m is typically 1 to 10 mA. The drain-to-source voltage required to maintain the constant I_m is equal to the forward source-drain diode voltage.



(c) Gate-Source Voltage

Figure 3. Schematics of Measurement Circuits for Each TSEP.

4.3.4.2 Drain-Source On-Resistance Measurement Circuit

The circuit used to measure the temperature using the on-resistance as the TSEP is shown in figure 3b. The circuit consists of the DUT, three power supplies, a constant current source, and two electronic switches. During the heating phase of the measurement, switches S_1 and S_2 are in position 1, and V_D and V_G are adjusted to achieve the desired I_D and V_{DS}.

To measure the temperature, both S_1 and S_2 are switched to position 2. This supplies 15 V to the gate terminal with respect to the source and also maintains a constant drain current, I_m. The magnitude of I_m is kept constant for a particular measurement for a device type but is different for various device types. The value of I_m is adjusted so that $V_{DS} \sim 0.5$ V. This helps to assure that the measured variation in V_{DS} with temperature is greater than about 1 mV/K. The voltage $V_{DS} = V_m$ is measured and is related to $r_{DS(on)}$ by:

$$r_{DS(on)} = V_m / I_m.$$

Because the magnitude of I_m can be rather high, kelvin contacts should be used in measuring $V_m(V_{DS})$.

4.3.4.3 Gate-Source Voltage Measurement Circuit

The circuit for controlling the device and measuring its temperature using the gate-source voltage as a thermometer is shown in figure 3c. The circuit consists of the DUT, two current sources, one power supply, and one electronic switch. During the heating phase, switch S_1 is in position 1. Thus, the drain current is equal to I_S, and the drain-source voltage

is equal to V_D. To measure the temperature, S_1 is switched to position 2, changing the drain current to I_m. For this measurement, $I_m \ll I_S$, and $I_m \sim 1$ to 10 mA. The source-gate voltage is monitored during the measurement phase (V_m) and is the TSEP.

4.4 SOME EXAMPLES OF MEASURED RESULTS

4.4.1 General

Temperature measurements using the three TSEPs as thermometers as well as with an infrared microradiometer (IRM) have been compared [5]. Only n-channel devices were included, but similar results would be expected on p-channel devices with the appropriate measurement circuit polarity reversals.

4.4.2 Calibration

Typical calibration curves are shown in figure 2. Each of the TSEPs is sufficiently linear with temperature and demonstrates a large enough change with temperatures to be considered as a practical TSEP. The amount of time required to generate a calibration curve depends upon the number of calibration points desired and the time required to externally heat the device (no internal device power dissipation) to the desired temperatures. Because each curve is relatively straight, only a few calibration points are required. For production measurements, where a large number of "identical" devices are measured, the variability of the calibration curve from device to device is of interest. Ideally, all devices of a given type would have identical (or at least sufficiently similar) calibration curves so that each device would not have to be calibrated. If the slope of the calibration curve does not vary from device to device, then a single calibration point is sufficient, even if the parameter itself is variable. The most stable parameter is V_{SD}. Only a 2- or 3-percent variation in V_{SD} is usually observed between identical devices, with an even smaller variation observed in dV_{SD}/dT. Most devices exhibit a 2- or 3-percent variability in both V_{GS} and $r_{DS(on)}$, but some devices will exhibit a 10- to 20-percent difference from the norm. The variations in dV_{GS}/dT and $dr_{DS(on)}/dT$ are comparable to but less than the variations in the parameters themselves. These results suggest that a "constant" variability with temperature for each parameter may be assumed for most devices of a given type, but care should be taken to detect "outliers" and perhaps a separate calibration performed for them if V_{GS} or $r_{DS(on)}$ are used as the TSEP [5].

4.4.3 Measured Temperature Comparisons

The results of temperature measurements on several devices for a number of operating conditions using the three TSEPs as well as an Infrared Microradiometer has shown that temperatures measured using V_{GS} as the TSEP are usually about 95 to 100 percent of the temperature determined using the IRM, whereas temperatures measured with V_{SD} or $r_{DS(on)}$ as the TSEP are usually about 80 to 90 percent of the IRM result [5].

4.5 GENERAL CONSIDERATIONS AND DISCUSSION

4.5.1 General

There are a number of "universal" difficulties encountered in measuring the temperature of a semiconductor device, whether it is a bipolar device or a MOSFET, a discrete power device, or an integrated circuit. Some of these will be discussed in this section, and it will be noted how they impact the temperature measurements for power MOSFETs.

4.5.2 Nonthermal Switching Transients

The term "nonthermal switching transient" refers to extraneous components of the measured TSEP waveform that are introduced as a result of switching from the heating to the measurement condition. That is, the measured TSEP has an extraneous, electrical component not present during calibration (no switching occurs during calibration). The TSEP must usually be measured with a resolution of at least 1 mV. Thus, even though one might consider the device to be fully "switched" for a typical circuit application, this is not the case for temperature measurement applications. Nonthermal switching transients are difficult to immediately discern, because the device is naturally cooling during the measurement phase (heating power has been removed) and the TSEP shows a natural thermal transient due to the temperature decay.

There are techniques for determining the presence of and correcting for nonthermal switching transients. It has been demonstrated that for the first 250 μs after switching, the device cools as if the flow of heat were strictly one-dimensional [4]. This means that $|\Delta T| \alpha t^{1/2}$ where ΔT is the temperature change from the instant switching occurred (t = 0) until time, t. If the measured temperature is plotted versus $\sqrt{t}$, a straight line relationship occurs if the nonthermal

switching transients have subsided [6]. The linear region of the temperature versus square root of time can be used to extrapolate the results to t = 0 to estimate the temperature at the instant of switching.

The nonthermal switching transients have several physical causes. A portion of the nonthermal switching transient is related to stored charge and the time required to charge and discharge device capacitances (both voltage dependent and voltage independent), to charge transit times, and to measurement circuit switching times. A significant and sometimes dominant portion of the nonthermal switching transients can result from the presence of the skin effect in magnetic leads [7]. It is well known that high-frequency alternating currents tend to be forced to the surface of a conductor. The "effective" conductor resistance due to this skin effect increases as the square root of the magnetic permeability of the conductor. Hermetic transistor packages typically have leads that are made of a material similar to kovar (~15 percent cobalt, 31 percent nickel, 54 percent iron) and are highly magnetic. When trying to rapidly switch from heating to measurement conditions, the increased lead resistance due to the high frequency components of the switching waveform can contribute significant nonthermal switching transient components to the TSEP waveform.

A technique has been developed for correcting for this effect [7] using a "dummy" package to replace the DUT. The "dummy" consists of a package with the leads used in the measurement internally shorted to one another such that a measurement of the TSEP voltage only measures the voltage across the leads.

4.5.3 Case Temperature Measurement Probe Location

The temperature at a specific location on the case of the transistor is maintained constant during the measurement of the device temperature. Because the temperature of the case is not uniform, it is important to be able to always measure the temperature at the same location on the case. The position usually chosen is directly beneath the semiconductor chip on the outside surface of the case. Even though the device is placed on a temperature-controlled heat sink (the bottom surface is in contact with the heat sink with a thermal grease applied to the bottom surface), a significant temperature gradient can exist along the bottom surface while the device is dissipating power. The magnitude of the gradient depends upon the case material. For 60 W of power dissipation, a copper case may have a temperature difference from an extreme edge of the bottom to a point on the bottom directly beneath the chip (a distance of about 2 cm) of about 2°C; an aluminum package, a difference of about 3°C; and a kovar or steel package, a temperature difference of about 6°C. Because many packages are made of kovar or of a similar material, it is very important to measure the temperature each time at the same location on the case.

4.6 REFERENCES

(1) P. E. Gray, D. DeWitt, A. R. Boothroyd, and J. F. Gibbons, "Physical Electronics and Circuit Models of Transistors", SEEC Series, Volume 2 (John Wiley and Sons, New York, 1964), pp 47-50.

(2) S. C. Sun and J. D. Plummer, "Modeling of the On-Resistance of LDMOS, VDMOS and VMOS Power Transistor", IEEE Trans. Electron Devices, ED-27, pp 356-367; 1980.

(3) P. Norton and J. Brandt, "Temperature Coefficient of Resistance for p- and n-Type Silicon", Solid State Electronics, 21, pp 969-974; 1978.

(4) S. Rubin and F. F. Oettinger, "*Semiconductor Measurement Technology:* Thermal Resistance Measurements on Power Transistors", NBS Special Publication 400-14; 1979.

(5) D. L. Blackburn and D. W. Berning, "Power MOSFET Temperature Measurements", PESC '82 Record, IEEE Power Electronics Specialists Conference, Boston, Massachusetts, pp 400-407, June 1982.

(6) D. L. Blackburn and F. F. Oettinger, "Transient Thermal Response Measurements of Power Transistors", PESC '74 Record, IEEE Power Electronics Specialists Conference, Murray Hill, New Jersey, pp 140-148; June 1974.

(7) D. W. Berning and D. L. Blackburn, "The Effect of Magnetic Package Leads on the Measurement of Thermal Resistance of Semiconductor Devices", IEEE Trans. Electron Devices, ED-28, pp 609-611; May 1981.

CHAPTER 5

A USER'S GUIDE

5.1 INTRODUCTION

The purpose of this chapter is to offer to the user some general information about Power FET characteristics, different failure modes, temperature effects on transistor parameters, and troubleshooting. This information is not meant to be complete or exhaustive, and it does not include detailed application information.

5.2 PRODUCT SAFETY

It is the responsibility of the power transistor user to anticipate the possibility of transistor failure.

A transistor should not render the equipment unsafe for any reason in terms of electrical shock, explosion, etc.

5.3 TRANSISTOR CHARACTERISTICS

5.3.1 Introduction

The most important feature of the field-effect transistor is that the current is carried by majority carriers. This means that the switching time is limited only by the rate at which the gate can be charged and discharged. Two types of Vertical FETs are in use, the MOSFET and the Junction FET. The JFET is formed in the bulk of the semiconductor. As shown in figure 1, junctions are formed along the conductive channel. When they are reverse biased, the depletion layer can be expanded until the channel current is cut off. Figure 2 depicts a junction field-effect transistor which uses multiple gate junctions and multiple channels in a vertical structure.

The MOSFET and the characteristics it has in common with the JFET will be discussed in the next section.

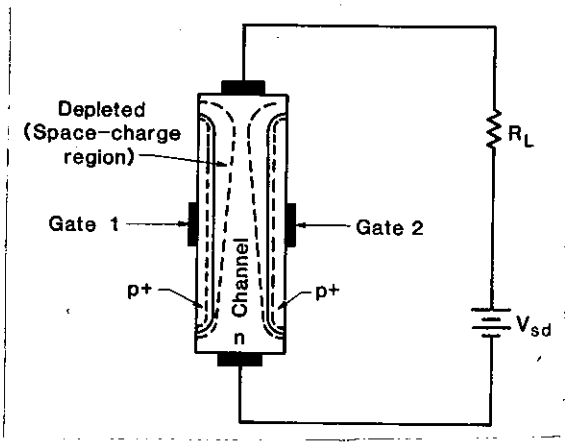


Figure 1. Junction-Gate Field Effect Transistor.

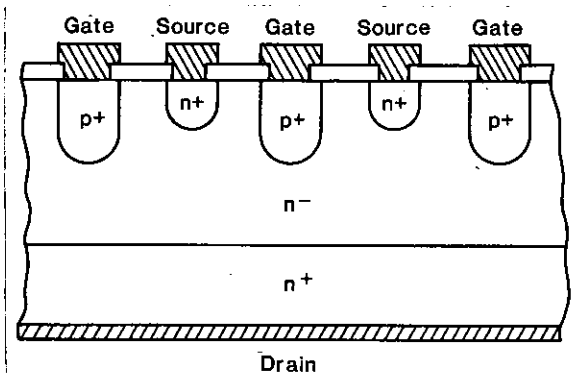


Figure 2. Junction-Gate Vertical Field Effect Transistor.

5.3.2 Fundamental Characteristics

To understand fundamental characteristics of vertical MOS transistors, an examination of construction is necessary. Figure 3 shows cross sections of two types of n-channel FETS. All MOSFETs are built in parallel with a bipolar transistor. In part (a), the V-groove cut into the structure forms the gate. To keep the bipolar inactive, its base is shorted to its emitter. This also stabilizes the threshold voltage of the FET, since the "subchannel" region is not electrically floating.

Referring to figure 3a, to cause current to flow in an n-channel device, the gate is made positive with respect to the source, causing electrons to be attracted into the p-region surface under the gate. Above a certain voltage (the threshold voltage), the p-type silicon surface inverts, forming an n-type channel and thereby creating a low resistance path from source to drain. The channel is made short to provide high gain; therefore, it cannot support significant voltage at the drain without punch-through occurring. The n-type epitaxial layer is used to provide sufficient depletion region for the drain-source voltage.

The vertical MOSFET of figure 3b operates in a similar manner to that of figure 3a. In this structure, there is a buried gate formed of polycrystalline silicon or metal silicide instead of a metal surface gate. Improved packing density and reliability are among the advantages of the silicon gate structure. A disadvantage is the increased resistance introduced in series with the gate capacitance which results in slower switching speed.

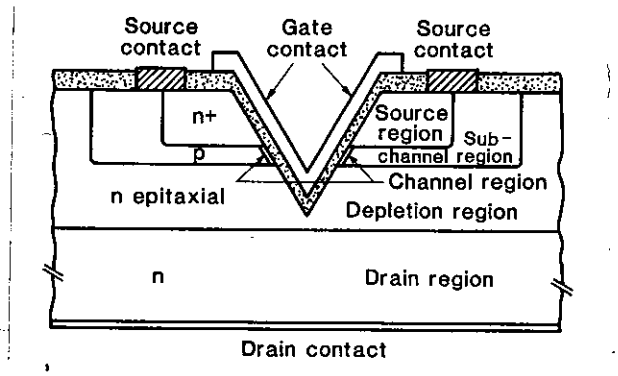


Figure 3a. Vertical V-Groove MOS Field Effect Transistor.

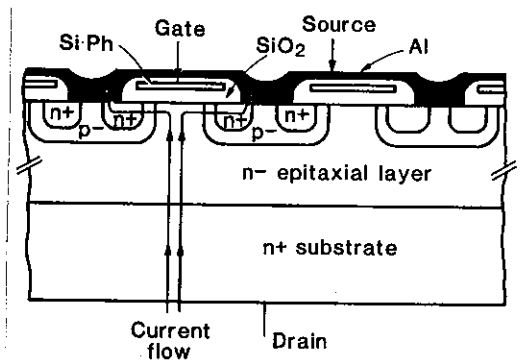


Figure 3b. Vertical D-MOS Field Effect Transistor with Silicon Gate.

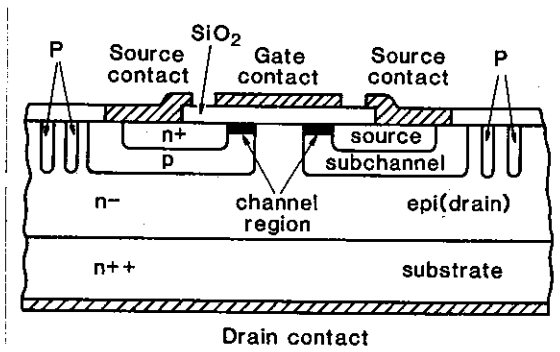


Figure 4. Cross Section of a Vertical D-MOSFET with Guard Rings.

The double-diffused or DMOS transistor in figure 4 is produced by sequentially diffusing the gate and source through the same opening in the oxide. Processing starts with a p-type junction formed on an n-type substrate. To the right and left of the main junction, other junctions of the same depth but narrower width may be formed. These additional junctions serve as field-limiting rings and allow the depletion width to spread along the chip surface, thus distributing the voltage.

The conventional MOSFET is constructed horizontally, as shown in figure 5. The n^+ source and drain regions are simultaneously diffused into the p-type substrate. The channel region occurs on the top surface of the substrate. Even though this structure is admirably suited to complex digital integrated circuit fabrication, a number of undesirable attributes occur which make it unattractive for linear applications and rule it out for power applications. The length of the channel is determined by the tolerances of the masks used to define the source and drain patterns. Since these are not controllable to a fine degree, the channels must be relatively long, resulting in fairly low gain per unit area, a high on-state resistance ($r_{DS(on)}$), and a square-law transfer curve. In contrast, the vertical FET channels are determined by diffusion so that short channels are achieved (shorter by a factor of three or so), which increases the gain, reduces $r_{DS(on)}$, and provides a linear transfer curve.

An obvious attribute not mentioned in the discussion above is the requirement for long reliable life. Chip temperature is usually the chief determinant of semiconductor longevity; in particular, if any part of the chip's temperature exceeds the critical intrinsic temperature, second breakdown may occur. Second breakdown is a condition which renders a device incapable of supporting voltage and usually results in destruction of the transistor. Although second break-

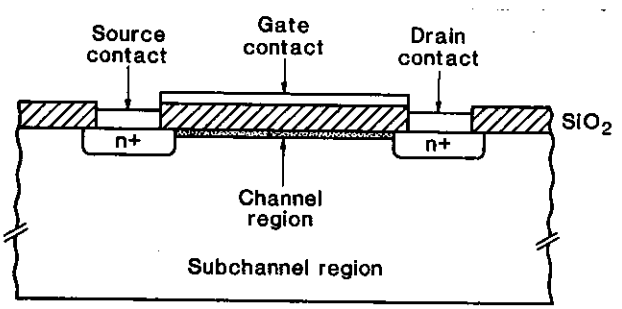


Figure 5. Cross Section of a Conventional MOSFET.

down has been observed in FET devices, the power levels required are extremely high compared to the power rating of the transistor.

5.3.3 Small-Signal High Frequency Characteristics

Power FET characteristics at high frequencies and small-signal conditions are similar to conventional FETs, and the commonly used FET circuit model of figure 6 is satisfactory to account for active-region behavior for frequencies up to about 100 MHz. The ratio between the capacitances is different from conventional FETs, and the capacitance and transconductance values are much larger for a power device than for a small-signal device. The origin of the capacitances is easily understood by examining figure 7, which shows one half of a V-groove channel. The gate-to-source capacitance C_{gs} is caused by the overlap of the gate conductor over the source region. The drain-to-source capacitance C_{ds} is effectively the C_{ob} of the parasitic bipolar device and is proportionally large compared to that of a standard horizontal FET. The capacitance, C_{ds}, is not a particular problem in most applications, however, as it is in parallel with the load. The important feedback capacitance, that from gate to drain (C_{gd}), is remarkably small because of the short channel and high resistivity of the epitaxial region.

Direct measurement of FET capacitances is possible with a three-terminal (guarded) arrangement. However, to avoid doing this for all tests, C_{iss}, C_{rss}, and C_{oss} have been adopted as standards and are related to the model capacitances of figure 6 as shown in table 1. The capacitances are affected by voltage as shown in figure 8. The solid lines represent the capacitances of a junction FET. The capacitances of a MOSFET and a junction FET are similar except for C_{oss} and C_{iss}. In a MOSFET, C_{iss} is nearly constant as indicated by the dotted line. The gate capacitor is merely a metal or polysilicon plate separated from a silicon plate by a thin layer of oxide. Increasing the gate voltage in a junction FET widens the depletion layer at the gate and decreases C_{iss} in accordance with normal junction behavior.

5.3.4 Switching Models

In large-signal or switching applications, the small-signal model applies when allowance is made for the variation of capacitances with voltage. In the off- and on-state, the simple models of figure 9 apply. The off-state current, I_{DSS}, is caused by the parasitic transistor and is equal to its I_{CES}. Consequently,

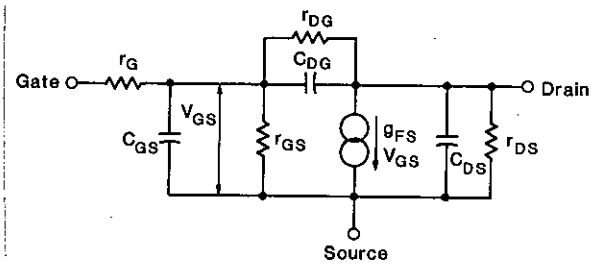


Figure 6. Mid-Frequency Small Signal FET Equivalent Circuit.

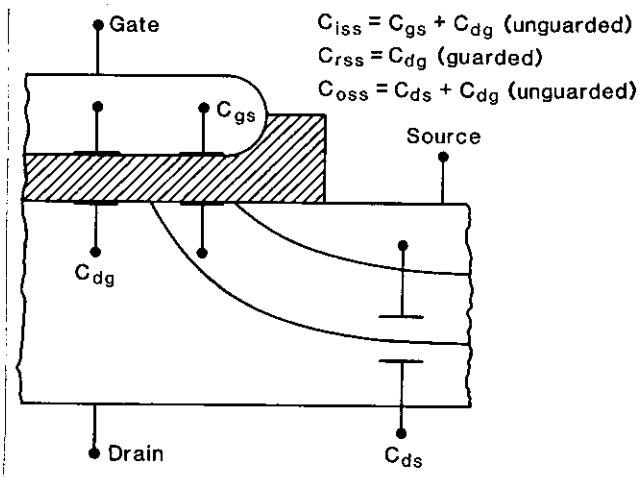


Figure 7. Vertical MOSFET Capacitances.

$$C_{iss} = C_{gs} + C_{dg}\,(\text{unguarded})$$
$$C_{rss} = C_{dg}\,(\text{guarded})$$
$$C_{oss} = C_{ds} + C_{dg}\,(\text{unguarded})$$

Table 1. Relation of Industry Standard Measurements to FET Model Capacitances.

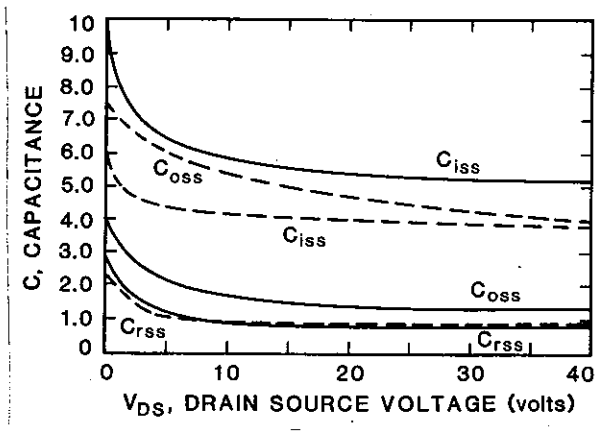


Figure 8. Normalized Capacitance vs. Drain-to-Source Voltage.

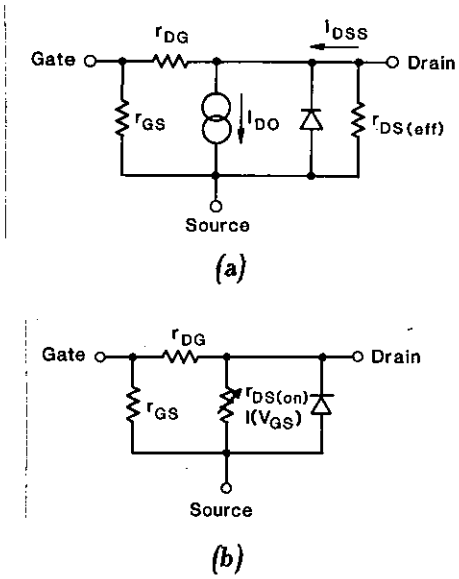


Figure 9. DC Switching Models for Analysis of Off and On Conditions.

the behavior of I_{DSS} with temperature and voltage is similar to a bipolar transistor.

The on-state resistance, $r_{DS(on)}$, is a function of the gate drive and, to a lesser extent, drain current and temperature. Figure 10 shows a more detailed look at the on-state region. Some care must be exercised in switching circuit designs to make sure that sufficient gate voltage is used to keep the device in the ohmic region under worst-case drain current and temperature conditions. As temperature increases, the on-state voltage increases and the gain decreases.

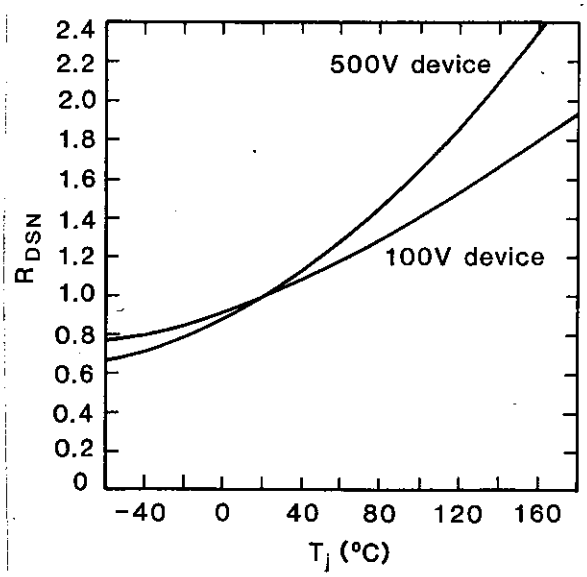


Figure 10. Normalized $r_{DS(on)}$ vs. Temperature.

5.4 TRANSISTOR FAILURE MODES

5.4.1 Introduction

There are two general classes of failure: catastrophic failure and degradation. Catastrophic failure occurs when at least one of the electrical parameters undergoes a sudden change which renders the transistor inoperable. Degradation occurs when at least one of the electrical parameters has changed so that it no longer meets the characteristic specified in the registration or those limits agreed upon by the buyer and seller.

Depending on the particular structure, the parasitic bipolar transistor that supports the MOSFET can cause a certain amount of anomalous behavior. Any discussion of these effects in the following material applies only to the MOSFET. The Junction Vertical FET contains no parasitic bipolar transistor. Likewise, the material on electrostatic discharge damage is of less importance to the Junction FET since it contains no MOS gate capacitance.

5.4.2 Thermally Induced Catastrophic Failures

The probability of catastrophic failure increases considerably whenever the transistor is operated beyond the maximum ratings. This failure is usually manifested either by a short circuit or an open circuit. While electrical or thermal overstress is usually the cause for failure, it is important to recognize that physical overstress to the package can also lead to device failure. Proper mounting procedures are discussed in section 5.7.

A drain-source open circuit is usually due to the vaporization of a part of a lead wire electrically connecting the terminal lead to the semiconductor die and is caused by excessive current through the wire.

A short circuit may be due to any one of a number of effects, for example, fusing of the source and drain and surface arcing across *p-n* junctions or adjacent evaporated leads.

Fusing of the drain and source can occur when the temperature in the bulk becomes high enough to melt the semiconductor material. It can also occur if the temperature at the surface is high enough to have the source metal contact alloy through to the drain. In planar devices with aluminum metallization, the location and lateral extent of the short circuit site usually may be determined by viewing the metallization. The high surface temperature can result in the formation

of a silicon-aluminum eutectic over the site. This is seen as an apparent discoloration of the metallization when viewed under a microscope.

The high temperature required to produce fusing or other thermal damage is usually caused by exceeding the design limits of ambient temperature and/or power dissipation of the transistor and heat sink combination. The area over which the fusing occurs depends on the distribution of power dissipation within the transistor at the time the intrinsic temperature of the semiconductor material is reached. The failure can be the result of using an inadequate heat sink or poor circuit design which allows a cumulative increase in power dissipation with increasing junction temperature. This thermal runaway condition can occur because of the positive temperature coefficient of the on-state resistance in the ohmic region.

5.4.3 Electrostatic Discharge Failures

Increasing numbers of electronic component failures are being attributed to electrostatic discharges. It is now an accepted fact that some MOS devices can be destroyed by less than 100 V of static charge. An individual can easily generate 10,000 V on his body by taking a few steps across a dielectric floor. If at this point he were to pick up a static-sensitive device, the stored charge could break down the oxide of its gate region.

While electrostatic discharge is seldom a problem with large VMOS transistors because of their large gate capacitance (about 1,000 pF), a few simple precautions are recommended to ensure trouble-free usage. The first place to start is the work area. Bench tops and working surfaces should ideally be grounded, or be covered with a conductive material. Metal tote pans should be used in moving devices from one area to another. The important point is to avoid any material that will allow the accumulation of charge such as plastic. The worker should be trained to ground himself on the work area before handling devices. It is recommended that anti-static clothing be used. In the handling of devices, cotton gloves are recommended. Since the accumulation of static charge is a function of humidity, very low humidity should be avoided; a minimum of 35 percent is usually acceptable. Ideally, work areas should not be carpeted; but if they are, the carpet should have metal threads or be treated with an anti-static solution. Retreatment is usually required weekly and in extreme cases, daily.

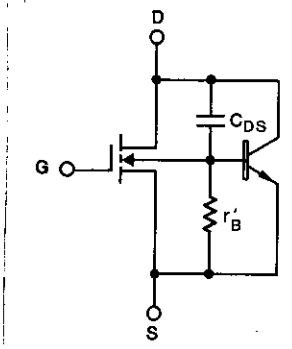


Figure 11. Detailed Vertical MOSFET Model.

5.4.4 Electrical Anomalies

Tests indicate that FET power capability is determined essentially by thermal resistance. However, the structure of the vertical MOS transistors is such that under certain kinds of operation anomalous behavior may occur. This is caused by the parasitic bipolar transistor that supports the VMOS device. The relationship between the two is shown in figure 11. Circuitry must not allow conditions to occur which would permit the bipolar transistor to become active. The source and base are shorted, but problems could occur if a voltage spike on the drain exceeded the breakdown voltage of the bipolar support transistor. This would cause the bipolar to breakdown into a $V_{(BR)CER(sus)}$ mode. $V_{(BR)CER(sus)}$ is roughly half of $V_{(BR)DSS}$. ($V_{(BR)DSS}$ is the same as $V_{(BR)CBO}$ of the bipolar). If the supply voltage exceeds $V_{(BR)CER(sus)}$, the device might remain latched on in the $V_{(BR)CER(sus)}$ mode and could possibly be destroyed due to overdissipation or second breakdown in the bipolar transistor. It is also possible for a very fast rising voltage at the drain to feed enough current into the bipolar base through the collector base capacitance to cause loss of blocking ability. For the transient, the breakdown curve would more nearly resemble a $V_{(BR)CEO}$ characteristic than a $V_{(BR)CES}$ characteristic. Thus, a latch-up similar to that caused by overvoltage could occur if the supply voltage exceeds the $V_{(BR)CEO(sus)}$ of the bipolar.

Similar problems can occur with VMOS transistors utilizing a zener protected gate. The gate zener diode is normally constructed monolithically, as shown in figure 12, because the p and n^+ regions can be diffused at the same time as the p-channel and n^+ source are diffused. However, the zener diode is really a transistor whose emitter-base junction breakdown is being used. The circuit model of figure 13 applies. Be-

cause of transistor action, the gate-zener-diode breakdown characteristic may exhibit a negative resistance as shown in figure 14. The curve is the $V_{(BR)GEX}$ characteristic of the zener transistor which is slightly affected by the electrical condition at the drain terminal. Under some situations, failure to account for the negative resistance could cause problems. For example, for the device in figure 13, it is inadvisable to have the gate connected through a low impedance source to a voltage above 12 V, since a latch up could occur, resulting in excessive gate dissipation.

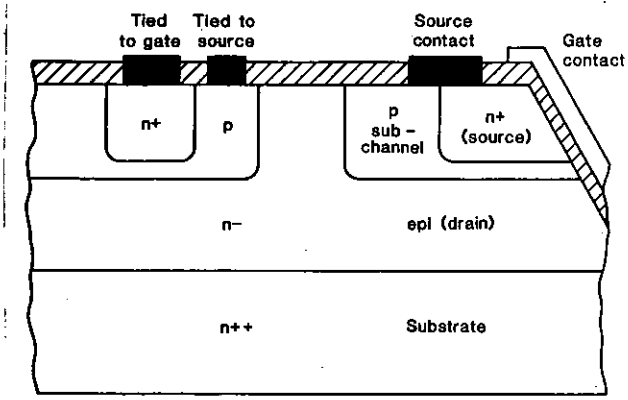


Figure 12. Gate Zener Construction.

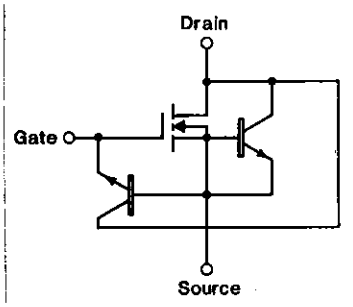


Figure 13. Gate Protected MOSFET Model.

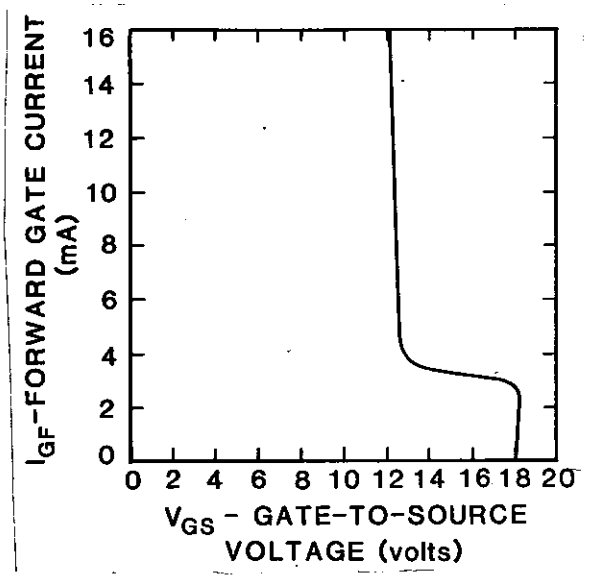


Figure 14. Gate Zener Breakdown Characteristics.

If a reverse voltage signal is applied to the gate, the resulting "zener" current appears at the drain terminal because the *n-p-n* zener transistor has an alpha close to unity. Where reverse voltages must be handled, a resistance in series with the gate to limit the current to a low value is often a satisfactory solution at low frequencies. In high frequency or fast switching circuits, it may be necessary to use a Schottky diode clamp from gate to source to prevent reverse current flow.

Since reverse zener current causes the bipolar to become active, the maximum drain voltage is limited by the $V_{(BR)CEO}$ breakdown of the zener bipolar, which is about half the $V_{(BR)DSS}$ breakdown. Therefore, when zener protected devices are operated from drain supplies which exceed about 40 percent of the V_{DSS} rating, it is particularly important that no reverse gate-zener current is allowed to flow.

5.4.5 Degradation

Some change in the transistor's electrical parameters with time is considered normal. Such changes can take place during storage or operation. Degradation is defined to occur when such changes are so large that one or more of these parameters no longer meets the limits of the registration or those limits agreed upon by the buyer and seller. Those parameters which are most often found to vary are the junction leakage currents and the threshold voltage. The user may reduce such changes and hence also the possibility of degradation by operating within the conditions specified by the maximum ratings, especially for temperature and maximum operating conditions.

5.5 EFFECT OF TEMPERATURE VARIATIONS ON ELECTRICAL PARAMETERS

The electrical parameters of semiconductor devices are temperature sensitive. This fact should be taken into consideration whenever a parameter of a semiconductor is being measured or is being relied upon. In an effort to eliminate a device temperature variation during measurements, the industry has adopted short-pulse, low duty cycle tests (usually 300 μs at 1 or 2 percent duty cycle). This is particularly neces-

sary for measurements of power semiconductors because of the high power levels involved during some of the measurements.

Some general rules of how different parameters behave with temperature are as follows:

(1) I_{DSS}: This parameter is a cut-off test for enhancement-type MOS devices and may be divided into two components: the bulk and the surface leakage. In general, the bulk current will double for every 8°C rise for silicon devices. The surface component is rather unpredictable, but in general, it will increase with temperature. Since the surface leakage is often the predominant component, it is almost impossible to extrapolate the cut-off current of a typical power transistor at high temperature.

(2) g_{fs}: The temperature coefficient of the small-signal transconductance depends on the device structure and varies slightly with current and temperature. The temperature coefficient of transconductance is negative.

(3) $V_{(BR)DSS}$: The temperature coefficient is positive for silicon transistors.

(4) $V_{GS(th)}$: Threshold voltage is the most temperature-sensitive characteristic of an MOS transistor. It varies with drain current level but is on the order of −6 mV/°C.

(5) C_{iss}, C_{rss}, C_{oss}, C_{gs}, C_{DS}, C_{gd}: The capacitances increase slightly with temperature. The changes in dielectric constant and resistivity result in a temperature coefficient of approximately 35 ppm°/C.

(6) $t_{d(on)}$, t_r, $t_{d(off)}$, t_f: The switching times are primarily determined by the rate at which the device capacitance can be charged. Therefore, switching time has a small positive temperature coefficient, the same as the capacitances.

(7) $r_{DS(on)}$: Channel resistance has a positive temperature coefficient. Typically, it ranges from 0.6 to 0.8%/°C depending on the design of that particular transistor; see figure 10.

5.6 SIMPLE MEASUREMENTS IN TROUBLESHOOTING TRANSISTOR CIRCUITS

5.6.1 Introduction

For most people, troubleshooting is as much a part of the equipment design process as breadboarding and worst-case analyses. This section will discuss briefly some of the basic tools and techniques of troubleshooting. For the purposes of this discussion, it will be assumed the circuit is one that has been designed by or is of a type with which the engineer is familiar.

5.6.2 Tools

(1) The Circuit Diagram – Though one feels one knows the circuit totally, a circuit diagram is a necessity.

(2) Oscilloscope – A good oscilloscope with at least 100 MHz bandwidth is essential in troubleshooting Power FET circuits. It permits detection of faulty waveforms and spurious oscillations in isolating problems to a single section of a circuit.

(3) Low-Current, High-Voltage Power Supply – In the absence of a curve tracer, a small 0 to 500 V power supply with only 10-mA capability can be used to verify that the I_{DSS} of MOSFETs is within the normal range.

(4) A 20,000-Ω/V Volt-Ohmmeter (VOM) – A VOM is an extremely useful instrument. Make a record of the voltage, polarity, and short- circuit current for each ohms range position of the VOM.

(5) An Electronic Voltmeter – For use in high-impedance circuits, an electronic VOM is a necessity. It should have a position for 0.5-V full-scale deflection. Also, it is most desirable that it have a floating common which will permit the unit to measure potential drops where both points are above ground.

(6) A Heat Gun and Cold Spray – These are indispensible aids when servicing for temperature-sensitive defects.

5.6.3 Basic Transistor Tests

(1) Functional Test – The circuit in figure 15 is an open or short and gain tester for MOS transis-

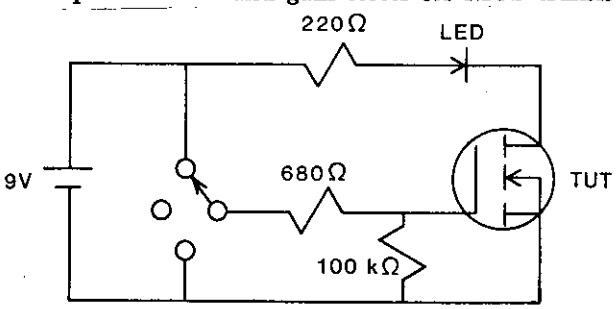


Figure 15. Functional Test Circuit.

tors. The battery polarity is shown for an *n*-channel transistor. If the transistor is operative, the lamp will light when the gate resistor is connected to the plus side of the battery; likewise, the lamp will go out if the resistor is in the open position or connected to the source side of the battery.

(2) Ohmmeter Test – A rough but useful check of the condition of the junctions may also be made with an ohmmeter. First, however, the polarity of the ohmmeter leads should be determined.

The forward resistance from drain to source (parasitic diode) may be measured first. A normal unit will have less than 50 Ω resistance. Reversing the leads, the reverse resistance of the junction may then be measured. The reverse leakage resistance of a normal unit will be 500,000 Ω or greater.

The ohmmeter may also be used to check for the presence of a gate protection zener. The forward resistance of the gate zener will be 500 Ω or less.

5.6.4 Circuit Tests

(1) Visual check – Check all electrolytics and diodes to ascertain that they have been inserted with the correct polarity and are operable. An ohmmeter may be used. Look for discolored resistors indicating overheating, solder balls, wire scraps, etc. Check the fuses.

(2) Functional test – Apply power to the circuit. Observe which of its functions is missing or defective. This will narrow the investigation to one area of the circuit.

(3) Waveform checks – Refer to the existing circuit diagram or draw one of the circuit under consideration. Determine what the waveforms should be at the key points in the circuit. This will permit further isolation of the fault.

(4) Voltage measurements – Use the circuit diagram to determine the voltages that would be normal at important points throughout the circuit. An estimate of the transistors I_D versus V_{GS} characteristic is necessary to calculate circuit voltages with reasonable accuracy for an amplifier. However, an assumed V_{GS} voltage of 3 V may be used for rough calculation.

(5) Resistance measurements – The waveform checks and voltage measurements should have narrowed the possible fault to a few components. Now the power can be turned off and the suspect parts tested with an ohmmeter.

(6) Click test – Should the voltage measurements not show up the difficulty, another technique is "click testing". This may be done by momentarily forcing one device or another into the cut-off condition and observing the voltage change at the collectors of the devices in question. This is especially useful when checking out logic chains and flip-flops.

Enhancement-mode devices may be forced into cut-off by shorting the gate to the source; depletion-mode devices require using a 1,000- to 10,000-Ω resistor (depending on the circuit) and a battery of appropriate value and polarity.

When dealing with power devices, it is well to remember that transistors seldom fail without an external cause. If a defective device is found, the trouble search should continue until one is satisfied that all the defective elements have been located.

(7) Temperature tests – When the circuit problem is one of intermittents, drifting, or wandering, a voltage test or a test for oscillations while the circuit is temperature stressed is worthwhile. A heat gun and a bottle of compressed fluorocarbon will quickly heat or cool the troublesome circuit while voltages are monitored or signal trace procedures are followed. This hot-cold technique is good for quickly testing the circuit under worst-case conditions as well as for locating cold-solder joints, poor socket contacts, defective electrolytics, and intermittent resistors.

(8) Oscillations – If the voltages measured appear to be wildly askew and bear little relation to circuit values, parasitic oscillations should be suspected. Of course, the test leads of the VOM could be responsible.

One way of checking for oscillations is to vary the supply voltage and monitor the devices for sudden voltage changes. It may be possible to reduce the supply voltage to the troublesome circuit until it just starts to oscillate and then proceed with the troubleshooting routine. As the

cures are effected, the voltage can be increased until it is back to the design value. If the oscillations worsen as the voltage is reduced, it is often a symptom of deficient power supply filtering.

When dealing with parasitic problems, one must remember that transistors do not oscillate by themselves. They need power and reactive components to make them oscillate. Search for defective or deficient filtering or bypassing. Do not rely on the "500 μF ought to be enough" attitude. Calculate the reactance of the capacitor at the frequencies of concern and relate the values to the circuit loads and currents. Many electrolytics do not work very well at high frequencies and may require additional bypassing with ceramic or mica capacitors.

Usually oscillations are prevented by observing one or more of the following guidelines:

(a) Keep lead and trace lengths short.

(b) Place ferrite beads on the gate lead close to the gate terminal or use a resistor of 100 to 1000 Ω in series with the gate.

(c) Avoid a layout which may couple output signal to the input.

(d) Surround the MOSFET with a ground plane and shield output from input.

(e) Use noninductive resistors.

5.7 THERMAL CONSIDERATIONS AND COOLING TECHNIQUES

5.7.1 Introduction

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, semiconductor industry field history indicates that the failure rate of most silicon semiconductors decreases approximately by one half for a decrease in junction temperature from 160°C to 135°C, a fact which emphasizes the importance of conservative thermal design.

Many failures of power semiconductors can be traced to faulty mounting procedures. With metal-packaged devices, faulty mounting generally causes unnecessarily high junction temperature resulting in reduced component lifetime, although mechanical damage has occurred on occasion from mounting securely to a warped surface or by overtorquing stud-mounted packages. With the widespread use of various plastic-packaged semiconductors, the dimension of mechanical damage becomes very significant.

The material in this section is aimed to bring into focus the major problems in selecting a heat sink and particularly in mounting the power semiconductor to the heat sink surface.

5.7.2 Thermal Resistance Concepts

Basically, there are three methods by which heat is transferred: (1) conduction (heat travels through a material), (2) convection (heat is transferred by physical motion of a fluid), and (3) radiation (heat is transferred by electromagnetic wave progagation). Semiconductors depend on conduction as a means of transferring heat from the junction to the external surface of the package and from the package to the heat exchanger, commonly called a heat sink. The package is cooled by convection and radiation. Both components are comparable in a still air ambient at sea level. Convection dominates when forced air or liquid cooling is used; radiation dominates in applications where semiconductors are used in a vacuum or at high altitudes.

The basic equation for heat transfer is generally written as

$$q = hA\Delta T, \tag{1}$$

where:

- q = rate of heat transfer or power dissipation (P_D),
- h = heat transfer coefficient or thermal transmittance per unit area,
- A = area involved in heat transfer, and
- ΔT = temperature difference between regions of heat transfer.

Electrical engineers find it easier to work in terms of thermal resistance defined as the ratio of temperature to power. From equation (1), thermal resistance R_θ is:

$$R_\theta = \frac{\Delta T}{q} = \frac{1}{hA}. \tag{2}$$

The coefficient h depends upon the heat transfer mechanism used and various factors involved in that par-

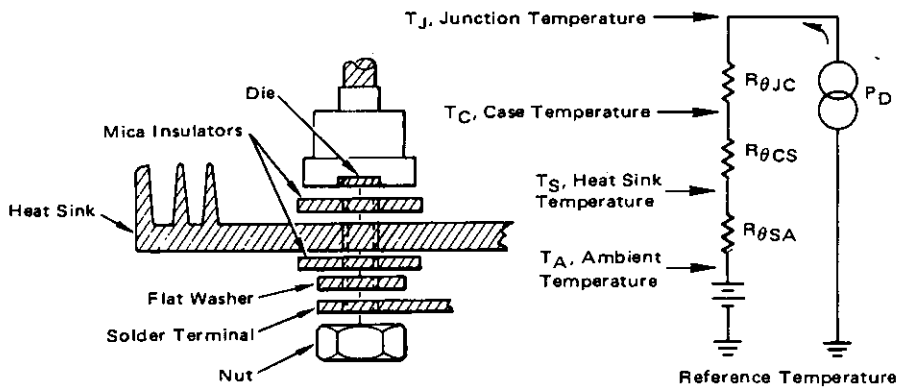


Figure 16. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor.

ticular mechanism. The coefficient h may be thought of as a thermal conductivity, regardless of the heat transfer mechanism.

An analogy between equation (2), and Ohm's Law is often made to form models of heat flow. Note that ΔT could be thought of as a voltage (V), thermal resistance corresponds to electrical resistance (R), and power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by figure 16.

The equivalent electrical circuit may be analyzed by Kirchoff's Law and the following equation results:

$$T_J = P_D (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A = P_D (R_{\theta JA}) + T_A, \quad (3)$$

where:

$R_{\theta JA}$ = total thermal resistance junction to ambient,
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat sink), and
$R_{\theta SA}$ = heat sink thermal resistance (heat sink to ambient).

The thermal characteristics and measurements of the semiconductor are described elsewhere and will not be further discussed here. The interface thermal resistance ($R_{\theta CS}$) resulting from imperfect mating surfaces and use of insulators may be appreciable in high power applications. Factors in minimizing $R_{\theta CS}$ are discussed following some guidance on heat sink selection and thermal design.

5.7.3 Application and Characteristics of Heat Sinks

Heat sinks are available in an endless assortment of sizes, shapes, colors and materials. The manufacturer should be contacted for exact design data. Heat sinks fall into several categories.

(1) Flat vertical finned types: normally aluminum extrusions with or without an anodized black finish, they are unexcelled for natural convection cooling and provide reasonable thermal resistance at moderate air-flow rates for forced convection.

(2) Cylindrical or radial vertical-finned types: normally cast aluminum with an anodized black finish, they are used when maximum cooling in minimum lateral displacement is required.

(3) Cylindrical horizontal-finned types: normally fabricated from sheet metal with a painted black matte finish, they are used in confined spaces for maximum cooling in minimum vertical displacement but are less efficient than types 1 and 2.

(4) Closely spaced fins in a box: strictly a forced-air cooler, they provide maximum cooling per unit area.

(5) Plates with integral ducts for liquid cooling.

Natural convection heat sinks should have the fins in a vertical position for maximum efficiency. A horizontal position could increase thermal resistance 30 percent. A painted or hard anodized surface improves radiation efficiency. It is also important not to block air flow currents above or below the heat sink.

When forced-air cooling is employed, an interlock is generally necessary to prevent catastrophic system failure in the event of a blower malfunction. The use of an air switch, comprised of a moving vane in the air flow mechanically coupled to a microswitch, can be used to interlock the electrical system.

Most efficient use of a given air flow will be achieved by locating components demanding minimum temperature rise (for example, semiconductors) closer to the inlet end of the cooling column and locating those elements for which maximum temperature rise is permitted (for example, power resistors) at the exhaust end.

Determination of the required air flow must also take into account the location of the air mover (fan or blower). If the air mover is located at the intake, its own heat loss must be added to the power which the system is required to dissipate. In this location, however, the ambient temperature which the blower experiences will be relatively low. At the exhaust, the air mover operates in a higher ambient temperature, but its own power loss does not raise the ambient temperature of the assembly and is, therefore, generally preferable.

5.7.4 Surface Conditions

Air pockets can be trapped in the depressions and voids between two mating surfaces. The majority of these can be avoided with proper care and handling of the two surfaces before mounting. Since devices are generally cooled by contact of heat dissipators or heat exchangers against the semiconductor mounting surfaces, the mounting should ideally distribute the pressure evenly across the mating surfaces.

In general, the heat dissipator mounting surface should have a flatness and surface finish comparable to that of the semiconductor package. In lower-power applications, the heat dissipator surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required.

"Surface Flatness" is determined by comparing the variance in height (h) of the test specimen to that of a reference standard as indicated in figure 17. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e., $\Delta h/TIR$, is satisfactory in most cases if it is less than 4 mils per inch, which is normal for extruded aluminum. "Surface Finish" is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 μin. is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance.

Care should be taken to ensure that all mating surfaces are free from foreign materials and oxides. If semiconductors and heat dissipators are stored, a cleaning operation before use is good practice. A satisfactory cleaning technique is to polish the mounting areas with Number 400-600 grit paper, followed by a solvent rinse. Number 000 steel wool can be used to polish contact areas, but care must be exercised to remove steel particles so that flash-over will not occur.

Many aluminum heat sinks are black anodized to improve heat radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Another treated aluminum finish is iridite, or chromate acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. For economy, paint is sometimes used on dissipators. Removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance; however, when it is necessary to electrically insulate the semiconductor package from the heat dissipator, a painted surface may be satisfactory.

Even though all the procedures listed are followed, minute air voids between mating surfaces will still exist. To reduce the thermal resistance introduced

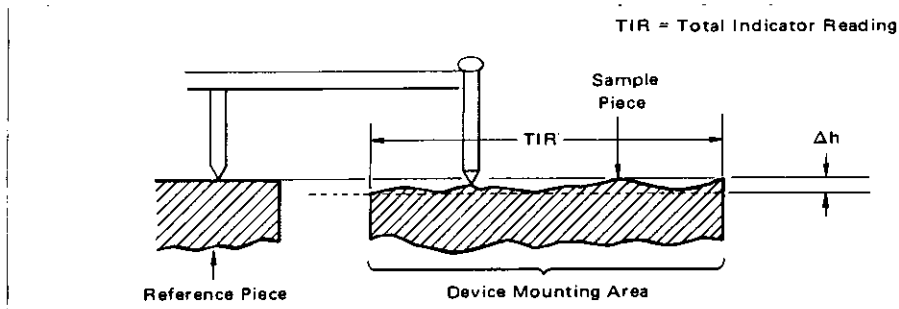


Figure 17. Surface Flatness.

at these mating surfaces, a thermal joint compound may be used. Such a compound also has the desirable property of keeping moisture away from the mating surfaces, and hence, inhibiting corrosion.

5.7.5 Thermal Compounds

To reduce thermal resistance, thermal joint compounds or greases are used to fill air voids between all mating surfaces. Values of thermal resistivity vary from 0.1°C-in./W for copper oxide film to 1200°C-in./W for air, whereas satisfactory joint compounds have a resistivity of approximately 60°C-in./W. Therefore, the voids, scratches, and imperfections which are filled with a joint compound will have a thermal resistance of about 1/20th of the original value, which makes a significant reduction in the overall interface thermal resistance.

Joint compounds are usually a formulation of fine metallic particles in a silicone oil which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Partial rotation of the package will help the compound spread evenly over the entire contact area. Experience will indicate whether the quantity is sufficient, as any excess will appear around the edges of the contact area. To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the assembly.

5.7.6 Insulation Considerations

Since most Power FETs have the drain electrically common to the case, the problem of isolating the case from ground is a common one. For lowest overall thermal resistance, it is best to isolate the entire heat dissipator-semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heat sink. Where heat sink isolation is not possible because of safety reasons or in instances where a chassis serves as a heat sink or where a heat sink is common to several devices, insulators are used to isolate the individual components from the heat sink.

When an insulator is used, thermal compounds assume greater importance than with a metal-to-metal contact, because two interfaces exist instead of one, and some materials, such as mica, have a markedly uneven surface. Reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when a thermal compound is used.

With some arrangements, the interface thermal resistance may exceed that of the semiconductor junction-to-case thermal resistance. When high power is handled, beryllium oxide is unquestionably the best choice, but care must be exercised in handling as even small particles are toxic. Polyimide material is fairly popular for low-power applications because it is low in cost, withstands high temperatures, and is easily handled, in contrast to mica which chips and flakes easily.

When using insulators, care must be taken to keep mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly so that having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal compound usually raises the breakdown voltage of the insulation system. Because of these factors, which are not amenable to analysis, high-potential testing should be done on prototypes and a large margin of safety employed.

5.7.7 Mounting Hole Preparation

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger packages having mounting holes removed from the semiconductor die location, such as a TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heat sink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heat sink indentation, or the device may only bridge the "crater" and leave a significant percentage of the heat dissipating surface out of contact with the heat sink.

The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heat sinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heat sinks. The holes are pierced using Class A progressive die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer and increase mounting stress. The edges should be broken to remove burrs, which cause poor contact between device and heat sink and may puncture isolation material.

5.7.8 Mounting Procedure

Unequal thermal expansion of the semiconductor mounting base and the heat dissipator, e.g., a copper stud and an aluminum heat dissipator, can cause the mounting to gradually loosen as the assembly is cycled through temperature extremes. A spring washer on the reverse side of the heat dissipator minimizes this effect by allowing the aluminum to expand against the washer compression rather than the copper.

Mounting errors with stud-mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heat sink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The best fastening method is to use a nut and washer; the details are shown in figure 18.

The torques specified for lubricated and nonlubricated threads are normally different. Most torque specifications are for dry threads and care must be exercised when applying thermal compounds to avoid contact with the threads. Precise adherence to the manufacturer's torque recommendation is necessary and should be verified using a torque wrench.

Few known mounting difficulties exist with the flange type of package. The rugged base and distance be-

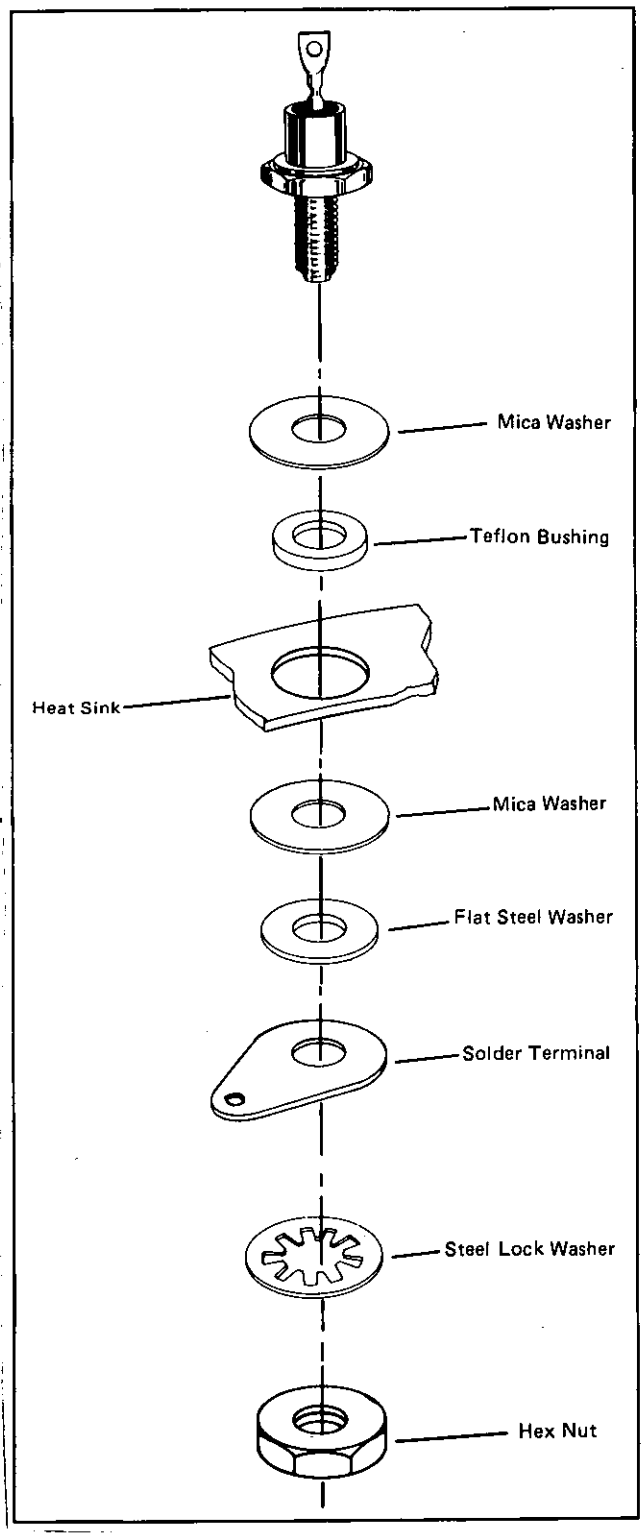


Figure 18. Mounting Details for Stud Mounted Semiconductors.

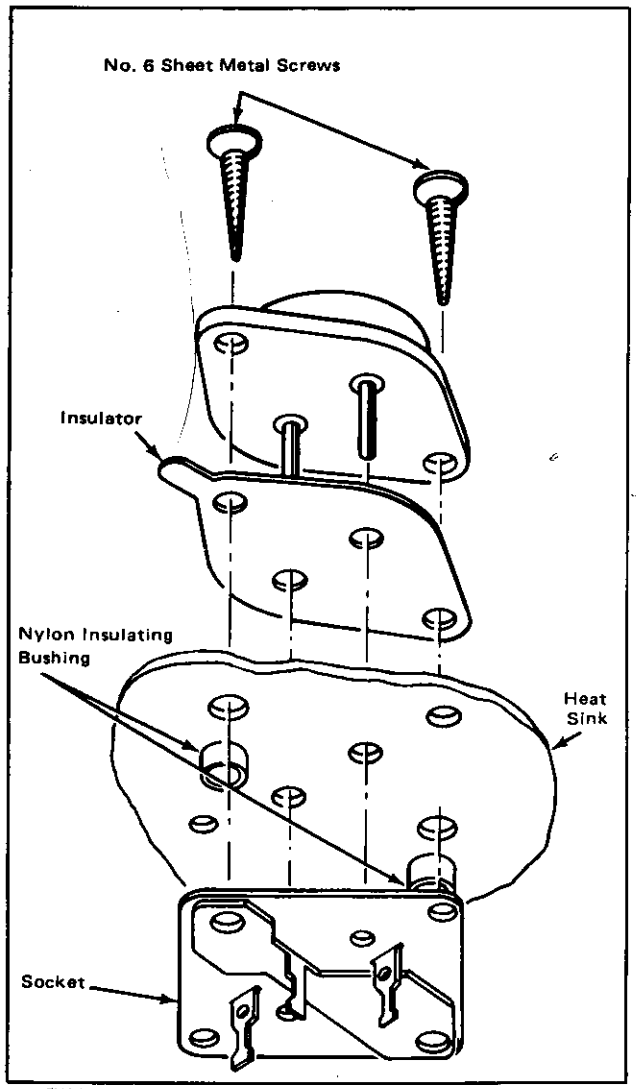


Figure 19. Mounting Details for Flange Mounted Semiconductors (TO-3 shown).

tween die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. A typical mounting installation is shown in figure 19. Machine screws, self-tapping screws, eyelets, or rivets may be used to secure the package.

The popular TO-220 package requires stricter attention to mounting details. Figure 20 shows suggested mounting arrangements and hardware. The rectangular washer shown in figure 20a is used to minimize

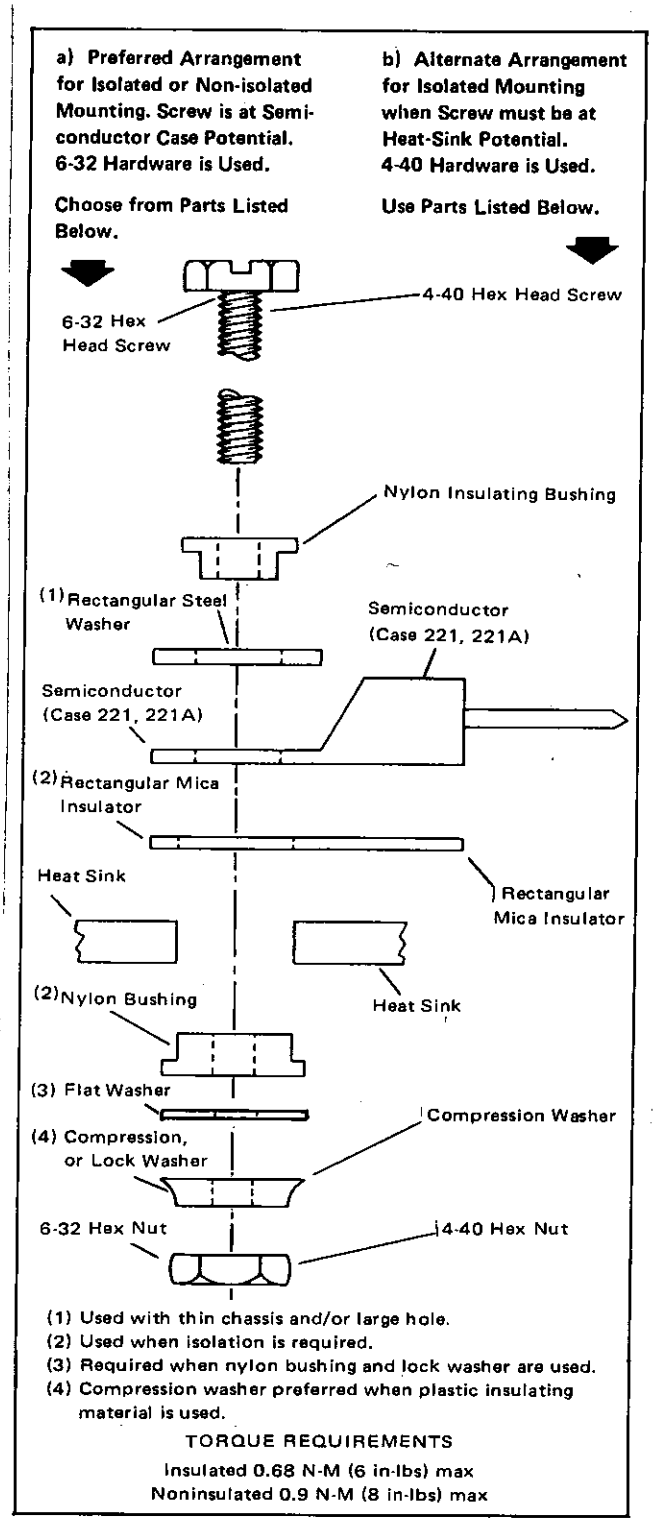
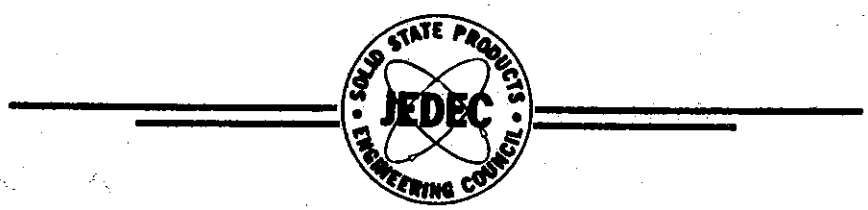


Figure 20. Mounting Arrangements for TO-220 Packages.

distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.14 in. (6-32 clearance). Larger holes are needed to accommodate insulating bushings when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.25 in. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6-32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Contact may damage the body and internal device connections.

In situations where the package is in direct contact with the heat sink, an eyelet may be used, provided sharp blows or impact shock is avoided.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