JEDEC STANDARD

The Measurement of Small-Signal VHF-UHF Transistor Short-Circuit Forward Current Transfer Ratio

JESD371

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FEBRUARY 1970 (Reaffirmed: April 1981, April 1999, March 2009)

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FEBRUARY 1970

EIA STANDARD

For

THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO

ELECTRONIC INDUSTRIES ASSOCIATION
STANDARD RS-371

Formulated by

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STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO

(From Standards Proposal No. 1028, formulated under the cognizance of JEDEC Committee JS-9 on Low Power Transistors.)

1. DEFINITIONS

1.1 Definition of the short-circuit forward current transfer ratio

Given a two-port network as shown in Fig. 1, where v_1 i_1, v_2 and i_2 represent the voltage and the current at ports one and two respectively, the short-circuit forward current transfer ratio may be defined as the element h_{21} of the matrix

$$H = \begin{vmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{vmatrix} \tag{1}$$

associated with the linear equations

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2, \tag{2}$$

and

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2. \tag{3}$$

According to the above equation, h_{21} may be expressed by the ratio

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{v_2 = 0} \tag{4}$$

which represents the forward current transfer ratio with port two short-circuited.

The short-circuited forward current transfer ratio of a transistor is also commonly represented by the following symbols:

h_{fe} for a bipolar transistor in common-emitter configuration
h_{fb} for a bipolar transistor in common-base configuration
h_{fc} for a bipolar transistor in common-collector configuration
h_{fd} for a field-effect transistor in common-drain configuration
h_{fg} for a field-effect transistor in common-gate configuration
h_{fs} for a field-effect transistor in common-source configuration

1.2 Definition of small-signal conditions

Transistors are essentially nonlinear devices which, for sufficiently small applied signals, behave as linear two ports.

Small-signal conditions may, therefore, be defined as the values of the voltage and current at ports one and two, below which the transistor may be considered a linear two-port.

For practical applications, the following definition will be used: Small-signal conditions are satisfied where reduction of 50% in the amplitude of i_1 will not result in a variation of the ratio defined by (4) of more than 1%*.

1.3 Definition of the transistor terminals

In standard single-ended axial-lead transistor packages, the transistor terminals for the purposes of this standard are the points on said leads at a distance of 1.5 mm (0.06") from the seating plane of the transistor package (see Fig. 2), which points define the reference plane of the transistor terminals.

In special packages not provided with leads (e.g. strip-line or coaxial packages), the transistor terminals must be specifically defined for each particular package.

2. TRANSISTOR MOUNTS FOR SINGLE ENDED AXIAL-LEAD TRANSISTORS

The transistor mount must satisfy the following requirements:

a – It shall have two well-shielded terminals, preferrably coaxial, to which ports one and two of the transistor-under-test shall be connected.

b – It shall have two ground connections to which the common terminal and a possible shield of the transistor package shall be connected.

*All asterisks in this document refer to the following footnote:

The numerical values quoted have been agreed upon by the JS-9 JEDEC committee as those representing a practical compromise between the usual requirements of circuit design applications of current gain parameters and the measurement technology at the time of writing this document.

c – The magnitude of the transfer susceptance between the two shielded terminals (when no device is inserted in the mount) shall be less than 1) 5%* of the magnitude of the reverse transfer susceptance of the transistor under test, or 2) less than that susceptance corresponding to a capacitance of 0.001 pF*, whichever is greater.

d – The shielded terminals shall be designed to eliminate the high-frequency effects of that part of each lead extending from the transistor terminal defined in 1.3 above to the physical extremity of said lead. This is normally achieved by the use of tubular inputs in which the transistor leads are inserted.

e – The location of the reference plane of shielded terminals shall be known within less than ± one thousandth of the wave length at the test frequency.*

f – Repeatable low-resistance electrical contact between the transistor leads and the terminals of the mount shall be made within 0.5 mm (0.02")* of the intended contact points.

g – No portion of the mount shall extend beyond the reference plane defined in paragraph (e) above.

h – No insulating materials shall be placed in the air-gap between the seating plane of the transistor package and the reference plane of the transistor mount (see Fig. 2).

i – When the transistor mount consists of constant-impedance transmission lines, the VSWR introduced by the transistor mount shall be less than $(1.01 + 0.03\ f_{GHz})$ with respect to the characteristic impedance of the system to which the transistor mount is connected. The expression f_{GHz} represents the test frequency in gigahertz.

j – When transmission lines are used to make the connection between the transistor and the measuring system, a d-c blocked damping resistor may be connected provided the connection is made within 0.5 mm (0.02")* of the reference plane of the shielded terminals if a short circuit is effectively reflected at this terminal.

3. THE MEASURING SYSTEM FOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO

3.1 General

The measuring system must provide a means for applying bias to the transistor under test. The bias system must be such as not to influence the accuracy of the measurements. The signal applied by the measuring system to the transistor must be sufficiently small to satisfy the "small-signal conditions" defined in 1.2. In addition, any spurious signals which might appear at the transistor terminals, and in particular, the local oscillator feedthrough when a superheterodyne receiver is used, must be kept at least 20 dB* below the specified small-signal conditions.

Ideally, the measurement of the short-circuit forward current transfer ratio would require a perfect short circuit at the output and the capability of sensing both input and output currents

simultaneously. As an alternative, an ideal current source of known magnitude and phase can replace the sensing of the input current.

3.2 Source Impedance and Load Admittance

If the measuring system has the capability of simultaneously sensing both input and output currents, there are no requirements on the source impedance Z_S but the load admittance Y_L must be subject to the restriction expressed by inequality (5) below. If the measuring system does not have the capability of sensing the input current and instead uses a current source of impedance Z_S, both Z_S and the load admittance Y_L must be subject to the restrictions expressed by inequalities (5) and (6) below. (For derivation, see Appendix.)

$$|Y_L| > 50\,|h_{22}| \quad * \tag{5}$$

$$|Z_S| > 50\,|h_{11}| \quad * \tag{6}$$

3.3 Correction Formulas

For more accurate results, the correction formulas given below and derived in the Appendix may be used.

When simultaneous input current sensing is not employed:

$$h_{21} = h'_{21}\left[1 + (h_{22}/Y_L + h_{11}/Z_S)\right], \tag{7}$$

where h_{21} represents the true value of the short-circuit forward current transfer ratio whereas h'_{21} represents the measured value.

When simultaneous input current sensing is employed:

$$h_{21} = h'_{21}\,(1 + h_{22}/Y_L). \tag{8}$$

3.4 Transmission Lines

Transmission lines may be used to make the connection between the transistor mount and the measuring system. These lines may include adjustable-length sections and may also be used for impedance transformations. However, the VSWR created by any residual reflections in the lines must not exceed $(1.025 + 0.005\ f_{GHz})$* where f_{GHZ} represents the test frequency expressed in gigahertz. Also, the errors in the measured parameters caused by losses in the lines must be less than 10%.* If these errors exceed 1%* appropriate corrections should be made.

APPENDIX

1. SIMULTANEOUS INPUT CURRENT SENSING NOT EMPLOYED

Let the source driving the transistor-under-test be characterized by the voltage v_s and by the impedance Z_S and let Y_L be the load admittance. The test circuit (see Figs. 1 and 3) may be described by the following equations:

$$v_s - h_{12}\, v_2 = i_1 (Z_S + h_{11}), \tag{9}$$

$$h_{21}\, i_1 = -(h_{22} + Y_L)\, v_2, \tag{10}$$

$$v_2 = -\frac{i_2}{Y_L}. \tag{11}$$

Eliminating i_1, gives:

$$h_{21} = \frac{(h_{22} + Y_L)(h_{11} + Z_S)}{-v_s/v_2 + h_{12}}. \tag{12}$$

Let a reference current gain equal to negative one be established by a short circuit applied between the shielded terminals of the test system. Then equation (12) reduces to:

$$1 = Y_L Z_S/(v_s/v_2^{+} - 1), \tag{13}$$

where v_2^{+} is the voltage developed across Y_L when the short is applied between the terminals.

Equations (12) and (13) may be combined to yield

$$h_{21} = \frac{Z_S Y_L}{\left[-(1 + Z_S Y_L)\, v_2^{+}/v_2\right] + h_{12}} \quad (1 + h_{22}/Y_L)(1 + h_{11}/S). \tag{14}$$

The product, $|Z_S Y_L|$, is easily made much greater than one whereas $|h_{12}|$ is always less than one. Therefore, (14) may be simplified giving

$$h_{21} = \frac{-v_2}{v_2^{+}} \left[1 + (H_{22}/Y_L + h_{11}/Z_S)\right], \tag{15}$$

where the second order term, $H_{11}h_{22}/|Z_S Y_L|$ has been neglected. Since. in this case

$$\left(\frac{-v_2}{v_2^+}\right) = \left(\frac{v_2 Y_L}{v_2^+ Y_L}\right) = \frac{i_2}{i_1} = h'_{21} , \tag{16}$$

then

$$h_{21} = h'_{21} \left[1 + (h_{22}/Y_L + h_{11}/Z_S)\right] . \tag{17}$$

2. SIMULTANEOUS INPUT CURRENT SENSING EMPLOYED

Eliminating v_2 from equation (10) by means of equation (11) gives directly

$$h_{21} = h'_{21} \left(1 + (h_{22}/Y_L)\right) . \tag{18}$$

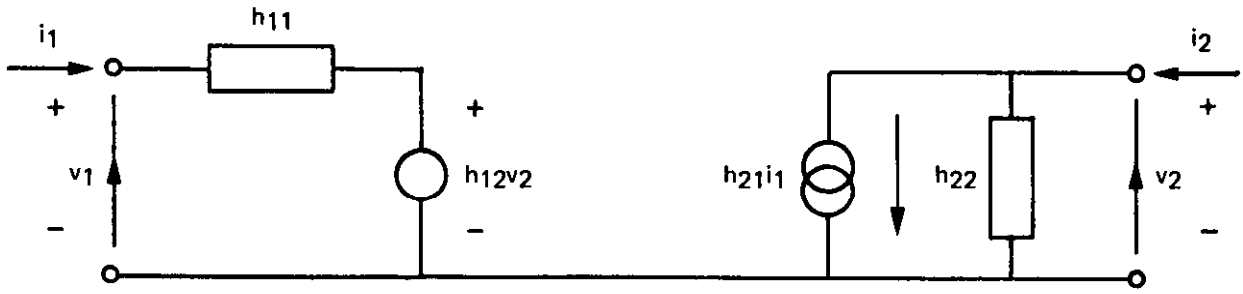

Fig. 1 – Hybrid Parameters of Transistor Under Test

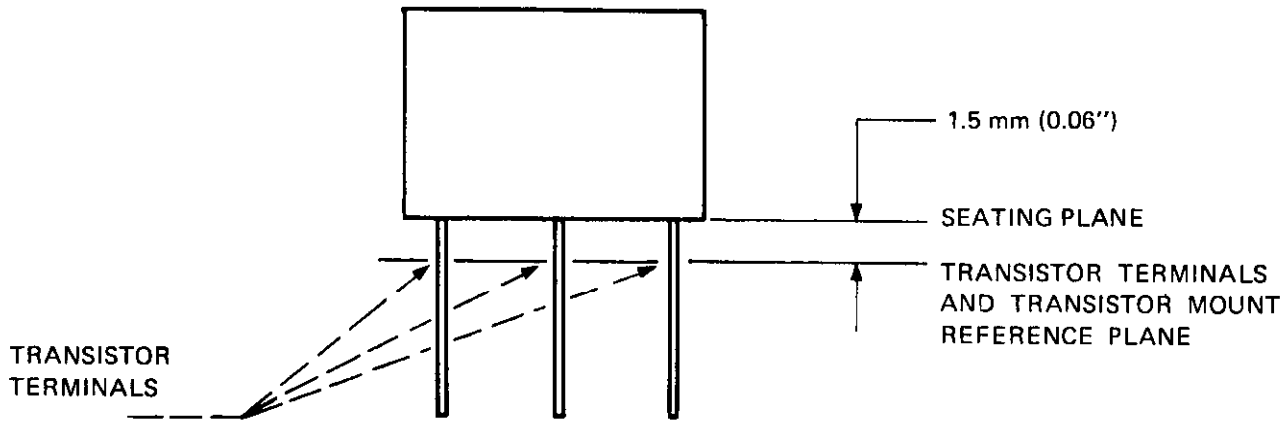

Fig. 2 – Transistor Terminals

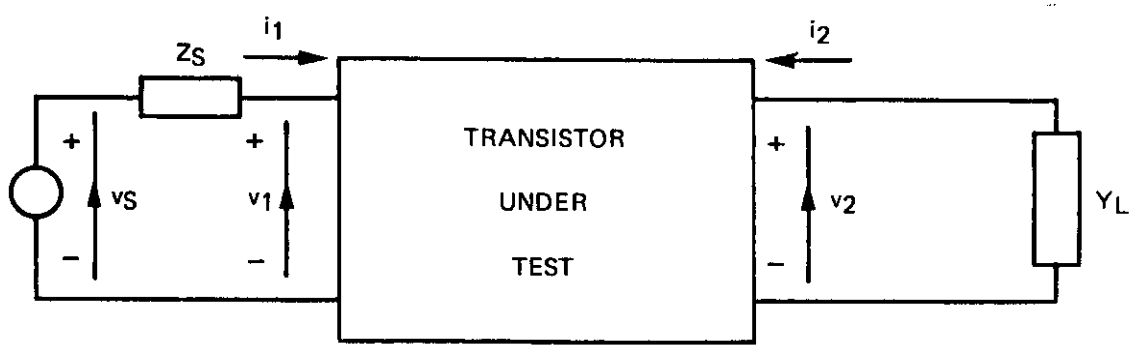

Fig. 3 – Source Impedance and Load Admittance

RELATED EIA STANDARDS

In addition to this Standard, the following EIA Standards are available on measurements of semiconductor devices in VHF and UHF applications:

RS-306	Standards for Measurement of Small Signal HF, VHF and UHF Power Gain Transistors (NEMA Publication No. SK 506-1965)	$ .60
RS-311	Measurement of Transistor Noise Figure at HF and VHF (NEMA Publication No. SK 509-1965)	$1.00
RS-372	The Measurement of Small Signal VHF-UHF Transistor Admittance Parameters	$1.80

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