JEDEC STANDARD

Ball Grid Array Pinouts Standardized for 16-Bit Logic Functions

JESD75-2

JULY 2001

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

EIA
Electronic Industries Alliance

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Council level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7559 or www.jedec.org.

Published by

JEDEC Solid State Technology Association 2001
2500 Wilson Boulevard
Arlington, VA 22201-3834

Price: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada (1-800-854-7179), International (303-397-7956)

Printed in the U.S.A.

PLEASE!

DON'T VIOLATE
THE
LAW!

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS

(Formerly JEDEC Board Ballot JCB-00-104, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines device pinout for 16-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to VFBGA-packaged 16-bit logic devices.

To provide a pinout standard for 16-bit logic devices offered in a 56-ball area grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Definitions for the purpose of this document

DIP: Dual In-line Pin Package (gull-wing)

VFBGA: Very-Thin-Profile Fine-Pitch Ball Grid Array (MO-225)

SSOP: Shrink Small-Outline Package; 0.25" lead pitch; 0.3" wide body (MO-118)

TSSOP: Thin Shrink Small-Outline Package; 0.5-mm lead pitch; 6.4-mm wide body (MO-153)

TVSOP: Thin Very Small-Outline Package; 0.4-mm lead pitch; 4.4-mm wide body (MO-194)

3 Pinout standard

3.1 Description

The following criteria shall be used to convert existing 16-bit logic device functions offered in 48- and 56-pin DIP packages (SSOP, TSSOP, TVSOP) to 16-bit logic device functions offered in the 56-ball VFBGA package:

A. Attributes for the VFBGA package shall be as follows:

56-Ball, 0.65-mm ball pitch with 4.5-mm × 7-mm body size and 6-row × 10-column ball matrix.

B. Device conversion shall be as follows:

DIP package	VFBGA package
48-pin	56-ball
56-pin	56-ball

C. The pinout conversions shall be in accordance with the diagrams shown in section 3.3 and 3.6.

3 Pinout standard (cont'd)

3.2 56-ball VFBGA (MO-225)

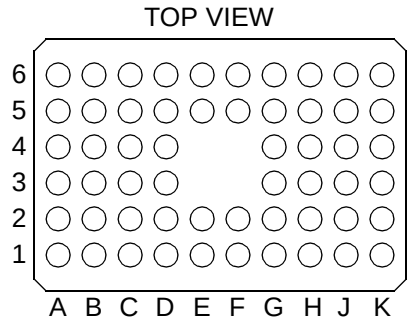

Figure 1 — Pinout configuration

3.3 Pin conversion from 48-pin DIP to 56-ball VFBGA

The pin conversion adopts the naming convention of logic devices in 48-pin DIP packages (e.g., SSOP, TSSOP, TVSOP).

	A	B	C	D	E	F	G	H	J	K
6	48§	46¶	43¶	40¶	37¶	36¶	33¶	30¶	27¶	25§
5	NC*	47¶	44¶	41¶	38¶	35¶	32¶	29¶	26¶	NC*
4	NC*	45†	42‡	39†			34†	31‡	28†	NC*
3	NC*	4†	7‡	10†			15†	18‡	21†	NC*
2	NC*	2¶	5¶	8¶	11¶	14¶	17¶	20¶	23¶	NC*
1	1§	3¶	6¶	9¶	12¶	13¶	16¶	19¶	22¶	24§

Figure 2 — Pin conversion top view

3.4 Pin assignment for 56-ball VFBGA converted from 48-pin DIP

†GND Pins: B3, B4, D3, D4, G3, G4, J3, and J4

‡V_{DD} Pins: C3, C4, H3, and H4

§Control Pins: A1, A6, K1, and K6

¶I/O and Signal Pins: B1, B2, B5, B6, C1, C2, C5, C6, D1, D2, D5, D6, E1, E2, E5, E6, F1, F2, F5, F6, G1, G2, G5, G6, H1, H2, H5, H6, J1, J2, J5, and J6

*No Connection Pins: A2, A3, A4, A5, K2, K3, K4, and K5

Unpopulated Locations: E3, E4, F3, and F4

3 Pinout standard (cont'd)

3.5 56-ball VFBGA (MO-225)

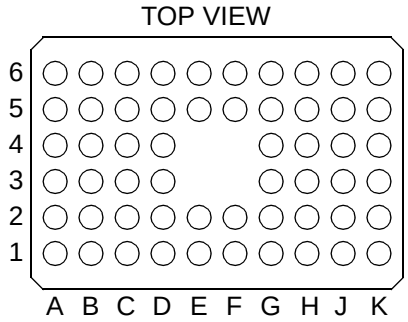

Figure 3 — Pinout configuration

3.6 Pin conversion from 56-pin DIP to 56-ball VFBGA

The pin conversion adopts the naming convention of logic devices in 56-pin DIP packages (e.g. SSOP, TSSOP, TVSOP).

	A	B	C	D	E	F	G	H	J	K
6	54§	51#	48#	45#	43#	42#	40#	37#	34#	31§
5	55§	52#	49#	47#	44#	41#	38#	36#	33#	30§
4	56¶	53†	50‡	46†			39†	35‡	32†	29¶
3	1§	4†	7‡	11†			18†	22‡	25†	28§
2	2§	5#	8#	10#	13#	16#	19#	21#	24#	27§
1	3§	6#	9#	12#	14#	15#	17#	20#	23#	26§

Figure 4 — Pin conversion top view

3.7 Pin assignment for 56-ball VFBGA converted from 56-pin DIP

†GND Pins: B3, B4, D3, D4, G3, G4, J3, and J4

‡V_{DD} Pins: C3, C4, H3, and H4

§Control Pins: A1, A2, A3, A5, A6, K1, K2, K3, K5 and K6

¶GND or Control Pins: A4, and K4

#I/O Pins: B1, B2, B5, B6, C1, C2, C5, C6, D1, D2, D5, D6, E1, E2, E5, E6, F1, F2, F5, F6, G1, G2, G5, G6, H1, H2, H5, H6, J1, J2, J5, and J6

Unpopulated Locations: E3, E4, F3, and F4

4 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*


JEDEC