JEDEC STANDARD

Ball Grid Array Pinouts Standardized for 8-Bit Logic Functions

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BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS

(Formerly JEDEC Board Ballot JCB-01-16, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

PLEASE!

DON'T VIOLATE
THE
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1 Scope

This standard defines device pinout for 8-bit wide buffer, driver, transceiver, latch and flip-flop functions. This pinout specifically applies to the conversion of DIP-packaged 8-bit logic devices to VFBGA-packaged 8-bit logic devices.

The purpose of this standard is to provide a pinout standard for 8-bit logic devices offered in a 20-ball area grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Definitions for the purpose of this document

DIP: Dual In-line Pin Package (gull-wing)

VFBGA: Very-Thin-Profile Fine-Pitch Ball Grid Array (MO-225, Variation BC)

SSOP: Shrink Small-Outline Package; 0.65-mm lead pitch; 5.3-mm wide body (MO-150)

TSSOP: Thin Shrink Small-Outline Package; 0.65-mm lead pitch; 4.4-mm wide body (MO-153)

TVSOP: Thin Very Small-Outline Package; 0.4-mm lead pitch; 4.4-mm wide body (MO-194)

3 Pinout standard

3.1 Description

The following criteria shall be used to convert existing 8-bit logic device functions offered in 20-pin DIP packages (SSOP, TSSOP, TVSOP) to 8-bit logic device functions offered in the 20-ball VFBGA package:

A. Attributes for the VFBGA package shall be as follows:

   20-Ball, 0.65-mm ball pitch with 3-mm × 4-mm body size and 4-row × 5-column ball matrix.

B. The pinout conversion shall be in accordance with the diagram shown in section 3.3.

3 Pinout standard (cont'd)

3.2 20-ball VFBGA (MO-225 Variation BC)

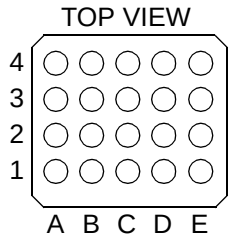

Figure 1 — Pinout configuration

3.3 Pin conversion from 20-pin DIP to 20-ball VFBGA

The pin conversion adopts the naming convention of logic devices in 20-pin DIP packages (e.g., SSOP, TSSOP, TVSOP).

4	19[§]	18[¶]	16[¶]	14[¶]	12[¶]
3	20[‡]	3[¶]	15[¶]	7[¶]	11[¶]
2	1[§]	17[¶]	5[¶]	13[¶]	9[¶]
1	2[¶]	4[¶]	6[¶]	8[¶]	10[†]
	A	B	C	D	E

Figure 2 — Pin conversion top view

3.4 Pin assignment for 20-ball VFBGA

[†]GND Pin: E1

[‡]V_{DD} Pin: A3

[§]Control Pins: A2, and A4

[¶]I/O and Signal Pins: A1, B1, B2, B3, B4, C1, C2, C3, C4, D1, D2, D3, D4, E2, E3, and E4

4 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*


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