JEDEC STANDARD

Definition of CVF857 PLL Clock Driver for Registered PC1600, PC2100, PC2700 and PC3200 DIMM Applications

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STANDARD FOR DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, PC2700 AND PC3200 DIMM APPLICATIONS

(From JEDEC Board Ballot JCB-03-86, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CVF857 PLL clock device for registered PC1600, PC2100, PC2700 and PC3200 DIMM applications.

The purpose is to provide a standard for a CVF857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Terms and definitions (for the purpose of this document)

$C_{I(\Delta)}$ – Delta input capacitance.

3 Device standard

3.1 Description

This PLL Clock Buffer is specified for a V_{DDQ} of 2.5 V (PC1600, PC2100 and PC2700) and 2.6 V (PC3200); an AV_{DD} of 2.5 V (PC1600, PC2100 and PC2700) and 2.6 V (PC3200); and differential data input and output levels. Package options include plastic 48-pin Thin Shrink Small-Outline Package (TSSOP) and 40-pin Very Fine Pitch Quad Flat No-Lead Package (VFQFPN).

The device is a zero delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pair of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the 2.5-V LVCMOS input ($\overline{\text{PWRDWN}}$) and the Analog Power input (AV_{DD}). When input $\overline{\text{PWRDWN}}$ is low while power is applied, the receivers are disabled, the PLL is turned off and the differential clock outputs are 3-stated. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes.

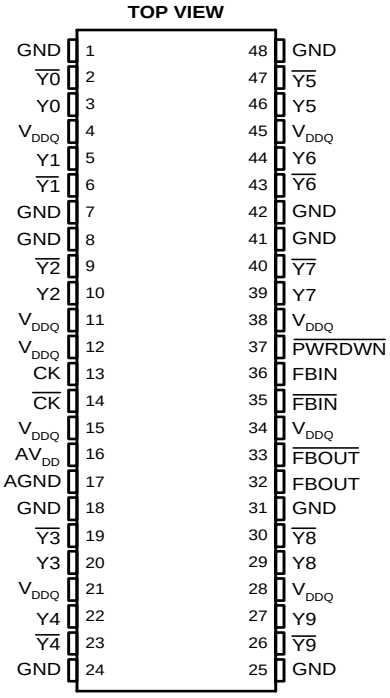
When the input frequency is less than approximately 20 MHz, which is below the operating frequency of the PLL, the device will enter a low power mode. An input frequency detection circuit on the differential inputs, independent from the input buffers, will detect the low frequency condition and perform the same low power features as when the $\overline{\text{PWRDWN}}$ input is low. When the input frequency increases to greater than approximately 20 MHz, the PLL will be turned back on, the inputs and outputs will be enabled and PLL will obtain phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the input clock pair (CK, $\overline{\text{CK}}$).

The PLL in the CVF857 clock driver uses the input clocks (CK, $\overline{\text{CK}}$) and the feedback clocks (FBIN, $\overline{\text{FBIN}}$) to provide high-performance, low-skew, low-jitter output differential clocks (Y[0:9], $\overline{\text{Y[0:9]}}$). The CVF857 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

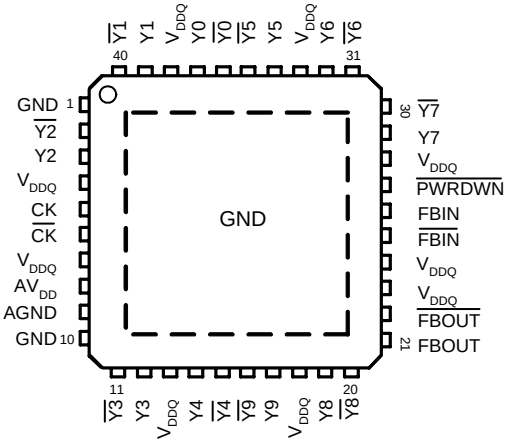
The CVF857 is characterized for operation from 0 ^{o}C to 70 ^{o}C.

3 Device standard (cont'd)

3.2 Pinout figure



48-pin TSSOP (MO-153-ED)



40-pin HP-VFQFP-N (6.0x6.0mm Body Size, 0.5mm Pitch, M0#220, variation VJJD-2, E2=D2=2.9mm +/- 0.15mm) package pinouts

Figure 1 — 48-Pin TSSOP and 40-pin HP-VFQFP-N package pinouts

3.3 Terminal functions

Table 1 — Terminal Functions

Terminal Name	Description		Electrical Characteristics
AGND	Analog Ground		Ground
AV_{DD}	Analog power	PC1600, PC2100, PC2700	2.5 V nominal
		PC3200	2.6 V nominal
CK	Clock input		Differential input
$\overline{CK}$	Complementary clock input		Differential input
FBIN	Feedback clock input		Differential input
$\overline{FBIN}$	Complementary feedback clock input		Differential input
FBOUT	Feedback clock output		Differential output
$\overline{FBOUT}$	Complementary feedback clock output		Differential output
$\overline{PWRDWN}$	Power down		LVCMOS input
GND	Ground		Ground
V_{DDQ}	Logic and output power	PC1600, PC2100, PC2700	2.5 V nominal
		PC3200	2.6 V nominal
Y[0:9]	Clock outputs		Differential outputs
$\overline{Y[0:9]}$	Complementary clock outputs		Differential outputs

3 Device standard (cont'd)

3.4 Function table

Table 2 — Function table (see Note 1)

Inputs				Outputs				PLL
AV_{DD}	$\overline{PWRDWN}$	CK	$\overline{CK}$	Y	$\overline{Y}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
Nominal	H	L	H	L	H	L	H	On
Nominal	H	H	L	H	L	H	L	On
Nominal	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

NOTE 1 AV_{DD} Nominal is 2.5 V for PC1600, PC2100 and PC2700; and 2.6 V for PC3200.

3.5 Logic diagram

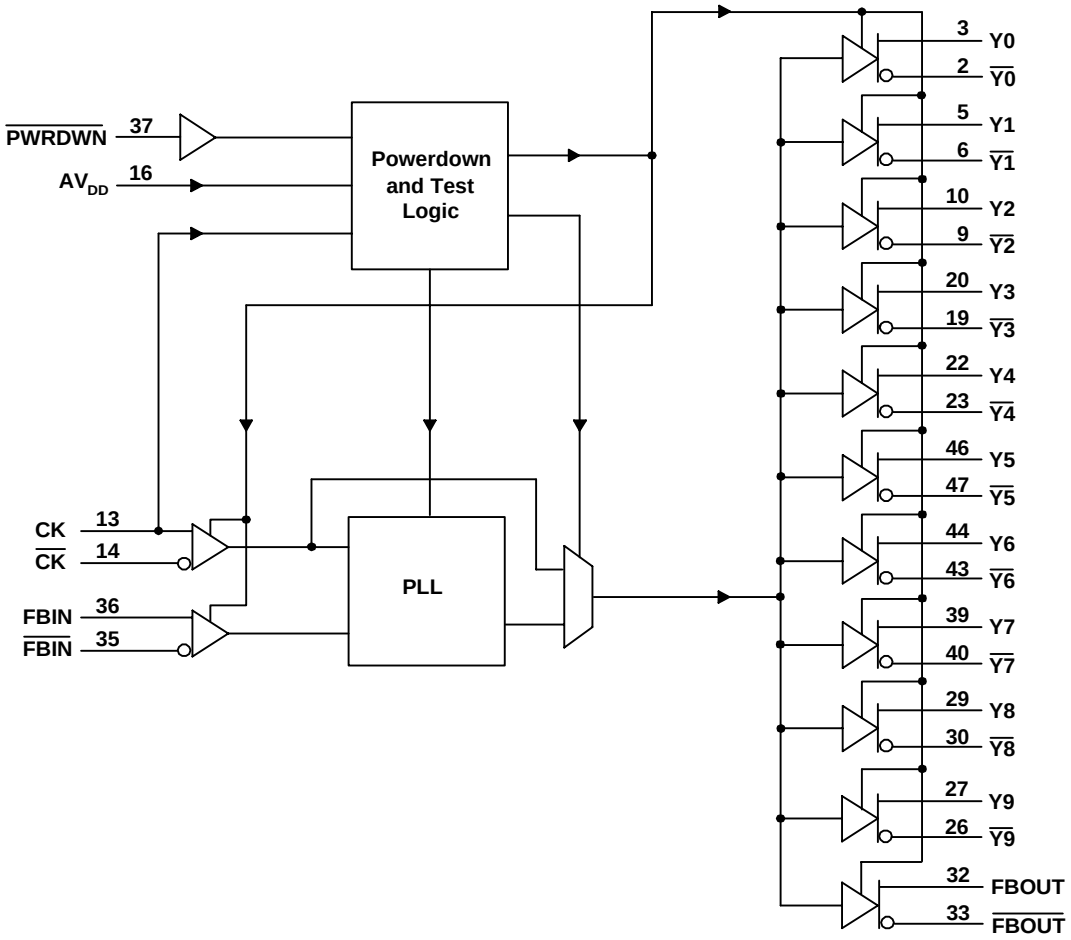


Figure 2 — Logic diagram (positive logic)

3 Device standard (cont'd)

3.6 Absolute maximum ratings

Table 3 — Absolute maximum ratings over operating free-air temperature range (see Note 2)

Supply voltage range, V_{DDQ} or AV_{DD} . . . . . –0.5 V to 3.6 V
Input voltage range, V_I (see Notes 3 and 4) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O (see Notes 3 and 4) . . . . . –0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ}) . . . . . ±50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDQ}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{DDQ}) . . . . . ±50 mA
Continuous current through each AV_{DD}, V_{DDQ} or GND. . . . . ±100 mA
Storage temperature range, T_{STG}. . . . . –65 °C to 150 °C

NOTE 2 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 3 The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 4 This value is limited to 3.6 V maximum.

3.7 Recommended operating conditions

Table 4 — Recommended operating conditions

			Min	Nom	Max	Unit
V_{DDQ}	Output supply voltage	PC1600-2700	2.3	2.5	2.7	V
		PC3200	2.5	2.6	2.7	V
AV_{DD}	Supply voltage	See Note 5,7	V_{DDQ}-0.12	V_{DDQ}	2.7	V
V_{IL}	Low-level input voltage	$\overline{PWRDWN}$	–0.3		0.7	V
V_{IH}	High-level input voltage	$\overline{PWRDWN}$	1.7		V_{DDQ} + 0.3	V
I_{OH}	High-level output current				12	mA
I_{OL}	Low-level output current				–12	mA
V_{IX}	Input differential-pair cross voltage		(V_{DDQ}/2) – 0.2		(V_{DDQ}/2) + 0.2	V
V_{IN}	Input voltage level		–0.3		V_{DDQ} + 0.3	V
V_{ID}	Input differential voltage, See Note 6	DC	0.36		V_{DDQ} + 0.6	V
		AC	0.70		V_{DDQ} + 0.6	V
T_A	Operating free-air temperature		0		70	°C

NOTE 5 The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operationing conditions and no timing parameters are guaranteed.

NOTE 6 V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

NOTE 7 $AV_{DD} \leq V_{DDQ}$ with a tolerance of 0.12 V.

3 Device standard (cont'd)

3.8 DC specifications

Table 5 — Electrical characteristics over recommended operating free-air temperature range for PC1600, PC2100 and PC2700

PARAMETER		TEST CONDITIONS	AV_{DD}, V_{DDQ}	MIN	TYP	MAX	UNIT
V_{IK}	All inputs	I_I = –18 mA	2.3 V			–1.2	V
V_{OH}	High output voltage	I_{OH} = –100 µA	2.3 V to 2.7 V	V_{DDQ}–0.1			V
		I_{OH} = –12 mA	2.3 V	1.7			
V_{OL}	Low output voltage	I_{OL} = 100 µA	2.3 V to 2.7 V			0.1	V
		I_{OL} = 12 mA	2.3 V			0.6	
I_I	CK, FBIN	$V_I = V_{DDQ}$ or GND	2.7 V			±10	µA
	$\overline{PWRDWN}$	$V_I = V_{DDQ}$ or GND	2.7 V			±10	
I_{DDPD}	Static supply current, $I_{DDQ} + I_{ADD}$	CK and $\overline{CK}$ = 0 MHz and $\overline{PWRDWN}$ = Low			100	200	µA
I_{DDQ}	Dynamic supply current, see Note 8 for C_{PD} calculation	CK and $\overline{CK}$ = 170 MHz, all outputs are open (not connected to a PCB)	2.7 V		200	300	mA
I_{ADD}	Dynamic supply current, see Note 8 for C_{PD} calculation	CK and $\overline{CK}$ = 170 MHz	2.7 V		9	12	mA
C_I	CK and $\overline{CK}$	$V_I = V_{DDQ}$ or GND, Part-to-Part variation (ΔC_I) is less than 1pF	2.5 V	2		3.5	pF
	FBIN and $\overline{FBIN}$			2		3.5	
$C_{I(\Delta)}$	CK and $\overline{CK}$	$V_I = V_{DDQ}$ or GND		–0.25		0.25	
	FBIN and $\overline{FBIN}$	$V_I = V_{DDQ}$ or GND		–0.25		0.25	

NOTE 8 Total $I_{DD} = I_{DDQ}+I_{ADD} = F_{CK}* C_{PD}* V_{DDQ}$, solving for $C_{PD} = (I_{DDQ}+I_{ADD})/(F_{CK}*V_{DDQ})$ where F_{CK} is the input Frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

Table 6 — Electrical characteristics over recommended operating free-air temperature range for PC3200

PARAMETER		TEST CONDITIONS	AV_{DD}, V_{DDQ}	MIN	TYP	MAX	UNIT
V_{IK}	All inputs	I_I = –18 mA	2.5 V			–1.2	V
V_{OH}	High output voltage	I_{OH} = –100 µA	2.5 V to 2.7 V	V_{DDQ}–0.1			V
		I_{OH} = –12 mA	2.5 V	1.7			
V_{OL}	Low output voltage	I_{OL} = 100 µA	2.5 V to 2.7 V			0.1	V
		I_{OL} = 12 mA	2.5 V			0.6	
I_I	CK, FBIN	$V_I = V_{DDQ}$ or GND	2.7 V			±10	µA
	$\overline{PWRDWN}$	$V_I = V_{DDQ}$ or GND	2.7 V			±10	
I_{DDPD}	Static supply current, $I_{DDQ} + I_{ADD}$	CK and $\overline{CK}$ = 0 MHz and $\overline{PWRDWN}$ = Low			100	200	µA
I_{DDQ}	Dynamic supply current, see Note 9 for C_{PD} calculation	CK and $\overline{CK}$ = 200 MHz, all outputs are open (not connected to a PCB)	2.7 V		200	300	mA
I_{ADD}	Dynamic supply current, see Note 9 for C_{PD} calculation	CK and $\overline{CK}$ = 200 MHz	2.7 V		9	12	mA
C_I	CK and $\overline{CK}$	$V_I = V_{DDQ}$ or GND, Part-to-Part variation (ΔC_I) is less than 1pF	2.6 V	2		3.5	pF
	FBIN and $\overline{FBIN}$			2		3.5	
$C_{I(\Delta)}$	CK and $\overline{CK}$	$V_I = V_{DDQ}$ or GND		–0.25		0.25	
	FBIN and $\overline{FBIN}$	$V_I = V_{DDQ}$ or GND		–0.25		0.25	

NOTE 9 Total $I_{DD} = I_{DDQ}+I_{ADD} = F_{CK}* C_{PD}* V_{DDQ}$, solving for $C_{PD} = (I_{DDQ}+I_{ADD})/(F_{CK}*V_{DDQ})$ where F_{CK} is the input Frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

3 Device standard (cont'd)

3.9 Timing requirements

Table 7 — Timing requirements over recommended operating free-air temperature range.

	DESCRIPTION	DIMM	AV_{DD}, V_{DDQ}	MIN	MAX	UNIT
f_{CK}	Operating clock frequency (see Notes 10 and 11)	PC1600-2700	2.5 V ± 0.2 V	60	170	MHz
		PC3200	2.6 V ± 0.1 V	60	220	
	Application clock frequency (see Notes 10 and 12)	PC1600-2700	2.5 V ± 0.2 V	95	170	MHz
		PC3200	2.6 V ± 0.1 V	95	220	
t_{DC}	Input clock duty cycle	PC1600-2700	2.5 V ± 0.2 V	40	60	%
		PC3200	2.6 V ± 0.1 V	40	60	
t_L	Stabilization time (see Note 13)	PC1600-2700	2.5 V ± 0.2 V		100	µs
		PC3200	2.6 V ± 0.1 V		100	

NOTE 10 The PLL must be able to handle spread spectrum induced skew.

NOTE 11 Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)

NOTE 12 Application clock frequency indicates a range over which the PLL must meet all timing parameters.

NOTE 13 Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when the input clock frequency falls below 20 MHz, entered the power-down mode and later increased above 20 MHz.

3 Device standard (cont'd)

3.10 AC specifications

Table 8 — Switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (Figures 3 and 4)

PARAMETER	DESCRIPTION	DIAGRAM	PC1600, PC2100, and PC2700 AV_{DD}, V_{DDQ} = 2.5 V ± 0.2 V			UNIT
			MIN	Nom	MAX	
*t*jit(cc)	Cycle-to-cycle period jitter	see Figure 6	–75		75	ps
t(∅)	Static phase offset (see Note 14)	see Figure 7	–50	0	50	ps
*t*sk(o)	Output clock skew	see Figure 8			100	ps
*t*jit(per)	Period jitter (see Note 15)	see Figure 9	–75		75	ps
*t*jit(hper)	Half-period jitter (see Note 15)	see Figure 10	–100		100	ps
slr(i)	Input clock slew rate, measured single-ended	see Figure 11	1.0		4.0	V/ns
slr(o)	Output clock slew rate, measured single-ended (see Note 16)	see Figure 11	1.0		2.0	V/ns
V_{OX}	Output differential-pair cross- voltage, See Note 18 and Figure 4		$(V_{DDQ}/2)$ – 0.15		$(V_{DDQ}/2)$ + 0.15	V
The PLL on the CVF857 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
CVF857 PLL designs should target the values below to meet the 200 ps maximum of SSC induced skew:						
	PLL loop bandwidth (see Note 17)		2.0			MHz
	Phase angle				–0.031	degrees

NOTE 14 Static Phase Offset does not include Jitter.

NOTE 15 Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

NOTE 16 The Output Slew Rate is calculated using the load shown in Figure 5 and measured at the 20% and 80% voltage points, see Figure 11.

NOTE 17 The SSC requirements meets the Intel PC100 SDRAM Registered DIMM specification.

NOTE 18 V_{OX} specified at the DRAM clock input or the test load, see Figure 4

3 Device standard (cont'd)

Table 9 — Switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (Figures 3 and 4)

PARAMETER	DESCRIPTION	DIAGRAM	AV_{DD}, V_{DDQ} = 2.6 V ± 0.1 V			UNIT
			MIN	Nom	MAX	
PC3200, Class A						
*t*jit(cc)	Cycle-to-cycle period jitter	see Figure 6	–75		75	ps
t(∅)	Static phase offset (see Note 22)	see Figure 7	–50	0	50	ps
*t*sk(o)	Output clock skew	see Figure 8			75	ps
*t*jit(per)	Period jitter (see Note 24)	see Figure 9	–50		50	ps
*t*jit(hper)	Half-period jitter (see Note 24)	see Figure 10	–75		75	ps
PC3200, Class A+						
*t*jit(cc)	Cycle-to-cycle period jitter	see Figure 6	–50		50	ps
t(∅)	Static phase offset (see Note 19)	see Figure 7	–50	0	50	ps
*t*sk(o)	Output clock skew	see Figure 8			40	ps
*t*jit(per)	Period jitter (see Note 20)	see Figure 9	–40		40	ps
*t*jit(hper)	Half-period jitter (see Note 20)	see Figure 10	–75		75	ps
PC3200, Class A and A+						
slr(i)	Input clock slew rate, measured single-ended	see Figure 11	1.0		4.0	V/ns
slr(o)	Output clock slew rate, measured single-ended (see Note 21)	see Figure 11	1.0		2.0	V/ns
V_{OX}	Output differential-pair cross- voltage, See Note 23 and Figure 4		$(V_{DDQ}/2)$ – 0.15		$(V_{DDQ}/2)$ + 0.15	V
The PLL on the CVF857 must be capable of meeting all the above test parameters while supporting SSC synthesizers with the following parameters:						
	SSC modulation frequency		30.00		50.00	kHz
	SSC clock input frequency deviation		0.00		–0.50	%
CVF857 PLL designs should target the values below to meet the 200 ps maximum of SSC induced skew:						
	PLL loop bandwidth (see Note 22)		2.0			MHz
	Phase angle				–0.031	degrees

NOTE 19 Static Phase Offset does not include Jitter.

NOTE 20 Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.

NOTE 21 The Output Slew Rate is calculated using the load shown in Figure 5 and measured at the 20% and 80% voltage points, see Figure 11.

NOTE 22 The SSC requirements meets the Intel PC100 SDRAM Registered DIMM specification.

NOTE 23 V_{OX} specified at the DRAM clock input or the test load, see Figure 4

4 Output Buffer Characteristics

4.1 Purpose

The following table describes output-buffer Voltage vs. Current (V/I) characteristics that are sufficient to meet the requirements of registered DDR DIMM performance and timings. These characteristics are not necessarily production tested but can be guaranteed by design or characterization. Compliance with these curves is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR DIMM application.

Table 10 — Output buffer voltage vs. current (V/I) characteristics

Voltage (V)	Pull-Down			Pull-Up		
	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)
	TYP	MIN	MAX	TYP	MIN	MAX
–2.7	–91.7	–79.2	–112	127	100	169
–2.6	–88.2	–76.2	–108	122	96.6	162
–2.5	–84.8	–73.2	–104	117	92.8	156
–2.4	–81.3	–70.2	–99.4	112	88.9	150
–2.3	–77.9	–67.2	–95.3	108	85.1	143
–2.2	–74.4	–64.1	–91.1	103	81.3	137
–2.1	–71.0	–61.1	–86.9	98.2	77.4	131
–2.0	–67.5	–58.1	–82.7	93.5	73.6	124
–1.9	–64.1	–55.1	–78.6	88.7	69.8	118
–1.8	–60.6	–52.1	–74.4	83.9	65.9	112
–1.7	–57.2	–49.0	–70.2	79.2	62.1	106
–1.6	–53.8	–46.0	–66.1	74.4	58.2	99.2
–1.5	–50.3	–43.0	–61.9	69.7	54.4	92.9
–1.4	–46.9	–40.0	–57.7	64.9	50.6	86.6
–1.3	–43.4	–37.0	–53.6	60.1	46.7	80.3
–1.2	–40.0	–33.9	–49.4	55.4	42.9	74.0
–1.1	–36.5	–30.9	–45.2	50.6	39.1	67.7
–1.0	–33.1	–27.9	–41.0	45.9	35.2	61.4
–0.9	–29.6	–24.9	–36.9	41.1	31.4	55.1
–0.8	–26.2	–21.9	–32.7	36.3	27.6	48.8
–0.7	–22.8	–18.9	–28.5	31.6	23.8	42.6
–0.6	–19.4	–16.0	–24.4	26.8	19.7	36.2
–0.5	–15.7	–12.5	–20.1	22.1	16.2	29.9
–0.4	–12.5	–9.9	–16.1	17.5	12.7	23.8
–0.3	–9.4	–7.4	–12.1	12.9	9.4	17.7
–0.2	–6.3	–4.9	–8.1	8.5	6.1	11.7
–0.1	–3.1	–2.5	–4.0	4.2	3.0	5.8
0	0	0	0	0	0	0
0.1	3.1	2.4	4.0	–4.0	–2.8	–5.6
0.2	6.2	4.8	8.0	–7.8	–5.4	–10.9

Table 10 — Output buffer voltage vs. current (V/I) characteristics (Continued)

Voltage (V)	Pull-Down			Pull-Up		
	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)
	TYP	MIN	MAX	TYP	MIN	MAX
0.3	9.2	7.2	11.9	–11.3	–7.9	–16.0
0.4	12.2	9.5	15.8	–14.7	–10.2	–20.8
0.5	15.1	11.8	19.6	–17.8	–12.3	–25.3
0.6	17.9	14.0	23.3	–20.7	–14.2	–29.5
0.7	20.7	16.1	27.0	–23.4	–15.9	–33.5
0.8	23.4	18.2	30.5	–25.8	–17.4	–37.1
0.9	26.1	20.2	34.0	–28.0	–18.8	–40.5
1.0	28.7	22.1	37.4	–29.9	–19.9	–43.6
1.1	31.2	24.0	40.8	–31.6	–20.8	–46.4
1.2	33.6	25.7	44.0	–33.1	–21.6	–48.9
1.3	35.9	27.4	47.1	–34.3	–22.1	–51.1
1.4	38.1	29.0	50.1	–35.3	–22.6	–53.0
1.5	40.2	30.4	53.0	–36.1	–22.9	–54.6
1.6	42.2	31.8	55.7	–36.7	–23.1	–55.9
1.7	44.0	32.9	58.3	–37.3	–23.3	–57.1
1.8	45.7	34.0	60.8	–37.7	–23.5	–58.0
1.9	47.2	34.8	63.0	–38.1	–23.7	–58.8
2.0	48.6	35.5	65.0	–38.5	–23.9	–59.6
2.1	49.6	36.0	66.7	–38.9	–24.1	–60.2
2.2	50.5	36.4	68.1	–39.2	–24.2	–60.8
2.3	51.1	36.7	69.1	–39.5	–24.3	–61.3
2.4	51.6	37.0	69.8	–39.7	–24.5	–61.8
2.5	52.0	37.2	70.4	–40.0	–24.6	–62.3
2.6	52.3	37.4	70.8	–40.3	–24.7	–62.7
2.7	52.6	37.6	71.1	–40.5	–24.9	–63.1
2.8	52.8	37.8	71.4	–40.7	–25.0	–63.5
2.9	53.0	38.0	71.7	–40.9	–25.1	–63.9
3.0	53.2	38.2	71.9	–41.2	–25.2	–64.2
3.1	53.5	38.3	72.1	–41.4	–25.4	–64.6
3.2	53.7	38.5	72.4	–41.6	–25.5	–64.9
3.3	53.9	38.7	72.6	–41.8	–25.6	–65.2
3.4	54.1	38.9	72.9	–42.1	–25.7	–65.6
3.5	54.3	39.1	73.1	–42.3	–25.9	–65.9
3.6	54.6	39.2	73.4	–42.5	–26.0	–66.3
3.7	54.8	39.4	73.6	–42.7	–26.1	–66.6
3.8	55.0	39.6	73.9	–43.0	–26.2	–66.9
3.9	55.2	39.8	74.1	–43.2	–26.4	–67.3

Table 10 — Output buffer voltage vs. current (V/I) characteristics (Continued)

Voltage (V)	Pull-Down			Pull-Up		
	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)	I(mA)
	TYP	MIN	MAX	TYP	MIN	MAX
4.0	55.4	40.0	74.4	–43.4	–26.5	–67.6
4.1	55.7	40.1	74.6	–43.6	–26.6	–68.0
4.2	55.9	40.3	74.8	–43.9	–26.7	–68.3
4.3	56.1	40.5	75.1	–44.1	–26.9	–68.6
4.4	56.3	40.7	75.3	–44.3	–27.0	–69.0
4.5	56.5	40.9	75.6	–44.5	–27.1	–69.3
4.6	56.8	41.0	75.8	–44.8	–27.2	–69.7
4.7	57.0	41.2	76.1	–45.0	–27.4	–70.0
4.8	57.2	41.4	76.3	–45.2	–27.5	–70.3
4.9	57.4	41.6	76.6	–45.4	–27.6	–70.7
5.0	57.6	41.8	76.8	–45.7	–27.7	–71.0
5.1	57.9	41.9	77.1	–45.9	–27.9	–71.4
5.2	58.1	42.1	77.3	–46.1	–28.0	–71.7
5.3	58.3	42.3	77.5	–46.3	–28.1	–72.0
5.4	58.5	42.5	77.8	–46.6	–28.2	–72.4

5 Test circuit and switching waveforms

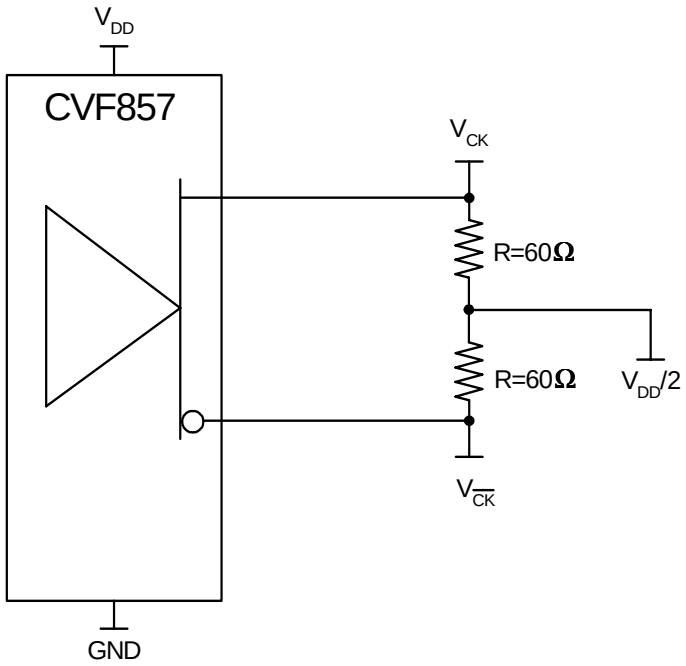


Figure 3 — IBIS Model Output Load

5 Test circuit and switching waveforms (cont'd)

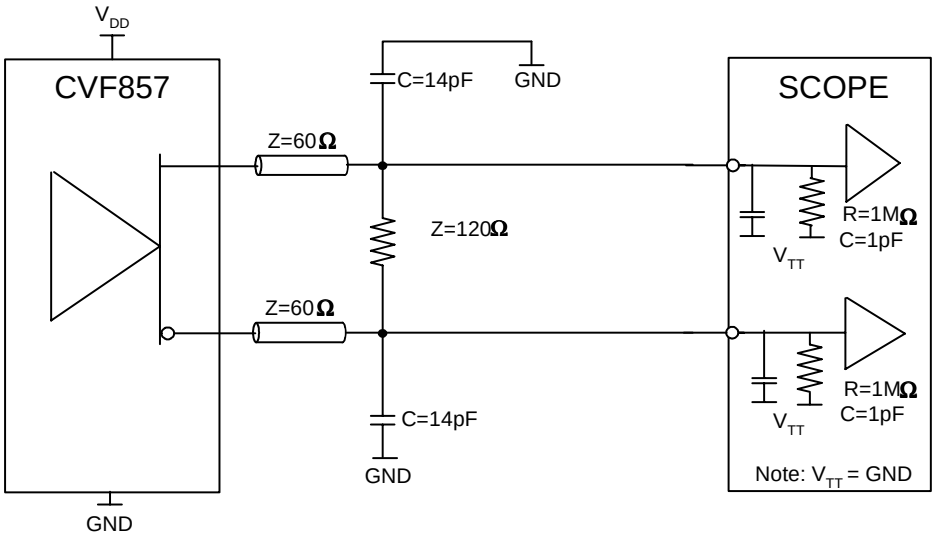


Figure 4 — Output Load Test Circuit 1

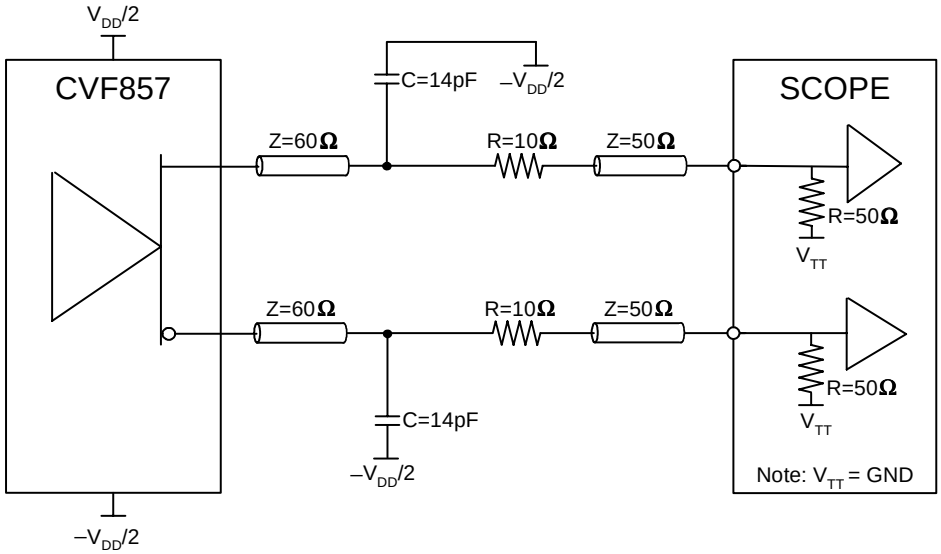


Figure 5 — Output Load Test Circuit 2

5 Test circuit and switching waveforms (cont'd)

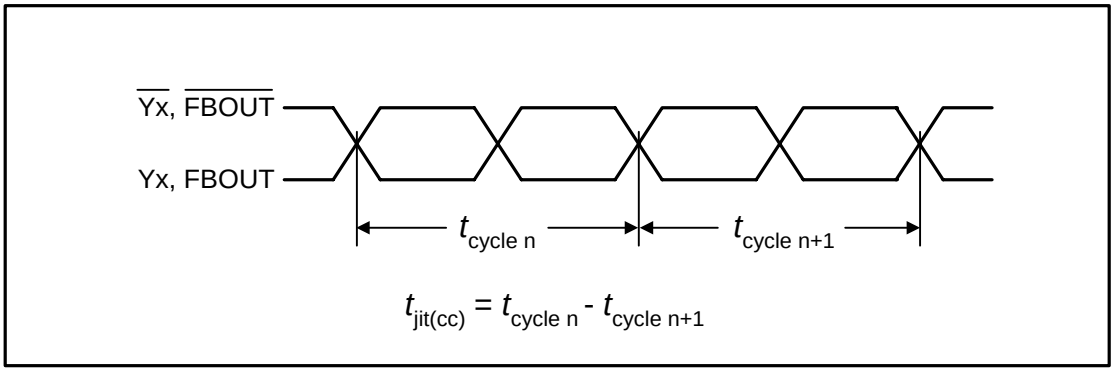


Figure 6 — Cycle-to-Cycle Period Jitter

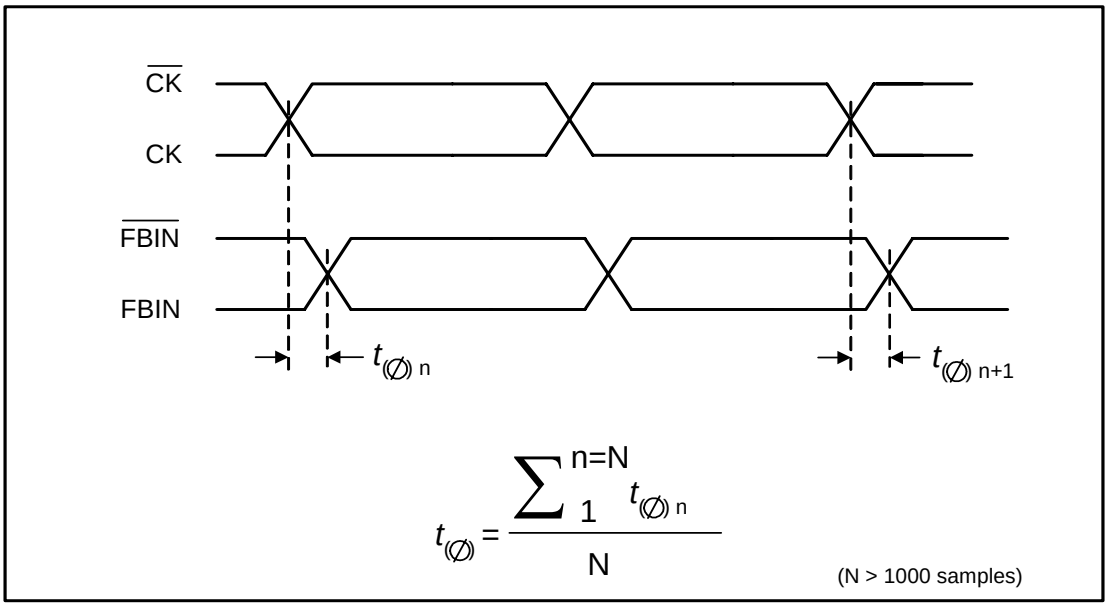


Figure 7 — Static Phase Offset

5 Test circuit and switching waveforms (cont'd)

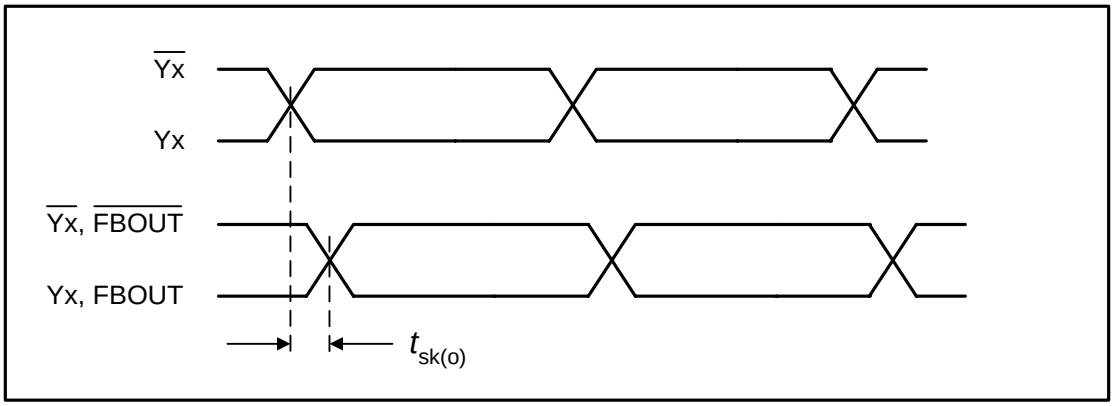


Figure 8 — Output Skew

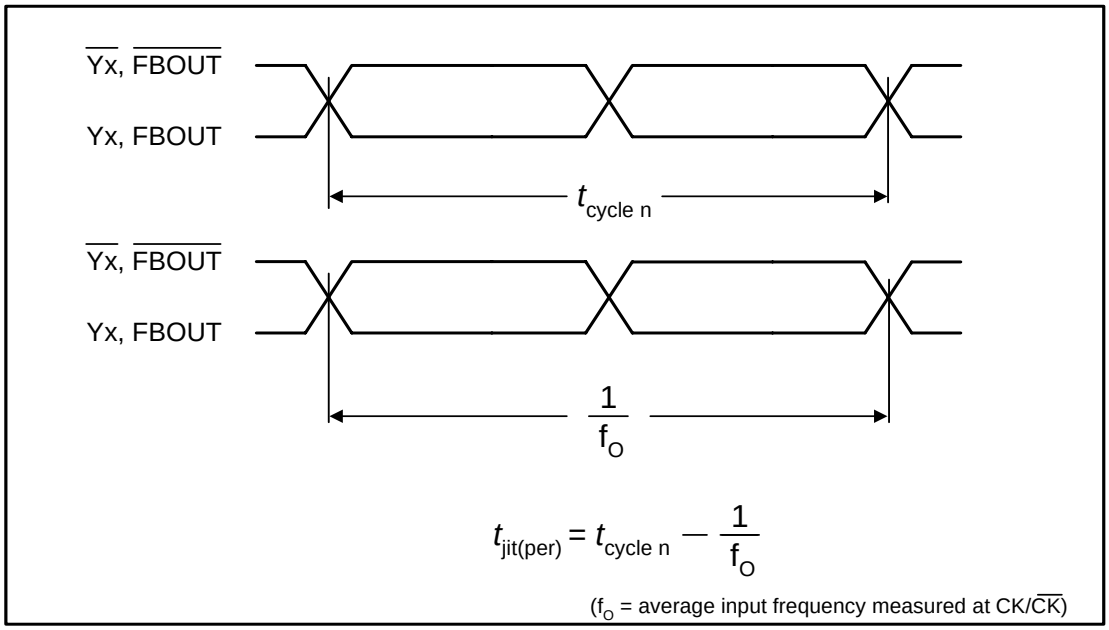


Figure 9 — Period Jitter

5 Test circuit and switching waveforms (cont'd)

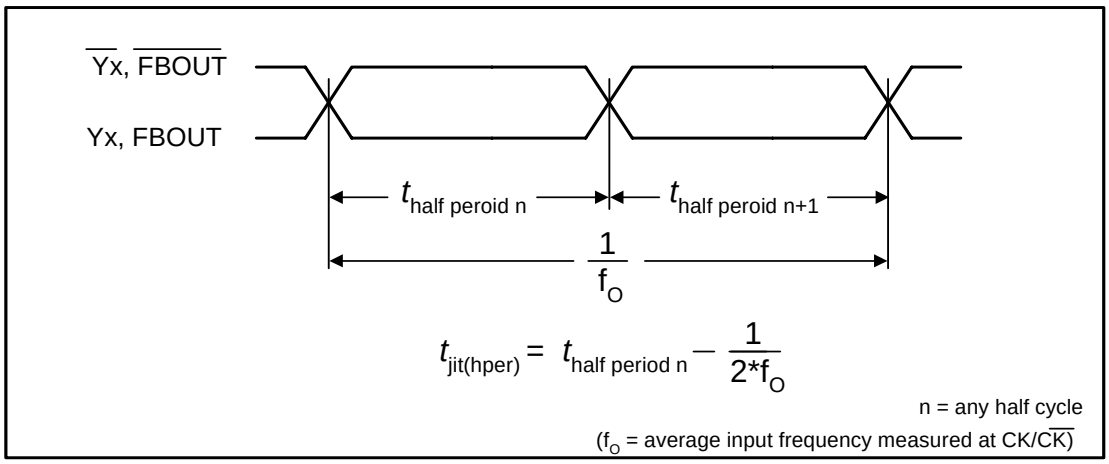


Figure 10 — Half-Period Jitter

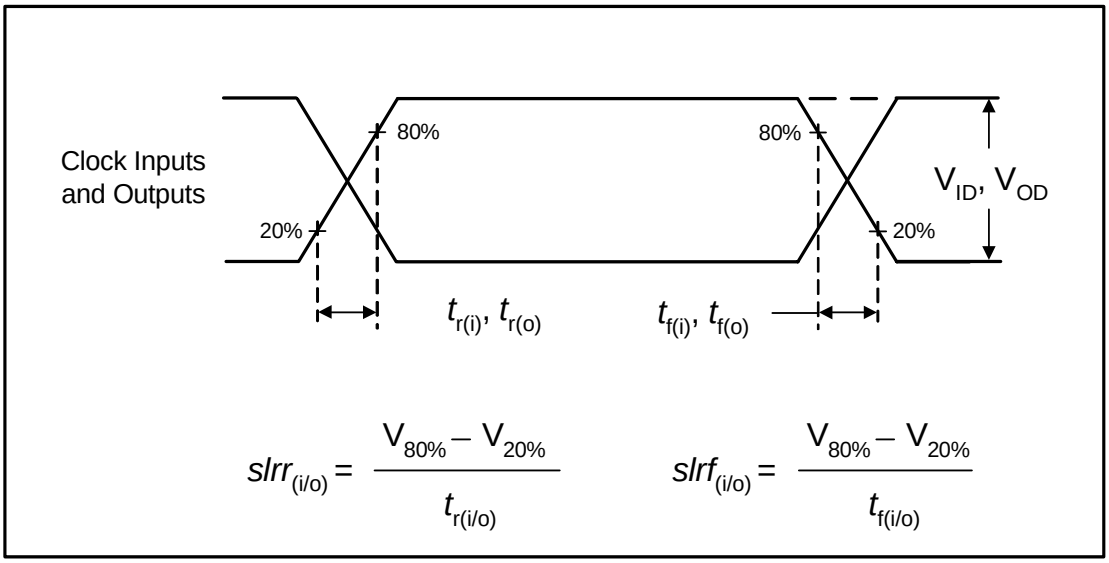
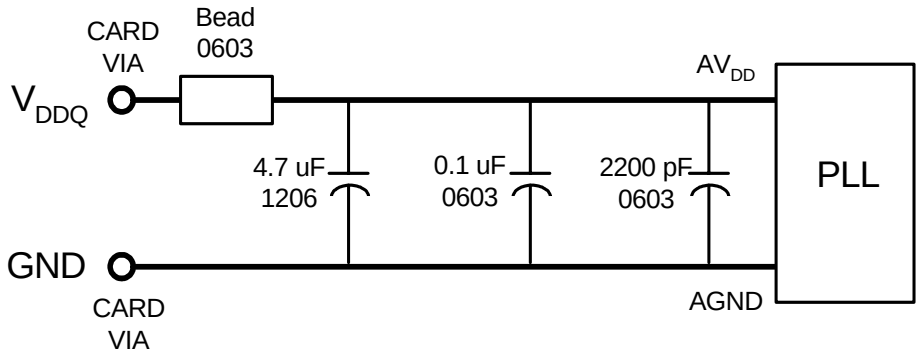


Figure 11 — Input and Output Slew Rates

6 Recommended Filtering for the Analog Power Supply (AV_{DD})



(see Notes 24, 25 and 26)

Figure 12 — AV_{DD} Filtering

NOTE 24 Place the 2200 pF capacitor close to the PLL

NOTE 25 Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from PLL).

NOTE 26 Recommended bead: Fair-Rite P/N 2506036017Y0 or equivalent (0.8 ohms DC max, 600 ohms @ 100 MHz).

7 Reference to other applicable JEDEC standards and publications

JESD65, *Definition of Skew Specification for Standard Logic Devices*

JESD8-5, *2.5 Volt ± 0.2 V (Normal Range) and 1.8 V to 2.7 V (Wide Range) Power Supply Voltage and Interface for Nonterminated Digital Integrated Circuits.*

JESD21-C, *Configuration for Solid State Memories*

Annex A Differences Between JESD82-1A and JESD82-1

This table briefly describes most of the changes made to this standard, JESD82-1A, compared to its predecessor, JESD82-1 (October 2002). Some punctuation changes are not included.

Page	Description of change
2	Scope: Editorially added PC3200 DIMM to description
2	Description: Editorially added PC3200 and "40 pin Very Fine Pitch Quad Flat No-Lead Package (VFQFPN)"
3	figure 1: Added pinout for the 40-pin HP-VFQFP-N package
3	table 1 Av_{DD}: Added 2.6 V nominal voltage for PC3200
3	table 1 $V_{DDQ:}$: Added 2.6V nominal voltage for PC3200
4	table 2 AV_{DD}: from 2.5V (nom) to Nominal
4	table 2: Added "Note: 1 AV_{DD} Nominal is 2.5 V for PC1600, PC2100, and PC2700, and 2.6 V for PC3200"
5	table 4 V_{DDQ}: Added PC3200
6	Table 5: table applies to PC1600, PC2100, and PC2700
7	table 6: Added "Electrical characteristics over recommended operating free-air temperature range for PC3200" table
8	table 7: Added PC3200 to table
9	table 8 slr(i), slr(o): Added "measured single-ended" to description
9	table 8: table applies to PC1600, PC2100, and PC2700
10	table 9: Added "Switching characteristics over recommended operating free-air temperature range" table for PC3200
19	Figure 12: Added AV_{DD} Filtering schematic and Notes 24, 25 and 26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