JEDEC STANDARD

GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD

JESD232A.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD

(From JEDEC Board Ballot JCB-16-39, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories, item number 1827.99B v1.2).

1 SCOPE

This standard defines the GDDR5X SGRAM memory standard, including features, device operation, electrical characteristics, timings, signal pin assignments, and package.

The purpose of this standard is to define the minimum set of requirements for JEDEC standard compatible 4 Gb through 16 Gb x32 GDDR5X SGRAM devices. System designs based on the required aspects of this standard will be supported by all GDDR5X SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR5X standard such as AC timings were not standardized. Some features are optional and therefore may vary among vendors. In all cases, vendor data sheets should be consulted for specifics.

This standard was created based on the GDDR5 SGRAM standard (JESD212). Each aspect of the changes were considered and balloted. The accumulation of these ballots were then incorporated to prepare this GDDR5X SGRAM standard.

2 GDDR5X SGRAM STANDARD OVERVIEW

4 Gb = 128 Mb x 32 (8 Mb x 32 x 16 banks) / 256 Mb x 16 (16 Mb x 16 x 16 banks)
6 Gb = 192 Mb x 32 (12 Mb x 32 x 16 banks) / 384 Mb x 16 (24 Mb x 16 x 16 banks)
8 Gb = 256 Mb x 32 (16 Mb x 32 x 16 banks) / 512 Mb x 16 (32 Mb x 16 x 16 banks)
12 Gb = 384 Mb x 32 (24 Mb x 32 x 16 banks) / 768 Mb x 16 (48 Mb x 16 x 16 banks)
16 Gb = 512 Mb x 32 (32 Mb x 32 x 16 banks) / 1 Gb x 16 (64 Mb x 16 x 16 banks)

2.1 FEATURES

- Single ended interface for command, address and data
- Differential clock input CK_t/CK_c for ADD/CMD
- Two differential clock inputs WCK_t/WCK_c, each associated with two data bytes (DQ, DBI_n, EDC)
- Single Data Rate (SDR) commands (CK)
- Double Data Rate (DDR) addresses (CK)
- QDR and DDR operating modes:
  - QDR mode: Quad Data Rate (QDR) data (WCK); 16n prefetch architecture with 512 bit per array read or write access; burst length 16
  - DDR mode: Double Data Rate (DDR) data (WCK); 8n prefetch architecture with 256 bit per array read or write access; burst length 8
- 16 internal banks
- 4 bank groups for t_{CCDL} = 3 t_{CK} and 4 t_{CK}
- Programmable read latency: 5 to 36 t_{CK}; programmable write latency: 1 to 7 t_{CK}
- Write data mask function via address bus (single/double/quad byte mask)
- Data bus inversion (DBI) and address bus inversion (ABI)
- Input/output PLL/DLL
- Address training: address input monitoring via DQ/DBI_n/EDC pins
- WCK2CK clock training with phase information via EDC pins
- Data read and write training via READ FIFO (depth = 6)
- Read FIFO pattern preload by LDFF command
- Direct write data load to READ FIFO via WRTR command
- Consecutive read of READ FIFO via RDTR command
- Read/write EDC on/off mode
- Programmable EDC hold pattern for CDR
- Read/write data transmission integrity secured by cyclic redundancy check (CRC-8)
- Programmable CRC read latency = 1 to 4 t_{CK}; programmable CRC write latency = 7 to 14 t_{CK}
- Low Power modes
- RDQS mode on EDC pins
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh mode with per-bank refresh option
- Temperature sensor controlled self refresh rate
- Optional digital t_{RAS} lockout
- On-die termination (ODT) for all high-speed inputs
- Pseudo open drain (POD-135) compatible outputs
- ODT and output driver strength auto-calibration with external resistor ZQ pin (120 Ω)
- Programmable termination and driver strength offsets
- Internal V_{REF} for data inputs with programmable levels
- Selectable external or internal V_{REF} for address / command inputs
- Vendor ID for device identification
- Mirror function with MF pin
- IEEE 1149.1 compliant boundary scan
- 1.35 V supply voltage for device operation (V_{DD}) and I/O interface (V_{DDQ})
- 1.8 V pump voltage (V_{PP})
- 190 ball BGA package

3 FUNCTIONAL DESCRIPTION

3.1 FUNCTIONAL OVERVIEW

The GDDR5X SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. It is internally configured as 16-bank memory and contains the following number of bits:

4 Gb has 4,294,967,296 bits
6 Gb has 6,442,450,944 bits
8 Gb has 8,589,934,592 bits
12 Gb has 12,884,901,888 bits
16 Gb has 17,179,869,184 bits

The GDDR5X SGRAM's high-speed interface is optimized for point-to-point connections to a host controller. On-die termination (ODT) is provided for all high-speed interface signals to eliminate the need for termination resistors in the system.

The GDDR5X SGRAM supports two operating modes which mainly differ in the internal prefetch and DQ/DBI_n pin to WCK clock frequency ratio. The operating mode is set by a mode register bit:

- In Quad Data Rate (QDR) mode the interface transfers four 32-bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 16-n prefetch a single write or read access consists of a 512 bit wide, two CK clock cycle data transfer at the internal memory core and sixteen corresponding 32 bit wide one-quarter WCK clock cycle data transfers to the I/O pins.
- In Double Data Rate (DDR) mode the interface transfers two 32-bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8-n prefetch a single write or read access consists of a 256 bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32 bit wide one-half WCK clock cycle data transfers to the I/O pins.

Read and write accesses to the GDDR5X SGRAM are burst oriented; an access starts at a selected location and consists of a total of sixteen data words in QDR mode and eight data words in DDR mode. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command and the next rising CK_c edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK_c edge are used to select the bank and the column location for the burst access.

This standard includes all features and functionality required for JEDEC GDDR5X SGRAM devices. Users benefit from knowing that any system design based on the required aspects of the standard are supported by all GDDR5X SGRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

3.2 SIGNAL STATE TERMINOLOGY

The GDDR5X SGRAM will be operated in both ODT enable (terminated) and ODT disable (unterminated) modes. For highest data rates it is recommended to operate in the ODT enable mode. ODT disable mode is designed to reduce power and may operate at reduced data rates. There exist situations where ODT enable mode can not be guaranteed for a short period of time, for example during power-up.

Four terminologies define the state of a device pin (GDDR5X SGRAM or controller) during operation. The state of the bus will be determined by the combination of the device pins connected to the bus in the system. For example, with GDDR5X it is possible for the device pin to be tristated while the controller pin is High or ODT. In both cases the bus would be High if the ODT is enabled.

Device pin signal level:

- High: a device pin drives the Logic "1" state.
- Low: a device pin drives the Logic "0" state.
- High-Z: a device pin is tristate.
- ODT: a device pin terminates with ODT setting, which could be terminating or tristate depending on mode register setting.

Bus signal level:

- High: one device on the bus is High and all other devices on bus are either ODT or High-Z. The voltage level on the bus would be nominally V_{DDQ}.
- Low: one device on the bus is Low and all other devices on bus are either ODT or High-Z. The voltage level on the bus would be nominally V_{OL}(DC) if ODT is enabled, or V_{SSQ} if High -Z.
- High-Z: all devices on the bus are High-Z. The voltage level on bus is undefined as the bus is floating.
- ODT: at least one device on the bus is ODT and all others are High-Z. The voltage level on the bus would be nominally V_{DDQ}.

3.3 CLOCKING

The GDDR5X SGRAM operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

The data interface uses two differential forwarded clocks WCK_t and WCK_c, each associated with two data bytes. WCK_t and WCK_c are continuously running and operate at twice the frequency of the command/address clock (CK_t/CK_c). A PLL/DLL is associated with each WCK pair. The use of the PLL/DLL is mandatory in QDR mode and vendor specific in DDR mode.

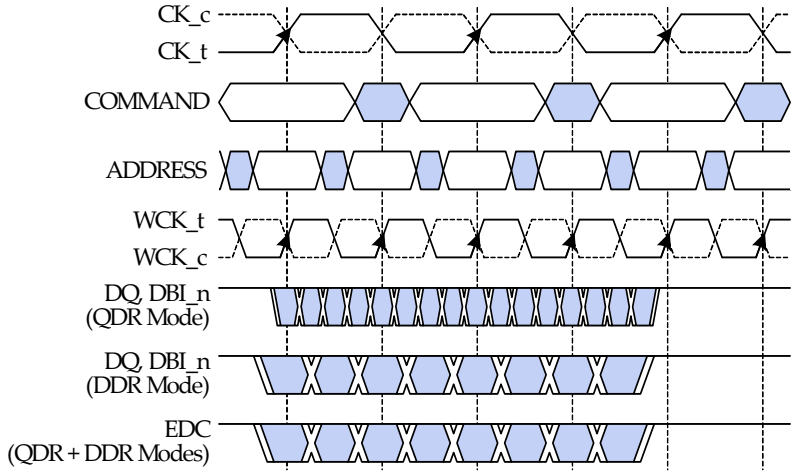
- QDR mode uses a quad data rate data interface and a 16n-prefetch architecture for DQ/DBI_n, and a double data rate data interface and 8n-prefetch architecture for EDC. The PLL/DLL generates four equally spaced clock edges per WCK clock cycle. QDR means that four DQ/DBI_n data words per WCK cycle are registered at these internally generated clock edges. DDR means that two EDC data words per WCK cycle are registered at every second of these internally generated clock edges.
- DDR mode uses a double data rate data interface and an 8n-prefetch architecture for DQ/DBI_n/EDC. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c.

3.3 CLOCKING (cont'd)

Table 1 and Figure 1 illustrate the clock and interface signal relationship for both QDR and DDR operating modes.

Table 1 — Example Clock and Interface Signal Frequency Relationship

PIN	QDR MODE	DDR MODE	UNIT
CK_t, CK_c	1.5	1.5	GHz
Command	1.5	1.5	Gbps/pin
Address	3.0	3.0	Gbps/pin
WCK_t, WCK_c	3.0	3.0	GHz
DQ, DBI_n	12.0	6.0	Gbps/pin
EDC	6.0	6.0	Gbps/pin



NOTE 1 Figure 1 shows the relationship between the data rate of the buses and the clocks and is not a timing diagram.

Figure 1 — GDDR5X Clocking and Interface Relationship

3.3 CLOCKING (cont'd)

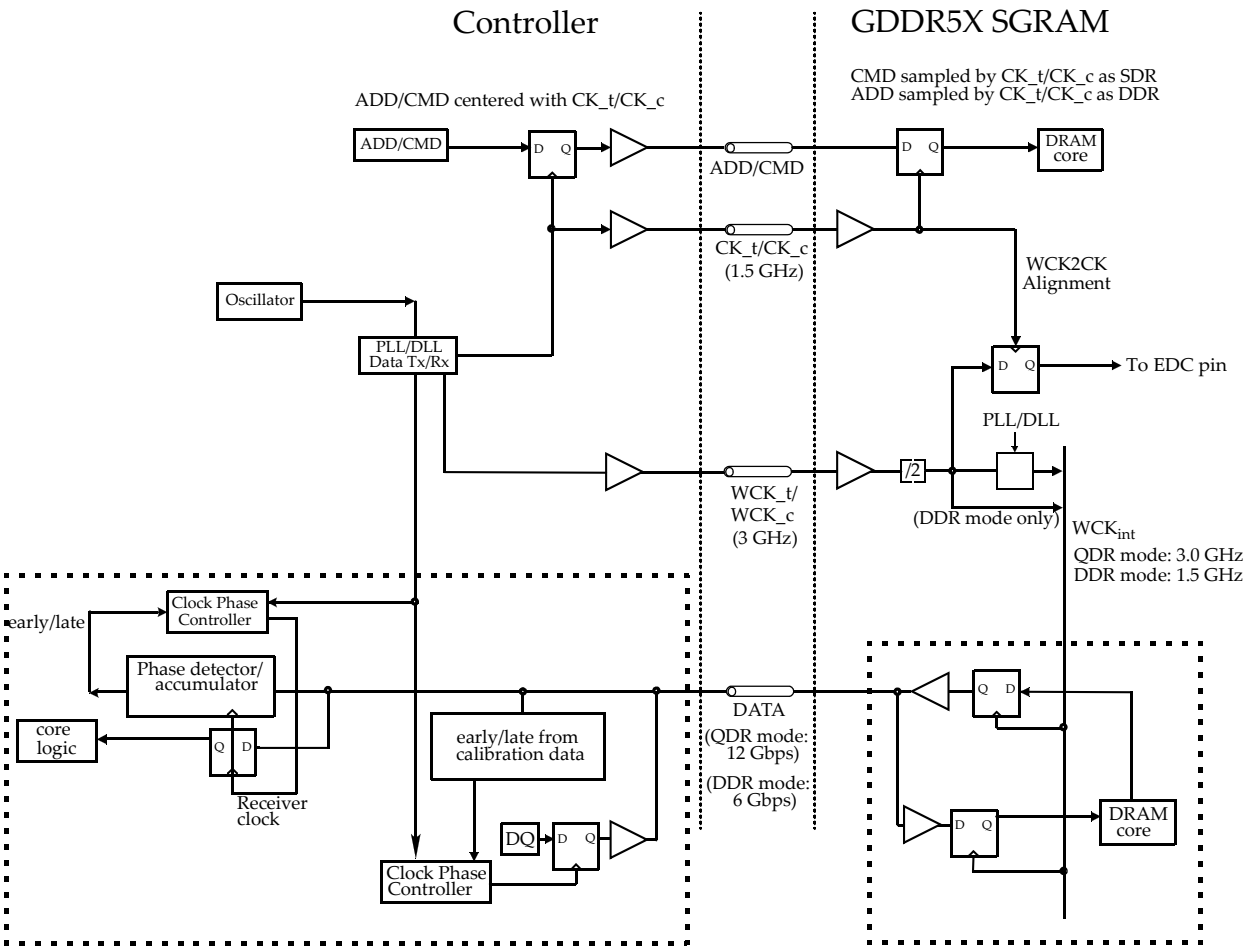


Figure 2 — Block Diagram of an Example Clock System

3.4 ADDRESSING

GDDR5X SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 2. The addresses should be provided in two parts; the first half is latched on the rising edge of CK_t along with the command pins such as RAS_n, CAS_n and WE_n; the second half is latched on the next rising edge of CK_c.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 2 — Address Pairs

Clock	Address Pins									
Rising CK_t	BA3	BA2	BA1	BA0	A14	A12	A11	A10	A9	A8
Rising CK_c	A3	A4	A5	A2	A15	A13	A6	A0	A1	A7

The addressing includes support for 4 Gb to 16 Gb densities and both QDR and DDR operating modes as shown in Table 3.

Table 3 — Addressing Scheme

Density		4 Gb		6 Gb		8 Gb		12 Gb		16 Gb	
I/O Configuration		**x32**	**x16**	**x32**	**x16**	**x32**	**x16**	**x32**	**x16**	**x32**	**x16**
Row address		A0~A12	A0~A13	A0-A13	A0-A14	A0~A13	A0~A14	A0~A14	A0~A15	A0~A14	A0~A15
Column address DQ[15:0]	**QDR Mode**	A0~A5		A0~A5		A0~A5		A0~A5		A0~A5	
	DDR Mode	A0~A6		A0~A6		A0~A6		A0~A6		A0~A6	
Column address DQ[31:16]	**QDR Mode**	A7,A9,A12~A15		A7,A9,A12~A15		A7,A9,A12~A15		A7,A9,A12~A15		A7,A9,A12~A15	
	DDR Mode	A7,A9,A12~A15,A6		A7,A9,A12~A15,A6		A7,A9,A12~A15,A6		A7,A9,A12~A15,A6		A7,A9,A12~A15,A6	
Bank address		BA0~BA3		BA0~BA3		BA0~BA3		BA0~BA3		BA0~BA3	
Autoprecharge		A8		A8		A8		A8		A8	
Page Size		4K	2K	4K	2K	4K	2K	4K	2K	4K	2K
Refresh		16K/32 ms		16K/32 ms		16K/32 ms		16K/32 ms		16K/32 ms	
Refresh period		1.9 μs		1.9 μs		1.9 μs		1.9 μs		1.9 μs	

NOTE 1 The burst order is fixed for Reads and Writes, and the GDDR5X SGRAM does not assign column address bits to distinguish between the UIs of a burst. A memory controller may internally assign such column address bits but these column address bits are not transmitted on the colum address bus to the GDDR5X SGRAM.

NOTE 2 Row address range with A[13:12] = 11 (x32 mode) or A[14:13] = 11 (x16 mode) is not present for 6 Gb density. Row address range with A[14:13] = 11 (x32 mode) or A[15:14] = 11 (x16 mode) is not present for 12 Gb density. ACT/RD/WR commands to these memory locations are illegal.

NOTE 3 Two column addresses CAL and CAU with shared bank addresses are provided with each WRITE and READ command.

NOTE 4 For complete details on refresh refer to the vendor's datasheets for values for refresh interval, refresh period and t_{RFC} as t_{RFC} will scale with density and is vendor specific.

3.4 ADDRESSING (cont'd)

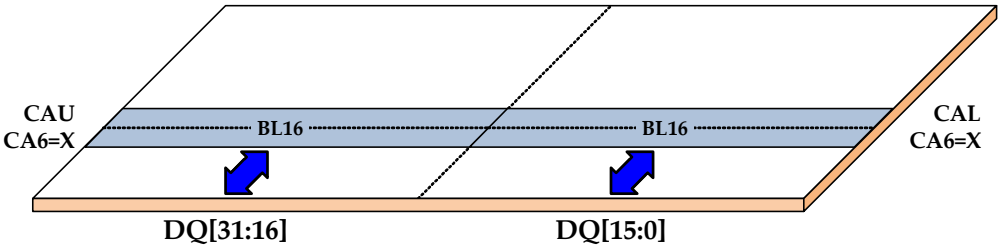
Two column addresses with a common bank address are provided with each READ and WRITE command, allowing two pseudo-independent memory accesses with 32 bytes access granularity in QDR operating mode and 16 bytes access granularity in DDR operating mode:

- The lower column address (CAL) is associated with DQ[15:0] and received on addresses A[5:0].
- The upper column address (CAU) is associated with DQ[31:16] and received on addresses A[15:12, 9, 7].

GDDR5X SGRAM's addressing is transparent between QDR and DDR operating modes: data can be written in QDR operating mode with a single BL=16 WRITE burst, and read in DDR operating mode with two BL=8 READ bursts, and vice versa. Column address A6 is evaluated in DDR operating mode only; it can be considered the LSB and selects between the data corresponding to the first half of a BL=16 burst (UI 0..7) with A6 being set Low, and the data corresponding to the second half of a BL=16 burst (UI 8..15) with A6 being set High.

Figure 3 illustrates the addressing in QDR and DDR operating modes assuming the same column addresses CAL and CAU for lower and upper data bytes. This is equivalent to accesses using a single column address, however, it is required to provide both CAL and CAU along with the READ or WRITE command.

Case 1: Single READ/WRITE burst in QDR Mode (BL16) with CAL = CAU



Case 2: Two READ/WRITE bursts in DDR Mode (BL8) with CAL = CAU

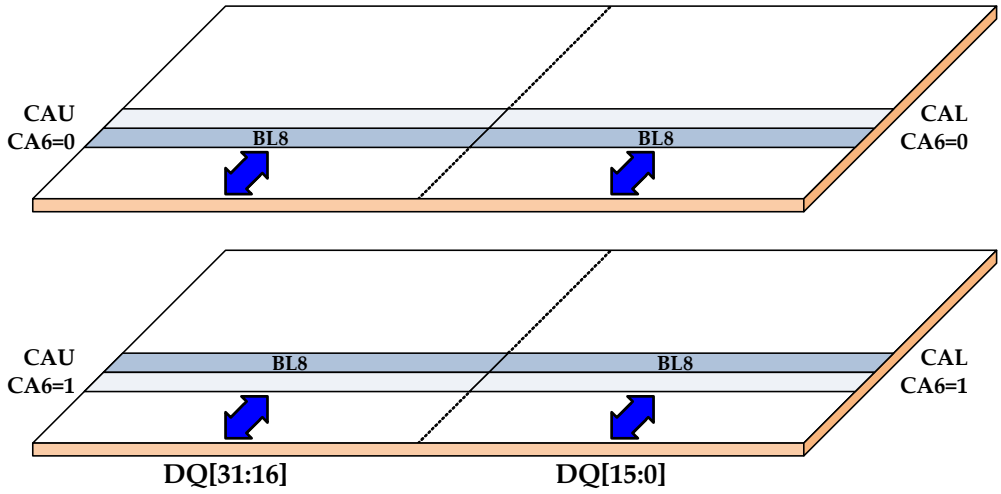
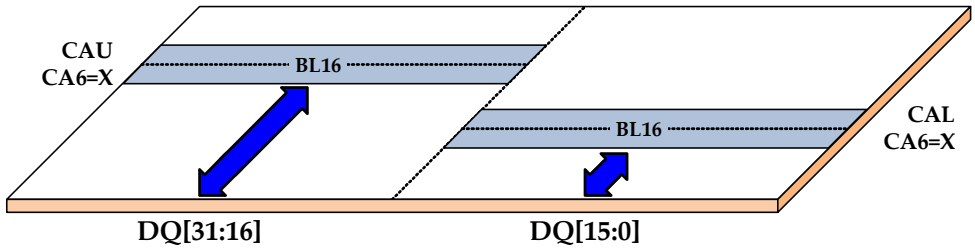


Figure 3 — Column Accesses with Identical Lower and Upper Column Addresses

3.4 ADDRESSING (cont'd)

Figure 4 illustrates the addressing in QDR and DDR operating modes assuming different column address for lower and upper bytes. This corresponds to two pseudo-independent memory accesses with 32 bytes access granularity in QDR operating mode and 16 bytes in DDR operating mode. It is pointed out that both accesses share the bank address and therefore access the same open row in that bank.

Case 3: One READ/WRITE burst in QDR Mode with CAL <> CAU



Case 4: Two READ/WRITE bursts in DDR Mode with CAL <> CAU

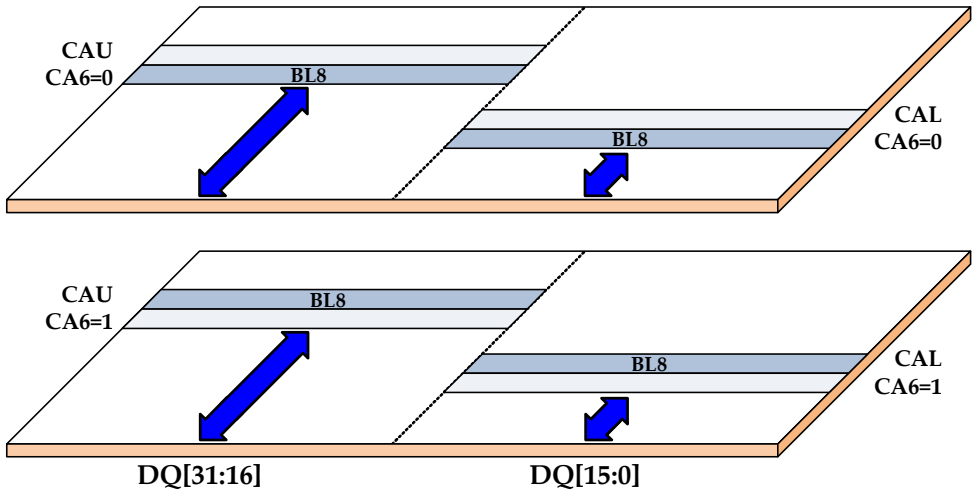
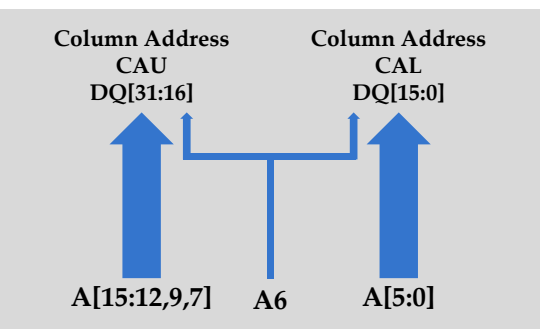


Figure 4 — Column Accesses with Different Lower and Upper Column Addresses

3.4.1 Address Compatibility Mode

GDDR5 SGRAMs receive the column address on the lower address pins only; this column address is used for all data bytes. The address compatibility mode adopts this functionality for GDDR5X SGRAMs (see Figure 3): if enabled by bit A8 in MR8, the device will use the column address received on A[5:0] as CAL and CAU. Address inputs A[15:12, 9, 7] are ignored in this mode. The memory accesses will be identical to those shown in Figure 3 for both BL=16 and BL=8 cases.

Address Compatibility Mode Off



Address Compatibility Mode On

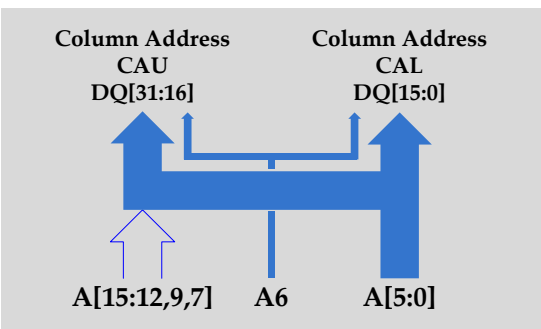


Figure 5 — Address Compatibility Mode

3.5 BANK GROUPS

For devices operating at frequencies above a certain threshold (f_{CKBG}), the activity within a bank group must be restricted to ensure proper operation of the device. The 16 banks are divided into four bank groups. The bank groups feature is controlled by bits A[11:10] in MR3.

Table 4 — Bank Groups

BANKS	ADDRESSING				BANK GROUP
	BA3	BA2	BA1	BA0	
0 to 3	0	0	X	X	Group A
4 to 7	0	1	X	X	Group B
8 to 11	1	0	X	X	Group C
12 to 15	1	1	X	X	Group D

These bank groups allow the specification of different command delay parameters depending on whether back-to-back accesses are to banks within one bank group or across bank groups as shown in Table 5. Figure 6 shows back-to-back column accesses based on t_{CCDL} and t_{CCDS} parameters.

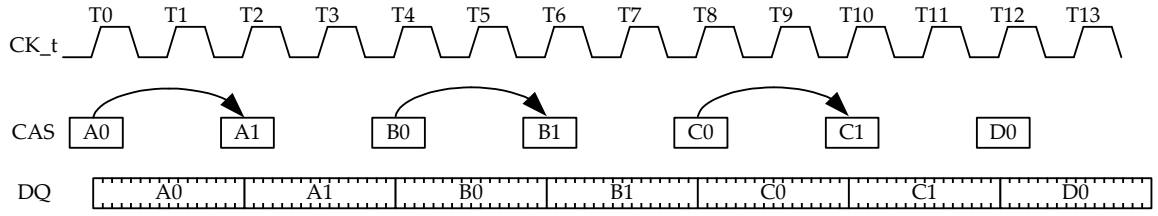
Table 5 — Command Sequences Affected by Bank Groups

COMMAND SEQUENCE	CORRESPONDING AC TIMING PARAMETER			NOTES
	BANK GROUPS DISABLED	BANK GROUPS ENABLED		
		ACCESSES TO DIFFERENT BANK GROUPS	ACCESSES WITHIN THE SAME BANK GROUP	
ACTIVATE to ACTIVATE	t_{RRDS}	t_{RRDS}	t_{RRDL}	
WRITE to WRITE	t_{CCDS}	t_{CCDS}	t_{CCDL}	
READ to READ	t_{CCDS}	t_{CCDS}	t_{CCDL}	
Internal WRITE to READ	t_{WTRS}	t_{WTRS}	t_{WTRL}	
READ to PRECHARGE	t_{RTPS}	1 t_{ck}	t_{RTPL}	1

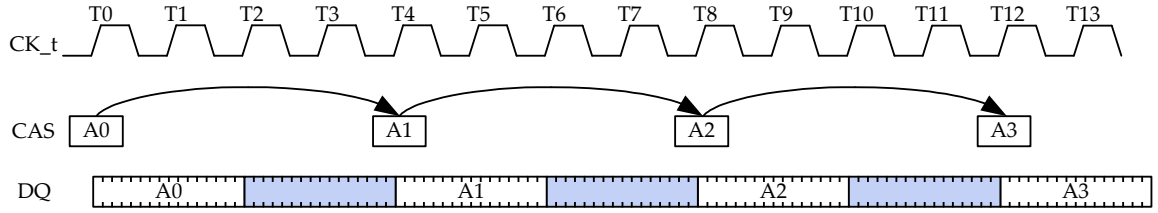
NOTE 1 Parameters t_{RTPS} and t_{RTPL} apply only when READ and PRECHARGE go to the same bank; use t_{RTPS} when BG are disabled, and t_{RTPL} when BG are enabled.

3.5 BANK GROUPS (cont'd)

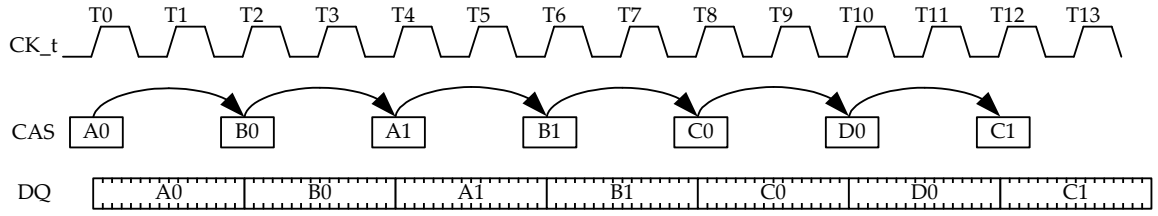
Example 1 (Bank Groups Disabled): t_{CCDS} = 2 t_{CK}



Example 2 (Bank Groups Enabled): t_{CCDL} = 4 t_{CK}



Example 3 (Bank Groups Enabled): t_{CCDS} = 2 t_{CK}



NOTE 1 Column accesses are to open banks, and t_{RCD} has been met.
NOTE 2 RLmrs = 0 assumed.
NOTE 3 Ax, Bx, C, Dx: accesses to bank groups A, B, C and D, respectively.
NOTE 4 With bank groups enabled, t_{CCDL} is 3 * t_{CK} or 4 * t_{CK} as programmed in MR3.

Figure 6 — t_{CCDS} and t_{CCDL} Timings

3.6 ADDRESS BUS INVERSION (ABI)

Address Bus Inversion (ABI) reduces the power requirements on address pins, as the number of address lines driving a low level can be limited to 5.

The ABI function is associated with the electrical signalling on the address lines between a controller and the GDDR5X SGRAM regardless of whether the information conveyed on the address lines is a row or column address, a mode register op-code, a write data mask, or any other pattern.

The ABI_n input is an active Low double data rate (DDR) signal and sampled by the GDDR5X SGRAM at the rising edge of CK_t and the rising edge of CK_c along with the address inputs.

Once enabled by the corresponding ABI mode register bit, the device inverts the pattern received on the address inputs in case ABI_n is sampled Low, or leaves the pattern non-inverted in case ABI_n is sampled High, as shown in Figure 7.

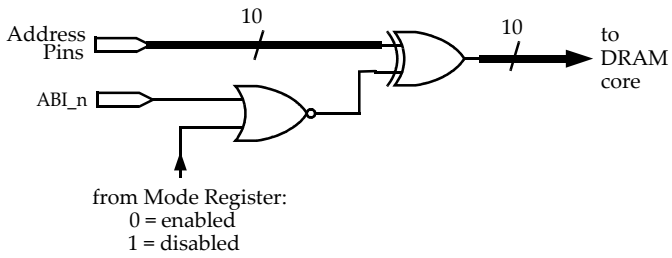


Figure 7 — Example of Address Bus Inversion Logic

The flow diagram in Figure 8 illustrates the ABI operation. The controller decides whether to invert or not invert the data conveyed on the address lines. The GDDR5X SGRAM has to perform the reverse operation based on the level of the ABI_n pin. Address input timing parameters are only valid with ABI being enabled and a maximum of 5 address inputs driven Low.

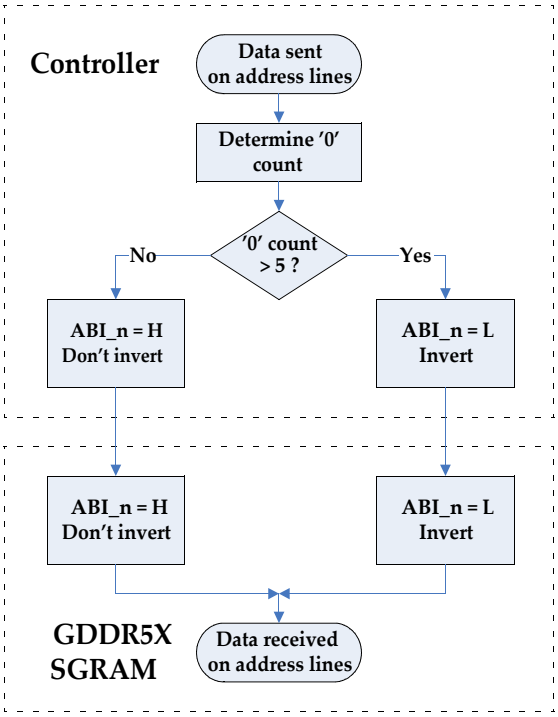


Figure 8 — Address Bus Inversion (ABI) Flow Diagram

3.7 READ and WRITE DATA BUS INVERSION (DBI)

The Data Bus Inversion (DBIdc) reduces the DC power consumption and supply noise-induced jitter on data pins because the number of DQ lines driving a low level can be limited to 4 within a byte. DBIdc is evaluated per byte.

There is one DBI_n pin per byte: DBI0_n is associated with DQ0-DQ7, DBI1_n with DQ8-DQ15, DBI2_n with DQ16-DQ23 and DBI3_n with DQ24-DQ31.

The DBI_n pins are bidirectional active Low double data rate (DDR) signals. For writes, they are sampled by the device along with the DQ of the same byte; for reads, they are driven by the device along with the DQ of the same byte.

Once enabled by the corresponding RDBI mode register bit, the device inverts read data and sets DBI_n Low when the number of '0' data bits within a byte is greater than 4; otherwise the device does not invert the read data and sets DBI_n High, as shown in Figure 9.

Once enabled by the corresponding WDBI Mode Register bit, the device inverts write data received on the DQ inputs in case DBI_n is sampled Low, or leaves the data non-inverted in case DBI_n is sampled High, as shown in Figure 10.

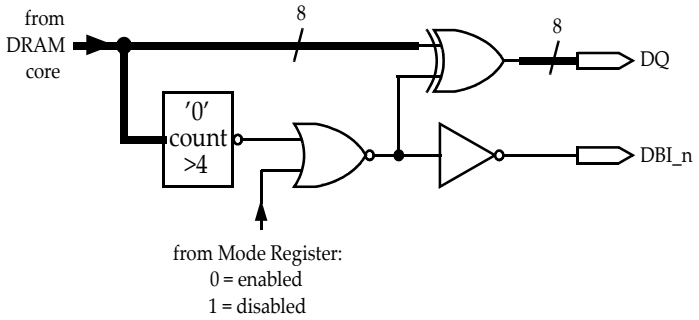


Figure 9 — Example of Data Bus Inversion Logic for READs

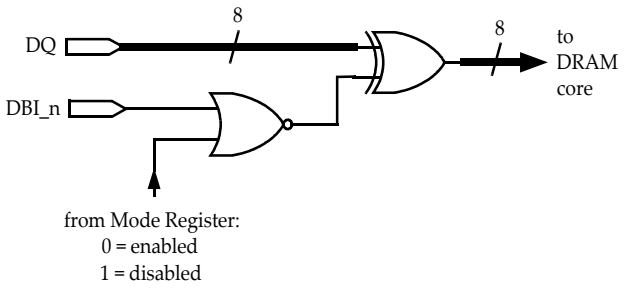


Figure 10 — Example of Data Bus Inversion Logic for WRITEs

The flow diagram in Figure 11 illustrates the DBIdc operation. In any case, the transmitter (the controller for writes, the GDDR5X SGRAM for reads) decides whether to invert or not invert the data conveyed on the DQs. The receiver (the GDDR5X SGRAM for writes, the controller for reads) has to perform the reverse operation based on the DBI_n pin level. Data input and output timing parameters are only valid with DBI being enabled and a maximum of 4 data lines per byte driven Low.

3.7 READ and WRITE DATA BUS INVERSION (DBI) (cont'd)

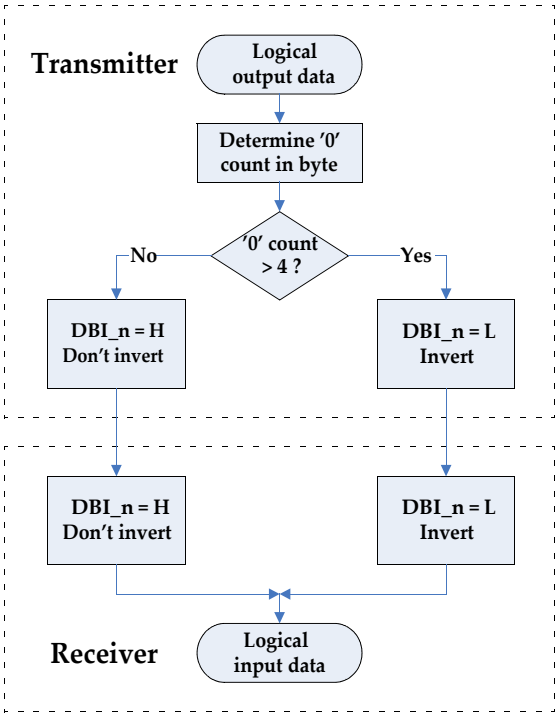


Figure 11 — DBI Flow Diagram

3.7.1 DBI_n Pin Special Function Overview

The DBI_n pin has special behavior compared to DQ pins because of the ability to enable and disable it via MRS. For either WRITE or READ DBI_n pin training, both READ DBI (RDBI) and WRITE DBI (WDBI) must be enabled. The behavior of the DBI_n pin in various mode register settings is summarized as follows:

- If both RDBI and WDBI are enabled, the pin drives DBI FIFO data with RDTR bursts, and the DBI FIFO accepts data from WRTR bursts.
- If only RDBI is enabled, the pin drives ODT except for READ or RDTR bursts.
- If only WDBI is enabled, the pin always drives ODT (unless in reset).
- If both RDBI and WDBI are disabled, the pin always drives ODT (unless in reset).

3.8 ERROR DETECTION CODE (EDC)

Error detection on the data bus is provided to improve system reliability. The device generates a checksum per byte lane for both READ and WRITE data and returns the checksum to the controller. Based on the checksum, the controller can decide if the data (or the returned CRC) was transmitted in error and retry the READ or WRITE command. The GDDR5X SGRAM itself does not perform any error correction. The algorithm detects 100% single bit errors and >99% double bit errors.

The features of the EDC are:

- 8 bit checksum on 144 bits (9 channels x 16 bit burst) in QDR mode, and 72 bits (9 channels x 8 bit burst) in DDR mode;
- dedicated EDC transfer pin per 9 channels;
- asymmetrical latencies on EDC transfer for reads and writes.

The CRC calculation is embedded into the write and read data stream as shown in Figure 46 "Data Paths used for Read and Write Training":

- for writes, the checksum is calculated on the DQ and DBI_n input data before decoding with DBI;
- for reads, the checksum is calculated on the DQ and DBI_n output data after encoding with DBI.

The CRC calculation is not affected by any data mask sent along with WDM, WDMA, WSM or WSMA commands. It is controlled separately for READ and WRITE bursts by the following bits in MR4:

- Bit A9 controls the CRC calculation for READ bursts, and bits A[8:7] hold the CRC read latency (CRCRL);
- Bit A10 controls the CRC calculation for WRITE bursts, and bits A[6:4] hold the CRC write latency (CRCWL)

The EDC latency is based on the RL and CRCRL latencies for read data, and the WL and CRCWL latencies for write data as shown in Table 6. The CRC bursts replace the EDC hold pattern for the duration of the bursts if CRC is enabled.

Table 6 — EDC Latencies

DESCRIPTION	SYMBOL	VALUE	UNITS
EDC READ Latency	EDCRL	RL + CRCRL	t_{CK}
EDC WRITE Latency	EDCWL	WL + CRCWL	t_{CK}

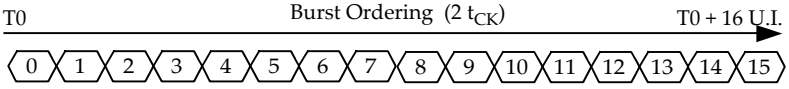
The GDDR5X SGRAM uses a 2-stage algorithm in the CRC calculation on a byte lane basis:

- Step 1: two-input XOR gates compress the first eight bits (D0 - D7) and the second eight bits (D8 - D15) of a 16-bit data burst into an 8-bit data word as shown in Figure 12. The inputs of the 2-input XOR have been carefully chosen to minimize the probability of undetectable double bit errors:
  - a temporal decorrelation combines UI that are latched by different internal WCK clock phases;
  - a spatial decorrelation combines UI from different bit lanes.
  In DDR mode this step 1 is effectively bypassed by forcing the second eight bits of the 16-bit data burst to 0.
- Step 2: the ATM-8 HEC, X^8+X^2+X^1+1, CRC polynomial calculates an 8-bit checksum as shown in Figure 13. The starting seed value is set to 0 in hardware. The bit order is optimized for errors in the time burst direction. All 1s are assumed in the calculation for the DBI_n pin when DBI is disabled for writes or reads in the mode register.

A typical combinatorial logic block implementation of the CRC algorithm consists of 72 parallel two-input XOR gates for step 1 followed by 272 two-input XOR gates in eight 6 XOR gate deep trees for step 2, resulting in a total XOR gate logic depth of 7.

3.8 ERROR DETECTION CODE (EDC) (cont'd)

CRC Input Data
(8 DQ + DBI_n)



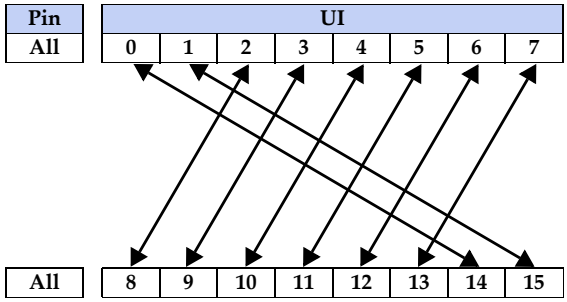
Input Data Bit Numbering

Pin	Burst 16															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
DQ0	0	1	2	3	4	5	6	7	72	73	74	75	76	77	78	79
DQ1	8	9	10	11	12	13	14	15	80	81	82	83	84	85	86	87
DQ2	16	17	18	19	20	21	22	23	88	89	90	91	92	93	94	95
DQ3	24	25	26	27	28	29	30	31	96	97	98	99	100	101	102	103
DQ4	32	33	34	35	36	37	38	39	104	105	106	107	108	109	110	111
DQ5	40	41	42	43	44	45	46	47	112	113	114	115	116	117	118	119
DQ6	48	49	50	51	52	53	54	55	120	121	122	123	124	125	126	127
DQ7	56	57	58	59	60	61	62	63	128	129	130	131	132	133	134	135
DBI0_n	64	65	66	67	68	69	70	71	136	137	138	139	140	141	142	143

Part A: Spatial decorrelation scheme

PIN	UI	UI
DQ0	0 ... 7	8 ... 15
DQ1	0 ... 7	8 ... 15
DQ2	0 ... 7	8 ... 15
DQ3	0 ... 7	8 ... 15
DBI0_n	0 ... 7	8 ... 15
DQ4	0 ... 7	8 ... 15
DQ5	0 ... 7	8 ... 15
DQ6	0 ... 7	8 ... 15
DQ7	0 ... 7	8 ... 15

Part B: Temporal decorrelation scheme



Step 1 Intermediate Result
(8 DQ + DBI_n)

Pin	Intermediate Result (Burst 8)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ0	0 ^ 142	1 ^ 143	2 ^ 136	3 ^ 137	4 ^ 138	5 ^ 139	6 ^ 140	7 ^ 141
DQ1	8 ^ 110	9 ^ 111	10 ^ 104	11 ^ 105	12 ^ 106	13 ^ 107	14 ^ 108	15 ^ 109
DQ2	16 ^ 118	17 ^ 119	18 ^ 112	19 ^ 113	20 ^ 114	21 ^ 115	22 ^ 116	23 ^ 117
DQ3	24 ^ 126	25 ^ 127	26 ^ 120	27 ^ 121	28 ^ 122	29 ^ 123	30 ^ 124	31 ^ 125
DQ4	32 ^ 78	33 ^ 79	34 ^ 72	35 ^ 73	36 ^ 74	37 ^ 75	38 ^ 76	39 ^ 77
DQ5	40 ^ 86	41 ^ 87	42 ^ 80	43 ^ 81	44 ^ 82	45 ^ 83	46 ^ 84	47 ^ 85
DQ6	48 ^ 94	49 ^ 95	50 ^ 88	51 ^ 89	52 ^ 90	53 ^ 91	54 ^ 92	55 ^ 93
DQ7	56 ^ 102	57 ^ 103	58 ^ 96	59 ^ 97	60 ^ 98	61 ^ 99	62 ^ 100	63 ^ 101
DBI0_n	64 ^ 134	65 ^ 135	66 ^ 128	67 ^ 129	68 ^ 130	69 ^ 131	70 ^ 132	71 ^ 133

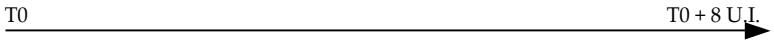
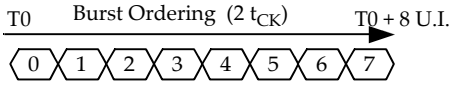


Figure 12 — EDC Calculation Matrix (Step 1)

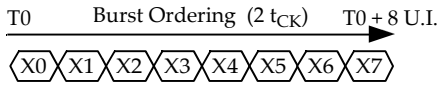
3.8 ERROR DETECTION CODE (EDC) (cont'd)

Step 1 Intermediate Result
(8 DQ + DBI_n)



Pin	0	1	2	3	4	5	6	7
DQ0	0	1	2	3	4	5	6	7
DQ1	8	9	10	11	12	13	14	15
DQ2	16	17	18	19	20	21	22	23
DQ3	24	25	26	27	28	29	30	31
DQ4	32	33	34	35	36	37	38	39
DQ5	40	41	42	43	44	45	46	47
DQ6	48	49	50	51	52	53	54	55
DQ7	56	57	58	59	60	61	62	63
DBI0_n	64	65	66	67	68	69	70	71

CRC Polynomial
$X^8 + X^2 + X + 1$



CRC Data Output Bit Ordering

Figure 13 — EDC Calculation Matrix (Step 2)

CRC Equations (Step 2)

```
CRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^ D[56] ^ D[54] ^
         D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[45] ^ D[43] ^ D[40] ^ D[39] ^
         D[35] ^ D[34] ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^
         D[16] ^ D[14] ^ D[12] ^ D[8]  ^ D[7]  ^ D[6]  ^ D[0];
CRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^ D[56] ^ D[55] ^
         D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^ D[44] ^ D[43] ^ D[41] ^ D[39] ^
         D[36] ^ D[34] ^ D[32] ^ D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^
         D[21] ^ D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^ D[12] ^
         D[9]  ^ D[6]  ^ D[1]  ^ D[0];
CRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^ D[58] ^ D[57] ^
         D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^ D[44] ^ D[43] ^ D[42] ^ D[39] ^
         D[37] ^ D[34] ^ D[33] ^ D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^
         D[15] ^ D[13] ^ D[12] ^ D[10] ^ D[8]  ^ D[6]  ^ D[2]  ^ D[1]  ^ D[0];
CRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^ D[58] ^ D[55] ^
         D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^ D[44] ^ D[43] ^ D[40] ^ D[38] ^
         D[35] ^ D[34] ^ D[30] ^ D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^
         D[14] ^ D[13] ^ D[11] ^ D[9]  ^ D[7]  ^ D[3]  ^ D[2]  ^ D[1];
CRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^ D[59] ^ D[56] ^
         D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^ D[45] ^ D[44] ^ D[41] ^ D[39] ^
         D[36] ^ D[35] ^ D[31] ^ D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^
         D[15] ^ D[14] ^ D[12] ^ D[10] ^ D[8]  ^ D[4]  ^ D[3]  ^ D[2];
CRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^ D[53] ^
         D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^ D[45] ^ D[42] ^ D[40] ^ D[37] ^
         D[36] ^ D[32] ^ D[31] ^ D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^
         D[15] ^ D[13] ^ D[11] ^ D[9]  ^ D[5]  ^ D[4]  ^ D[3];
CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^ D[54] ^ D[52] ^
         D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^ D[43] ^ D[41] ^ D[38] ^ D[37] ^
         D[33] ^ D[32] ^ D[29] ^ D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^
         D[14] ^ D[12] ^ D[10] ^ D[6]  ^ D[5]  ^ D[4];
CRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^ D[55] ^ D[53] ^
         D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[44] ^ D[42] ^ D[39] ^ D[38] ^
         D[34] ^ D[33] ^ D[30] ^ D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^
         D[15] ^ D[13] ^ D[11] ^ D[7]  ^ D[6]  ^ D[5];
```

3.8 ERROR DETECTION CODE (EDC) (cont'd)

3.8.1 EDC Pin Special Function Overview

The EDC pin is used for many different functions. The behavior of the EDC pin in various modes is summarized in Table 7.

Table 7 — EDC Pin Behavior

DEVICE STATUS	CONDITION	EDC[3:0] PIN STATUS
Device power-up	RESET_n = Low	High-Z
	RESET_n = High; no WCK clocks	High
	RESET_n = High; stable WCK clocks	EDC hold pattern (default = 1111)
Address training	ADT on (MR15 A10 = 1)	A14/A15 address inputs
WCK2CK training	WCK is sampled High	High
	WCK is sampled Low	Low
Idle	EDC13 INV off (MR4 A11 = 0)	EDC hold pattern
	EDC13 INV on (MR4 A11 = 1)	EDC0, EDC2: EDC hold pattern EDC1, EDC3: inverted EDC hold pattern
WRITE burst	WRCRC on (MR4 A10 = 0)	CRC data
	WRCRC off (MR4 A10 = 1)	EDC hold pattern
READ or RDTR burst	RDCRC on (MR4 A9 = 0)	CRC data
	RDCRC off (MR4 A9 = 1)	EDC hold pattern
LDFF	WRCRC + RDCRC both on or both off	EDC hold pattern
WRTR burst	-	EDC hold pattern
Power-down	WCK enabled (MR5 A1 = 0)	EDC hold pattern
	WCK disabled (MR5 A1 = 1)	High
Self refresh	-	High
READ burst in RDQS mode	RDQS mode on (MR3 A5 = 1)	Fixed 1010 strobe pattern (DDR mode only)
Vendor ID mode	WCK is stable	EDC hold pattern
All except reset	EDC High-Z on (MR8 A2 = 1)	High-Z
	VREFD Monitor on (MR8 A7 = 1)	internal V_{REFD} voltage level

3.9 VREFC and VREFD

The GDDR5X SGRAM offers multiple options for the reference voltages for address/command (V_{REFC}) and data inputs (V_{REFD}).

3.9.1 Reference Voltage for Address/Command Inputs (V_{REFC})

The reference voltage for the address/command inputs (V_{REFC}) can be supplied via the external VREFC pin or be generated internally as illustrated in Figure 14. The selection is made with the rising edge of RESET_n: the device selects internal V_{REFC} with a default level of 0.7 x V_{DDQ} when the VREFC pin is pulled Low in the system; otherwise external V_{REFC} is selected.

Half VREFC mode enables the V_{REFC} level to be adjusted when the ADD/CMD inputs operate without termination. When bit A6 in MR7 is set to 1, a level of nominally 0.5 x V_{DDQ} is generated. The maximum operating frequency for this mode is defined by $f_{CKVREFC2}$. A Half V_{REFC} mode reference voltage change requires t_{VREFC2} to settle.

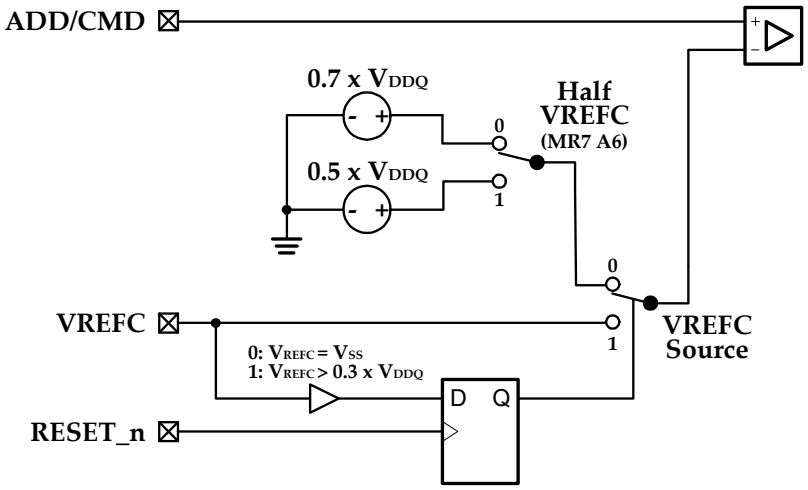


Figure 14 — VREFC Options

3.9.2 Reference Voltage for Data Inputs (V_{REFD})

The reference voltage for the DQ and DBI_n inputs (V_{REFD}) is generated internally, and separate V_{REF} circuits are associated with each data byte.

The V_{REFD} level is linear with a nominal step size of 1/210 x V_{DDQ} in a range from 0.55 x V_{DDQ} to 0.85 x V_{DDQ} as illustrated in Figure 16 and Table 8, and must be set by programming bits A[11:0] in MR6 and bits A[11:0] in MR9 as shown in Table 10. The V_{REFD} settling time t_{VREFD} is a constant value for the device, and is referenced from the MRS command to when the 90% level of the delta between old and new V_{REFD} voltage has been reached as illustrated in Figure 17.

Half VREFD mode enables the V_{REFD} level to be adjusted when the DQ and DBI_n inputs operate without termination. When bit A7 in MR7 is set to 1, a level of nominally 0.5 x V_{DDQ} is generated. The maximum operating frequency for this mode is defined by $f_{CKVREFD2}$. A Half VREFD mode reference voltage change requires t_{VREFD2} to settle.

VREF C2D mode enables a backup solution for external VREFD. When bit A6 in MR8 is set to 1, an internal bridge is enabled that connects both V_{REFD} circuits with the V_{REFC} circuit and further with the external VREFC pin. VREF C2D mode requires that external V_{REFC} is selected at power-up.

3.9.2 Reference Voltage for Data Inputs (V_{REFD}) (cont'd)

VREFD Monitor mode allows the observation the internal V_{REFD} voltages at the EDC pins of both double bytes. The mode is controlled by bit A7 in MR8. The settling time is longer than t_{MRD} and depends on the external capacitve load at the EDC pins.

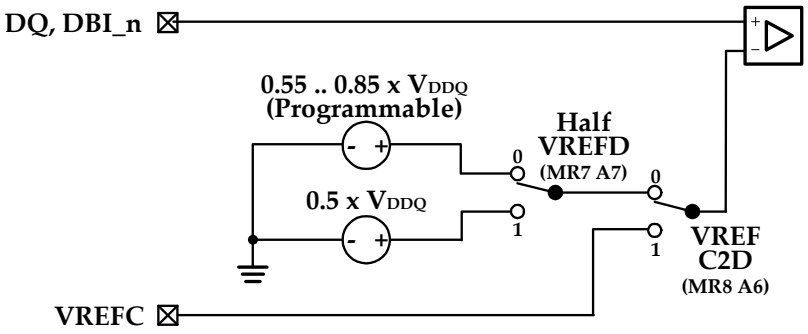


Figure 15 — VREFD Options

Table 8 — VREFD Level

VREFD Level Code		VREFD Level		
MR6 A[11:6] / MR9 A[11:6] MR6 A[5:0] / MR9 A[5:0]	Decimal	% V_{DDQ}	Divider	V_{REFD} [V]
1 1 1 1 1 1	63	0.852	179 /2 10	1.151
1 1 1 1 1 0	62	0.848	178 / 210	1.144
1 1 1 1 0 1	61	0.843	177 / 210	1.138
...				
1 0 0 0 0 1	33	0.710	149 / 210	0.958
1 0 0 0 0 0	32	0.705	148 / 210	0.951
0 1 1 1 1 1	31	**0.700**	147 / 210	0.945
0 1 1 1 1 0	30	0.695	146 / 210	0.939
0 1 1 1 0 1	29	0.690	145 / 210	0.932
...				
0 0 0 0 1 0	2	0.562	118 / 210	0.759
0 0 0 0 0 1	1	0.557	117 / 210	0.752
0 0 0 0 0 0	0	0.552	116 / 210	0.746

3.9.2 Reference Voltage for Data Inputs (V_{REFD}) (cont'd)

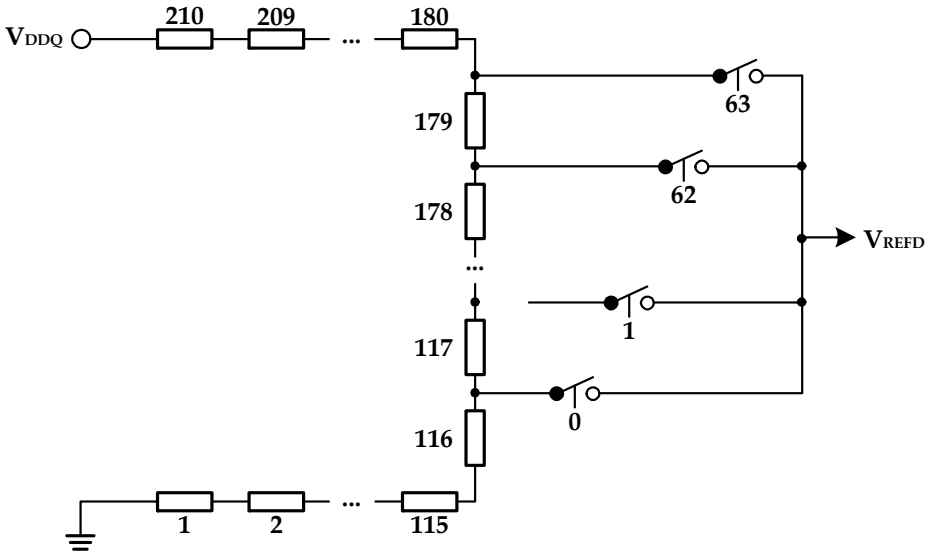


Figure 16 — VREFD Circuit

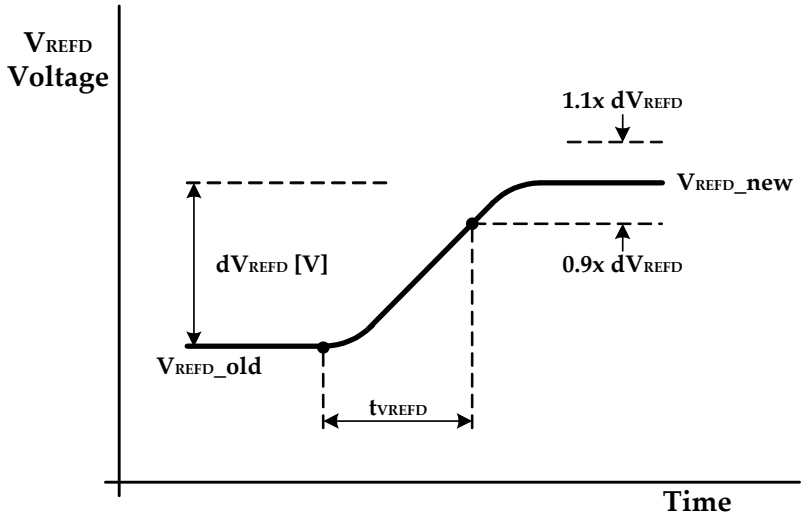


Figure 17 — VREFD Settling Time

3.10 TEMPERATURE SENSOR

GDDR5X SGRAMs incorporate a temperature sensor with digital temperature readout function. This function allows the controller to monitor the device's junction temperature and use this information to make sure the device is operated within the specified temperature range or to adjust interface timings relative to temperature changes over time.

The temperature sensor is permanently enabled.

The temperature readout uses the DRAM Info mode feature. The digital value is driven asynchronously on DQ[7:0] following the MRS command to MR3 that sets bit A7 to 1 and bit A6 to 0. The temperature readout is continuously driven until an MRS command sets both bits to 0.

The device's junction temperature is linearly encoded as shown in Table 9 and Figure 18. The sensor's accuracy is vendor specific.

Table 9 — Temperature Sensor Readout Pattern

TEMPERATURE [°C]	DECIMAL TEMPERATURE READOUT	BINARY TEMPERATURE READOUT DQ[7:0]
-40	0	0000 0000
...	...	...
0	20	0001 0100
2	21	0001 0101
4	22	0001 0110
6	23	0001 0111
8	24	0001 1000
...	...	...
120	80	0101 0000
>120	80	0101 0000

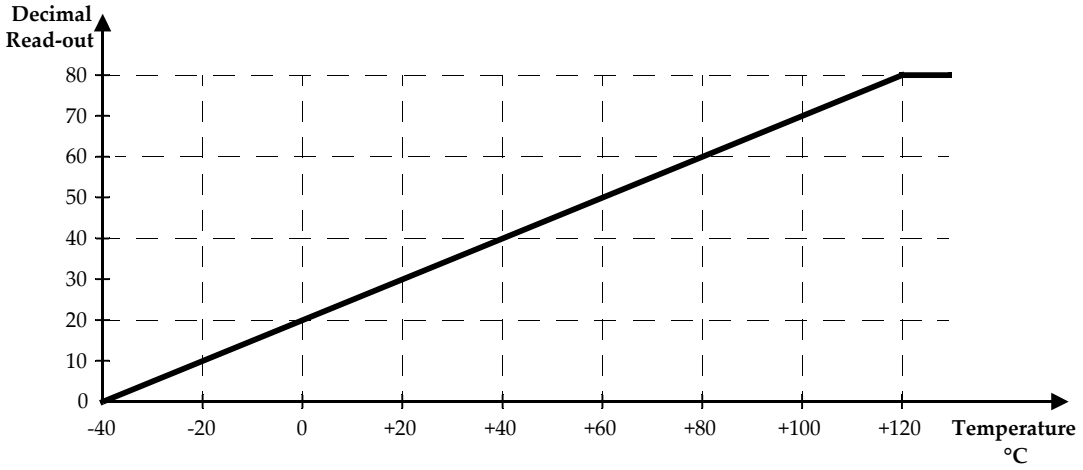


Figure 18 — Temperature Sensor Readout Characteristic

3.11 DUTY CYCLE CORRECTOR (DCC)

The use of the optional Duty Cycle Corrector (DCC) can correct for the static duty cycle error of the WCK clock, resulting in improved timing margins for Reads and Writes. It is recommended to enable the DCC prior to the phase search in WCK2CK training because any shift of rising and falling WCK edges can impact the WCK2CK training results.

DCC operation is controlled by MR7 bits A[11:10]. The duty cycle correction is started by setting bit A10. The DCC must be held in this state for a minimum duration of t_{DCC}. After t_{DCC} is met, bit A11 shall be set to terminate the duty cycle correction and hold the correction code. The DCC may be disabled at any time by resetting bits A11 and A10.

When in the hold state, the DCC remembers its correction code during power-down (with LP2 enabled) and self refresh. In this case the WCK2CK training time upon power-down exit or self refresh exit is not gated by t_{DCC}, as the correction code will be automatically restored. Alternatively, a new duty cycle correction cycle could be started by resetting bit A11.

A new duty cycle correction cycle is required upon a frequency change.

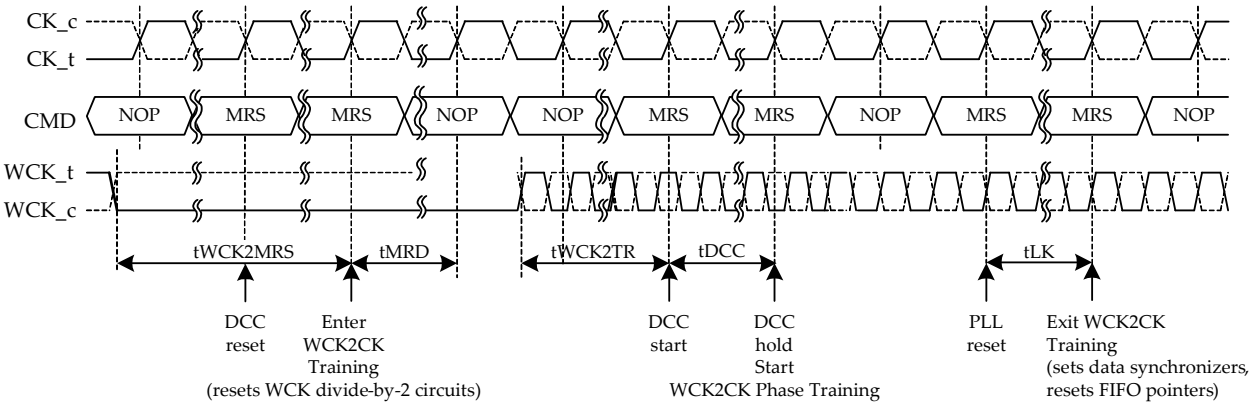


Figure 19 — WCK2CK Training Sequence with DCC

4 MODE REGISTERS

Sixteen mode registers define the specific mode of operation for the GDDR5X SGRAM. MR0 to MR9, MR11, and MR15 are defined as shown in Figure 20. MR10 is reserved for future use, and MR12 to MR14 are reserved for vendor specific features. Reprogramming the mode registers does not alter the contents of the memory array.

All mode registers are programmed via the MODE REGISTER SET (MRS) command and retain the stored information until they are reprogrammed, chip reset, or until the device loses power. Mode registers must be loaded when all banks are idle and no bursts are in progress; the controller must wait the specified time t_{MRD} before initiating any subsequent operations. Violating either of these requirements results in unspecified operation.

No default states are defined for mode registers except when otherwise noted. Users therefore must fully initialize all mode registers to the desired values upon power-up or after a subsequent chip reset.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0. Bits A[15:12] are not used to program the mode registers and not shown in subsequent register definitions.

If the user activates bits in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is not implemented).

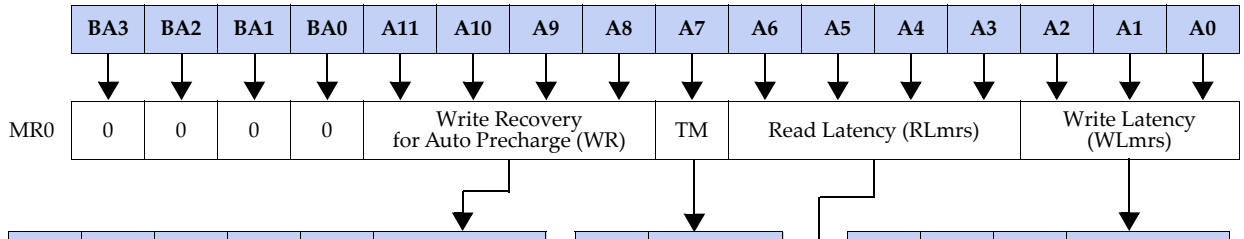
4 MODE REGISTERS (cont'd)

	BA3	BA2	BA1	BA0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MR0	0	0	0	0	Write Recovery for Auto Precharge (WR)				TM	Read Latency (RLmrs)				Write Latency (WLmrs)		
MR1	0	0	0	1	PLL Reset	ABI	WDBI	RDBI	PLL DLL	Cal Upd	ADD/CMD Termination		Data Termination		Driver Strength	
MR2	0	0	1	0	ADD/CMD/CK Termination Offset			Data and WCK Termination Offset			OCD Pull-up Driver Offset			OCD Pull-down Driver Offset		
MR3	0	0	1	1	Bank Groups		WCK Termination		Info		RDQS Mode	WCK 2CK	WCK 23Inv	WCK 01Inv	Self Refresh	
MR4	0	1	0	0	EDC13 INV	WR CRC	RD CRC	CRC Read Latency (CRCRL)		CRC Write Latency (CRCWL)			EDC Hold Pattern			
MR5	0	1	0	1	RAS						RFU	PLL/DLL Bandwidth (PLLBW)		LP3	LP2	LP1
MR6	0	1	1	0	VREFD Level Byte 0 (MF=0) / Byte 3 (MF=1)						VREFD Level Byte 2 (MF=0) / Byte 1 (MF=1)					
MR7	0	1	1	1	DCC		VDD Range		Half VREFD	Half VREFC	DQ PreA	Auto Sync	LF Mode	PLL DelC	PLL FLock	WCK PIN
MR8	1	0	0	0	CK Termination		Oper. Mode	Add Comp	VREFD Mon	VREF C2D	PLL/DLL Range		Hiber-nate	EDC Hi-Z	WR MSB	RL MSB
MR9	1	0	0	1	VREFD Level Byte 1 (MF=0) / Byte 2 (MF=1)						VREFD Level Byte 3 (MF=0) / Byte 0 (MF=1)					
MR10	1	0	1	0	Reserved											
MR11	1	0	1	1	PASR Row Segment Mask				PASR 2-Bank Mask							
MR12	1	1	0	0	Reserved for Vendor Specific Features											
MR13	1	1	0	1	Reserved for Vendor Specific Features											
MR14	1	1	1	0	Reserved for Vendor Specific Features											
MR15	1	1	1	1	RFU	ADT	MRE MF1	MRE MF0								

Figure 20 — Mode Registers Overview

4.1 MODE REGISTER 0 (MR0)

MR0 controls operating modes such as write latency, read latency, write recovery and test mode as shown in Figure 21. The register is programmed via the MRS command with BA[3:0] = 0000.



MR8 A1	A11	A10	A9	A8	Write Recovery (WR)
0	0	0	0	0	4 / optional
0	0	0	0	1	5 / optional
0	0	0	1	0	6 / optional
0	0	0	1	1	7 / optional
0	0	1	0	0	8 / optional
0	0	1	0	1	9 / optional
0	0	1	1	0	10 / optional
0	0	1	1	1	11 / optional
0	1	0	0	0	12 / optional
0	1	0	0	1	13 / optional
0	1	0	1	0	14 / optional
0	1	0	1	1	15 / optional
0	1	1	0	0	16 / optional
0	1	1	0	1	17 / optional
0	1	1	1	0	18 / optional
0	1	1	1	1	19 / optional
1	0	0	0	0	20 / optional
1	0	0	0	1	22 / optional
1	0	0	1	0	24 / optional
1	0	0	1	1	26 / optional
1	0	1	0	0	28 / optional
...					...
1	1	1	1	0	48 / optional
1	1	1	1	1	50 / optional

Please note that the MSB is located in MR8

A7	Test Mode
0	Normal
1	Test Mode

A2	A1	A0	Write Latency (WLmrs)
0	0	0	RFU
0	0	1	1 / optional
0	1	0	2 / optional
0	1	1	3 / optional
1	0	0	4 / optional
1	0	1	5 / optional
1	1	0	6 / optional
1	1	1	7 / optional

Please note that the MSB is located in MR8

MR8 A0	A6	A5	A4	A3	Read Latency (RLmrs)
0	0	0	0	0	5 / optional
0	0	0	0	1	6 / optional
0	0	0	1	0	7 / optional
0	0	0	1	1	8 / optional
0	0	1	0	0	9 / optional
0	0	1	0	1	10 / optional
0	0	1	1	0	11 / optional
0	0	1	1	1	12 / optional
0	1	0	0	0	13 / optional
0	1	0	0	1	14 / optional
0	1	0	1	0	15 / optional
0	1	0	1	1	16 / optional
0	1	1	0	0	17 / optional
0	1	1	0	1	18 / optional
0	1	1	1	0	19 / optional
0	1	1	1	1	20 / optional
1	0	0	0	0	21 / optional
1	0	0	0	1	22 / optional
...					...
1	1	1	1	0	35 / optional
1	1	1	1	1	36 / optional

Figure 21 — Mode Register 0 (MR0) Definition

4.1 MODE REGISTER 0 (MR0) (cont'd)

Write Latency (WLmrs)

The write latency (WLmrs) is the delay in clock cycles used in the calculation of the total write latency (WL) between the registration of a WRITE or WRTR command and the availability of the first piece of input data.

WLmrs is specified by bits A[2:0], defining a WLmrs range of 1 to 7 t_{CK}. All WLmrs values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported WLmrs values; the supported WLmrs range must be contiguous. The full write latency definition can be found in the clause entitled OPERATION.

When the write latency is set to small values (i.e., 1,2,... clocks), the input receivers turn off in bank idle and power-down states only, in turn, raising the average operating power. When the write latency is set to higher values (i.e., .. 6, 7 clocks) the input receivers turn on when the WRITE or WRTR command is registered. Refer to vendor datasheets for value(s) of WLmrs where the input receivers only turn on when the WRITE or WRTR command is registered.

Read Latency (RLmrs)

The read latency (RLmrs) is the delay in clock cycles used in the calculation of the total read latency (RL) between the registration of a READ or RDTR command and the availability of the first piece of output data.

RLmrs is specified by bits MR8 A0 and A[6:3], defining a RLmrs range of 5 to 36 t_{CK}. Please note that the MSB is located in MR8; a read latency change therefore may require two MRS commands. All RLmrs values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported RLmrs values; the supported RLmrs range must be contiguous. The full read latency definition can be found in the clause entitled OPERATION.

Write Recovery for Auto Precharge (WR)

The programmed WR value is used for the auto precharge feature along with t_{RP} to determine t_{DAL}.

WR must be programmed with a value greater than or equal to RU{t_{WR}/t_{CK}}, where RU stands for round up, t_{WR} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time.

WR is specified by bits MR8 A1 and A[11:8], with 1 t_{CK} increments for lower WR values and 2 t_{CK} increments for higher WR values, defining a total WR range of 4 to 50 t_{CK}. Please note that the MSB is located in MR8; a WR change therefore may require two MRS commands.

All WR values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported WR values; the supported WR range must be contiguous.

Test Mode

The normal operating mode is selected by issuing an MRS command with bit A7 set to 0, and bits A[11:8] and A[6:0] set to the desired values. Programming bit A7 to 1 places the device into a test mode that is only to be used by the DRAM manufacturer. No functional operation is specified with test mode enabled.

4.2 MODE REGISTER 1 (MR1)

MR1 controls functions like driver strength, data termination, address/command termination, Read DBI, Write DBI, ABI, control of calibration updates and PLL/DLL as shown in Figure 22. The register is programmed via the MRS command with BA[3:0] = 0001. Bits A10, A[6:4] and A[1:0] of this register are initialized with 0.

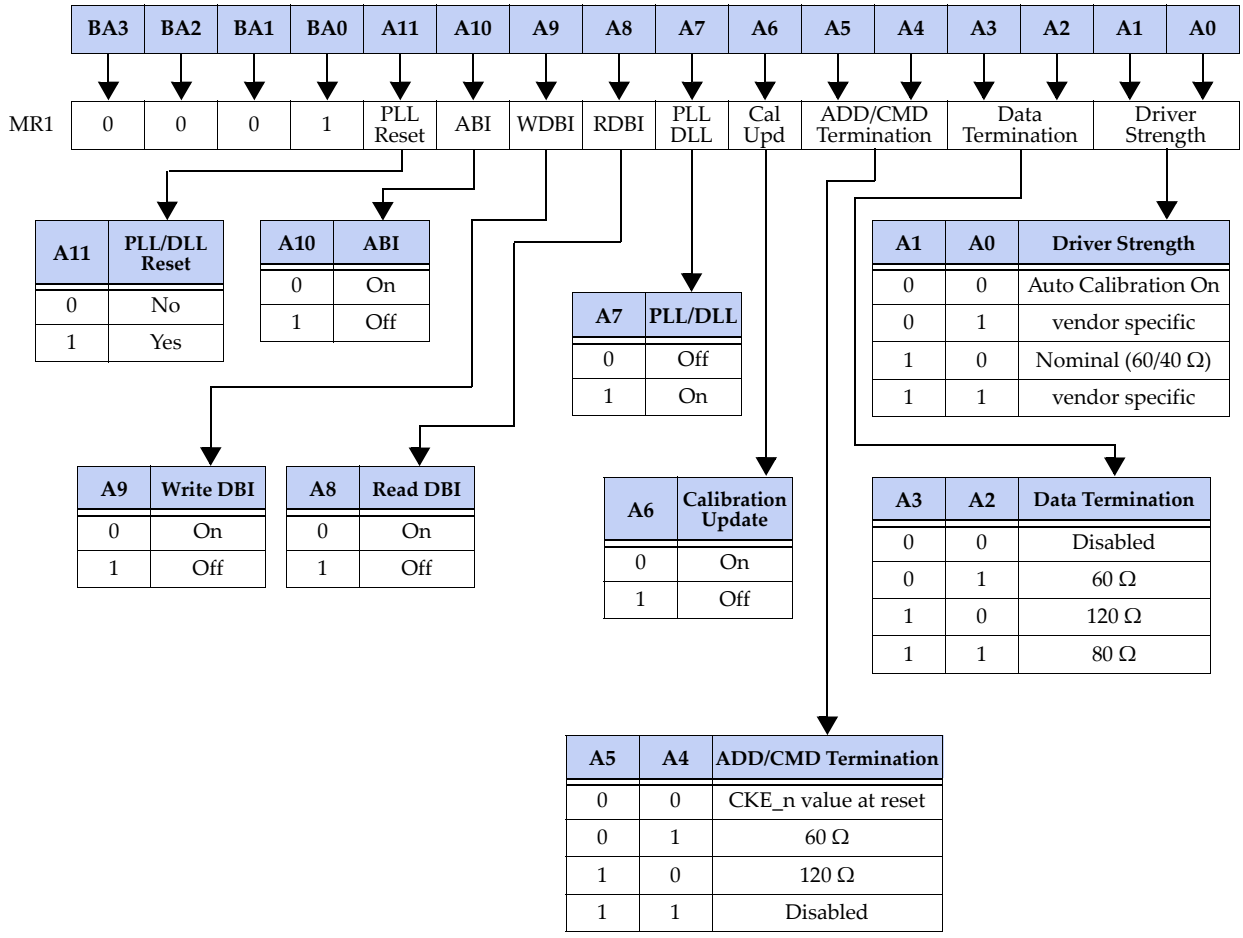


Figure 22 — Mode Register 1 (MR1) Definition

Impedance Autocalibration of Output Buffer and Active Terminator

GDDR5X SGRAMs offer auto calibrating output buffers and on-die terminations (ODT) which enable driver impedance and terminations to be matched to the system within a given range. To adjust the impedance, an external precision resistor is connected between the ZQ pin and V_{SSQ}. A nominal resistor value of 120 Ω is equivalent to the 40 Ω pull-down and 60 Ω pull-up nominal impedances of the device. RESET_n is not internally terminated.

The output driver and on-die termination impedances are updated during all REFRESH (REFAB) commands to compensate for variations in supply voltage and temperature. The impedance updates are transparent to the system.

4.2. MODE REGISTER 1 (MR1) (cont'd)

Driver Strength

Bits A[1:0] define the driver strength. The auto calibration setting enables the auto calibration functionality for the pull-down, pull-up and termination over process, temperature and voltage changes.

The design target for the factory setting is 40 Ω pull-down, 60 Ω pull-up driver strength with nominal process, voltage and temperature conditions. The nominal option enables the factory setting for the pull-down, pull-up driver strength and termination. With this option enabled, driver strength and termination are expected to change with process, voltage and temperature. AC timings are only guaranteed with auto calibration enabled.

Data Termination

Bits A[3:2] define the data termination value for the DQ and DBI_n pins in combination with the driver strength setting. Data termination is disabled by default; it can be set to a value of 60 Ω, 80 Ω or 120 Ω depending on system conditions. Data termination may also be turned off.

ADD/CMD Termination

Bits A[5:4] define the address/command termination. The default setting (00) provides that the address/command termination is determined by latching CKE_n on the rising edge of RESET_n. The address/command termination can also be set to a value of 60 Ω which is intended for a single loaded system, or 120 Ω which is intended for clamshell configurations with two devices sharing a common address/command bus. The address/command termination may also be turned off.

Calibration Update

The calibration update setting enables the calibration value to be updated automatically by the auto calibration engine. The function is enabled by default to reduce update induced jitter. The user may decide to suppress updates from the auto calibration engine by disabling calibration update.

The calibration updates can occur with any REFRESH (REFAB) command. The update is not complete for a time t_{KO} after the REFRESH command is latched. During this t_{KO} time, only NOP commands may be issued.

PLL/DLL and PLL/DLL Reset

The use of a PLL or DLL is mandatory in QDR mode and optional in DDR mode. If PLL/DLL-on operation is desired, the PLL/DLL must be enabled by setting bit A7 to 1.

A PLL/DLL reset is done by turning the PLL/DLL off and then on, or by use of the PLL/DLL reset bit A11. The PLL/DLL reset bit is self clearing, meaning that it returns to 0 after the PLL/DLL reset function has been initiated.

RDBI and WDBI

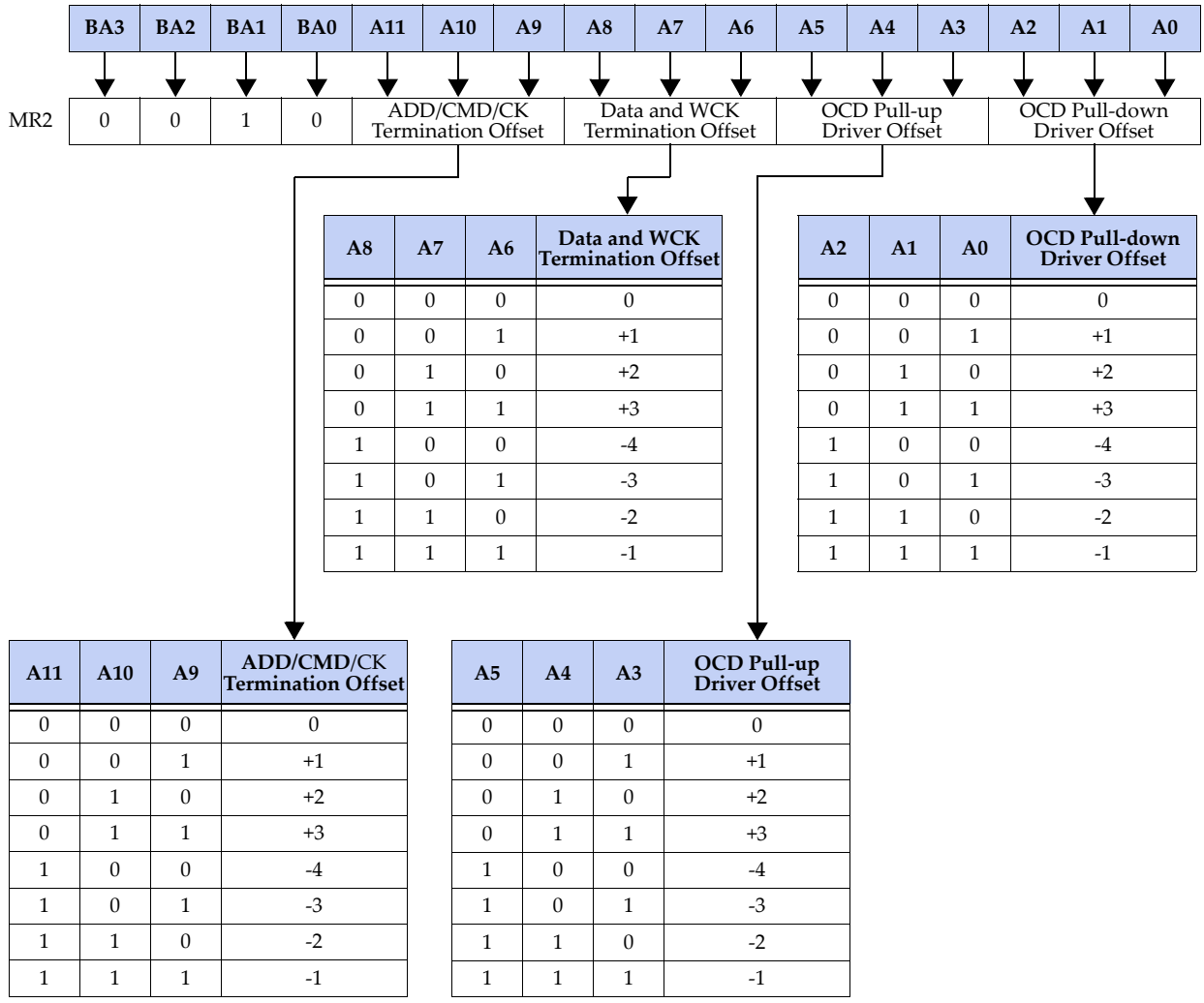
Bit A8 controls the read data bus inversion (RDBI), and bit A9 controls the write data bus inversion (WDBI). See the Data Bus Inversion (DBI) clause for more details.

ABI

Bit A10 controls the address bus inversion (ABI). ABI is enabled by default. See the Address Bus Inversion (ABI) clause for more details.

4.3 MODE REGISTER 2 (MR2)

MR2 defines the output driver (OCD) and termination (ODT) offsets as shown in Figure 23. The register is programmed via the MRS command with BA[3:0] = 0010.



A8	A7	A6	Data and WCK Termination Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A2	A1	A0	OCD Pull-down Driver Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A11	A10	A9	ADD/CMD/CK Termination Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A5	A4	A3	OCD Pull-up Driver Offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Figure 23 — Mode Register 2 (MR2) Definition

Impedance Offsets

The driver and termination impedances may be offset individually for pull-down driver, pull-up driver, DQ/DBI_n/WCK termination, and address/command/CK termination. The offset impedance step values may not be linear and vary across DRAM vendors and across PVT. With negative offset steps the driver strengths is decreased, and Ron and the termination value are increased. With positive offset steps the driver strengths is increased, and Ron and the termination value are decreased.

IV curves and AC timings are only guaranteed with zero offset.

4.3. MODE REGISTER 2 (MR2) (cont'd)

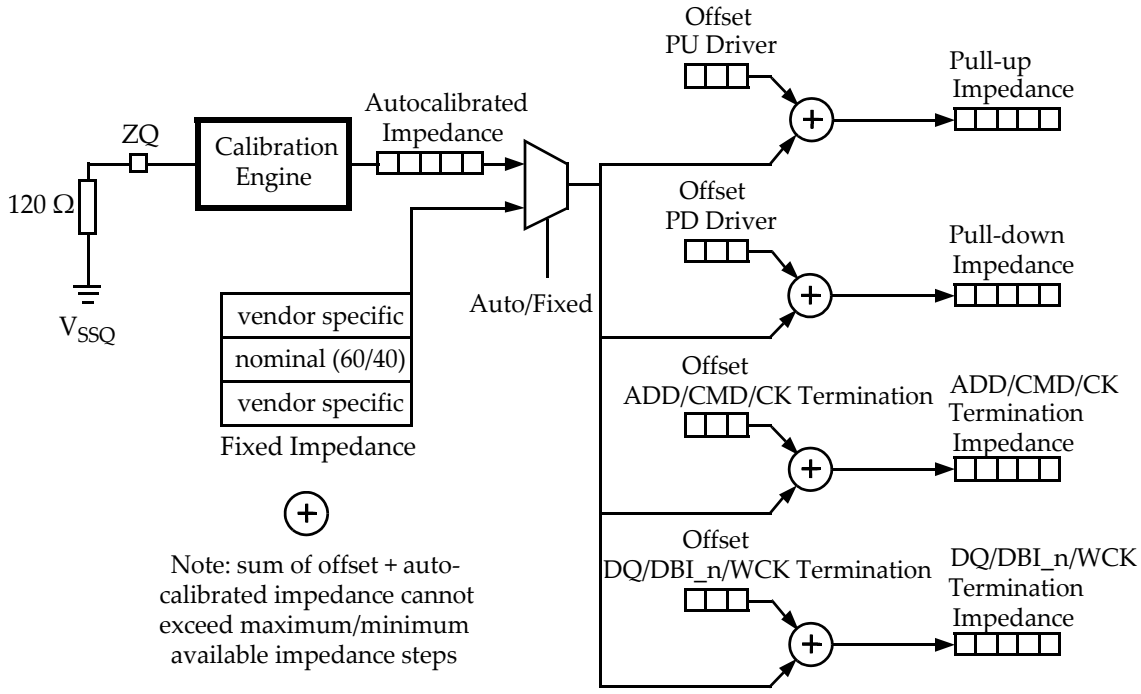


Figure 24 — Impedance Offsets

4.4 MODE REGISTER 3 (MR3)

MR3 controls functions like self refresh, WCK2CK training, RDQS mode, DRAM info, WCK termination and bank groups as shown in Figure 25. The register is programmed via the MRS command with BA[3:0] = 0011. Bits A[9:8] of this register are initialized with 0.

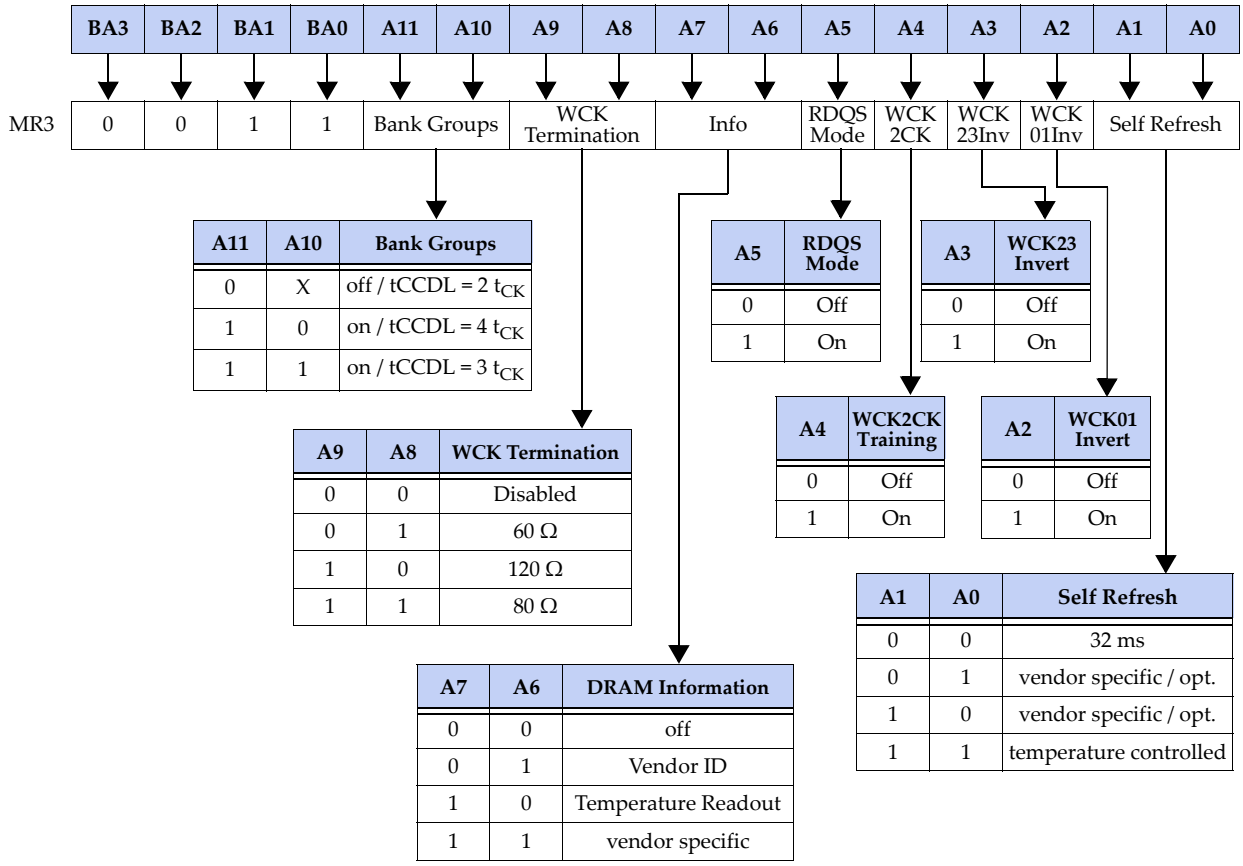


Figure 25 — Mode Register 3 (MR3) Definition

Self Refresh

The refresh interval in self refresh mode may be set to 32ms, or being controlled by an integrated temperature sensor. DRAM vendors may support additional settings related to other temperatures.

WCK01 / WCK23 Inversion

Bits A[3:2] control whether the internal phase should be flipped (inverted) after internally dividing the WCK01 and WCK23 clock inputs by 2, corresponding to a 4 UI phase shift in QDR mode and a 2 U.I. phase shift in DDR mode. The bits are used in conjunction with WCK2CK training mode.

WCK2CK

Bit A4 (WCK2CK) enables and disables the WCK2CK alignment training. For details on this training sequence, see the clause on TRAINING.

RDQS Mode

Bit A5 enables RDQS mode where the EDC pins act as a read strobe. CRC is not supported in RDQS mode, and all related bits in MR4 are ignored. See RDQS mode for more details.

4.4. MODE REGISTER 3 (MR3) (cont'd)

DRAM Information

Bits A[7:6] enable the DRAM information mode which outputs either the Vendor ID, the device's junction temperature or optionally other vendor specific device info. The Vendor ID identifies the manufacturer of the device, and provides the die revision and memory density.

WCK Termination

Bits A[9:8] define the (single-ended) termination for the WCK01_t, WCK01_c, WCK23_t and WCK23_c pins in combination with the driver strength setting. The termination is disabled by default; it can be set to a value of 60 Ω, 80 Ω or 120 Ω depending on system conditions. WCK termination may also be turned off.

Bank Groups

Bit A11 enables the bank groups feature, and bit A10 specifies the min column-to-column command delay t_{CCDL}. With A11 set to 1, back-to-back column accesses within a bank group have to be spaced by 3 or 4 clocks as defined by bit A10. With A11 set to 0, the bank groups feature is disabled and t_{CCDL} equals t_{CCDS}.

Parameter f_{CKBG} specifies the maximum CK clock frequency the device may be operated at with the bank groups feature disabled.

4.5 MODE REGISTER 4 (MR4)

MR4 defines the error detection code (EDC) features as shown in Figure 26. The register is programmed via the MRS command with BA[3:0] = 0100. Bits A[3:0] of this register are initialized with 1111.

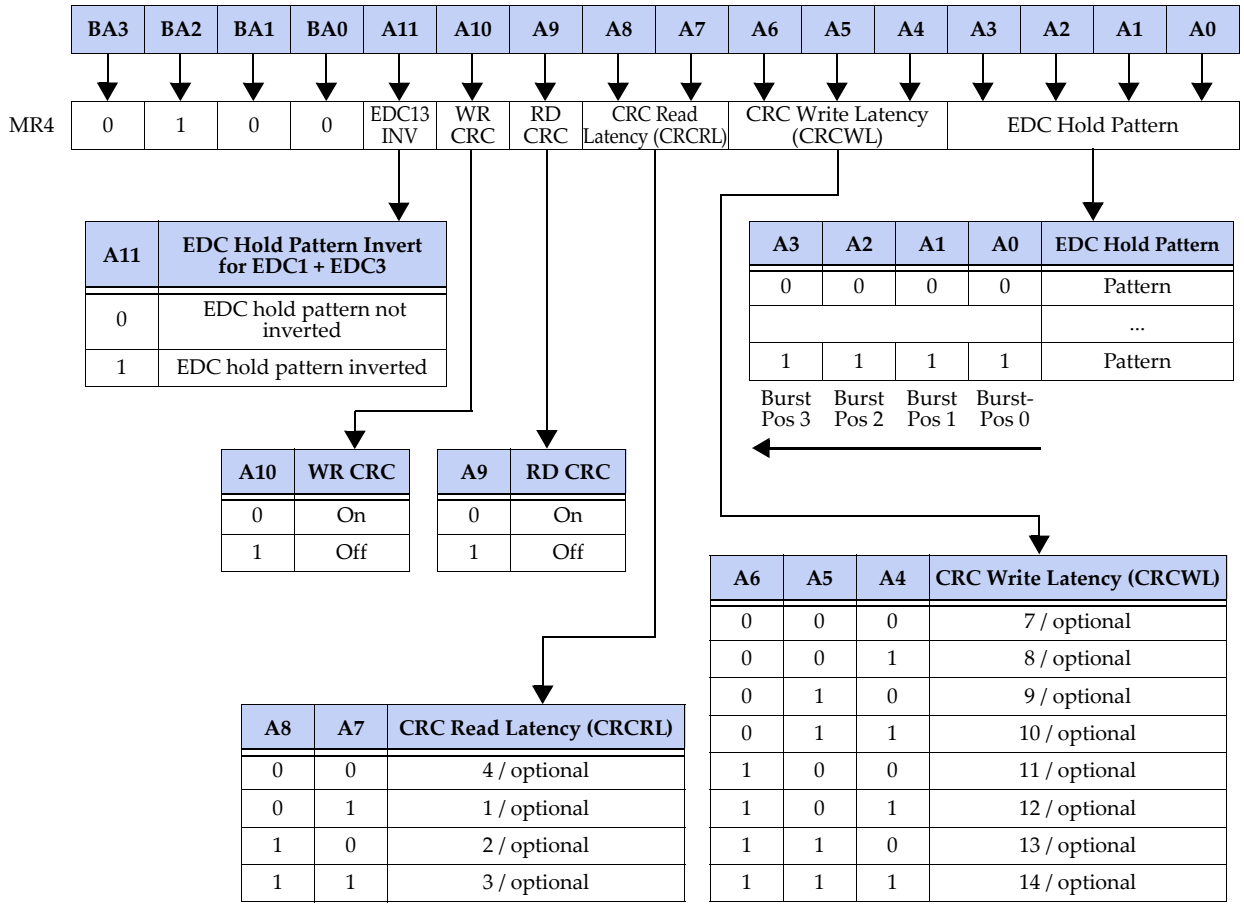


Figure 26 — Mode Register 4 (MR4) Definition

4.5. MODE REGISTER 4 (MR4) (cont'd)

EDC Hold pattern / EDC13 Invert

The 4-bit EDC hold pattern is considered a background pattern transmitted on the EDC pins. The register is initialized with 1111. The pattern is shifted from right to left and repeated with every clock cycle. The output timing is the same as of a READ burst.

CRC bursts calculated from writes or reads replace the EDC hold pattern for the duration of the bursts if CRC is enabled.

With each MRS command to MR4 that changes bits A[11:9] or A[3:0], the EDC hold pattern will be undefined for t_{MRD}.

The EDC hold pattern is not transmitted when the device is in address training mode, in WCK2CK training mode, RDQS mode, self refresh mode, reset state, in power-down state with the LP2 bit set, or when either EDC High-Z or VREFD Monitor mode are enabled.

With bit A11 set to 1, EDC1 and EDC3 transmit the inverted EDC hold pattern, resulting in a pseudo-differential pattern. Please note that this function is not available in x16 mode. Bit A11 is ignored for READ, WRITE and RDTR CRC bursts and the clock phase information in WCK2CK training mode.

Read CRC and CRC Read Latency (CRCRL)

Bit A9 controls the CRC calculation for READ bursts, and bits A[8:7] hold the CRC read latency. When enabled, the calculated CRC pattern is transmitted on the EDC pins after the CRC read latency. With Read CRC off, no CRC is calculated for READ bursts, and the EDC hold pattern is transmitted instead.

All CRCRL values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported CRCRL values; the supported CRCRL range must be contiguous.

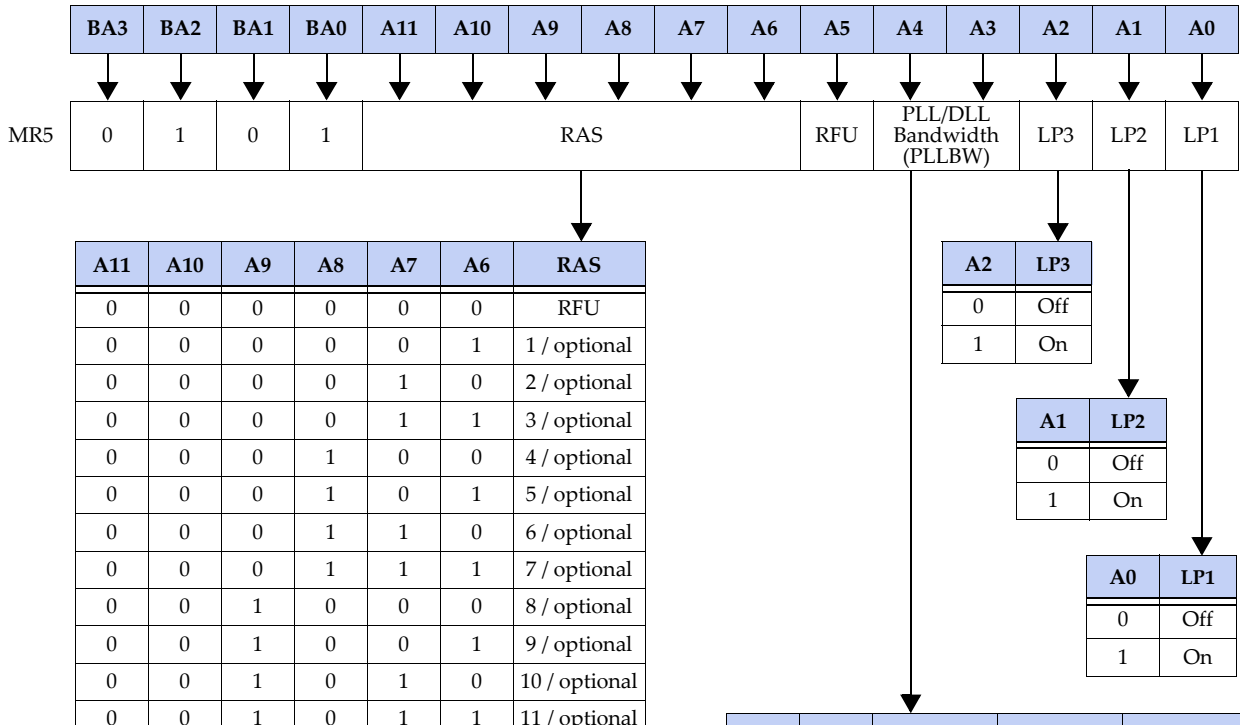
Write CRC and CRC Write Latency (CRCWL)

Bit A10 controls the CRC calculation for WRITE bursts, and bits A[6:4] hold the CRC write latency. When enabled, the calculated CRC pattern is transmitted on the EDC pins after the CRC write latency. With Write CRC off, no CRC is calculated for WRITE bursts, and the EDC hold pattern is transmitted instead.

All CRCWL values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported CRCWL values; the supported CRCWL range must be contiguous.

4.6 MODE REGISTER 5 (MR5)

MR5 defines low power modes, PLL/DLL bandwidth and digital RAS as shown in Figure 27. The register is programmed via the MRS command with BA[3:0] = 0101.



A11	A10	A9	A8	A7	A6	RAS
0	0	0	0	0	0	RFU
0	0	0	0	0	1	1 / optional
0	0	0	0	1	0	2 / optional
0	0	0	0	1	1	3 / optional
0	0	0	1	0	0	4 / optional
0	0	0	1	0	1	5 / optional
0	0	0	1	1	0	6 / optional
0	0	0	1	1	1	7 / optional
0	0	1	0	0	0	8 / optional
0	0	1	0	0	1	9 / optional
0	0	1	0	1	0	10 / optional
0	0	1	0	1	1	11 / optional
0	0	1	1	0	0	12 / optional
0	0	1	1	0	1	13 / optional
0	0	1	1	1	0	14 / optional
0	0	1	1	1	1	15 / optional
		...				...
1	1	1	1	1	1	63 / optional

A4	A3	-3dB [MHz] BW_{3dBLL}	Peak [MHz] BW_{PKLL}	Peak [dB] PK_{LL}
0	0	vendor specific		
0	1	optional		
1	0	optional		
1	1	optional		

Figure 27 — Mode Register 5 (MR5) Definition

Low Power Modes (LP1, LP2, LP3)

Bits A[2:0] control several low power modes of the device. The modes are independent of each other.

When bit A0 (LP1) is set, several core parameters are relaxed for lower power consumption of the device.

When bit A1 (LP2) is set, the WCK receivers may be turned off during power-down.

When bit A2 (LP3) is set, RDTR, WRTR and LDFF commands shall not be issued while a REFRESH command is being executed.

PLL/DLL Bandwidth

The PLL/DLL bandwidth may optionally be configured to match system characteristics. Each setting defines a unique combination of -3dB corner frequency, peaking frequency and peaking magnitude. All values and tolerances are vendor specific. The use of all settings except 000 is optional.

4.6. MODE REGISTER 5 (MR5) (cont'd)

RAS

RAS must be programmed with a value greater than or equal to RU{t_{RAS}/t_{CK}}, where RU stands for round up, t_{RAS} is the analog value from the vendor datasheet and t_{CK} is the operating clock cycle time. All RAS values are marked as "optional", allowing the DRAM vendor to define the minimum and maximum supported RAS values; the supported RAS range must be contiguous.

If the DRAM vendor does not support the mode register definition of t_{RAS} in clock cycles, the RAS mode register settings will be ignored.

4.7 MODE REGISTER 6 (MR6)

MR6 controls V_{REFD} levels for two of the two of the four data bytes as shown in Figure 28. The register is programmed via the MRS command with BA[3:0] = 0110.

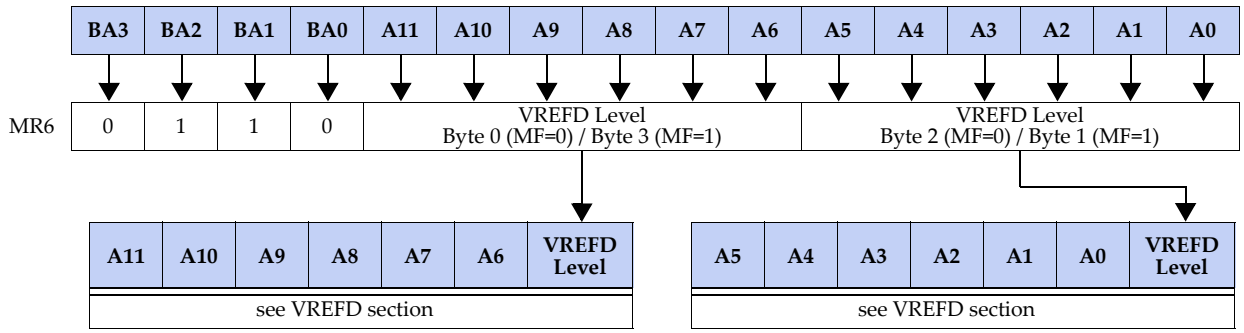


Figure 28 — Mode Register 6 (MR6) Definition

Input Reference Voltage for DQ and DBI_n Pins

Separate reference voltage circuits are associated with each data byte (see VREFD clause). Register bits in MR6 and MR9 (see MODE REGISTER 9 (MR9)) control the V_{REFD} level as summarized in Table 10; the bits are associated with the physical location of the data bytes (see BALLOUT). It is pointed out that in x16 (clamshell) mode it is required to use the Mode Register 0-14 Enable (MRE) bits in MR15 to selectively program the V_{REFD} levels either for the non-mirrored or the mirrored device.

Table 10 — V_{REFD} Level Control

Pin Group	Data Byte (MF=0)	Data Byte (MF=1)	Control Bits	Byte Active	
				x32 Mode	x16 Mode
Rows B to G, columns 3 + 4	Byte 0	Byte 3	MR6 A[11:6]	Yes	Yes
Rows B to G, columns 11 + 12	Byte 1	Byte 2	MR9 A[11:6]	Yes	No
Rows N to V, columns 11 + 12	Byte 2	Byte 1	MR6 A[5:0]	Yes	Yes
Rows N to V, columns 3 + 4	Byte 3	Byte 0	MR9 A[5:0]	Yes	No

4.8 MODE REGISTER 7 (MR7)

MR7 controls functions like the WCK alignment point, PLL fast lock, PLL delay compensation, low frequency mode, auto synchronization, DQ preamble, half VREFC, half VREFD, VDD range and DCC as shown in Figure 29. The register is programmed via the MRS command with BA[3:0] = 0111.

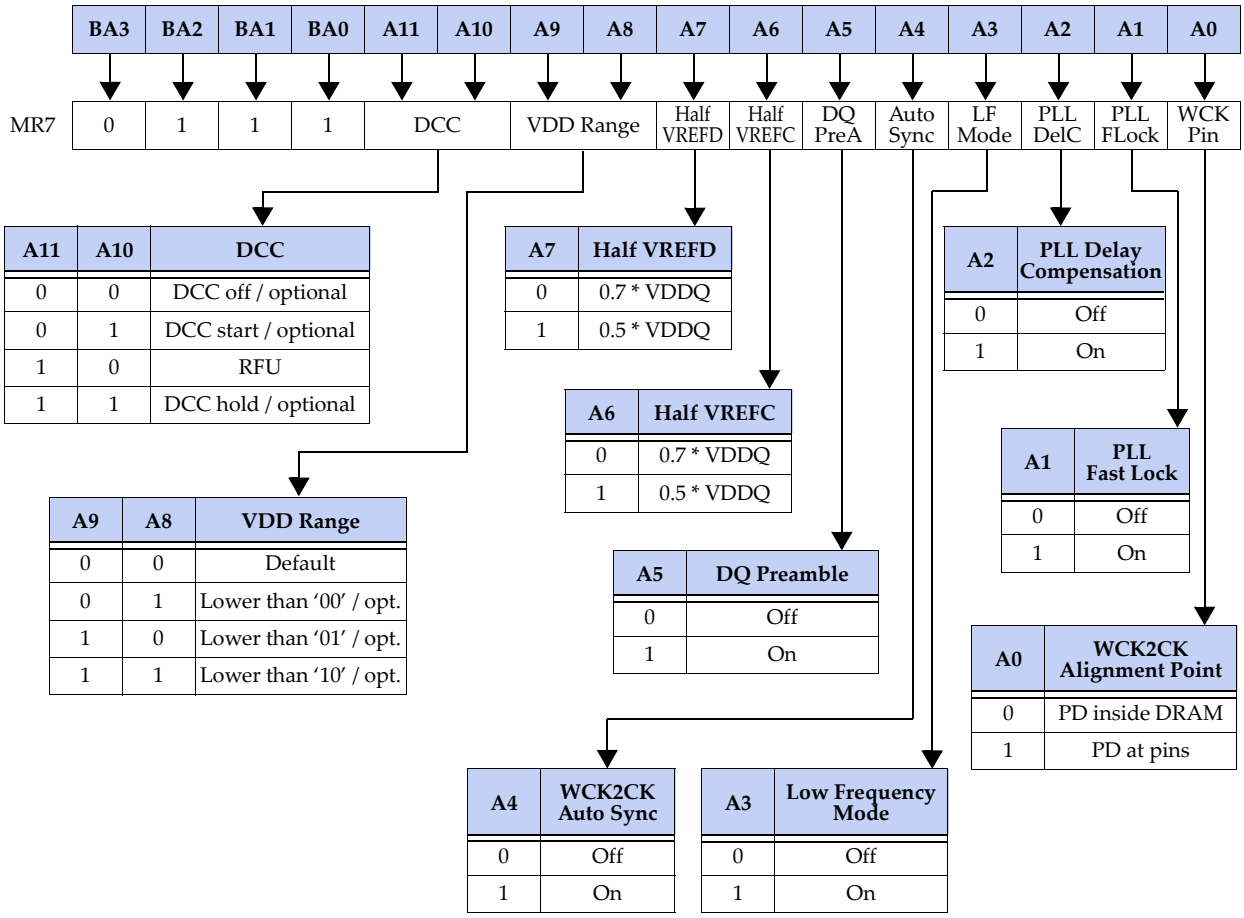


Figure 29 — Mode Register 7 (MR7) Definition

WCK2CK Alignment Point (WCK PIN)

Bit A0 defines the position of the alignment point between CK and WCK clocks. When set to 0, the alignment point will be located at the phase detector inside the GDDR5X SGRAM. When set to 1, the alignment point will be located at the CK and WCK pins. The maximum CK clock frequency in PIN mode is specified by f_{CKPIN}.

PLL Fast Lock

When enabled by bit A1, the PLL's lock time is reduced to t_{FLK} at the expense of a higher power consumption. The bit may be reset once the PLL has locked. PLL Fast Lock is optional.

PLL Delay Compensation

When enabled by bit A2, the PLL's feedback path has a delay equivalent to the WCK clock tree delay.

4.8. MODE REGISTER 7 (MR7) (cont'd)

Low Frequency Mode

When Low Frequency Mode is enabled by bit A3, the power consumption of input receivers and clock trees is reduced. The maximum operating frequency for this low frequency mode (f_{CKLF}) is given in the vendor's datasheet.

WCK2CK Auto Synchronization

GDDR5X SGRAMs support a WCK2CK automatic synchronization mode that eliminates the need for WCK2CK training upon power-down exit or for reducing WCK2CK training time at low frequency. This mode is controlled by bit A4. For a detailed description see WCK2CK Auto Synchronization in the clause entitled WCK2CK Training.

DQ Preamble

When enabled by bit A5, non-gapless READ bursts are preceded by a fixed DQ preamble on the DQ and DBI_n pins of 1 t_{CK} duration. The programmed READ latency does not change when DQ preamble is enabled. The pattern is not encoded with RDBI, however, if RDBI is disabled, the DBI_n pins do not toggle and drive a HIGH.

DQ preamble is supported in QDR mode only; it must be disabled in DDR mode.

Half VREFC and Half VREFD

Bits A6 controls Half VREFC and bit A7 controls Half VREFD. The bits shall be used to adjust the V_{REF} level in case the device is operated without termination. See VREFC and VREFD clause for more details.

VDD Range

Bits A[9:8] are used to adapt DRAM characteristics like internal supply voltages when the actual V_{DD} is lower than the default operating range. The default 00 setting represents the highest V_{DD} supply voltage range supported by the device which typically is 1.35V. All other field values are optional, and the VDD ranges of the optional fields represent voltage ranges lower than the default range in a decreasing voltage order. The actual V_{DD} supply voltage ranges itself are vendor specific.

The bits must be set during device initialization prior to WCK2CK training. GDDR5X SGRAMs supporting multiple voltage and requiring the use of the VDD range must tolerate power-up with a VDD range setting that does not correspond to the actual supply voltage; this includes that the device must be able to execute the MRS command that sets VDD range to the correct value while being operated with an incorrect VDD range setting.

Duty Cycle Correction (DCC)

Bits A[11:10] control the operation of the optional duty cycle corrector (DCC). The DCC can be used to cancel out a static duty cycle error on the WCK clocks. See the clause entitled Duty Cycle Correction (DCC) for more details.

4.9 MODE REGISTER 8 (MR8)

MR8 controls functions like the MSBs for read latency (RLmrs) and write recovery (WR), EDC High-Z, Hibernate self refresh, PLL/DLL range, VREF C2D, VREFD monitor, address compatibility mode, QDR/ DDR operating mode, and CK termination as shown in Figure 30. The register is programmed via the MRS command with BA[3:0] = 1000. Bits A[11:10] of this register are initialized with 0.

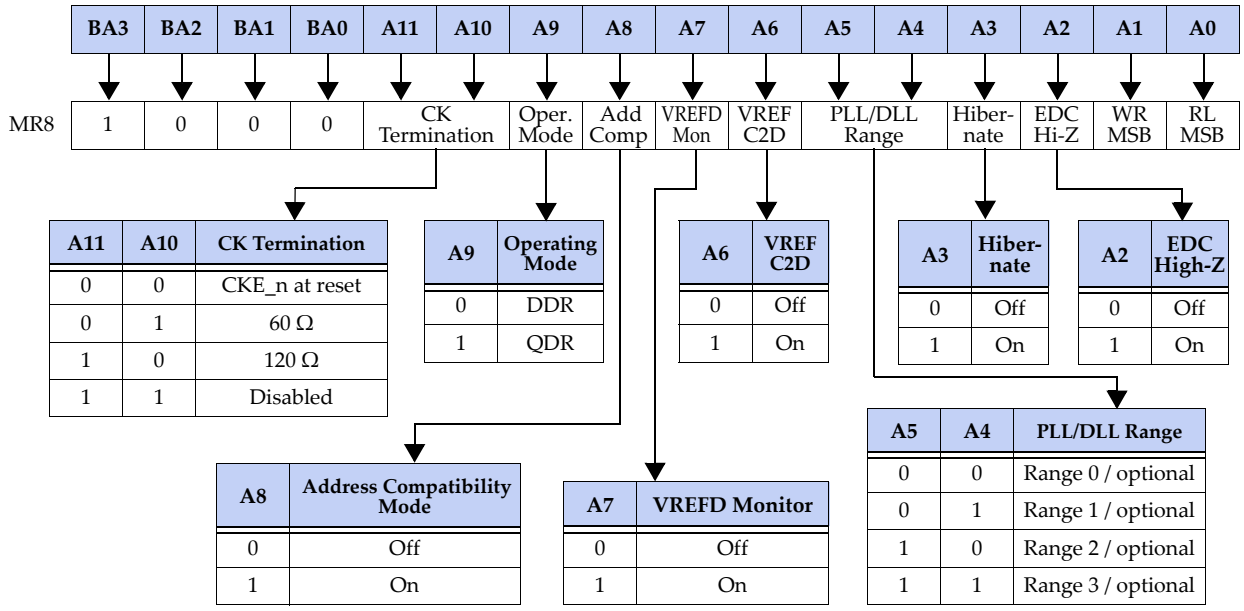


Figure 30 — Mode Register 8 (MR8) Definition

RL MSB and WR MSB

Bits A0 and A1 define the MSB for the read latency (RLmrs) and the write recovery (WR), respectively. See MR0 for more details.

EDC High-Z

With bit A2 set to 1, the EDC pins are in High-Z state. The EDC High-Z function takes precedence over all other features that define the EDC pin's data pattern.

Hibernate Self Refresh

With bit A3 set to 1, the device enters Hibernate self refresh mode with the next SELF REFRESH ENTRY command. The bit is self-clearing.

PLL/DLL Range

Bits A[5:4] may be used to adapt the PLL/DLL characteristics to distinct minimum-to-maximum WCK frequency ranges. All settings and associated WCK frequencies are vendor specific. The DRAM vendor specifications should be consulted for more details.

VREF C2D

Bit A6 enables an internal bridge between the V_{REFC} and V_{REFD} circuits that allows an external V_{REFD} voltage to be supplied via the VREFC pin. See the VREFD clause for more details.

VREFD Monitor

Bit A7 controls the VREFD Monitor mode which allows the observation of the internal V_{REFD} voltage at the EDC pins of both double bytes. See the VREFD clause for more details.

4.9. MODE REGISTER 8 (MR8) (cont'd)

Address Compatibility Mode (Add Comp)

Bit A8 enables the address compatibility mode. The column address received on address inputs A[5:0] is internally used as CAL and CAU in this mode. This mode is intended for controllers that do not support different column addresses CAL and CAU. See the ADDRESSING clause for more details.

Operating Mode

Bit A9 selects between DDR and QDR operating modes.

CK Termination

Bits A[11:10] define the (single-ended) termination for the CK_t and CK_c pins. The default setting (00) provides that the CK termination is determined by latching CKE_n on the rising edge of RESET_n. The CK termination can also be set to a value of 60 Ω which is intended for a single loaded system, or 120 Ω which is intended for clamshell configurations with two devices sharing a common CK clock. The CK termination may also be turned off.

4.10 MODE REGISTER 9 (MR9)

MR9 controls V_{REFD} levels for two of the four data bytes as shown in Figure 31. The register is programmed via the MRS command with BA[3:0] = 1001.

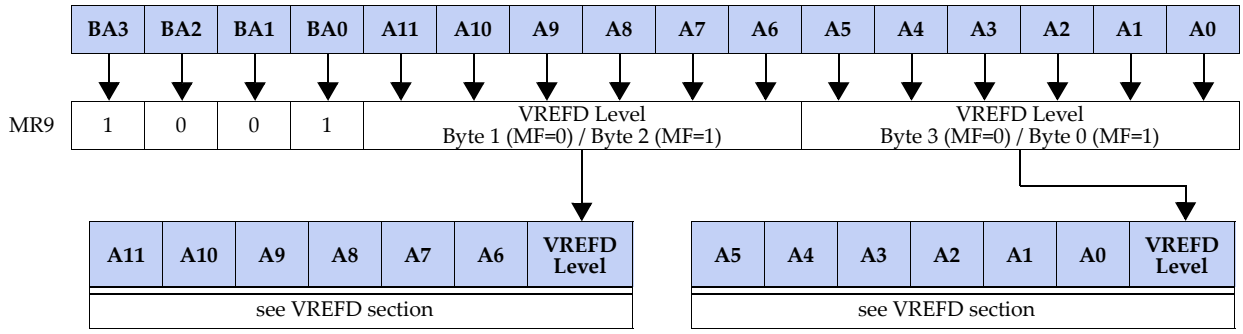


Figure 31 — Mode Register 9 (MR9) Definition

Please refer to MODE REGISTER 6 (MR6) for details.

4.11 MODE REGISTER 10 (MR10)

MR10 is reserved. The register is programmed via the MRS command with BA[3:0] = 1010.

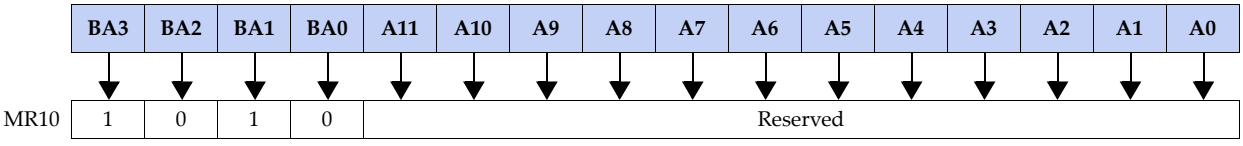
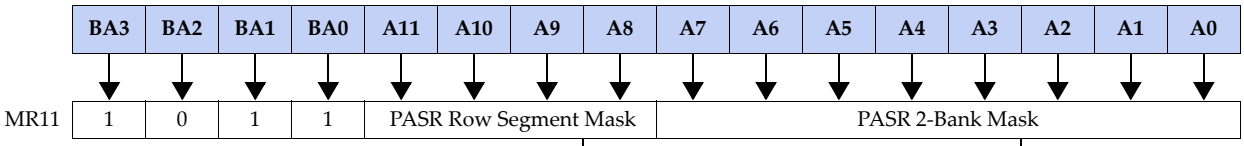


Figure 32 — Mode Register 10 (MR10) Definition

4.12 MODE REGISTER 11 (MR11)

MR11 defines row segment and 2 banks mask for the Partial Array Self Refresh (PASR) as shown in Figure 33. The register is programmed via the MRS command with BA[3:0] = 1011.



A[11:0]	PASR Mask (all bits)
0	Refresh enabled (= unmasked, default)
1	Refresh blocked (= masked)
X	Don't Care for the particular segment or banks

A11	A10	A9	A8	PASR Row Segment Mask	Mode	4 Gb	6 Gb (*)	8 Gb	12 Gb (*)	16 Gb
					x32	A[12:11]	A[13:12]	A[13:12]	A[14:13]	A[14:13]
					x16	A[13:12]	A[14:13]	A[14:13]	A[15:14]	A[15:14]
X	X	X	1	Segment 0	00					
X	X	1	X	Segment 1	01					
X	1	X	X	Segment 2	10					
1	X	X	X	Segment 3	11					

(*): no memory present for row segment 3.

A7	A6	A5	A4	A3	A2	A1	A0	PASR 2 Banks Mask
X	X	X	X	X	X	X	1	Banks 0 and 1
X	X	X	X	X	X	1	X	Banks 2 and 3
X	X	X	X	X	1	X	X	Banks 4 and 5
X	X	X	X	1	X	X	X	Banks 6 and 7
X	X	X	1	X	X	X	X	Banks 8 and 9
X	X	1	X	X	X	X	X	Banks 10 and 11
X	1	X	X	X	X	X	X	Banks 12 and 13
1	X	X	X	X	X	X	X	Banks 14 and 15

Figure 33 — Mode Register 11 (MR11) Definition

Partial Array Self Refresh (PASR)

Bits A[11:8] define the row segment mask and bits A[7:0] define the 2 banks mask for the Partial Array Self Refresh (PASR) feature. The default 0 setting enables the refresh, and the 1 setting blocks the refresh for the selected row segment or 2 banks. An example of how the bits can be used to mask banks and row segments from refresh can be found in the Partial Array Self Refresh (PASR) clause.

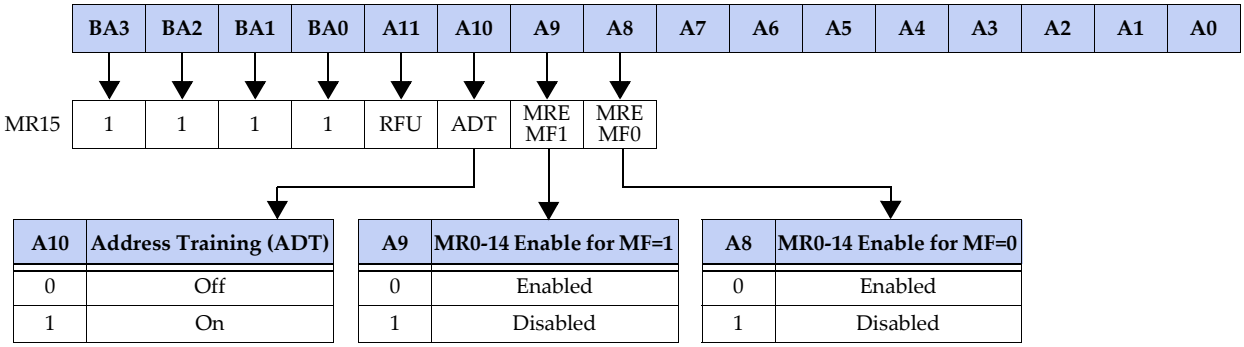
4.13 MODE REGISTERS 12 TO 14 (MR12, MR13, MR14)

MR12, MR13, and MR14 is reserved for vendor specific features. The registers are programmed via the MRS command with BA[3:0] = 1100, 1101 and 1110, respectively.

4.14 MODE REGISTER 15 (MR15)

MR15 controls address training mode and access to Mode Registers 0 to 14 (MRE) as shown in Figure 34. The register is programmed via the MRS command with BA[3:0] = 1111.

MR15 is a special register that operates in SDR addressing mode and latches data on the rising edge of CK_t. Therefore nothing is latched on the rising edge of CK_c as shown in Figure 34. Increased address setup and hold times are assumed to ensure the MRS command to this register is successful while address training (ADT) has not taken place and the integrity of DDR addresses may not be guaranteed.



A10	Address Training (ADT)
0	Off
1	On

A9	MR0-14 Enable for MF=1
0	Enabled
1	Disabled

A8	MR0-14 Enable for MF=0
0	Enabled
1	Disabled

Figure 34 — Mode Register 15 (MR15) Definition

Address Training (ADT)

Address training mode is enabled and disabled with bit A10.

Mode Register 0-14 Enable (MRE)

When disabled by bit A8 (for devices configured as MF=0) or bit A9 (for devices configured as MF=1), the device will ignore any MRS command to registers MR0 to MR14 as shown in Figure 35. MRS commands to MR15 are not affected and are always executed. This function allows for the individual configuration of two devices sharing a common address bus.

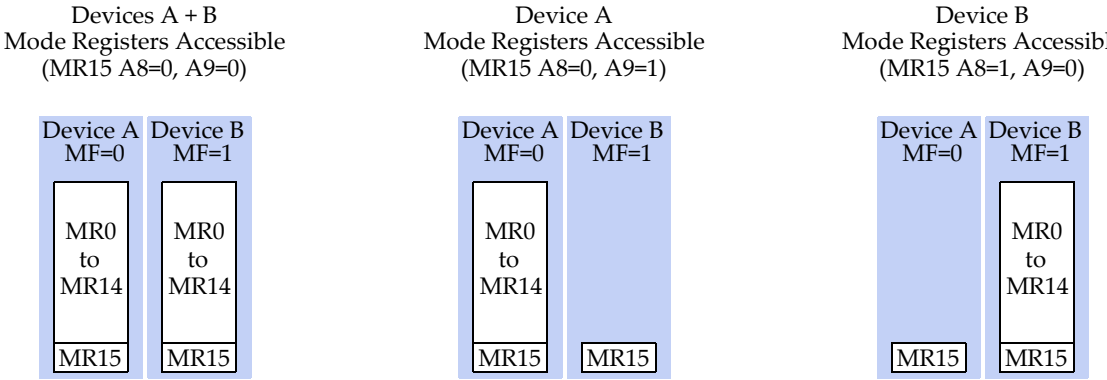


Figure 35 — Mode Register Enable

5 DEVICE INITIALIZATION

5.1 POWER-UP SEQUENCE

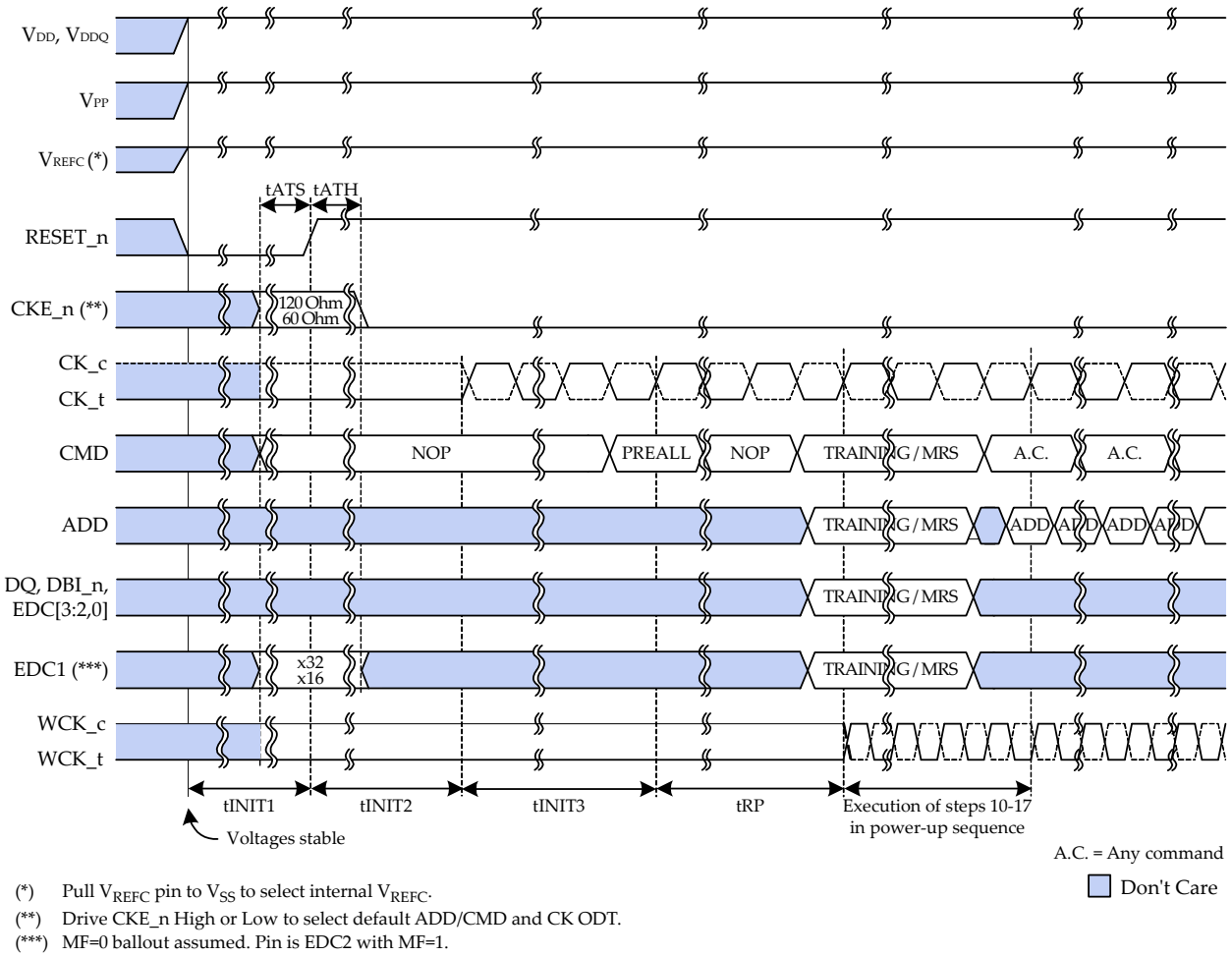
GDDR5X SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The mode registers do not have reset default values, except for ADD/CMD, CK, WCK and data termination, ABI, the EDC hold pattern and PASR. If the mode registers are not set during the initialization sequence, it may lead to unspecified operation.

1. Apply power to V_{PP}. Apply power to V_{DD} at the same time or after power is applied to V_{PP}. Apply power to V_{DDQ} at the same time or after power is applied to V_{DD}. V_{PP} must be equal to or higher than V_{DD} at all times the device is powered up.
2. Apply V_{REFC} at same time or after power is applied to V_{DDQ}, or pull the VREFC pin Low to select internal V_{REFC}.
3. The voltage levels on all signal pins must be less than or equal to V_{DD} and V_{DDQ} on one side and must be larger than or equal to V_{SS} on the other side.
4. Assert RESET_n Low to ensure all drivers are in High-Z and all ODT are off. Maintain RESET_n Low for a minimum time of t_{INIT1}.
5. Assert and hold NOP command. Assert CKE_n Low or High for the desired ADD/CMD and CK ODT at least a time of t_{ATS} before RESET_n is pulled High. At the same time pull EDC1 (with MF=0; pin is EDC2 with MF=1) High for x32 mode or Low for x16 mode. Drive CK_t, WCK_t to static Low level, and CK_c, WCK_c to static High level.
6. After RESET_n is pulled High, maintain CKE_n and EDC1 (with MF=0; pin is EDC2 with MF=1) stable for a minimum time of t_{ATH}.
7. Pull CKE_n Low after t_{ATH} is satisfied. The device performs the initial impedance calibration during this time; this will be done without external clocks. Latest after t_{INIT2} the device enables the CK and ADD/CMD ODT as determined by CKE_n in steps 5 and 6.
8. Provide a stable CK clock for a minimum of t_{INIT3} cycles.
9. Issue a PRECHARGE ALL command followed by NOP commands until t_{RP} is satisfied.
10. Issue MRS command to MR15 to set the GDDR5X SGRAM into address training mode (optional).
11. Complete address training (optional).
12. Issue MRS command to read the Vendor ID.
13. Issue MRS command to set WCK termination values.
14. Provide stable WCK clocks.
15. Issue MRS commands to the mode registers in any order to select QDR or DDR operating mode, PLL/DLL on/off mode, the position of the WCK2CK alignment point, and to set WLmrs, RLmrs, CRCWL and CRCRL to appropriate values. All these features must be programmed before WCK2CK training, and t_{MRD} must be met during this procedure.
16. Issue two REFRESH commands followed by NOP until t_{RFC} is satisfied.
17. After any necessary training sequences such as WCK2CK training, READ training (LDFF, RDTR) and WRITE training (WRTR, RDTR), the device is ready for normal operation.

Table 11 — Address/Command and CK ODT

CKE_n AT RESET_n HIGH TRANSITION	VALUE
Low	ZQ/2 = 60 Ω
High	ZQ = 120 Ω

5.1 POWER-UP SEQUENCE (cont'd)



(*) Pull V_{REFC} pin to V_{SS} to select internal V_{REFC}.
(**) Drive CKE_n High or Low to select default ADD/CMD and CK ODT.
(***) MF=0 ballout assumed. Pin is EDC2 with MF=1.

Figure 36 — Power-up Initialization

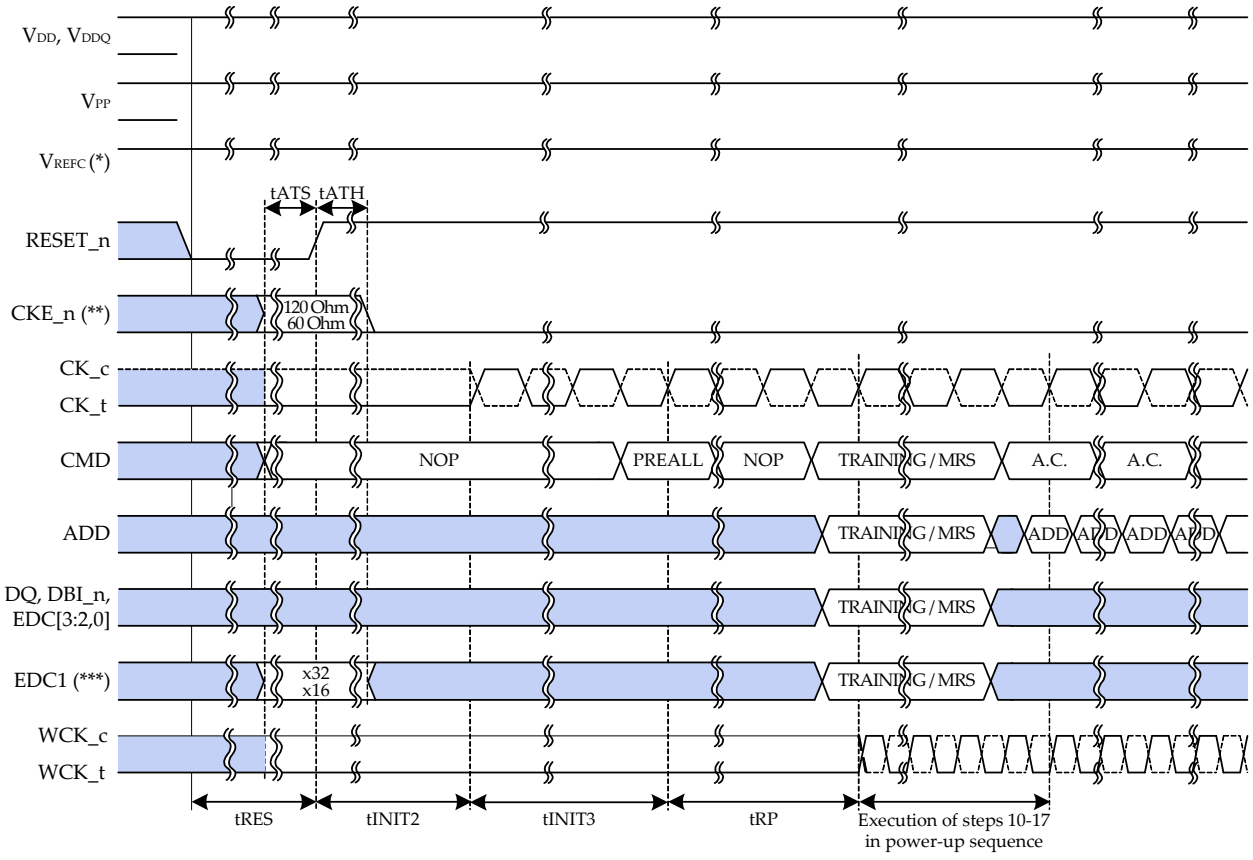
Table 12 — Device Initialization Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
RESET_n initial low time after power-up	t_{INIT1}	200	–	µs	
CKE_n and EDC1/2 (x32/x16 mode select) setup time before RESET_n de-assertion	t_{ATS}	10	–	ns	
CKE_n and EDC1/2 (x32/x16 mode select) hold time after RESET_n de-assertion	t_{ATH}	10	–	ns	
Time after RESET_n de-assertion before starting the CK clock	t_{INIT2}	500	–	µs	
Stable CK clock cycles before issuing valid commands	t_{INIT3}	100	–	t_{CK}	
RESET_n low time with stable power	t_{RES}	100	–	ns	

5.2 INITIALIZATION WITH STABLE POWER

The following sequence is required for reset subsequent to power-up initialization. This requires that the power has been stable within the specified V_{DD}, V_{DDQ} and V_{PP} ranges since power-up initialization (see Figure 36):

1. Assert RESET_n Low anytime when reset is needed.
2. Maintain RESET_n Low for a minimum time of t_{RES}.
3. Assert and hold NOP command. Assert CKE_n Low or High for the desired ADD/CMD and CK ODT at least a time of t_{ATS} before RESET_n is pulled High. At the same time pull EDC1 (with MF=0; pin is EDC2 with MF=1) to the same level as during power-up initialization as device functionality is not guaranteed if the I/O width changes. Drive CK_t, WCK_t to static Low level, and CK_c, WCK_c to static High level.
4. Continue with step 6 of the power-up initialization sequence.



(*) Pull V_{REFC} pin to V_{SS} to select internal V_{REFC}.
(**) Drive CKE_n High or Low to select default ADD/CMD and CK ODT.
(***) MF=0 ballout assumed. Pin is EDC2 with MF=1.

Figure 37 — Initialization with Stable Power

5.3 VENDOR ID

GDDR5X SGRAMs include a Vendor ID feature that allows the controller to receive information from the device to differentiate between different vendors and different devices using a software algorithm.

When the Vendor ID function is enabled the GDDR5X SGRAM will provide its Manufacturers Vendor Code, Revision ID and density on the two bytes that are enabled in x16 mode as shown in Table 13. The FIFO depth is fixed to 6 and not included in the Vendor ID.

Vendor ID is part of the INFO field of Mode Register 3 (MR3) and is selected by issuing a MODE REGISTER SET command with MR3 bit A6 set to 1, and bit A7 set to 0. MR3 bits A[5:0] and A[11:8] are set to the desired values. Additional information can optionally be provided by the vendor using the vendor specific settings on the INFO field and will follow the same protocol as vendor ID unless explicitly stated in the vendor data sheet.

The Vendor ID will be driven onto the DQ bus after the MRS command that sets bits A6 to 1 and A7 to 0. The DQ bus will be continuously driven until an MRS command sets MR3 A6 and A7 back to 0 to disable the INFO field or to another valid state for the INFO field if the INFO field includes support for additional vendor specific information. The DQ bus will be in ODT state after $t_{WRIDOFF}$(max). The code can be sampled by the controller after waiting t_{WRIDON}(max) and before $t_{WRIDOFF}$(min). DBI is not enabled or ignored during all Vendor ID operations.

The EDC hold pattern is continuously driven on the EDC pins provided a stable WCK clock is applied.

Table 13 — Vendor ID to DQ Mapping

Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	**RFU ("11111")**					**Density see Table 15**			**Revision ID**				**Manufacturers Vendor Code see Table 14**			
MF=0	DQ]23:19]					DQ[18:16]			DQ[7:4]				DQ[3:0]			
MF=1	DQ[15:11]					DQ[10:8]			DQ[31:28]				DQ[27:24]			

Table 14 — Manufacturers Vendor Code

3	2	1	0	Manufacturer's Name
0	0	0	1	Samsung
0	1	1	0	SK hynix
1	1	1	1	Micron
all others				Reserved

Table 15 — Density

10	9	8	Density
0	0	0	4 Gb
0	0	1	6 Gb
0	1	0	8 Gb
0	1	1	12 Gb
1	0	0	16 Gb
all others			Reserved

5.3 VENDOR ID (cont'd)

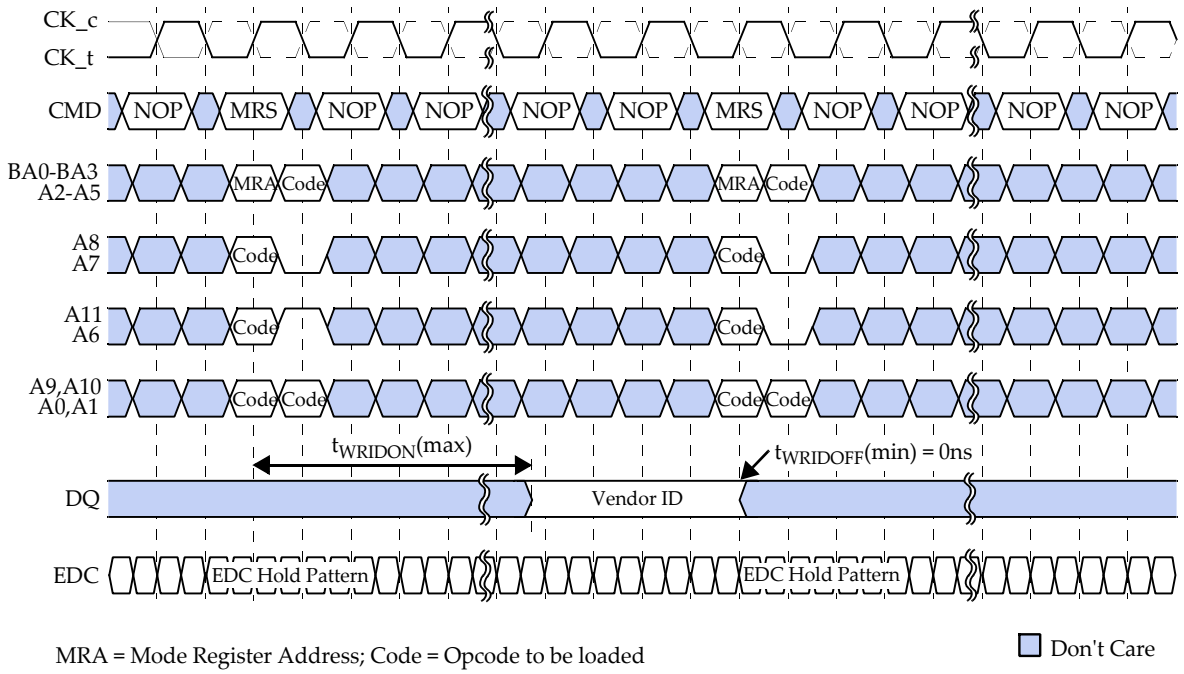


Figure 38 — Vendor ID Timing Diagram

6 TRAINING

6.1 INTERFACE TRAINING SEQUENCE

Due to the high data rates of GDDR5X, it is recommended that the interfaces be trained to operate with the optimal timings. The device has defined features that allow for complete and efficient training of the I/O interface without the use of the device's memory array. The interface trainings are required for normal DRAM functionality unless deemed optional by the DRAM vendor or unless the device is operating in lower frequency mode as described in the low frequency clause. Interface timings will only be guaranteed after all required trainings have been executed.

A recommended order of training sequences is based on the following criteria:

The address training must be done first to allow full access to the mode registers. (MR15 for address training is a special SDR mode register guaranteed to work without training.) Address input timing shall function without training as long as t_{AS}/t_{AH} are met.

WCK2CK training must be done before read training because a shift in WCK relative to CK will cause a shift in all read timings relative to CK.

Read training should be done before write training because optimal write training depends on correct read data.

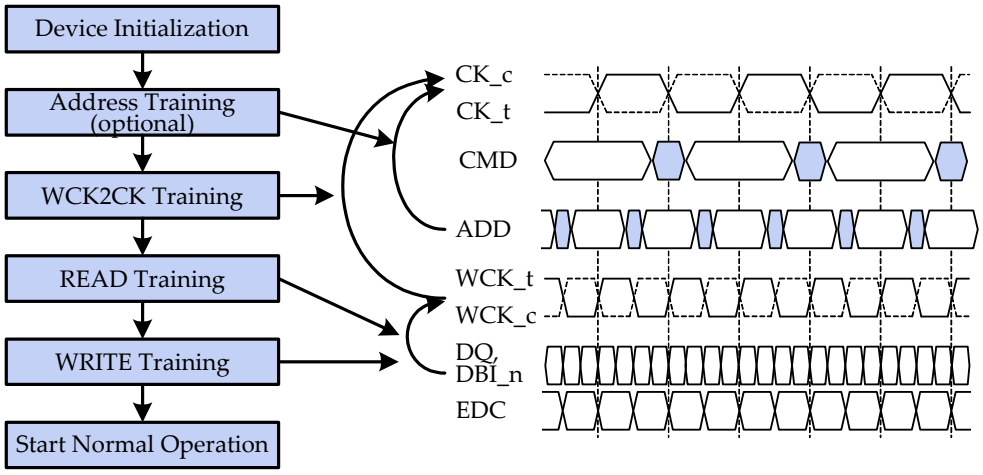


Figure 39 — Interface Training Sequence

6.2 ADDRESS TRAINING

The GDDR5X SGRAM provides a means for address bus interface training. The controller may use the address training mode to improve the timing margins on the address bus.

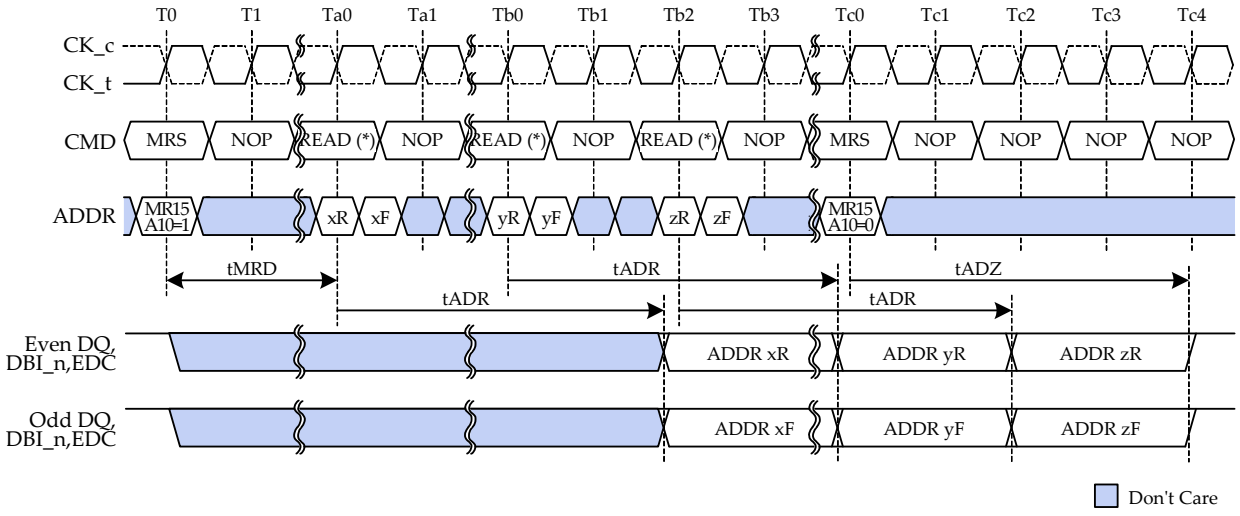
Address training mode is entered and exited via the ADT bit in MR15. MR15 supports the same setup and hold times on the addresses as for commands to allow a safe entry into address training mode.

Address training mode uses an internal bridge between the device's address inputs and DQ/DBI_n/EDC outputs. It also uses a special READ command for address capture that is encoded using the SDR command pins only (RAS_n,CAS_n,WE_n = H,L,H) without interpreting the address values typically used to encode the commands. Once the address training mode has been entered, the address values registered coincident with this special READ command are transmitted to the controller on the DQ/DBI_n/EDC pins. The controller is then expected to compare the address pattern received to the expected value and to adjust the address transmit timing accordingly. The procedure may be repeated using different address pattern and interface timings. No WCK clock is required for this special READ command operation during address training mode. The latched addresses are driven out asynchronously.

The only commands allowed during address training mode are this special READ, MRS (e.g., to exit address training mode) and NOP.

The ABI_n pin's interface timing may be trained together with the other address lines. Note that ABI is enabled in MR1 upon power-up, and the ABI_n pin can only be observed indirectly by receiving the returned addresses as true (ABI_n = High) or inverted (ABI_n = Low).

The timing diagram in Figure 40 illustrates the typical command sequence in address training mode. The DQ/DBI_n/EDC output drivers are enabled as long as the ADT bit is set. The minimum spacing between consecutive special READ commands is 2 t_{CK}.



NOTE 1 READ command encoding: RAS_n = H, CAS_n = L, WE_n = H.

NOTE 2 ADDx,y,zR = 1st half of address x,y,z, sampled on rising CK_t edge. ADDx,y,zF = 2nd half of address x,y,z, sampled on rising CK_c edge.

NOTE 3 Addresses sampled on rising CK_t edge are returned on even DQ after t_{ADR}. Addresses sampled on rising CK_c edge are returned on odd DQ simultaneously with even DQ.

NOTE 4 Outputs are enabled when ADT bit in MR15 set to 1 (enter address training mode). Outputs are disabled after t_{ADZ} when ADT bit in MR15 set to 0 (exit address training mode).

Figure 40 — Address Training Timing

6.2 ADDRESS TRAINING (cont'd)

Table 16 — AC timings in Address Training Mode

Parameter	Symbol	Min	Max	Unit
READ command to data out delay	t_{ADR}	0	vendor specific	ns
ADT off to DQ/DBI_n in ODT state delay	t_{ADZ}	--	vendor specific	ns

Table 17 defines the correspondence between address bits and DQ/DBI_n/EDC. The table applies to MF=0 and MF=1 ballouts as well as to x32 and x16 modes. In x16 mode the address bits are returned on the two bytes enabled in that mode, which are bytes 0 and 2 for MF=0 and bytes 1 and 3 for MF=1 configurations. In x32 mode the address bits are returned on all 4 bytes.

Table 17 — Address to DQ/DBI_n/EDC Mapping in Address Training Mode

Output	Address bits registered at rising edge of CK_t									
	A14	A12	A8	A11	BA1	BA2	BA3	BA0	A9	A10
Data Return	EDC0	DBI0_n	DQ22	DQ20	DQ18	DQ16	DQ6	DQ4	DQ2	DQ0
	EDC1	DBI1_n	DQ30	DQ28	DQ26	DQ24	DQ14	DQ12	DQ10	DQ8
Output	Address bits registered at rising edge of CK_c									
	A15	A13	A7	A6	A5	A4	A3	A2	A1	A0
Data Return	EDC2	DBI2_n	DQ23	DQ21	DQ19	DQ17	DQ7	DQ5	DQ3	DQ1
	EDC3	DBI3_n	DQ31	DQ29	DQ27	DQ25	DQ15	DQ13	DQ11	DQ9

6.3 WCK2CK TRAINING

The purpose of WCK2CK training is to align the data WCK clock with the command CK clock to aid in the device's internal data synchronization between the logic clocked by CK and WCK. This will help to define both Read and Write latencies between the device and the memory controller. WCK2CK training mode is controlled via MR3 bit A4.

Before starting WCK2CK training, the following conditions must be met:

- CK clock is stable and toggling;
- Address and command pin timing must be guaranteed;
- The QDR/DDR operating mode select bit (MR8 A9) is set to the desired mode;
- PLL on/off (MR1 A7) and PLL delay compensation enable (MR7 A2) are set to desired mode;
- The desired WCK2CK alignment point (MR7 A0) is selected;
- 2 mode register bits for internal WCK01 and WCK23 inversion (MR3 bits A[3:2]) are set to a known state;
- All banks are idle and no other command execution is in progress.

WCK2CK training must occur after any of the following:

- Device initialization;
- CK and WCK frequency changes;
- Any RLmrs, WLmrs, CRCRL or CRCWL latency change;
- Change between QDR and DDR operating modes;
- PLL on/off (MR1 A7) and PLL delay compensation mode (MR7 A2) changes;
- Change of the WCK2CK alignment point (MR7 A0).

6.3 WCK2CK TRAINING (cont'd)

At self refresh exit, at a minimum, the device's divide-by-2 circuits must be reset by setting MR3 A4 to High and WCK is restarted in the same way as the initial training value at power up. Alternatively full WCK2CK training can be at done at self refresh exit. See Self Refresh clause for more details on self refresh. See WCK2CK auto synchronization clause for more details on options for WCK2CK alignment at power-down exit.

Figure 41 and Figure 42 show example WCK2CK training sequences. WCK2CK training is entered via MRS by setting bit A4 in MR3. This initiates the WCK divide-by-2 circuits associated with WCK01 and WCK23 clocks. In case the divide-by-2 circuits are at opposite output phases, which is indicated by opposite "early/late" phases on the EDC pins associated with WCK01 and WCK23 (see Figure 43), they may be put in phase by using the WCK01 and WCK23 inversion bits. Alternatively, the WCK clocks may be put into a stable inactive state for this initialization event to aid in resetting all dividers to the same output phase as shown in Figure 42. The challenge of this method is to restart the WCK clocks in a way that even their first clock edges meet the WCK clock input specification. Otherwise, divide-by-2 circuits for both WCK01 and WCK23 might again have opposite phase alignment. The use of this WCK2CK training method is restricted to lower operating frequencies up to $f_{WCKSTOP}$.

Figure 43 illustrates how the WCK phase information is derived. Phase detectors (PD) sample the internal divided-by-2 WCK clocks. Only one sample point is shown for clarity; however, in reality, when WCK2CK training mode is enabled, a sample occurs every t_{CK} and is translated to the EDC pins accordingly. If the divided-by-2 WCK clock arrives early, then the EDC pin outputs a High during the time interval specified; if the divide-by-2 WCK clock arrives late, then the EDC pin outputs a Low during the time interval specified. If the divide-by-2 WCK and CK clocks are perfectly aligned at the phase detector, the EDC pins are indeterminate.

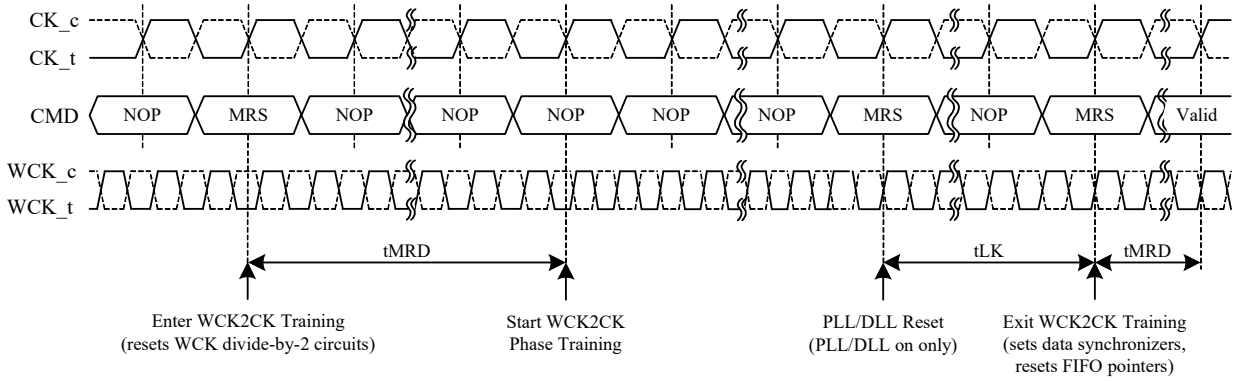


Figure 41 — Example WCK2CK Training Sequence with Free-Running WCK

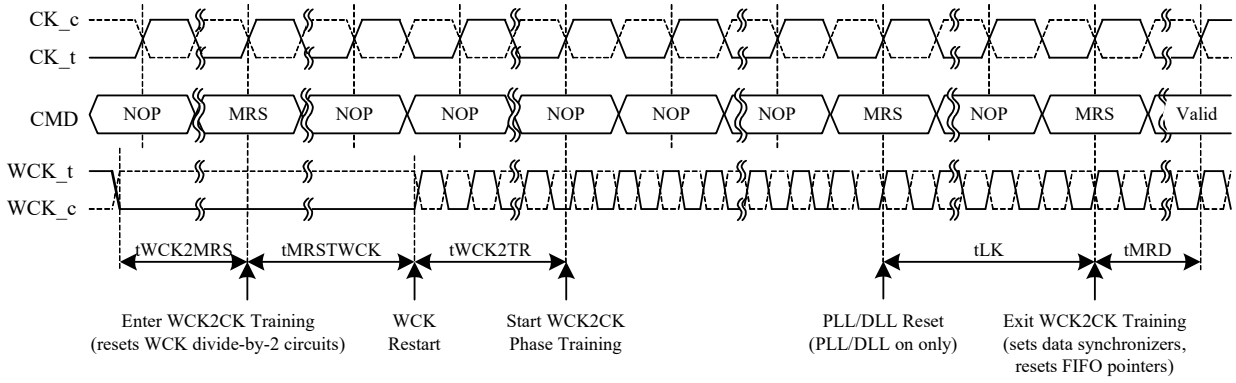


Figure 42 — Example WCK2CK Training Sequence with WCK Stop

6.3 WCK2CK TRAINING (cont'd)

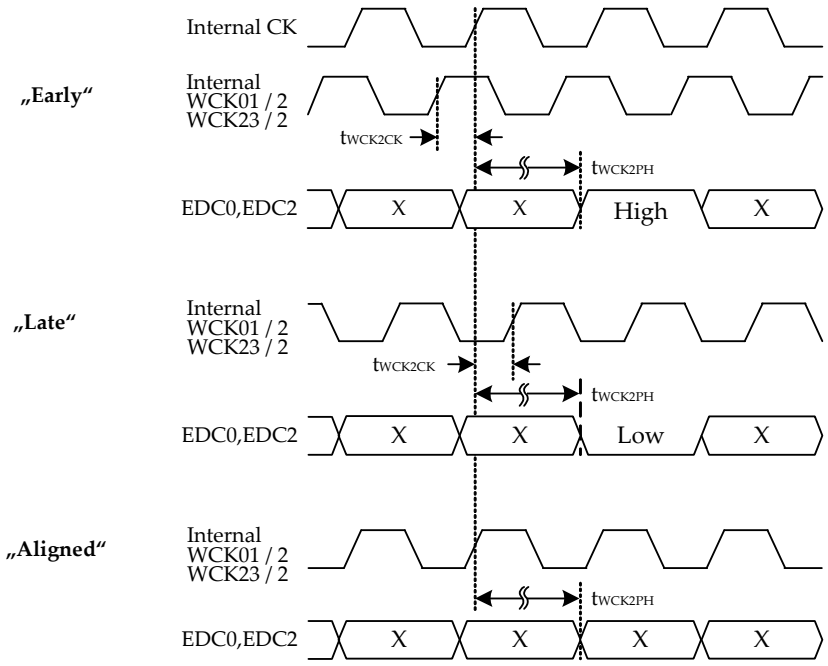


Figure 43 — EDC Pin Behavior for WCK2CK Training

The ideal alignment is indicated by the phase detector output transitioning from "early" to "late" when the delay of the WCK phase is continuously increased. The WCK phase range for ideal alignment is specified by the parameter $t_{WCK2CKPIN}$ in the vendor's datasheet; the value(s) vary with the PLL/DLL mode (on or off) and the selected alignment point.

Table 18 — Phase Detector and EDC Pin Behavior

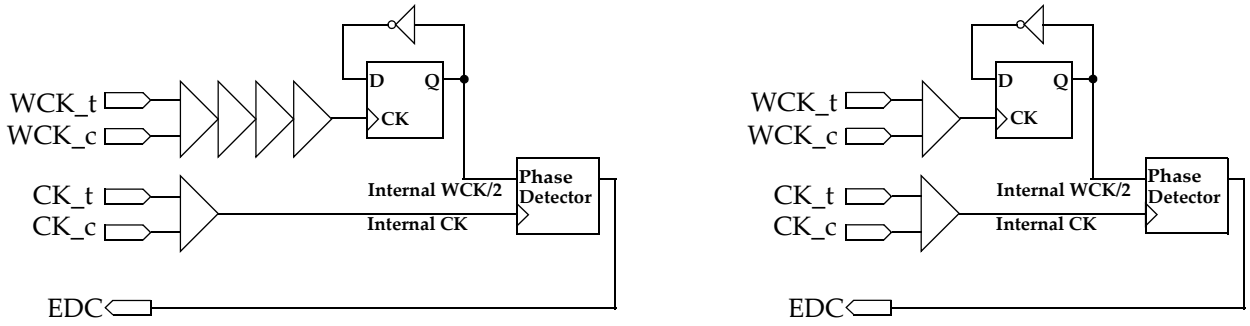
WCK/2 value sampled by CK	WCK2CK Phase	EDC Pin Output	Recommended Action
1	'Early'	High	Increase Delay on WCK
0	'Late'	Low	Decrease Delay on WCK

If enabled, the PLL/DLL does not interfere in the behavior of the WCK2CK training. Significantly moving the phase and/or stopping the WCK during training may disturb the PLL/DLL. It is required to perform a PLL/DLL reset after the WCK2CK training has determined and selected the proper alignment between WCK and CK clocks. The PLL/DLL lock time t_{LK} must be met before exiting WCK2CK training to guarantee that the PLL/DLL is in lock such that the data synchronizers are set upon WCK2CK training exit.

WCK2CK training is exited via MRS by resetting bit A4 in MR3. Proper reset of the data synchronizers requires that the WCK and CK clocks are aligned within $t_{WCK2CKSYNC}$ upon WCK2CK training exit. After exiting WCK2CK training mode, the WCK phase is allowed to further drift from the ideal alignment point by a maximum of t_{WCK2CK} (e.g., due to voltage and temperature variation). Once this WCK phase drift exceeds t_{WCK2CK}(min) or t_{WCK2CK}(max), WCK2CK training must be repeated and the clocks must be realigned.

6.3.1 WCK2CK Alignment at Pin Mode

The WCK and CK phase alignment point can be changed via MRS by setting bit A0 in MR7. In normal mode, when MR7 A0 is set to 0, the phases of CK and WCK are aligned at the phase detector. On the other hand, when MR7 A0 is set to 1, the phases of CK and WCK are aligned at the pins. Pin mode is supported up to the max CK clock frequency of f_{CKPIN}, and is an option to reduce the WCK2CK training time at low frequency since no phase search for the ideal alignment position is required.



Normal Mode **Pin Mode**

Figure 44 — Normal and Pin Mode

6.3.2 WCK2CK Auto Synchronization

WCK2CK automatic synchronization mode reduces the WCK2CK training time upon power-down exit. This mode is controlled by the AutoSync bit (MR7 A4), and is effective when the LP2 bit (MR5 A1) is set and the WCK clocks are stopped during power-down. This mode works for both normal and pin mode. When WCK2CK automatic synchronization mode is enabled, a full WCK2CK training including phase search is not required after power-down exit, although WCK2CK MRS must be issued momentarily for setting the data synchronizers. However, WCK and CK clocks must meet the $t_{WCK2CKSYNC}$ specification upon power-down exit. Any allowed command may be issued after t_{XP} or after t_{LK} in case the PLL/DLL had been enabled upon power-down entry. The PLL/DLL sequence is not affected by this mode. The use of WCK2CK automatic synchronization mode is restricted to lower operating frequencies up to $f_{CKAUTOSYNC}$.

6.3.3 WCK2CK Training Examples

Table 19 describes WCK2CK training methods for different frequency ranges. The actual frequency ranges are vendor specific. Divider initialization can be done by training with WCK2CK inversion, WCK2CK stop, or WCK2CK auto-sync. In case of WCK2CK stop for divider initialization it is required to disable WCK2CK auto-sync. The combined use of pin and WCK2CK auto-sync modes can minimize WCK2CK training time at low frequency.

Table 19 — An Example of WCK2CK Training Simplified for Normal Mode and Pin Mode

	High Frequency		Middle Frequency		Low Frequency	
WCK2CK Alignment Mode	**Normal**	**Pin**	**Normal**	**Pin**	**Normal**	**Pin**
Phase Search	Required	N/A	Required	No	No	No

6.3.3 WCK2CK Training Examples (cont'd)

The following examples describe the WCK2CK training in more detail.

Example 1: outline of a basic WCK2CK training sequence without WCK clock stop:

1. Enable training mode via MRS and wait t_{MRD}.
2. Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; in case the internal divide-by-2 circuits are at opposite phase use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits.
3. Adjust the WCK phases independently for WCK01 and WCK23 to the optimal point ("ideal alignment").
4. Issue a PLL/DLL reset and wait for t_{LK} (PLL/DLL on mode only).
5. While all WCK and CK clocks are aligned, exit WCK2CK training mode via MRS.
6. Wait t_{MRD} for the reset of data synchronizers.

Example 2: outline of a basic WCK2CK training sequence with WCK clock stop:

1. Stop WCK clocks with WCK01_t/WCK23_t LOW and WCK01_c/WCK23_c HIGH.
2. Wait $t_{WCK2MRS}$ for internal WCK clocks to settle.
3. Enable training mode via MRS and wait $t_{MRSTWCK}$ for divide-by-2 circuits to reset.
4. Start WCK clocks without glitches (both divide-by-2 circuits remain in sync).
5. Wait t_{WCK2TR} for internal WCK clocks to stabilize.
6. Sweep and observe the phase independently for WCK01 on EDC0 and WCK23 on EDC2; adjust the WCK phase to the optimal point ("ideal alignment").
7. Issue a PLL/DLL reset and wait t_{LK} (PLL/DLL on mode only).
8. While all WCK and CK clocks are aligned, exit WCK2CK training mode via MRS.
9. Wait t_{MRD} for the reset of data synchronizers.

WCK2CK Training in x16 Mode

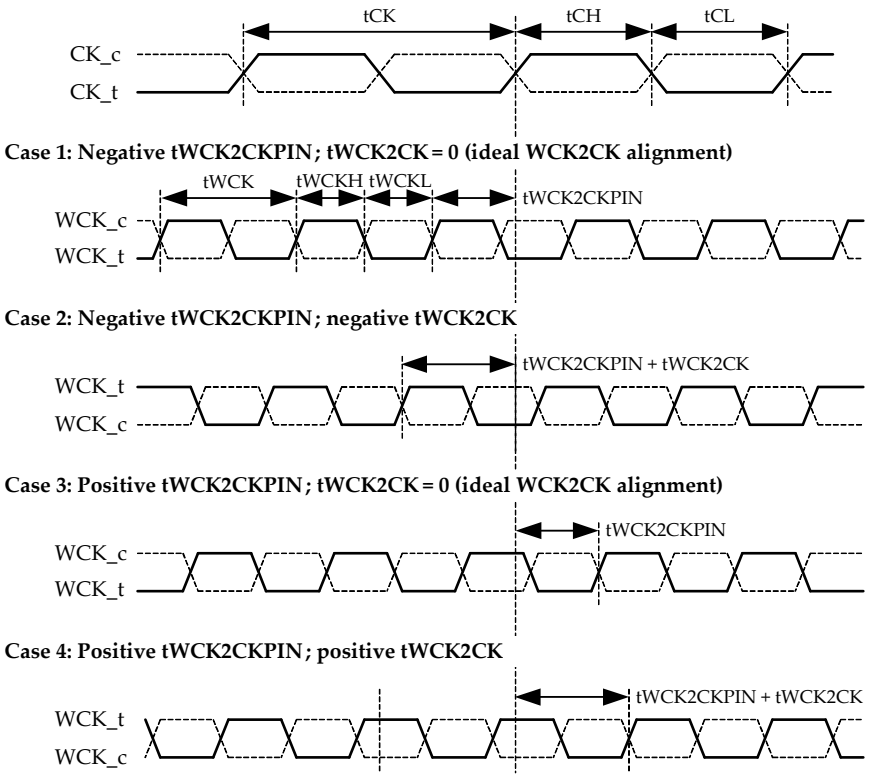
For configurations where the WCK clocks are not shared between two devices, the WCK phase should be set to the ideal alignment point. However, for configurations where two devices share the WCK clocks as in a x16 clamshell, an offset may be required, given by the midpoint of both device's ideal WCK positions. The maximum allowed offset is specified by parameter $t_{WCK2CKSYNC}$: $t_{WCK2CKSYNC}$ defines the WCK offset range from the ideal alignment which guarantees that a device's WCK and CK clocks will internally synchronize upon training exit.

Example 3: outline of training sequence for x16 configurations with 2 devices sharing their WCK clocks:

1. Enable training mode for both devices via MRS and wait wait t_{MRD}.
2. For both devices sweep and observe the phase independently for WCK01 and WCK23 on each EDC pin; in case the internal divide-by-2 circuits are at opposite phases use either the WCK01 or WCK23 inversion bit to flip one of the WCK divide-by-2 circuits; use MREMF0 and MREMF1 bits in MR15 ("soft chip select") to explicitly direct the MRS command for this phase flipping to either the device that is configured to non-mirrored mode (MF=0) or to mirrored (MF=1) mode.
3. Sweep and observe the phase on the first device independently for WCK01 and WCK23; store the setting for the optimal WCK phases.
4. Sweep and observe the phase on the second device independently for WCK01 and WCK23; store the setting for the optimal WCK phases.
5. Sweep WCK01 and WCK23 phases to the midpoint of the both device's optimal settings.
6. Issue a PLL/DLL reset and wait t_{LK} (PLL/DLL on mode only).
7. While all WCK and CK clocks are aligned, exit WCK2CK training mode via MRS.
8. Wait t_{MRD} for the reset of data synchronizers.

6.3.4 Read and Write Latencies

Read and write latency timings are defined relative to CK. Any offset in WCK and CK at the pins and/or the phase detector will be reflected in the latency timings. The parameters used to define the relationship between WCK and CK are shown in Figure 45. For more details on the impact on read and write timings see the OPERATIONS clause.



NOTE 1 tWCK2CKPIN and tWCK2CK parameter values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. WCK2CK training is required to determine the correct WCK2CK phase for stable device operation.

Figure 45 — WCK2CK Timings

6.4 READ TRAINING

Read training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed output of the device. Each pin (DQ[31:0], DBI[3:0]_n, EDC[3:0]) can be individually trained during this sequence.

For read training the following conditions must be true:

- at least one bank is active, or a REFRESH must be in progress and bit A2 in MR5 is set to 0 to allow training during refresh (to disable this special REFRESH enabling of the WCK clock tree an ACTIVATE command must be issued, or the device must be set to power-down or self refresh mode).
- WCK2CK training must be complete.
- the PLL/DLL must be locked, if enabled.
- RDBI and WDBI must both be either enabled or disabled prior to and during read training. They must be enabled if read training includes the DBI_n pins, and they must be disabled if read training does not include the DBI_n pins.
- RDCRC and WRCRC must both be either enabled or disabled prior to and during read training. They must be enabled if read training includes the EDC pins, and they must be disabled if read training does not include the EDC pins.

The following commands are associated with Read Training:

- LDFF to preload the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither LDFF nor RDTR access the memory array. No MRS command is required to enter read training.

Figure 46 shows an example of the internal data paths used with LDFF and RDTR. Table 20 lists AC timing parameters associated with read training.

Table 20 — LDFF and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVATE to RDTR command delay	t_{RCDRTR}		–	ns	
ACTIVATE to LDFF command delay	t_{RCDLTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
READ/WRITE bank A to READ/WRITE bank B command delay different bank groups	t_{CCDS}		–	t_{CK}	1
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF15 to LDFF command cycle time	t_{LTLFTR}		–	t_{CK}	2
LDFF15 to RDTR command delay	t_{LTRTR}		–	t_{CK}	2
READ or RDTR to LDFF command delay	t_{RDTLT}		–	t_{CK}	

NOTE 1 Use t_{CCDS} for gapless consecutive RDTR commands regardless whether Bank Groups is enabled or not.
NOTE 2 In DDR mode this parameter refers to LDFF7 instead of LDFF15.

6.4 READ TRAINING (cont'd)

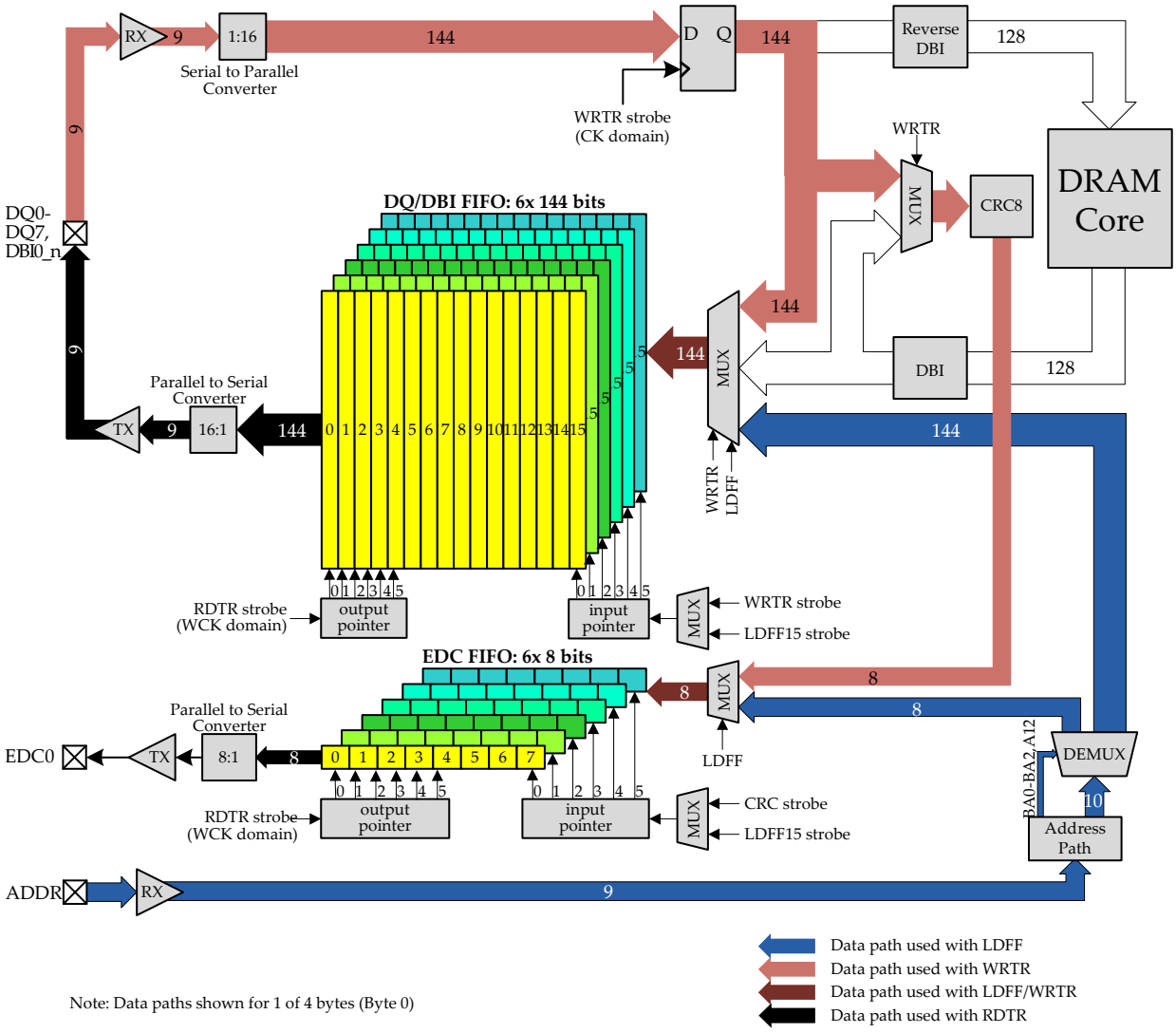


Figure 46 — Data Paths Used for Read and Write Training

6.4.1 LDFF Command

The LDFF command is used to securely load data to the device's Read FIFOs via the address bus. The Read FIFO has a fixed depth of 6 bursts and thus can store a 6 x 16 = 96 U.I. long bit pattern in QDR mode, and a 6 x 8 = 48 U.I. long bit pattern in DDR mode uniquely to every DQ, DBI_n and EDC pin within a byte. The pattern length for the EDC pin is 48 U.I. in both modes.

The data pattern is conveyed on addresses A[7:0] for DQ[7:0], A9 for DBI0_n, and BA3 for EDC0 as shown in Figure 48 for QDR mode and Figure 49 for DDR mode; the data are internally replicated to all 4 bytes.

Each LDFF command loads one burst position. Sixteen LDFF commands are required in QDR mode to fill one FIFO stage, and addresses A12, BA[2:0] select the burst position from 0 to 15. Eight LDFF commands are required in DDR mode to fill one FIFO stage, and addresses BA[2:0] select the burst position from 0 to 7 with address A12 being Don't Care. The EDC data pattern conveyed with LDFF commands to burst locations 8 to 15 are ignored.

6.4.1 LDFF Command (cont'd)

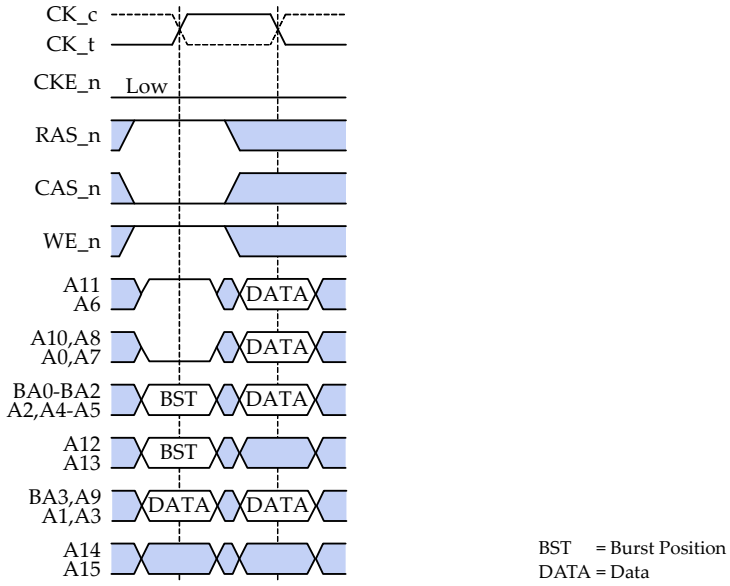


Figure 47 — LDFF Command

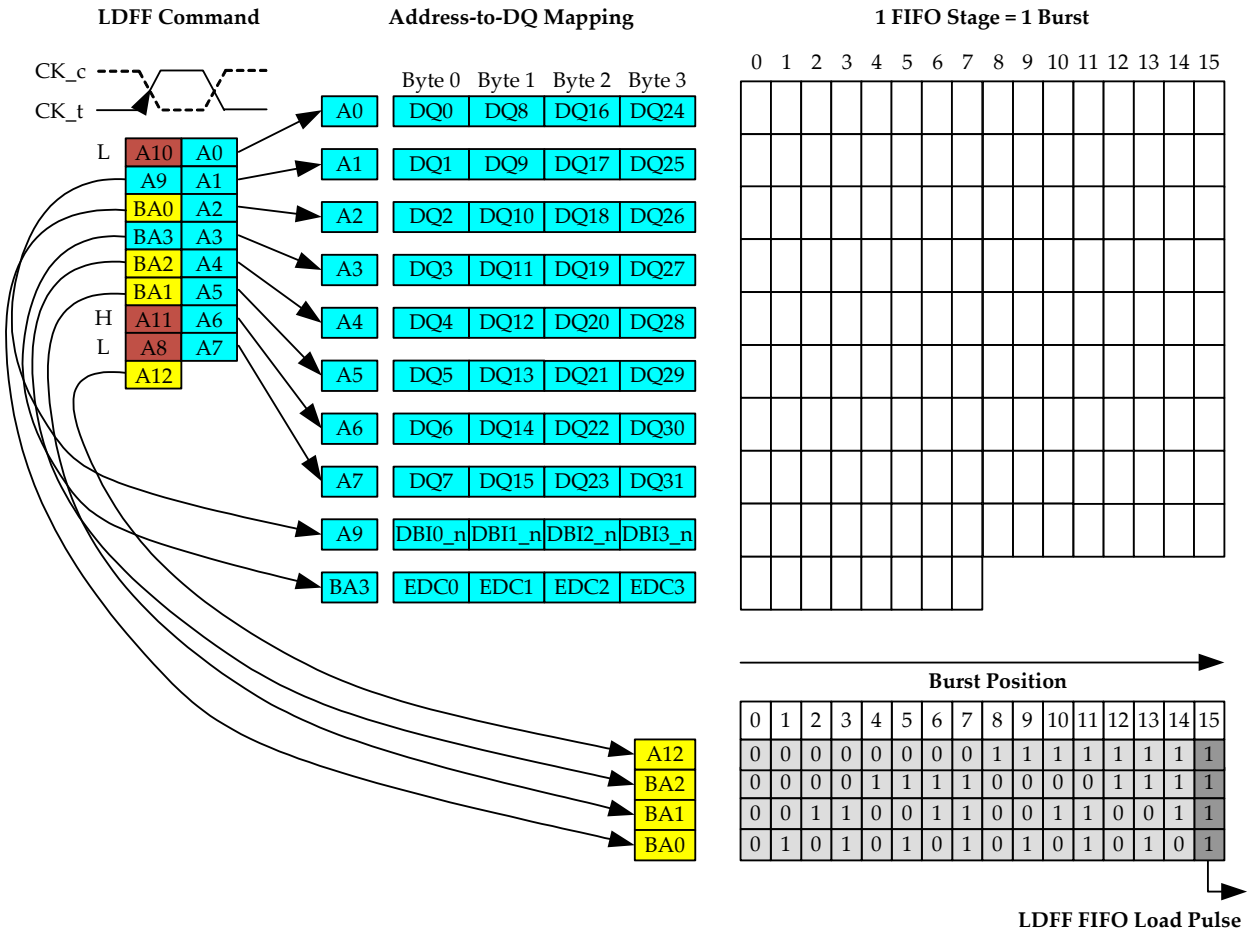


Figure 48 — LDFF Command Address to DQ/DBI_n/EDC Mapping in QDR Mode

6.4.1 LDFF Command (cont'd)

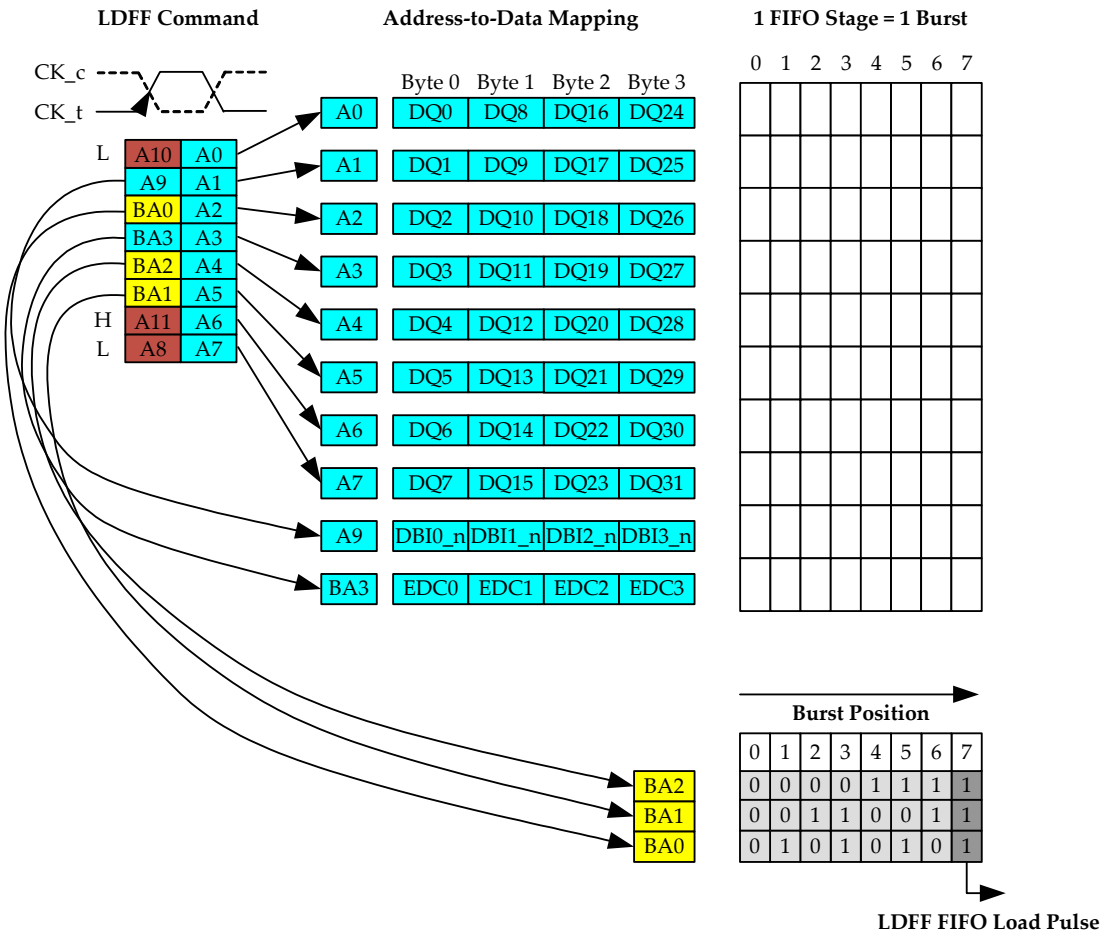


Figure 49 — LDFF Command Address to DQ/DBI_n/EDC Mapping in DDR Mode

LDFF loads the DBI FIFO regardless of the WDBI and RDBI mode register bits. It also loads the EDC FIFO regardless of the WRCRC and RDCRC mode register bits, and no CRC is calculated; however, RDBI and RDCRC must be enabled to read the DBI and EDC bits, respectively, with the RDTR command. The DQ/DBI_n output buffers remain in ODT state during LDFF, and the EDC hold pattern is driven on the EDC pins during LDFF (provided RDQS mode is not enabled).

All burst addresses 0 to 15 must be loaded; LDFF commands to burst address 0 to 14 may be issued in random order; the LDFF command to burst address 15 (LDFF15) must be the last of 16 consecutive LDFF commands, as it effectively loads the data into the FIFO and results in a FIFO pointer increment. Consecutive LDFF commands have to be spaced by at least t_{LTLTR}, and at least t_{LTLFTR} cycles are required after each LDFF command to burst address 15.

LDFF pattern may efficiently be replicated to the next FIFO stages by issuing consecutive LDFF commands to burst address 15 (with identical data pattern). The data pattern in the scratch memory for LDFF will be available until the first RDTR command. An amount of LDFF15 commands greater than the FIFO depth of 6 is allowed and results in a looping of the FIFO's data input.

The total number of LDFF15 commands modulo 6 must equal the total number of RDTR commands modulo 6 when used in conjunction with RDTR. No READ or WRITE commands are allowed between LDFF and RDTR.

Above rules apply to DDR mode as well, with the difference that the LDFF7 command instead of LDFF15 effectively loads the data into the FIFO and results in a FIFO pointer increment.

6.4.2 RDTR Command

An RDTR burst is initiated with a RDTR command as shown in Figure 50. No bank or column addresses are used as the data is read from the internal READ FIFO, not the memory array. The length of the burst initiated with a RDTR command depends on the selected mode: in QDR mode the burst length is sixteen for DQ/DBI_n and eight for EDC, and in DDR mode the burst length is eight for DQ/DBI_n/EDC. There is no interruption nor truncation of RDTR bursts.

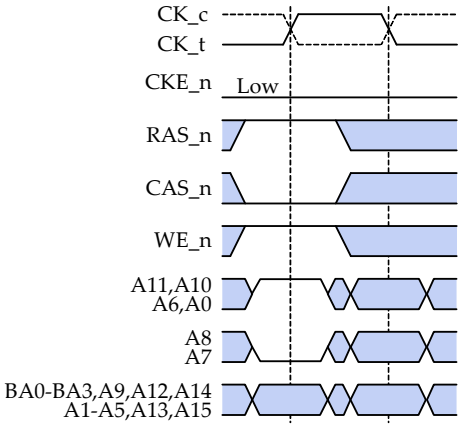


Figure 50 — RDTR Command

A RDTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

RDBI must be enabled to read the DBI FIFO bits with the RDTR command, otherwise the DBI_n pins remain in ODT state. The DBI_n pin behaves like a DQ, and no encoding with DBI is performed.

RDCRC must be enabled to read the EDC FIFO bits with the RDTR command, otherwise the EDC pins drive the EDC hold pattern. In RDQS mode the EDC pin functions like with a normal READ in that mode.

An amount of RDTR commands greater than the FIFO depth of 6 is allowed and results in a looping of the FIFO's data output.

During RDTR bursts, the first valid data-out element will be available after the read latency (RL) which is the same as for READ. EDC pin data come with the additional CRC read latency (CRCRL) after the RL.

Upon completion of a burst, assuming no other RDTR command has been initiated, all DQ and DBI_n pins will drive a High and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive High-Z.

Data from any RDTR burst may be concatenated with data from a subsequent RDTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new RDTR command should be issued after the first RDTR command according to the t_{CCDS} timing.

A WRTR can be issued any time after a RDTR command as long as the bus turn around time t_{RTW} is met.

The total number of RDTR commands modulo 6 must be equal to total number of WRTR commands modulo 6 when used in conjunction with WRTR. No READ or WRITE commands are allowed between WRTR and RDTR.

The total number of RDTR commands modulo 6 must be equal to the total number of LDFF commands to burst position 15 (LDFF15) modulo 6 when used in conjunction with LDFF. No READ or WRITE commands are allowed between LDFF and RDTR.

6.5 WRITE TRAINING

Write training allows the memory controller to find the data-eye center (symbol training) and burst frame location (frame training) for each high-speed input of the device. Each pin (DQ[31:0], DBI[3:0]_n) can be individually trained during this sequence.

For write training the following conditions must be true:

- at least one bank is active, or a REFRESH must be in progress and bit A2 in MR5 is set to 0 to allow training during refresh (to disable this special REFRESH enabling of the WCK clock tree an ACT command must be issued, or the device must be set to power-down or self refresh mode).
- WCK2CK training must be complete.
- the PLL/DLL must be locked, if enabled.
- Read training must be complete.
- RDBI and WDBI must both be either enabled or disabled prior to and during write training. They must be enabled if write training includes the DBI_n pins, and they must be disabled if write training does not include the DBI_n pins.
- RDCRC and WRCRC must both be either enabled or disabled prior to and during write training. They must be enabled if write training includes the EDC pins, and they must be disabled if write training does not include the EDC pins.

The following commands are associated with write training:

- WRTR to write a burst of data directly into the Read FIFO;
- RDTR to read a burst of data directly out of the Read FIFO.

Neither WRTR nor RDTR access the memory array. No MRS command is required to enter write training.

Figure 46 shows an example of the internal data paths used with WRTR and RDTR. A typical write training command sequence using WRTR and RDTR is illustrated in Figure 52. Table 21 lists AC timing parameters associated with write training.

Table 21 — WRTR and RDTR Timings

PARAMETER	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
ACTIVATE to RDTR command delay	t_{RCDRTR}		–	ns	
ACTIVATE to WRTR command delay	t_{RCDWTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
READ/WRITE bank A to READ/WRITE bank B command delay different bank groups	t_{CCDS}		–	t_{CK}	1
WRTR to RDTR command delay	t_{WTRTR}		–	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}		–	t_{CK}	
READ or RDTR to WRITE or WRTR command delay	t_{RTW}		–	ns	2

NOTE 1 Use t_{CCDS} for gapless consecutive WRTR and RDTR commands regardless whether Bank Groups is enabled or not.
NOTE 2 t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQO}$ and $t_{WCK2DQI}$ shall be considered in the calculation of the bus turnaround time.

6.5.1 WRTR Command

A WRTR burst is initiated with a WRTR command as shown in Figure 51. No bank or column addresses are used as the data is written to the internal READ FIFO, not the memory array. The length of the burst initiated with a WRTR command depends on the selected mode: in QDR mode the burst length is sixteen, and in DDR mode the burst length is eight. There is no interruption nor truncation of WRTR bursts.

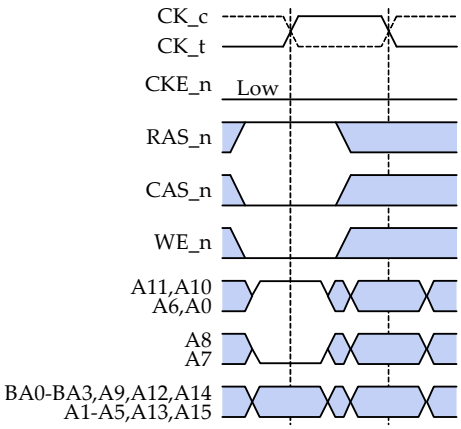


Figure 51 — WRTR Command

A WRTR command may only be issued when a bank is open or a refresh is in progress and bit A2 in MR5 is set to 0 to allow training during refresh.

WDBI must be enabled to write the DBI FIFO bits with the WRTR command, otherwise the DBI_n pins remain in ODT state and a 1 will be written to the DBI FIFO and be assumed for the DBI_n input in the CRC calculation.

WRCRC must be enabled to write the EDC FIFO bits with the WRTR command. In contrast to a normal WRITE, no CRC is returned by the WRTR command and the EDC pins will drive the EDC hold pattern. In RDQS mode the EDC pin functions like with a normal READ in that mode. Please note that RDCRC must be enabled to read the calculated CRC data with the RDTR command.

An amount of WRTR commands equal to the FIFO depth of 6 is required to fully load the Read FIFO; any number of WRTR commands greater than 6 is allowed and will result in a looping of the FIFO's data input.

During WRTR bursts, the first valid data-in element must be available at the input latch after the write latency (WL). The write latency is the same as for WRITE.

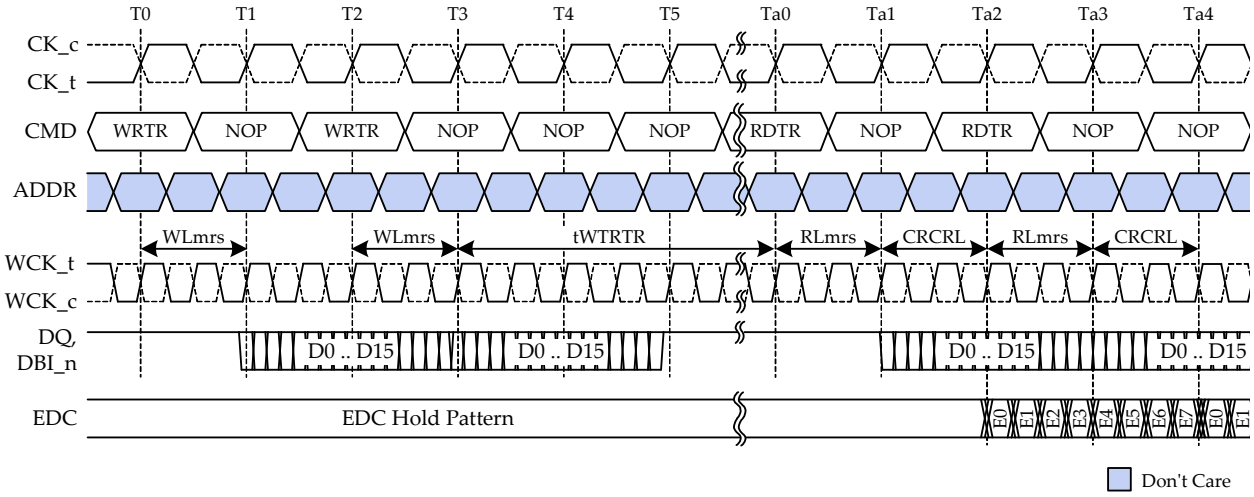
Upon completion of a burst, assuming no other WRTR data is expected on the bus the DQ and DBI_n pins will be driven according to the ODT state. Any additional input data will be ignored.

Data from any WRTR burst may be concatenated with data from a subsequent WRTR command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRTR command should be issued after the previous WRTR command according to the t_{CCDS} timing.

A RDTR can be issued any time after a WRTR command as long as the internal bus turn around time t_{RTWTR} is met.

The total number of WRTR commands modulo 6 must equal the total number of RDTR commands modulo 6 when used in conjunction with RDTR. No READ or WRITE commands are allowed between WRTR and RDTR.

6.5.1 WRTR Command (cont'd)



NOTE 1 D0..D15 = data burst with BL=16. E0..E7 = CRC burst with BL=8.

NOTE 2 WLmrs = 1, RLmrs = 1 and CRCRL = 1 are used for ease of illustration. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).

NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

NOTE 4 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.

NOTE 5 $t_{WCK2DQI}$, $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 52 — Write Training Using WRTR and RDTR Commands

7 OPERATION

7.1 COMMANDS

Table 22 — Truth Table - Commands

Operation	Symbol	CKE_n		RAS_n	CAS_n	WE_n	BA3	BA2-BA0	A13-A15	A12	A11	A10	A8	A7, A9	A6	A0-A5	Notes
		Previous cycle	Current cycle														
NO OPERATION	NOP	L	V	H	H	H	V	V	V	V	V	V	V	V	V	V	1, 2
MODE REGISTER SET	MRS	L	L	L	L	L	MRA		V	V	CODE						1, 2, 3
ACTIVATE	ACT	L	L	L	H	H	BA		RA								1, 2, 4
READ	RD	L	L	H	L	H	BA		CAU		L	L	L	CAU	CA	CAL	1, 2, 5, 10
READ with Autoprecharge	RDA	L	L	H	L	H	BA		CAU		L	L	H	CAU	CA	CAL	1, 2, 5
Load FIFO	LDFF	L	L	H	L	H	DATA	BST	V	BST	H	L	L	DATA			1, 2, 9
READ Training	RDTR	L	L	H	L	H	V	V	V	V	H	H	L	V	V	V	1, 2
WRITE without Mask	WOM	L	L	H	L	L	BA		CAU		L	L	L	CAU	CA	CAL	1, 2, 5
WRITE without Mask with Autoprecharge	WOMA	L	L	H	L	L	BA		CAU		L	L	H	CAU	CA	CAL	1, 2, 5
WRITE lower DQ	WOML	L	L	H	H	L	BA		V	V	L	L	L	V	CA	CAL	1, 2, 6
WRITE lower DQ with Autoprecharge	WOMLA	L	L	H	H	L	BA		V	V	L	L	H	V	CA	CAL	1, 2, 6
WRITE upper DQ	WOMU	L	L	H	H	L	BA		CAU		L	H	L	CAU	CA	CAL	1, 2, 7
WRITE upper DQ with Autoprecharge	WOMUA	L	L	H	H	L	BA		CAU		L	H	H	CAU	CA	CAL	1, 2, 7
WRITE with single-byte mask	WSM	L	L	H	L	L	BA		CAU		L	H	L	CAU	CA	CAL	1, 2, 5
WRITE with single-byte mask with Autoprecharge	WSMA	L	L	H	L	L	BA		CAU		L	H	H	CAU	CA	CAL	1, 2, 5
WRITE with double-byte mask	WDM	L	L	H	L	L	BA		CAU		H	L	L	CAU	CA	CAL	1, 2, 5
WRITE with double-byte mask with Autoprecharge	WDMA	L	L	H	L	L	BA		CAU		H	L	H	CAU	CA	CAL	1, 2, 5
WRITE Training	WRTR	L	L	H	L	L	V	V	V	V	H	H	L	V	V	V	1, 2
PRECHARGE	PRE	L	L	L	H	L	BA		V	V	V	V	L	V	V	V	1, 2
PRECHARGE ALL	PREALL	L	L	L	H	L	V	V	V	V	V	V	H	V	V	V	1, 2
PER-BANK REFRESH	REFPB	L	L	L	L	H	BA		V	V	V	V	L	V	V	V	1, 8
REFRESH	REFAB	L	L	L	L	H	V	V	V	V	V	V	H	V	V	V	1, 8
POWER-DOWN ENTRY	PDE	L	H	H	H	H	V	V	V	V	V	V	V	V	V	V	1
POWER-DOWN EXIT	PDX	H	L	H	H	H	V	V	V	V	V	V	V	V	V	V	1
SELF REFRESH ENTRY	SRE	L	H	L	L	H	V	V	V	V	V	V	V	V	V	V	1, 8
SELF REFRESH EXIT	SRX	H	L	H	H	H	V	V	V	V	V	V	V	V	V	V	1

NOTE 1 H = Logic High Level; L = Logic Low Level; V = Valid Signal (H or L, but not floating).
NOTE 2 Addresses shown are logical addresses; physical addresses are inverted when address bus inversion (ABI) is activated and ABI_n=L.
NOTE 3 BA0-BA3 provide the Mode Register address (MRA), A0-A11 the op-code to be loaded.
NOTE 4 BA0-BA3 provide the bank address (BA), A0-A12 (A13, A14, A15) provide the row address (RA).
NOTE 5 BA0-BA3 provide the bank address, A0-A5 provide the lower column address (CAL) and A7,A9,A12-A15 the upper column address (CAU) in QDR operating mode, and A6 an additional column address bit (CA) in DDR operating mode. No sub-word addressing within a burst of 16 or 8.
NOTE 6 BA0-BA3 provide the bank address, A0-A5 provide the column address (CAL) in QDR operating mode, and A6 an addition-al column address bit (CA) in DDR operating mode. No sub-word addressing within a burst of 16 or 8.
NOTE 7 BA0-BA3 provide the bank address, A7,A9,A12-A15 the column address (CAU) in QDR operating mode, and A6 an additional column address bit (CA) in DDR operating mode. With address compatibility mode enabled in MR8 bit A8, A0-A5 provide the column address instead of A7,A9,A12-A15. No sub-word addressing within a burst of 16 or 8.
NOTE 8 The command is REFRESH or PER-BANK REFRESH when CKE_n(n) = L and SELF REFRESH ENTRY when CKE_n(n) = H.
NOTE 9 BA0-BA2,A12 select the burst position (BST) in QDR operating mode, BA0-BA2 select the burst position (BST) in DDR operating mode, and A0-A9, BA3 provide the data (DATA) in both modes.
NOTE 10 In address training mode READ is decoded from the commands pins only with RAS_n = H, CAS_n = L, WE_n = H.

7.2 COMMAND, ADDRESS, AND WRITE DATA INPUT TIMINGS

Figure 53 illustrates the timings associated with the command and address inputs, and Figure 54 the timings associated with the write data inputs.

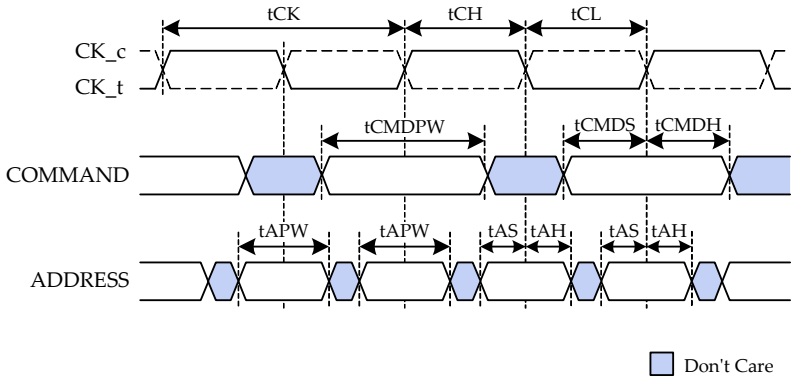


Figure 53 — Command and Address Input Timings

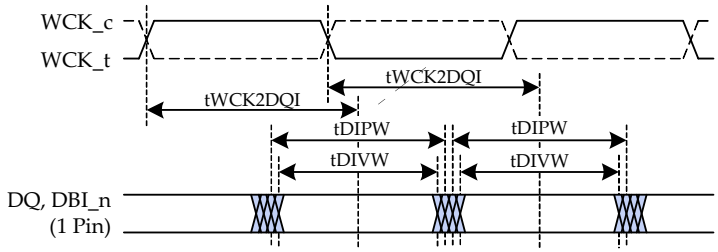


Figure 54 — Write Data Input Timings

7.3 NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the device to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

7.4 MODE REGISTER SET

The MODE REGISTER SET command is used to load the mode registers of the device. The bank address inputs BA[3:0] select the mode register, and address puts A[11:0] determine the op-code to be loaded. See MODE REGISTER for a register definition. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until t_{MRD} is met.

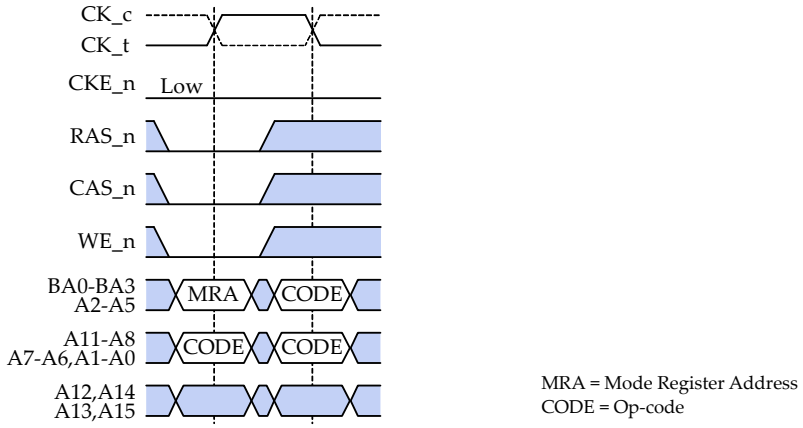


Figure 55 — MODE REGISTER SET Command

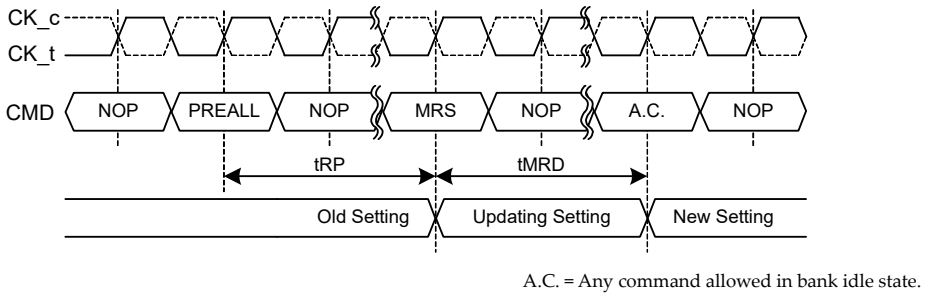


Figure 56 — Mode Register Set Timings

7.5 ROW ACTIVATION

Before any READ or WRITE command can be issued to a bank, a row in that bank must be opened. This is accomplished by the ACTIVATE command which selects both the bank and row to be activated. After a row is opened, a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification.

A subsequent ACTIVATE command to the same bank can only be issued after the previous row has been closed (precharged). The minimum time interval between two successive ACTIVATE commands on the same bank is defined by t_{RC}. A minimum time t_{RAS} must elapse between opening and closing a row.

A subsequent ACTIVATE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between two successive ACTIVATE commands to different banks is defined by t_{RRD}.

The row remains active until a PRECHARGE command (or READ or WRITE command with auto precharge) is issued to the bank.

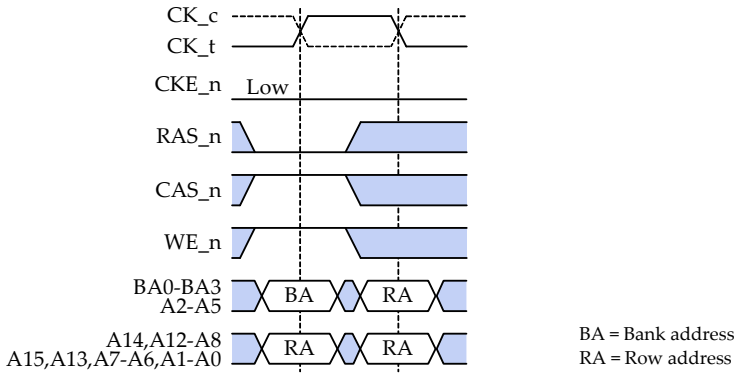
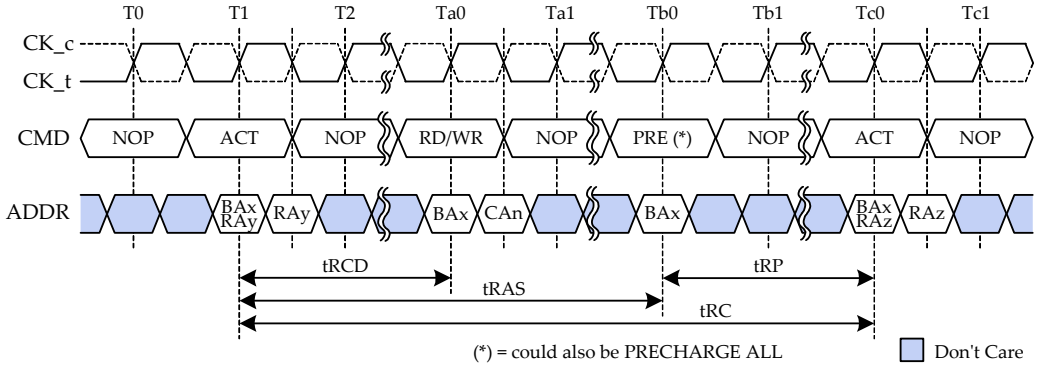


Figure 57 — ACTIVATE Command



NOTE 1 BA = bank address; CA = column address.
NOTE 2 $t_{RCD} = t_{RCDRD}$, t_{RCDWR}, t_{RCDRTR}, t_{RCDWTR} or t_{RCDLTR} depending on commands.

Figure 58 — Bank Activation Command Cycle

7.5.1 Bank Restrictions

Limiting the number of bank activations in a rolling window ensures that the instant current supply capability of the device is not exceeded. To reflect the short term capability of the GDDR5X SGRAM current supply, t_{FAW} (four activate window) is defined: no more than 4 banks may be activated in a rolling t_{FAW} window. To convert this to clocks, divide t_{FAW} (ns) by t_{CK} (ns) and round up to next integer. For example, if (t_{FAW}/t_{CK}) rounds up to 10 clocks and an ACTIVATE command is issued at clock N, no more than three further ACTIVATE commands may be issued at clocks N+1 through N+9 as illustrated in Figure 59.

7.5.1 Bank Restrictions (cont'd)

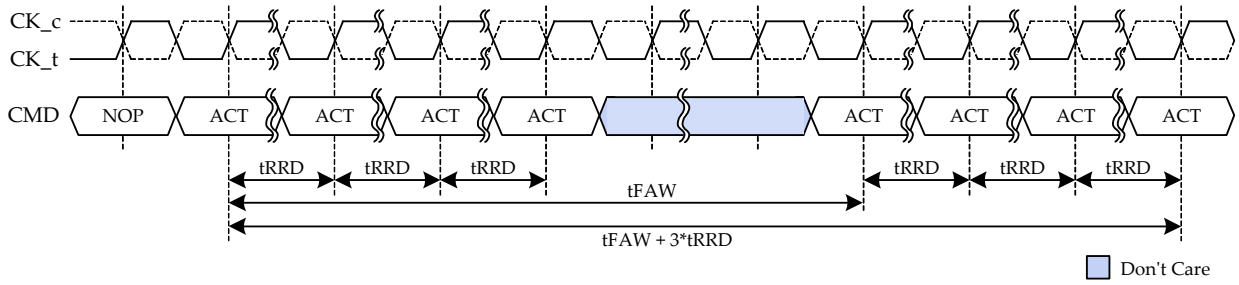


Figure 59 — t_{RRD} and t_{FAW} Timings

Parameter t_{32AW} (32 activate window) is defined to reflect a longer-term current supply capability. No more than 32 banks may be activated in a rolling t_{32AW} window. To convert this to clocks, divide t_{32AW} (ns) by t_{CK} (ns) and round up to next integer. Using a shorter and longer rolling activation window allows the GDDR5X SGRAM to handle higher currents in a shorter window and still limits the current strain over a longer period of time. Figure 60 illustrates cases where t_{32AW} is greater than or equals 8 * t_{FAW}.

It is preferable that GDDR5X SGRAMs have no rolling activation window restrictions (t_{FAW} = 4 * t_{RRD}).

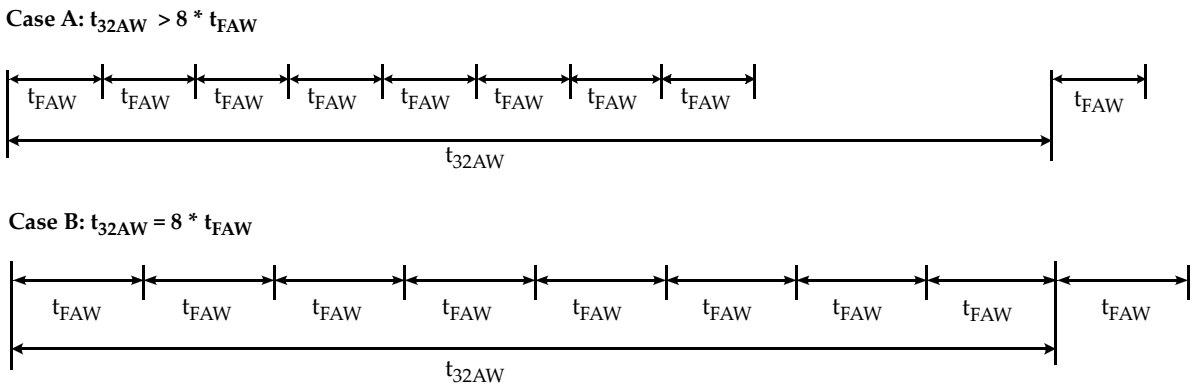


Figure 60 — t_{32AW} Timing

GDDR5X SGRAMs include a feature LP1 that allows DRAM vendors to relax t_{FAW} and t_{32AW} parameters to achieve lower power consumption. With LP1 t_{FAW} and t_{32AW} may have two values depending on whether LP1 is enabled or not. LP1 is controlled by MR5 bit A0.

7.6 WRITE (WOM)

WRITE bursts are initiated with a WRITE command as shown in Figure 61. The bank and column addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS}(min) has been met or after the number of clock cycles programmed in the RAS field of MR5 bits A[11:6], depending on the implementation choice per DRAM vendor. The length of the burst initiated with a WRITE command depends on the selected mode: in QDR mode the burst length is sixteen, and in DDR mode the burst length is eight. The column address is unique for this burst of sixteen or eight. There is no interruption nor truncation of WRITE bursts.

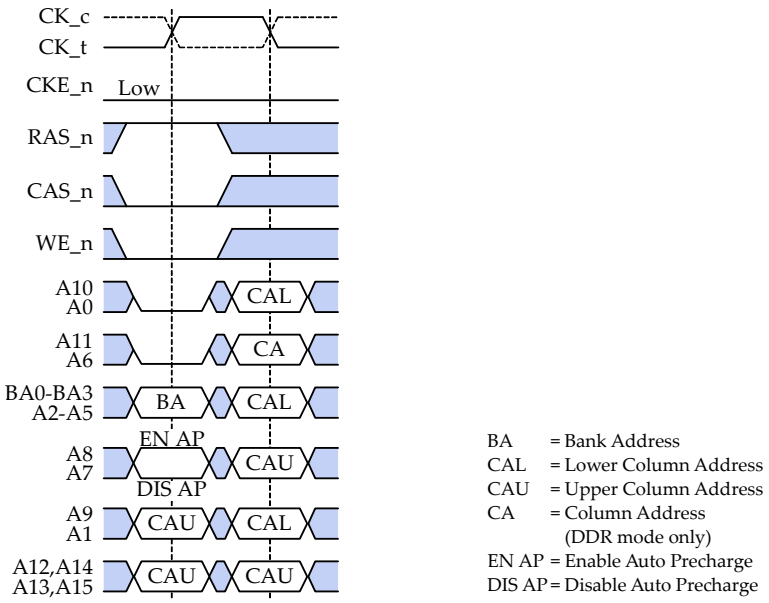


Figure 61 — WRITE Command

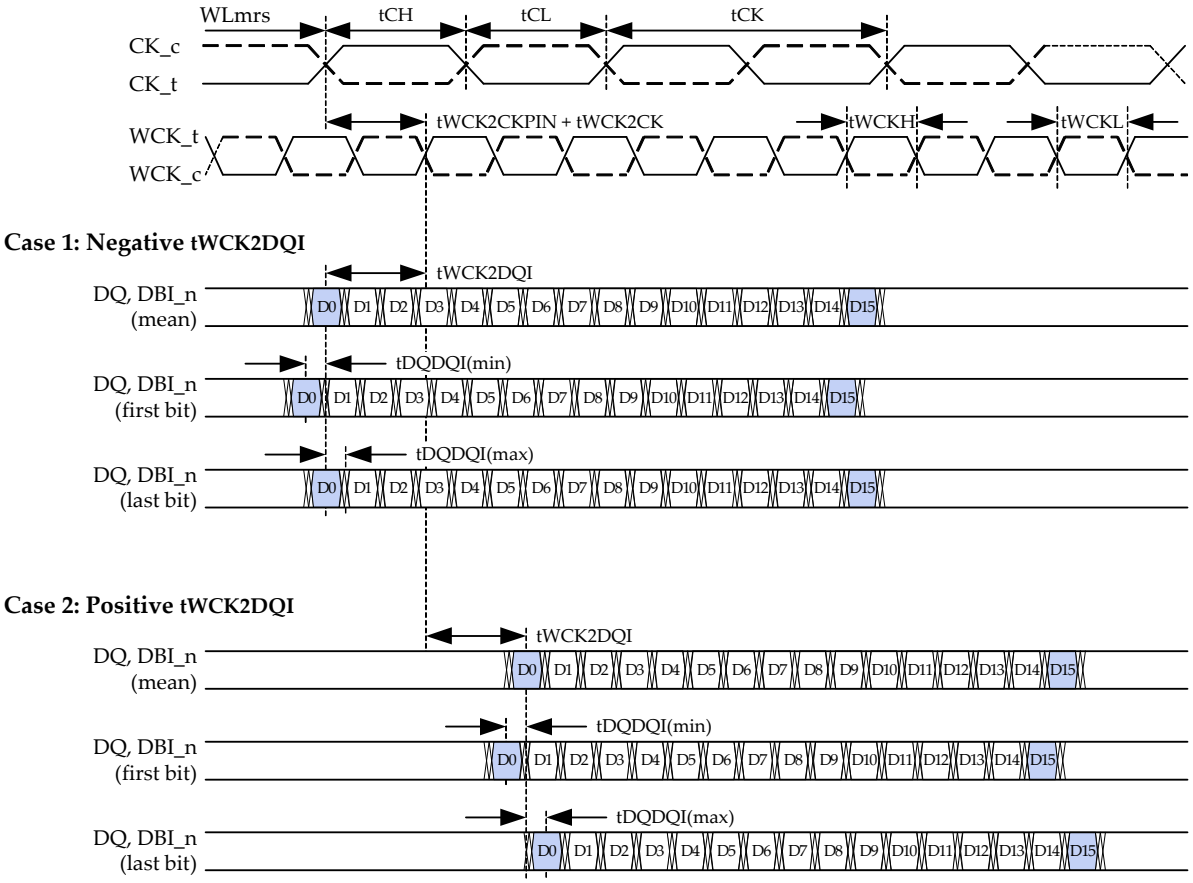
During WRITE bursts, the first valid data-in element must be available at the input latch after the write latency (WL). The write latency is defined as WLmrs * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQI}$, where WLmrs is the number of clock cycles programed in MR0, $t_{WCK2CKPIN}$ is the phase offset between WCK and CK at the pins when phase aligned at phase detector, t_{WCK2CK} is the alignment error between WCK and CK at the phase detector, and $t_{WCK2DQI}$ is the WCK to DQ/DBI_n offset as measured at the DRAM pins to ensure concurrent arrival at the latch. The total delay is relative to the data eye center averaged over one double-byte. The maximum skew within a double-byte is defined by t_{DQDQI}.

The data input valid window, t_{DIVW}, defines the time region when input data must be valid for reliable data capture at the receiver for any one worst-case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (i.e., within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL bandwidth. t_{DIVW} is measured at the pins and must be specified for each supported PLL/DLL bandwidth. In general t_{DIVW} is smaller than t_{DIPW}.

The data input pulse width, t_{DIPW}, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. t_{DIPW} is measured at the pins. In general t_{DIPW} is larger than t_{DIVW}.

WRITE word lane timings for QDR mode are illustrated in Figure 62, and WRITE word lane timings for DDR mode in Figure 63.

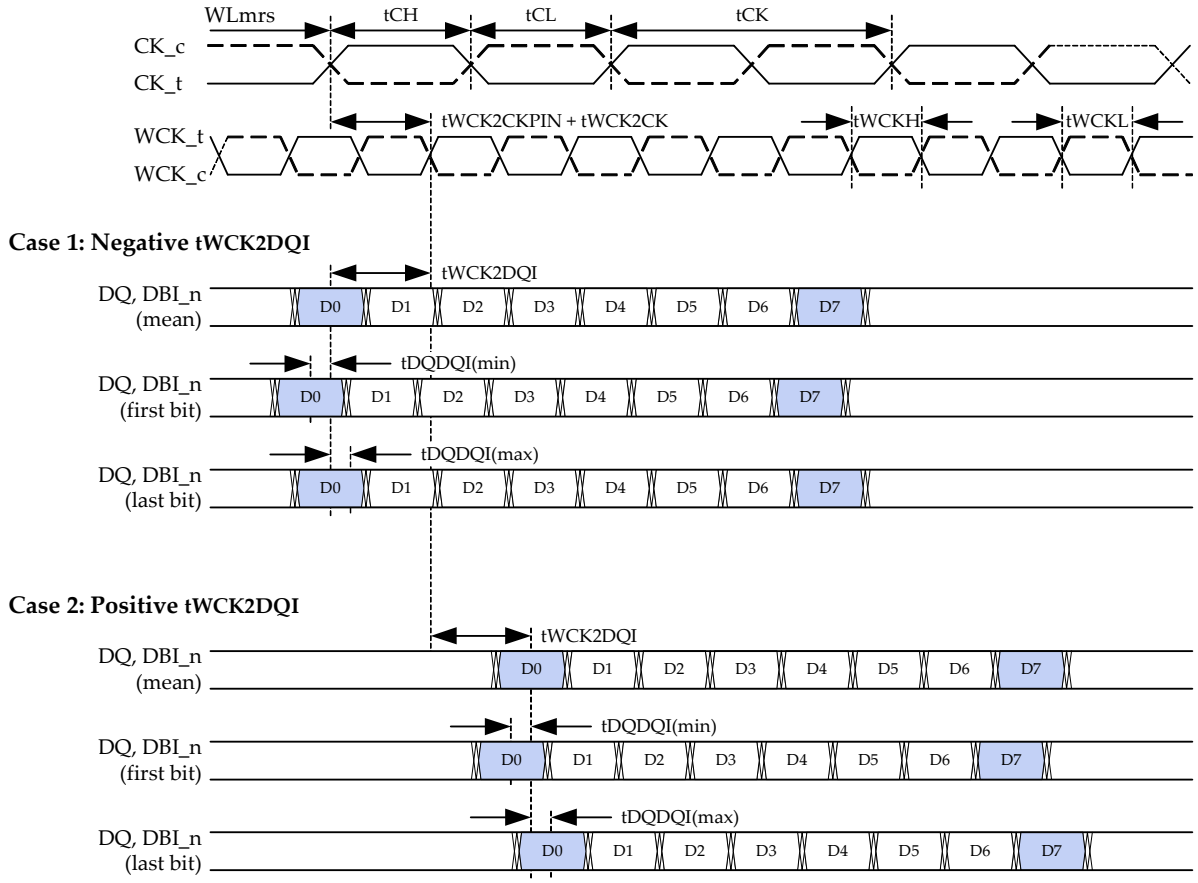
7.6 WRITE (WOM) (cont'd)



NOTE 1 WLmrs is the WRITE latency programmed in Mode Register MR0.
NOTE 2 Timings are shown with positive tWCK2CKPIN and tWCK2CK values. See WCK2CK timings for tWCK2CKPIN and tWCK2CK ranges.
NOTE 3 tWCK2DQI parameter values could be negative or positive numbers, depending on PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual tWCK2DQI value for stable WRITE operation.
NOTE 4 tDQDQI defines the minimum to maximum variation of tWCK2DQI within a double byte.
NOTE 5 Data Read timings are used for CRC return timing from WRITE commands with CRC enabled.

Figure 62 — WRITE Word Lane Timing in QDR Mode

7.6 WRITE (WOM) (cont'd)



NOTE 1 WLmrs is the WRITE latency programmed in Mode Register MR0.
NOTE 2 Timings are shown with positive tWCK2CKPIN and tWCK2CK values. See WCK2CK timings for tWCK2CKPIN and tWCK2CK ranges.
NOTE 3 tWCK2DQI parameter values could be negative or positive numbers, depending on PLL-on or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual tWCK2DQI value for stable WRITE operation.
NOTE 4 tDQDQI defines the minimum to maximum variation of tWCK2DQI within a double byte.
NOTE 5 Data Read timings are used for CRC return timing from WRITE commands with CRC enabled.

Figure 63 — WRITE Word Lane Timing in DDR Mode

Upon completion of a burst, assuming no other WRITE data is expected on the bus, the DQ and DBI_n pins are driven according to the ODT state and any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command.

Subsequent timing diagrams illustrate different cases of write operations. The figures are drawn for QDR mode; they also apply to DDR mode with the exception that the data burst of 16 (D0 .. D15) on the DQ/DBI_n pins is replaced by a data burst of 8 (D0 .. D7) as shown in Figure 66 for a single WRITE burst.

Data from any WRITE burst may be concatenated with data from a subsequent WRITE command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new WRITE command should be issued after the previous WRITE command according to the t_{CCD} timing. If that WRITE command is to another bank then an ACTIVATE command must precede the WRITE command and t_{RCDWR} also must be met.

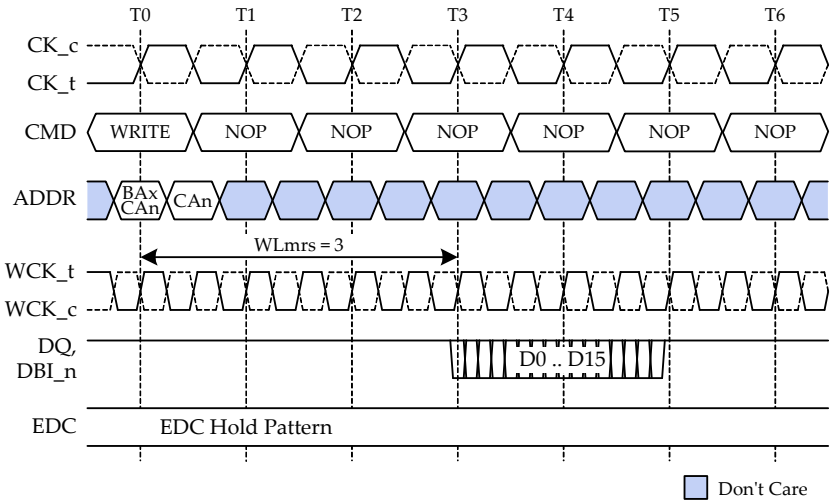
A READ can be issued any time after a WRITE command as long as the internal turn around time t_{WTR} is met. If that READ command is to another bank, then an ACTIVATE command must precede the READ command and t_{RCDRD} also must be met.

7.6 WRITE (WOM) (cont'd)

A PRECHARGE can also be issued after t_{WR} has been met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

The data inversion flag is received on the DBI_n pin. If DBI_n is Low, the data is stored after the inversion and is not inverted if DBI_n is High. WRITE data inversion can be enabled (A9 = 0) or disabled (A9 = 1) using WDBI in MR1.

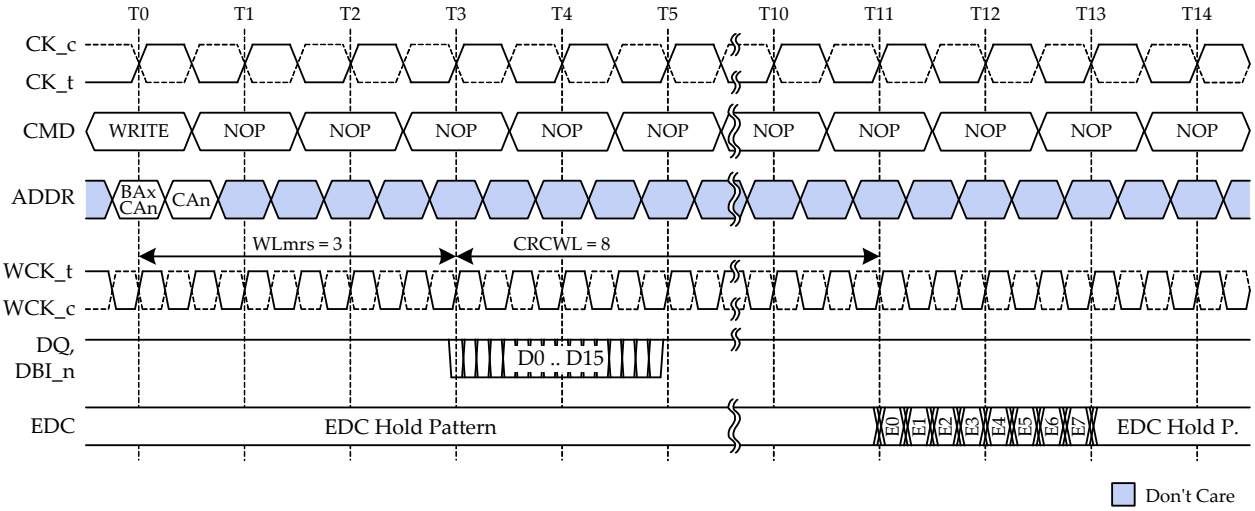
When enabled by the WRCRC flag in MR4, EDC data are returned to the controller with a latency of (WLmrs + CRCWL) * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CRCWL is the CRC write latency programmed in MR4 and $t_{WCK2DQO}$ is the WCK to DQ/DBI_n/EDC phase offset at the DRAM pins.



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 5 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 6 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

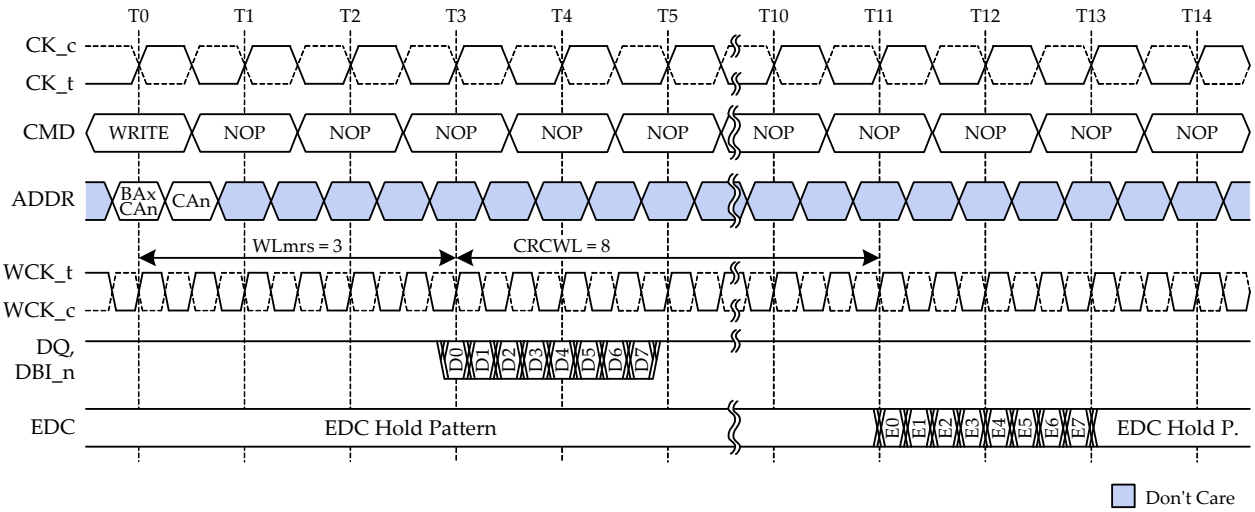
Figure 64 — Single WRITE without EDC

7.6 WRITE (WOM) (cont'd)



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16. E0..E7 = CRC burst with BL=8.
NOTE 2 WLmrs = 3 and CRCWL = 8 are shown as examples. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 5 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 6 $t_{WCK2DQI}$, $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

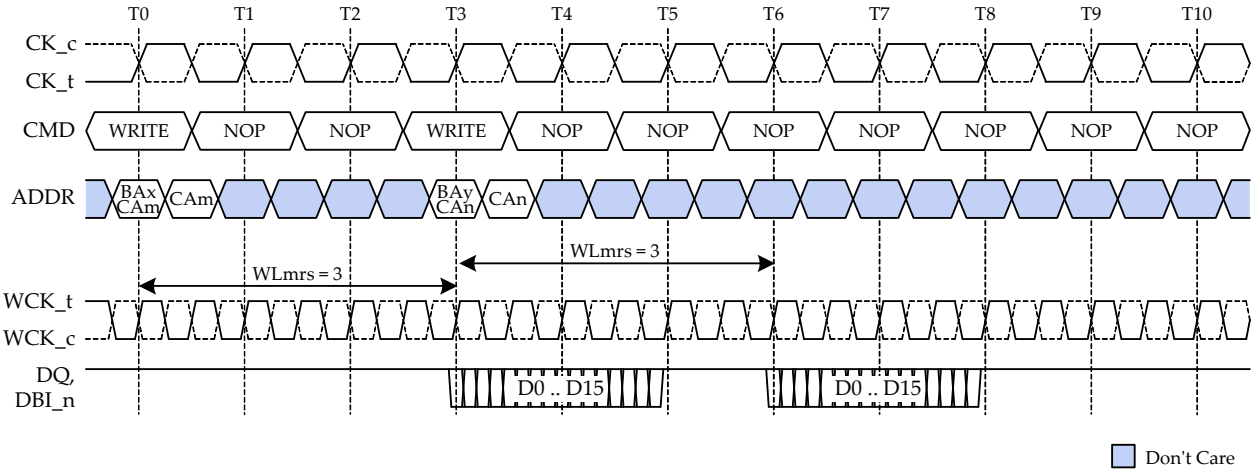
Figure 65 — Single WRITE with EDC



NOTE 1 BAx = bank address x; CAn = column address n. D0..D7 = data burst with BL=8. E0..E7 = CRC burst with BL=8.
NOTE 2 WLmrs = 3 and CRCWL = 8 are shown as examples. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 5 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 6 $t_{WCK2DQI}$, $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

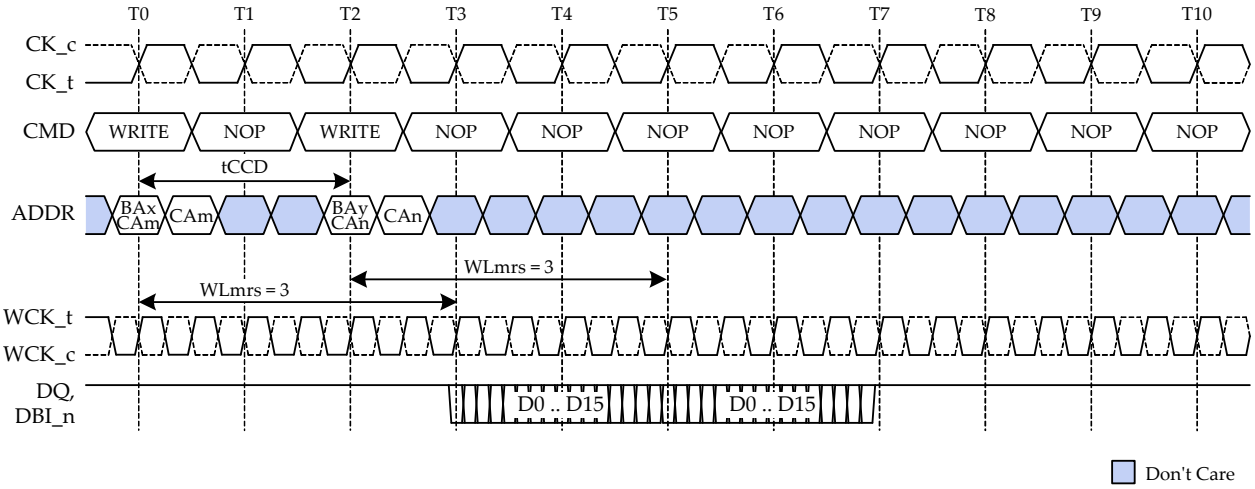
Figure 66 — Single WRITE with EDC in DDR Mode

7.6 WRITE (WOM) (cont'd)



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 t_{CCD} = t_{CCDL} when bank groups are enabled and both WRITEs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.
NOTE 6 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 7 An ACTIVATE (ACT) command is required to be issued before the WRITE commands, and t_{RCDWR} must be met.
NOTE 8 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

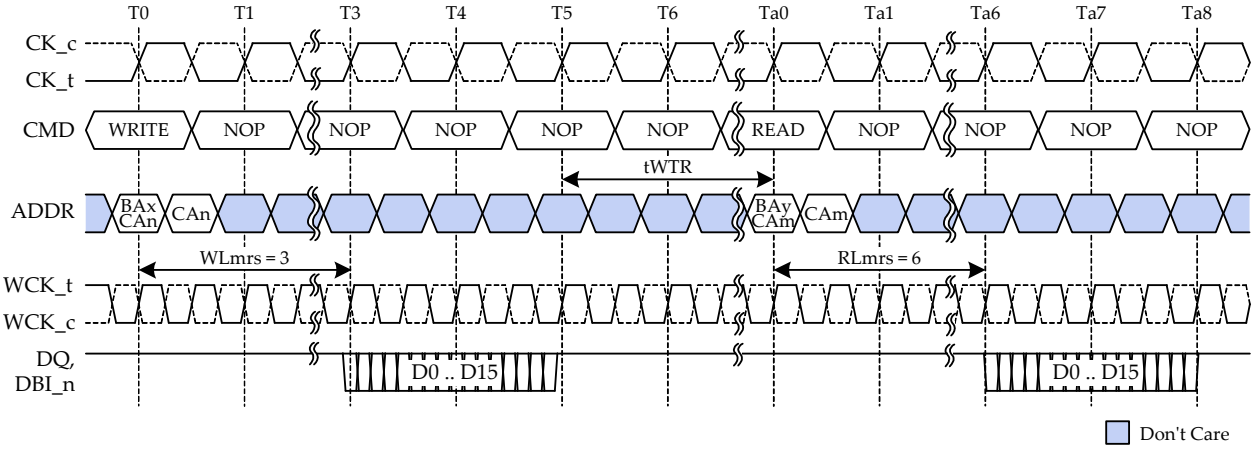
Figure 67 — Non-Gapless WRITEs



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 t_{CCD} = t_{CCDL} when bank groups are enabled and both WRITEs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.
NOTE 6 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 7 An ACTIVATE (ACT) command is required to be issued before the WRITE commands, and t_{RCDWR} must be met.
NOTE 8 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

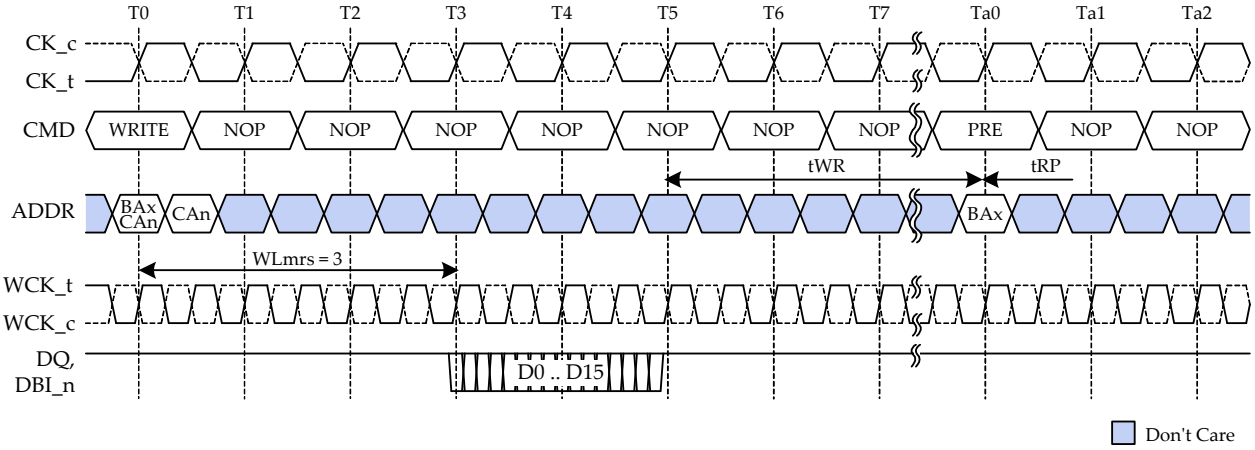
Figure 68 — Gapless WRITEs

7.6 WRITE (WOM) (cont'd)



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 and RLmrs = 6 are shown as examples.. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 $t_{WTR} = t_{WTRL}$ when bank groups is enabled and both WRITE and READ access banks in the same bank group, otherwise t_{WTR}=t_{WTRS}.
NOTE 6 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 7 An ACTIVATE (ACT) command is required to be issued before the WRITE and READ commands, and t_{RCDWR} or t_{RCDRD}, respectively, must be met.
NOTE 8 $t_{WCK2DQI}$, $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 69 — WRITE to READ



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 70 — WRITE to PRECHARGE

7.6.1 DQ Write Preamble

DQ write preamble may precede all WRITE bursts to condition the GDDR5X SGRAM's power system and data input receiver for better signal integrity on the initial data of a WRITE burst.

The actual preamble data pattern is not specified and may vary depending on system characteristics. All data received during DQ write preamble cycles are ignored.

7.7 WRITE LOWER and UPPER BYTES (WOML/WOMU)

The GDDR5X SGRAM adds two single-cycle WRITE commands that perform the same write operation as the WOM command but only on either the lower or uppper half of the data bus. The commands provide implicit data masking for the other half of the data bus; they reflect that consecutive blocks of data are favorably stored in memory locations associated with either CAL and CAU column addresses. The same data masking function can also be achieved by the use of the WDM command, but at the expense of an additional data mask cycle on the address/command bus.

- WOML: WRITE to lower bytes performs the same write as a WOM command except that write data are received on bytes 0 and 1 (WCK01 domain) only, while write data received on bytes 2 and 3 (WCK23 domain) are implicitly masked and ignored. The lower column address (CAL) is associated with the WOML command, and the upper column address (CAU) is ignored.
- WOMU: WRITE to upper bytes performs the same write as a WOM command except that write data are received on bytes 2 and 3 (WCK23 domain) only, while write data received on bytes 0 and 1 (WCK01 domain) are implicitly masked and ignored. The upper column address (CAU) is associated with the WOMU command, and the lower column address (CAL) is ignored. With address compatibility mode enabled, CAL becomes the valid column address.

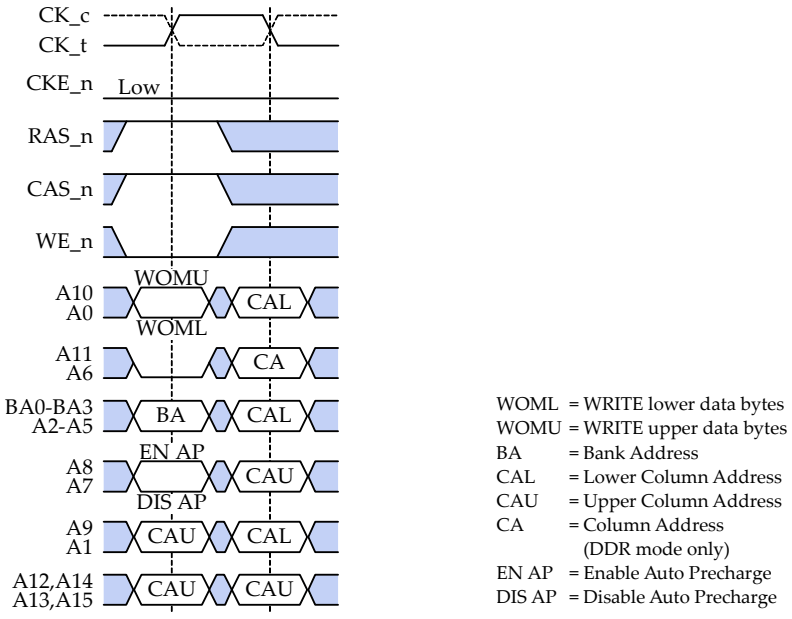
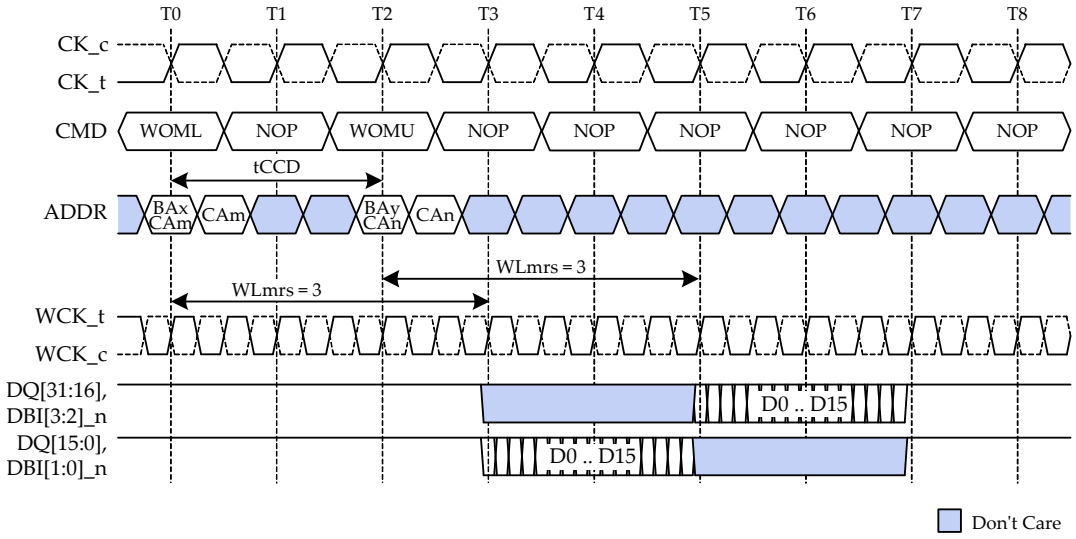


Figure 71 — WRITE Lower / Upper Bytes Commands

7.7 WRITE LOWER and UPPER BYTES (WOML/WOMU) (cont'd)

Figure 72 illustrates the use of the WOML and WOMU commands. The commands are also available in DDR operating mode, with the only difference that the commands initiate a write with a burst of 8.



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data burst with BL=16.

NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).

NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.

NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.

NOTE 5 t_{CCD} = t_{CCDL} when bank groups are enabled and both WRITEs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.

NOTE 6 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.

NOTE 7 An ACTIVATE (ACT) command is required to be issued before the WRITE commands, and t_{RCDWR} must be met.

NOTE 8 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 72 — WRITE Lower and Upper Bytes

7.8 WRITE DATA MASK (WDM/WSM)

The traditional method of using a DM pin for write data mask must be abandoned for a new method. Due to the high data rate of GDDR5X SGRAMs, bit errors are expected on the interface and are not recoverable when they occur on the traditional DM pin.

The write data mask is received over the address following the bank/column address cycle associated with the command, during the NOP command(s) between the WRITE command and the next command. The data mask is used to mask the corresponding data according to Table 23.

Table 23 — Data Mask States

FUNCTION	DM, LDM, UDM VALUE	DQ
Write Enable	0	Valid
Write Inhibit	1	Ignored

Two additional WRITE commands that augment the traditional WRITE Without Mask (WOM) are required for proper DM support.

- WDM: WRITE with double-byte mask is a two-cycle command where the first cycle carries address information and the second cycle carries data mask, Lower Lane Data Mask (LDM) and Upper Lane Data Mask (UDM) information as shown in Figure 73 and Table 25. The command provides quad-byte mask granularity when LDM and UDM are both set to 0. The command provides double-byte mask granularity on the upper two data bytes when LDM is set to 1 to inhibit writes on the lower two data bytes. Similarily, the command provides double-byte mask granularity on the lower two data bytes when UDM is set 1 to inhibit writes on the upper two data bytes.
- WSM: WRITE with single-byte mask is a three-cycle command where the first cycle carries address information and the second and third cycle carry data mask, Lower Lane Data Mask (LDM) and Upper Lane Data Mask (UDM) information as shown in Figure 74 and Table 26. The command provides double-byte mask granularity when LDM and UDM are both set to 0. The command provides single-byte mask granularity on the upper two data bytes when LDM is set to 1 to inhibit writes on the lower two data bytes. Similarily, the command provides single-byte mask granularity on the lower two data bytes when UDM is set 1 to inhibit writes on the upper two data bytes.

Table 24 summarizes the options using UDM and LDM in conjunction with WDM and WSM commands.

Table 24 — Use of UDM and LDM with WDM and WSM Commands in QDR Mode

UDM	LDM	DQ[31:16]	DQ[15:0]
0	0	Write determined by DM bits	
0	1	Write determined by DM bits	Write Inhibit
1	0	Write Inhibit	Write determined by DM bits
1	1	Reserved	

7.8 WRITE DATA MASK (WDM/WSM) (cont'd)

The following timing diagrams illustrate the use of LDM and UDM for lane masking in detail:

- Figure 75 and Figure 77 illustrate the use of the LDM and UDM to achieve double-byte and single-byte granularity with WDM and WSM commands, respectively. Both figures show two seamless WDM and WSM commands. A12 (LDM) is set to 0 and A13 (UDM) is set to 1 along with the first WDM or WSM command; the DM bits are applied to the lower two data bytes only while writes to the upper two data bytes are masked by UDM. A12 and A13 are then set to opposite values along with the second WDM and WSM command; the data mask bits are applied to the upper two data bytes only while writes to the lower two data bytes are masked by LDM.
- Figure 76 and Figure 78 illustrate WDM and WSM commands without LDM or UDM to achieve quad-byte and double-byte granularity, respectively. The figures show single WDM and WSM commands with A12 and A13 both set to 0. The DM bits are applied to all four data bytes.

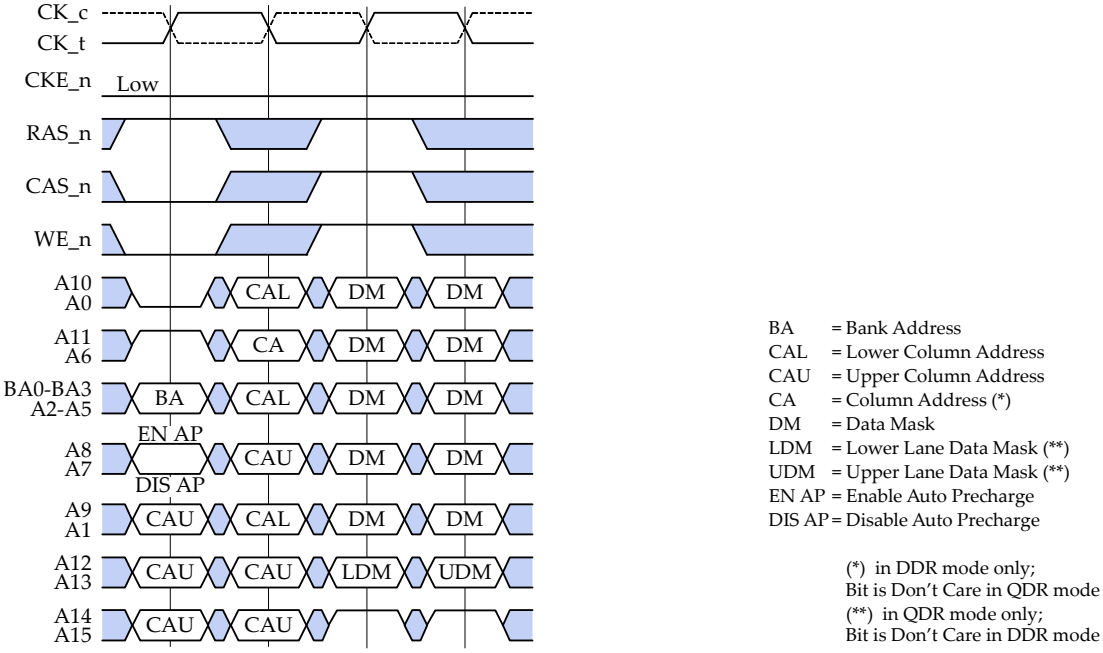


Figure 73 — WRITE-With-Doublebyte-Mask Command

7.8 WRITE DATA MASK (WDM/WSM) (cont'd)

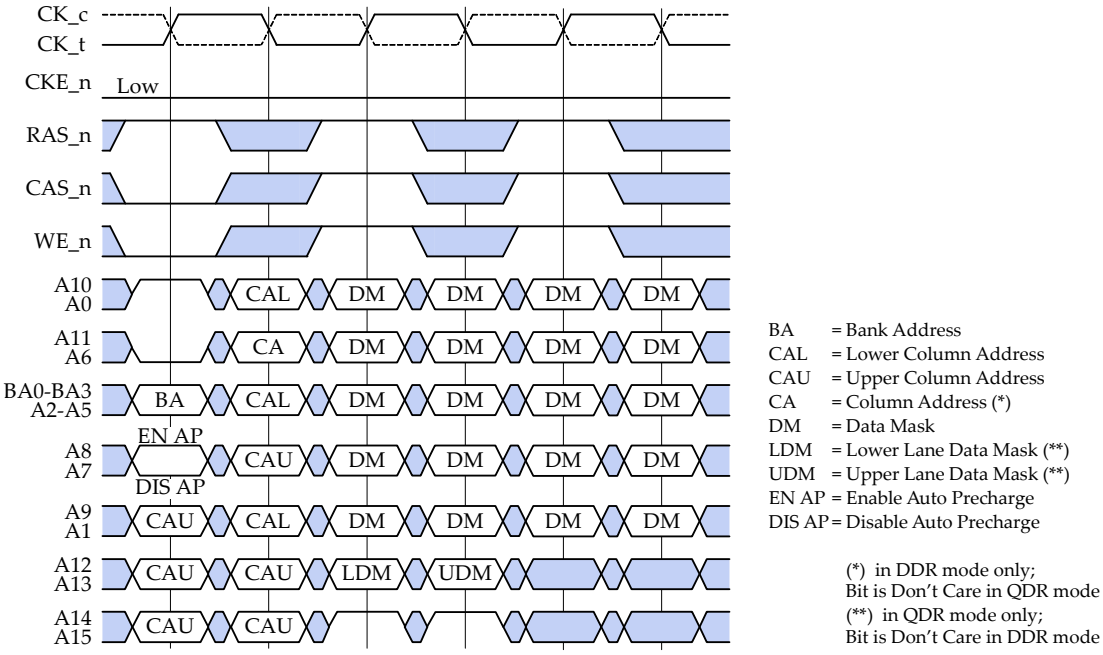


Figure 74 — WRITE-With-Singlebyte-Mask Command

7.8 WRITE DATA MASK (WDM/WSM) (cont'd)

Table 25 — WDM Mapping (QDR Mode)

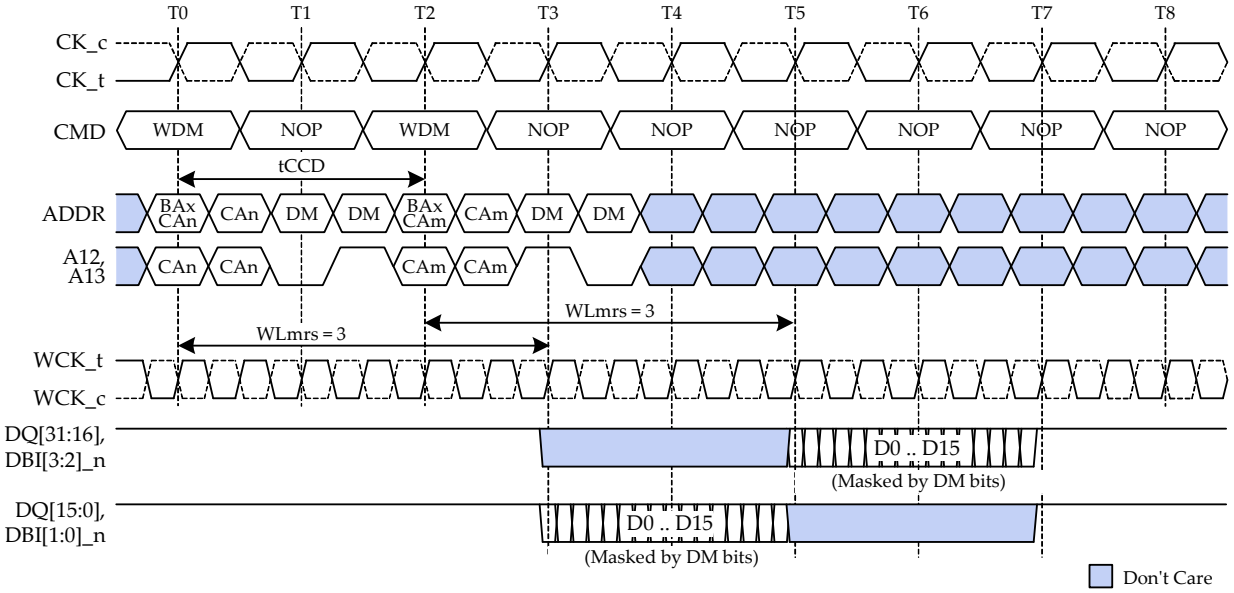
Byte and Burst Position Masked during WDM					
A12 = 0, A13 = 0					
	ADD CK_t Rising Edge			ADD CK_c Rising Edge	
ADD	Byte	Burst	ADD	Byte	Burst
A10	DQ[31:0]	0	A0	DQ[31:0]	4
A9	DQ[31:0]	1	A1	DQ[31:0]	5
BA0	DQ[31:0]	2	A2	DQ[31:0]	6
BA3	DQ[31:0]	3	A3	DQ[31:0]	7
BA2	DQ[31:0]	8	A4	DQ[31:0]	12
BA1	DQ[31:0]	9	A5	DQ[31:0]	13
A11	DQ[31:0]	10	A6	DQ[31:0]	14
A8	DQ[31:0]	11	A7	DQ[31:0]	15
A12 = 0, A13 = 1					
	ADD CK_t Rising Edge			ADD CK_c Rising Edge	
ADD	Byte	Burst	ADD	Byte	Burst
A10	DQ[15:0]	0	A0	DQ[15:0]	4
A9	DQ[15:0]	1	A1	DQ[15:0]	5
BA0	DQ[15:0]	2	A2	DQ[15:0]	6
BA3	DQ[15:0]	3	A3	DQ[15:0]	7
BA2	DQ[15:0]	8	A4	DQ[15:0]	12
BA1	DQ[15:0]	9	A5	DQ[15:0]	13
A11	DQ[15:0]	10	A6	DQ[15:0]	14
A8	DQ[15:0]	11	A7	DQ[15:0]	15
A12 = 1, A13 = 0					
	ADD CK_t Rising Edge			ADD CK_c Rising Edge	
ADD	Byte	Burst	ADD	Byte	Burst
A10	DQ[31:16]	0	A0	DQ[31:16]	4
A9	DQ[31:16]	1	A1	DQ[31:16]	5
BA0	DQ[31:16]	2	A2	DQ[31:16]	6
BA3	DQ[31:16]	3	A3	DQ[31:16]	7
BA2	DQ[31:16]	8	A4	DQ[31:16]	12
BA1	DQ[31:16]	9	A5	DQ[31:16]	13
A11	DQ[31:16]	10	A6	DQ[31:16]	14
A8	DQ[31:16]	11	A7	DQ[31:16]	15
A12 = 1, A13 = 1					
	ADD CK_t Rising Edge			ADD CK_c Rising Edge	
ADD	Byte	Burst	ADD	Byte	Burst
Reserved					

7.8 WRITE DATA MASK (WDM/WSM) (cont'd)

Table 26 — WSM Mapping (QDR Mode)

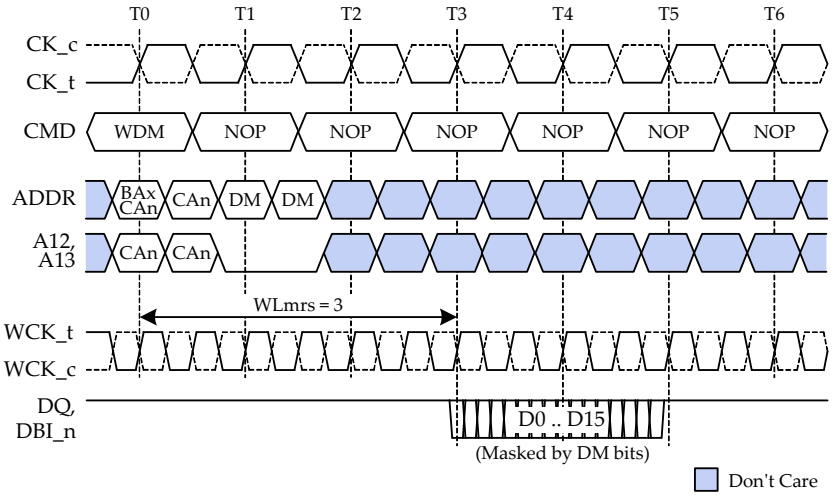
Byte and Burst Position Masked during WSM												
A12 = 0, A13 = 0												
	ADD CK_t 1st Rising Edge			ADD CK_c 1st Rising Edge			ADD CK_t 2nd Rising Edge			ADD CK_c 2nd Rising Edge		
ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	
A10	DQ[31:24,7:0]	0	A0	DQ[31:24,7:0]	4	A10	DQ[23:8]	0	A0	DQ[23:8]	4	
A9	DQ[31:24,7:0]	1	A1	DQ[31:24,7:0]	5	A9	DQ[23:8]	1	A1	DQ[23:8]	5	
BA0	DQ[31:24,7:0]	2	A2	DQ[31:24,7:0]	6	BA0	DQ[23:8]	2	A2	DQ[23:8]	6	
BA3	DQ[31:24,7:0]	3	A3	DQ[31:24,7:0]	7	BA3	DQ[23:8]	3	A3	DQ[23:8]	7	
BA2	DQ[31:24,7:0]	8	A4	DQ[31:24,7:0]	12	BA2	DQ[23:8]	8	A4	DQ[23:8]	12	
BA1	DQ[31:24,7:0]	9	A5	DQ[31:24,7:0]	13	BA1	DQ[23:8]	9	A5	DQ[23:8]	13	
A11	DQ[31:24,7:0]	10	A6	DQ[31:24,7:0]	14	A11	DQ[23:8]	10	A6	DQ[23:8]	14	
A8	DQ[31:24,7:0]	11	A7	DQ[31:24,7:0]	15	A8	DQ[23:8]	11	A7	DQ[23:8]	15	
A12 = 0, A13 = 1												
	ADD CK_t 1st Rising Edge			ADD CK_c 1st Rising Edge			ADD CK_t 2nd Rising Edge			ADD CK_c 2nd Rising Edge		
ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	
A10	DQ[7:0]	0	A0	DQ[7:0]	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4	
A9	DQ[7:0]	1	A1	DQ[7:0]	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5	
BA0	DQ[7:0]	2	A2	DQ[7:0]	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6	
BA3	DQ[7:0]	3	A3	DQ[7:0]	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7	
BA2	DQ[7:0]	8	A4	DQ[7:0]	12	BA2	DQ[15:8]	8	A4	DQ[15:8]	12	
BA1	DQ[7:0]	9	A5	DQ[7:0]	13	BA1	DQ[15:8]	9	A5	DQ[15:8]	13	
A11	DQ[7:0]	10	A6	DQ[7:0]	14	A11	DQ[15:8]	10	A6	DQ[15:8]	14	
A8	DQ[7:0]	11	A7	DQ[7:0]	15	A8	DQ[15:8]	11	A7	DQ[15:8]	15	
A12 = 1, A13 = 0												
	ADD CK_t 1st Rising Edge			ADD CK_c 1st Rising Edge			ADD CK_t 2nd Rising Edge			ADD CK_c 2nd Rising Edge		
ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	
A10	DQ[31:24]	0	A0	DQ[31:24]	4	A10	DQ[23:16]	0	A0	DQ[23:16]	4	
A9	DQ[31:24]	1	A1	DQ[31:24]	5	A9	DQ[23:16]	1	A1	DQ[23:16]	5	
BA0	DQ[31:24]	2	A2	DQ[31:24]	6	BA0	DQ[23:16]	2	A2	DQ[23:16]	6	
BA3	DQ[31:24]	3	A3	DQ[31:24]	7	BA3	DQ[23:16]	3	A3	DQ[23:16]	7	
BA2	DQ[31:24]	8	A4	DQ[31:24]	12	BA2	DQ[23:16]	8	A4	DQ[23:16]	12	
BA1	DQ[31:24]	9	A5	DQ[31:24]	13	BA1	DQ[23:16]	9	A5	DQ[23:16]	13	
A11	DQ[31:24]	10	A6	DQ[31:24]	14	A11	DQ[23:16]	10	A6	DQ[23:16]	14	
A8	DQ[31:24]	11	A7	DQ[31:24]	15	A8	DQ[23:16]	11	A7	DQ[23:16]	15	
A12 = 1, A13 = 1												
	ADD CK_t 1st Rising Edge			ADD CK_c 1st Rising Edge			ADD CK_t 2nd Rising Edge			ADD CK_c 2nd Rising Edge		
ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	
Reserved												

7.8 WRITE DATA MASK (WDM/WSM) (cont'd)



NOTE 1 BAx = bank address x; CAn,m = column address n,m. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE commands, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

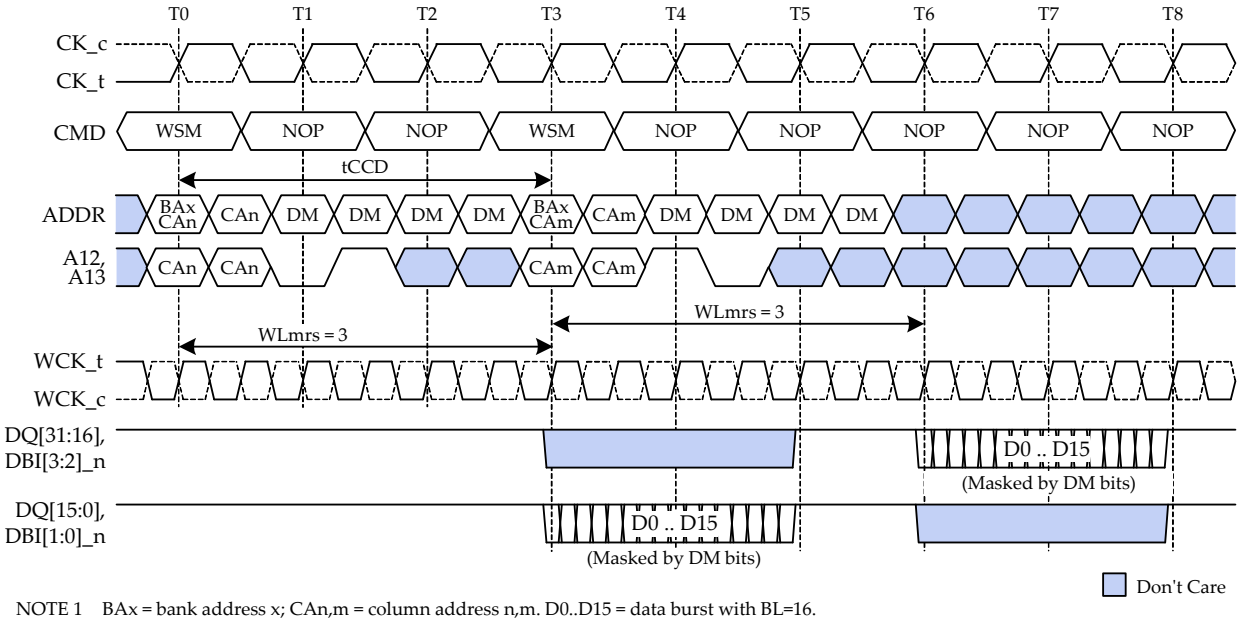
Figure 75 — WDM Timing with Byte Lane Masking



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

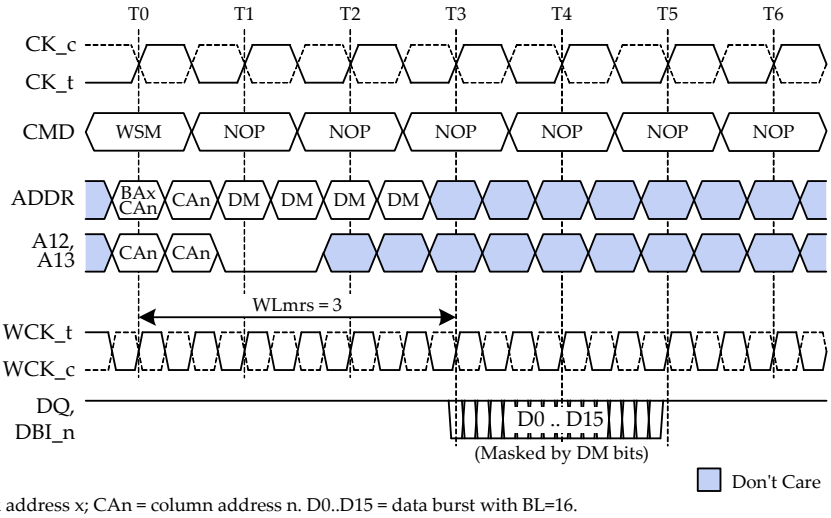
Figure 76 — WDM Timing without Byte Lane Masking

7.8 WRITE DATA MASK (WDM/WSM) (cont'd)



NOTE 1 BAx = bank address x; CAn,m = column address n,m. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE commands, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 77 — WSM Timing with Byte Lane Masking



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 78 — WSM Timing without Byte Lane Masking

7.8.1 Write with Data Mask (DM) in DDR Operating Mode

No LDM or UDM bits are associated with WDM and WSM commands in DDR operating mode, making address bits A12 and A13 Don't Care. The data mask information is applied according to Table 27 and Table 28.

Figure 79 and Figure 80 illustrate WDM and WSM commands in DDR operating mode.

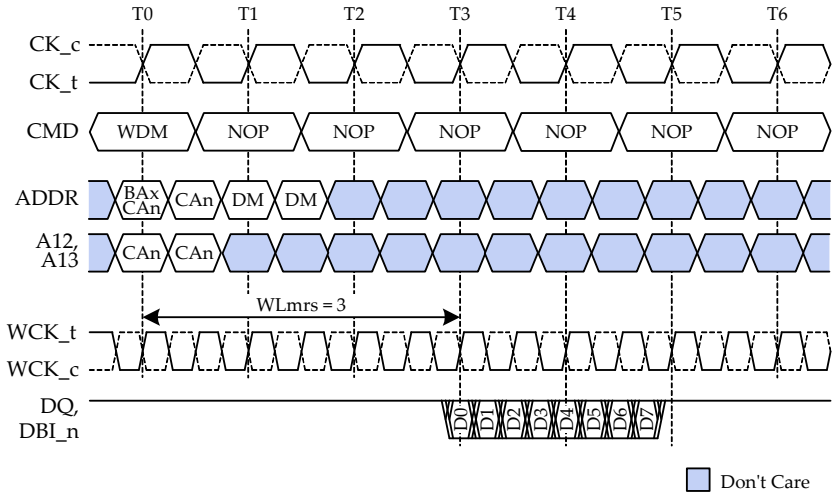
Table 27 — WDM Mapping (DDR Mode)

Byte and Burst Position Masked during WDM					
	ADD CK_t Rising Edge			ADD CK_c Rising Edge	
ADD	Byte	Burst	ADD	Byte	Burst
A10	DQ[15:0]	0	A0	DQ[15:0]	4
A9	DQ[15:0]	1	A1	DQ[15:0]	5
BA0	DQ[15:0]	2	A2	DQ[15:0]	6
BA3	DQ[15:0]	3	A3	DQ[15:0]	7
BA2	DQ[31:16]	0	A4	DQ[31:16]	4
BA1	DQ[31:16]	1	A5	DQ[31:16]	5
A11	DQ[31:16]	2	A6	DQ[31:16]	6
A8	DQ[31:16]	3	A7	DQ[31:16]	7

Table 28 — WSM Mapping (DDR Mode)

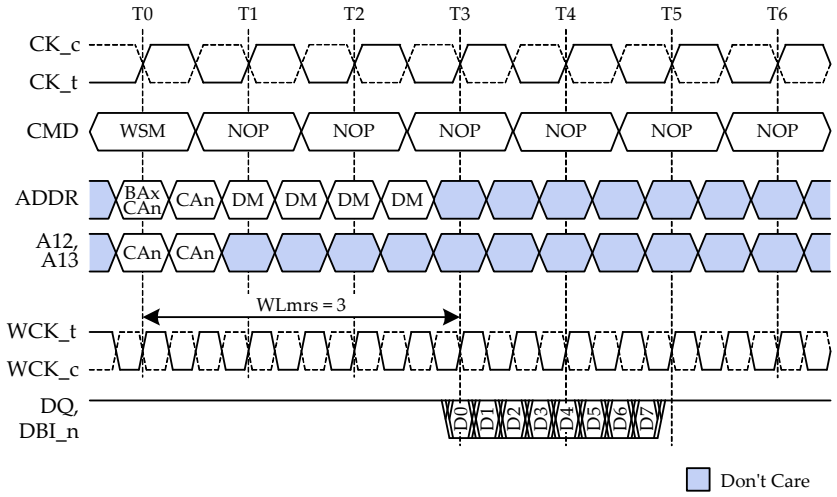
Byte and Burst Position Masked during WSM											
	ADD CK_t 1st Rising Edge			ADD CK_c 1st Rising Edge			ADD CK_t 2nd Rising Edge			ADD CK_c 2nd Rising Edge	
ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst	ADD	Byte	Burst
A10	DQ[7:0]	0	A0	DQ[7:0]	4	A10	DQ[15:8]	0	A0	DQ[15:8]	4
A9	DQ[7:0]	1	A1	DQ[7:0]	5	A9	DQ[15:8]	1	A1	DQ[15:8]	5
BA0	DQ[7:0]	2	A2	DQ[7:0]	6	BA0	DQ[15:8]	2	A2	DQ[15:8]	6
BA3	DQ[7:0]	3	A3	DQ[7:0]	7	BA3	DQ[15:8]	3	A3	DQ[15:8]	7
BA2	DQ[23:16]	0	A4	DQ[23:16]	4	BA2	DQ[31:24]	0	A4	DQ[31:24]	4
BA1	DQ[23:16]	1	A5	DQ[23:16]	5	BA1	DQ[31:24]	1	A5	DQ[31:24]	5
A11	DQ[23:16]	2	A6	DQ[23:16]	6	A11	DQ[31:24]	2	A6	DQ[31:24]	6
A8	DQ[23:16]	3	A7	DQ[23:16]	7	A8	DQ[31:24]	3	A7	DQ[31:24]	7

7.8.1 Write with Data Mask (DM) in DDR Operating Mode (cont'd)



NOTE 1 BAx = bank address x; CAn = column address n. D0..D7 = data burst with BL=8.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 79 — WDM Timing in DDR Mode



NOTE 1 BAx = bank address x; CAn = column address n. D0..D7 = data burst with BL=8.
NOTE 2 WLmrs = 3 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 For WRITE operations it is important that the latching point meets the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the WRITE command, and t_{RCDWR} must be met.
NOTE 7 $t_{WCK2DQI}$ = 0 is shown for illustration purposes.

Figure 80 — WSM Timing in DDR Mode

7.9 READ

A READ burst is initiated with a READ command as shown in Figure 81. The bank and column addresses are provided with the READ command and auto precharge is either enabled or disabled for that access with the A8 address. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS}(min) has been met or after the number of clock cycles programmed in the RAS field of MR5 bits A[11:6], depending on the implementation choice per DRAM vendor. The length of the burst initiated with a READ command depends on the selected mode: in QDR mode the burst length is sixteen for DQ/DBI_n and eight for EDC, and in DDR mode the burst length is eight for DQ/DBI_n/EDC. The column address is unique for this burst of sixteen or eight. There is no interruption nor truncation of READ bursts.

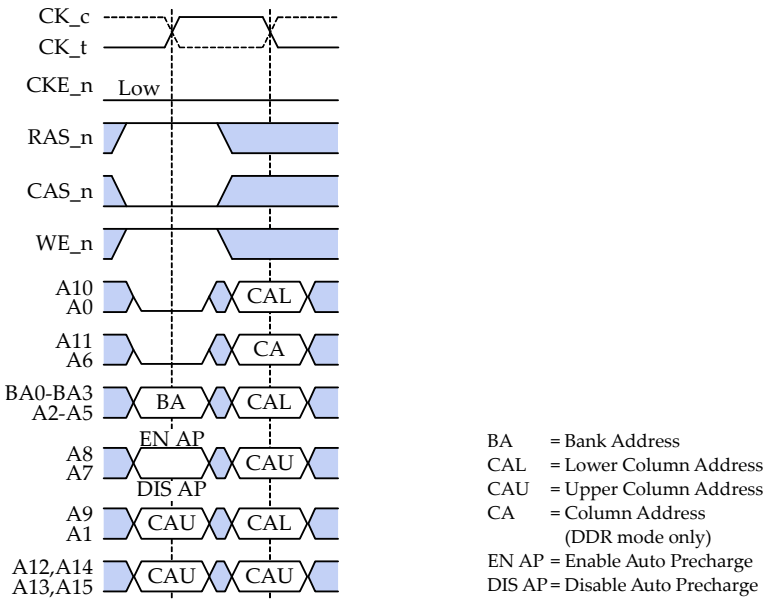
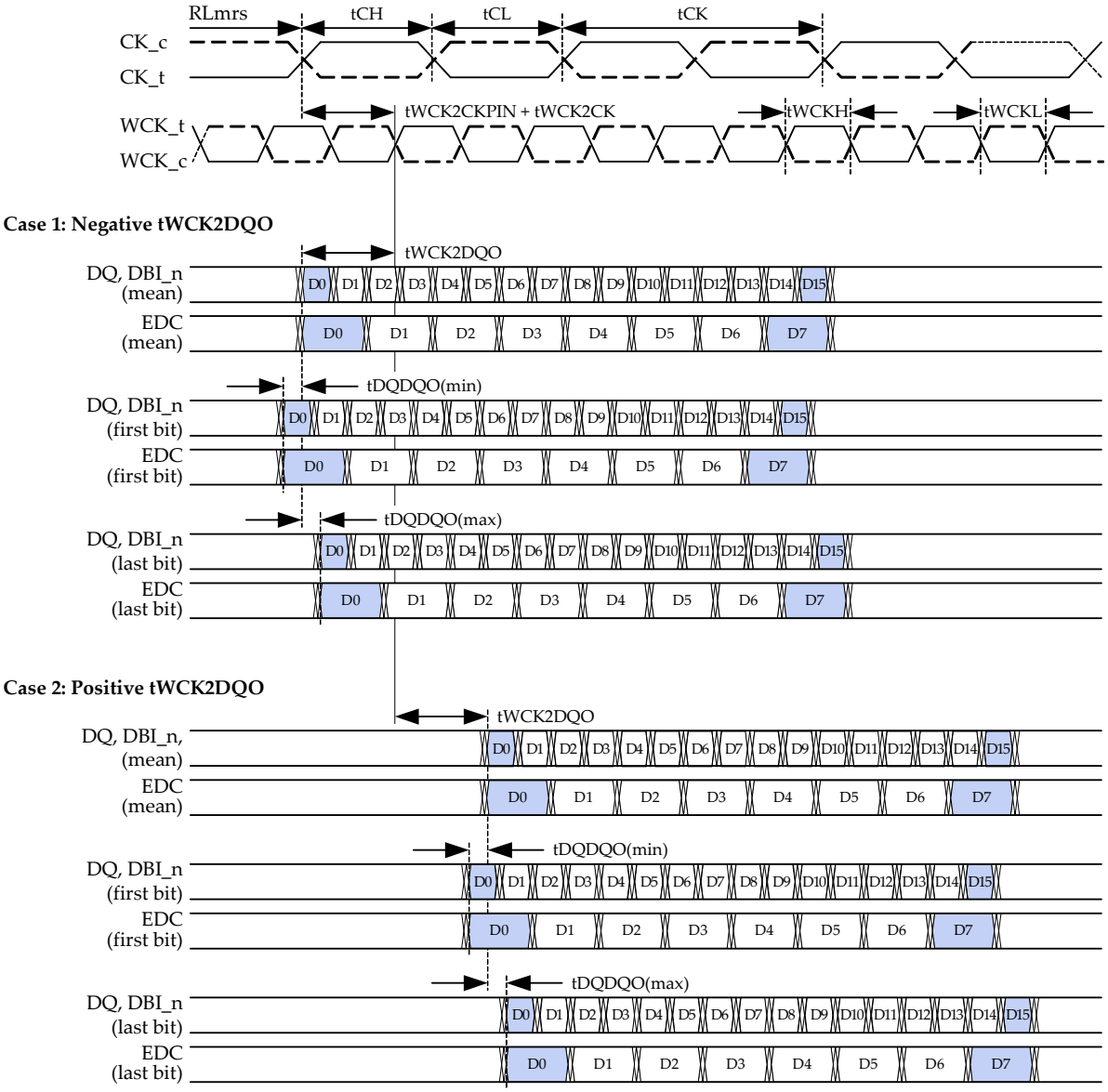


Figure 81 — READ Command

During READ bursts, the first valid data-out element will be available after the read latency (RL). The read latency is defined as RLmrs * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where RLmrs is the number of clock cycles programed in MR0, $t_{WCK2CKPIN}$ is the phase offset between WCK and CK at the pins when phase aligned at the phase detector, t_{WCK2CK} is the alignment error between WCK and CK at the phase detector, and $t_{WCK2DQO}$ is the WCK to DQ/DBI_n/EDC offset as measured at the DRAM pins. The total delay is relative to the data eye initial edge averaged over one double-byte. The maximum skew within a double-byte is defined by t_{DQDQO}.

READ word lane timings for QDR mode are illustrated in Figure 82, and READ word lane timings for DDR mode in Figure 83.

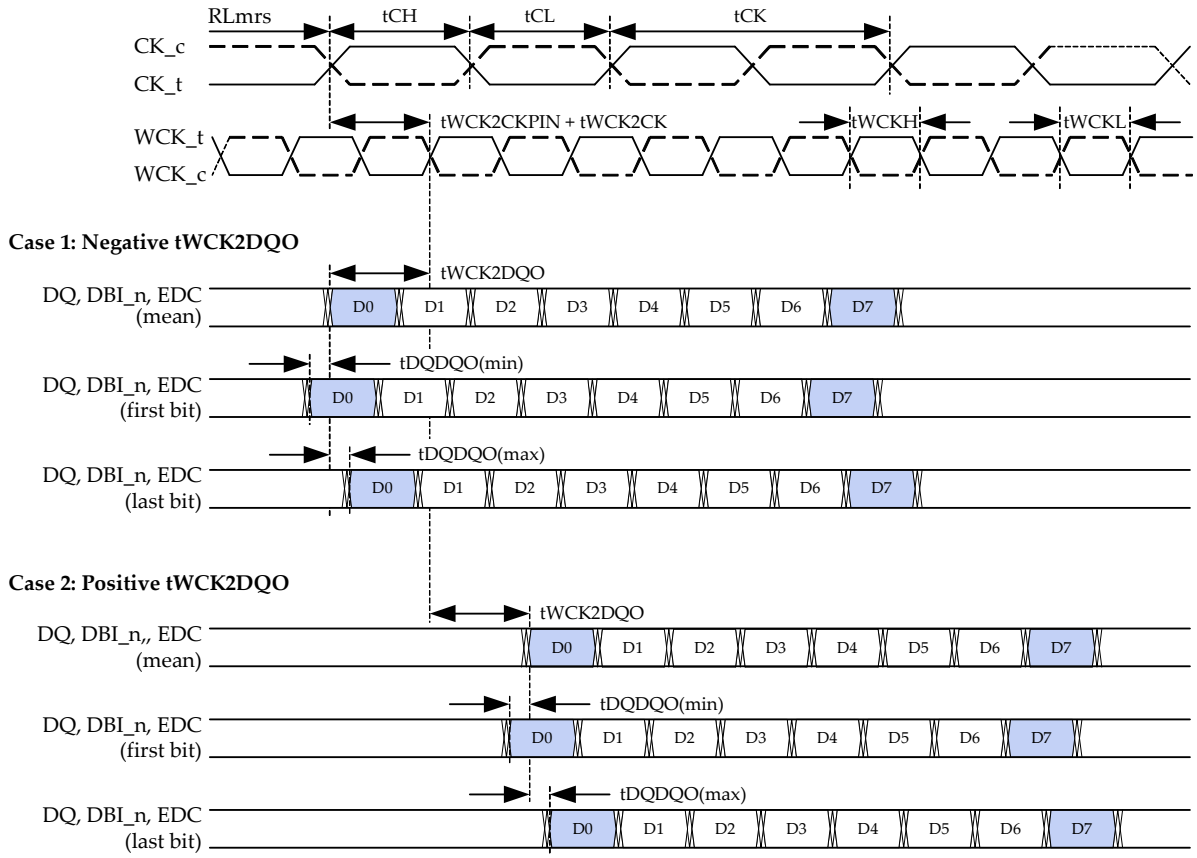
7.9 READ (cont'd)



NOTE 1 RLmrs is the READ latency programmed in Mode Register MR0.
NOTE 2 Timings are shown with positive tWCK2CKPIN and tWCK2CK values. See WCK2CK timings for tWCK2CKPIN and tWCK2CK ranges.
NOTE 3 tWCK2DQO parameter values could be negative or positive numbers, depending on PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual tWCK2DQO value for stable READ operation.
NOTE 4 tDQDQO defines the minimum to maximum variation of tWCK2DQO within a double byte.

Figure 82 — READ Word Lane Timing in QDR Mode

7.9 READ (cont'd)



NOTE 1 RLmrs is the READ latency programmed in Mode Register MR0.
NOTE 2 Timings are shown with positive tWCK2CKPIN and tWCK2CK values. See WCK2CK timings for tWCK2CKPIN and tWCK2CK ranges.
NOTE 3 tWCK2DQO parameter values could be negative or positive numbers, depending on PLL-on-or PLL-off mode operation and design implementation. They also vary across PVT. Data training is required to determine the actual tWCK2DQO value for stable READ operation.
NOTE 4 tDQDQO defines the minimum to maximum variation of tWCK2DQO within a double byte.

Figure 83 — READ Word Lane Timing in DDR Mode

Upon completion of a burst, assuming no other READ command has been initiated, all DQ and DBI_n pins will drive a value of '1' and the ODT will be enabled at a maximum of 1 t_{CK} later. The drive value and termination value may be different due to separately defined calibration offsets. If the ODT is disabled, the pins will drive High-Z.

Subsequent timing diagrams illustrate different cases of read operations. The figures are drawn for QDR mode; they also apply to DDR mode with the exception that the data burst of 16 (D0 .. D15) on the DQ/DBI_n pins is replaced by a data burst of 8 (D0 .. D7) as shown in Figure 86 for a single READ burst.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued after the previous READ command according to the t_{CCD} timing. If that READ command is to another bank then an ACTIVATE command must precede the READ command and t_{RCDRD} also must be met.

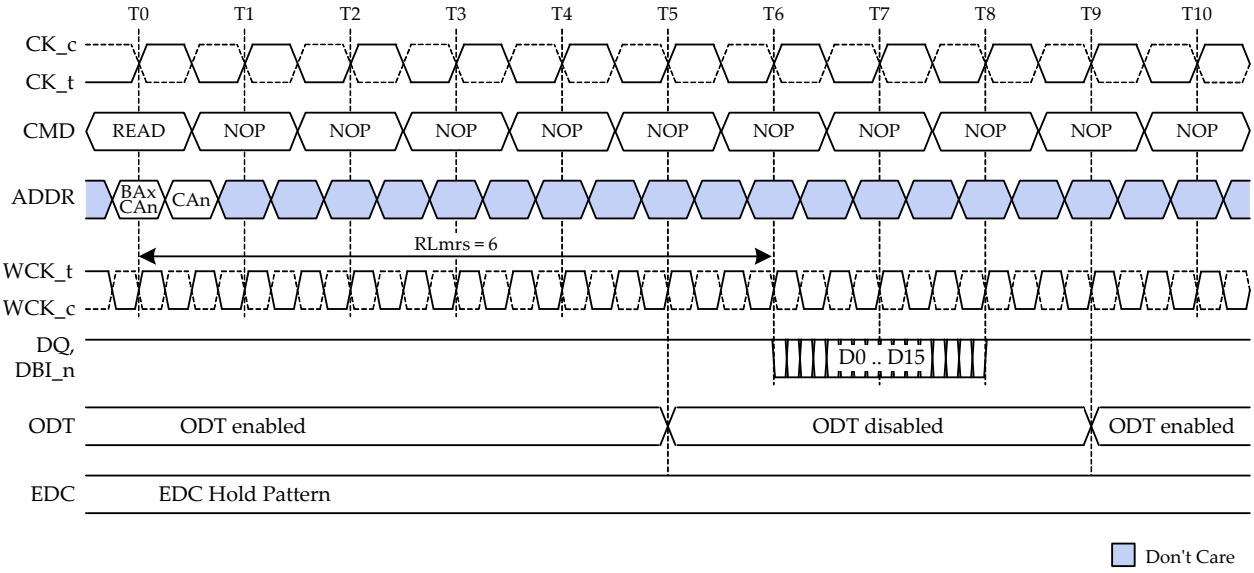
A WRITE can be issued any time after a READ command as long as the bus turn around time t_{RTW} is met. If that WRITE command is to another bank, then an ACTIVATE command must precede the second WRITE command and t_{RCDWR} also must be met.

7.9 READ (cont'd)

A PRECHARGE can also be issued with the same timing restriction as the new READ command if t_{RAS} is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

The data inversion flag is driven on the DBI_n pin to identify whether the data is true or inverted data. If DBI_n is High, the data is not inverted, and if Low it is inverted. READ data inversion can be enabled (A8=0) or disabled (A8=1) using RDBI in MR1.

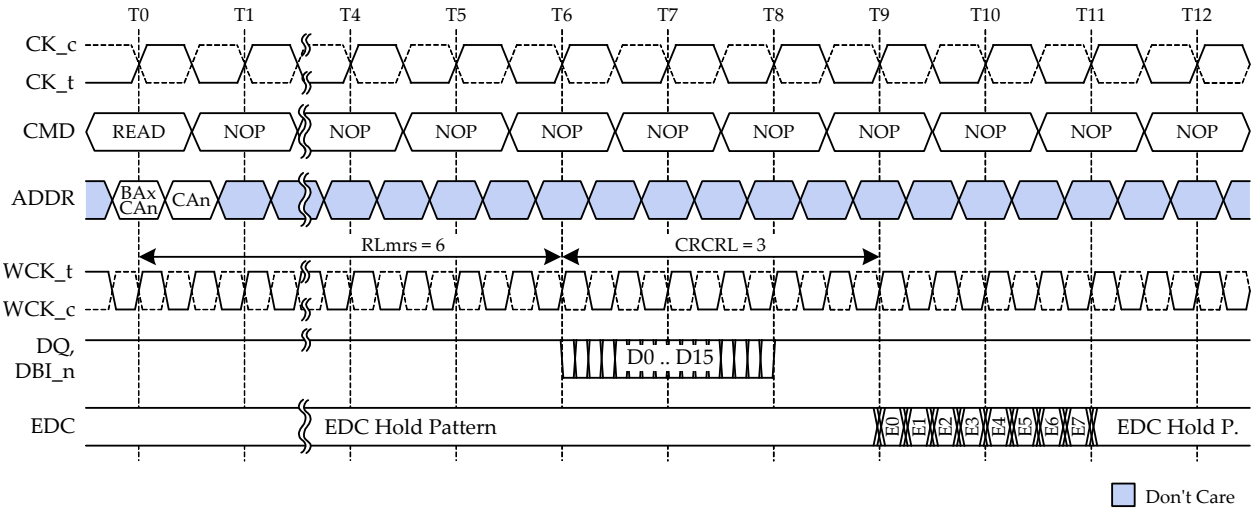
When enabled by the RDCRC flag in MR4, EDC data is returned to the controller with a latency of (RLmrs + CRCRL) * t_{CK} + $t_{WCK2CKPIN}$ + t_{WCK2CK} + $t_{WCK2DQO}$, where CRCRL is the CRC read latency programmed in MR4.



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 RLmrs = 6 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 An ACTIVATE (ACT) command is required to be issued before the READ command, and t_{RCDRD} must be met.
NOTE 5 Drive Strengths offsets are programmed in MR2 independently for Pulldown (PD), Pullup (PU) and ODT.
NOTE 6 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

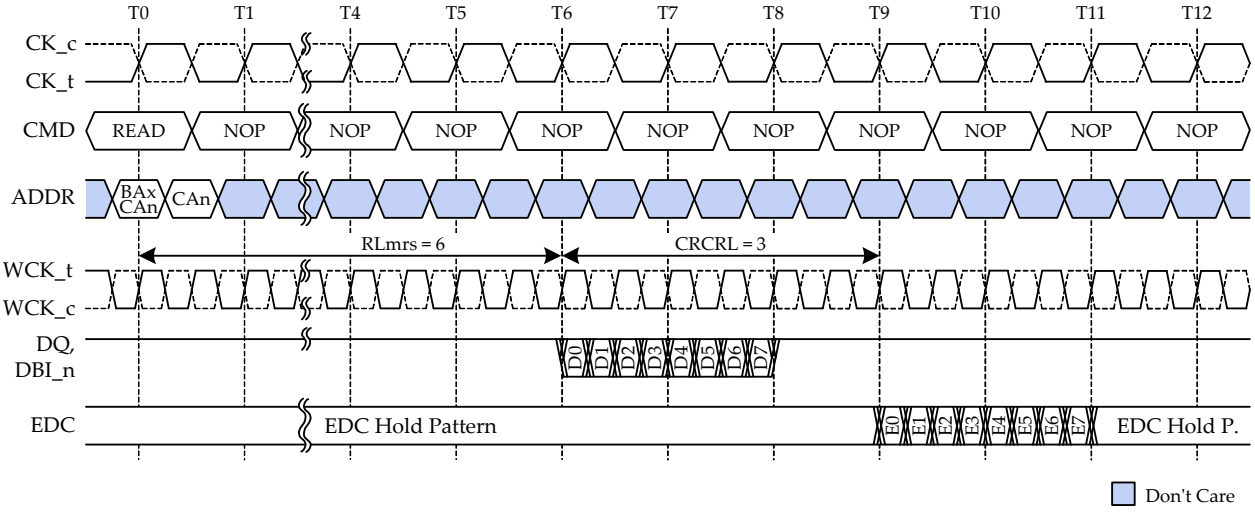
Figure 84 — Single READ without EDC

7.9 READ (cont'd)



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16. E0..E7 = CRC burst with BL=8.
NOTE 2 RLmrs = 6 and CRCRL = 3 are shown as examples. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 An ACTIVATE (ACT) command is required to be issued before the READ command, and t_{RCDRD} must be met.
NOTE 5 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

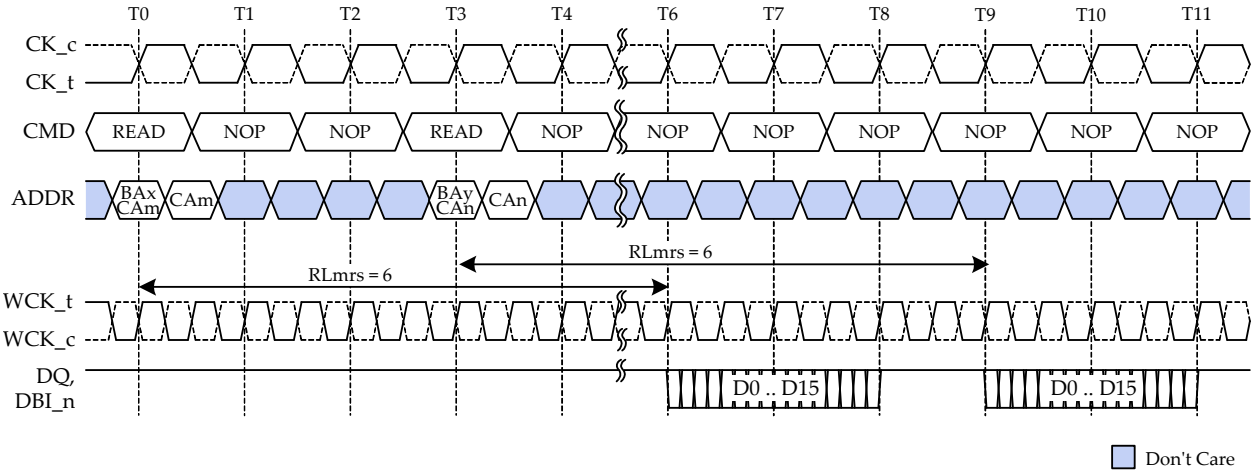
Figure 85 — Single READ with EDC



NOTE 1 BAx = bank address x; CAn = column address n. D0..D7 = data burst with BL= 8. E0..E7 = CRC burst with BL=8.
NOTE 2 RLmrs = 6 and CRCRL = 3 are shown as examples. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 An ACTIVATE (ACT) command is required to be issued before the READ command, and t_{RCDRD} must be met.
NOTE 5 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

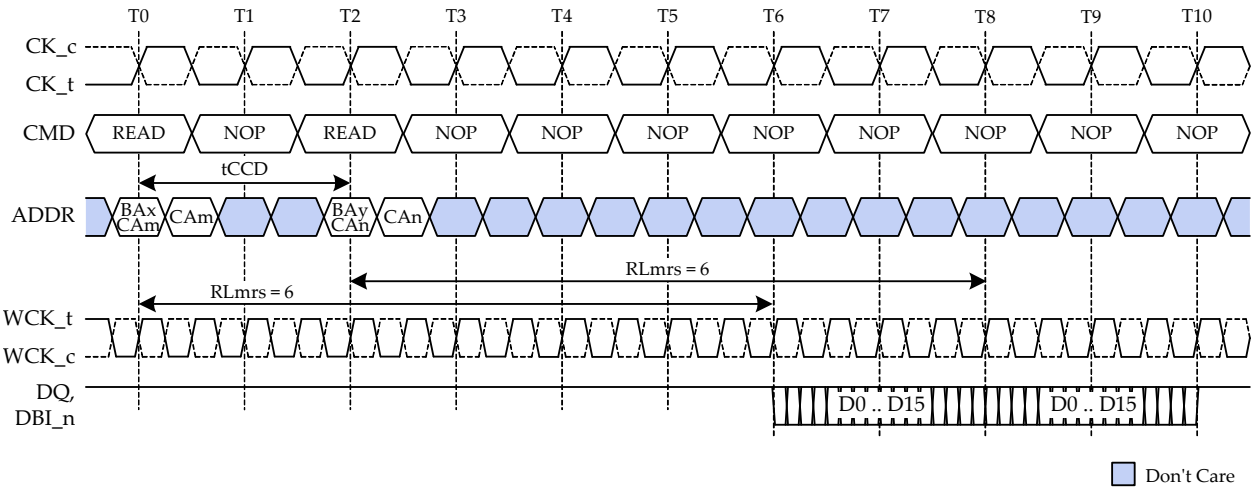
Figure 86 — Single READ with EDC in DDR Mode

7.9 READ (cont'd)



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data bursts with BL=16.
NOTE 2 RLmrs = 6 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 t_{CCD} = t_{CCDL} when bank groups are enabled and both READs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the READ commands, and t_{RCDRD} must be met.
NOTE 7 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

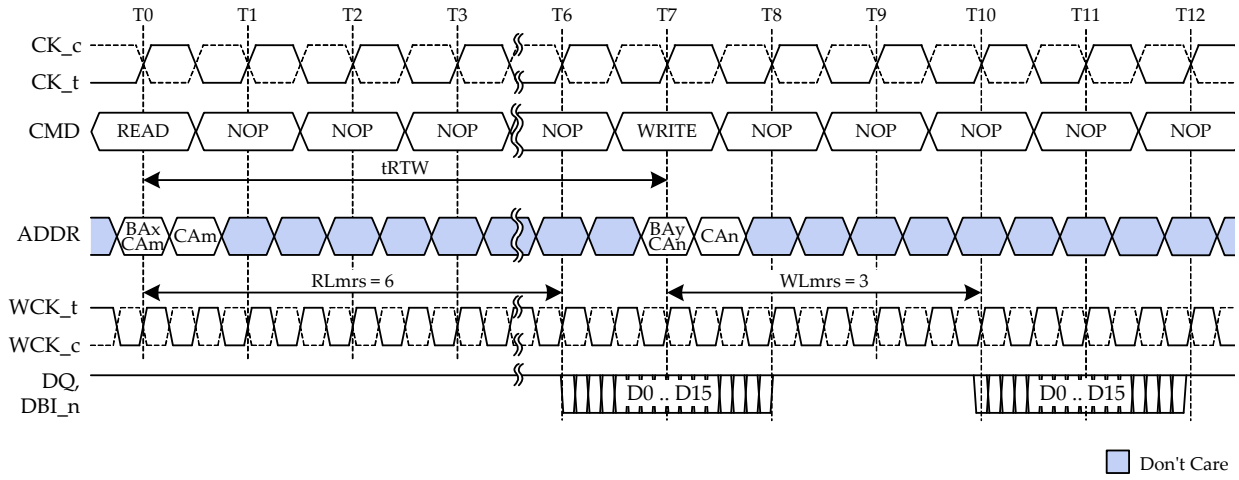
Figure 87 — Non-Gapless READs



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data bursts with BL=16.
NOTE 2 RLmrs = 6 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 t_{CCD} = t_{CCDL} when bank groups are enabled and both READs access banks in the same bank group; otherwise t_{CCD}=t_{CCDS}.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the READ commands, and t_{RCDRD} must be met.
NOTE 7 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

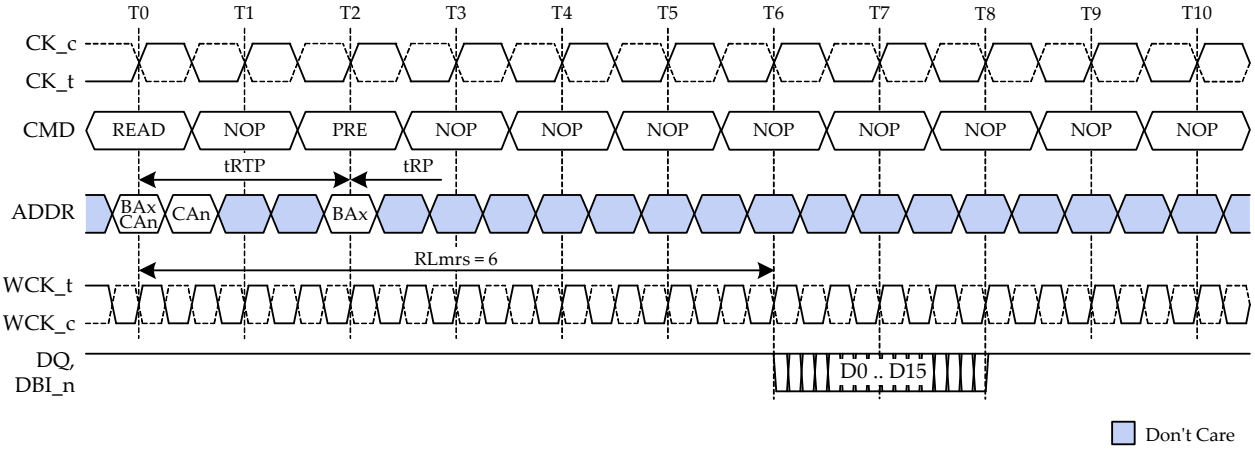
Figure 88 — Gapless READs

7.9 READ (cont'd)



NOTE 1 BAx,y = bank addresses x,y; CAm,n = column addresses m,n. D0..D15 = data bursts with BL=16.
NOTE 2 RLmrs = 6 and WLmrs = 3 are shown as examples. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQO}$ and $t_{WCK2DQI}$ shall be considered in the calculation of the bus turnaround time.
NOTE 6 For WRITE operations it is important that the latching point meet the data valid window requirements, which may or may not be center aligned at the pins.
NOTE 7 An ACTIVATE (ACT) command is required to be issued before the READ and WRITE commands, and t_{RCDRD} or t_{RCDWR}, respectively, must be met.
NOTE 8 $t_{WCK2DQI}$, $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 89 — READ to WRITE



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 RLmrs = 6 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 t_{RTP} = t_{RTPL} when bank groups are enabled and the PRECHARGE command accesses the same bank; otherwise t_{RTP} = t_{RTPS}.
NOTE 6 An ACTIVATE (ACT) command is required to be issued before the READ command, and t_{RCDRD} must be met.
NOTE 7 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 90 — READ to PRECHARGE

7.9.1 DQ Read Preamble

DQ read preamble conditions the DQs for better signal integrity on the initial data of a READ burst.

Once enabled by bit A5 in MR7, the DQ read preamble will precede all READ bursts, including non-consecutive READ bursts with a minimum gap of 1 t_{CK}, as shown in Figure 87. When enabled, the DQ read preamble pattern applies to all DQ and DBI_n pins in a byte, and the same pattern is used for all bytes as shown in Figure 91. DQ read preamble is enabled or disabled for all bytes. The EDC pin in each byte is not included in the DQ read preamble. If ODT is enabled, the ODT is disabled 1 t_{CK} before the start of the preamble pattern as shown in Figure 92.

The preamble pattern on the DBI_n pin is only enabled if RDBI is enabled by bit A8 in MR1. During the preamble the DBI_n pin is treated as another DQ pin and the preamble pattern on the DQs is not encoded with RDBI. If RDBI is disabled, then the DBI_n pin drives ODT.

DQ preamble is supported in QDR mode only; it must be disabled in DDR mode.

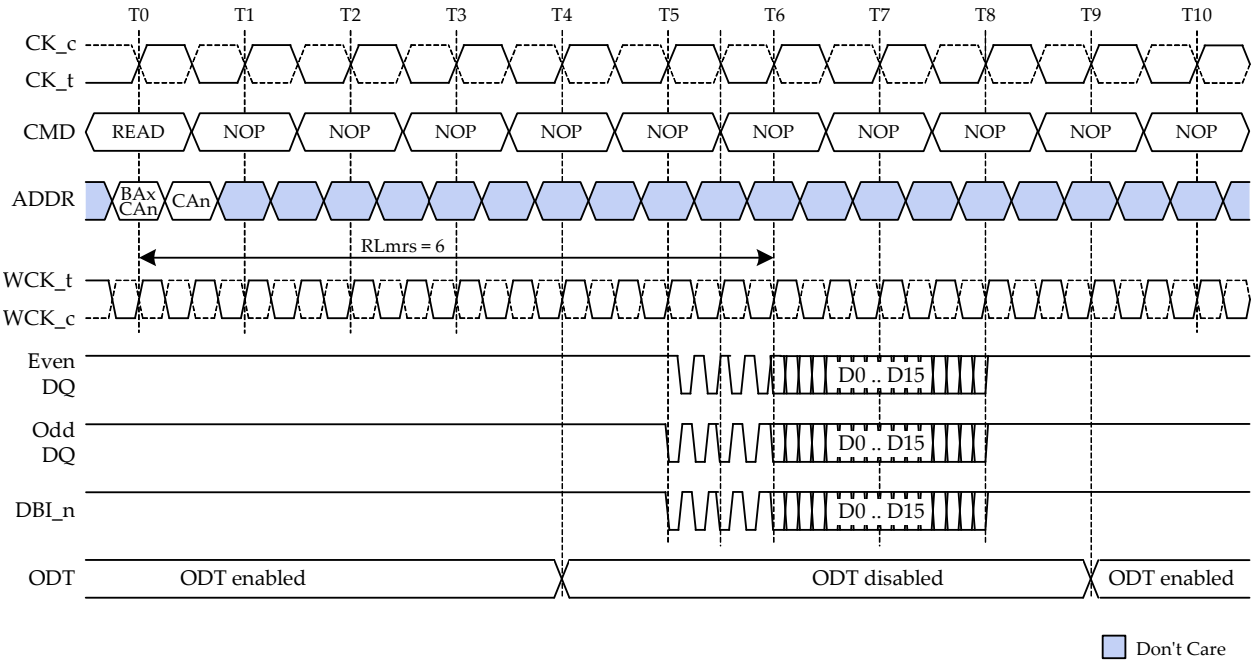
Byte 0	**Idle**								**Preamble**								**Burst**															
DQ7	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ6	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ5	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ4	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ3	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ2	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DQ0	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
DBI0_n	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
Max 0's	0	0	0	0	0	0	0	0	5	4	5	4	5	4	5	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4

Time →

NOTE 1 Byte 0 shown; the same pattern applies to bytes 1 ... 3.
NOTE 2 The number of Max 0's in the burst is 4 only if RDBI is enabled. Max 0's is on a per byte basis and does not include the EDC pin.
NOTE 3 V = Valid Data

Figure 91 — DQ Read Preamble Pattern

7.9.1 DQ Read Preamble (cont'd)



NOTE 1 BAx = bank address x; CAn = column address n. D0..D15 = data burst with BL=16.
NOTE 2 RLmrs = 6 is shown as an example. Actual supported values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 EDC may be on or off. See Figure 86, Single READ with EDC, for EDC pin timing.
NOTE 5 An ACTIVATE (ACT) command is required to be issued before the READ command, and t_{RCDRD} must be met.
NOTE 6 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 92 — Read Preamble Timing Diagram

7.9.2 READ with RDQS Mode

To operate at lower clock frequencies, the GDDR5X SGRAM may be put into RDQS mode in which a read data strobe (RDQS) will be sent on the EDC pins along with the read data. The controller uses the RDQS to latch the read data.

RDQS mode is enabled by setting bit A5 in MR3. When the bit is set, the device asynchronously terminates any EDC hold pattern and drives a logic High after t_{MRD} at the latest. All features controlled by MR4 are ignored in RDQS mode. RDQS mode also requires that the operating mode in MR8 bit A9 is set to DDR mode.

READ commands are executed as in normal mode regarding command to data out delay and programmed read latencies. A fixed clock-like pattern as shown in Figure 93 is driven on the EDC pins in phase (edge aligned) with the DQ. Prior to the first valid data element, this fixed clock-like pattern or read preamble is driven for 4 U.I. .

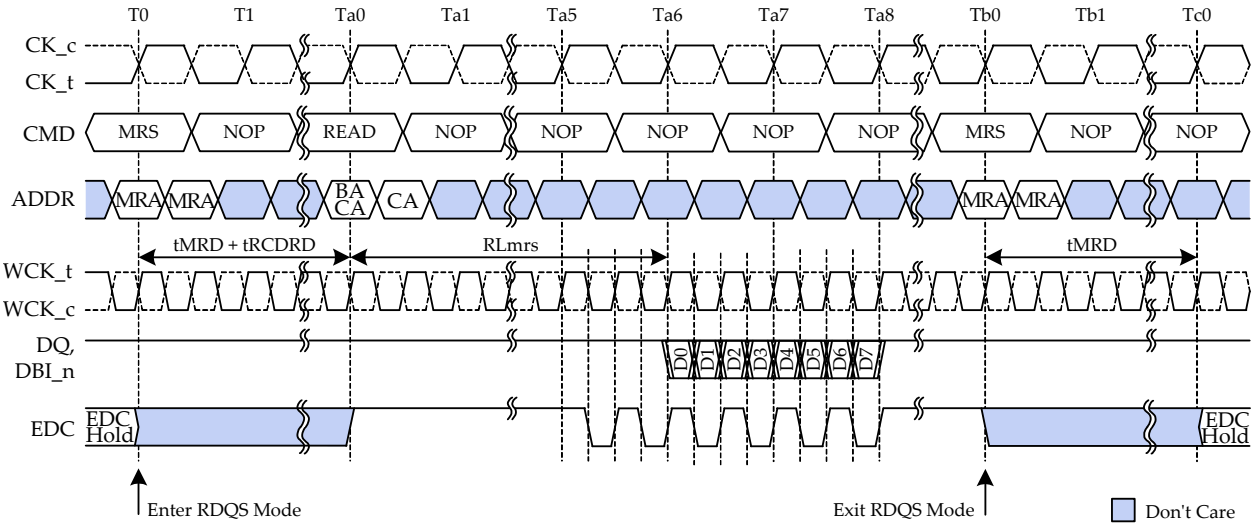
No CRC is calculated in RDQS mode for reads or writes. The CRC engine is effectively disabled, and the corresponding WRCRC and RDCRC mode register bits are ignored.

The use of RDQS mode requires that the PLL/DLL is disabled in MR1.

There is no equivalent WDQS mode; WRITE commands to the device are not affected by RDQS mode.

RDQS mode is exited by resetting the RDQS mode bit. In this case the device asynchronously begins driving the EDC hold pattern after t_{MRD} at the latest.

7.9.2 READ with RDQS Mode (cont'd)



NOTE 1 MRA = mode register address; BA = bank address; CA = column address . D0..D7 = data burst with BL=8.
NOTE 2 RLmrs = 6 is shown as an example. Actual supported RL values will be found in clause 4 (MR) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 An ACTIVATE (ACT) command is required to be issued before the READ command, and t_{RCDRD} must be met.
NOTE 5 $t_{WCK2DQO}$ = 0 is shown for illustration purposes.

Figure 93 — RDQS Mode Timings

7.10 PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank (PRE) or the open row in all banks (PREALL). The bank(s) will be available for a subsequent row access a specified time t_{RP} after the PRECHARGE command is issued as illustrated in Figure 94.

A8 determines whether one or all banks are precharged. When only one bank is to be precharged, BA[3:0] select the bank, otherwise BA[3:0] are treated as "Don't Care".

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued to that bank. A PRECHARGE command is allowed and treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

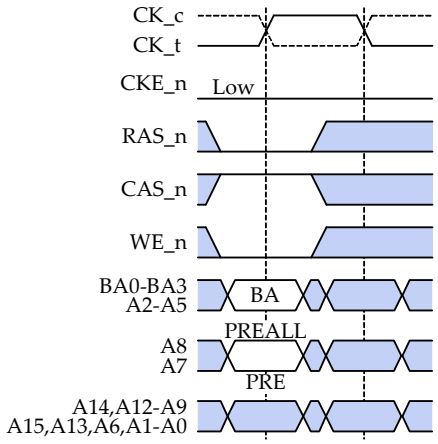


Figure 94 — PRECHARGE Command

7.10.1 AUTO PRECHARGE

The auto precharge feature performs the same individual bank precharge operation as described in Clause 7.10 but without an explicit command. This is engaged when a READ or WRITE command is issued with A8 High, and is performed upon completion of the read or write operation. Auto precharge is non persistent so it must be either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures the precharge is initiated at the earliest valid stage within a read or write operation. No other command can be issued to the same bank until the precharge time t_{RP} is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for READ and WRITE commands. An auto precharge operation can occur in parallel with a PRECHARGE or PRECHARGE ALL command.

7.11 REFRESH

The (all bank) REFRESH (REFAB) and PER-BANK REFRESH (REFPB) commands are provided for the refresh of the device during normal operation. The commands are non persistent, so they must be issued each time a refresh is required. REFAB and REFPB commands are distinguished by the level of the A8 address pin as shown in Figure 95 and Figure 97.

7.11.1 REFRESH (REFAB) Command

A minimum time t_{RFC} is required between two REFRESH commands. The same rule applies to any access command after the refresh operation. All banks must be precharged prior to the REFRESH command.

Refresh addressing is generated by the internal refresh controller. This makes the address bits (except A8) "Don't Care" during a REFRESH command. The device requires REFRESH cycles at an average periodic interval of t_{REFI}(max). To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight REFRESH commands can be posted to the device, and the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * t_{REFI}.

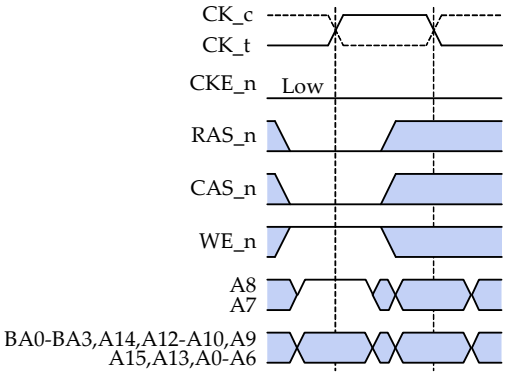
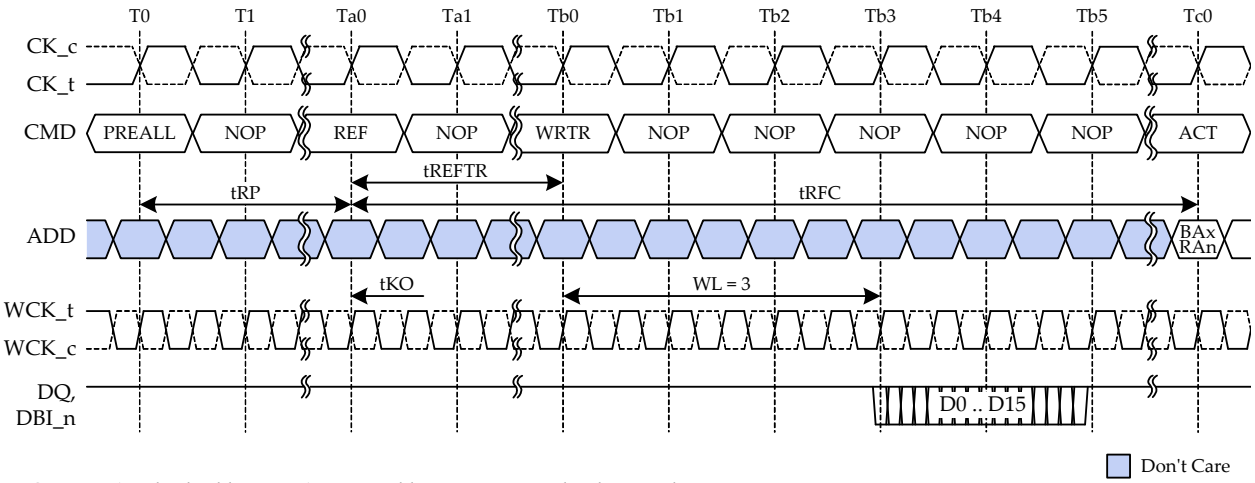


Figure 95 — REFRESH (REFAB) Command

7.11.1 REFRESH (REFAB) Command (cont'd)



NOTE 1 BAx = bank address x; RAn = row address n. D0..D15 = data burst with BL=16.
NOTE 2 WLmrs = 3 is shown as an example.. Actual supported values will be found in clause 4 (Mode Register) and 8.8 (AC Timings).
NOTE 3 WCK and CK are shown aligned ($t_{WCK2CKPIN}$=0, t_{WCK2CK}=0) for illustration purposes. WCK2CK training determines the needed offset between WCK and CK.
NOTE 4 WRTR and RDTR commands are allowed during refresh unless disabled in the mode register.

Figure 96 — Refresh Timings

During REFRESH, and when bit A2 in MR5 is set to 0, WRTR, RDTR, and LDFF commands are allowed at t_{REFTR} after the REFRESH command, which enable (incremental) data training to occur in parallel with the internal refresh operation without loss of performance on the interface. See READ Training and WRITE Training for details.

As impedance updates from the auto-calibration engine may occur with any REFRESH command, it is safe to only issue NOP commands during t_{KO} period to prevent false command, address or data latching resulting from impedance updates.

7.11.2 PER-BANK REFRESH (REFPB) Command

The PER-BANK REFRESH command provides an alternative solution for the refresh of the device. The command initiates a refresh cycle on a single bank selected by BA[3:0] while accesses to other banks including writes and reads are not affected.

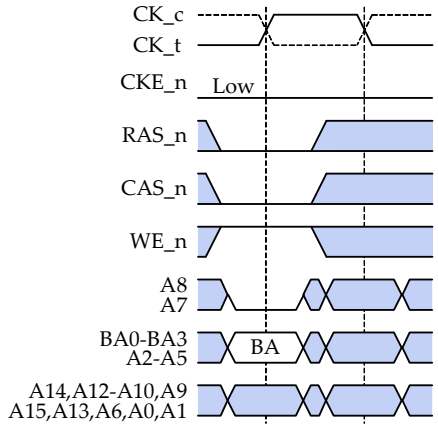


Figure 97 — PER-BANK REFRESH (REFPB) Command

7.11.2 PER-BANK REFRESH (REFPB) Command (cont'd)

A minimum time t_{RRD} is required between an ACTIVATE command and a REFPB command to a different bank. A minimum time t_{RREFD} is required between any two REFPB commands (see Figure 99 and Note 1 in Table 30 for an exception requiring t_{RFCPB}), and between a REFPB command and an ACTIVATE command to a different bank. A minimum time t_{RFCPB} is required between a REFPB command and an access command to the same bank that follows. The selected bank must be precharged prior to the REFPB command.

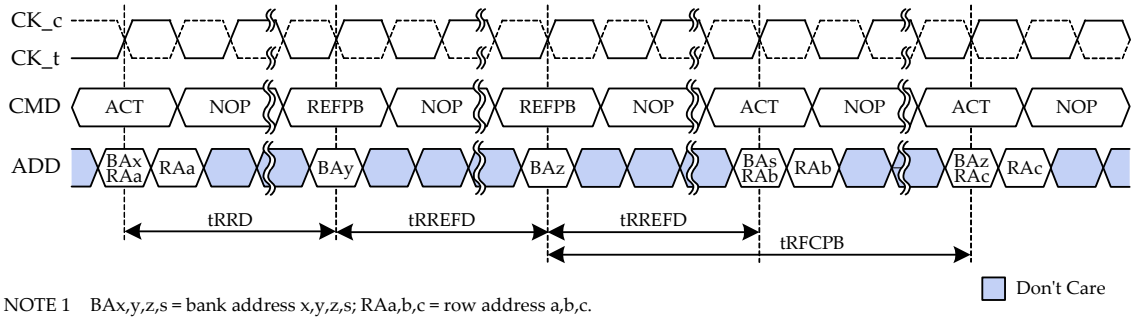
The row address is generated by an internal counter. This makes the row address bits (except A8) "Don't Care" during a REFPB command.

A REFPB command to one of the 16 banks can be issued in any order. After all 16 banks have been refreshed using the REFPB command, and after waiting for at least t_{RFCPB}, the internal refresh counter is incremented and the controller can issue another set of REFPB commands in the same or a different order. However, it is illegal to send another REFPB command to a bank unless all 16 banks have been refreshed using the REFPB command. The controller must track the banks being refreshed by the REFPB command.

The bank count is synchronized between the controller and the device by resetting the bank count to zero. Synchronization occurs upon exit from reset state or by issuing a REFRESH or SELF REFRESH ENTRY command. Both commands may be issued at any time even if a preceding sequence of REFPB commands has not completed cycling through all 16 banks. The internal refresh counter is not incremented in case of such incomplete cycling. It is pointed out that multiple occurences of synchronization events without refresh counter increment may result in an insufficient refresh of the memory array; it is suggested to issue additional REFAB commands in that case.

The average rate of REFPB commands t_{REFIPB} is given by t_{REFI} / 16.

At least one REFAB command must be issued upon exit from self refresh mode or after a clock frequency change. REFAB commands must also be issued during normal operation at a minimum rate of t_{ABREF} = 1ms to allow impedance updates from the auto-calibration engine to occur.



NOTE 1 BAx,y,z,s = bank address x,y,z,s; RAa,b,c = row address a,b,c.

Figure 98 — Per-Bank Refresh Timings

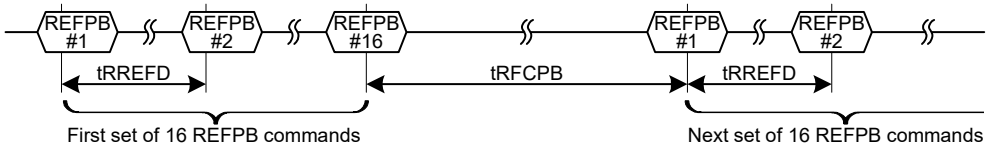


Figure 99 — Sets of Per-Bank Refresh Commands

7.11.2 PER-BANK REFRESH (REFPB) Command (cont'd)

The example in Table 29 shows two full sets of REFPB commands with the bank counter reset to zero and the refresh counter incremented after 16 REFPB commands each. The 3rd set ot REFPB commands is interrupted by the REFAB command which resets the bank counter to 0 and performs refreshes to all banks indicated by the refresh counter.

Table 29 — Refresh Counter Increments

CNT	SUB-CNT	COMMAND	BA[3:0]	REFRESH BANK	BANK COUNTER	REFRESH COUNTER
0	0	Reset, REFAB or SRE command			To 0	
1	1	REFPB	0000	0	0 to 1	
2	2	REFPB	0001	1	1 to 2	
3	3	REFPB	0010	2	2 to 3	
4	4	REFPB	0011	3	3 to 4	n
. . .						
15	15	REFPB	1110	14	14 to 15	
16	16	REFPB	1111	15	15 to 0	
17	1	REFPB	0100	4	0 to 1	
18	2	REFPB	0111	7	1 to 2	
19	3	REFPB	1011	11	2 to 3	
20	4	REFPB	0110	6	3 to 4	n + 1
. . .						
31	15	REFPB	1100	12	14 to 15	
32	16	REFPB	0001	1	15 to 0	
33	1	REFPB	0010	2	0 to 1	
34	2	REFPB	1001	9	1 to 2	n + 2
35	3	REFPB	0000	0	2 to 3	
36	0	**REFAB**	**V**	**all**	**To 0**	**n + 2**
37	1	REFPB	1010	10	0 to 1	
38	2	REFPB	0101	5	1 to 2	n + 3
. . .						

7.11.2 PER-BANK REFRESH (REFPB) Command (cont'd)

Table 30 — REFRESH and PER-BANK REFRESH Command Scheduling Requirements

FROM COMMAND	TO COMMAND	MINIMUM DELAY BETWEEN "FROM COMMAND" TO "TO COMMAND"	NOTES
REFRESH	REFRESH or SELF REFRESH ENTRY	t_{RFC}	
	PER-BANK REFRESH (any bank)	t_{RFC}	
	ACTIVATE (any bank)	t_{RFC}	
PER-BANK REFRESH	REFRESH or SELF REFRESH ENTRY	t_{RFCPB}	2
	PER-BANK REFRESH (other bank)	t_{RREFD}	
	PER-BANK REFRESH (any bank)	t_{RFCPB}	1
	ACTIVATE (other bank)	t_{RREFD}	
	ACTIVATE (same bank)	t_{RFCPB}	
ACTIVATE	REFRESH or SELF REFRESH ENTRY	t_{RC}	3
	PER-BANK REFRESH (other bank)	t_{RRD}	4
	PER-BANK REFRESH (same bank)	t_{RC}	3

NOTE 1 t_{RFCPB} parameter must be observed when the first REFPB command completes a set of 16 per-bank refresh operations, and the second REFPB command initiates the next set of 16 per-bank refresh operations.
NOTE 2 All banks must be in the idle state before issuing a REFRESH or SELF REFRESH ENTRY command.
NOTE 3 A bank must be in the idle state with t_{RP} satisfied before it is refreshed.
NOTE 4 t_{FAW} parameters must be observed as well.

7.12 SELF REFRESH

Self refresh can be used to retain data in the GDDR5X SGRAM, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The SELF REFRESH ENTRY command is like a REFRESH command except that CKE_n is pulled High.

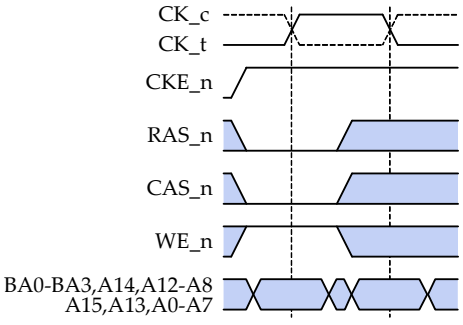


Figure 100 — SELF REFRESH ENTRY Command

SELF REFRESH ENTRY is only allowed when all banks are precharged with t_{RP} satisfied, and when either the last read data or CRC data element from a preceding READ or WRITE command have been pushed out (t_{RDSRE} or t_{WRSRE}). NOP commands are required after entering self refresh until t_{CPDED} is met .

The PLL/DLL is automatically disabled upon entering self refresh and is automatically enabled and reset upon exiting self refresh. If the device enters self refresh with the PLL/DLL disabled, it will exit self refresh with the PLL/DLL disabled.

7.12 SELF REFRESH (cont'd)

After the SELF REFRESH ENTRY command is registered, CKE_n must be held High to keep the device in self refresh mode. When the device has entered the self refresh mode, all external control signals except CKE_n and RESET_n are "Don't care". The user can halt the external CK and WCK clocks or change the external clock frequency t_{CKSRE} after self refresh entry. The address, command, data, CK and WCK pins are in ODT state, and the EDC pins drive a High (or High-Z when the EDC High-Z bit is set). CK and WCK clocks are internally disabled during self refresh operation to save power.

For proper self refresh operation, all power supply and reference voltage pins (V_{PP}, V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, V_{REFC}) must be at valid levels.

The device initiates a minimum of one internal refresh within t_{CKE} once it enters self refresh mode. The minimum time the device must remain in self refresh mode is t_{CKE}.

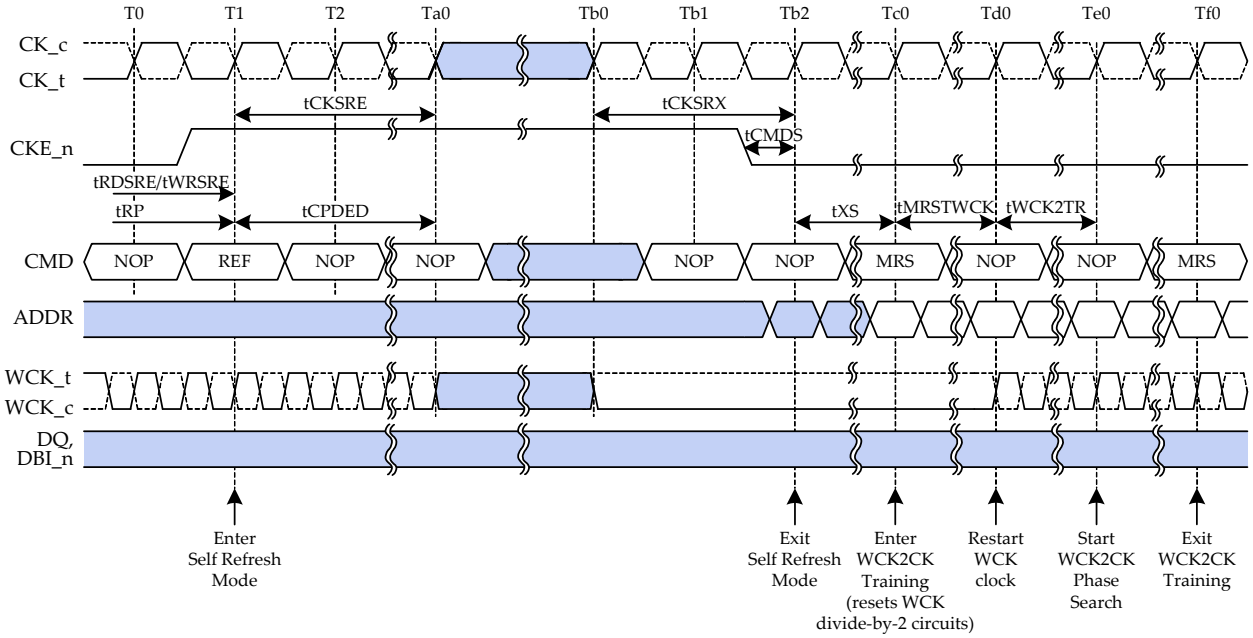
Exiting self refresh requires a sequence of events. First, the CK clock must be stable t_{CKSRX} prior to CKE_n going Low. The WCK clocks could be on or off at self refresh exit, depending on the preferred method for resetting the WCK by two divider in WCK2CK training, which is required upon self refresh exit. The vendor datasheet should be consulted for frequencies supported by each method. To allow completion of any internal refresh in progress, a delay of at least t_{XS} must be satisfied before a valid command can be issued to the device.

During self refresh the on-die termination (ODT) and driver are not auto-calibrated. Recalibration is initiated automatically upon self refresh exit. During this period, commands other than NOP shall be issued with caution, depending on anticipated or measured voltage and temperature changes.

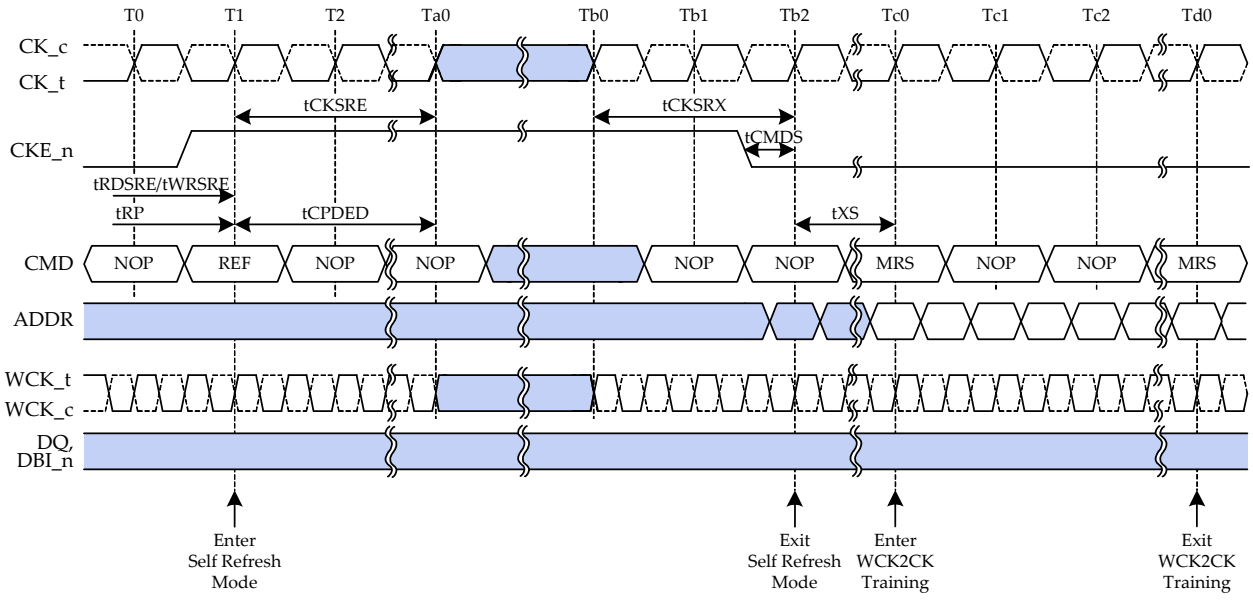
After the device has exited self refresh, it can re-enter self refresh after a period of at least t_{XS} and after issuing one extra REFRESH (REFAB) command.

7.12 SELF REFRESH (cont'd)

Option A: Self Refresh Entry and Exit; SRX with WCK stopped



Option B: Self Refresh Entry and Exit; SRX without WCK stopped



NOTE 1 WCK2CK training is required upon self refresh exit prior to any READ or WRITE command.
- Option A: to aid in resetting the WCK divide-by-2 circuits at WCK2CK training entry, self refresh mode is exited with the WCK clock stopped; the WCK clock is enabled tMRSTWCK after WCK2CK training entry.
- Option B: the WCK clock is enabled prior to self refresh exit

NOTE 2 At least one REFRESH command shall be issued after tXS to allow output driver and termination impedance updates.

Figure 101 — Self Refresh Entry and Exit

7.12 SELF REFRESH (cont'd)

Table 31 — Pin States During Self Refresh

Pin	State
EDC	High (High-Z when EDC High-Z is enabled (MR8 A2 = 1))
DQ/DBI_n	ODT
CK_t, CK_c	ODT
ADD/CMD	ODT
CKE_n	ODT (driven High by controller)
WCK_t/WCK_c	ODT

7.12.1 Hibernate Self Refresh

Hibernate self refresh is a special mode that provides the same data retention as in the regular self refresh mode, but allows the device to disable additional circuits to achieve an even lower power consumption at the expense of a significantly extended period to return to normal operation.

MR8 bit A3 is associated with hibernate self refresh. The bit is self-clearing, meaning that an MRS command must set this bit any time the device shall enter hibernate self refresh using the SELF REFRESH ENTRY command.

After the SELF REFRESH ENTRY command is registered, CKE_n must be held High to keep the device in hibernate self refresh mode. Exiting this mode requires a sequence of events as shown in Figure 102: at first CKE_n must be pulled Low and again pulled High after t_{XHP} has elapsed. The device is now in regular self refresh mode, and must be held in this mode for at least t_{XSH} period, to retain data during the extended exit time from hibernate self refresh mode. After t_{XSH} period the sequence for self refresh exit shall be followed to return to normal device operation.

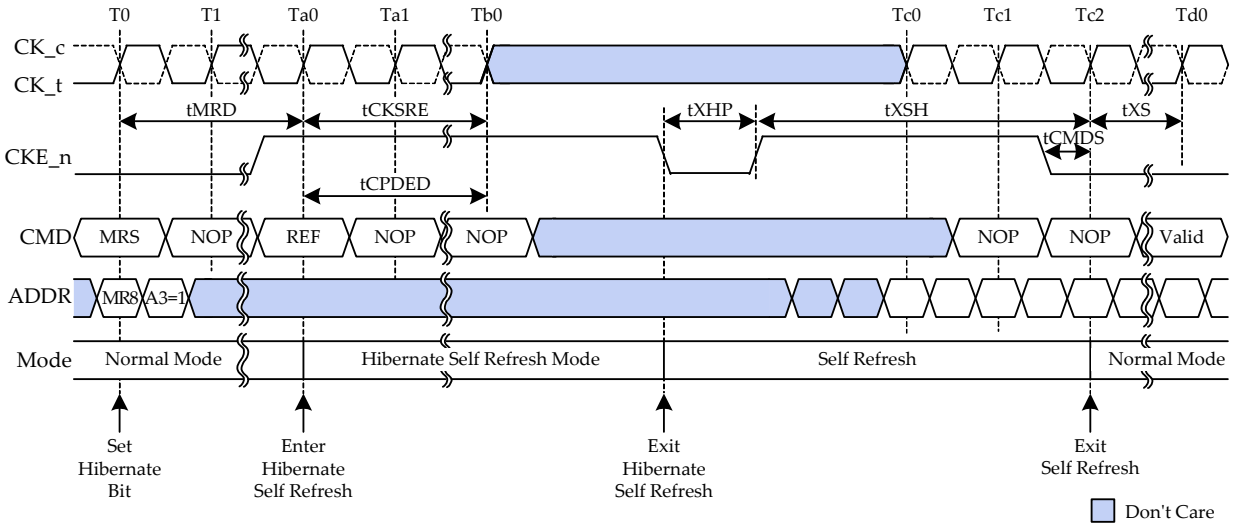


Figure 102 — Hibernate Self Refresh

7.12.2 Partial Array Self Refresh (PASR)

The GDDR5X SGRAM can be programmed to exclude parts of the memory array from refresh when the device is held in self refresh mode. Bits A[11:0] in MR11 are associated with the Partial Array Self Refresh (PASR) feature.

PASR Bank Masking

Two banks can individually be configured to be excluded from refresh in self refresh mode by programming the bank mask bit(s) A[7:0] in MR11. The banks are excluded from refresh when the corresponding 2-bank mask bit is set to 1. When a 2-bank mask bit is set to 0, a refresh to the banks is determined by the status of the row segment mask bits as described in the following chapter.

PASR Row Segment Masking

The row address space of a GDDR5X SGRAM is virtually divided into 4 row segments along the two MSB row address bits. Each row segment can individually be configured to be excluded from refresh in self refresh mode by programming the row segment mask bit(s) A[11:8] in MR11. An entire row segment across all 16 banks is excluded from refresh when the corresponding row segment mask bit is set to 1. When a row segment mask bit is s set to 0, a refresh to the row segment in each group of 2 banks is determined by the status of the corresponding 2-bank mask bits as described in the previous chapter.

An example of using the PASR bank and row segment masking is shown in Table 32.

Table 32 — Example of PASR Bank and Row Segment Masking in Self Refresh Mode

	Row Segment Mask MR11 A[11:8]	Banks [15:14]	Banks [13:12]	Banks [11:10]	Banks [9:8]	Banks [7:6]	Banks [5:4]	Banks [3:2]	Banks [1:0]
2-Bank Mask MR11 A[7:0]		0	0	0	0	0	1	0	0
Row Segment 0	0						M		
Row Segment 1	0						M		
Row Segment 2	1	M	M	M	M	M	M	M	M
Row Segment 3	0						M		

NOTE Refresh operation to banks 4 and 5 as well as to row segment 2 in all banks is masked.

7.13 POWER-DOWN

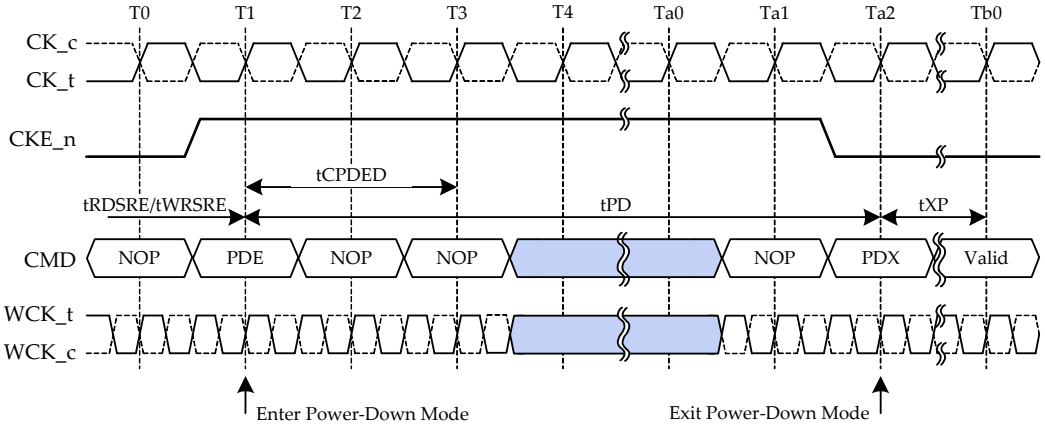
GDDR5X SGRAMs requires CKE_n to be Low at all times an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined as when the last data element including CRC has been transmitted on the DQ outputs, for WRITEs, a burst completion is defined as when the last data element has been written to the memory array and CRC data has been returned to the controller.

Power-down is entered when CKE_n is registered High. If power-down occurs when all banks are idle, this is referred to as precharge power-down mode; if power-down occurs when there is a row active in any bank, this is referred to as active power-down mode.

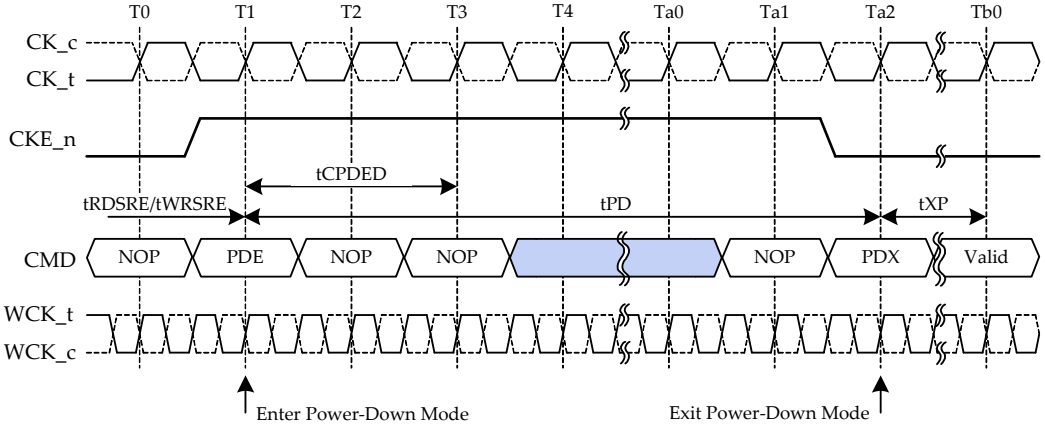
Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, WCK_t, WCK_c, RESET_n, EDC pins and CKE_n if LP2 (MR5 A1) is disabled. If LP2 is enabled, WCK_t, WCK_c input buffers and EDC output buffers are additionally de-activated in power-down.

7.13 POWER-DOWN (cont'd)

Option A: LP2 Enabled (MR5A1 = 1)



Option B: LP2 Disabled (MR5A1 = 0)



NOTE 1 Minimum CKE_n pulse width must satisfy t_{CKE}.
NOTE 2 Two more NOPs shall be issued after the POWER-DOWN ENTRY command.

Figure 103 — Power-Down Entry and Exit

For maximum power savings, the user has the option of disabling the PLL/DLL prior to entering power-down. In that case, on exiting power-down, WCK2CK training is required to set the internal synchronizers which will include the enabling of the PLL/DLL, PLL/DLL reset, and t_{LK} clock cycles must occur before any READ or WRITE command can be issued.

While in power-down, CKE_n High, a stable CK clock (except when clock frequency is changed) and RESET_n signal must be maintained at the device inputs if LP2 is enabled as shown in Figure 103, option A. If LP2 is disabled, WCK signals must also be maintained in power-down and the device continuously drives the EDC hold pattern as shown in Figure 103, option B. The power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE_n is registered Low (in conjunction with a NOP command). A valid executable command may be applied t_{XP} cycles later. The min. power-down duration is specified by t_{PD}.

7.13 POWER-DOWN (cont'd)

Table 33 — Pin States During Power Down

Pin	LP2 on (MR5 A1 = 1)	LP2 off (MR5 A1 = 0)
EDC	High	Hold
DQ/DBI_n	ODT	ODT
ADD/CMD	ODT	ODT
CK_t/CK_c	ODT	ODT
CKE_n	ODT (Driven High by Controller)	ODT (Driven High by Controller)
WCK_t/WCK_c	ODT (receiver off)	ODT (receiver active)

7.14 LOW FREQUENCY MODES

GDDR5X SGRAMs have been designed to operate over a contiguous frequency range from f_{CK} = 50 MHz to the maximum rated clock frequency of the device.

Features such as PLL/DLL off mode, RDQS mode, ODT control bits and the low power mode register bits (MR5 bits A[2:0], MR7 bit A3) have been developed for low power or low frequency operation. DRAM vendor datasheets should be consulted for frequency ranges supported for each feature. Example frequency ranges are shown in Table 34 for reference only.

Table 34 — Example of Frequency Modes

Frequency Range	Operating Mode	PLL Mode	READ Data Clock	IO Training	ODT	Low Power Mode Bits
Very High (i.e., > 6.0 Gbps)	QDR	PLL/DLL on	CDR (RDQS mode off)	Full Training	Full	Off
High (i.e., > 3.0 Gbps)	DDR	PLL/DLL on/off	CDR (RDQS mode off)	Full Training	Full	Off
Medium (i.e., < 3.0 Gbps)	DDR	PLL/DLL off	RDQS mode	Full Training	Full/Half	On/Off
Low (i.e., < 1.5 Gbps)	DDR	PLL/DLL off	RDQS mode	No Training (static offset between WCK and DQ)	Half/Off	On
NOTE The use of RDQS mode requires that the PLL/DLL is disabled in MR1.						

7.15 CLOCK FREQUENCY CHANGE SEQUENCE

1. Wait until all commands have finished and all banks are idle.
2. Send NOP (must meet input setup/hold relative to clock while clock is changing) to the device for the entire sequence unless stated to do otherwise. The user must take care of refresh requirements.
3. If the new desired clock frequency is below the min frequency supported by PLL/DLL-on mode, turn the PLL/DLL off via an MRS command.
4. Change the clock frequency and wait until clock is stabilized.
5. Perform address training if required.
6. If the new clock frequency is within the PLL/DLL on range and the PLL/DLL-on mode is desired, enable the PLL/DLL via an MRS command if it is not already enabled.
7. Issue MRS commands to adjust the programmable latencies (WL, RL, CRCWL, CRCRL, RAS, WR) and set other programmble features to their desired modes.
8. Perform WCK2CK training. As defined in the WCK2CK training process, if the PLL/DLL is enabled, then reset the PLL/DLL and wait t_{LK} clock cycles.
9. Exit WCK2CK training.
10. Perform READ and WRITE training, if required.
11. The device is ready for normal operation after any necessary interface training.

7.16 COMMAND TRUTH TABLES

Table 35 — Truth Table – CKE_n

CKE_n 2		CURRENT STATE 3,5	COMMAND(*n*) 4	ACTION(*n*) 4	NOTES
Previous Cycle (*n-1*)	Current Cycle (*n*)				
H	H	Power-Down	X	Maintain Power-Down	
H	H	Self Refresh	X	Maintain Self Refresh	
H	L	Power-Down	NOP	Exit Power-Down	
H	L	Self Refresh	NOP	Exit Self Refresh	6
L	H	All Banks Idle	NOP	Precharge Power-Down Entry	
L	H	Bank(s) Active	NOP	Active Power-Down Entry	
L	H	All Banks Idle	REFRESH	Self Refresh Entry	
L	L	See Table 36 and Table 37			

NOTE 1 H = Logic High Level; L = Logic Low Level. X = Don't Care (command decoder disabled).
NOTE 2 CKE_n(*n*) is the logic state of CKE_n at clock edge *n*; CKE_n(*n-1*) was the state of CKE_n at the previous clock edge.
NOTE 3 Current state is the state of the GDDR5X SGRAM immediately prior to clock edge n.
NOTE 4 COMMAND(*n*) is the command registered at clock edge *n*, and ACTION(*n*) is a result of COMMAND*n*.
NOTE 5 All states and sequences not shown are illegal or reserved.
NOTE 6 NOP commands should be issued on any clock edges occurring during the t_{XS} period. A minimum of t_{LK} is needed for the PLL/DLL to lock before applying a READ or WRITE command if the PLL/DLL was disabled.

7.16 COMMAND TRUTH TABLES (cont'd)

Table 36 — Truth Table – Current State Bank *n* – Command To Bank *n*

CURRENT STATE	RAS_n	CAS_n	WE_n	COMMAND/ACTION	NOTES
Any	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	H	H	ACTIVATE (select and activate row)	
	L	L	H	REFRESH / PER-BANK REFRESH	8
	L	L	L	MODE REGISTER SET	8
Row Active	H	L	H	READ (select column and start READ burst)	10
	H	L	L	WRITE (select column and start WRITE burst)	10,12
	L	H	L	PRECHARGE (deactivate row in bank or banks)	9
Read (Auto Precharge Disabled)	H	L	H	READ (select column and start new READ burst)	10
	H	L	L	WRITE (select column and start WRITE burst)	10, 11,12
	L	H	L	PRECHARGE (only after the READ burst is complete	9
Write (Auto Precharge Disabled)	H	L	H	READ (select column and start READ burst)	10
	H	L	L	WRITE (select column and start new WRITE burst)	10,12
	L	H	L	PRECHARGE (only after the WRITE burst is complete)	9

NOTE 1 H = Logic High Level; L = Logic Low Level.

NOTE 2 This table applies when CKE_n(*n-1)* was Low and CKE_n(*n*) is Low (see Table 35) and after t_{XS} has been met (if the previous state was self refresh).

NOTE 3 This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the following notes.

NOTE 4 Current state definitions:

- Idle: The bank has been precharged, and t_{RP} has been met.
- Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
- Read: A Read burst has been initiated, with auto precharge disabled.
- Write: A Write burst has been initiated, with auto precharge disabled.

NOTE 5 The following states must not be interrupted by a command issued to the same bank. NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 36, and according to Table 37.

- Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
- Row Activating: Starts with registration of an ACTIVATE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the "row active" state.
- Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
- Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

NOTE 6 The following states must not be interrupted by any executable command; NOP commands must be applied on each positive clock edge during these states.

- Refreshing: Starts with registration of a REFRESH command and ends when t_{RFC} is met. Once t_{RFC} is met, the device will be in the all banks idle state.
- Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the device will be in the all banks idle state.
- Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.
- READ or WRITE: Starts with the registration of the ACTIVATE command and ends the last valid data nibble.

NOTE 7 All states and sequences not shown are illegal or reserved.

NOTE 8 Not bank-specific (REFRESH, MODE REGISTER SET) or bank-specific (PER-BANK REFRESH); requires that all banks (REFRESH, MODE REGISTER SET) or the current bank (PER-BANK REFRESH) are idle, and bursts are not in progress.

NOTE 9 May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.

NOTE 10 Reads or Writes listed in the Command/Action column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.

NOTE 11 A WRITE command may be applied after the completion of the READ burst.

NOTE 12 WRITE in this table refers to WOM/WOMA, WOML/WOMLA, WOMU/WOMUA, WSM/WSMA and WDM/WDMA commands.

7.16 COMMAND TRUTH TABLES (cont'd)

Table 37 — Truth Table – Current State Bank *n* – Command To Bank *m*

CURRENT STATE	RAS_n	CAS_n	WE_n	COMMAND/ACTION	NOTES
Any	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	V	V	V	Any command otherwise allowed to bank m	
Row Activating, Active, or Precharging	L	H	H	ACTIVATE (select and activate row)	
	H	L	H	READ (select column and start READ burst)	7
	H	L	L	WRITE (select column and start WRITE burst)	7,9
	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	H	H	ACTIVATE (select and activate row)	
	H	L	H	READ (select column and start new READ burst)	7
	H	L	L	WRITE (select column and start WRITE burst)	7,8,9
	L	H	L	PRECHARGE	
Write (Auto Precharge Disabled)	L	H	H	ACTIVATE (select and activate row)	
	H	L	H	READ (select column and start READ burst)	7
	H	L	L	WRITE (select column and start new WRITE burst) (WOM, WSM or WDM)	7
	L	H	L	PRECHARGE	
Read (With Auto Precharge)	L	H	H	ACTIVATE (select and activate row)	
	H	L	H	READ (select column and start new READ burst)	7
	H	L	L	WRITE (select column and start WRITE burst)	7,8,9
	L	H	L	PRECHARGE	
Write (With Auto Precharge)	L	H	H	ACTIVATE (select and activate row)	
	H	L	H	READ (select column and start READ burst)	7
	H	L	L	WRITE (select column and start new WRITE burst)	7,9
	L	H	L	PRECHARGE	

NOTE 1 H = Logic High Level; L = Logic Low Level; V = Valid Signal (H or L, but not floating).

NOTE 2 This table applies when CKE_n*(n-1)* was Low and CKE_n*(n)* is Low (see Table 35) and after t_{XS} has been met (if the previous state was self refresh).

NOTE 3 This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the following notes.

NOTE 4 Current state definitions:

Idle: The bank has been precharged, and t_{RP} has been met.

Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

Read: A Read burst has been initiated, with auto precharge disabled.

Write: A Write burst has been initiated, with auto precharge disabled.

Read with Auto Precharge Enabled: See 4a and 4b.

Write with Auto Precharge Enabled: See 4a and 4b.

4a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVATE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

4b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized in Table 38.

NOTE 5 REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.

NOTE 6 All states and sequences not shown are illegal or reserved.

NOTE 7 Reads or Writes listed in the Command/Action column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.

NOTE 8 A WRITE command may be applied after the completion of the READ burst.

NOTE 9 WRITE in this table refers to WOM/WOMA, WOML/WOMLA, WOMU/WOMUA, WSM/WSMA and WDM/WDMA commands.

7.16 COMMAND TRUTH TABLES (cont'd)

Table 38 — Minimum Delay Between Commands to Different Banks with Auto Precharge Enabled

From Command	To Command	Minimum delay (with concurrent auto precharge)	Notes
WRITE with AUTO PRECHARGE (WOMA, WOMLA, WOMUA)	READ or READ with Auto Precharge	[WLmrs + (BL/8)] * t_{CK} + t_{WTR} [WLmrs + (BL/4)] * t_{CK} + t_{WTR}	2,3,4
	WRITE or WRITE with Auto Precharge	t_{CCD}	5,6
	PRECHARGE	1 * t_{CK}	
	ACTIVATE	1 * t_{CK}	
WRITE with AUTO PRECHARGE (WDMA)	READ or READ with Auto Precharge	[WLmrs + (BL/8)] * t_{CK} + t_{WTR} [WLmrs + (BL/4)] * t_{CK} + t_{WTR}	2,3,4
	WRITE or WRITE with Auto Precharge	t_{CCD}	5,6
	PRECHARGE	2 * t_{CK}	
	ACTIVATE	2 * t_{CK}	
WRITE with AUTO PRECHARGE (WSMA)	READ or READ with Auto Precharge	[WLmrs + (BL/8)] * t_{CK} + t_{WTR} [WLmrs + (BL/4)] * t_{CK} + t_{WTR}	2,3,4
	WRITE or WRITE with Auto Precharge	MAX [t_{CCD}, 3 * t_{CK}]	5,6
	PRECHARGE	3 * t_{CK}	
	ACTIVATE	3 * t_{CK}	
READ with AUTO PRECHARGE	READ or READ with Auto Precharge	t_{CCD}	5
	WRITE or WRITE with Auto Precharge	[RLmrs + (BL/8) + t_{CCD} - WLmrs] * t_{CK} [RLmrs + (BL/4) + t_{CCD} - WLmrs] * t_{CK}	2,3,6
	PRECHARGE	1 * t_{CK}	
	ACTIVATE	1 * t_{CK}	

NOTE 1 RLmrs = READ latency (RL)
NOTE 2 BL = Burst length; use "BL/8" in QDR operating mode and "BL/4" in DDR operating mode.
NOTE 3 WLmrs = WRITE latency.
NOTE 4 t_{WTR} = t_{WTRL} if Bank Groups enabled and access to the same bank group otherwise t_{WTR} = t_{WTRS}.
NOTE 5 t_{CCD} = t_{CCDL} if Bank Groups enabled and access to the same bank group otherwise t_{CCD} = t_{CCDS}.
NOTE 6 WRITE in the "To Command" column refers to WOM/WOMA, WOML/WOMLA, WOMU/WOMUA, WSM/WSMA, and WDM/WDMA commands.

8 OPERATING CONDITIONS

8.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational clauses of this standard is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 39 — Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Voltage on V_{DD} pin relative to V_{SS}	V_{DD}	-0.3	+2.0	V	1
Voltage on V_{DDQ} pin relative to V_{SS}	V_{DDQ}	-0.3	+2.0	V	1
Voltage on V_{PP} pin relative to V_{SS}	V_{PP}	-0.3	+2.3	V	1, 2
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3	+2.0	V	
Storage temperature	T_{STG}	-55	+125	°C	

NOTE 1 V_{DD} and V_{DDQ} must be within 300 mV of each other at all times the device is powered-up.
NOTE 2 V_{PP} must be equal or greater than V_{DD} and V_{DDQ} at all times the device is powered-up.

8.2 PAD CAPACITANCES

Table 40 — Silicon Pad Capacitances

PARAMETER 1	SYMBOL	MIN	MAX	UNIT	NOTES
Delta Input/Output Capacitance: DQs, DBI_n, EDC	DC_{IO}			pF	2
Delta Input Capacitance: Command and Address	DC_{I1}			pF	3, 6
Delta Input Capacitance: CK_t, CK_c	DC_{I2}		0.1	pF	4
Delta Input Capacitance: WCK_t, WCK_c	DC_{I3}		0.1	pF	5
Input/Output Capacitance: DQs, DBI_n, EDC	C_{IO}			pF	
Input Capacitance: Command and Address	C_{I1}			pF	6
Input Capacitance: CK_t, CK_c	C_{I2}			pF	
Input Capacitance: WCK_t, WCK_c	C_{I3}			pF	

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The silicon pad capacitance is validated by deembedding the package L & C parasitics. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied with all other signal pins floating.
NOTE 2 $DC_{IO} = C_{IO}(Max) - C_{IO}(Min)$
NOTE 3 $DC_{I1} = C_{I1}(Max) - C_{I1}(Min)$
NOTE 4 DC_{I2} = Absolute value of C_{I2} CK_t – C_{I2} CK_c
NOTE 5 DC_{I3} = Absolute value of C_{I3} WCK_t – C_{I3} WCK_c
NOTE 6 Command and address pins: CKE_n, RAS_n, CAS_n, WE_n, ABI_n and all address inputs

8.3 PACKAGE ELECTRICAL SPECIFICATION

Table 41 — Package Electrical Specifications

PARAMETER 1, 2, 3	SYMBOL	MIN	MAX	UNIT	NOTES
Input/Output package impedance: DQs, DBI_n, EDC	Z_{IO}			Ω	
Input/Output package delay: DQs, DBI_n, EDC	Td_{IO}			ps	
Input package impedance: Command and Address	Z_{I1}			Ω	4
Input package delay: Command and Address	Td_{I1}			ps	4
Input package impedance: CK_t, CK_c	Z_{I2}			Ω	
Input package delay: CK_t, CK_c	Td_{I2}			ps	
Delta input package impedance: CK_t, CK_c	DZ_{I2}	–		Ω	5
Delta input package delay: CK_t, CK_c	DTd_{I2}	–		ps	6
Input package impedance: WCK_t, WCK_c	Z_{I3}			Ω	
Input package delay: WCK_t, WCK_c	Td_{I3}			ps	
Delta input package impedance: WCK_t, WCK_c	DZ_{I3}	–		Ω	7
Delta input package delay: WCK_t, WCK_c	DTd_{I3}	–		ps	8

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package L & C parasitics are validated using package only samples. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS} and V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{DD}, V_{DDQ}, V_{SS} and V_{SSQ} shorted and all other signal pins shorted at the die side (not pin).

NOTE 2 Package only impedance (Z_{pkg}) is calculated based on the L_{pkg} and C_{pkg} total for a given pin where

$$Z_{pkg}(\text{total per pin}) = \sqrt{L_{pkg}/C_{pkg}}$$

NOTE 3 Package only delay(Td_{pkg}) is calculated based on L_{pkg} and C_{pkg} total for a given pin where

$$Td_{pkg}(\text{total per pin}) = \sqrt{L_{pkg} * C_{pkg}}$$

NOTE 4 Command and address pins: CKE_n, RAS_n, CAS_n, WE_n, ABI_n and all address inputs
NOTE 5 DZ_{I2} = Absolute value of Z_{I2} CK_t – Z_{I2} CK_c
NOTE 6 DTd_{I2} = Absolute value of Td_{I2} CK_t – Td_{I2} CK_c
NOTE 7 DZ_{I3} = Absolute value of Z_{I3} WCK_t – Z_{I3} WCK_c
NOTE 8 DTd_{I3} = Absolute value of Td_{I3} WCK_t – Td_{I3} WCK_c

8.4 PACKAGE THERMAL CHARACTERISTICS

Table 42 — Thermal Characteristics

PARAMETER 1, 2	SYMBOL	MIN	MAX	UNIT	NOTES
Operating case temperature	TC			°C	3
Thermal resistance junction to ambient	Theta_JA			°C/W	4, 5, 6
Thermal resistance junction to board	Theta_JB			°C/W	4, 7
Thermal resistance from junction to case	Theta_JC			°C/W	7

NOTE 1 Measurement procedures for each parameter must follow those defined in the JEDEC JESD-51 standard.
NOTE 2 Values are guaranteed by design but not tested in production.
NOTE 3 TC is documented for normal operation and is not intended to reflect reliability limits.
NOTE 4 Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
NOTE 5 Airflow information must be documented for Theta_JA.
NOTE 6 Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction temperature prediction.
NOTE 7 Theta_JB and Theta_JC are derived through a package thermal simulation.

8.5 ELECTROSTATIC DISCHARGE SENSITIVITY CHARACTERISTICS

Table 43 — Electrostatic Discharge Sensitivity Characteristics

PARAMETER 1, 2	SYMBOL	MIN	MAX	UNIT	NOTES
Human body model (HBM)	ESD_{HBM}	1000	–	V	3
Charged-device model (CDM)	ESD_{CDM}	250	–	V	4

NOTE 1 Electrostatic discharge minimum requirements are defined for the high-speed interface pins of the device only. They do not apply to pins MF, ZQ, RESET_n, TCK, TMS, TDI and TDO.
NOTE 2 State-of-the-art basic ESD control measures have to be in place when handling the device.
NOTE 3 Refer to ESDA / JEDEC Joint Standard JS-001-2012 for measurement procedures.
NOTE 4 Refer to JESD22-C101F for measurement procedures.

8.6 DC and AC OPERATING CONDITIONS

GDDR5X SGRAMs are designed for 1.35 V typical operating voltages. The interface of GDDR5X SGRAMs follows the POD135 standard (JESD8-21A). All AC and DC values are measured at the ball.

Table 44 — DC Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTES
Device supply voltage	V_{DD}	1.3095	1.35	1.3905	V	1
Output supply voltage	V_{DDQ}	1.3095	1.35	1.3905	V	1
Pump voltage	V_{PP}	1.746	1.8	1.908	V	2
Reference voltage: DQ and DBI_n pins	V_{REFD}	0.69 * V_{DDQ}		0.71 * V_{DDQ}	V	3, 4
	V_{REFD2}	0.49 * V_{DDQ}		0.51 * V_{DDQ}	V	3, 4, 5
Reference voltage: ADD/CMD pins	V_{REFC}	0.69 * V_{DDQ}		0.71 * V_{DDQ}	V	6
	V_{REFC2}	0.49 * V_{DDQ}		0.51 * V_{DDQ}	V	6
DC input logic high voltage with V_{REFC}: ADD/CMD pins	V_{IHA}(DC)	V_{REFC} + 0.135			V	7, 9
DC input logic low voltage with V_{REFC}: ADD/CMD pins	V_{ILA}(DC)			V_{REFC} - 0.135	V	7, 9
DC input logic high voltage with V_{REFC2}: ADD/CMD pins	V_{IHA2}(DC)	V_{REFC2} + 0.27			V	9
DC input logic low voltage with V_{REFC2}: ADD/CMD pins	V_{ILA2}(DC)			V_{REFC2} - 0.27	V	9
DC input logic high voltage with V_{REFD}: DQ and DBI_n pins	V_{IHD}(DC)	V_{REFD} + 0.09			V	8, 9
DC input logic low voltage with V_{REFD}: DQ and DBI_n pins	V_{ILD}(DC)			V_{REFD} - 0.09	V	8, 9
DC input logic high voltage with V_{REFD2}: DQ and DBI_n pins	V_{IHD2}(DC)	V_{REFD2} + 0.27			V	9
DC input logic low voltage with V_{REFD2}: DQ and DBI_n pins	V_{ILD2}(DC)			V_{REFD2} - 0.27	V	9
RESET_n, MF and Boundary Scan input logic high voltage; EDC1/2 input logic high voltage for x32/x16 mode select	V_{IHR}	0.8 * V_{DDQ}			V	9
RESET_n, MF and Boundary Scan input logic low voltage; EDC1/2 input logic low voltage for x32/x16 mode select	V_{ILR}			0.2 * V_{DDQ}	V	9
Input leakage current (any input 0V <= V_{IN} <= V_{DDQ}; all other pins not under test = 0V)	I_L				µA	
Output Leakage Current (outputs are disabled; 0V <= V_{OUT} <= V_{DDQ})	I_{OZ}				µA	
Output logic low voltage	V_{OL}(DC)			0.56	V	

NOTE 1 GDDR5X SGRAMs are designed to tolerate PCB designs with separate V_{DD} and V_{DDQ} power regulators.
NOTE 2 DC bandwidth is limited to 20 MHz.
NOTE 3 AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design.
NOTE 4 The reference voltage source and control for DQ and DBI_n pins are determined by Half VREFD, VREF C2D and VREFD Level mode register bits.
NOTE 5 Programmable V_{REFD} levels are not supported with V_{REFD2}.
NOTE 6 The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by Half VREFC mode register bit.
NOTE 7 ADD/CMD input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFC} crossing and V_{IHA}(AC) or V_{ILA}(AC).
NOTE 8 DQ/DBI_n input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFD} crossing and VI_{HD}(AC) or V_{ILD}(AC) or V_{REFD2} crossing and VI_{HD2}(AC) or V_{ILD2}(AC).
NOTE 9 V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS and TCK. V_{IHR} and V_{ILR} also apply to ADD/CMD, CK_t/_c, DQ, DBI_n and WCK_t/_c input pins when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.

8.6 DC and AC OPERATING CONDITIONS (cont'd)

Table 45 — AC Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTES
AC input logic high voltage with V_{REFC}: ADD/CMD pins	$V_{IHA}(AC)$	V_{REFC} + 0.18			V	
AC input logic low voltage with V_{REFC}: ADD/CMD pins	$V_{ILA}(AC)$			V_{REFC} - 0.18	V	
AC input logic high voltage with V_{REFC2}: ADD/CMD pins	$V_{IHA2}(AC)$	V_{REFC} + 0.36			V	
AC input logic low voltage with V_{REFC2}: ADD/CMD pins	$V_{ILA2}(AC)$			V_{REFC} - 0.36	V	
AC input logic high voltage with V_{REFD}: DQ and DBI_n pins	$V_{IHD}(AC)$	V_{REFD} + 0.135			V	
AC input logic low voltage with V_{REFD}: DQ and DBI_n pins	$V_{ILD}(AC)$			V_{REFD} - 0.135	V	
AC input logic high voltage with V_{REFD2}: DQ and DBI_n pins	$V_{IHD2}(AC)$	V_{REFD2} + 0.36			V	
AC input logic low voltage with V_{REFD2}: DQ and DBI_n pins	$V_{ILD2}(AC)$			V_{REFD2} - 0.36	V	
NOTE 1 Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.						

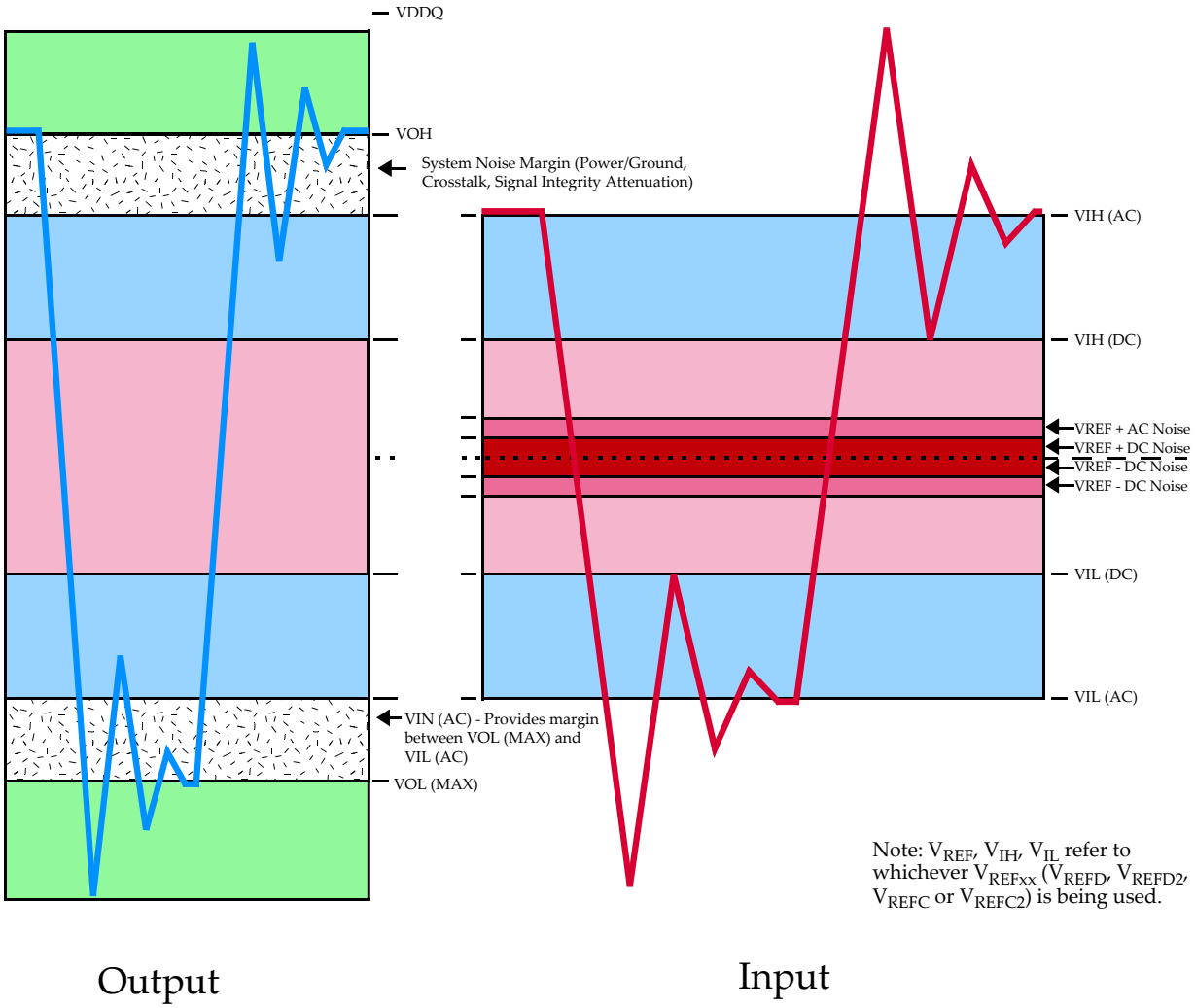


Figure 104 — Voltage Waveform

8.6 DC and AC OPERATING CONDITIONS (cont'd)

Table 46 — Clock Input Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Clock input mid-point voltage: CK_t, CK_c	$V_{MP}(DC)$	V_{REFC} - 0.10	V_{REFC} + 0.10	V	1, 6
Clock input differential voltage: CK_t, CK_c	$V_{IDCK}(DC)$	0.198		V	4, 6
Clock input differential voltage: CK_t, CK_c	$V_{IDCK}(AC)$	0.36		V	2, 4, 6
Clock input differential voltage: WCK_t, WCK_c	$V_{IDWCK}(DC)$	0.18		V	5, 7
Clock input differential voltage: WCK_t, WCK_c	$V_{IDWCK}(AC)$	0.27			2, 5, 7
Single ended clock input voltage level: CK_t, CK_c, WCK_t, WCK_c	V_{IN}	-0.30	V_{DDQ} + 0.30		14
Single ended slew rate: CK_t, CK_c	CK_{SLEW}	2.7		V/ns	9
Single ended slew rate: WCK_t, WCK_c	WCK_{SLEW}	2.7		V/ns	10
Clock input crossing point voltage; CK_t, CK_c	$V_{IXCK}(AC)$	V_{REFC} - 0.108	V_{REFC} + 0.108	V	2, 3, 6
Clock input crossing point voltage: WCK_t, WCK_c	$V_{IXWCK}(AC)$	V_{REFD} - 0.09	V_{REFD} + 0.09	V	2, 3, 7, 8
Allowed time before ringback of CK/WCK below $V_{IDCK}(AC)/V_{IDWCK}(AC)$	t_{DVAC}			ps	11, 12, 13

NOTE 1 This provides a minimum of 0.845 V to a maximum of 1.045 V, and is normally 70% of V_{DDQ}. DRAM timings relative to CK_t cannot be guaranteed if these limits are exceeded.
NOTE 2 For AC operations, all DC clock requirements must be satisfied as well.
NOTE 3 The value of V_{IXCK} and V_{IXWCK} is expected to equal 70% V_{DDQ} for the transmitting device and must track variations in the DC level of the same.
NOTE 4 V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
NOTE 5 V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD} or V_{REFD2}.
NOTE 6 The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Please refer to the applicable timings in Table 54, AC timings table.
NOTE 7 The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Please refer to the applicable timings in Table 54, AC Timings table.
NOTE 8 V_{REFD} is either V_{REFD}, V_{REFD2} or V_{REFC}.
NOTE 9 The slew rate is measured between V_{REFC} crossing and $V_{IXCK}(AC)$.
NOTE 10 The slew rate is measured between V_{REFD} crossing and $V_{IXWCK}(AC)$.
NOTE 11 Figure 105 illustrates the exact relationship between (CK_t - CK_c) or (WCK_t - WCK_c) and $V_{ID}(AC)$, $V_{ID}(DC)$ and t_{DVAC}.
NOTE 12 Ringback below $V_{ID}(DC)$ is not allowed.
NOTE 13 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.
NOTE 14 Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the Capture-DR TAP controller state.

8.6 DC and AC OPERATING CONDITIONS (cont'd)

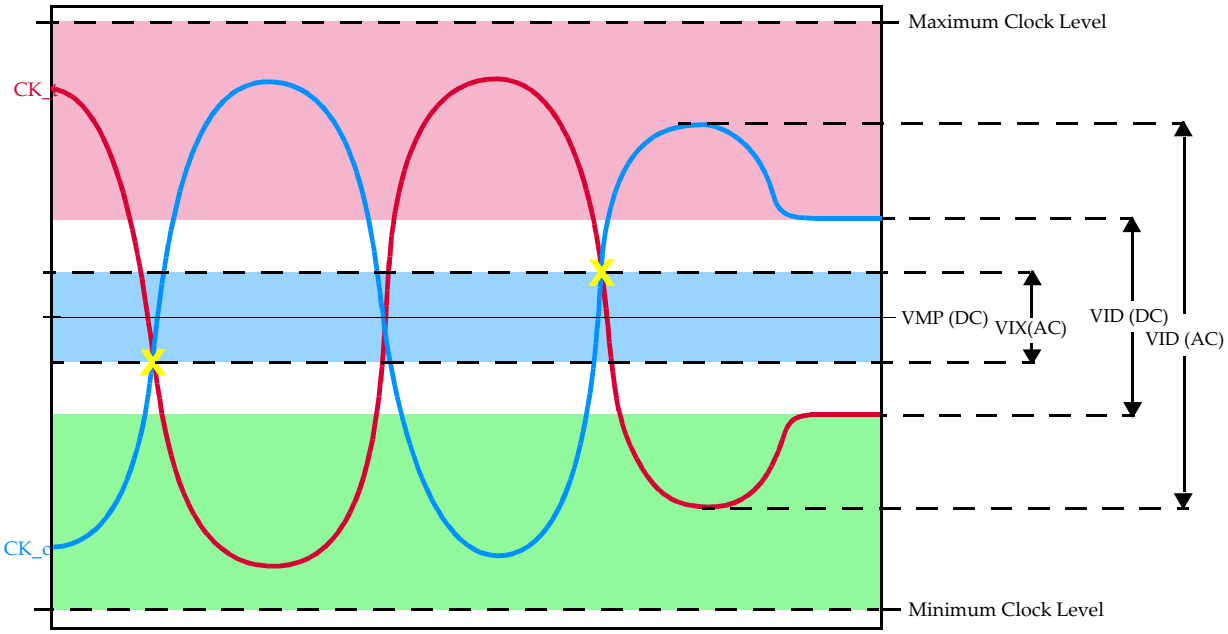


Figure 105 — Clock Waveform

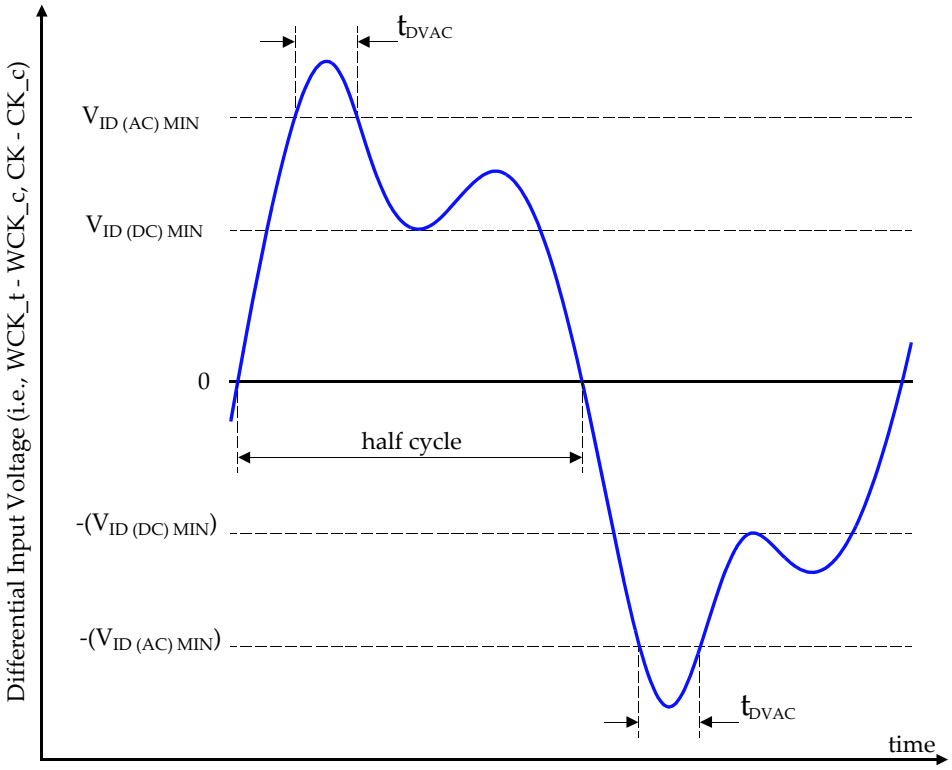


Figure 106 — Definition of Differential AC-Swing and "Time Above AC-Level" t_{DVAC}

8.7 IDD AND IPP SPECIFICATIONS and TEST CONDITIONS

Table 47 — IDD Specifications and Test Conditions

PARAMETER/CONDITION	SYMBOL	NOTES
One Bank Activate Precharge Current: $t_{CK} = t_{CK}(min)$; $t_{WCK} = t_{WCK}(min)$; $t_{RC} = t_{RC}(min)$; CKE_n = Low; DQ, DBI_n are High; bank and row addresses as defined in Table 48 with ACT command	I_{DD0}	1
One Bank Activate Precharge I_{PP} Current	I_{PP0}	1,2
One Bank Activate Read Precharge Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; $t_{RC} = t_{RC}(min)$; CKE_n = Low; one bank activated; single read burst with 50% data toggle on each data transfer, with 4 outputs per data byte driven Low; otherwise DQ, DBI_n are High; bank, row and column addresses as defined in Table 49 with ACT and READ commands; I_{OUT} = 0mA	I_{DD1}	1
Precharge Power-down Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; all banks idle; CKE_n = High; all other inputs are High; PLL/DLLs are off	I_{DD2P}	
Precharge Standby Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; all banks idle; CKE_n = Low; all other inputs are High	I_{DD2N}	
Active Power-down Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; one bank active; CKE_n = High; all other inputs are High	I_{DD3P}	
Active Standby Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; one bank active; CKE_n = Low; all other inputs are High	I_{DD3N}	
Active Standby I_{PP} Current	I_{PP3N}	1,2
Read Burst Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; CKE_n = Low; one bank in each of the 4 bank groups activated; continuous read burst across bank groups with 50% data toggle on each data transfer as defined in Table 50; bank and column addresses as defined in Table 50 with READ command; I_{OUT} = 0mA	I_{DD4R}	
Write Burst Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; CKE_n = Low; one bank in each of the 4 bank groups activated; continuous write burst across bank groups with 50% data toggle on each data transfer as defined in Table 51; bank and column addresses as defined in Table 51 with WRITE command; no data mask	I_{DD4W}	
Refresh Current: $t_{CK} = t_{CK}$ (min); $t_{WCK} = t_{WCK}(min)$; $t_{RFC} = t_{RFC}(min)$; CKE_n = Low; DQ, DBI_n are High; address inputs are High	I_{DD5}	1
Refresh I_{PP} Current	I_{PP5}	1,2
Self Refresh Current: CKE_n = High; all other inputs are High	I_{DD6}	
Four Bank Interleave Read Current: $t_{CK} = t_{CK}(min)$; $t_{WCK} = t_{WCK}(min)$; CKE_n = Low; one bank in each of the 4 bank groups activated and precharged at $t_{RC}(min)$; continuous read burst across bank groups as defined in Table ; bank, row and column addresses as defined in Table with ACT and READ/READA commands; I_{OUT} = 0mA	I_{DD7}	
Four Bank Interleave Read I_{PP} Current	I_{PP7}	1,2

NOTE 1 Min t_{RC} or t_{RFC} for IDD measurements is the smallest multiple of t_{CK} that meets the minimum of the absolute value for the respective parameter.
NOTE 2 I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions. I_{PP3N} test and limit is applicable for all I_{DD2X}, I_{DD3X}, I_{DD4X} and I_{DD6} conditions.
NOTE 3 See DRAM vendor datasheets for t_{RAS}, t_{RCDRD}, t_{RC}, t_{RFC} values.

Common Test Conditions:

- Device is configured to QDR mode
- Device is configured to x32 mode first and then to x16 mode (if x16 mode is supported; 2 separate measurements)
- ABI and DBI are enabled
- Address inputs include ABI_n pin
- Each data byte consists of eight DQs and one DBI_n pin
- All ODTs are enabled with ZQ/2
- The PLL/DLLs is enabled unless noted otherwise
- CRC is enabled for READs and WRITEs, and the EDC hold pattern is programmed to '1010'

8.7 IDD AND IPP SPECIFICATIONS and TEST CONDITIONS (cont'd)

- Bank groups are enabled if required for device operation at t_{CK}(min)
- NOP condition during idle command cycles
- Data pattern (BL=16):
  DATA0 = 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh
  DATA1 = 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h 1Eh 55h

Table 48 — IDD0 Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	ACT	0	1	1	0 1	1111 0001	1 0	00 11	00 11	–
	1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...	repeat NOP until cycle (nRAS -1)									
	nRAS	PRE	0	1	0	1 1	0000 1111	1 1	11 11	10 11	–
	nRAS + 1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...	repeat NOP until cycle (nRC -1)									
1	nRC	repeat sub-loop 0 pattern until cycle (2* nRC -1); use BA = 03h and RA = 03C7h instead									
2	2* nRC	repeat sub-loop 0 pattern until cycle (3* nRC -1); use BA = 04h and RA = 07C7h instead									
3	3* nRC	repeat sub-loop 0 pattern until cycle (4* nRC -1); use BA = 07h and RA = 01C7h instead									

Table 49 — IDD1 Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	ACT	0	1	1	0 1	1111 0001	1 0	00 11	00 11	–
	1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...	repeat NOP until cycle (nRCDRD -1)									
	nRCDRD	READ	1	0	1	0 1	1111 0011	0 1	11 10	01 00	DATA0
	nRCDRD + 1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...	repeat NOP until cycle (nRAS -1)									
	nRAS	PRE	0	1	0	0 1	1111 1111	1 1	11 11	10 11	–
	nRAS + 1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	...	repeat NOP until cycle (nRC -1)									
1	nRC	repeat sub-loop 0 pattern until cycle (2* nRC -1); use BA = 03h, RA = 03C7h, CA = 23h and DATA1 instead									
2	2* nRC	repeat sub-loop 0 pattern until cycle (3* nRC -1); use BA = 04h, RA = 07C7h, CA = 4Ch and DATA0 instead									
3	3* nRC	repeat sub-loop 0 pattern until cycle (4* nRC -1); use BA = 07h, RA = 01C7h, CA = 23h and DATA1 instead									

8.7 IDD AND IPP SPECIFICATIONS and TEST CONDITIONS (cont'd)

Table 50 — IDD4R Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	READ	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA0
	1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	2	READ	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA1
	3	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	4	READ	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA0
	5	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	6	READ	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA1
	7	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–

Table 51 — IDD4W Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	WRITE	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA0
	1	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	2	WRITE	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA1
	3	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	4	WRITE	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA0
	5	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	6	WRITE	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA1
	7	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–

8.7 IDD AND IPP SPECIFICATIONS and TEST CONDITIONS (cont'd)

Table 52 — IDD7 Measurement-Loop Pattern

Sub-Loop	Cycle Number	Command	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	0	ACT	0	1	1	0 1	0111 0001	1 0	10 11	00 11	–
	1	READ	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA0
	2	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	3	READ	1	0	1	1 1	0111 0011	1 1	00 10	00 00	DATA1
	4	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	5	READ	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA0
	6	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	7	READ	1	0	1	1 1	0011 0011	0 1	00 10	10 00	DATA1
	8	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	9	READA	1	0	1	1 1	0011 1000	0 1	00 01	11 01	DATA0
	10	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	11	READ	1	0	1	1 1	0111 0011	1 1	00 10	00 00	DATA1
	12	ACT	0	1	1	0 1	1011 0001	1 0	10 11	00 11	–
	13	READ	1	0	1	1 1	0111 1000	1 1	00 01	00 01	DATA0
	14	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	15	READ	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA1
	16	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	17	READ	1	0	1	0 1	0111 1000	0 1	11 01	01 01	DATA0
	18	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	19	READ	1	0	1	1 1	0111 0011	1 1	00 10	00 00	DATA1
	20	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	21	READA	1	0	1	1 1	0111 1000	1 1	00 01	01 01	DATA0
	22	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	23	READ	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA1

Table 52 — IDD7 Measurement-Loop Pattern (cont'd)

Sub-Loop	Cycle Number	Command	RAS_n	CAS_n	WE_n	ABI_n	BA[3:0] A[5:2]	A[12] A[13]	A[11:10] A[6;0]	A[9:8] A[7;1]	Data
0	24	ACT	0	1	1	0 1	1100 0001	1 0	11 11	00 11	–
	25	READ	1	0	1	0 1	0111 1000	0 1	11 01	01 01	DATA0
	26	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	27	READ	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA1
	28	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	29	READ	1	0	1	0 1	1011 1000	1 1	11 01	01 01	DATA0
	30	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	31	READ	1	0	1	0 1	0111 0011	0 1	11 10	01 00	DATA1
	32	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	33	READA	1	0	1	0 1	0111 1000	0 1	11 01	10 01	DATA0
	34	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	35	READ	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA1
	36	ACT	0	1	1	1 1	0111 0001	1 0	00 11	01 11	–
	37	READ	1	0	1	0 1	1011 1000	1 1	11 01	01 01	DATA0
	38	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	39	READ	1	0	1	1 1	0011 0011	0 1	00 10	10 00	DATA1
	40	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	41	READ	1	0	1	1 1	0011 1000	0 1	00 01	10 01	DATA0
	42	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	43	READ	1	0	1	0 1	1011 0011	1 1	11 10	01 00	DATA1
	44	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	45	READA	1	0	1	0 1	1011 1000	1 1	11 01	10 01	DATA0
	46	NOP	1	1	1	1	1111 1111	1 1	11 11	11 11	–
	47	READ	1	0	1	1 1	0011 0011	0 1	00 10	10 00	DATA1

8.7 IDD AND IPP SPECIFICATIONS and TEST CONDITIONS (cont'd)

Table 53 — Self Refresh Current Definitions

SYMBOL	TEMPERATURE RANGE	VALUE	UNIT	NOTES
IDD6N	0^oC - T_N		mA	2, 3, 8
IDD6E (optional)	0^oC - T_E		mA	1, 3, 4, 9
IDD6R (optional)	0^oC - T_R		mA	3, 5, 10
IDD6A (optional)	0^oC - T_a		mA	3, 5, 6, 7
	T_b - T_y (optional)		mA	3, 5, 6, 7
	T_z - $T_{OPERmax}$		mA	3, 5, 6, 7, 11

NOTE 1 Max. values for IDD currents considering worst case conditions of process, temperature and voltage.
NOTE 2 Applicable for MR3 setting A[1:0] = 00.
NOTE 3 Supplier data sheets include a max value.
NOTE 4 IDD6E is only specified for devices which support the Extended Temperature Range feature. Refer to the supplier datasheet for the appropriate MR3 setting.
NOTE 5 Refer to the supplier data sheet for the value specification method (e.g., max, typical) for IDD6E and IDD6A.
NOTE 6 IDD6A is specified for the Temperature Controlled Self Refresh (TCSR) feature enabled by MR3 A[1:0] = 11.
NOTE 7 The number of discrete temperature ranges supported and the associated T_a - T_z, and $T_{OPERmax}$ values are supplier/ design specific. Temperature ranges are intended to denote the nominal trip points for the internal temperature sensor to bracket discrete self refresh rates internal to the DRAM. Refer to supplier datasheet for more information.
NOTE 8 When TCSR is disabled, T_N represents the temperature limit for normal operation of the device.
NOTE 9 When TCSR is disabled, some devices may support an extended temperature range that is typically 10 ^oC higher than T_N and often requires additional refresh cycles. T_E represents this extended temperature limit.
NOTE 10 T_R represents the temperature used to reflect the current consumed in a typical room temperature environment.
NOTE 11 $T_{OPERmax}$ represents the max temperature supported by the device when TCSR is enabled.

8.8 AC TIMINGS

Table 54 — AC Timings

PARAMETER 1, 2			SYMBOL	VALUES		UNIT	NOTES
				MIN	MAX		
CK_t and WCK_t Timings							
CK clock cycle time	QDR mode	PLL/DLL on	t_{CK}			ns	
	DDR mode	PLL/DLL on					
		PLL/DLL off					
CK clock high-level width			t_{CH}			t_{CK}	3
CK clock low-level width			t_{CL}			t_{CK}	3
Min. CK clock half period			t_{HP}	min(t_{CH},t_{CL})	–	t_{CK}	
CK clock frequency	QDR mode		f_{CK}	50		MHz	
	DDR mode			50			
CK clock frequency with bank groups disabled			f_{CKBG}	f_{CK}(min)		MHz	4,5
CK clock frequency with bank groups enabled and t_{CCDL} = 3 t_{CK}			f_{CKBG3}	f_{CK}(min)		MHz	4
CK clock frequency with WCK2CK alignment at pins			f_{CKPIN}	f_{CK}(min)		MHz	6
CK clock frequency in RDQS Mode			f_{CKRDQS}	f_{CK}(min)		MHz	7
CK clock frequency for device operation with VREFC2			$f_{CKVREFC2}$	f_{CK}(min)		MHz	8
CK clock frequency for device operation with VREFD2			$f_{CKVREFD2}$	f_{CK}(min)		MHz	9
CK clock frequency for WCK-to-CK auto synchronization in WCK2CK training mode			$f_{CKAUTO-SYNC}$	f_{CK}(min)		MHz	10
CK clock frequency for device operation with LP1 low power mode enabled			f_{CKLP1}	f_{CK}(min)		MHz	11
CK clock frequency for device operation with Low Frequency Mode enabled			f_{CKLF}	f_{CK}(min)		MHz	12
WCK clock cycle time	QDR mode	PLL/DLL on	t_{WCK}			ns	13
	DDR mode	PLL/DLL on					
		PLL/DLL off					
WCK clock high-level width			t_{WCKH}			t_{WCK}	14,15
WCK clock low-level width			t_{WCKL}			t_{WCK}	14,15
Min. WCK clock half period			t_{WCKHP}	min (t_{WCKH},t_{WCKL})	–	t_{WCK}	
Command and Address Input Timings							
Command input setup time			t_{CMDS}		–	ns	16,17
Command input hold time			t_{CMDH}		–	ns	16,17
Command input pulse width			t_{CMDPW}		–	ns	16,17,18
Address input setup time			t_{AS}		–	ns	16,17,19
Address input hold time			t_{AH}		–	ns	16,17,19
Address input pulse width			t_{APW}		–	ns	16,17,18, 19

Table 54 — AC Timings (cont'd)

PARAMETER 1, 2		SYMBOL	VALUES		UNIT	NOTES
			MIN	MAX		
WCK2CK Timings						
WCK stop to MRS delay for entering WCK2CK training		$t_{WCK2MRS}$		–	ns	
MRS to WCK restart delay after entering WCK2CK training		$t_{MRSTWCK}$		–	ns	20
WCK clock frequency for WCK2CK training with WCK stop		$f_{WCKSTOP}$	–		MHz	
WCK start to WCK phase movement delay		t_{WCK2TR}		–	t_{CK}	
WCK phase change to phase detector out delay		t_{WCK2PH}		–	ns	
WCK clock high-level width during WCK2CK training		t_{WCKHTR}			t_{WCK}	14,15,21
WCK clock low-level width during WCK2CK training		t_{WCKLTR}			t_{WCK}	14,15,21
WCK2CK offset when zero offset at phase detector or at pins	PLL/DLL on; MR7A0=0 (at phase detector)	$t_{WCK2CKPIN}$			ns	22
	PLL/DLL on; MR7A0=1 (at pins)					
	PLL/DLL off; MR7A0=0 (at phase detector)					
	PLL/DLL off; MR67A0=1 (at pins)					
WCK2CK phase offset upon WCK2CK training exit	MR7A0=0 (at phase detector)	$t_{WCK2CK-SYNC}$			t_{CK}	23
	MR7A0=1 (at pins)				ns	
WCK2CK phase offset	MR7A0=0 (at phase detector)	t_{WCK2CK}			t_{CK}	24
	MR7A0=1 (at pins)				ns	
Data Input and Output Timings						
WCK to DQ/DBI_n offset for input data	PLL/DLL on	$t_{WCK2DQI}$			ns	25
	PLL/DLL off					
WCK to DQ/DBI_n/EDC offset for output data	PLL/DLL on	$t_{WCK2DQO}$			ns	26,27
	PLL/DLL off					
DQ/DBI_n input pulse width		t_{DIPW}		–	ns	28,29,30
DQ/DBI_n data input valid window	PLL/DLL on	t_{DIVW}		–	ns	28,29,31
	PLL/DLL off			–	ns	
DQ/DBI_n input skew within double byte		t_{DQDQI}			ns	32
DQ/DBI_n/EDC output skew within double byte		t_{DQDQO}			ns	33
Row Access Timings						
ACTIVATE to ACTIVATE command period		t_{RC}		–	ns	
ACTIVATE to PRECHARGE command period		t_{RAS}		$9 * t_{REFI}$	ns	34
ACTIVATE to READ command delay		t_{RCDRD}		–	ns	
ACTIVATE to WRITE command delay		t_{RCDWR}		–	ns	

Table 54 — AC Timings (cont'd)

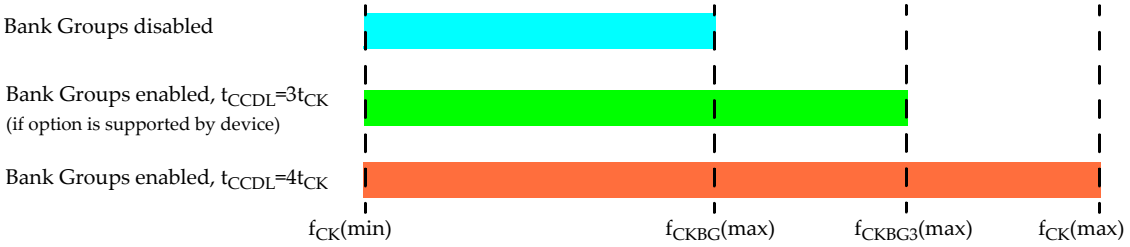
PARAMETER 1, 2	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
Row Access Timings (cont'd)					
ACTIVATE to RDTR command delay	t_{RCDRTR}		–	ns	
ACTIVATE to WRTR command delay	t_{RCDWTR}		–	ns	
ACTIVATE to LDFF command delay	t_{RCDLTR}		–	ns	
REFRESH to RDTR or WRTR command delay	t_{REFTR}		–	ns	
ACTIVATE bank A to ACTIVATE bank B command delay same bank group	t_{RRDL}		–	ns	35
ACTIVATE bank A to ACTIVATE bank B command delay different bank groups	t_{RRDS}		–	ns	36
Four bank activate window	t_{FAW}		–	ns	37
Thirty two bank activate window	t_{32AW}		–	ns	38
PER-BANK REFRESH to ACTIVATE or PER-BANK REFRESH command delay	t_{RREFD}		–	ns	39
READ to PRECHARGE command delay same bank with bank groups enabled	t_{RTPL}		–	t_{CK}	40
READ to PRECHARGE command delay same bank with bank groups disabled	t_{RTPS}		–	t_{CK}	41
PRECHARGE to PRECHARGE command delay	t_{PPD}		–	ns	
PRECHARGE command period	t_{RP}		–	ns	
WRITE recovery time	t_{WR}		–	ns	
Auto precharge write recovery + precharge time	t_{DAL}	–	–	t_{CK}	42
Column Access Timings					
READ/WRITE bank A to READ/WRITE bank B command delay same bank group	t_{CCDL}		–	t_{CK}	35,43
READ/WRITE bank A to READ/WRITE bank B command delay different bank groups	t_{CCDS}		–	t_{CK}	36,44
LDFF to LDFF command cycle time	t_{LTLTR}	4	–	t_{CK}	
LDFF15 to LDFF command cycle time	t_{LTLFTR}		–	t_{CK}	45,46
LDFF15 to RDTR command delay	t_{LTRTR}		–	t_{CK}	46
READ or RDTR to LDFF command delay	t_{RDTLT}		–	t_{CK}	
WRITE to LDFF command delay	t_{WRTLT}		–	t_{CK}	
WRTR to RDTR command delay	t_{WTRTR}		–	t_{CK}	
WRITE to WRTR command delay	t_{WRWTR}		–	t_{CK}	
Internal WRITE to READ command delay same bank group	t_{WTRL}		–	ns	35
Internal WRITE to READ command delay different bank groups	t_{WTRS}		–	ns	36
READ or RDTR to WRITE or WRTR command delay	t_{RTW}		–	ns	47

Table 54 — AC Timings (cont'd)

PARAMETER 1, 2	SYMBOL	VALUES		UNIT	NOTES
		MIN	MAX		
Power-Down and Refresh Timings					
CKE_n min. high and low pulse width	t_{CKE}		–	t_{CK}	
Valid CK clocks required after self refresh entry	t_{CKSRE}		–	t_{CK}	
Valid CK clocks required before self refresh exit	t_{CKSRX}		–	t_{CK}	
READ to SELF REFRESH ENTRY or POWER-DOWN ENTRY command delay	t_{RDSRE}		–	t_{CK}	48
WRITE to SELF REFRESH ENTRY or POWER-DOWN ENTRY command delay	t_{WRSRE}		–	t_{CK}	49
REFRESH command period	t_{RFC}		–	ns	
PER-BANK REFRESH command period	t_{RFCPB}		–	ns	
Exit self refresh to any command delay	t_{XS}		–	t_{CK}	50
CKE_n low pulse width to exit from hibernate self refresh mode	t_{XHP}	10	–	ns	
Exit hibernate self refresh to self refresh exit command delay	t_{XSH}	500	–	µs	
Refresh period	t_{REF}	–	32	ms	
Average periodic refresh interval with (all-bank) REFRESH command	t_{REFI}	–	1.9	µs	51
Average periodic refresh interval with PER-BANK REFRESH command	t_{REFIPB}	–	t_{REFI} / 16	µs	
REFRESH to REFRESH command period required for impedance calibration updates	t_{ABREF}	1		ms	52
Min. power-down entry to exit time	t_{PD}		9 * t_{REFI}	ns	
NOP/DESELECT commands required upon power-down and self refresh entry	t_{CPDED}	2	–	t_{CK}	
Power-down exit time	t_{XP}		–	t_{CK}	
Miscellaneous Timings					
MODE REGISTER SET command period	t_{MRD}		–	t_{CK}	
PLL/DLL enable to PLL/DLL lock delay	t_{LK}	–		t_{CK}	
PLL/DLL enable to PLL/DLL lock delay with PLL Fast Lock (MR7A1) enabled	t_{FLK}	–		t_{CK}	53
Required time for duty cycle corrector (DCC)	t_{DCC}			t_{CK} or ns	54
REFRESH to calibration update complete delay	t_{KO}	–		ns	
V_{REFC} to V_{REFC2} reference voltage settling time	t_{VREFC2}	–		ns	55
V_{REFD} reference voltage level change settling time	t_{VREFD}	–		ns	56
V_{REFD} to V_{REFD2} reference voltage settling time	t_{VREFD2}	–		ns	57
Active termination setup time	t_{ATS}		–	ns	
Active termination hold time	t_{ATH}		–	ns	
READ to data out delay in address training mode	t_{ADR}	–		t_{CK}	
Address training exit to DQ in ODT state delay	t_{ADZ}	–		ns	
Vendor ID on	t_{WRIDON}		10	ns	
Vendor ID off	$t_{WRIDOFF}$		10	ns	

Table 54 — AC Timings (cont'd)

NOTE 1 All parameters assume proper device initialization.
NOTE 2 Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
NOTE 3 CK_t and CK_c single-ended input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFC} crossing and V_{IXCK}(AC).
NOTE 4 Parameter f_{CKBG3} is required for those devices supporting both 3 * t_{CK} and 4 * t_{CK} settings for bank groups. Devices supporting only 3 * t_{CK} or 4 * t_{CK} need only to specify f_{CKBG}.
NOTE 5 Bank Group Frequency ranges



NOTE 6 Parameter f_{CKPIN} applies when the alignment point in MR7, bit A0 is set to "at pins", the phase difference between the WCK and CK clocks at the DRAM pins is within $t_{WCK2CKSYNC}$ or t_{WCK2CK} for pin mode, and no phase search in WCK2CK training is performed.
NOTE 7 Parameter f_{CKRDQS} applies when RDQS Mode is enabled in MR3, bit A5.
NOTE 8 Parameter $f_{CKVREFC2}$ applies when the ADD/CMD input reference voltage in MR7, bit A6 (Half VREFC) is set to V_{REFC2}.
NOTE 9 Parameter $f_{CKVREFD2}$ applies when the data input reference voltage in MR7, bit A7 (Half VREFD) is set to V_{REFD2}.
NOTE 10 Parameter $f_{CKAUTOSYNC}$ applies when WCK2CK Auto Synchronization is enabled in MR7, bit A4.
NOTE 11 Parameter f_{CKLP1} applies when Low Power Mode LP1 is enabled in MR5, bit A0.
NOTE 12 Parameter f_{CKLF} applies when Low Frequency Mode is enabled in MR7, bit A3.
NOTE 13 By definition the nominal WCK clock cycle time always is 1/2 of the CK clock cycle time (not including jitter).
NOTE 14 WCK_t and WCK_c single-ended input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFD} crossing and V_{IXWCK}(AC).
NOTE 15 The phase relationship between WCK_t/WCK_c and CK_t/CK_c clocks must meet the t_{WCK2CK} specification.
NOTE 16 Command and address input timings are referenced to V_{REFC}.
NOTE 17 Command and address input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFC} crossing and V_{IHA}(AC) or V_{ILA}(AC).
NOTE 18 Command and address input pulse widths are design targets. The values will be characterized but not tested on each device.
NOTE 19 Address input timings are only valid with ABI being enabled and a maximum of 5 address inputs driven Low.
NOTE 20 Parameter may be specified as a combination of t_{CK} and ns.
NOTE 21 Parameters t_{WCKHTR} and t_{WCKLTR} specify the max. allowed WCK clock-to-clock phase shift during WCK2CK training. For READ and WRITE bursts use t_{WCKH} and t_{WCKL}.
NOTE 22 Parameter $t_{WCK2CKPIN}$ defines the WCK2CK phase offset range at the CK and WCK pins for ideal (phase = 0°) clock alignment at the phase detector (when the alignment point in MR7, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR7, bit A0 is set to "at pins"). The minimum and maximum values could be negative or positive numbers, depending on the selected WCK2CK alignment point, PLL-on or PLL-off mode and design implementation.
NOTE 23 Parameter $t_{WCK2CKSYNC}$ defines the max. phase offset from the ideal (phase = 0°) clock alignment at the phase detector (when the alignment point in MR7, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR7, bit A0 is set to "at pins"), where the internal logic synchronizes the CK and WCK clocks; it is expected to be a fraction of t_{WCK2CK}.
NOTE 24 Parameter t_{WCK2CK} defines the max. phase offset from the ideal (phase = 0°) clock alignment at the phase detector (when the alignment point in MR7, bit A0 is set to "at phase detector"), or at the WCK and CK pins (when the alignment point in MR7, bit A0 is set to "at pins"), for stable device operation.
NOTE 25 Parameter $t_{WCK2DQI}$ defines the WCK to DQ/DBI_n time delay range for WRITEs for PLL-on and PLL-off mode. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQI}$ value for reliable WRITE operation.
NOTE 26 Parameter $t_{WCK2DQO}$ defines the WCK to DQ/DBI_n time delay range for READs for PLL-on and PLL-off mode. The minimum and maximum values could be negative or positive numbers, depending on design implementation and PLL-on or PLL-off mode. They also vary across PVT. Data training is required to determine the actual $t_{WCK2DQO}$ value for reliable READ operation.
NOTE 27 Outputs measured with equivalent load (vendor specific) terminated with 60 Ω to V_{DDQ}.
NOTE 28 DQ/DBI_n input timings are valid only with DBI being enabled and a maximum of 4 data inputs per byte driven Low.
NOTE 29 Data input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFD} crossing and $V_{IHD(AC)}$ or $V_{ILD(AC)}$.

Table 54 — AC Timings (cont'd)

NOTE 30 The data input pulse width, t_{DIPW}, defines the minimum positive or negative input pulse width for any one worst-case channel required for proper propagation of an external signal to the receiver. t_{DIPW} is measured at the pins. t_{DIPW} is independent of the PLL/DLL mode. In general t_{DIPW} is larger than t_{DIVW}.

NOTE 31 The data input valid window, t_{DIVW}, defines the time region where input data must be valid for reliable data capture at the receiver for any one worst case channel. It accounts for jitter between data and clock at the latching point introduced in the path between the DRAM pads and the latching point. Any additional jitter introduced into the source signals (e.g., within the system before the DRAM pad) must be accounted for in the final timing budget together with the chosen PLL/DLL mode and bandwidth. t_{DIVW} is measured at the pins. t_{DIVW} is defined for PLL/DLL off and on mode separately. In the case of PLL/DLL on, t_{DIVW} must be specified for each supported bandwidth. In general t_{DIVW} is smaller than t_{DIPW}.

NOTE 32 t_{DQDQI} defines the maximum skew among all DQ/DBI_n inputs of a double byte under worst case conditions. Parameter $t_{WCK2DQI}$ defines the mean value of the earliest and latest DQ/DBI_n pin, t_{DQDQI}(min) the negative offset to $t_{WCK2DQI}$ for the earliest DQ/DBI_n pin and t_{DQDQI}(max) the positive offset to $t_{WCK2DQI}$ for the latest DQ/DBI_n pin.

NOTE 33 t_{DQDQO} defines the maximum skew among all DQ/DBI_n outputs of a double byte under worst case conditions. Parameter $t_{WCK2DQO}$ defines the mean value of the earliest and latest DQ/DBI_n/EDC pin, t_{DQDQO}(min) the negative offset to $t_{WCK2DQO}$ for the earliest DQ/DBI_n/EDC pin and t_{DQDQO}(max) the positive offset to $t_{WCK2DQO}$ for the latest DQ/DBI_n/EDC pin.

NOTE 34 For READs and WRITEs with AUTO PRECHARGE enabled the device will hold off the internal PRECHARGE until t_{RAS}(min) has been satisfied.

NOTE 35 Parameter applies when bank groups are enabled and consecutive commands access the same bank group.

NOTE 36 Parameter applies when bank groups are disabled or consecutive commands access different bank groups.

NOTE 37 Not more than 4 ACTIVATE commands are allowed within period.

NOTE 38 Not more than 32 ACTIVATE commands are allowed within t_{32AW} period. The parameter need not to be specified in case t_{32AW}(min) would not be greater than 8 * t_{FAW}(min).

NOTE 39 Parameter applies between any two PER-BANK REFRESH commands and between a PER-BANK REFRESH command and a subsequent ACTIVATE command to a different bank.

NOTE 40 Parameter applies when bank groups are enabled and READ and PRECHARGE commands access the same bank.

NOTE 41 Parameter applies when bank groups are disabled or READ and PRECHARGE commands access the same bank.

NOTE 42 $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round up to the next integer.

NOTE 43 t_{CCDL} is either for gapless consecutive READ or gapless consecutive WRITE commands.

NOTE 44 t_{CCDS} is either for gapless consecutive READ or RDTR (any combination), gapless consecutive WRITE, or gapless consecutive WRTR commands.

NOTE 45 The min. value is vendor specific and does not exceed 8 t_{CK}.

NOTE 46 In DDR mode this parameter refers to LDFF7 instead of LDFF15.

NOTE 47 t_{RTW} is not a device limit but determined by the system bus turnaround time. The difference between $t_{WCK2DQO}$ and $t_{WCK2DQI}$ shall be considered in the calculation of the bus turnaround time.

NOTE 48 Read data including CRC data must have been clocked out before entering self refresh or power-down mode.

NOTE 49 Write data must have been written to the memory core, and CRC data must have been clocked out before entering self refresh or power-down mode.

NOTE 50 Time for WCK2CK training and data training not included.

NOTE 51 A maximum of 8 consecutive REFRESH commands can be posted to a GDDR5X SGRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is 9 * t_{REFI}.

NOTE 52 t_{ABREF} is relevant only when refresh is normally performed using the PER-BANK REFRESH command. REFRESH commands must be issued at a minimum rate of t_{ABREF} to allow impedance updates from the auto-calibration engine to occur.

NOTE 53 Replaces parameter t_{LK} when PLL Fast Lock has been enabled prior to the PLL/DLL enable or reset.

NOTE 54 The parameter may be specified in t_{CK} or ns (vendor specific).

NOTE 55 The parameter applies when the ADD/CMD reference voltage selection in MR7, bit A6 (Half VREFC) has changed.

NOTE 56 The parameter applies when the V_{REFD} level has been changed in MR6. t_{VREFD} is a constant value for the device, and is referenced from the MRS command to when the 90% level of the delta between old and new V_{REFD} voltage has been reached.

NOTE 57 The parameter applies when the data reference voltage selection in MR7, bit A7 (Half VREFD) has changed.

8.9 CLOCK-TO-DATA TIMING SENSITIVITY

The availability of clock-to-data (WCK2DQ) timing sensitivity information provides the controller the opportunity to anticipate the impact to timings from variations in environmental conditions such as changes in voltage or temperature, allowing the controller to take corrective action if necessary (e.g., realigning WCK and DQ).

Variations in relative timing between WCK and data are reported for READ and WRITE paths. The reported values are characterized but not tested in production.

Table 55 — WCK-to-Data-In Timing Sensitivity

PARAMETER		SYMBOL	VALUES	UNIT	NOTES
WCK2DQI Sensitivity to variations in V_{DDQ}	PLL on	$t_{I2VQSens}$		ps/V	1, 2
	PLL off				
WCK2DQI Sensitivity to variations in V_{DD}	PLL on	$t_{I2VSens}$		ps/V	3, 4
	PLL off				
WCK2DQI Sensitivity to variations in T_{case}	PLL on	$t_{I2TSens}$		ps/°C	5, 6
	PLL off				

NOTE 1 $tI2VQSens = ((t_{WCK2DQI}(V_{DDQ}(max)) - t_{WCK2DQI}(V_{DDQ}(min))) / (V_{DDQ}(max) - V_{DDQ}(min)))$.
NOTE 2 $V_{DD}(typ)$, T_{case} = 85 °C, worst-case process corner.
NOTE 3 $tI2VSens = ((t_{WCK2DQI}(V_{DD}(max)) - t_{WCK2DQI}(V_{DD}(min))) / (V_{DD}(max) - V_{DD}(min)))$.
NOTE 4 $V_{DDQ}(typ)$, T_{case} = 85 °C, worst-case process corner.
NOTE 5 $tI2TSens = ((t_{WCK2DQI}(T_{case}(max)) - t_{WCK2DQI}(T_{case}(min))) / (T_{case}(max) - T_{case}(min)))$.
NOTE 6 $V_{DDQ}(typ)$, $V_{DD}(typ)$, worst-case process corner.

Table 56 — WCK-to-Data-Out Timing Sensitivity

PARAMETER		SYMBOL	VALUES	UNIT	NOTES
WCK2DQO Sensitivity to variations in V_{DDQ}	PLL on	$t_{O2VQSens}$		ps/V	1, 2
	PLL off				
WCK2DQO Sensitivity to variations in V_{DD}	PLL on	$t_{O2VSens}$		ps/V	3, 4
	PLL off				
WCK2DQO Sensitivity to variations in T_{case}	PLL on	$t_{O2TSens}$		ps/°C	5, 6
	PLL off				

NOTE 1 $tO2VQSens = ((t_{WCK2DQO}(V_{DDQ}(max)) - t_{WCK2DQO}(V_{DDQ}(min))) / (V_{DDQ}(max) - V_{DDQ}(min)))$.
NOTE 2 $V_{DD}(typ)$, T_{case} = 85 °C, worst-case process corner.
NOTE 3 $tO2VSens = ((t_{WCK2DQO}(V_{DD}(max)) - t_{WCK2DQO}(V_{DD}(min))) / (V_{DD}(max) - V_{DD}(min)))$.
NOTE 4 $V_{DDQ}(typ)$, T_{case} = 85 °C, worst-case process corner.
NOTE 5 $tO2TSens = ((t_{WCK2DQO}(T_{case}(max)) - t_{WCK2DQO}(T_{case}(min))) / (T_{case}(max) - T_{case}(min)))$.
NOTE 6 $V_{DDQ}(typ)$, $V_{DD}(typ)$, worst-case process corner.

8.10 POD I/O SYSTEM

The POD I/O system is optimized for small systems with very high data rates. The system allows a single Initiator device to control one Target in the case of GDDR5X. The POD driver uses a 40/60 Ω output impedance that drives into a 60 Ω equivalent terminator tied to V_{DDQ} as shown in Figure 108.

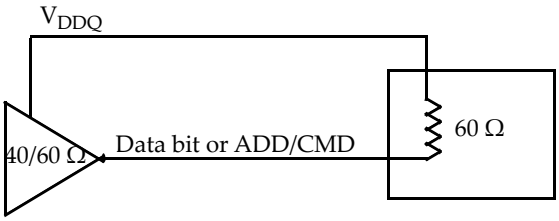


Figure 107 — System Configuration

The POD I/O cell is comprised of a 40/60 Ω driver and a programmable terminator of 60 or 120 Ω for address/command inputs and 60, 80 or 120 Ω for data inputs. The POD cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 108.

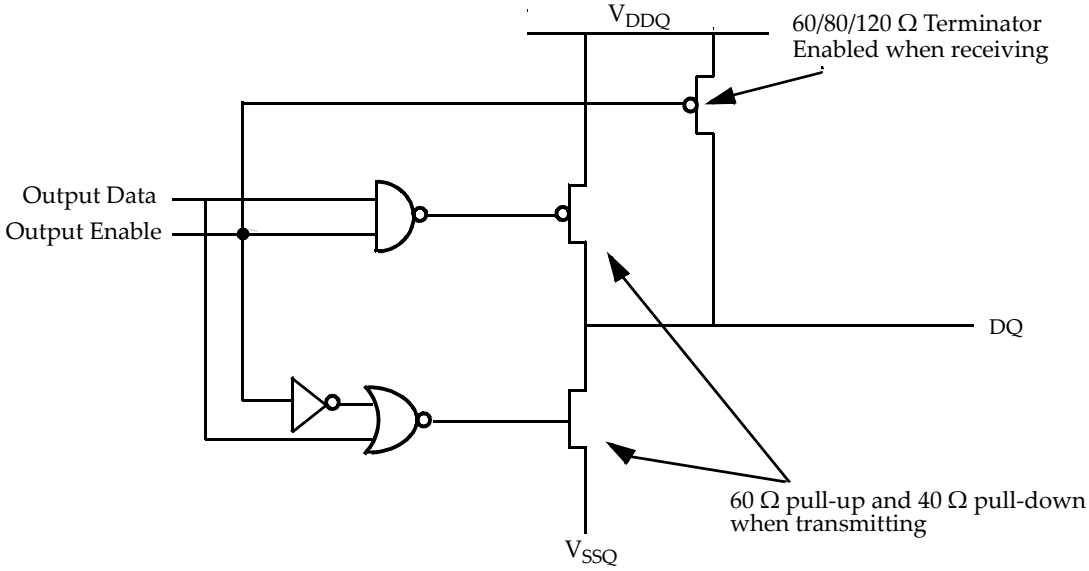


Figure 108 — POD I/O Cell

The POD I/O cell is intended to have its driver and terminators combined together to minimize the area needed to implement the cell and reduce pad capacitance. To ensure that the target impedance is achieved the POD I/O cell is designed to be calibrated to an external 1% precision resistor.

The following procedure may be used to calibrate the cell:

1) Calibrate the PMOS device against a 120 Ω resistor to V_{SS} via the ZQ pin as illustrated in Figure 109.

- Set Strength Control to minimum setting
- Increase drive strength until the comparator detects data bit is greater than $V_{DDQ}/2$
- The PMOS device is calibrated to 120 Ω

2) Calibrate the NMOS device against the calibrated 120 Ω PMOS device as illustrated in Figure 110.

- Set Strength Control to minimum setting
- Increase drive strength until the comparator detects data bit is less than $V_{DDQ}/2$
- The NMOS device is now calibrated to 120 Ω

8.10 POD I/O SYSTEM (cont'd)

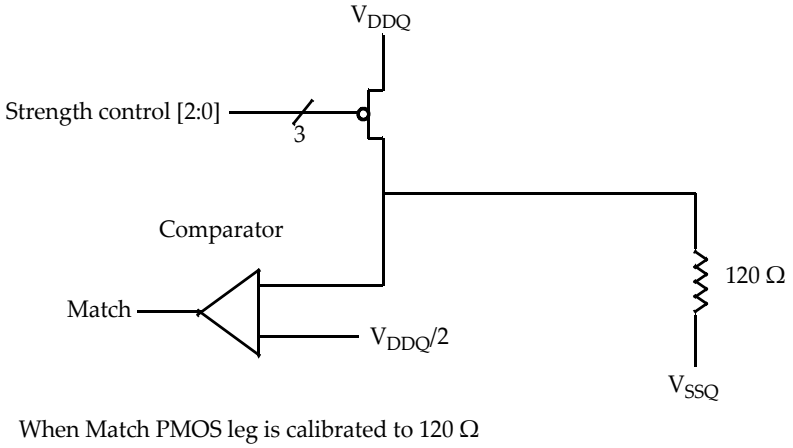


Figure 109 — PMOS Calibration

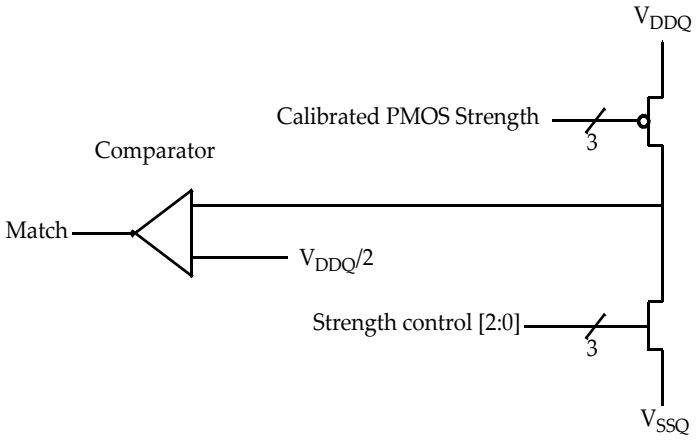


Figure 110 — NMOS Calibration

The driver and termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal V_{DD}/V_{DDQ}
2. Power the device and calibrate the output drivers and termination at 25 °C to eliminate process variation.
3. Reduce the temperature to 10 °C and recalibrate.
4. Reduce the temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate.
6. Raise temperature to 85 °C and take the slow corner measurement.
7. Reiterate steps 2 to 6 with V_{DD}/V_{DDQ} of 1.3095 V.
8. Reiterate steps 2 to 6 with V_{DD}/V_{DDQ} of 1.3905 V.
9. All obtained driver and termination IV characteristics have to be bounded by the specified MIN and MAX I/V characteristics

8.10 POD I/O SYSTEM (cont'd)

The following values (ideal with +/- 10% MIN/MAX) are targets for the designer and are not required to be met. Vendor datasheets should be consulted for further details. It is expected that the characteristics of the real curves will have some nonlinearity as shown in Figure 113 and Figure 114. This may help to reduce the overall capacitance and boost performance. It is up to the designer to find the optimum combination of linearity and capacitance for best Rx and Tx performance.

Table 57 — 1.35 V I/O Impedances

PULL-DOWN CHARACTERISTIC AT 40 Ω			
Voltage (V)	**MIN(mA)**	**Ideal(mA)**	**MAX(mA)**
0.1	2.25	2.50	2.75
0.2	4.50	5.00	5.50
0.3	6.75	7.50	8.25
0.4	9.00	10.00	11.00
0.5	11.25	12.50	13.75
0.6	13.50	15.00	16.50
0.7	15.75	17.50	19.25
0.8	18.00	20.00	22.00
0.9	20.25	22.50	24.75
1.0	22.50	25.00	27.50
1.1	24.75	27.50	30.25
1.2	27.00	30.00	33.00
1.3	29.25	32.50	35.75
1.35	30.375	33.75	37.125

PULL-UP / TERMINATION CHARACTERISTIC AT 60 Ω			
Voltage (V)	**MIN(mA)**	**Ideal(mA)**	**MAX(mA)**
0.1	-1.50	-1.67	-1.83
0.2	-3.00	-3.33	-3.67
0.3	-4.50	-5.00	-5.50
0.4	-6.00	-6.67	-7.33
0.5	-7.50	-8.33	-9.17
0.6	-9.00	-10.00	-11.00
0.7	-10.50	-11.67	-12.83
0.8	-12.00	-13.33	-14.67
0.9	-13.50	-15.00	-16.50
1.0	-15.00	-16.67	-18.33
1.1	-16.50	-18.33	-20.17
1.2	-18.00	-20.00	-22.00
1.3	-19.50	-21.67	-23.83
1.35	-20.25	-22.50	-24.75

8.10 POD I/O SYSTEM (cont'd)

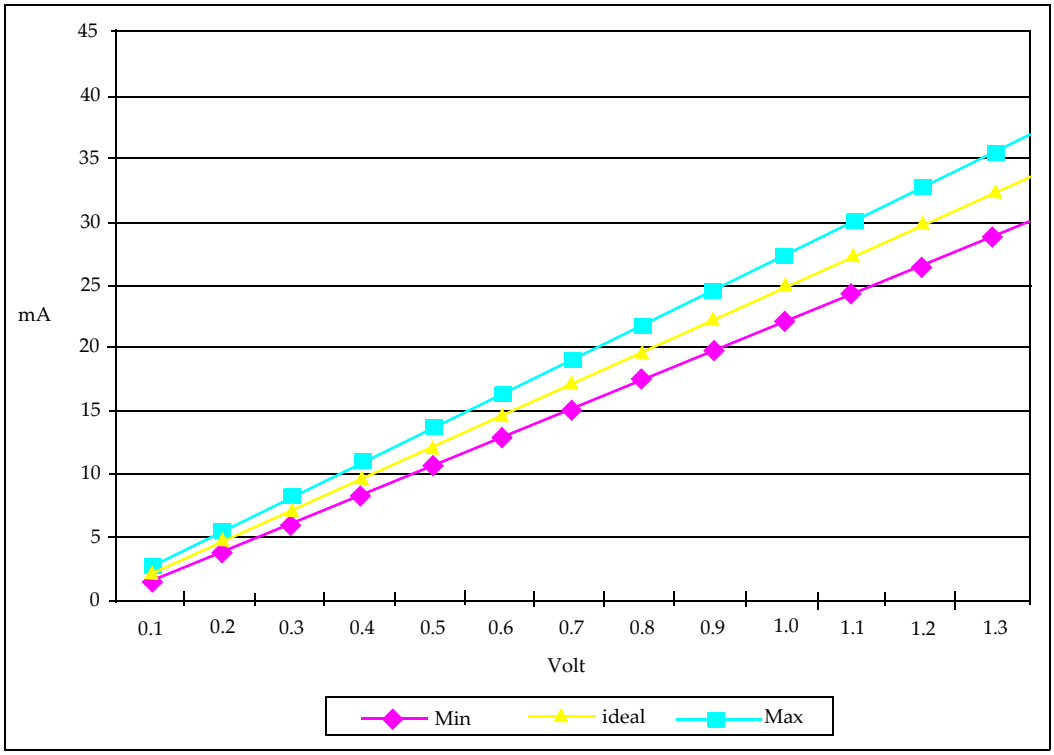


Figure 111 — Target Pull-Down Characteristic at 40 Ω

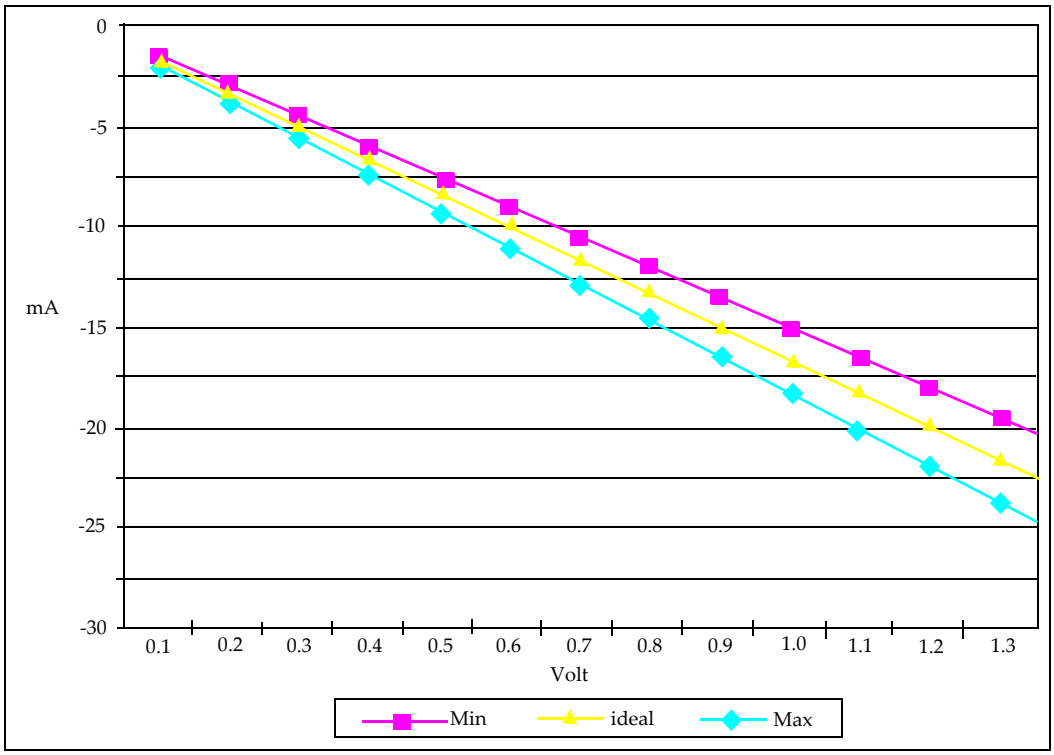


Figure 112 — Target Pull-Up/Termination Characteristic at 60 Ω

8.10 POD I/O SYSTEM (cont'd)

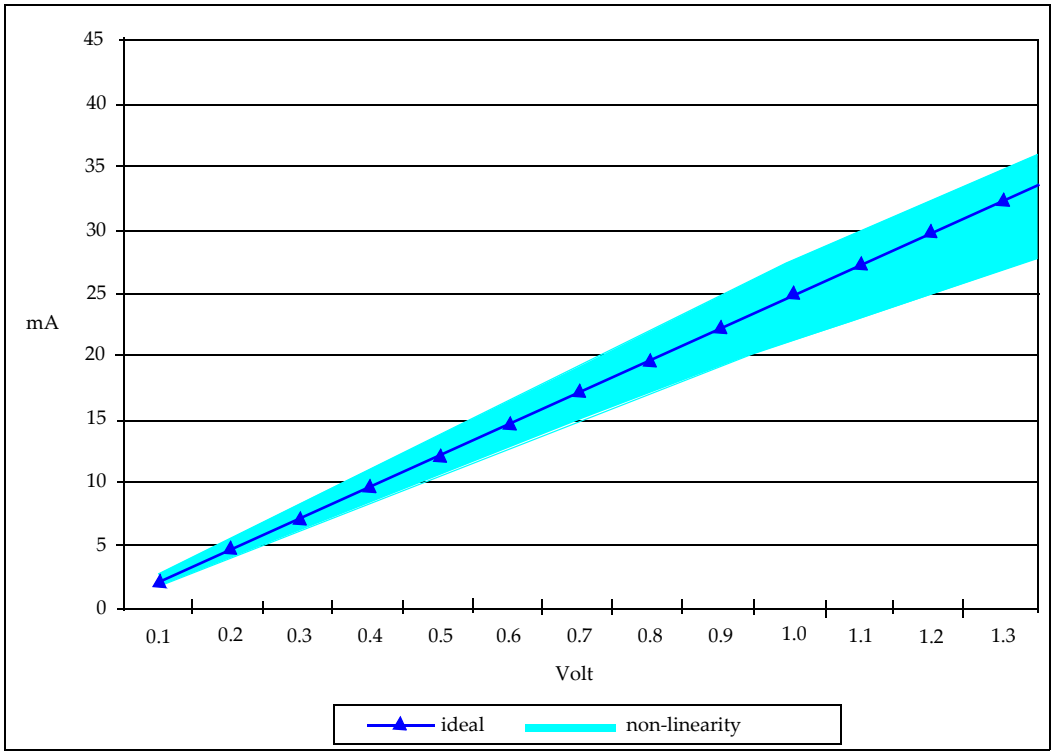


Figure 113 — Example of Non Linearity, Pull-Down Characteristic at 40 Ω

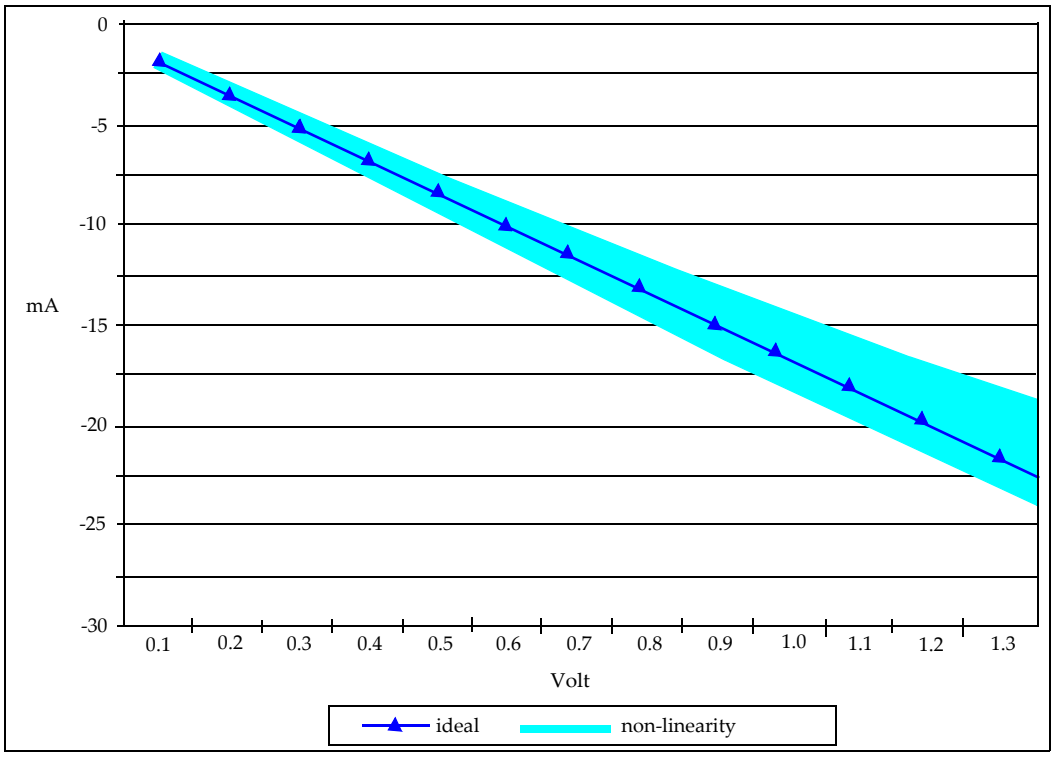


Figure 114 — Example of Non Linearity, Pull-Up/Termination Characteristic at 60 Ω

9 PIN DEFINITION and BALLOUT

9.1 SIGNAL DESCRIPTION

Table 58 — Signal Description

SYMBOL	TYPE	DESCRIPTION
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. Command inputs are latched on the rising edge of CK_t. Address inputs are latched on the rising edge of CK_t and the rising edge of CK_c. All latencies are referenced to CK_t.
WCK01_t, WCK01_c, WCK23_t, WCK23_c	Input	Write Clocks: WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output. WCK01_t/WCK01_c is associated with DQ0-DQ15, DBI0_n, DBI1_n, EDC0 and EDC1. WCK23_t/WCK23_c is associated with DQ16-DQ31, DBI2_n, DBI3_n, EDC2 and EDC3.
CKE_n	Input	Clock Enable: CKE_n Low activates and CKE_n High deactivates the internal clock, device input buffers, and output drivers. Taking CKE_n High provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE_n must be maintained Low throughout read and write accesses.
RAS_n, CAS_n, WE_n	Input	Command Inputs: RAS_n, CAS_n, and WE_n define the command being entered.
BA0–BA3	Input	Bank Address Inputs: BA0-BA3 define to which bank an ACTIVATE, READ, WRITE, PRECHARGE or PER-BANK REFRESH command is being applied. BA0-BA3 also determine which Mode Register is accessed with a MODE REGISTER SET command. BA0-BA3 are sampled with the rising edge of CK_t.
A0–A15	Input	Address Inputs: A0-A12 (A13, A14, A15) provide the row address for ACTIVATE commands. A0-A5 provide the lower column address (CAL) and A7,A9,A12-A15 the upper column address (CAU) in QDR operating mode; A0-A6 provide the lower column address (CAL) and A6-A7, A9, A12-A15 the upper column address (CAU) in DDR operating mode. A8 defines the auto precharge function for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 Low, bank selected by BA0-BA3) or all banks (A8 High). The address inputs also provide the op-code during a MODE REGISTER SET command and the data bits during a LDFF command. A8-A12,A14 are sampled with the rising edge of CK_t and A0-A7,A13,A15 are sampled with the rising edge of CK_c. CAL is associated with DQ0-DQ15 and CAU is associated with DQ16-DQ31.
ABI_n	Input	Address Bus Inversion
DQ0–DQ31	I/O	Data Input/Output: 32-bit data bus
DBI0_n–DBI3_n	I/O	Data Bus Inversion. DBI0_n is associated with DQ0-DQ7, DBI1_n is associated with DQ8-DQ15, DBI2_n is associated with DQ16-DQ23, DBI3_n is associated with DQ24-DQ31.
EDC0–EDC3	Output	Error Detection Code. The calculated CRC data is transmitted on these pins. In addition these pins drive a 'hold' pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ0-DQ7, EDC1 is associated with DQ8-DQ15, EDC2 is associated with DQ16-DQ23, EDC3 is associated with DQ24-DQ31.
V_{DDQ}	Supply	I/O Power Supply
V_{SSQ}	Supply	I/O Ground
V_{DD}	Supply	Power Supply
V_{SS}	Supply	Ground
V_{REFC}	Supply	Reference Voltage for address and command pins
V_{PP}	Supply	Pump Voltage
MF	Input	Mirror Function. Must be tied to power or ground.
ZQ	Supply	Reference Pin for ZQ calibration
TDI	Input	JTAG test data input
TDO	Output	JTAG test data output
TMS	Input	JTAG test mode select
TCK	Input	JTAG test clock
RESET_n	Input	Reset Pin. RESET_n Low asynchronously initiates a full chip reset. With RESET_n Low all ODTs are disabled. A full chip reset may be performed at any time by pulling RESET_n Low.

9.2 CLAMSHELL (x16) MODE

A GDDR5X SGRAM based memory system is typically divided into several channels each being 32 bit wide. A channel can be comprised of a single GDDR5X SGRAM operated in x32 mode, or optionally two GDDR5X SGRAMs each operated in x16 (clamshell) mode and typically assembled on opposite sides of the PCB. Clamshell mode is an elegant method to double the channel's memory density.

In x32 mode all high speed data pins (DQ, DBI_n, EDC) and WCK clocks shall be routed point-to-point (P2P). In x16 mode, all high speed data pins (DQ, DBI_n, EDC) and WCK clocks are recommended to be routed P2P. WCK is allowed to be routed point-to-two-point (P22P) for x16 mode but may limit achievable frequencies. The address and command pins and CK clock shall be routed P2P when the device is operated in x32 mode, and P22P when the devices are operated in x16 mode as shown in Figure 115. Please note that in x16 mode one device must be configured to MF=0 (non-mirrored) and the other device to MF=1 (mirrored). In x32 mode the device can be configured to MF=0 or MF=1 depending on PCB routing preferences.

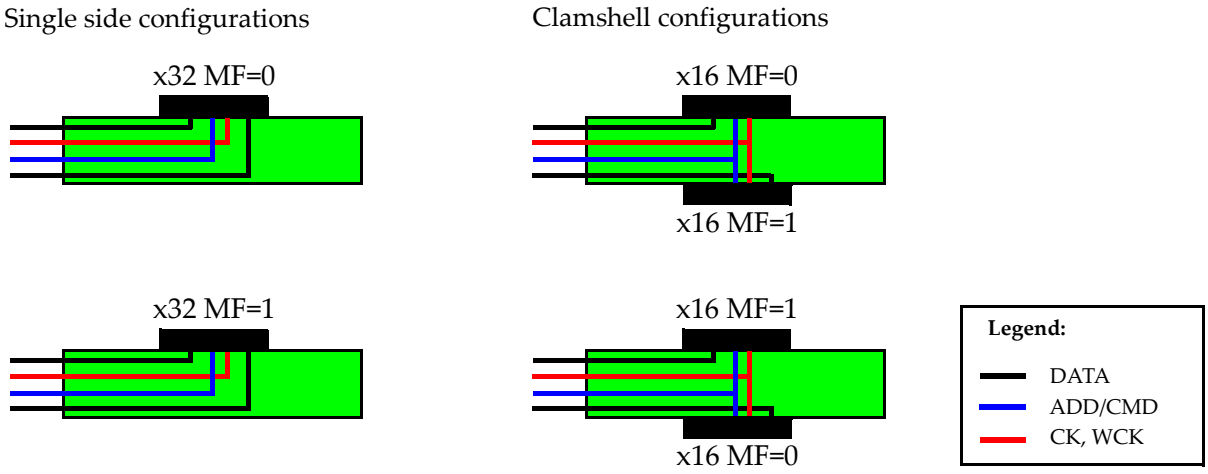


Figure 115 — Example GDDR5X PCB Layout Topologies

GDDR5X SGRAMs supporting the optional x16 mode are configured to either x32 mode or x16 mode at power-up with RESET_n going High. The mode is selected on the pin at location D-12 which is EDC1 when configured to MF=0 and EDC2 when configured to MF=1. For x16 mode this pin is tied to V_{SSQ}; the pin is part of the two bytes that are disabled in this mode and therefore not needed for EDC functionality. For x32 mode this pin is active and terminated to V_{DDQ} in the system or by the controller. The disabled pins in x16 mode are all in a High-Z state, non-terminating.

GDDR5X SGRAMs not supporting the optional x16 mode are pre-configured to x32 mode.

The ADD/CMD and CK pin ODT is enabled with a value as determined by the level of the CKE_n pin at RESET_n going HIGH.

Table 59 — MF, x32/x16 Mode and Default ADD/CMD/CK ODT

MODE	MF	EDC1 (MF=0) or EDC2 (MF=1)	Default ADD/CMD ODT
x16 non-mirrored	V_{SSQ}	V_{SSQ}	ZQ = 120 Ω
x32 non-mirrored	V_{SSQ}	V_{DDQ} (terminated by the system or controller)	ZQ/2 = 60 Ω
x16 mirrored	V_{DDQ}	V_{SSQ}	ZQ = 120 Ω
x32 mirrored	V_{DDQ}	V_{DDQ} (terminated by the system or controller)	ZQ/2 = 60 Ω

9.2 CLAMSHELL (x16) MODE (cont'd)

Usually, the configuration is fixed in the system. Once the configuration has been set, it cannot be changed during normal operation. Details of the x32/x16 mode selection are depicted in Figure 117. A comparison of x32 mode and x16 mode systems is shown in Figure 116.

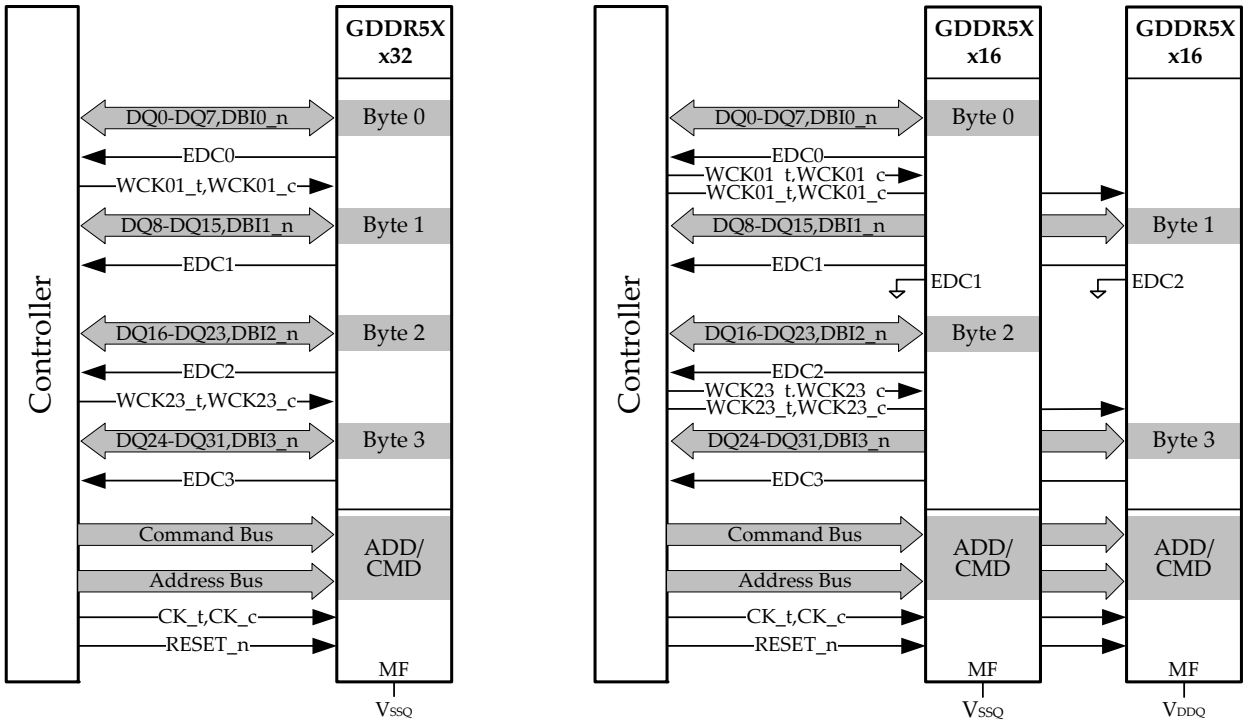


Figure 116 — System View for x32 Mode vs. x16 Mode

9.2 CLAMSHELL (x16) MODE (cont'd)

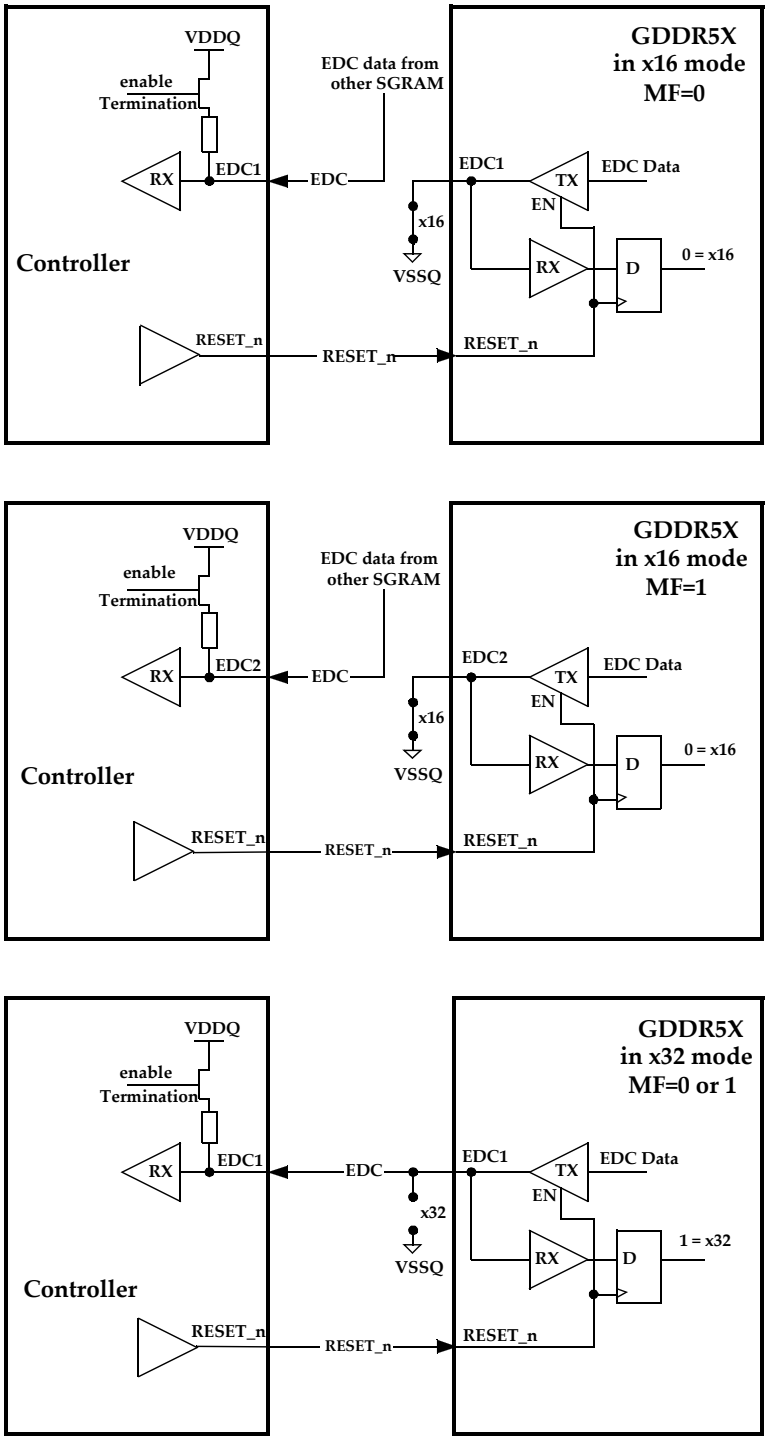


Figure 117 — Enabling x32 or x16 Mode

9.3 MIRROR FUNCTION (MF) ENABLE

A mirror function (MF) mode is provided to change the physical location of the data, command and address pins assisting in PCB signal routing. The MF pin should be tied directly to V_{SSQ} or V_{DDQ} depending on the desired ballout.

It is pointed out that this mirror function mode swaps the location of the data bytes (Byte 0 .. Byte 3). The controller must strictly adhere to this data byte order because this byte order is assumed in the internal assignment of the write data mask received with WDM and WSM commands.

Table 60 — ADD/CMD Signals Affected by Mirror Function Mode (MF)

	SIGNAL			SIGNAL			SIGNAL	
Ball	MF=0	MF=1	Ball	MF=0	MF=1	Ball	MF=0	MF=1
H-4	RAS_n	CAS_n	J-10	BA3 A3	BA1 A5	L-10	BA1 A5	BA3 A3
H-11	CKE_n	WE_n	J-11	BA0 A2	BA2 A4	L-11	BA2 A4	BA0 A2
J-4	A10 A0	A8 A7	L-4	A8 A7	A10 A0	M-4	CAS_n	RAS_n
J-5	A9 A1	A11 A6	L-5	A11 A6	A9 A1	M-11	WE_n	CKE_n

9.4 BALLOUT

Table 61 — GDDR5X SGRAM 190-ball BGA Ballout MF=0

1	2	3	4	5	6	7	8	9	10	11	12	13	14
		BYTE 0									**BYTE 1**		
V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}		A			V_{SS}	V_{DD}	TDO	V_{DDQ}	V_{DD}
V_{SS}	V_{SSQ}	DQ1	DQ0	V_{DDQ}		B			V_{DDQ}	DQ8	DQ9	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DQ3	DQ2	V_{SSQ}		C			V_{SSQ}	DQ10	DQ11	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	EDC0	WCK01_t	WCK01_c		D			V_{DD}	V_{SS}	EDC1	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DBI0_n	V_{DDQ}	V_{SSQ}		E			V_{SSQ}	V_{DDQ}	DBI1_n	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	DQ5	DQ4	V_{DDQ}		F			V_{DDQ}	DQ12	DQ13	V_{SSQ}	V_{SS}
V_{DD}	V_{DDQ}	DQ7	DQ6	V_{SSQ}		G			V_{SSQ}	DQ14	DQ15	V_{DDQ}	V_{DD}
V_{SS}	TMS	V_{DDQ}	RAS_n	V_{DD}		H			V_{DD}	CKE_n	V_{DDQ}	ZQ	V_{SS}
V_{DD}	V_{DDQ}	V_{SS}	A10 A0	A9 A1		J			BA3 A3	BA0 A2	V_{SS}	V_{DDQ}	V_{DD}
V_{SS}	RESET_n	V_{SS}	ABI_n	A12 A13		K			CK_c	CK_t	A14 A15	VREFC	V_{SS}
V_{DD}	V_{DDQ}	V_{SS}	A8 A7	A11 A6		L			BA1 A5	BA2 A4	V_{SS}	V_{DDQ}	V_{DD}
V_{SS}	TCK	V_{DDQ}	CAS_n	V_{DD}		M			V_{DD}	WE_n	V_{DDQ}	TDI	V_{SS}
V_{DD}	V_{DDQ}	DQ31	DQ30	V_{SSQ}		N			V_{SSQ}	DQ22	DQ23	V_{DDQ}	V_{DD}
V_{SS}	V_{SSQ}	DQ29	DQ28	V_{DDQ}		P			V_{DDQ}	DQ20	DQ21	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DBI3_n	V_{DDQ}	V_{SSQ}		R			V_{SSQ}	V_{DDQ}	DBI2_n	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	EDC3	WCK23_t	WCK23_c		T			V_{DD}	V_{SS}	EDC2	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DQ27	DQ26	V_{SSQ}		U			V_{SSQ}	DQ18	DQ19	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	DQ25	DQ24	V_{DDQ}		V			V_{DDQ}	DQ16	DQ17	V_{SSQ}	V_{SS}
V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}		W			V_{SS}	V_{DD}	MF	V_{DDQ}	V_{DD}
		BYTE 3									**BYTE 2**		

NOTE 1 Top View (as seen thru package).
NOTE 2 Bytes 1 and 3 are disabled when the device is configured to x16 mode, non-mirrored (MF=0).

9.4 BALLOUT (cont'd)

Table 62 — GDDR5X SGRAM 190-ball BGA Ballout MF=1

1	2	3	4	5	6	7	8	9	10	11	12	13	14
		BYTE 3									**BYTE 2**		
V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}		A			V_{SS}	V_{DD}	TDO	V_{DDQ}	V_{DD}
V_{SS}	V_{SSQ}	DQ25	DQ24	V_{DDQ}		B			V_{DDQ}	DQ16	DQ17	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DQ27	DQ26	V_{SSQ}		C			V_{SSQ}	DQ18	DQ19	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	EDC3	WCK23_t	WCK23_c		D			V_{DD}	V_{SS}	EDC2	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DBI3_n	V_{DDQ}	V_{SSQ}		E			V_{SSQ}	V_{DDQ}	DBI2_n	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	DQ29	DQ28	V_{DDQ}		F			V_{DDQ}	DQ20	DQ21	V_{SSQ}	V_{SS}
V_{DD}	V_{DDQ}	DQ31	DQ30	V_{SSQ}		G			V_{SSQ}	DQ22	DQ23	V_{DDQ}	V_{DD}
V_{SS}	TMS	V_{DDQ}	CAS_n	V_{DD}		H			V_{DD}	WE_n	V_{DDQ}	ZQ	V_{SS}
V_{DD}	V_{DDQ}	V_{SS}	A8 A7	A11 A6		J			BA1 A5	BA2 A4	V_{SS}	V_{DDQ}	V_{DD}
V_{SS}	RESET_n	V_{SS}	ABI_n	A12 A13		K			CK_c	CK_t	A14 A15	VREFC	V_{SS}
V_{DD}	V_{DDQ}	V_{SS}	A10 A0	A9 A1		L			BA3 A3	BA0 A2	V_{SS}	V_{DDQ}	V_{DD}
V_{SS}	TCK	V_{DDQ}	RAS_n	V_{DD}		M			V_{DD}	CKE_n	V_{DDQ}	TDI	V_{SS}
V_{DD}	V_{DDQ}	DQ7	DQ6	V_{SSQ}		N			V_{SSQ}	DQ14	DQ15	V_{DDQ}	V_{DD}
V_{SS}	V_{SSQ}	DQ5	DQ4	V_{DDQ}		P			V_{DDQ}	DQ12	DQ13	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DBI0_n	V_{DDQ}	V_{SSQ}		R			V_{SSQ}	V_{DDQ}	DBI1_n	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	EDC0	WCK01_t	WCK01_c		T			V_{DD}	V_{SS}	EDC1	V_{SSQ}	V_{SS}
V_{DDQ}	V_{DDQ}	DQ3	DQ2	V_{SSQ}		U			V_{SSQ}	DQ10	DQ11	V_{DDQ}	V_{DDQ}
V_{SS}	V_{SSQ}	DQ1	DQ0	V_{DDQ}		V			V_{DDQ}	DQ8	DQ9	V_{SSQ}	V_{SS}
V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}		W			V_{SS}	V_{DD}	MF	V_{DDQ}	V_{DD}
		BYTE 0									**BYTE 1**		

NOTE 1 Top View (as seen thru package).
NOTE 2 Bytes 0 and 2 are disabled when the device is configured to x16 mode, mirrored (MF=1).

10 PACKAGE OUTLINE

Table 63 — Package Dimensions

Parameter	Symbol	Minimum	Nominal	Variation
Length	D		14.00	+/- 0.100
Width	E		10.00	+/- 0.100
Height	A		1.10	+/- 0.100
Ball diameter	b		0.40	+/- 0.050
Standoff	A1	0.21		
Ball pitch	e		0.65	

NOTE 1 GDDR5X package dimension specification is compliant to MO-246 Rev. G, variation T14.0x10.0-HK-190G.
NOTE 2 All dimensions in mm unless otherwise noted.

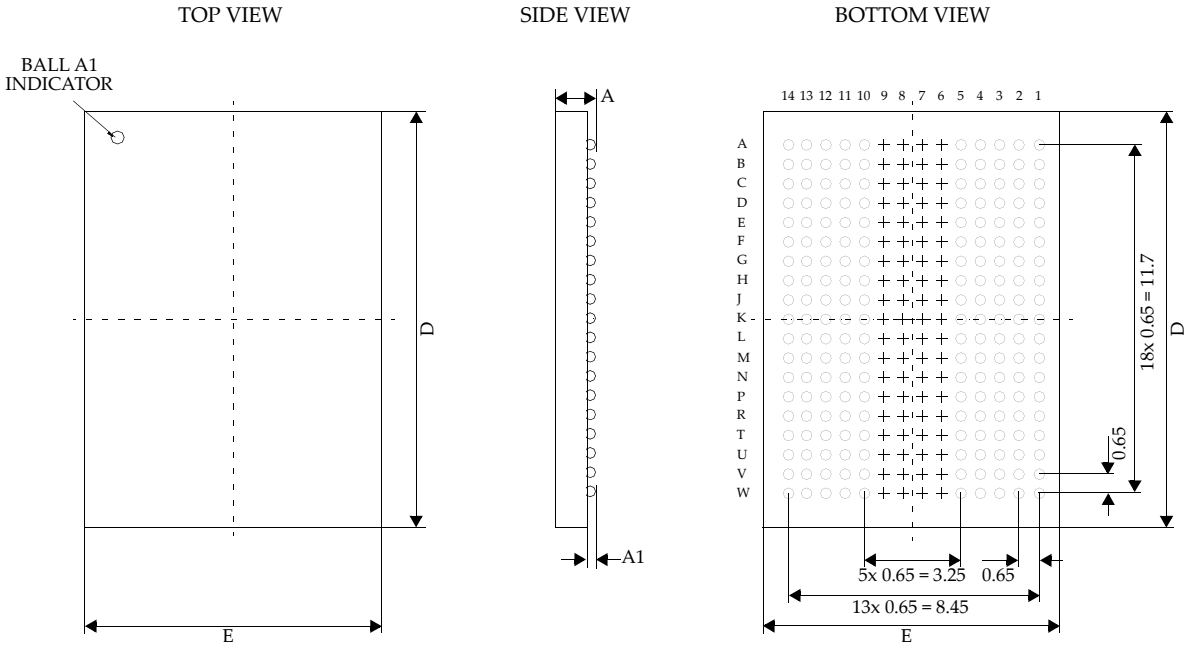


Figure 118 — Package Dimensions (for Reference Only)

11 BOUNDARY SCAN

The GDDR5X SGRAM incorporates a boundary scan standard test access port that operates in accordance with IEEE Standard 1149.1-2013. It allows monitoring and control of the device's external I/O pins through a dedicated test port, and is controlled by an integrated test access port (TAP) controller.

DRAM vendors may in addition use this test access port to gain access to proprietary test modes built into the device; this access will be provided through vendor defined instructions as outlined in clause 11.4.

11.1 TEST PINS

Four dedicated pins are associated with the boundary scan test access port.

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

Commands to the TAP controller are received through the test mode select input. An internal pull-up resistor ensures that an undriven input is latched as a logic 1.

Test Data Input (TDI)

The pin is used to serially load test instructions and data into the registers and can be connected to the input of any register. The register between TDI and TDO is selected by the instruction that is loaded into the TAP instruction register. An internal pull-up resistor ensures that an undriven input is latched as a logic 1. TDI is connected to the most significant bit (MSB) of any register.

Test Data Output (TDO)

The pin is used to clock test instructions and data serially out of the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states (see Figure 119) and is High-Z in all other states. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

11.2 TAP CONTROLLER

The TAP controller is a finite state machine that uses the logic level of the TMS pin at the rising edge of TCK to navigate through its various operating modes as illustrated in Figure 119. The states are described subsequently. Actions of the test logic (e.g., data capture, shift or register updates) occur on the next falling or rising TCK edge in each state.

Test-Logic-Reset

The Test-Logic-Reset state is entered when TMS is held High for at least five consecutive rising edges of TCK. As long as TMS remains High, the TAP controller remains in the test-logic-reset state, and the test logic is inactive during this state. The test-logic-reset state is also asychronously entered upon device initialization to prevent any false interaction with the functional I/O of the device when boundary scan mode operation is not desired.

Run-Test/Idle

Run-Test/Idle is a controller state in between scan operations. The state can be maintained by holding TMS Low. From here, either the data register scan, or subsequently, the instruction register scan can be selected.

Select-DR-Scan

This is a temporary controller state. All test data registers retain their state while here.

11.2 TAP CONTROLLER (cont'd)

Capture-DR

This state is where data is parallel-loaded into the test data registers.

Shift-DR

Data is shifted serially through the data register while in this state. As new data is input through the TDI pin, data is shifted out of the TDO pin.

Exit1-DR, Pause-DR, and Exit2-DR

The purpose of Exit1-DR is to provide a path for return to the Run-Test/Idle state (through the Update-DR state). The Pause-DR state is entered when there is a need to suspend data shifting through the test registers. When shifting is to reconvene, the controller enters the Exit2-DR state and can then re-enter the Shift-DR state.

Update-DR

Data is parallel loaded from the shift register to the parallel output register on the falling edge of TCK in this controller state.

Instruction Register States

The instruction register states of the TAP controller are similar to the data register states. The desired instruction is shifted serially into the instruction register during the Shift-IR state and is loaded during the Update-IR state.

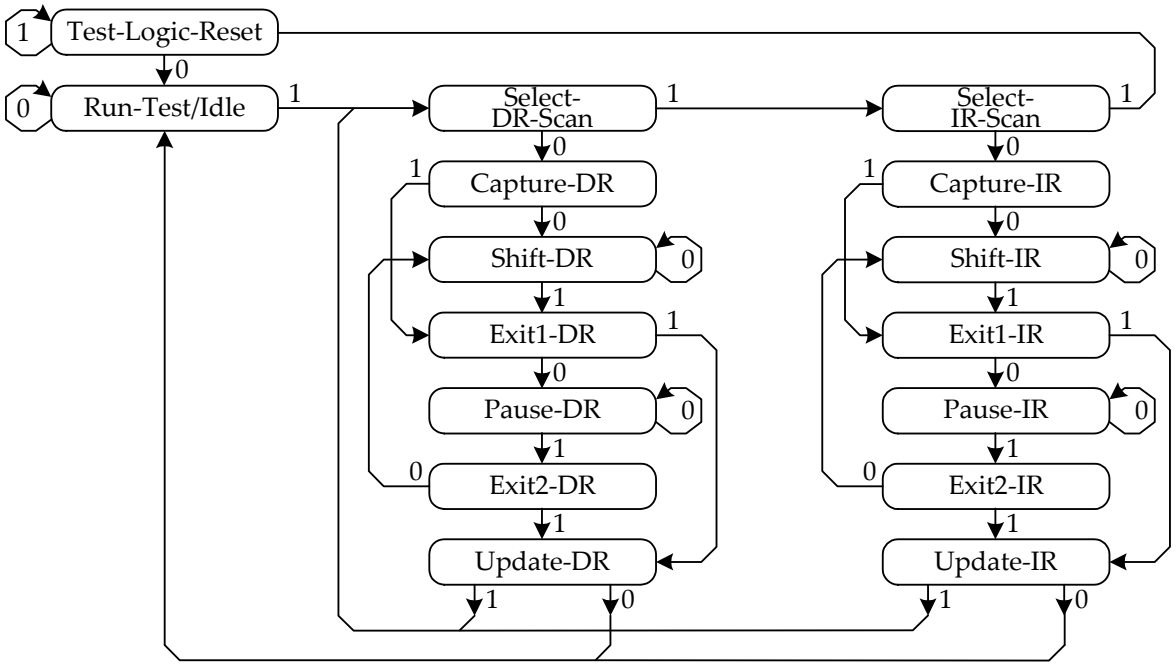


Figure 119 — TAP Controller

11.3 TAP REGISTERS

Several registers are provided to serially load and scan out instructions and data through the TDI and TDO pins. Only a single register can be selected at a time; the selection is determined by the active instruction and the TAP controller state.

Instruction (IR) Register

Eight-bit instructions (see Table 65) can be loaded serially into the instruction register. This register is loaded during the Update-IR state of the TAP controller. The instruction register is loaded with the IDCODE instruction upon power-up or when the TAP controller is in the Test-Logic-Reset state. When the TAP controller is in the Capture-IR state, the register is loaded with a hexadecimal 0x01 pattern to accommodate fault isolation of the board-level serial test data path.

Bypass (BY) Register

The BY register is a single-bit register that can be placed between the TDI and TDO pins. This enables data shifting through the device with minimal delay. The BY register is loaded with 0 in the Capture-DR controller state when the BYPASS, CLAMP or HIGH-Z instruction is executed.

Identification (ID) Register

The ID register contains a vendor specific 32-bit hardwired device identification code as shown in Figure 120. The register is loaded during the Capture-DR state when the IDCODE command is loaded in the instruction register. The register is shifted out in the Shift-DR controller state. The manufacturer identity field shall be programmed according to the latest revision of JEP106.

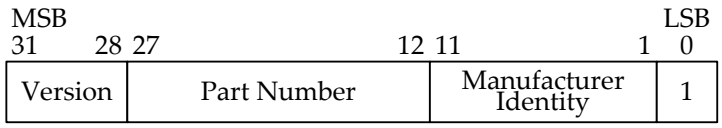


Figure 120 — Identification Register

Boundary Scan (BS) Register

The BS register is the primary test register that monitors and controls the data flow through the functional I/O of the device. The register is parallel-loaded with the contents of the I/O when the TAP controller is in the Capture-DR state. It is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state; in that state new test data are serially shifted in from the TDI pin while the captured pin state are shifted out on the TDO pin at the same time.

Different types of boundary scan cells are associated with each device pin. Example implementations of boundary scan cells are shown in Figure 121.

Each input pin is equipped with an observe-only cell for input data capture. Differential clocks (CK, WCK) are equipped with an observe-only input cell on both their true and complement inputs. VREFC and ZQ pins are as well equipped with an observe-only cell; their scan result may be masked (ignored) if, e.g., internal VREFC is used.

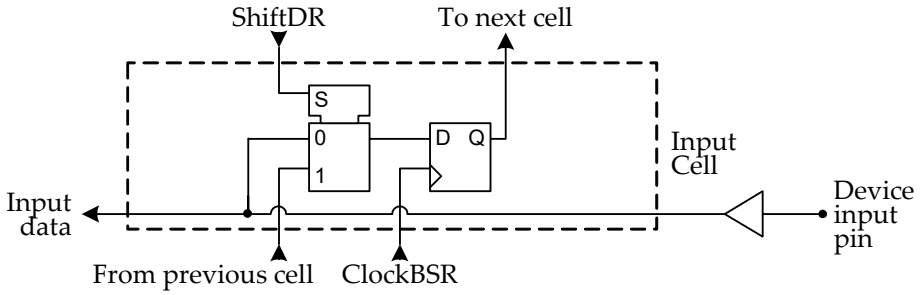
Each DQ pin is equipped with one combined input and output boundary scan cell. The cell performs the same function for input data capture as provided for the input pins, and also holds the output data. An additional boundary scan cell per byte controls the output enable of the 8 DQs of that byte.

Each DBI_n pin is equipped with two boundary scan cells. The first cell is the same combined input and output boundary scan cell for input data capture and output data as for a DQ pin. The second cell controls the output enable.

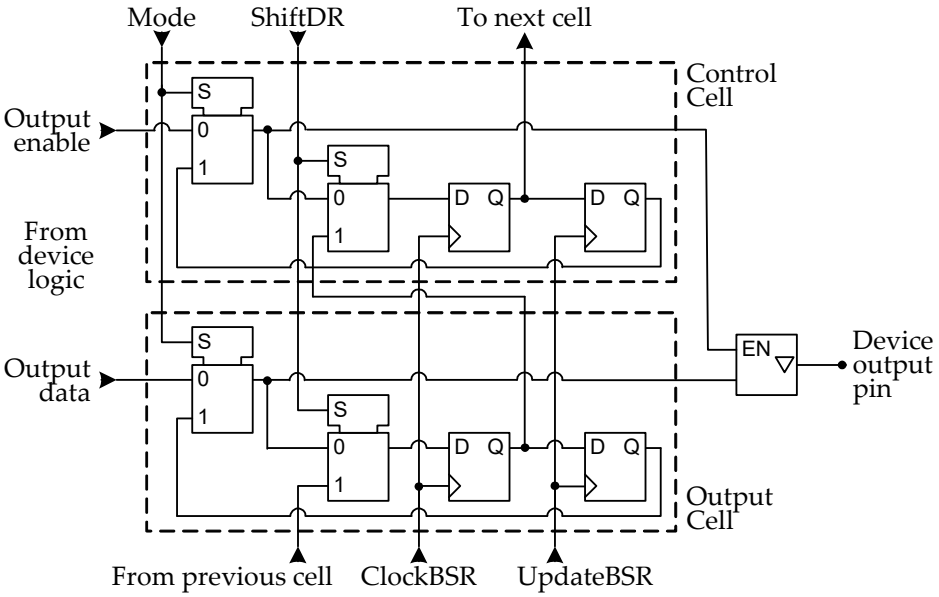
Each EDC pin is equipped with two boundary scan cells. For EDC 1 the first cell is the same combined input and output boundary scan cell for input data capture and output data as for a DQ pin. For the other EDC pins the first cell holds the output data. For all EDC pins the second cell controls the output enable.

11.3 TAP REGISTERS (cont'd)

Boundary scan input cell



Boundary scan cell at three-state output



Boundary scan cell at bidirectional I/O

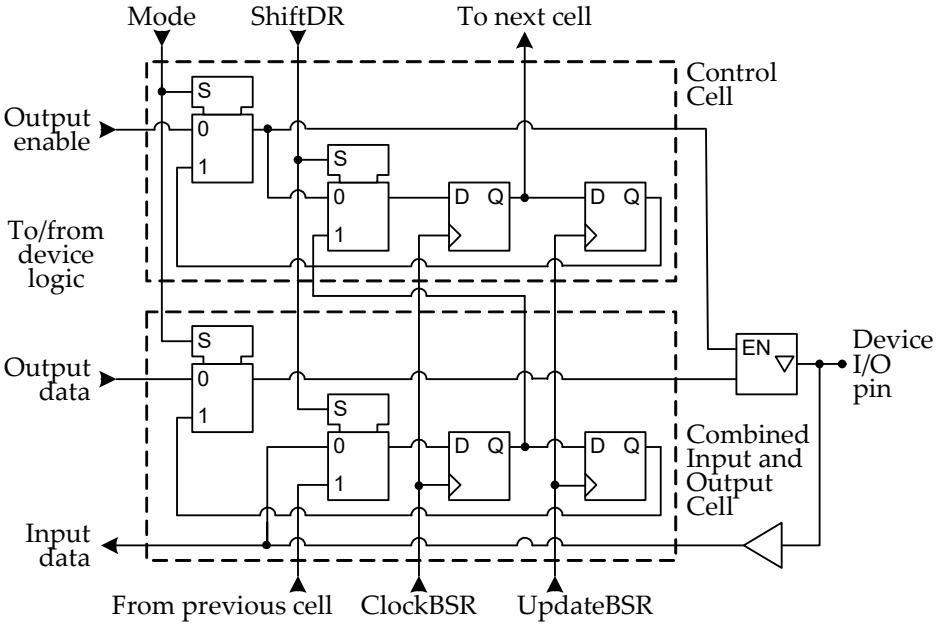


Figure 121 — Example Boundary Scan Cells

11.3 TAP REGISTERS (cont'd)

The boundary scan register has a fixed length of 77 for all densities, and the boundary scan cells shall be connected as outlined in Table 64.

Table 64 — Boundary Scan Register Bit Order

BIT	BALL	TYPE	PIN	BIT	BALL	TYPE	PIN	BIT	BALL	TYPE	PIN	BIT	BALL	TYPE	PIN
0	B-4	I/O	DQ0	20	K-2	I	RESET_n	40	V-11	I/O	DQ16	60	J-11	I	BA0 A2
1	B-3	I/O	DQ1	21	L-4	I	A8 A7	41	V-12	I/O	DQ17	61	J-10	I	BA3 A3
2	C-4	I/O	DQ2	22	L-5	I	A11 A6	42	U-11	I/O	DQ18	62	H-11	I	CKE_n
3	C-3	I/O	DQ3	23	M-4	I	CAS_n	43	U-12	I/O	DQ19	63	H-13	I	ZQ
4	D-3	OE	EDC0	24	N-3	I/O	DQ31	44	T-12	OE	EDC2	64	G-12	I/O	DQ15
5	D-3	O	EDC0	25	N-4	I/O	DQ30	45	T-12	O	EDC2	65	G-11	I/O	DQ14
6	D-5	I	WCK01_c	26	P-3	I/O	DQ29	46	–	OE	DQ[23:16]	66	F-12	I/O	DQ13
7	D-4	I	WCK01_t	27	P-4	I/O	DQ28	47	R-12	OE	DBI2_n	67	F-11	I/O	DQ12
8	–	OE	DQ[7:0]	28	R-3	OE	DBI3_n	48	R-12	I/O	DBI2_n	68	E-12	OE	DBI1_n
9	E-3	OE	DBI0_n	29	R-3	I/O	DBI3_n	49	P-11	I/O	DQ20	69	E-12	I/O	DBI1_n
10	E-3	I/O	DBI0_n	30	–	OE	DQ[31:24]	50	P-12	I/O	DQ21	70	–	OE	DQ[15:8]
11	F-4	I/O	DQ4	31	T-4	I	WCK23_t	51	N-11	I/O	DQ22	71	D-12	OE	EDC1
12	F-3	I/O	DQ5	32	T-5	I	WCK23_c	52	N-12	I/O	DQ23	72	D-12	I/O	EDC1
13	G-4	I/O	DQ6	33	T-3	OE	EDC3	53	M-11	I	WE_n	73	C-12	I/O	DQ11
14	G-3	I/O	DQ7	34	T-3	O	EDC3	54	L-10	I	BA1 A5	74	C-11	I/O	DQ10
15	H-4	I	RAS_n	35	U-3	I/O	DQ27	55	L-11	I	BA2 A4	75	B-12	I/O	DQ9
16	J-5	I	A9 A1	36	U-4	I/O	DQ26	56	K-13	I	VREFC	76	B-11	I/O	DQ8
17	J-4	I	A10 A0	37	V-3	I/O	DQ25	57	K-12	I	A14 A15				
18	K-5	I	A12 A13	38	V-4	I/O	DQ24	58	K-11	I	CK_t				
19	K-4	I	ABI_n	39	W-12	I	MF	59	K-10	I	CK_c				

NOTE 1 Register types: I = input cell; O = output cell; I/O = combined input and output cell; OE = output enable control cell.
NOTE 2 Pin names are shown for MF=0 configuration.

11.4 TAP INSTRUCTION SET

Table 65 summarizes the instructions supported by the TAP controller. Instruction codes not listed in the table may be used by the DRAM vendor for vendor specific instructions.

Table 65 — Boundary Scan Instructions

Instruction	Op-Code	Active Data Register
BYPASS	0x00	Bypass
SAMPLE/PRELOAD	0x01	Boundary Scan
IDCODE	0x02	Identification
CLAMP	0x04	Boundary Scan / Bypass
HIGH-Z	0x08	Bypass
EXTEST	0x10	Boundary Scan
BYPASS	0xFF	Bypass

SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction provides two functions. The SAMPLE function allows a snapshot of the states of the device's input and output signals to be taken without interfering with the system's normal operation; the snapshot is taken and captured in the boundary scan register on the rising edge of TCK when the TAP controller is in the Capture-DR state. The data can then be viewed by shifting through the device's TDO output.

The PRELOAD function allows an initial data pattern to be placed at the latched parallel outputs of boundary scan register cells before the selection of another boundary scan test operation, for example, before the selection of the EXTEST instruction. As soon as the EXTEST instruction has been transferred to the parallel output of the instruction register, the preloaded data are driven through the system output pins.

IDCODE

The IDCODE instruction causes loading of a vendor-specific, 32-bit code into the identification register. It also places the identification register between the TDI and TDO pins and enables shifting the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is in the Test-Logic-Reset state.

CLAMP

The CLAMP instruction allows the state of the device's output pins to be determined from the boundary scan register, while the bypass register is selected as the serial path between TDI and TDO. Data in the boundary scan register may result from the previous use of the PRELOAD instruction. The signals driven from the output pins do not change while the CLAMP instruction is selected.

HIGH-Z

The High-Z instruction places all device output pins into a High-Z state; it causes the bypass register to be connected between TDI and TDO.

EXTEST

The EXTEST instruction allows testing of off-chip circuitry and board-level interconnections. Test data typically would be loaded onto the latched parallel outputs of boundary scan shift-register stages using the PRELOAD instruction before selection of the EXTEST instruction.

When the EXTEST instruction is selected, the state of all signals driven from the device's output pins changes only on the falling edge of TCK in the Update-DR controller state, and the state of all signals received at the device's input pins shall be loaded into the boundary scan register on the rising edge of TCK in the Capture-DR controller state.

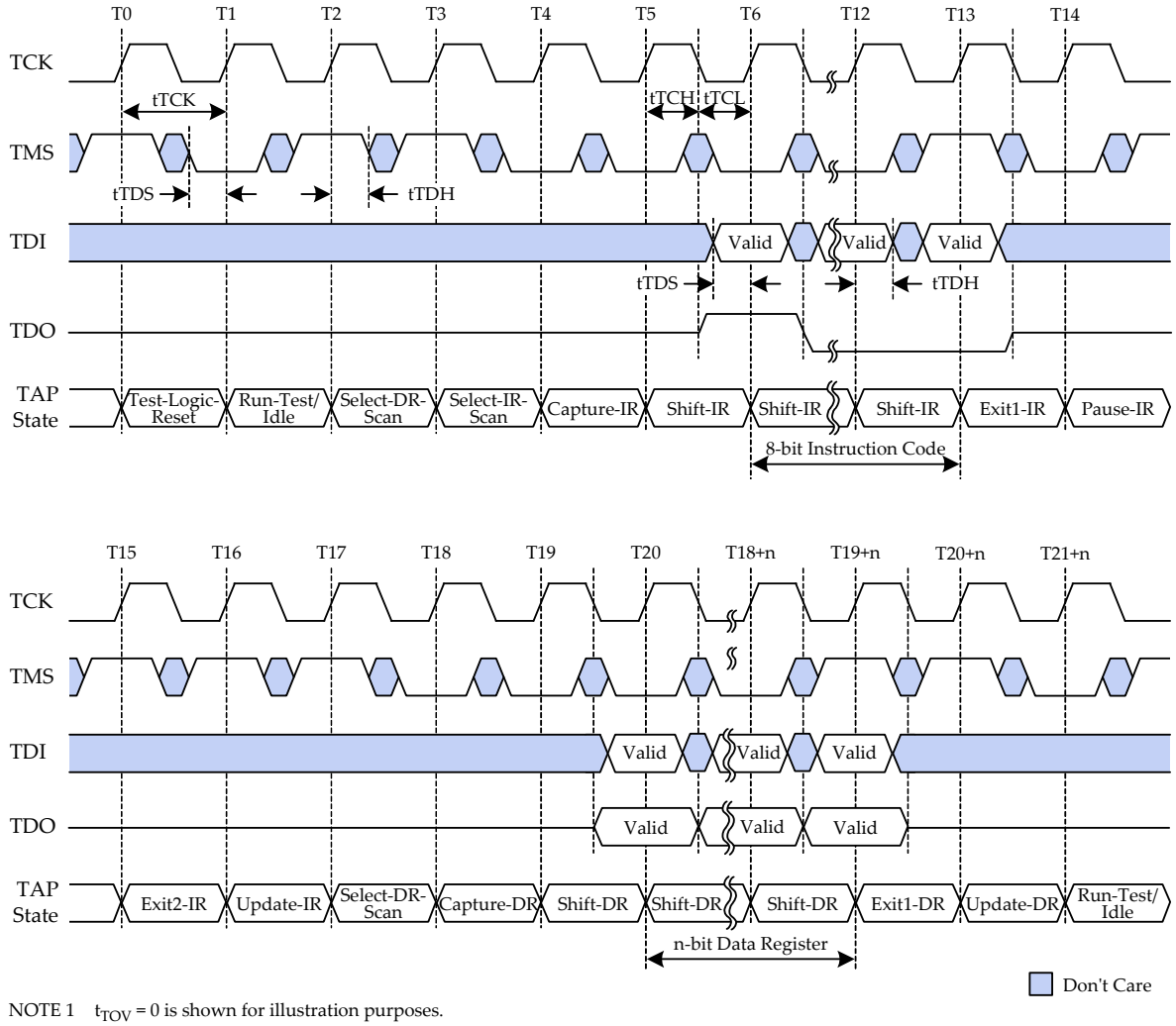
11.4 TAP INSTRUCTION SET (cont'd)

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. Please note that two op-codes are associated with the BYPASS instruction.

11.5 BOUNDARY SCAN OPERATION

Figure 122 illustrates a typical boundary scan test port operating sequence. The TAP states correspond to those shown in Figure 119. The sequence starts from the Test-Logic-Reset state. At first an instruction is serially loaded into the instruction register at clock edges T6 through T13 and latched in the Update_IR state at T16. The TAP then advances to the data register states, to parallel-load test data into the test data register in the Capture-DR state at T19, serially shift the test data in the Shift-DR state starting at T20, and finally to update the test data register's parallel outputs in the Update-DR state at T20+n.



NOTE 1 t_{TOV} = 0 is shown for illustration purposes.

Figure 122 — Example Boundary Scan Operation

11.5 BOUNDARY SCAN OPERATION (cont'd)

Table 66 — Boundary Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNIT
TCK clock cycle time	t_{TCK}	20	-	ns
TCK clock high-level width	t_{TCH}	0.45	-	t_{TCK}
TCK clock low-level width	t_{TCL}	0.45	-	t_{TCK}
TDI, TMS input setup time to rising TCK edge	t_{TDS}	2.5	-	ns
TDI, TMS input hold time from rising TCK edge	t_{TDH}	2.5	-	ns
TDO output hold time from falling TCK edge	t_{TOH}	0	-	ns
TDO output valid time from falling TCK edge	t_{TOV}	-	5	ns

11.6 INTERACTIONS BETWEEN BOUNDARY SCAN AND NORMAL DEVICE OPERATION

Boundary scan operation may be initiated at any time after all voltages are stable (step 3 of the power-up sequence). Interactions between normal device operation and boundary scan operation depend on the selected scan instruction (see Table 65):

- Instructions BYPASS, IDCODE and SAMPLE/PRELOAD can be loaded and executed in parallel with normal device operation. The state of the high speed pins is not impacted by these scan instructions, and all commands are executed as normal. It is pointed out that the SAMPLE function of the SAMPLE/PRELOAD instruction is not supported; any data sampled with this instruction shall be ignored.
- Instructions EXTEST, CLAMP and HIGH-Z take control of the high speed pins and therefore cannot be executed in parallel with normal device operation. The device disables the command decoder, terminates all ongoing command executions and forces the device into reset state once one of these instructions is loaded into the instruction register.

  Once boundary scan operation has been completed, the device may return to normal operation without cycling through power-off and power-on by following this sequence:

  1. Assert RESET_n to Low.

  2. Terminate boundary scan operation by setting the TAP controller back to Test-Logic-Reset state; this state will load the IDCODE instruction into the instruction register, enable the command decoder and release control of the high speed pins.

  3. Maintain RESET_n Low for a minimum time of t_{RES}, then continue with step 3 of the initialization with stable power sequence.

Annex A - (Informative) Differences between JESD232 and JESD232A

This annex briefly describes most of the changes made to entries that appear in this standard, JESD232A, compared to its predecessor, JESD232 (November 2015). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Minor punctuation and formatting changes are not included.

Page	Description of Change
3	3.1, Functional overview: two redundant paragraphs deleted; paragraphs are part of section 3.3 (Clocking)
15, 19,107, 138,141	Minor wording changes for improved readability
25,35	4, Mode Registers; 4.6, MR5: "PLL/DLL Bandwidth" field width reduced from 3 bits to 2 bits; bit A5 is now RFU
51	6.3, WCK2CK training: condition added that training with WCK stop is restricted to $f_{WCKSTOP}$
64	7.1, Commands: abbreviation for all-bank refresh command changed from "REF" to "REFAB"
76	7.6.1, DQ write preamble: wording changes; timing diagram deleted
93	7.9, Read: redundant arrow "t_{CCD}" in Figure 90 (Read-to-Write) deleted
100	7.11.2, Per-Bank Refresh command: example added (Table 29 and text); self refresh entry command added to Table 30
107	7.13, Power-down: typo fixed in Table 33 ("off" to "active")
117	8.6, DC & AC Operating Conditions: V_{IDCK}(DC) value in Table 46 corrected from 0.19V to 0.198V (typo)
119	8.7, I_{DD} and I_{PP} Specifications and Test Conditions: definition of I_{PPx} currents added
126	8.8, AC Timings: parameter $f_{WCKSTOP}$ added; "PLL" changed to "PLL/DLL" for consistency
137	9.1, Signal Description: descriptions for BA[3:0] and MF pins corrected
147,149	11.3, TAP registers: EDC1 pin changed from output to bidirectional; text and bit 72 in Table 64 adjusted

Annex B - (Informative) Differences between JESD232A.01 and JESD232A

This annex briefly describes most of the changes made to entries that appear in this standard, JESD232A.01, compared to its predecessor, JESD232A (August 2016). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Minor punctuation and formatting changes are not included.

1. Terminology update, replacing all instances of “master” with “controller” and “slave” with “target”
2. Reformatted Table of Contents to JEDEC standard

Standard Improvement Form **JEDEC Standard JESD232A.01**

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