JEDEC STANDARD

POD15 - 1.5V Pseudo Open Drain I/O

JESD8-20A.01

(Revision of JESD8-20A, October 2009)

AUGUST 2022

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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POD15 - 1.5V PSEUDO OPEN DRAIN I/O

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POD15 - 1.5V PSEUDO OPEN DRAIN I/O

(From JEDEC Board ballot JCB-09-71, formulated under the cognizance of the JC-16 Committee on Voltage Level and Electrical Interface.)

1 Scope

This standard defines the DC and AC single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.5 V Pseudo Open Drain I/Os. The 1.5 V Pseudo Open Drain interface, also known as POD15, is primarily used to communicate with GDDR4 and GDDR5 SGRAM devices.

2 Operating Conditions

Table 1 — DC Operating Conditions

Parameter	Symbol	POD15			Unit	Notes
		Min	Typ	Max		
Device Supply Voltage	VDD	1.455	1.5	1.545	V	1
Output Supply Voltage	VDDQ	1.455	1.5	1.545	V	1
Reference Voltage	VREF	0.69 * VDDQ		0.71 * VDDQ	V	2, 9
Reference Voltage for DQ and DBI# pins	VREFD	0.69 * VDDQ		0.71 * VDDQ	V	2, 3, 10
Reference Voltage for DQ and DBI# pins	VREFD2	0.49 * VDDQ		0.51 * VDDQ	V	2, 3, 4, 10
External Reference Voltage for address and command	VREFC	0.69 * VDDQ		0.71 * VDDQ	V	5, 10
DC Input Logic HIGH Voltage	VIH (DC)	VREF + 0.12			V	9
DC Input Logic LOW Voltage	VIL (DC)			VREF - 0.12	V	9
DC Input Logic HIGH Voltage for address and command	VIHA (DC)	VREFC + 0.15			V	10
DC Input Logic LOW Voltage for address and command	VILA (DC)			VREFC - 0.15	V	10
DC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD	VIHD (DC)	VREFD + 0.10			V	10
DC Input Logic LOW Voltage for DQ and DBI# pins with VREFD	VILD (DC)			VREFD - 0.10	V	10
DC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD2	VIHD2 (DC)	VREFD2 + 0.30			V	10
DC Input Logic LOW Voltage for DQ and DBI# pins with VREFD2	VILD2 (DC)			VREFD2 - 0.30	V	10
Input Logic HIGH Voltage for RESET#, SEN, MF	VIHR	VDDQ - 0.50			V	10
Input Logic LOW Voltage for RESET#, SEN, MF	VILR			0.30	V	10
Input logic HIGH voltage for EDC1/2 (x16 mode detect)	VIHX	VDDQ - 0.3			V	8, 10
Input logic LOW voltage for EDC1/2 (x16 mode detect)	VILX			0.30	V	8, 10
Input Leakage Current Any Input 0V <= V_{IN} <= VDDQ (All other pins not under test = 0V)	Il				µA	
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz				µA	
Output Logic LOW Voltage	VOL (DC)			0.62	V	

NOTE 1 GDDR4 and GDDD5 SGRAMs are designed to tolerate PCB designs with separate VDD and VDDQ power regulators.

NOTE 2 AC noise in the system is estimated at 50 mV pk-pk for the purpose of DRAM design.

NOTE 3 Source of Reference Voltage and control of Reference Voltage for DQ and DBI# pins is determined by VREFD, Half VREFD, Auto VREFD, VREFD MERGE and VREFD Offsets mode registers.

NOTE 4 VREFD Offsets are not supported with VREFD2.

NOTE 5 External VREFC is to be provided by the controller as there is no other alternative supply.

NOTE 6 DQ/DBI# input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFD crossing and VIHD(AC) or VILD(AC) or VREFD2 crossing and VIHD2(AC) or VILD2(AC).

NOTE 7 ADR/CMD input slew rate must be greater than or equal to 3V/ns. The slew rate is measured between VREFC crossing and VIHA(AC) or VILA(AC).

NOTE 8 VIHX and VILX define the voltage levels for the receiver that detects x32 or x16 mode with RESET# going High.

NOTE 9 Applicable to GDDR4 or other interface with a single VREF for the device.

NOTE 10 Applicable to GDDR5 or other interface with multiple VREF pins and levels.

2 Operating Conditions (cont'd)

Table 2 — AC Operating Conditions

Parameter	Symbol	POD15			Unit	Note
		Min	Typ	Max		
AC Input Logic HIGH Voltage	VIH (AC)	VREFC + 0.20			V	1
AC Input Logic Low Voltage	VIL (AC)			VREFC - 0.20	V	1
AC Input Logic HIGH Voltage for address and command	VIHA (AC)	VREFC + 0.20			V	2
AC Input Logic LOW Voltage for address and command	VILA (AC)			VREFC - 0.20	V	2
AC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD	VIHD (AC)	VREFD + 0.15			V	2
AC Input Logic LOW Voltage for DQ and DBI# pins with VREFD	VILD (AC)			VREFD - 0.15	V	2
AC Input Logic HIGH Voltage for DQ and DBI# pins with VREFD2	VIHD2 (AC)	VREFD2 + 0.40			V	2
AC Input Logic LOW Voltage for DQ and DBI# pins with VREFD2	VILD2 (AC)			VREFD2 - 0.40	V	2

NOTE 1 Applicable to GDDR4 or other interface with a single VREF for the device.
NOTE 2 Applicable to GDDR5 or other interface with multiple VREF pins and levels.

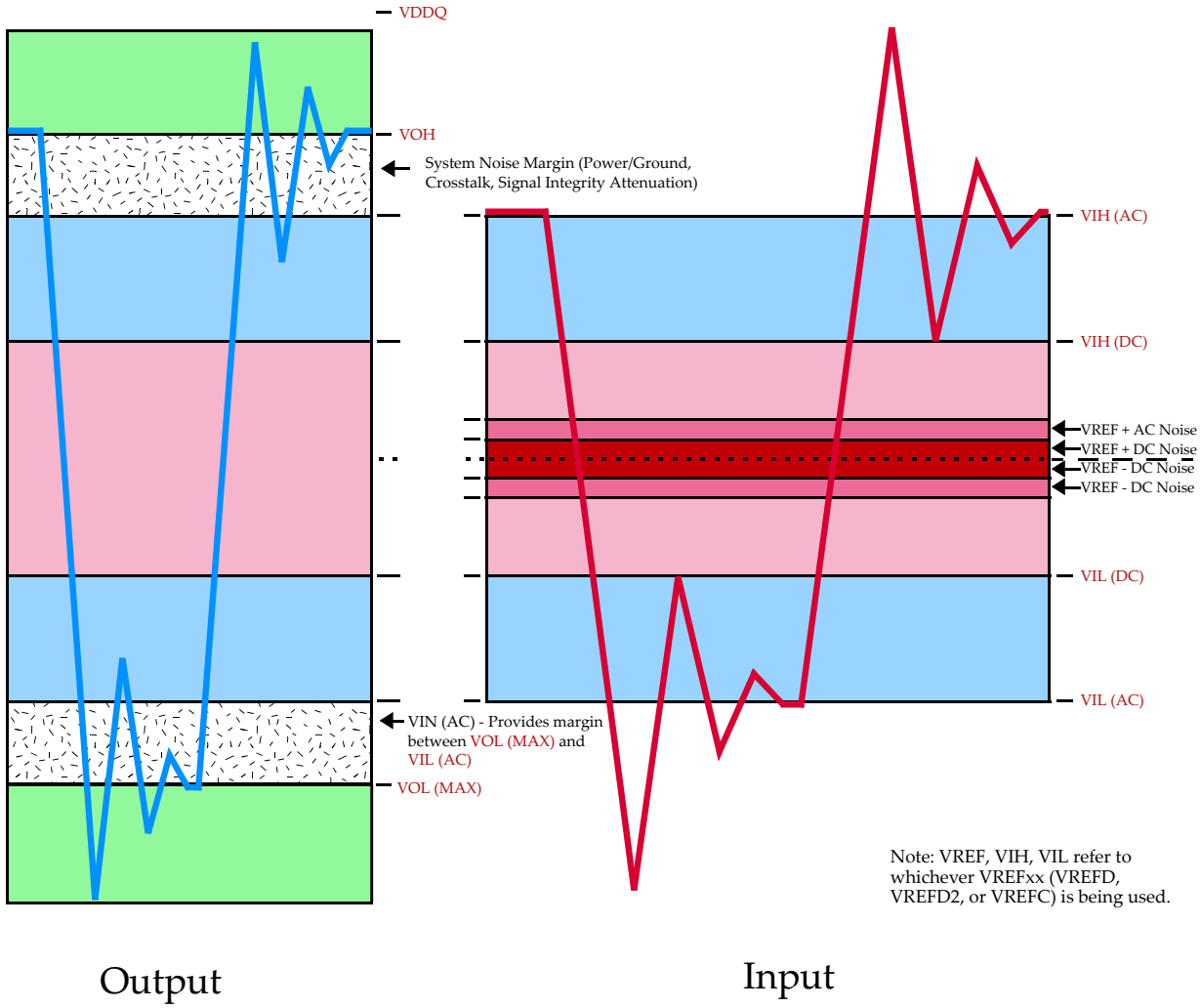


Figure 1 — Voltage Waveform

2 Operating Conditions (cont'd)

Table 3 — Clock Input Operating Conditions

Parameter	Symbol	POD15		Unit	Note
		Min	Max		
Clock Input Mid-Point Voltage; CK and CK#	VMP (DC)	VREFC - 0.10	VREFC + 0.10	V	1, 6
Clock Input Differential Voltage; CK and CK#	VID or VIDCK (DC)	0.22		V	4, 6
Clock Input Differential Voltage; CK and CK#	VID or VIDCK (AC)	0.40		V	2, 4, 6
Clock Input Differential Voltage; WCK and WCK#	VIDWCK (DC)	0.20		V	5, 7, 14
Clock Input Differential Voltage; WCK and WCK#	VIDWCK (AC)	0.30			2, 5, 7, 14
Clock Input Voltage Level; CK, CK#, WCK and WCK# single ended	VIN	-0.30	VDDQ + 0.30		
CK/CK# Single ended slew rate	CKslew	3		V/ns	9
WCK/WCK# Single ended slew rate	WCKslew	3		V/ns	10, 14
Clock Input Crossing Point Voltage; CK and CK#	VIX or VIXCK (AC)	VREFC - 0.12	VREFC + 0.12	V	2, 3, 6
Clock Input Crossing Point Voltage; WCK and WCK#	VIXWCK (AC)	VREFD - 0.10	VREFD + 0.10	V	2, 3, 7, 8, 14
Allowed time before ringback of CK/WCK below VIDCK/WCK(AC)	t_{DVAC}			ps	11, 12, 13, 14

NOTE 1 This provides a minimum of 0.9V to a maximum of 1.2 V, and is nominally 70% of VDDQ with POD15. DRAM timings relative to CK cannot be guaranteed if these limits are exceeded.

NOTE 2 For AC operations, all DC clock requirements must be satisfied as well.

NOTE 3 The value of VIXCK and VIXWCK is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.

NOTE 4 VIDCK is the magnitude of the difference between the input level in CK and the input level on CK#. The input reference level for signals other than CK and CK# is VREFC.

NOTE 5 VIDWCK is the magnitude of the difference between the input level in WCK and the input level on WCK#. The input reference level for signals other than WCK and WCK# is either VREFD, VREFD2 or the internal VREFD.

NOTE 6 The CK and CK# input reference level (for timing referenced to CK and CK#) is the point at which CK and CK# cross.

NOTE 7 The WCK and WCK# input reference level (for timing referenced to WCK and WCK#) is the point at which WCK and WCK# cross.

NOTE 8 VREFD is either VREFD, VREFD2 or the internal VREFD.

NOTE 9 The slew rate is measured between VREFC crossing and VIXCK(AC).

NOTE 10 The slew rate is measured between VREFD crossing and VIXWCK(AC).

NOTE 11 Figure 3 illustrates the exact relationship between (CK-CK#) or (WCK-WCK#) and VID(AC), VID(DC) and t_{DVAC}

NOTE 12 Ringback below VID(DC) is not allowed.

NOTE 13 t_{DVAC} is not measured in and of itself as a compliance specification, but is relied upon in measurement of clock operating conditions and clock related parameters.

NOTE 14 Applicable to GDDR5 or other interface with multiple VREF pins and levels.

2 Operating Conditions (cont'd)

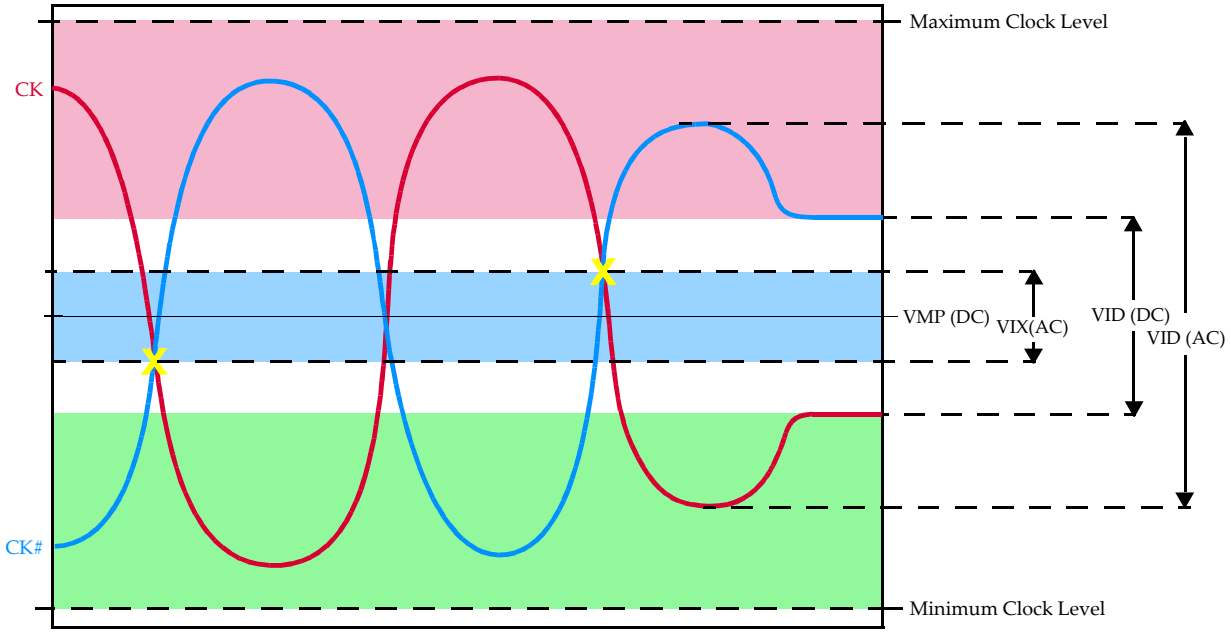


Figure 2 — Clock Waveform

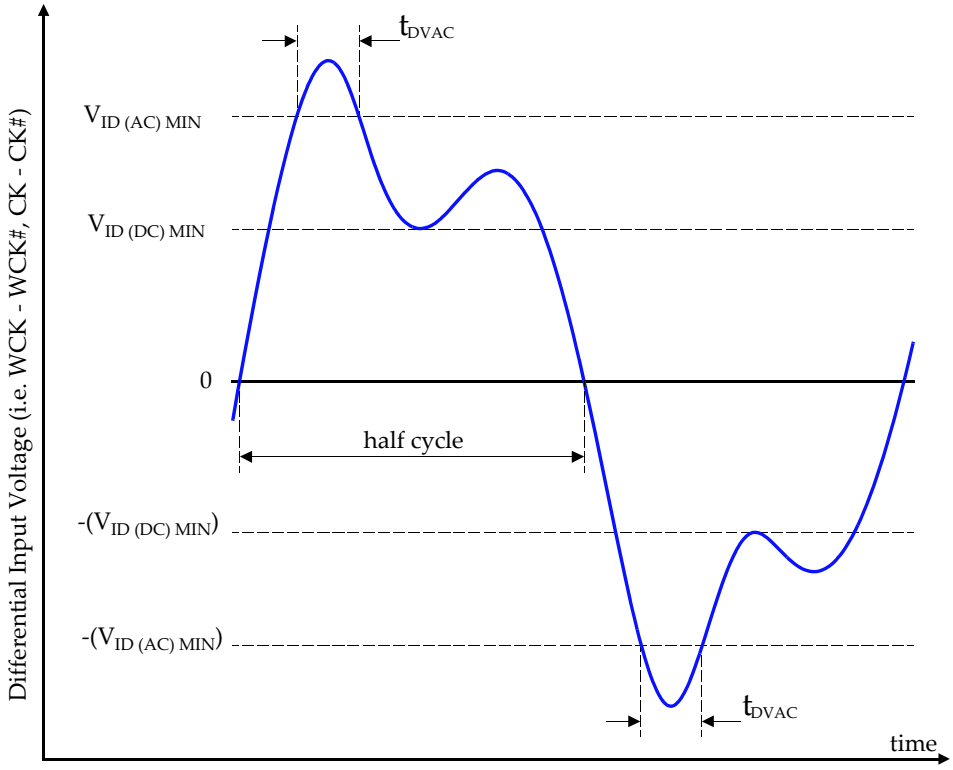


Figure 3 — Definition of Differential AC-Swing and "Time Above AC-Level" t_{DVAC}

2 Operating Conditions (cont'd)

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.5 V (VDD/VDDQ)
2. Power the DRAM device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3. Reduce temperature to 10 °C recalibrate.
4. Reduce temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate
6. Raise temperature to 85 °C and take the slow corner measurement
7. Reiterate 2 to 6 with VDD/VDDQ 1.455 V
8. Reiterate 2 to 6 with VDD/VDDQ 1.545 V
9. All obtained Driver and Termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics

The following values (Ideal with +/- 10% min/max) are targets for the designer and are not required to be met. Vendor datasheets should be consulted for further details. It is expected that the characteristics of the real curves will have some non-linearity as shown in Figure 6 and Figure 7. This may help to reduce the overall capacitance and boost performance. It is up to the designer to find the optimum combination of linearity and capacitance for best Rx and Tx performance.

Table 4 — 1.5 V I/O Impedances

Pull-Down Characteristic at 40 Ohms			
Voltage (V)	**MIN (mA)**	**Ideal (mA)**	**MAX (mA)**
0.1	2.25	2.50	2.75
0.2	4.50	5.00	5.50
0.3	6.75	7.50	8.25
0.4	9.00	10.00	11.00
0.5	11.25	12.50	13.75
0.6	13.50	15.00	16.50
0.7	15.75	17.50	19.25
0.8	18.00	20.00	22.00
0.9	20.25	22.50	24.75
1.0	22.50	25.00	27.50
1.1	24.75	27.50	30.25
1.2	27.00	30.00	33.00
1.3	29.25	32.50	35.75
1.4	31.50	35.00	38.50
1.5	33.75	37.50	41.25

Pull-Up/Termination Characteristic at 60 Ohms			
Voltage (V)	**MIN (mA)**	**Ideal (mA)**	**MAX (mA)**
0.1	-1.50	-1.67	-1.83
0.2	-3.00	-3.33	-3.67
0.3	-4.50	-5.00	-5.50
0.4	-6.00	-6.67	-7.33
0.5	-7.50	-8.33	-9.17
0.6	-9.00	-10.00	-11.00
0.7	-10.50	-11.67	-12.83
0.8	-12.00	-13.33	-14.67
0.9	-13.50	-15.00	-16.50
1.0	-15.00	-16.67	-18.33
1.1	-16.50	-18.33	-20.17
1.2	-18.00	-20.00	-22.00
1.3	-19.50	-21.67	-23.83
1.4	-21.00	-23.33	-25.67
1.5	-22.50	-25.00	-27.50

2 Operating Conditions (cont'd)

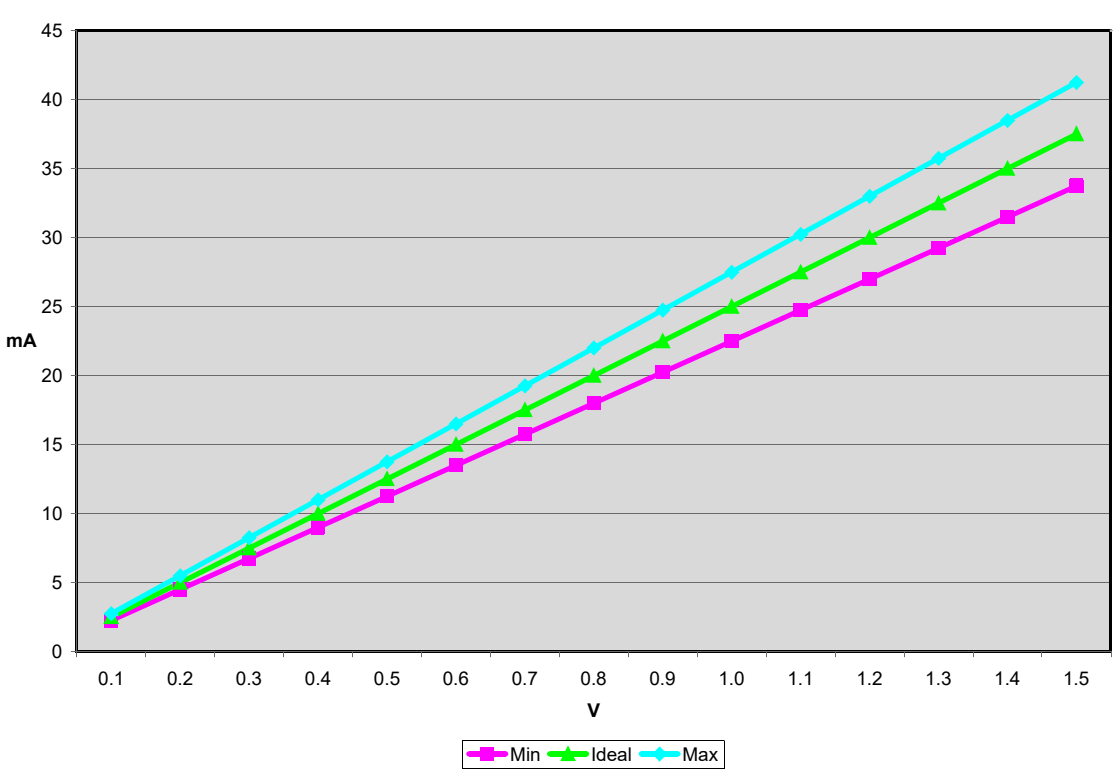


Figure 4 — Target Pull Down Characteristic at 40 Ohms

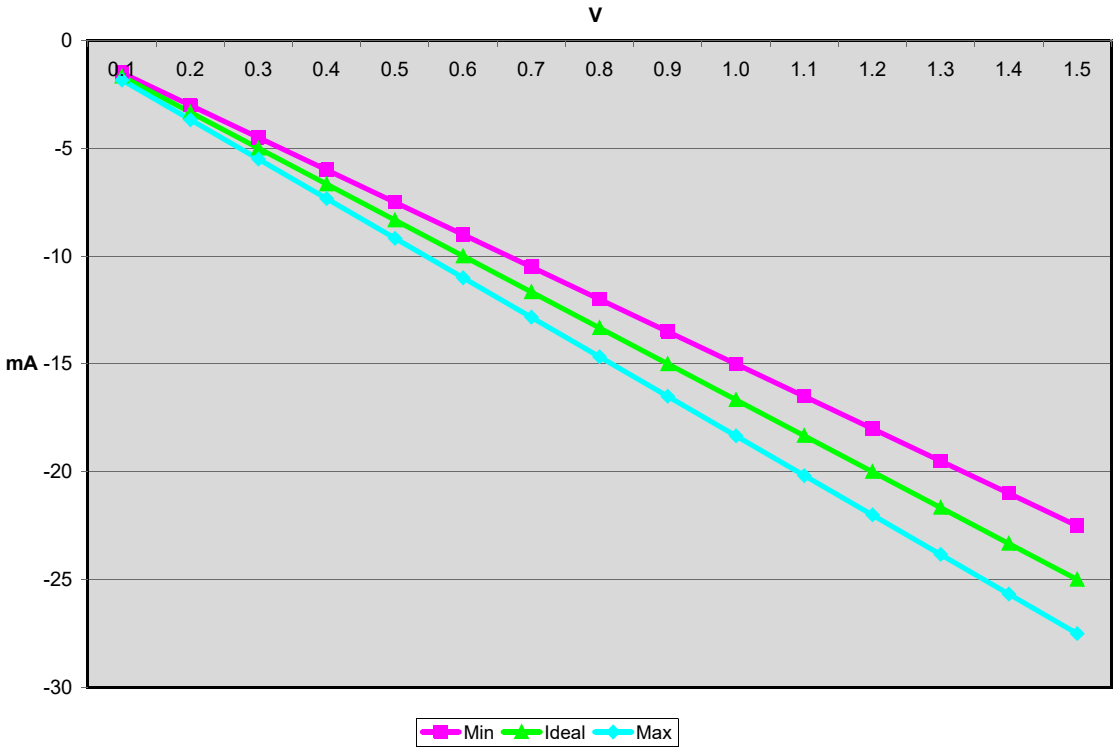


Figure 5 — Target Pull Up/Termination Characteristic at 60 Ohms

2 Operating Conditions (cont'd)

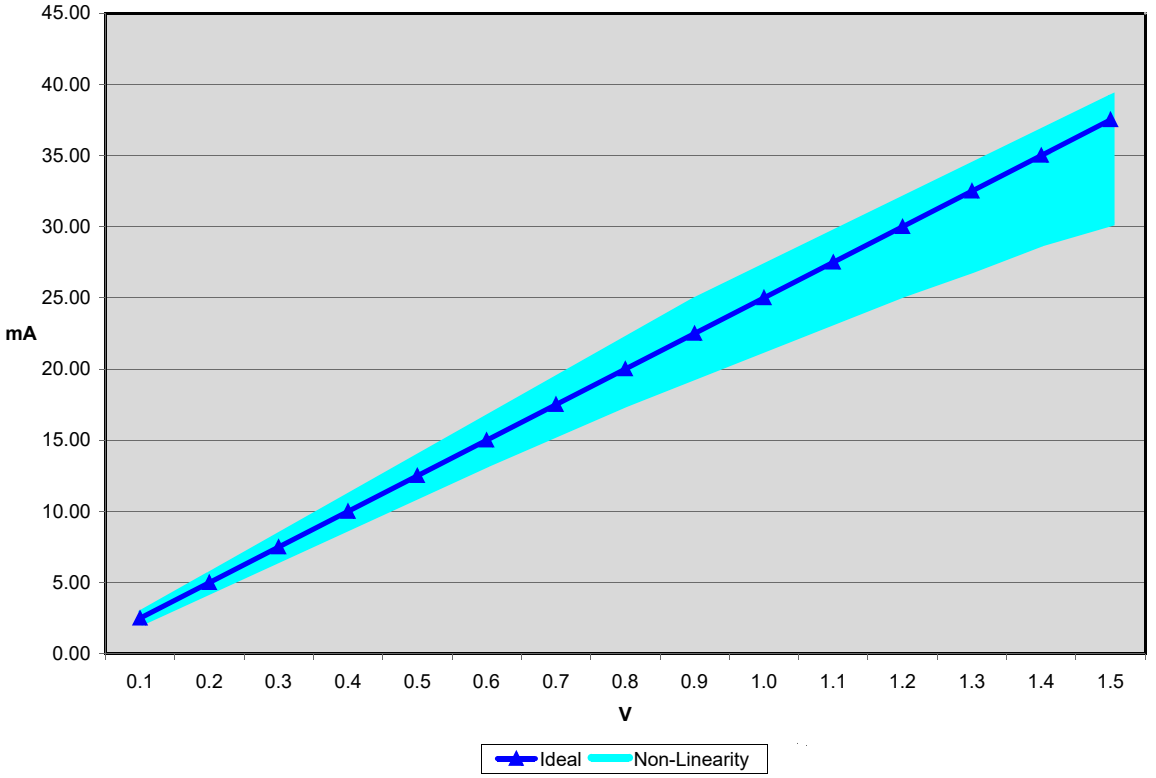


Figure 6 — Example of Non-linearity, Pull Down Characteristic at 40 Ohms

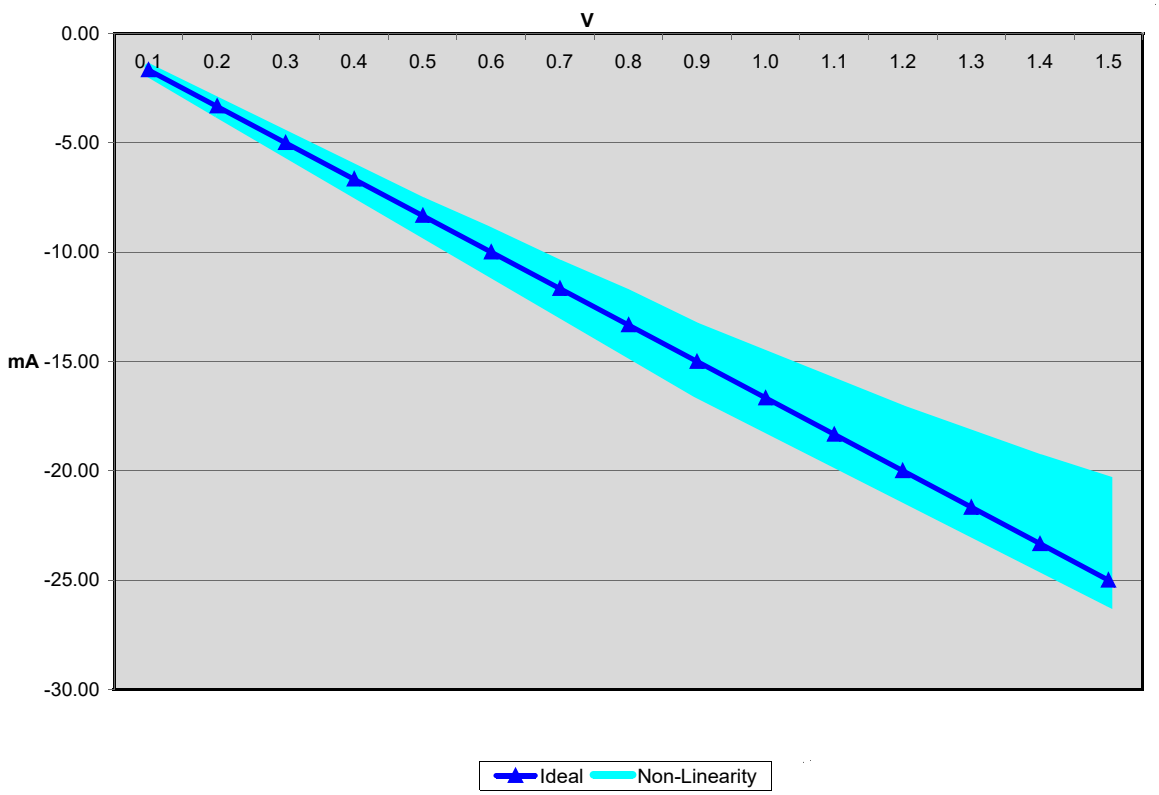


Figure 7 — Example of Non-linearity, Pull Up/Termination Characteristic at 60 Ohms

3 Additional Background Information

The POD I/O system is optimized for small systems with data rates exceeding 2.0 Gbps. The system allows a single Initiator to control one or two Targets in the case of GDDR5 and one, two or four Targets in the case of GDDR4. The POD driver uses a 40/60 ohm output impedance that drives into a 60 ohm equivalent terminator tied to VDDQ. Single, dual and quad load systems are shown as follows:

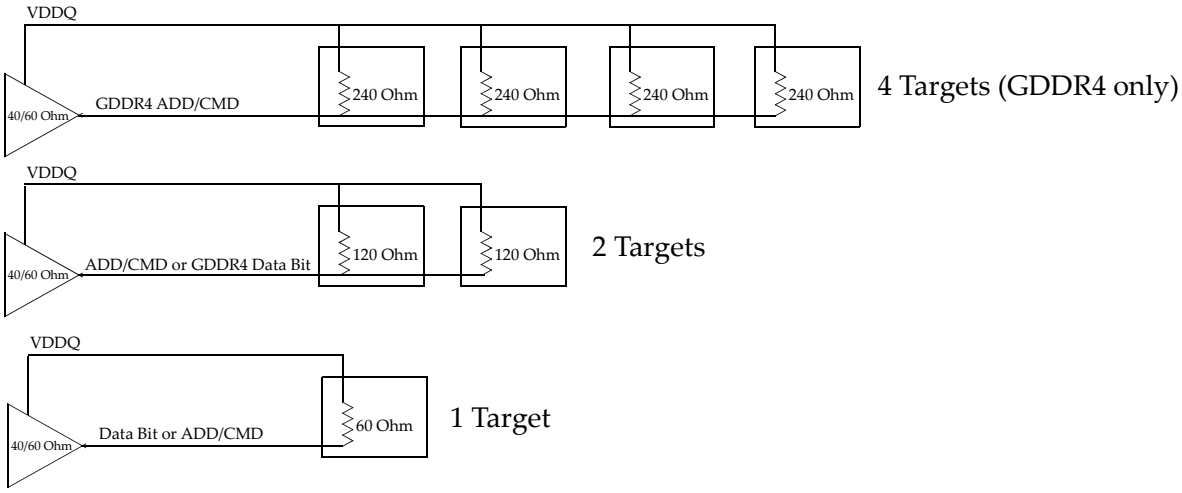


Figure 8 — System Configurations

The POD Initiator I/O cell is comprised of a 40/60 ohm driver and a terminator of 60 ohms. The Initiator POD cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 9.

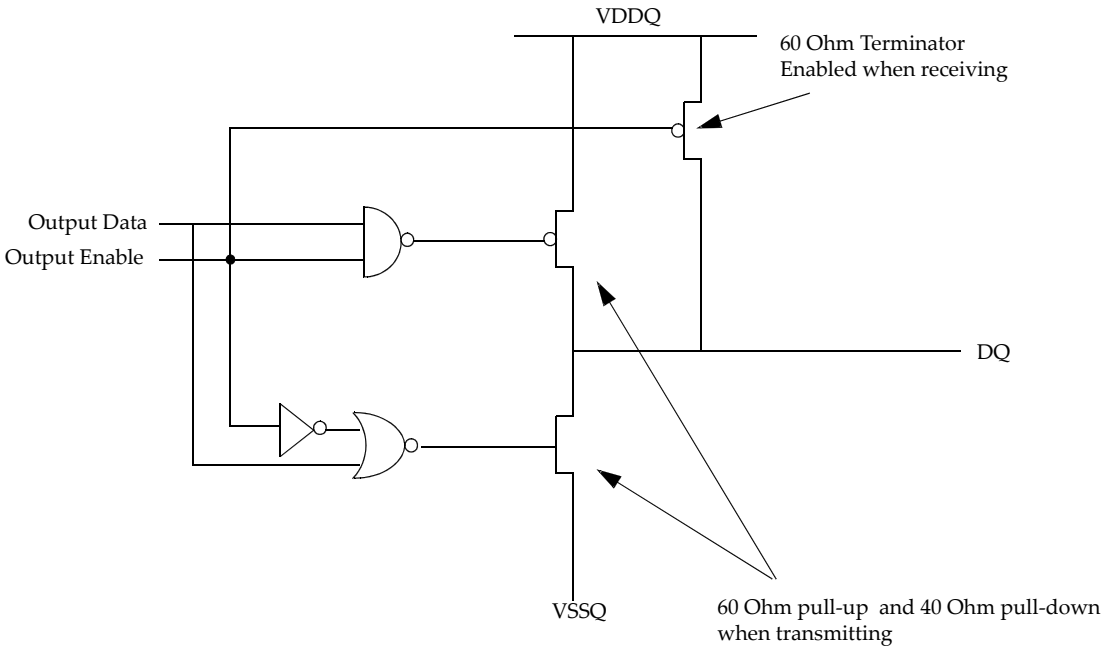


Figure 9 — Initiator I/O Cell

3 Additional Background Information (cont'd)

The POD Target I/O cell is comprised of a 40/60 ohm driver and programmable terminator of 60 or 120 ohms for GDDR5 and 60, 120, or 240 ohms for GDDR4. The Target POD cell's terminator is disabled when the output driver is enabled or any other Target output driver is enabled. The basic cell is shown in Figure 10.

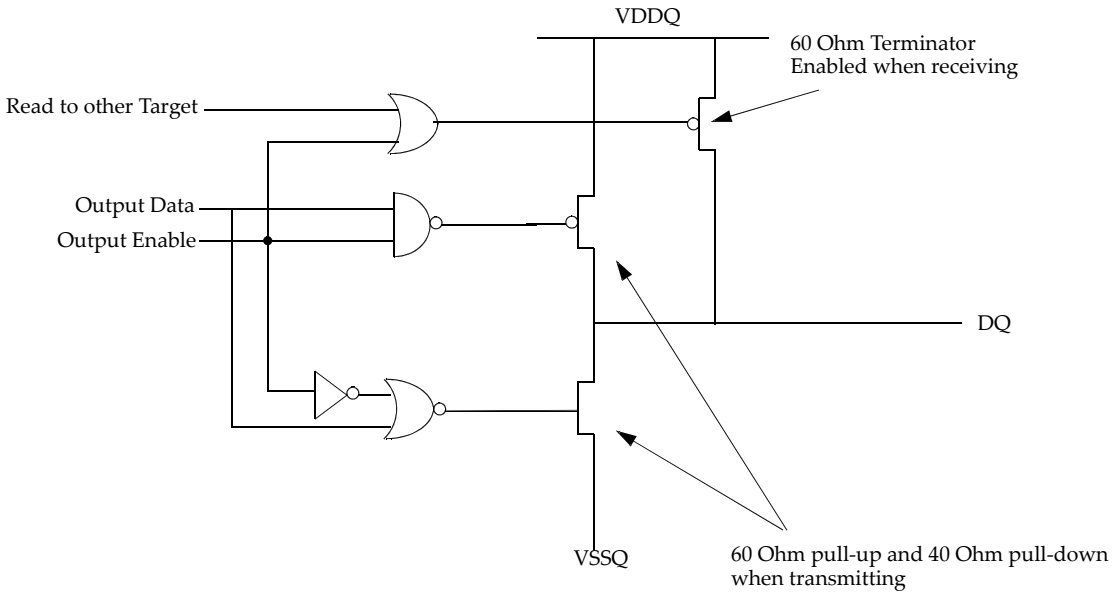


Figure 10 — Target I/O Cell

The POD Initiator and Target I/O cells are intended to have their driver and terminators combined together to minimize the area needed to implement the cell and reduce input capacitance. For GDDR4 this is possible by using six 240 ohm driver/terminator sub cells that are connected in parallel. The combinations used are shown in Table 5 and Table 6.

Table 5 — POD I/O Sub Cells, 240 Ohm Based

# of 240 Ohm Sub Cells Enabled	Resulting Impedance	Use
1	240 ohms	4 Target loads
2	120 ohms	2 Target loads
4	60 ohms	1 Target load or Initiator terminator
6	40 ohms	Initiator or Target Driver

For GDDR5 this is possible by using three 120 Ohm driver/terminator sub cells that are connected in parallel. The combinations used are as follows.

Table 6 — POD I/O Sub Cells, 120 Ohm Based

# of 120 Ohm Sub Cells Enabled	Resulting Impedance	Use
1	120 ohms	2 Target loads or
2	60 ohms	1 Target load or Initiator terminator
3	40 ohms	Initiator or Target Driver

3 Additional Background Information (cont'd)

To ensure that the target impedance is achieved the POD I/O cell is designed to be calibrated to an external 1% precision resistor.

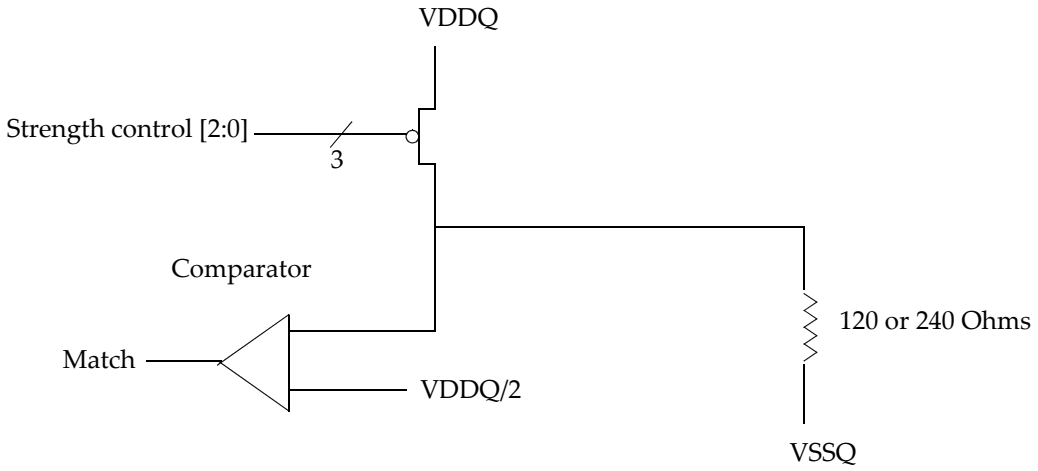
The following procedure may be used to calibrate the cell:

1.) First calibrate the PMOS device against a 120 (GDDR5) or 240 (GDDR4) ohm resister to VSS via the ZQ pin as illustrated in Figure 11.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VDDQ/2
- PMOS device is calibrated to 120 or 240 ohms

2.) Then calibrate the NMOS device against the calibrated 120 (GDDR5) or 240 (GDDR4) Ohm PMOS device as illustrate in Figure 12.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than VDDQ/2
- NMOS device is now calibrated to 120 or 240 ohms



When Match PMOS leg is calibrated to 120 or 240 ohms

Figure 11 — PMOS Calibration

3 Additional Background Information (cont'd)

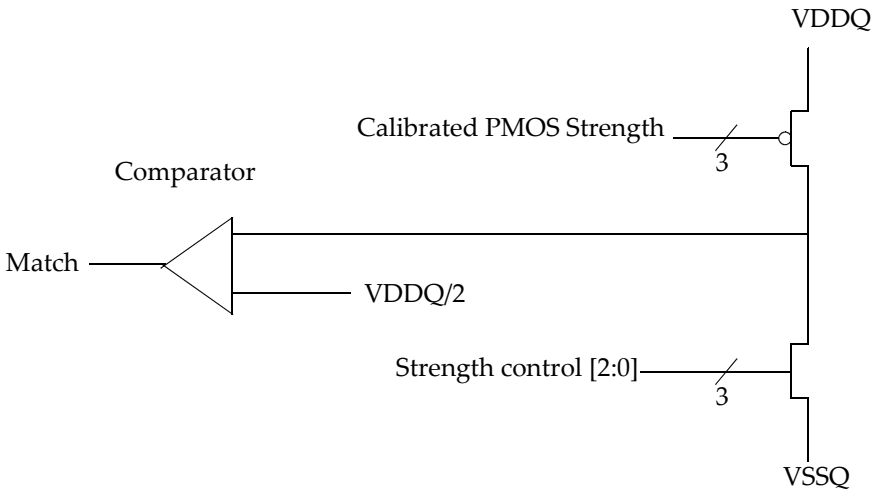


Figure 12 — NMOS Calibration

Annex A — (Informative) Difference between JESD8-20A and JESD8-20

This clause briefly describes most of the changes made to entries that appear in this standard, JESD8-20A, compared to its predecessor, JESD8-20 (December 2006).

Clause	Description of Change
1	Added GDDR5
2	Updated Table 1, Table 2, and table 3 for GDDR5
2	Added new Figure 3, Figure 4, Figure 5, Figure 6, and Figure 7
2	Removed Note 1 from Table 4
3	Renumbered old Figures 3-7, Figures 8-12
3	Renamed Table 5
3	Added Table 6

Annex B — (Informative) Difference between JESD8-20A.01 and JESD8-20A

This clause briefly describes most of the changes made to entries that appear in this standard, JESD8-20A.01, compared to its predecessor, JESD8-20A (October 2009).

B.1 Added Table of Contents, List of Figures, and List of Tables

B.2 Editorial change to replace every instance of “master” with “initiator” and “slave” with “target” as follows

- Clause 3
- Figure numbers 8, 9, and 10
- Table numbers 1, 5, and 6

B.3 Added back pages

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