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Procedure for Reliability Characterization of Metal-Insulator-Metal Capacitors

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PROCEDURE FOR RELIABILITY CHARACTERIZATION OF METAL-INSULATOR-METAL CAPACITORS

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Foreword

The intent of this procedure is to provide comprehensive recommendations for assessing all aspects of Reliability (Intrinsic, Defect and Thermo-mechanical) pertinent to MIM (Metal-Insulator-Metal) Capacitor that are offered as technology features on process nodes. The procedure describes the testing methods such as Constant Voltage Stress for getting insights into conduction mechanisms and TDDB (Time Dependent Dielectric Breakdown) physics.

This procedure will also comprehend potential parametric shifts as part of intrinsic reliability. VRDB (Voltage Ramp Dielectric Breakdown) test is also described as a tool to estimate 'extrinsic'/defect reliability and as a quick turn method for gaining insights into intrinsic reliability. Furthermore, conventional temperature cycle stresses (TCB, TCC) and HAST can be used to characterize the thermo-mechanical and environmental reliability of MIM Capacitors.

PROCEDURE FOR RELIABILITY CHARACTERIZATION OF METAL-INSULATOR-METAL CAPACITORS

(From JEDEC Board Ballot JCB-24-04, formulated under the cognizance of the JC-14.2 Subcommittee on Wafer-Level Reliability.)

1 Scope

This publication provides a complete framework and defines the standards for achieving Reliability certification and qualification of on-chip MIM capacitors or Trench capacitors (MIS Capacitor). The test methods and Merit definitions comprehend the full gamut of products across all market segments with respect to use condition and EOL targets. The scope covers all applications of MIMCAP, such as de-coupling capacitor and signal capacitance usage.

2 Normative References

JEP001, *Foundry Process Qualification Guidelines – Backend of Line*

JEP159A, *Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity*.

3 Terms and Definitions

For the purpose of this publication, the following terms and definitions apply.

3.1 Abbreviations

MIM: Metal Insulator Metal
CVS: Constant Voltage Stress
DUT: Device Under Test
TDDB: Time Dependent Dielectric Breakdown
VRDB: Voltage Ramp Dielectric Breakdown
ESR: Equivalent Series Resistance
DCAP: Decoupling Capacitor
TTF: Time to Fail
TCB: Temperature Condition B
TCC: Temperature Condition C
HAST: Highly Accelerated Stress Test
RF: Radio Frequency
FOM: Figure of Merit

3.2 Symbols and Definitions

I_{meas} (A): Measured current

I_{comp} (A): Maximum current/compliance current limit for a particular test

V_{stress} (V): DUT stress voltage

V_{use} (V)/V_{nom}(V): Use or Nominal voltage for a specific technology node; V_{nom} should include power supply tolerance (Range 5% to 10%)

C (F): Measured DUT capacitance

E_a (eV): Thermal activation energy

4 Technical Requirements

4.1 Test Structures

Test structures for MIM Capacitor can be a 2-plate or a multi-plate capacitor with dedicated bussing connection to each individual plate. The structure should have enough routing resources (lines/vias) to ensure that the voltage droop is minimal. Additional care should be taken with respect to routing if the MIM Capacitor is used for signal applications so as to minimize the resistive loss [ESR]. It is recommended to use RF pads for signal applications.

For intrinsic assessments, a minimum area of 10,000 μm^2 capacitor area is recommended (or representative mission profile "area" of the product). In addition, area skews spanning at least 2 orders of magnitude (either higher or lower than 10,000 μm^2) should be considered for extraction of TDDB dependence on area.

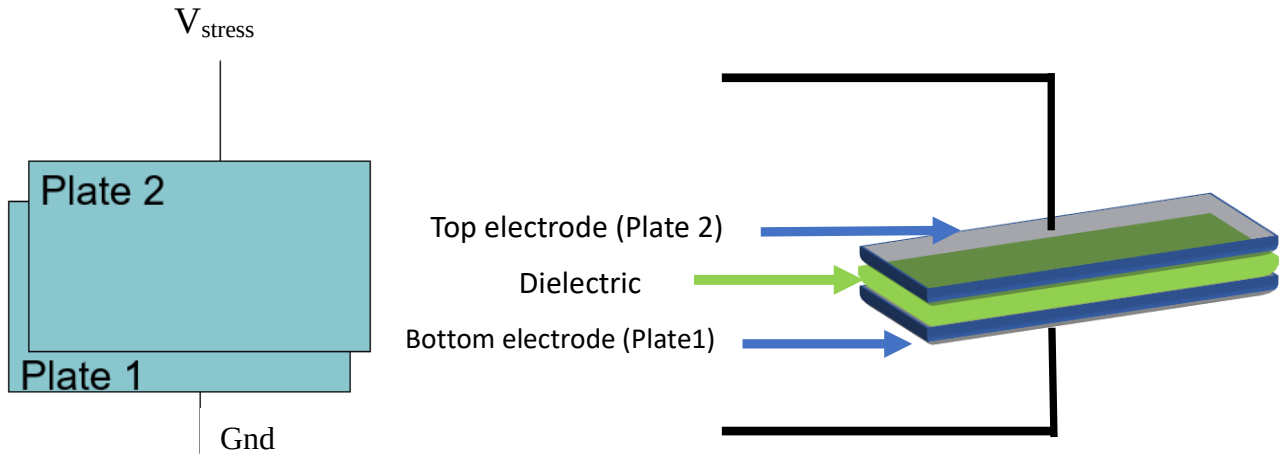


Fig.1(a) Fig.1(b)

Figure 1 — Top View and Cross-sectional View of Metal-Insulator-Metal Capacitor

A larger area structure of at least 25,000 μm^2 is recommended to be used for estimation of the 'extrinsic' / 'defect' reliability of the structure.

5 Intrinsic Reliability

5.1 Constant Voltage Stress

This section describes for method for applying Constant Voltage Stress to a MIM Capacitor for assessing the intrinsic/wear-out reliability of the capacitor. The goal of this test is to characterize the Time to Fail, Voltage acceleration, Temperature acceleration, Area scaling parameter, and Weibull beta, parametric shifts in capacitance. The test can be performed at wafer level or at a package level.

5.1.1 Stress and Measurement Setup

1) Measure time-zero leakage for all MIM Capacitors at V_{nom} condition for the technology.
2) Screen out 'extrinsic' or high leakage capacitors (high leakage is defined as DUTs with >10X leakage from expected values).
3) Apply Constant Voltage Stress V_{stress} at a fixed temperature and monitor leakage at V_{nom} or V_{stress} at regular intervals (minimum 3 readouts per decade). In-situ or continuous leakage monitoring can also be used as an alternative option.
4) Time to fail (TTF) is defined as the interval between which the measured leakage at V_{nom} exceeds a pre-defined fail criteria (recommend >10X as the fail criteria relative to t = 0 leakage or a value based on product use conditions). A sudden decrease in current is also possible and is a symptom of 'open' circuit failure due to transient current causing bussing fail.
5) The Time to Fail for each DUT should be recorded to estimate the probability of failure.

5.1.2 Data Extraction

1) Time to Fail (TTF) data from multiple DUTs should be fitted with a Weibull fit since the dielectric breakdown phenomenon is based on 'weakest' link percolation model. Both alpha (63.2% fail percent) and beta (slope of the distribution) should be extracted. A Weibull beta value of <1 may suggest convolution of intrinsic distribution with defect tails and should be further investigated. The failure probability for a Weibull distribution is:

$$F(t) = 1-\exp[-(t/\alpha)^{\beta}] \quad (1)$$

where α = Scale parameter, and β = Shape parameter or slope.

2) Acceleration parameter extraction:

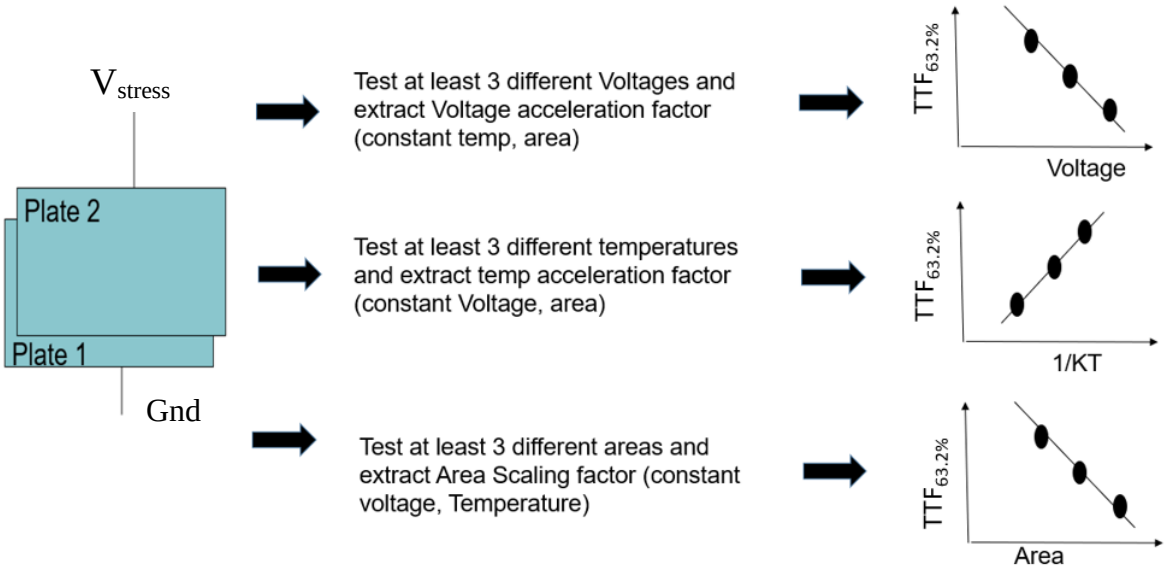
   a) Voltage Acceleration Parameter – This is extracted by testing the MIM Capacitor at at least 3 different voltages and fitting either an 'exponential' or 'power law' or 'Sqrt E' or another suitable model to TTF as shown in Figure 2. Other variables such as temperature and area should be kept constant.

   b) Temperature Acceleration Parameter – This is extracted by testing the MIM Capacitor at at least 3 different temperatures and fitting an Arrhenius model to TTF as shown in Figure 2. Other variables such as voltage and area should be kept constant.

5.1.2 Data Extraction (cont'd)

c) Area Scaling Parameter – This is extracted by testing the MIM capacitors at at least 3 different areas (minimum of 2 orders of magnitude delta in areas) and fitting a 'power' model to TTF as shown in Figure 2. Additional checks may be needed to ensure that Weibull beta is inversely correlated to Area Scaling Parameter emphasizing relevance of Poisson statistics. If the Weibull beta is statistically different (p-value < 0.05) for structures with different area, then follow up investigation is needed to understand the cause for the discrepant behavior. Parasitic breakdown paths, bussing related fails can contribute to non-monotonic TTF as a function of area.

d) It is also feasible to combine and optimize the above tests to extract acceleration parameters concurrently.



NOTE Acceleration factor can also be known as acceleration parameter for multiple conditions.

Figure 2 — Proposed Methodology for Extraction of Intrinsic TDDB Acceleration Model Parameters

5.1.2 Data Extraction (cont'd)

Table 1 — Minimum Sampling Requirements

Item	Minimum Samples	Recommended Stress Conditions
TTF (hrs)	Minimum of 3 wafers from multiple lots, 20 die per wafer.	Lowest stress voltage that yields failures in a reasonable time.
Weibull beta	Minimum of 3 wafers from multiple lots, 20 die per wafer or all die per wafer.	Lowest stress voltage that yields failures in a reasonable time. Data from multiple wafers can be pooled if the variation from wafer to wafer is minimal.
Voltage Acceleration Parameter	Minimum of 3 wafers from multiple lots, 20 die per Stress Voltage/wafer.	Stress voltages should be selected to ensure failures in reasonable time. Both wafer level and package level stresses can be employed to extract Voltage Acceleration Parameter. It is recommended to collect $TTF_{63.2\%}$ data spanning 2 orders of magnitude to ensure reasonable confidence in acceleration parameter extraction.
Temperature Acceleration Parameter [eV]	Minimum of 3 wafers from multiple lots, 20 die per Stress Temperature/wafer.	For e.g, 60 ^{o}C, 90 ^{o}C, 120 ^{o}C. Please ensure the temperature upper range envelopes the product use condition.
Area Scaling Parameter	Minimum of 3 wafers from multiple lots, 20 die per MIMCAP Area/wafer.	1X, 10X, 100X area sized structures.

5.2 TDDB Model Dependence on Voltage

Based on literature [1], several potential models can be used for TDDB Model dependence on voltage ('E' Model, 'Power Law' Model, 'SQRT E', and other models) and corresponding extrapolation to use conditions. It is highly recommended to collect low voltage stress conditions data at package level on the certifiable process with sufficient statistics to build confidence in extraction of Voltage Acceleration Parameter (a typical stress of 3 months to 6 months is recommended) and use Loglikelihood criteria to discern the applicable acceleration models.

5.2.1 Parametric Shift Characterization

For both decoupling and signal MIM operation, it is recommended that any parametric (capacitance) drift as a function of bias and temperature is well understood and characterized.

The key attributes that are critical for MIM usage as a capacitor are voltage linearity and temperature linearity coefficients.

MIM inherently exhibits non-linear characteristics as a function of voltage due to the material properties of the electrode (work function, etc.) and the dielectric as shown in Figure 3.

5.2.1 Parametric Shift Characterization (cont'd)

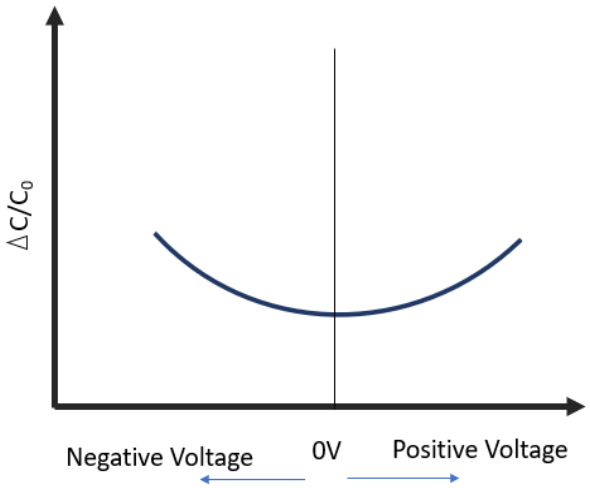


Figure 3 — Capacitance vs. Voltage Characteristics of MIM Capacitor

$$C(V) = C0\ (\alpha V^2 + \beta V + 1) \quad (2)$$

where α = Quadratic voltage capacitance coefficient, β = Linear voltage capacitance coefficient, and C0 = Zero bias capacitance.

Ideally, both quadratic and linear voltage capacitance should be low for signal cap usage.

The presence of trapped charges in MIM dielectrics impacts the dielectric polarization of the capacitor and thereby leads to change in capacitance. A significant change in capacitance due to aging might lead to circuit instability (as shown in Figure 4) for Analog/Mixed signal designs and hence could be reported as part of technology certification and qualification.

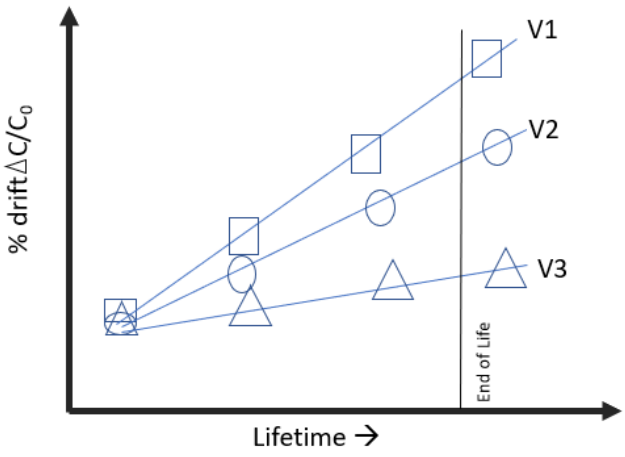


Figure 4 — Capacitance vs. Voltage Characteristics of MIM Capacitor with Electrical Stress

5.2.2 Stress and Measurement Setup

1) Measure time-zero capacitance for all MIM Capacitors at V_{nom} condition for the technology.
2) Apply Constant Voltage Stress V_{stress} at a fixed temperature and measure capacitance at V_{nom} or V_{stress} at regular intervals (minimum 3 readouts per decade). Please be cognizant of the fact that the measured capacitance is dependent on V_{stress} or V_{nom} due to the potential for de-trapping at lower voltages. V_{nom} is recommended to be the default condition for capacitance measurement.
    a) Record the capacitance values at each readout and extrapolate the drift to technology Figure of Merit lifetime and temperature.
    b) Recommended sample size of 3 wafers from multiple lots, 20 DUTs per wafer.

5.3 AC TDDB

There have been very few studies related to TDDB behavior of MIMCAPs with AC stress. It is recommended to understand the differences between DC and AC stresses to ensure that the MIMCAP's reliability is representative of the product use condition.

Under AC stress, the lifetime of a dielectric is expected to be higher compared to a DC stress due to partial recovery and de-trapping of charges. However, AC stress might result in worse TDDB than DC. One of the leading models for this discrepancy is due to the presence of oxygen vacancies in Hi-K dielectrics such as HfO_2. During stress, V_O^{2+} are created as a result of the injection of energetic electrons. Above a critical defect (V_O^{2+}) density, a conduction path is formed in between electrodes that leads to a breakdown event [5].

Figure 5a and Figure 5b show the typical stress/measurement waveform for assessing AC Reliability of a MIM Capacitor. Additional care should be taken to ensure that the measurement time is not too long to allow full recovery of trapped charges.

For AC TDDB stress at frequencies >1MHz, RF pads must be used to ensure minimal attenuation of the unipolar or bi-polar pulse.

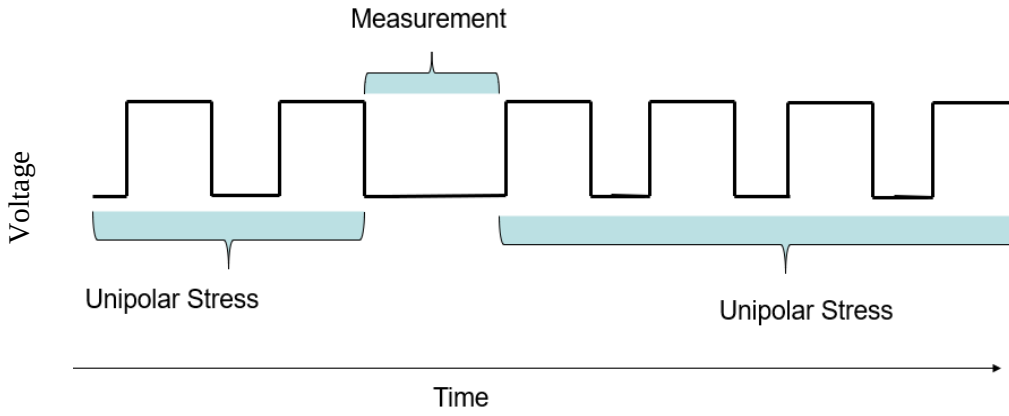


Figure 5a. Unipolar stress and measurement setup for AC TDDB on MIMCAP

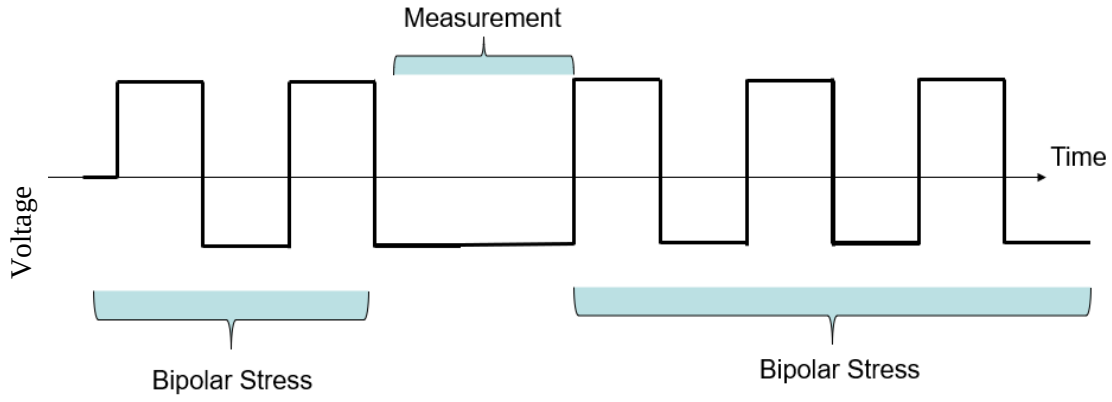


Figure 5b. Bi-polar stress and measurement setup for AC TDDB on MIMCAP

Figure 5 — Stress and Measurement Setup for AC TDDB on MIMCAP

5.3 AC TDDB (cont'd)

Literature studies [4] have indicated that TDDB Reliability may get worse at higher frequencies due to local power dissipation. Oxygen vacancies generation is a thermally activated process and hence with increase in local power at higher frequencies, the lifetime is significantly reduced as shown in Figure 6.

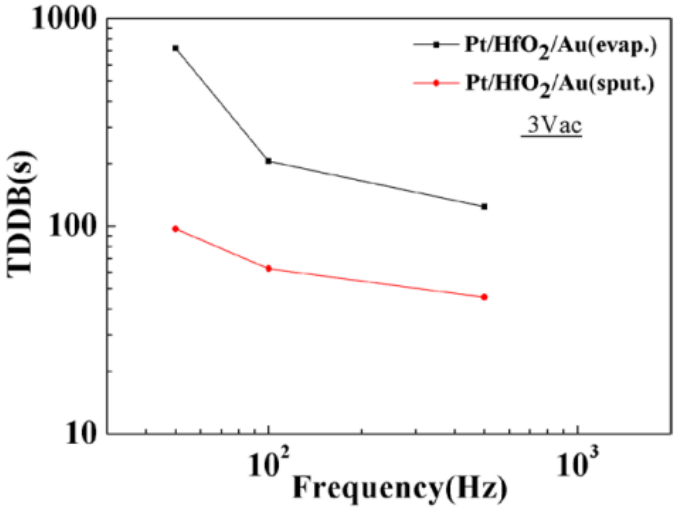


Figure 6 — TDDB Degradation as a Function of Stress Frequency

6 Defect Reliability

This section describes a method for characterizing the defect reliability aspect of MIM Capacitors. The intent of this test is to align on a standard methodology for defect density estimations, sample size requirements and report out a Reliability based defect density value for the technology. This test can be performed at wafer level or at package level

6.1 Test Structures

For assessing defect Reliability, the test structure area is recommended to be minimum of 25,000 μm^2 [0.0025 cm^2]. This is to ensure reasonable detectability for identifying process induced defect tails. Figure 7 shows the minimum resolvable defect density assuming Poisson statistics (other models can also be used to extract DD).

$$\text{Defect Density} = -1/A*\text{Ln}(Tg/TT) \quad (3)$$

where A = Area of the test structure, Tg = # of good samples, and TT = Total # of samples tested.

For extrinsic reliability characterization, both ramped voltage/current stress or Constant Voltage Stress can be used. Failure is defined as a sudden jump in leakage (>10X) compared to previous readout or if the current reaches a pre-defined threshold. It is recommended that as part of qualification report, the impact of extrinsic reliability is documented. Additional screening methods can be used to ensure that the impact to the customers is minimized. The goal for defect density is recommended to be <1 defect/cm^2 and can be tighter based on the MIMCAP mission profile and application.

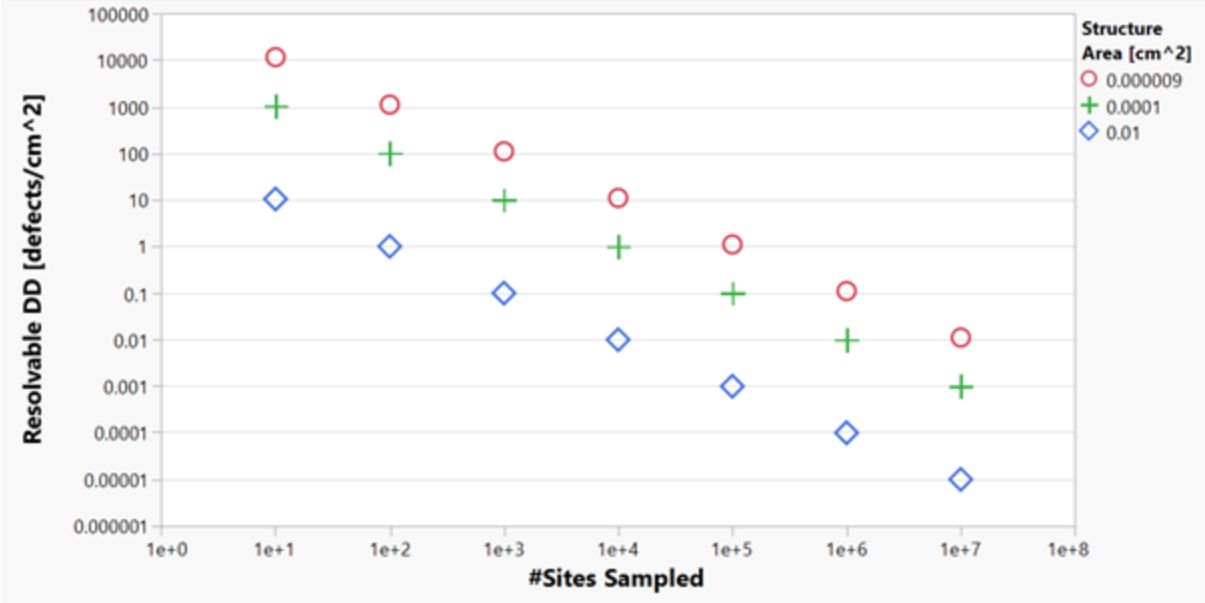


Figure 7 — Resolvable Defect Density as a Function of Test Structure Area and Total Number of Sampled Sites

6.1 Test Structures (cont'd)

An "extrinsic" defect is defined as a population of die with declining fail rate characteristics and typically fail within the useful life of the product. It is recommended that Ramped Voltage Stress (RVS) technique be used to identify extrinsic/defect tails. The success criteria for demarcation of defect tails are based on the equation below [5]. Note that TBD and VBD are applicable to the same test structure.

$$\mathrm{TBD} = \frac{\exp\left(\gamma * (\mathrm{VBD} - \mathrm{Vref})\right)}{\gamma * \mathrm{RR}} \tag{4}$$

where TBD = Failure time, γ = Voltage acceleration parameter, VBD = Breakdown voltage, Vref = Reference voltage, and RR = Ramp Rate of ramped voltage stress.

It is recommended that a lifetime based on product use conditions be used to define the fail criteria for defect density calculations. For example, Figure 8 shows a synthesized VBD distribution with 'population 1' and 'population 2'. Assuming a product mission profile of 10 years, the expected lifetime of population 1 is <10 years by applying measured TDDB parameters to equation 4, and hence is considered as a defect tail. 'Population 2' is the intrinsic part of the distribution and is expected to meet the full Figure of Merit lifetime.

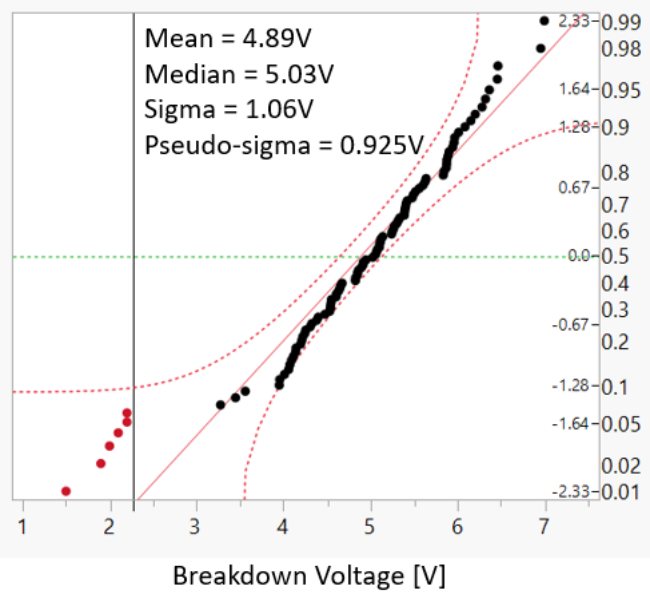


Figure 8 — Breakdown Voltage Plot Showing Intrinsic and Extrinsic Population

7 Thermo-mechanical Reliability

This section describes a method for characterizing the environmental and thermo-mechanical reliability aspect of MIM Capacitors. This test can be performed at wafer level or at package level and is aligned with JESD22 and JESD47 specs.

Incorporation of new metallurgies and dielectrics to an interconnect stack increases the risk for thermo-mechanical reliability. Both low-K dielectric and Hi-K dielectrics are susceptible to environmental related reliability risks as such as moisture induced fails, or thermal cycling related delamination effects. To ensure that MIM capacitors are robust for intrinsic Thermo-mechanical reliability, it is recommended that the following data is being used to certify the technology.

Table 2 — Recommended Thermo-mechanical Reliability Stresses for Qualification of MIM Capacitors

Item	Unit/Wafer Level	Reliability Test Specifications	# of Units	Success Criteria	Comments
uHAST	Unit level	110 °C temperature 85% Relative Humidity 264 hrs	3 x 25	0/75 units	To assess impact of hermeticity on MIM capacitors
Temp Cycle [use appropriate condition]	Unit level or Wafer level	e.g., TCB – 700 cycles Refer to JESD47 for additional details	3 x 25	0/75 units	To assess impact of thermal cycling/CTE mismatch related fail modes. NOTE Wafer level will not capture interactions due to different package types.

8 Plasma Process-induced Damage (PID)

Semiconductor processing involves etch and deposition techniques that uses plasma-based processes to achieve a desired patterning scheme. However, an unintended implication of plasma-based approaches is the potential charging of various dielectrics in the Front-End-Of-Line (FEOL), Middle-of-Line (MOL) and Back-End-Of-Line (BEOL). The manifestation of plasma-induced damage (PID) leads to dielectric damage in the form of degraded leakage and TDDB in addition to threshold voltage shifts in transistors as shown in Figure 9 [6].

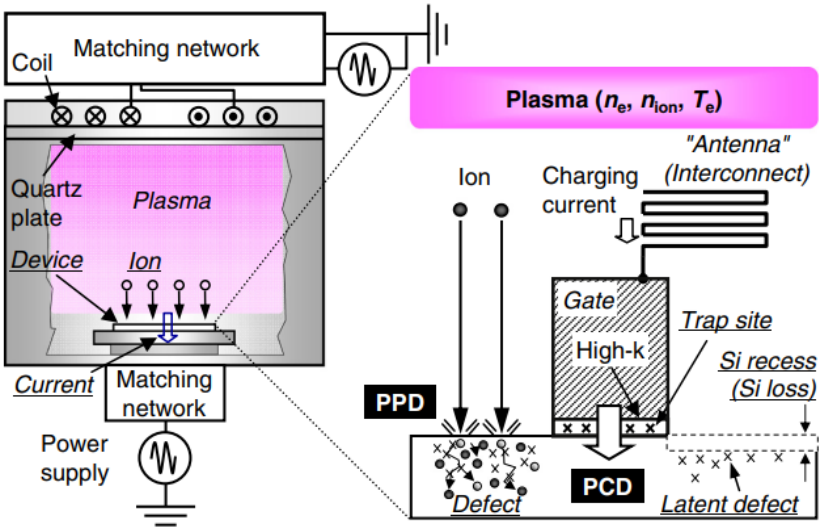


Figure 9 — Example of Devices Being Damaged by Bombardment of High-energy Ions and Associated Impact to High-k Dielectric Films

Some of the options to mitigate risk due to PID is to either limit the Antenna Ratio or add PID protection devices such as diodes to dissipate accumulated charges developed during processing.

Antenna Ratio is defined as the area of the metal (antenna) to the area of the MIM dielectric, as shown in Figure 10.

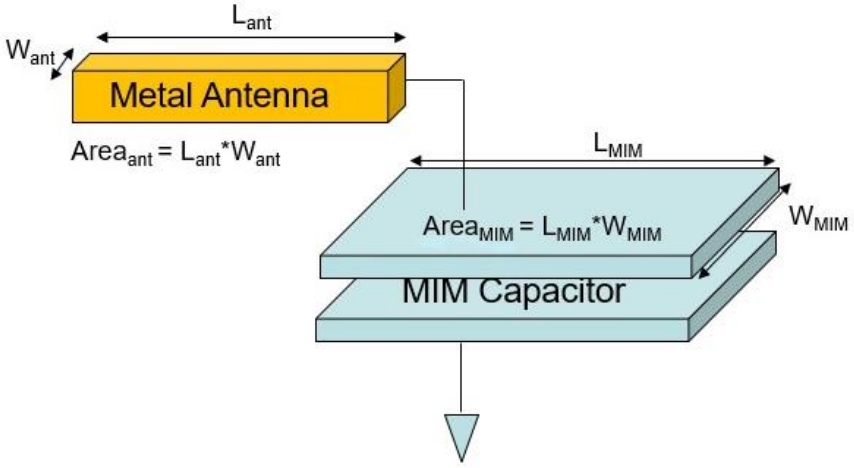
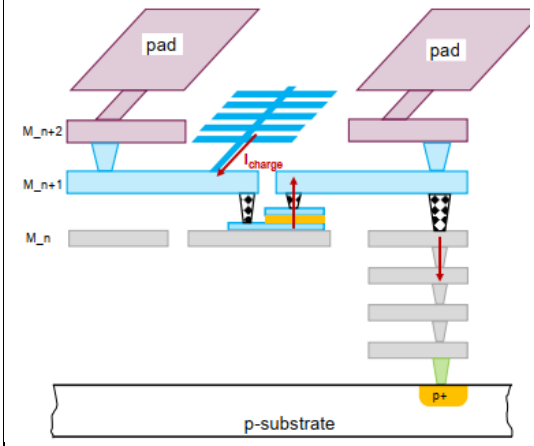
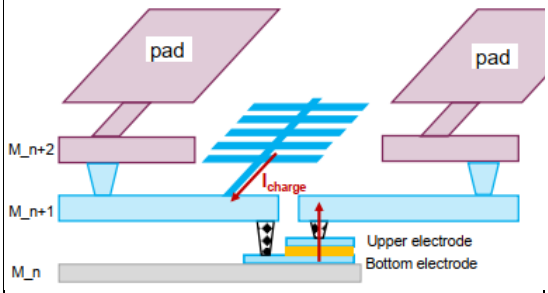
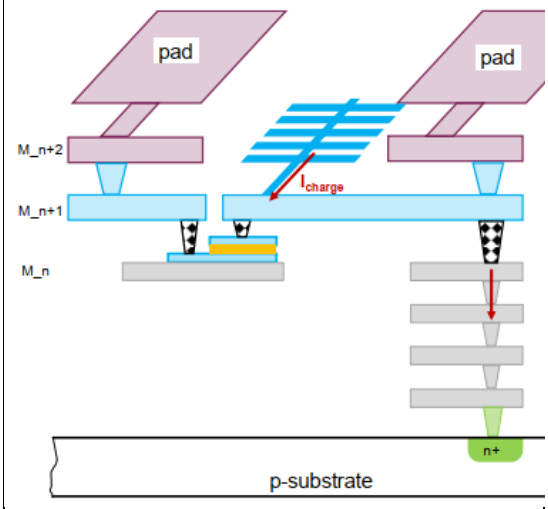


Figure 10 — Typical Antenna Connection to MIM Capacitor

8 Plasma-induced Damage PID (cont'd)

Table 3 — Recommended Structures for Assessing PID Risk on MIM Dielectrics

Structure	Objective	Structure Skew	
Reference MIM structure. [Negative Control]	Assess the impact of Charging.	Max Area Antenna, Min Area Victim with one side of capacitor grounded to ensure conduction through the capacitor.	
Reference MIM structure. [Positive Control]	Golden structure that is less susceptible to PID damage.	Min Area Antenna, Min Area Victim with both electrodes floating.	
Antenna Ratio Skews. [No PID protection]	Identify maximum Antenna Ratio that can be supported without PID protection.	Antenna Area Skew = Min[1X], Mid[10X], Max[100X]. MIM Area Skew = Min[1X], Mid[10X], Max[100X]. Permutation of Antenna Area and MIM Area structures can be used to assess the Antenna Ratio that can be supported without any PID protection.	
Antenna Ratio Skews. [With PID protection]	Identify Antenna Ratios that require PID protection.	Antenna Area = Max[100X]. MIM Area Skew = Min[1X], Mid[10X], Max[100X]. PID Protection Skew (Diode) = Min[1X], Mid[10X], Max[100X]. Permutation of Antenna ratio and protection device area can be used to assess the Antenna Ratio that requires PID protection. In the figure, the charges during processing are discharged through the n-p diode.	
Figures Courtesy: Andreas Martin			

8.1 Stress and Measurement Setup

1) Measure time-zero leakage and capacitance for all MIM Capacitors at V_{nom} condition for the technology.
2) Apply Ramped Voltage Stress or Constant Voltage Stress to DUTs and measure the leakage current, and capacitance at regular intervals. Recommended sample size of 3 wafers from multiple lots with sampling representative of spatial component within wafer.

Success Criteria for passing PID is to ensure that there are no tail failures in leakage, capacitance drift, TTF or VBD on DUTs (either by limiting the Antenna ratio for unprotected devices or by adding protection devices such as diodes). The definition of tail failures should be set based on the mission profile of the products that the technology caters to.

Annex A (Informative) Bibliography

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