# STANDARD PROCEDURES AND PRACTICES

**Number:** SPP-002

**Subject:** Pin #1 Mark Function and Location

**Effective Date: 20 June 1991**

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## BACKGROUND

Requirements for package marking for pin #1 identification have been defined ambiguously on certain registered outlines for high leadcount quad flatpacks. These outlines allow optional locations for pin #1 markings on either a corner lead or a center lead on one side of the package. The markings in these locations have been used both as pin #1 designators and as package orientation features and have been confused with various physical features such as notches or chamfers that are intended for mechanical orientation only. This ambiguity does not exist in other quad peripheral-leaded package standards such as those for LCCs and PLCCs with .050" lead pitches.

## PRACTICE

There shall be a mark, called the Pin #1 identifier (ID) mark, on each subject package. This mark shall be contained in an area located at one corner of the subject packages. Pin #1 shall then be located directly adjacent to, and counterclockwise from, this index corner when the package is viewed as-mounted on a PC board or other substrate.

## APPLICATION INFORMATION

This policy consists of two parts, nomenclature and location definition, and applies to packages with peripherally located terminal points (of either a leadless or leaded variety) on four sides with lead or terminal pitches $\leq .025"$ or $\leq 0.65$ mm.

All package outline drawings shall show a Pin #1 ID mark. This mark shall be shown located in an area at a corner of the package body adjacent to the actual pin #1 location and on the side opposite to the seating plane (viewing or top side).

Current drawings show an "Index Area"; on new drawings this area will be called "Pin #1 Mark Area" or "Index and Pin #1 Mark Area". The index area is that area of the package having a unique mechanical feature, but the Pin #1 Mark is located in the immediate vicinity of the actual pin #1.

Many of the subject package drawings will show a chamfered or notched corner signifying an index corner that is also the pin #1 corner (other mechanical features are used where necessary). Pin #1 is then located directly adjacent to, and counterclockwise from, this index corner when the package is viewed as-mounted on a PC board (See accompanying figure). This condition is in concurrence with one of the optional conventions for leadless package numbering as stated in the *JEDEC Leadless Package Terminal Numbering Convention* section of JEP-95, but runs counter to the practice used for many leaded and leadless chip carriers with .050" pitch. In the latter cases, the lead numbering followed the die-pad numbering scheme historically used with dual-in-line packages.

All new outline drawings will be required to follow this policy. Existing outline drawings thatallow alternative Pin #1 ID areas will not be affected, but new variations will not be added to these outlines

until such time as the optional areas are removed through the customary JC-11 balloting process. New variations of an existing outline configuration will be required to follow the new policy, however, and will, when approved for publication, be published under a separate outline number unless the parent outline has been brought into conformance with this policy. Reference to the parent outline will be included in this new outline publication.