JEDEC SPECIFICATION

JES2

Transistor, Gallium Arsenide Power Fet, Generic Specification

JES2

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ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT

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TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION

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TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION

(From JEDEC JCB-89-32 Council Ballot, formulated under the cognizance of JC-50, Committee on Gallium Arsenide)

1. SCOPE

1.1 General

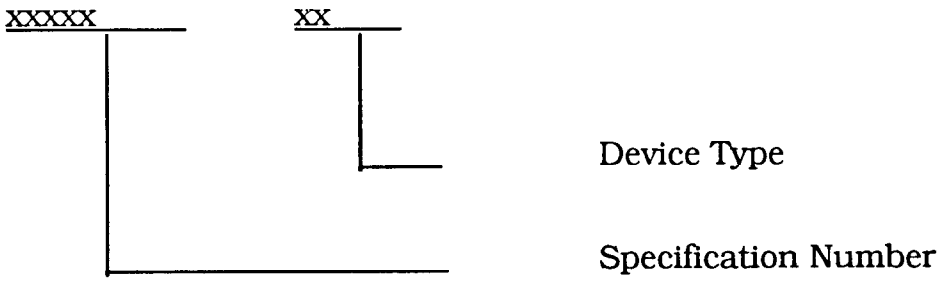
This specification establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also known as MESFETs) designed for use in high-reliability space applications such as spacecraft communications transmitters. The specification identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance inspection tests pertinent to power GaAs FETs. For the purposes of this specification, a power GaAs FET is defined as one used as an RF amplifier which is operated in compression. The specification is intended to be applicable to packaged and chip-carrier parts; consequently portions of the specification may not be applicable to unpackaged and unmounted chips.

The intent of this specification is to serve as a guideline for transistor manufacturers and users (purchasers) to use in the development of their own specifications for power GaAs FETs for applications requiring high reliability. The specific applications and device designs will define the values for parameters left undefined in this specification.

It is expected that the manufacturer, prior to acceptance of this specification, will have generated reliability data which indicate to the purchaser that they can fulfill the reliability goals of the specification and can identify the most probable failure mechanism.

1.2 Part Number

The complete part number shall be as follows:



1.2.1 Device Type and Package or Chip-Carrier Outline

The device type and package or chip-carrier outline shall be as follows:

Device Type	Package or Chip-Carrier Outline
xx	Figure 1

1.3 Absolute Maximum Ratings (see MIL-S-19500, Appendix A, Paragraph 20.1)

The device shall have the maximum rating at $T_A = 25 \pm 3^{\circ}C$ unless otherwise specified.

PARAMETER	SYMBOL	VALUE	UNIT
Minimum breakdown voltage drain to source	$V_{(BR)DSO}$		volts
Minimum breakdown voltage gate to source	$V_{(BR)GSO}$		volts
Minimum breakdown voltage gate to drain	$V_{(BR)GDO}$		volts
Maximum continuous drain current	I_{DM}		amps
Maximum power dissipation at 25°C base[1,2]	P_T		watts
Maximum thermal resistance (channel to base)[1]	R_{CC}		°C/W
Storage temperature range	T_{STG}	-65 to 175	°C
Operating temperature range (channel)[3]	T_{OP}	-65 to 175	°C
Maximum RF input power	P_{INMAX}		watts or dBm
Maximum gate current range under RF operation	I_{GMAX}, I_{GMIN}		mA

Notes:

1. The word "base" called out in this specification refers to the mounting fixture's surface. This rating is for a channel temperature of 175°C.

2. The total power dissipation shall be derated linearly from P_T watts at 25°C base temperature to 0 watts at 175°C base temperature.

3. The operating channel temperature will directly affect the MESFET MTTF (Mean Time To Failure). For maximum life, it is recommended that the channel temperature be maintained at the lowest possible level.

1.4 Handling Precautions

This device may be sensitive to electrostatic discharge (ESD), and proper care (see MIL-STD-1547) in packaging, handling, testing, and use must be exercised to prevent either immediate failure or degradation and reduced life of the device due to this cause. The leads (e.g., gate or drain) of packaged devices can be damaged by bending stress. Therefore, exercise care in handling and test; do not handle packaged devices by their leads. Chip-carrier devices are extremely vulnerable to contamination and physical damage to the chip metallization and

wire or ribbon bonds. Consequently, do not handle the devices without proper tools or open their containers outside an appropriate clean area.

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. In case of conflict the requirements of this specification shall take precedence. Date of issue shall be the latest date prior to start of contract unless otherwise specified.

MILITARY SPECIFICATIONS	
MIL-S-19491	Semiconductor, Devices, Packaging of
MIL-S-19500	Semiconductor Devices, General Specification for
MIL-G-45204	Gold Plating, Electro Deposited
MIL-M-38510	Microcircuits, General Specification for
MILITARY STANDARDS	
MIL-STD-129	Marking for Shipment and Storage
MIL-STD-202	Test Methods for Electronic and Electrical Component Parts
MIL-STD-750	Test Methods for Semiconductor Devices
MIL-STD-883	Test Methods for Microelectronic Devices
MIL-STD-1276	Leads; Weldable for Electronic Component Parts
MIL-STD-1285	Marking of Electrical and Electronic Parts
MIL-STD-1547	Parts, Materials, and Processes for Space and Launch Vehicles
MIL-STD-45662	Calibration Systems Requirements
APPENDICES	
1	Test Procedure for RF Power, Gain, Efficiency and Impedance

3. REQUIREMENTS

3.1 General
Devices supplied to this specification shall meet the requirements as specified herein. Depending on the application the device may be mounted in hermetic packages or unsealed chip-carriers.

3.2 Design, Construction, and Physical Dimensions
The design, construction, and physical dimensions shall be as specified herein.

3.2.1 Package (Chip Carrier) Outline
The package (chip carrier) outline shall be as specified in Figure 1.

3.2.2 Hermetic Package
The package design must have been qualified as hermetic for space applications, e.g., metal-ceramic construction is qualified.

3.2.3 Chip Carriers
Chip carriers may be required for mounting higher frequency devices. Such carriers are intended for use only in hermetically sealed circuits.

3.2.3.1 Chip Carrier Construction
Chip carriers may be constructed of a combination of metallized ceramic and metal to provide a mounting surface for the device and a thermal path for heat dissipation. Metal parts and metallized surfaces shall be gold plated (50 to 100 micro-inches) over nickel plate per MIL-G-45204.

3.3 Materials

3.3.1 Substrate Quality
Gallium arsenide substrates used in the production of the devices shall meet or exceed a minimum specification for quality. The specification on substrate quality prepared by the manufacturer, and any proposed change to the specification, must be approved by the purchaser. The results of tests on the substrates shall be available for examination by the purchaser.

3.3.2 External Metal Surfaces
External metal surfaces shall be plated with 50 to 100 microinches of gold except that ends of leads may be unplated.

3.3.3 Magnetic Materials (application related guideline)
Minimal use of magnetic materials in the construction of the GaAs FET should be considered to prevent magnetic interference with surrounding experiments and circuits.

3.3.4 Matching or Combining Circuit Components
The microstrip substrates and lumped element capacitors or resistors used in the production of matching or combining circuits internal to the device package or chip carrier shall meet or exceed a minimum specification for quality. These

specifications, prepared by the manufacturer, and any proposed change to the specifications must be approved by the purchaser. The results of tests on the subject parts shall be available for examination by the purchaser. Any metallization where die bonding or wire bonding is to be performed on the substrates or lumped element capacitors shall be gold. Any metal wires, ribbons or foils used for inductances or circuit interconnection shall be gold.

3.3.5 Fungus Resistance
External materials used in the construction of the device shall be non-nutrient to fungus.

3.4 Wafer Lot Control
All parts supplied to the requirements of this specification shall be: (1) from a single wafer, or (2) from wafers from the same wafer lot, or (3) from a minimum number of lots (in the order of preference shown). Each wafer lot shall be assigned a unique identifier that provides traceability to all processing steps. If the wafer lot consists of more than one wafer, the wafers within the lot shall be processed in a manner that requires every wafer to be subjected to each and every process step as a group through metal and dielectric deposition, etching, and annealing processes. A lot shall consist of devices originating from a given group of wafers from a common ingot and processed (under equivalent expitaxial or ion implantation conditions) in the same epitaxial growth or ion implantation run.

3.4.1 Wafer Acceptance Inspection
Each wafer designated for devices supplied to this specification shall conform to the requirements of paragraph 4.4.

3.5 Surface Passivation or Protection
The device shall be glassivated to preclude particles undetected by the PIND test from causing an internal short.

3.6 Surface Metallization
The top surface of the die metallization shall be gold with gold wire, ribbon, or foil attachments between the die and package or internal circuitry terminals. This does not preclude the use of aluminum for the gate metallization if the manufacturer can demonstrate the quality, uniformity, and reliability of their barrier metal system per MIL-STD-1547, Section 1400.

3.7 Electrical Characteristics and Ratings

3.7.1 Ratings
The ratings shall be as specified in paragraph 1.3.

3.7.2 Electrical Characteristics
The electrical characteristics shall be as specified in Table I. The RF electrical characteristics are to be measured as indicated in Appendix 1. Unless otherwise noted, the mounting fixture temperature shall be TBD°C±3°C.

3.8 Process Conditioning, Testing and Screening
All devices shall be subjected to the process-conditioning, testing, and screening as specified in Table II.

3.9 Qualification
Devices supplied to this specification shall be a product which has been tested and passed the qualification tests specified herein.

3.10 Lot Quality Conformance
Devices supplied to this specification shall be a product which has passed lot quality conformance as specified in Table V.

3.11 Traceability
A device supplied to this specification shall be traceable to a given wafer, wafer position in a given implantation or epitaxial run and wafer position in a given crystal ingot. The device package or chip carrier shall also be traceable through the various processing steps back to the original package production lot. Device lots shall conform to the requirements of paragraph 4.3.

3.12 Serialization
Each item shall be assigned a serial number that identifies the wafer from which the part was obtained and uniquely identifies the part from all other parts assembled within the lot.

3.13 Marking
Marking shall be in accordance with MIL-STD-1285 and shall consist of the following items (where size or other design considerations will not allow full marking of part, marking for each part shall be in accordance with the following precedence):

a. Part Number

b. Serial Number/Lot Code

c. Date Code

d. Manufacturer's Name or Symbol

Configuration or polarity of leads must always be indicated either by package marking or variation in lead geometry for the various leads.

3.13.1 Marking Permanence
Marking shall remain legible after brushing when the device is subjected to tests of MIL-STD-202, Method 215.

3.13.2 Date Code
All parts supplied to the requirements of this specification on a single purchase order shall be from a minimum number of lots and date codes. Each assembly lot shall be assigned a lot date code identifying the year and the week of the

year in which assembly of the part was completed (this is usually the assembly seal date for packaged parts).

3.14 Destructive Physical Analysis

A sample of devices shall be evaluated by the purchaser for conformance to the requirements of internal and external materials, construction, process and workmanship as specified herein. Destructive Physical Analysis (DPA) shall be performed by the purchaser in accordance with the purchaser's practices for acceptance. Lots failing the specified criteria shall be rejected. Scanning Electron Microscope (SEM) analysis should be part of DPA.

3.14.1 Sample Size

The sample size for the DPA shall consist of a minimum of two devices from each wafer randomly selected from the quantity received from a given purchase order. Two samples selected before burn-in and three afterward are recommended.

3.15 Radiation Survivability

The manufacturer shall supply the purchaser with a sample of five devices from each wafer lot for survivability radiation test. Radiation survivability testing imposes no lot jeopardy liability on the manufacturer.

The samples shall be immediately pulled from a lot after completion of the screening sequence specified in Table II.

3.16 Workmanship

Devices shall be manufactured and processed in a careful and workmanlike manner (in accordance with good design and sound engineering practice) with the requirements of this specification and the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of a product assurance program in accordance with paragraph 4.0.

3.17 Abbreviations, Symbols and Definitions

The abbreviations, symbols and definitions used herein shall be as defined in MIL-S-19500 or as they appear.

3.18 Record-Keeping and Data

The manufacturer shall maintain complete records and data, accessible to the purchaser, for the construction and test history of each device manufactured under a given purchase order for a period of 10 years after shipment. This requirement includes substrate, die, wafer, lot, package part, matching component and combining component processing and test histories. The information should be complete enough to show device yield at each step and allow construction of identical parts in the future without having to relearn the processing techniques involved. Proprietary information must be available for examination at the vendor's facility by the purchaser.

3.19 Inspectability
Device construction shall be such as to not preclude the processes of measuring, examining, gauging or otherwise comparing the article with the requirements of this specification. This requirement is not intended to exclude the use of air bridge technology.

3.20 Incoming Inspection
The manufacturer shall perform pertinent incoming inspection, in accordance with paragraph 4.11, of each delivery lot of component parts supplied by vendors.

4. QUALITY ASSURANCE PROVISIONS

Manufacturers making devices in accordance with this document shall maintain a Quality Assurance System in accordance with MIL-M-38510, Appendix "A" (or one approved by the purchaser).

4.1 General
Devices supplied to this specification shall meet the quality assurance provisions specified herein. Unless otherwise specified the manufacturer is responsible for the performance of all inspection requirements specified herein.

4.2 Classification of Inspection
The examination and testing of devices shall be classified as follows:

a. Lot Quality Conformance

b. Screening

c. Qualification

4.3 Lot Traceability
Lot size shall be defined per paragraph 3.4 at the process wafer level.

4.4 Lot Quality Conformance
In general, these tests shall be in accordance with the conditions specified in MIL-STD-883, METHOD 5007 entitled "Wafer Lot Acceptance," except that gold backing thickness may be up to 200,000 Å and wafer thickness may be as small as 0.001 inch. In particular, each wafer lot designated for supplying devices to this specification shall meet the requirements of Table V on a sampling basis. If one or more dies from the wafer fail to meet the SEM inspection requirements specified, the wafer shall be deemed a reject. Devices shall not be fabricated from wafers failing to meet the acceptance criteria.

All data results shall be made available for review by the purchaser. In case of conflict in interpretation of the results, the purchaser reserves the right of disapproval when the review of the results indicates unacceptable material.

4.4.1 Wafer SEM Inspection
The sample die from each wafer shall be subjected to scanning electron microscope (SEM) examination in accordance with MIL-STD-883, Method 2018 (or a purchaser-approved manufacturer's SEM inspection document), as described in Table V. A minimum of five dies shall be evaluated from each wafer. The metallization shall be examined with the surface glassivation coating in place and then removed or reduced in thickness to 500 angstroms or less on the die selected for SEM. If one or more dies from the wafer fail to meet the acceptable criteria, the wafer shall be deemed a reject. The SEM inspection die shall be kept in storage under controlled conditions for 5 years by the manufacturer or purchaser at purchaser's option.

4.4.2 Electrical Parameter Evaluation
The sample of devices used in Table V in the electrical tests (Accelerated Life, Device Impedance, and Temperature Sensitivity of RF Performance) shall be selected from those successfully completing the screening indicated in Table II and shall satisfy the limits of Table I. The samples used in the Device Impedance test may be used as part of the deliverable devices or, alternatively, in the Temperature Sensitivity of RF Performance test.

4.5 Quality Conformance Inspection and Screening
In general, Quality Conformance Inspection and Screening shall be in accordance with MIL-M-38510, Para. 4.5, entitled "Quality Conformation Inspection." In particular, screening shall be performed on all devices supplied to this specification in accordance with Table II.

4.5.1 Screening Reject Criteria

4.5.1.1 Device Failure
Any device which fails screening at any point shall be deemed a reject and shall not be delivered under this specification.

4.5.1.2 Screening Lot Failure (For the purposes of this paragraph, a screening lot is defined as a group of devices undergoing burn-in simultaneously in the same burn-in facility.)
If more than 20% of the devices subjected to burn-in fail to remain within the electrical drift limits of Table III, the screening lot shall be rejected. If less than 10% fail, the lot is accepted. If more than 10% but less than 20% fail, a second burn-in may be applied. If more than 5% fail in the second burn-in, the lot is rejected. The purchaser shall be notified within 2 working days of the lot rejection, and disposition of the lot shall not occur without the concurrence of the purchaser.

4.5.2 Data Requirements
The manufacturer shall supply one reproducible copy of the variables data from pre and post burn-in electrical measurements, including deltas. A summary of the electrical requirements in Table II identifying the serial number, test, number of parts tested, number accepted and number rejected shall be provided.

4.5.3 Visual Inspection Details

4.5.3.1 Chip Visual Inspection
Chip visual inspection shall be in accordance with criteria of MIL-STD-883, Method 2010, Criteria A, or a document approved by the purchaser.

4.5.3.2 Ceramic Package Visual
The inspections described for the ceramic packages are to be performed on 100% of the parts.

4.5.3.2.1 Package Visual
In general appropriate qualification and quality conformance tests per MIL-STD-883, Method 5005, Table IV, are required. The following parts give an example of additional detail for metal-ceramic packages. A magnification of ≥30X is to be used.

a. Exterior drain and gate lead frame joint--good solder fillet around three sides and leads centered on package ± 0.005 inch.

b. Ceramic to flange heat sink--good braze fillet all around.

c. No cracks in the ceramic.

d. No cracking, blistering, or peeling of plating metallization.

e. No delamination of ceramic or laminated metal.

4.5.3.2.2 Sealing Ring Surface.

a. There shall be no edge chips greater than 10% of narrowest width.

b. Sealing surface to be free of foreign material and discolorations.

c. There shall be no scratches or voids across the sealing surface which reduce the undisturbed metal width by more than 25%, or which affect the weld area on welded packages.

d. There shall be no cracking, blistering, or peeling of sealing ring plating or metallization.

e. Any warpage, nonflatness, or nonparallelism which leaves a sealing surface distorted by greater than 0.001 inch, the bottom distorted by greater than 0.001 inch, or the top to bottom not parallel to within 0.002 inch shall be rejected.

4.5.3.2.3 Leads and Attachments for Brazed Leads (excluding tie bar)
Under ≥30X magnification, the following shall be cause for rejection:

a. Braze material of leads increasing the lead dimensions by more than 0.005 inch above the specified dimensions within a distance of 0.040 inch from the edge of the package.

b. Braze material flowing beyond 0.040 inch from the body.

c. Braze material reducing the isolation between leads, or lead to lead pad.

4.5.3.2.3.1 Lead Braze and Braze Pads
See Figure 2 for brazed lead packages.

a. There shall be no voids extending under the braze material, i.e., the braze pad shall be visible.

b. The isolation between braze pads shall be 0.010 inch minimum.

c. There shall be no bridging between braze pads.

d. The braze fillet shall satisfy the following conditions:

1. Braze Fillet Top. There shall be a braze fillet at least three quarters along each of the two sides of the lead, plus the tip. If the lead is at the edge of the braze pad there shall be braze material visible along that entire bottom edge of the lead and the braze fillet shall be present along the entire length of the lead on the opposite side and also at the tip.

2. Braze Fillet Bottom. Braze materials shall be visible at least 75% across the bottom of the lead. A braze fillet can extend no more than 0.005 inch on to the lead measured from the edge of the package.

4.5.3.2.4 Foreign Material. Magnification of 30X shall be used.
Any package having attached foreign material shall be rejected. Unattached foreign material on, or within the package may be removed with a nominal gas blow of dry nitrogen of approximately 20 psig. Any material not removed by this method is considered attached.

4.5.3.2.5 Pretinned Cover. Magnification of ≥20X shall be used.

a. There shall be no untinned areas greater than 0.005 inch diameter.

b. Wetting and solder contour shall be uniform.

c. There shall be no cracking, blistering, or peeling of the plating or metallization.

d. The tinned surface shall be free of discoloration and foreign material.

4.5.3.3 Pre-Cap Visual
All devices procured per this document shall be examined in accordance with MIL-STD-883, Method 2010, Criteria A, or by a document approved by the purchaser.

4.5.3.4 External Visual
In general, all devices procured per this document shall be examined in accordance with MIL-STD-883, Method 2009 and applicable package inspection criteria. In particular, devices shall be considered to fail if they have any of the following. Magnification of ≥30X shall be used.

a. Device design, lead identification, markings (content, placement, and legibility), materials, construction, and workmanship are not in accordance with the applicable specification.

b. Defects or damage resulting from manufacturing, handling, or testing.

c. Visible evidence of corrosion, contamination or breakage (grossly bent or broken leads, cracked seals), defective (peeling, flaking, or blistering) or damaged plating (nicks, scratches, or gouges which expose base material). (Discoloration of the finish shall not be cause for failure unless there is evidence of flaking, pitting, or corrosion).

d. Leads which are not intact and aligned in their normal location, free of sharp or unspecified lead bends, and (for ribbon leads) free of twist outside the normal lead plane as defined in the package outline drawing.

e. Leads which are not free of foreign material such as paint, other adherent deposits, or dust which cannot be removed by a purchaser-approved process.

f. Other defects or features which will interfere with the normal application of the device.

g. Evidence of any nonconformance with the detail drawing or applicable procurement document, absence of any required

feature, or evidence of damage, corrosion, or contamination which will interfere with the normal application of the device.

h. Excess solder expulsion at seal area exceeding the package dimension specification or which reduces the distance between external lead pads and sealing ring to less than 0.002 inch.

i. Solder balls.

j. Cover misalignment which causes an out-of-dimension condition, or which reduces the sealing overlap by >0.005 inch at any point.

k. Lack of complete wetting at the solder seal interface or voids in the solder greater than 0.005 inch deep.

4.5.4 Radiographic Inspection
All devices procured per this document shall be examined in accordance with MIL-STD-750, Method 2076.

4.6 Qualification Inspection
In general, Qualification Inspection shall be in accordance with MIL-M-38510, Para. 4.4. entitled "Qualification Procedures." In particular, when specified on the purchase order, a sample of devices which have successfully completed screening shall be subjected to qualification testing in accordance with the flow diagram of Figure 3 and the test procedures of Table IV. Devices completing these tests shall not be supplied as flight parts, but shall be marked with a red dot on the device package and delivered separately from flight devices.

4.6.1 Rejection Criteria
If the acceptable number of failures in the sample, as defined in Table IV, Note 1 is exceeded, the purchaser shall be notified within 2 working days of a lot rejection, and disposition of the lot by the manufacturer shall not be made without concurrence of the purchaser.

4.6.2 Operating Life (RF)
Operating Life (RF), Test Number 20 of Table IV, shall be performed by the manufacturer or by the purchaser at the purchaser's option. Operating Life (RF) shall be performed for information only. As this is for information only, Note 1 above for Table IV shall not apply.

4.7 Failure Analysis
Electrical failures which occur after the initial electrical tests shall be analyzed as necessary per MIL-STD-883, Method 5003 to determine the cause of failure. Devices failing mechanically after the initial electrical tests shall be logged by serial number, the failure mode or symptom and failure mechanism identified, and shall be saved for 10 years for possible further failure analysis. For the

purposes of this specification, electric failure is defined as the following for the various tests:

a.	Burn-in test	Opens or shorts.
b.	Post burn-in dc electrical tests	Parameter drift outside the range shown in Table III.
c.	Final electrical test, dc	Characteristics outside the limits specified.
d.	Final electrical test, RF	Characteristics outside the limits specified.
e.	Accelerated life test	Gain or output power change more than allowed in Table V.

4.8 Source Inspection

The purchaser shall have the right of access to the manufacturer's plant to perform internal visual inspection; monitor wafer acceptance, screening and qualification tests; witness final tests; and review data from process-conditioning, testing, screening, and qualification. The manufacturer shall notify the purchaser at least 5 working days prior to the start of wafer acceptance, internal visual inspections, final test, and qualification.

4.9 Test and Inspection Data

Each shipment of devices shall include a report that, as a minimum, includes the following information for qualification (if qualification is done) or developmental device shipments:

a. Certificate of conformance to the contents of this specification.

b. Type and number of parts tested.

c. Record of and number of failures and failure modes at initial electrical (except no failure analysis on devices failing the manufacturer's dc go-no go test before the initial electrical measurement), final electrical, qualification and lot quality conformance measurements.

d. Recorded values of all measured parameters, including burn-in deltas, referenced to device serial number.

e. Failure analysis report on devices failing electrically after pre-burn-in electrical test per Table II.

f. Radiographs referenced to part serial number.

g. SEM inspection results including photographs.

h. Full report of qualification including test sequence, number of parts tested, number accepted, and recorded values of measured parameter referenced to the part serial number.

For non-qualification device shipments, only items a, b, d, e, f and a statement indicating the initial number of devices in the lot plus the number of failures need be included.

4.9.1 Certification

The manufacturer shall certify that the material meets all the requirements of this specification and the purchase order. The certification shall include the following information as a minimum:

Title: Test Data for (Complete Part No.)

Purchase Orders: (Number of all applicable)

Manufacturer: (Manufacturers name and address)

Period of Test: (Dates started and dates completed)

Lot Numbers: (Wafer lot/date code)

Date: (Date of documentation formation)

Name and Signature: (Name, title and signature of the quality control manager or his designated representative)

4.10 Notification of Changes

No change shall be made to the items listed below which affect the quality, reliability and electrical interchangeability of the device without written notification and approval of the purchaser.

a. Design

b. Configuration

c. Materials

d. Manufacturer

4.11 Incoming Inspection

The manufacturer shall perform pertinent incoming inspection of vendor-supplied component parts to insure uniformity and quality of the parts. Details of the incoming inspection will be outlined in manufacturer's detailed subspecifications to this specification.

4.12 Measurements

4.12.1 Equipment Checkout
The manufacturer shall verify the measurement/operation characteristics of electrical test equipment prior to each usage, in accordance with MIL-S-19500, paragraph 4.3.1.5.

4.12.2 Equipment Calibration
The manufacturer shall establish and maintain a program for calibration, control and maintenance of measuring and test equipment in accordance with MIL-STD-750, paragraph 4.1.4.

5. PREPARATION FOR DELIVERY

5.1 Preservation - Packaging and Packing
Devices shall be prepared for delivery with preservation, packaging, and packing in accordance with MIL-S-19491. The devices shall be packaged to prevent damage during transit.

5.1.1 Package and Unit Container Marking
Marking of the package and unit container shall be in accordance with MIL-STD-129 and shall consist of the following:

a. Purchase order

b. Part number (per para. 1.2)

c. Inspection lot identification code

d. Manufacturer's name or symbol

5.1.2 Qualification Samples
Qualification test samples shall be packaged separately and in addition to the marking above, each unit container shall be clearly marked with the following as applicable:

QUALIFICATION TEST SAMPLES NOT FOR FLIGHT USE

5.2 Electrostatic and Environmental Protection
The devices shall be protected from electrostatic damage by enclosing each device in the initial wrap or bag fabricated from barrier material conforming to the requirements of MIL-S-19491. In addition, the devices shall be in contact with a conductive material which shorts all leads together to prevent

electrostatic damage. The requirements of MIL-S-19491 shall also be used to provide environmental protection to the devices.

5.2.1 Unit Container Marking

In addition to the markings of paragraphs 5.1.1 and 5.1.2, each unit container shall be marked with the following warning lettered in black or contrasting color on a red or other brightly colored background.

WARNING
STATIC ELECTRICITY MAY DAMAGE THIS PART
EXERCISE PROPER PRECAUTIONS WHEN HANDLING OR TESTING

If the device is unpackaged (i.e., a chip-carrier), a warning against opening the container outside a Class ___ clean room should also be applied to the container. A label warning against testing the devices with ohmmeters should also be applied.

Table I. Electrical Characteristics
(T_A = TBD°C ± 3°C Unless Noted)

Examination or Test	MIL-STD or Appendix	Test Conditions and Details	Symbol	Limits		Unit/Type Measurement
				Min.	Max.	
GROUP 1 - POTENTIAL LIMITS						
Area of Safe Operation Drain Voltage Verification		V_{GS} = ___V NOTE 1	$ASOV_D$			V/dc
Breakdown Voltage, Gate to Source	MIL-STD-750 Method 3401	Cond. C, I_G = ___mA V_{DS} = open NOTE 1	$V_{(BR)GSS}$			V/dc
Breakdown Voltage Gate to Drain	MIL-STD-750 Method 3401	Cond. C, I_G = ___mA V_{DS} = open NOTE 1	$V_{(BR)GDS}$			V/dc
GROUP 2 - DC CHARACTERISTICS						
Saturated Drain Current	MIL-STD-750 Method 3413	Cond. C, V_{DS} -___V, V_{GS} = 0 V, NOTE 1	I_{DSS}			A/dc
Specific Drain Current	MIL-STD-750 Method 3413	Cond. C, V_{DS} = ___V ± ___V, V_{GS} = 0 V NOTE 1	$I_{DS'}$			A/dc
Gate Reverse Current	MIL-STD-750 Method 3411	Cond. C, V_{GS} = ___V, V_{DS} = 0 V	I_{GR}			mA/dc
Pinch Off Voltage	MIL-STD-750 Method 3403	V_{DS} = ___V I_D=___mA, MAX NOTE 1	V_P			V/dc

Table I. Electrical Characteristics (Continued)

Examination or Test	MIL-STD or Appendix	Test Conditions and Details	Symbol	Limits		Unit/Type Measurement
				Min.	Max.	
Gate Forward Voltage	MIL-STD-750 Method 3411	Cond. D, I_{GF} = ___mA NOTES 1 and 3	V_{GSFO}			V/dc
Transconductance	Appendix 1	V_{DS} =___V I_{DS} =___A ΔI_{DS} =___A	G_m			mS
GROUP 3 - RF PERFORMANCE						
Output Power	Appendix 1	V_{DS} = ___V I_D = ___A MAX I_{GS} = ___mA MAX P_{IN} = ___dBm f = ___GHz NOTE 2	P_{OUT}			dBm/RF
Power-added Efficiency	Appendix 1	$\frac{100(P_{OUT} - P_{IN})}{P_{dc}}$ NOTE 2	η_{PA}			%/RF
Frequency Limitation						
Bandwidth	Appendix 1	NOTE 4	BW			%/RF
Maximum Operating Frequency		NOTE 5	f_{MAX}			GHz/RF
Spurious Output Power	Note 6	V_{DS} = ___V I_D = ___A P_{IN} = 0 to ___dB	P_{SP}			dBm/RF

Table I. Electrical Characteristics (Continued)

Examination or Test	MIL-STD or Appendix	Test Conditions and Details	Symbol	Limits		Unit/Type Measurement
				Min.	Max.	
GROUP 4 - GATE QUALITY TESTS						
High Temperature Operation: Gate Reverse Current	MIL-STD-750 Method 3411	Cond. D, V_{GS} = ___ V V_{DS} = 0 V, T_A = 150°C NOTE 1	I_{GR}			ma/dc
Low Temperature Operation: Gate Forward Voltage	MIL-STD-750 See Note 3	Cond. D, I_{GF} = ___mA T_A = -55° C NOTES 1 and 3	V_{GF}			V/dc

NOTES to Table I

1. Test technique to be used must be approved by purchaser.
2. Measurements to be accomplished using a test fixture furnished by the purchaser or meeting the criteria given in Appendix 1 at purchaser's option. The efficiency η_{PA} is calculated from data taken from the operating point used to satisfy the P_{OUT} requirement.
3. V_{GF} is not specified in MIL-STD-750. The test is similar to method 3411 except for bias voltage polarity.
4. This measurement is made when testing a part which has a bandwidth limiting feature such as internal matching or combining circuitry. The measurement is made in the equipment described in Appendix 1 by tuning the frequency after the optimum performance point is found. The bandwidth is found as the difference between the frequencies on either side of the primary frequency where the output power is reduced by 1 dB divided by the primary frequency and then multiplied by 100.
5. This is the frequency at which zero dB gain as an amplifier or zero output power as an oscillator is available. It will be measured in a circuit approved by the purchaser for those devices where a bandwidth measurement is not appropriate.
6. This test is to be made in a circuit approved by the purchaser. The spurious output power, P_{SP}, is to be measured with the same V_{DS} and I_D as used to obtain P_{OUT}. Spurious output is defined as the sum of any nonharmonic components.

Table II. Screening Sequence

Test No.	Test	Specification (Note 9)	Test Condition and Details	Acceptance Criteria	Source Inspection
	Visual				
1	Chip	MIL-STD 883	Criteria A. Method 2010.4	Per 4.5.3.1	Yes
2	Package	MIL-STD 883 Method 5005.6	Table IV. Also per paragraph 4.5 herein	Per 4.5.3.2	Yes
3	Serial-ization and Marking		Paragraphs 3.12 and 3.13 herein		
4	IR Scan (Pre-Cap)		NOTE 8	$\leq$ 5°C Variation	Audit
5	Thermal Resistance	NOTE 7	NOTE 7	Per 1.3	Audit
6	Pre-Cap	MIL-STD 883 Method 2010.4	Criteria A. Also per paragraph 4.5 herein	Per 4.5.3.3	Yes
7	Voltage Screen		NOTE 3		Audit
8	High Tem-perature Storage	MIL-STD 883 Method 1008	T_A = 150°C, t = 48 hrs. Min., NOTE 6		
9	Temper-ature Cycling	MIL-STD 883 Method 1010	Condition D NOTE 6		Audit
10	Acceler-ation	MIL-STD 883 Method 2001.2	Condition D 20,000G,Y1 Plane NOTE 6		Audit
11	Mechan-ical Shock	MIL-STD 883 Method 2002.2	Condition B 1,500G, Y1 Plane NOTE 6		Audit

Table II. Screening Sequence (Continued)

Test No.	Test	Specification (Note 9)	Test Condition and Details	Acceptance Criteria	Source Inspection
12	PIND (Packaged Devices)	MIL-STD 883 Method 2020	Per MIL-STD-883 Condition B, NOTE 10	Per MIL-STD-883	Audit
13	High and Low Temp. Electrical		Per Table I, Group 4. NOTE 2	Per Table I, Group 4. NOTE 2	Audit
14	Pre Burn-In Electrical		Per Table I, Groups 1, 2, 3	Per Table I, Groups 1, 2, 3	Audit
15	Operating Burn-In		The operating burn-in shall be performed in a manner which allows λ_E to be determined. If $\lambda_E > 10^{-7}(HRS)^{-1} - \lambda_{EFF}$ at $T_{CH} = 125°C$, the lot shall be rejected or the burn-in continued. NOTE 5		
16	Post Burn-In Electrical		Per Table I, Groups 1, 2, 3	Apply PDA criteria of para. 4.5.1.2 to Group 2	Audit
17	Drift Limits			Per Table III	Audit
18	Hermetic Seal (Packaged Devices: Fine Leak)	MIL-STD 883 Method 1014	Per MIL-STD-883 NOTE 11	1×10^{-8} atm cc/sec MAX.	Yes
19	Hermetic Seal (Packaged Devices; Gross Leak)	MIL-STD 883 Method 1014	Per MIL-STD-883 Condition C, NOTE 11	Per MIL-STD-883	Yes

Table II. Screening Sequence (Continued)

Test No.	Test	Specification (Note 9)	Test Condition and Details	Acceptance Criteria	Source Inspection
20	Radio-graphic Inspection	MIL-STD 750 Method 2076	Two Views, X_2 and Z_2, NOTE 1, NOTE 11	Per MIL-STD-750	Audit
21	Final Electrical		Per Table I, Groups 1, 2 and 3, NOTE 11	Per Table I, Groups 1, 2 and 3	Yes
22	Final Visual	MIL-STD 883 Method 2009.2		NOTE 4	Yes

NOTES to Table II

1. The screening sequence of sealed devices may be adjusted to the manufacturer's standard flow except that hermetic seal and radiographic inspection shall occur after thermal, mechanical and burn-in stresses are completed.

2. A sample of 10% of the lot or 10 samples, whichever is greater, shall be subjected to the high and low temperature measurements listed in Table I and the limits quoted applied. If one or more devices exceeds the limits of Table I, the lot shall be 100% tested and any part not meeting the limits shall be rejected and eliminated from the lot.

3. All devices shall be subjected to the following drain voltage test at T_A = 25°C. Nonconforming devices shall be rejected and eliminated from the lot. The purpose of this screen is to remove those devices having insufficient drain to source breakdown capability. Test level to be recommended by the manufacturer and approved by purchaser.

Test	Conditions	Limits Min.	Limits Max.	Units
Drain Volts	V_{GS} - - ___V	_____	_____	V

4. In addition to the workmanship criteria denoted in the referenced specification, the physical dimensions shall be checked on all devices and shall conform to Figure 1 herein.

5. λ_E is the post burn-in early failure rate. The effective main population failure rate λ_{EFF} shall be determined from the biased accelerated life test (Table IV, Test 16). RF burn-in is suggested.

6. Chip-carriers shall be mounted in a suitable enclosure approved by the purchaser for this test.

Table II. Screening Sequence (Continued)

7. This test may be sequenced between Test No. 15 and 19 if desired. Measurement of the thermal resistance is dependent upon an accurate measurement of channel temperature. Channel temperature (T_{CH}) shall be measured accurately to within 3% of the difference between the channel temperature and the transistor base (ambient) temperature (T_A), e.g., if $T_{CH} - T_A = 100°C$, then the accuracy with which T_{CH} must be measured is $\pm$ 3°C. The transistor base temperature shall be held constant within $\pm$ 1°C during the measurement. The hottest channel shall be used for the measurement of thermal resistance. The technique used for channel temperature measurements can be electrical, as in MIL-STD-750, Method 3151, but the use of liquid crystal, infrared microscope, or other techniques are not prohibited if the measurement accuracy condition is met. To combine accuracy with ease of measurement, a combination of techniques may be used if the measurement accuracy can be maintained. Data must exist to show that the thermal resistance is not changed by subsequent processing after the measurement.

8. This measurement is made with an infrared microscope with resolution $\leq$ 35 micrometers. Locate the hottest channel and spot on the channel. Then, adjust the temperature of the hot spot to 100°C $\pm$ 5°C with the device biased to its maximum allowable drain power ratings. Then, holding the hot spot temperature constant, scan across the chip in the X and Y directions to find the coldest channel and spot. If the FET has a non-constant temperature profile by design, then the manufacturer shall provide that profile and the variation indicated in the table is about the design delta for the FET (e.g., if the FET is designed to have a 10° change in temperature across the chip, the variation in temperature must then be between 5°C and 15°C). Measurement accuracy for the difference in temperature between the hottest and coldest spots shall be $\pm$ 2°C. MESFET designs with structures, such as air bridges, which interfere with the temperature measurement may use an alternate acceptance criteria subject to approval by both purchaser and manufacturer.

9. A purchaser-approved document may also be used.

10. Test No. 15 may be sequenced any time after Test No. 7.

11. Tests numbers 16 thru 19 may be in any sequence as long as Test No. 16 is before Test No. 17.

Table III. Electrical Drift Requirements
(T_A = TBD°C ±3°C)

Examination or Test	Symbol	Limit	Unit	Reference Point
Specific Drain Current	$\Delta I_{DS'}$	± 15	%	Initial Value
Gate Reverse Current	ΔI_{GS}	3μA or 100% whichever is greater	μAdc or %	Initial Value
Pinch Off Voltage	ΔV_P	± 15	%	Initial Value
Gate Forward Voltage	ΔV_{GF}	± 15	%	Initial Value
Saturated Drain Current	ΔI_{DSS}	± 15	%	Initial Value
Output Power	ΔP_{OUT}	± 0.5	dB	Initial Value
Transconductance	ΔG_m	± 10	%	Initial Value

Table IV. Qualification Inspection

Test No.	Test	MIL-STD	Method	Details (NOTE 1)	Notes
	Subgroup 1 (12 samples)				
1	Shock	883	2002	Condition C, Y_1 Orientation	8
2	Vibration, Variable Frequency	883	2007	Condition A	8
3	Constant Acceleration	883	2001	Condition E, Y_1 Orientation	8
4	Seal				
	Fine Leak	883	1014	1×10^{-8} atm cc/sec, max.	9, 12
	Gross Leak	883	1014	Condition C	9, 12
5	Electrical Measurements			Measurements and Limits of Table I, Group 1, 2 and 3	
6	Visual Examination			Per 4.5.3.4 herein	3
	Subgroup 2 (12 samples)				
7	Solderability	750	2026	Gate and drain contacts	
8	Soldering Heat	750	2031	1 cycle	
9	Thermal Shock	883	1011	Condition D	8
10	Seal			Same as Test 4	9, 12
11	Electrical Measurements			Same as Test 5	
12	Visual Examination			Same as Test 6	3
	Subgroup 3 (5 samples)				
13	Terminal Strength	750	2036	Condition E	4,9
	Subgroup 4 (11 samples)				
14	Operating Life (DC or RF)	750	1026	T_{CH} = 175°C. V_{DS} = ___V	2,8

Table IV. Qualification Inspection (Continued)

Test No.	Test	MIL-STD	Method	Details (NOTE 1)	Notes
15	Visual Examination			Same as Test 6	3,5
	Subgroup 5	750			
16	Biased Accelerated Life			The stress potential and current shall conform to Table I, Group 3. The maximum temperature shall result in a median failure time of >100 HRS.	8, 10, 11
17	Determination of Main Population Failure Rate (λ_{EFF})			The student - t analysis shall be used to determine the λ_{EFF}. The lot shall be rejected if, at T_{CH} = 125°C, $\lambda_{EFF} > 10^{-7}(HRS)^{-1} - \lambda_E$	
	Subgroup 6	750			
18	Unbiased Accelerated Life			The maximum temperature shall result in a median failure time of >100 HRS.	8, 10, 11
19	Determination of Main Population Failure Rate (λ_{EFF})			The student - t analysis shall be used to determine the λ_{EFF}. The lot shall be rejected if, at T_{CH} = 125°C, $\lambda_{EFF} > 10^{-7}(HRS)^{-1} - \lambda_E$	
	Subgroup 7 (20 samples)	750	1026		
20	Operating Life (RF)			T_{CH} = 125°C, V_{DS} = ___Vdc, f = ___ GHz	6,7,8
21	Electrical Measurements			Measurements and Limits of Table I, Groups 1, 2, 3 and 4	

Table IV. Qualification Inspection (Continued)

NOTES to Table IV

1. The number of failures allowed is 3 to be dispersed as 1 from Subgroup 1, 1 from Group 2, 0 from Subgroup 3. The failures from Subgroup 4 shall be consistent with $\lambda_{EFF} + \lambda_E \leq 10^{-7}(HRS)^{-1}$.

2. The duration of the test shall be 2000 hours. The measurement of Table I Groups 1 and 2 shall be recorded and the limits quoted applied at 0 and 1000 ± 48 hours. The measurements of Table I Groups 1, 2, 3 and 4 shall be recorded and the limits quoted applied at 2000 ± 48 hours.

3. The external markings of the part shall be clearly legible and correct.

4. Electrical rejects may be used.

5. Damage done to leads from test fixturing and/or handling shall not be considered as failures.

6. Surviving devices from Subgroups 1 and 2 may be used in Subgroup 5 at the discretion of the purchaser.

7. The duration of the test shall be 10,000 hours and is for information purposes only. The measurements listed in Test No. 21 shall be recorded at 0, 500 ± 48 hrs., 1,000 ± 48 hrs, 5,000 ± 48 hrs, and 10,000 ± 48 hrs. As this is for information only, Note 1 above will not apply.

8. Chip-carriers shall be mounted in a suitable enclosure approved by the purchaser for this test.

9. This test not applicable to chip-carrier devices.

10. The following details apply for the accelerated life tests:

    a. One device from each test group (Biased Accelerated Life and Unbiased Accelerated Life) shall be selected as a control.

    b. The control specimen shall be measured electrically at room ambient conditions at the same time as for the stressed devices, but it shall not be subjected to the stress tests.

    c. The Table I, T_A = 25°C, electrical parameters, I_D, I_{DSS}, V_p, V_{GF}, P_{OUT}, shall be measured and recorded.

    d. The above electrical parameters (item c.) shall be remeasured at appropriately selected time intervals until 50 percent of the devices fail to meet C) above electrical parameters including the Delta Criteria; ΔP_{OUT} = ± 1 dB (Delta limit is maximum allowable).

       Note: a plot of cumulative percent failures versus time to failure may be used to interpolate the 50 percentile point for the lower stress tests. The maximum test time for stress testing shall be 5000 hours.

    e. Devices failing short, open, or inoperative shall be failure analyzed to the extent necessary to insure understanding of the failure mode and cause.

Table IV. Qualification Inspection (Continued)

11. The number of samples to be used shall be approved by the purchaser.
12. A document approved by the purchaser may be used instead of MIL-STD-883.

Table V. Lot Quality Conformance

Test	Specification	Method	Test Condition	Special Selection Criteria	Failure Criteria
SEM*	MIL-STD-883 NOTE 1, 10	2018		Five Die per wafer per 2018	NOTE 1
Wire Bond Pull Strength*	MIL-STD-1547 NOTE 2	Section 1400 Para-graph 4.1.3		Five bonds, of each type** per assembly lot before and after each bonding session	
Die Bond Shear	MIL-STD-883	2011 or 2019 NOTE 3		Five die per assembly lot before and after each bonding session	Per method 2011 or 2019
Package Lead Integrity	MIL-STD-883 NOTE 4	2004	A and B_2 except 2 arcs instead of 3	Ten bonds per assembly lot ***	Lead Break
Accelerated Life		Per burn-in condi-tions	200 hrs. RF test at 100 hours	2 devices per 10 devices per delivery lot. Channel temper-ature shall be 225°C	1 dB per Table I, 50% failures at 200 hrs
Thermal Shock	MIL-STD-883	1011	C, NOTE 7	Five devices per assembly lot.	NOTE 8
Seal Fine Leak	MIL-STD-883 NOTE 10	1014		Use device from thermal shock test	1×10^{-8} atm cc/sec, MAX
Gross Leak	MIL-STD-883 NOTE 10	1014	C	Use devices from thermal shock test	Per MIL-STD-883
Electrical Measurements		Per Table I Groups 1, 2 and 3		Use devices from thermal shock test 2 and 3	Per Table I Groups 1, 2 and 3

Table V. Lot Quality Conformance (Continued)

Test	Specification	Method	Test Condition	Special Selection Criteria	Failure Criteria
Visual Examination		Per 4.5.3.4 herein		Use devices from thermal shock test	Para. 4.5.3.4 herein
Package Lead Peel Test		NOTE 9		Two packages per assembly lot (may be packages from other tests if leads are undamaged)	NOTE 9
Package Lead Plating Integrity	MIL-G-45204			Five packages per assembly lot.** Bend leads per 45204	
Package (or Chip-Carrier) Plating Integrity			Bake samples at 350°C ± 5°C for 5 min. ± 15 sec	Five packages per assembly lot.** Conduct visual inspection using 30X microscope. Also perform tape test on plating.	Lifting, blistering or peeling of plating, or formation of a whitish or crystalline film or stains or discoloration on plating which cannot be removed by ultrasonic cleaning in Freon
Package Internal Water Vapor Content	MIL-STD-883	1018 except failure		Two packages per sealing lot	>1000 parts per million criteria
Moisture Resistance	MIL-STD-883	1004	End points per Table I, Group 2.	Five devices per assembly lot	Method 1004

Table V. Lot Quality Conformance (Continued)

Test	Specification	Method	Test Condition	Special Selection Criteria	Failure Criteria
Temperature Sensitivity of RF Performance			Per Table I, Group 3 P_{OUT} and η_{PA}	Five devices per wafer. Test temperatures to be 0°C and 50°C at base of package	>15% change in P_{OUT} >10% change in η_{PA} per Table I, Group 3
Device Impedance	NOTE 5	NOTE 5	Device base temperature at 25°C ± 3°C	Five devices per wafer	
DPA	MIL-STD-1547		Per 1547	Two devices per assembly lot NOTE 6	
Normal Operating Life		Per Table I, Group 3 conditions	1000 hrs RF Life Test. Test per Table I, Group 3 at 100, 500 and 1000 hrs	Ten devices per assembly lot	Change in $P_{OUT} \geq 0.3$dB per Table I, Group 3

* Purchaser will audit these tests.
** Mechanical samples from the same wafer and process lot may be substituted for electrically good die.
*** This test may be accomplished at the package lot assembly level prior to die bonding.

Table V. Lot Quality Conformance (Continued)

NOTES to Table V

1. Use MIL-STD-883 except for failure criteria. These are:

   a. Resist over an active area.

   b. Metal cracking, peeling or lifting anywhere in the active area.

   c. Nodules in the metallization greater than 10 microns.

   d. Extraneous metal within 0.001 inch of an active area or in a region of interference with other processing steps.

   e. Severed metallization that reduces metal cross-sectional area by more than 25%.

   f. Pits, perforations (metal holes that expose underlying material), and narrowing that reduce the metal cross-sectional area by 25% or more anywhere in the active areas. No more than ten such defects (pits, perforations or narrowing) that reduce cross-sectional area less than the prescribed limits are acceptable in any one active area.

   g. Unintentional metal undercutting that reduces metal cross-sectional area by 25% or more.

   h. Any extension of metal fingers or other metal boundaries that reduces the design width of separation between conducting paths or junctions by more than 50%.

   Any of the above conditions are cause for rejecting the sample and its wafer or processing lot. Samples that have one or more of the above defects due to accidental mechanical damage during sample preparation may be replaced by a sample from an adjacent position on the wafer.

2. Special configurations may require other specifications and procedures for this test. This test applies to matching or combining component wires as well.

3. Use METHOD 2011, Test Condition F for Flip-chip FET construction; otherwise use METHOD 2019. Test applies to matching and combining substrates and lumped element die as well as FET chip.

4. Brazed-on ribbon leads shall pass a 90° peel test of 1.5 lb.

5. The impedance presented by the test circuit to the device to achieve optimum performance is an important parameter. Uniformity of this impedance from device to device is a desirable goal. The procedure for the measurement is as follows:

   a. Tune device for optimum performance per Table I, Group 3.

   b. Remove test fixture and measure impedance being presented by the input (gate) and output (drain) tuners to the test fixture.

   c. The impedance presented to the gate and drain terminals of the device are then obtained by de-imbeding, i.e., adding the known perturbations of the input and output lines of the test fixture to the measured impedance. The de-imbeding process proposed to be used by the manufacturer shall be presented to the purchaser for approval before use.

Table V. Lot Quality Conformance (Continued)

d. The impedances for the gate and drain shall be presented as magnitudes and phases.

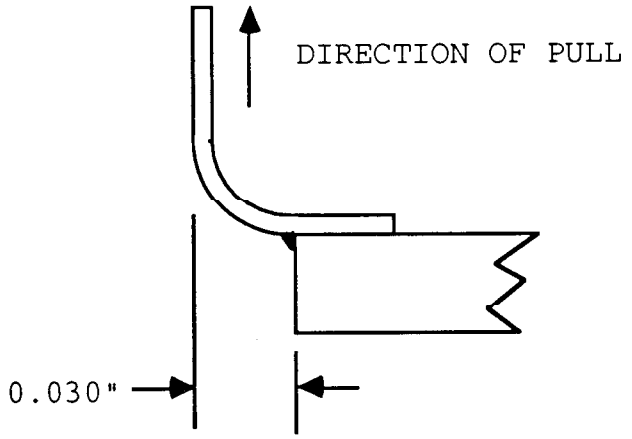
6. The two devices are to be selected from those having successfully passed the screening of Table II through the radiographic examination. The DPA may be performed by the manufacturer or the purchaser at the purchaser's option. The failure criteria is any non-conformance to the requirements that the purchaser (after discussions including the manufacturer) deems unsatisfactory from a quality control or device reliability standpoint. If the defect is process related, the device's assembly lot and all other lots using the suspect process are rejected.

7. Chip-carrier devices shall be mounted in a suitable enclosure approved by the purchaser for this test.

8. The devices shall pass hermetic seal (for packaged devices only), electrical and visual tests after thermal shock.

9. External package brazed lead peel test shall be performed on package braze joints which have passed visual inspection.

a. Bend package lead up 90^0 (as shown in the figure) at a point 0.030 inch from the package body. Clamp the lead during the bending operation to prevent stressing the braze joint.



b. Place the package in a pull tester taking care not to damage the lead or bond. Set the tester to pull at a rate no greater than 5 inches per minute.

Table V. Lot Quality Conformance (Continued)

c. Perform the peel test and record the failure strength and failure mode.

1. Acceptance pull values.
   Ribbon leads of cross-sectional area 0.006 inch x 0.020 inch or less - 1.5 pounds minimum.
   Ribbon leads of cross-sectional area greater than 0.006 inch x 0.020 inch. - 3.0 pounds minimum.

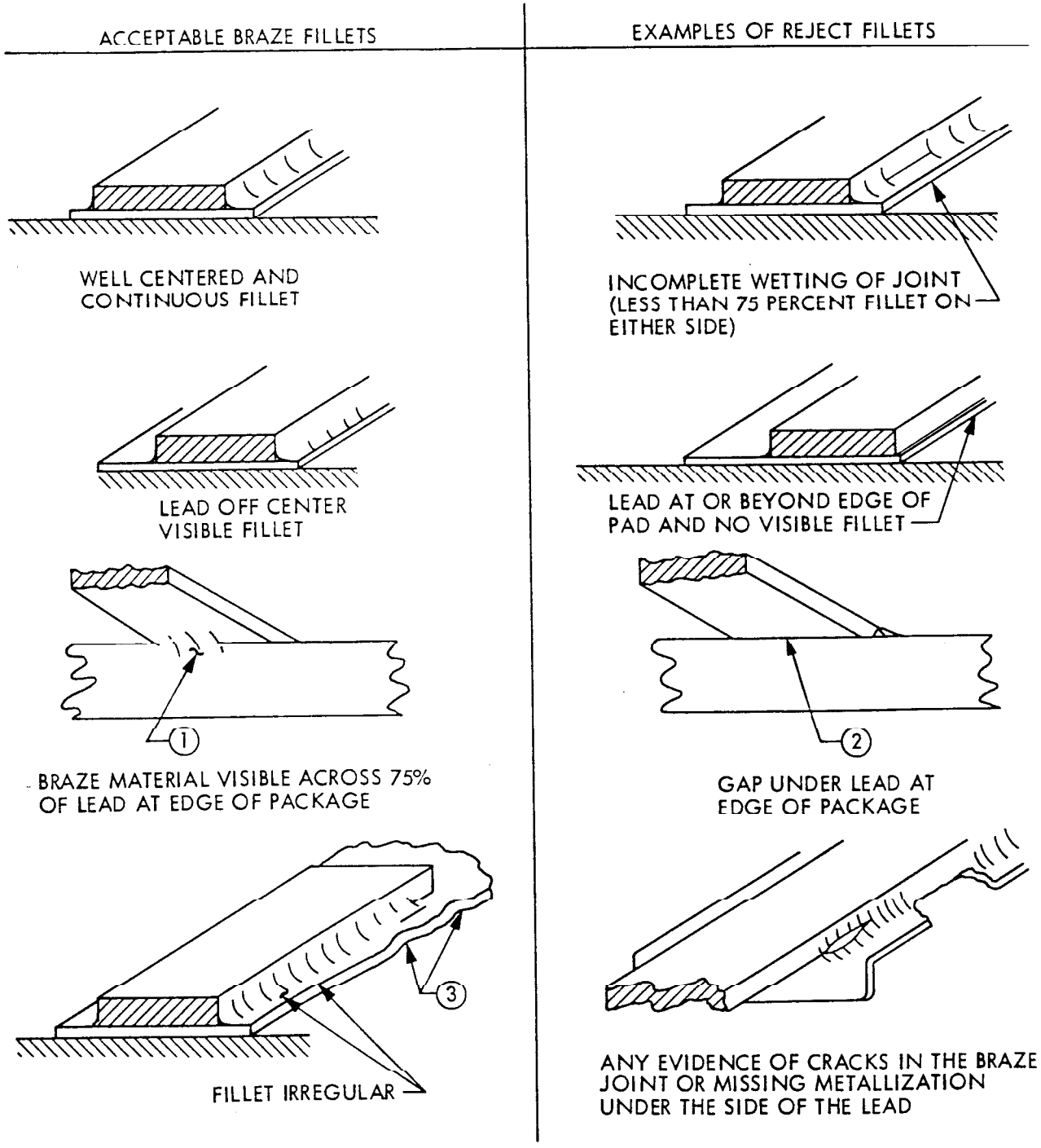
2. Failure mode classification
   Lead to braze material
   In braze material
   Braze to metallization
   Metallization to substrate
   In metallization

3) Retain the test specimens in a marked envelope and include with the test record. Mark the envelope with the package, part number, lot number, and date.

10. A purchaser-approved document may be used instead of MIL-STD-883.

TO BE SUPPLIED IN THE DETAILED SUBSPECIFICATION

FIGURE 1. Package Outline and Terminal Connections



(1) FULL FLOW OF BRAZE MATERIAL BETWEEN SURFACE

(2) SURFACES WET BY BRAZE MATERIAL BUT BRAZE MATERIAL HAS NOT FLOWED INTO THE INTERSECTION OF THE SURFACES

(3) VOID IN METALLIZATION DOES NOT EXTEND BENEATH THE BRAZE FILLET

FIGURE 2. Lead Braze Attachment

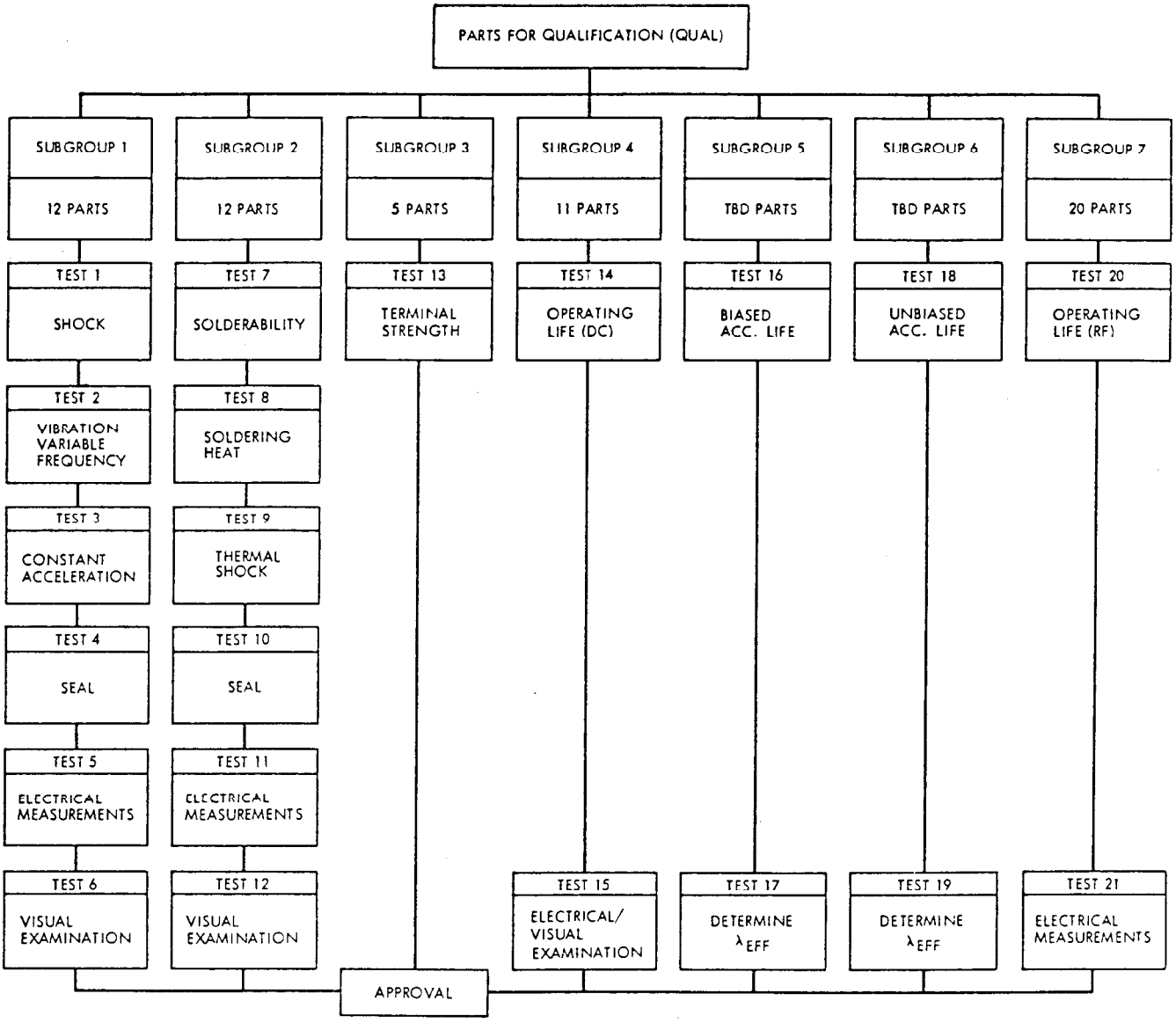


FIGURE 3. Qualification Flow Diagram

The numbers of parts for the Accelerated Life Tests are to be determined or approved by the purchaser.

APPENDIX 1

10. TEST PROCEDURE FOR RF POWER, GAIN, EFFICIENCY AND IMPEDANCE

11. SCOPE

This test specification defines requirements and procedures for measurement of input impedance, power added efficiency, output power (RF) and gain for power GaAs field effect transistors (GaAs FETs). This specification is a supplement to the requirements of the generic specification; if a conflict exists, those specifications shall govern.

12. PERFORMANCE TESTING

All devices submitted for final RF testing shall be measured in a system described in paragraph 12.1, and performance data shall be recorded as defined in paragraph 12.4.

12.1 Measurement System

A block diagram of the test set for GaAs FET performance measurements is shown in Figure A-1. The defined test equipment enclosed within the dashed lines are required. All other equipment except the power meter indicated are only recommended and equivalent types may be substituted.

12.1.1 Power Added Efficiency Calculations

Device η_{PA} shall be calculated from the following expression:

$$\eta_{PA} = 100 \frac{P_{OUT} - P_{IN}}{P_{dc}} \text{ percent}$$

where P_{dc} is the dc bias power (normally the drain power since gate power is usually negligible) and P_{OUT} and P_{IN} are RF output and input levels, respectively, as measured at the test fixture connector interfaces.

12.1.2 Gain Calculation

Device gain in dB is calculated as the difference between output and input power when both are expressed in dBm.

12.1.3 System Calibration

All input and output power levels shall be referred to the connectors on the test fixture. The losses associated with the input and output tuners may be determined as follows:

a. For each GaAs FET type, insert a device as close as possible to the input side of the device recess in the test fixture, insert in test system, and tune for maximum efficiency as in 12.2.

b. Replace the test fixture with an SMA F-F adapter.

c. Tune only the output tuner to match out the input tuner effect (a conjugate match condition).

d. Measure the insertion loss of the two tuners and adapter; divide the total loss by two and record as the input tuner loss.

e. Repeat a. and b.

f. Tune only the input tuner to match out the output tuner effect.

g. Divide the total loss by two and record as the output tuner loss.

h. Steps a. to g. are to be done for five devices of a given device type and the results averaged to provide the calibration losses.

i. Steps a. to h. are to be done separately for each device type.

12.1.4 Test Fixture

The test fixture used shall be based on that shown in Figure A-2. Glass-reinforced PTFE laminate (or alumina) microstrip with 50 ohm lines to the device and OSM or SMA launchers to the microstrip are used. No tuning is permitted inside the fixture. A machined dielectric part (e.g., Teflon or Rexolite) is used to hold down packaged parts on the fixture heat sink and also to hold the device beam leads in contact with the microstrip. The package or carrier can also be held down by screws when screw holes are provided. Chip carrier packages are also held down on the fixture heat sink by a dielectric part. In addition, however, metallic strips on the dielectric make contact between the 50 ohm microstrip line and the chip gate and drain terminals. In design of the fixture, the fixture temperature of 50°C ± 3°C typically required should be kept in mind so adequate allowance for temperature control in the design is made. Also, adequate shielding must be furnished to protect the operator from hazardous microwave radiation which can be generated in this type of fixture by GaAs FETs with more than 1 W output power. An aluminium cover for the device/microstrip area with a microwave absorber inside can provide adequate protection if properly designed.

At the purchaser's option the fixture may be furnished to the manufacturer or made by them. If the manufacturer produces the fixture, its design must be submitted to the purchaser for approval and an identical fixture supplied to the purchaser.

12.2 Test Procedure

The procedure for final RF testing of GaAs FET devices given below is not a requirement, step e. excepted, but is the recommended procedure and may be used as a guide. The device is to be installed as close as possible to the input side of the device recess in the test fixture for these measurements.

a. Turn on sequence:

1. Turn on gate supply to ≈ -3.5 V and vary slightly while observing a change of input impedance or reflected power to assure gate is connected.

2. Turn on drain supply and set to the specified potential.

3. Increase P_{IN} to desired level (from a level of at least 20 dB below the rated level).

b. Adjust output tuner for maximum output power.

c. Adjust input tuner for minimum reflection.

d. Adjust P_{IN}, V_{GS}, and input and output tuning to achieve maximum efficiency while achieving P_{OUT} and keeping I_{GS} within its limits.

e. Record data per 12.3

NOTE: Several output tuner modes may give maximum P_{OUT} while only one mode results in a maximum η_{PA}.

12.3 Impedance Measurement

The input impedance for all devices submitted for acceptance shall be referred to the gate lead to microstrip interface (see Figure A-2). A shorted package shall be used in the test fixture to establish the reference plane extension during impedance measurement system calibration. The devices or the shorted package are to be installed as close as possible to the input side of the device recess in the device test fixture for all calibrations or measurements.

12.3.1 Input Power and Impedance Calibration

The input power shall be the same as that required by paragraph 12.2. Calibration of the input tuner and polar display shall be accomplished by the following procedure:

a. Disconnect input tuner from device test fixture.

b. Connect a precision load to output of input tuner and adjust tuner for $\rho \leq 0.025$ as displayed on polar display. Note that more than one minimum tuning point may be obtained. It is

recommended that the tuning point nearest the load be chosen. Record the two calibration points as indicated on the tuner vernier scales, e.g. 1.06 and 4.34.

c. Disconnect 50 ohm load from tuner and reconnect device test fixture to tuner.

d. Insert the shorted package in the device test fixture.

e. Adjust NETWORK ANALYZER, REFLECTION TEST UNIT, and POLAR DISPLAY for the proper display shorting condition ($\rho = 1.0 \angle 180^{o}$).

f. Remove the shorted package from the device test fixture.

g. Test system is now calibrated for direct impedance measurements.

12.3.2 Test Procedure

This procedure is required for measurement of device input impedance using calibration data obtained in paragraph 12.3.1. The sequence is as follows:

a. Perform RF test procedure as required by paragraph 12.2.

b. Adjust input tuner to the calibration points obtained in paragraph 12.3.1b.

c. Read polar display impedance data and record per 12.4.

12.4 Data Recording

Test data shall be recorded on a separate data sheet for each type of device. Performance data shall be recorded for all devices including those not meeting the acceptance requirements. A sample data sheet is given in Table A-1. The quantity I_{DSWD} is the drain current measured after the optimum performance point is found by reducing the input drive level by 20 dB.

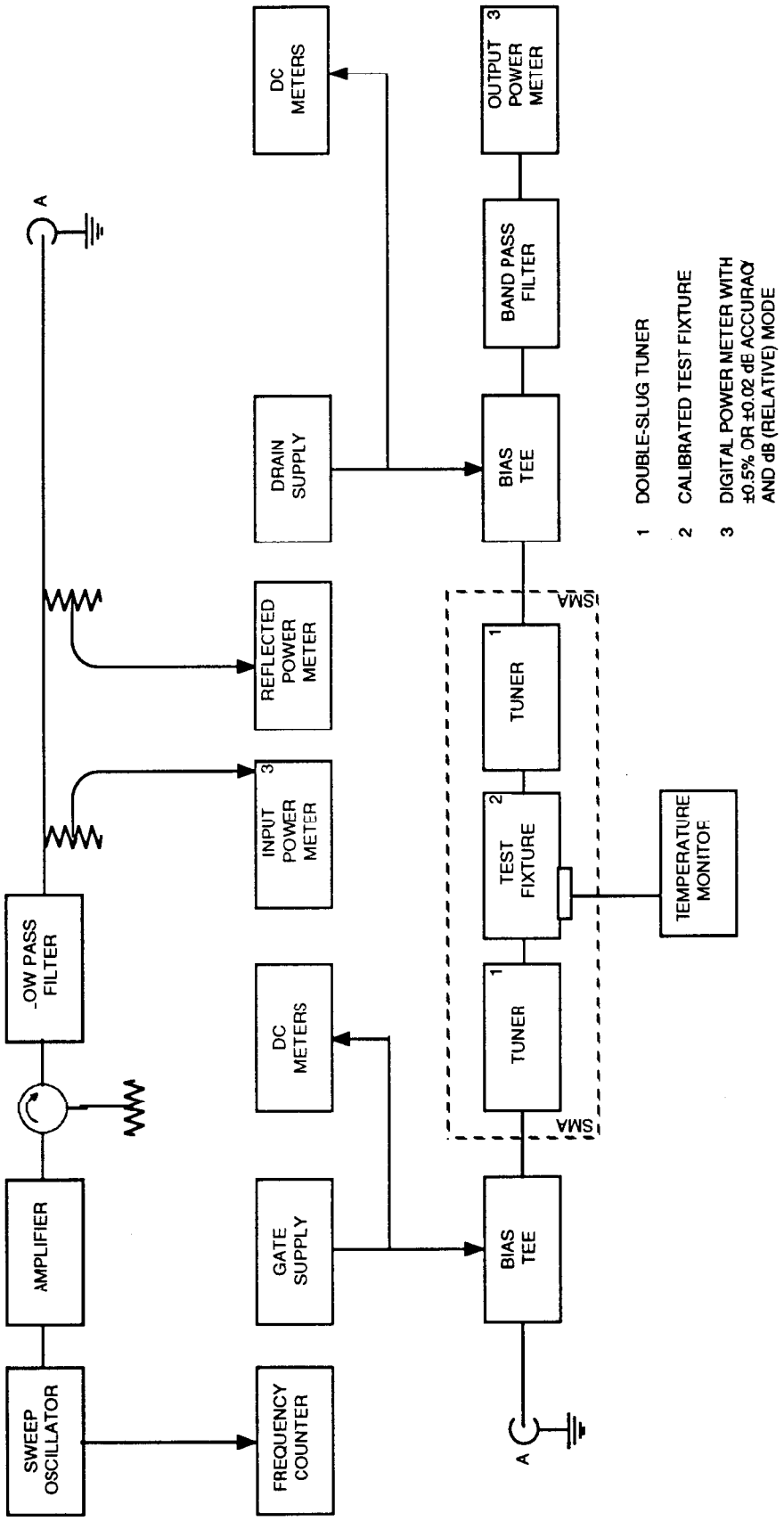
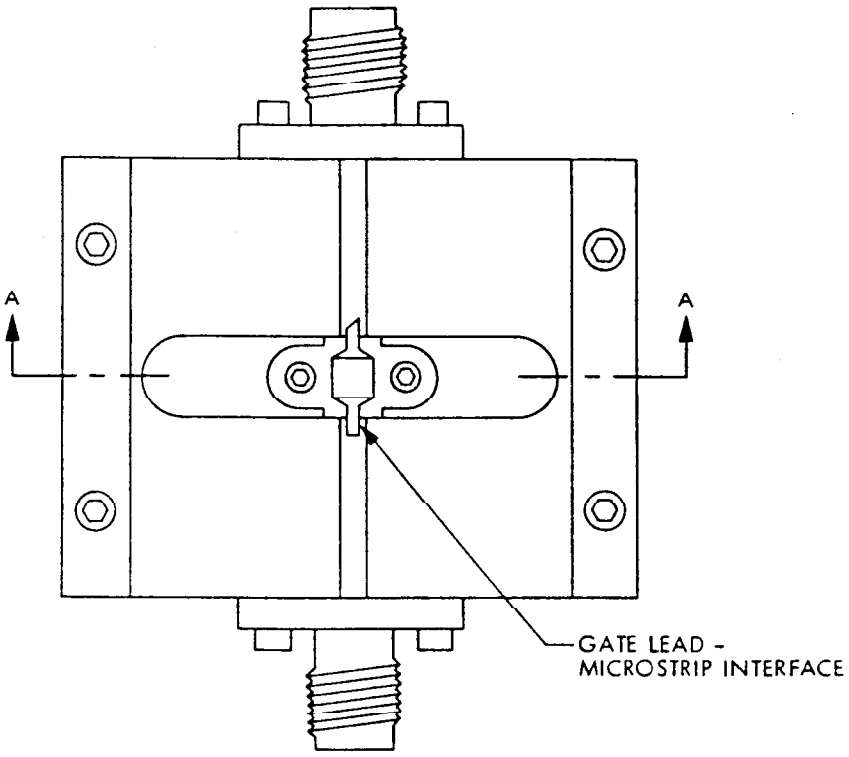
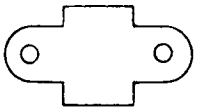


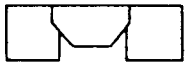
FIGURE A-1 Test Circuit



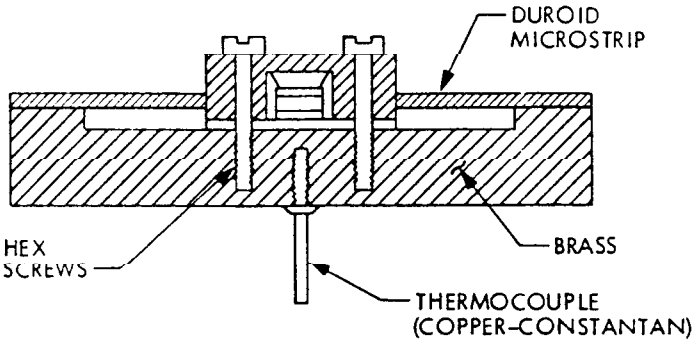
a) TOP VIEW OF FIXTURE



b) TOP VIEW OF HOLD DOWN



c) SIDE VIEW OF HOLD DOWN



d) SECTION A-A OF FIXTURE
WITH HOLD DOWN

FIGURE A-2 Test Fixture for GaAs FETs

TABLE A-1 Data Table Format

FET TYPE: _____ DATE: _____

LOT - WAFER #: _____ TEST BY: _____

η_{PA} REQUIREMENT: _____ %

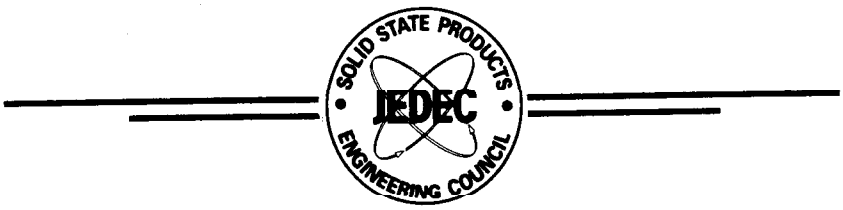
FREQUENCY: _____ MHz

V_{DS}: _____ Volts

P_{IN}: ± _____ dBm; INPUT LOSS CORRECTION USED = _____ dB

P_{OUT} REQUIREMENT: ± _____ dBm; OUTPUT LOSS CORRECTION USED = _____ dB

DEVICE SERIAL NUM.	I_{DS} (mA)	$-V_{GS}$ (VOLTS)	I_G (mA)	P_{OUT} (dBm)	V_P (VOLTS)	I_{DSS} (mA)	FIXTURE TEMP. (°C)	η_{PA} (%)	I_{DSWD} (mA)	INPUT IMPEDENCE (OHMS)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